REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 21-11-17	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** JAMES R. ESCHMEYER	TITLE MICROCIRCUIT, LINEAR, 40 V, 2.1 A, LOW DROPOUT ADJUSTABLE LINEAR REGULATOR, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/22602**
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AMSC N/A

5962-V005-22

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 40 V, 2.1 A, low dropout adjustable linear regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/22602	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	LT3086-EP	40 V, 2.1 A low dropout adjustable linear regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	See figure 1	Plastic thin shrink small outline package (TSSOP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

IN pin voltage	±45 V
OUT pin voltage	±36 V
Input to output differential voltage	±45 V 2/
SET pin voltage	36 V
$\overline{\text{SHUTDOWN}}$ ($\overline{\text{SHDN}}$) pin voltage	±45 V
CDC pin (internally clamped, current into pin)	< 8 mA
I_{MON} pin voltage	7 V
I_{LIM} pin voltage	2 V
TRACK pin voltage	Internally clamped at 1.25 V
TEMP pin voltage	0 V, 5 V
PWRGN pin voltage	36 V
R_{PWRGD} pin voltage	36 V
Output short circuit duration	Indefinite
Operating junction temperature range (T_J)	-55°C to +125°C 3/ 4/ 5/
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction to case (θ_{JC})	10°C/W
Thermal resistance, junction to ambient (θ_{JA})	25°C/W

1.4 Recommended operating conditions.

V_{IN}	1.55 V to 40 V
V_{OUT}	+32 V
Operating junction temperature range (T_J)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Absolute maximum input-to-output differential voltage is not achievable with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 45 V, the OUT pin may not be pulled below 0 V. The total IN to OUT differential voltage must not exceed ±45 V.

3/ The device is tested and specified under pulse load conditions such that $T_J \cong T_A$. The device is 100% tested over the –55°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

4/ Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. Limit the output current range if operating at large input-to-output voltage differentials. Limit the input-to-output voltage differential if operating at maximum output current. Current limit foldback limits the maximum output current as a function of input-to-output voltage. See Current Limit versus $V_{IN} – V_{OUT}$ in the manufacturer’s datasheet.

5/ The integrated circuit (IC) includes overtemperature protection circuitry that protects the device during momentary overload conditions. Junction temperature exceeds 125°C when the over temperature circuitry is active unless thermal limit is externally set by loading the TEMP pin. Continuous operation above the specified maximum junction temperature may impair device reliability.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Minimum input voltage 2/		I_{LOAD} = 2.1 A, ΔV_{OUT} = -1 %	-55°C to +125°C	01		1.55	V
					1.4 typical		
Reference voltage 3/ 4/	V_{SET}	1.55 V < V_{IN} < 40 V, 1 mA < I_{LOAD} < 2.1 A	T_J < +125°C	01	396	404	mV
					400 typical		
Reference current	I_{SET}	1.55 V < V_{IN} < 40 V, 1 mA < I_{LOAD} < 2.1 A	-55°C to +125°C	01	49.5	50.5	µA
					50 typical		
Line regulation	V_{SET}	V_{IN} = 1.55 V to 40 V, I_{LOAD} = 1 mA	T_J < +125°C	01		0.8	mV
			-55°C to +125°C		0.1 typical		
	I_{SET}	V_{IN} = 1.55 V to 40 V, I_{LOAD} = 1 mA	T_J < +125°C		-0.12		µA
					-0.03 typical		
Load regulation 5/ 6/	V_{SET}	I_{LOAD} = 1 mA to 2.1 A, V_{IN} = V_{OUT} + 0.55 V	T_J < +125°C	01		1	mV
					0.25 typical		
	I_{SET}	I_{LOAD} = 1 mA to 2.1 A, V_{IN} = V_{OUT} + 0.55 V				0.08	µA
					0.02 typical		
Minimum load current 7/			-55°C to +125°C	01		1	mA
Dropout voltage 6/ 8/ V_{IN} = $V_{OUT(NOMINAL)}$		I_{LOAD} = 1 mA	+25°C	01		65	mV
					10 typical		
			-55°C to +125°C			100	
		I_{LOAD} = 100 mA	+25°C			135	
					100 typical		
			-55°C to +125°C			160	
		I_{LOAD} = 500 mA	+25°C			195	
					150 typical		
			-55°C to +125°C			235	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dropout voltage 6/ 8/ $V_{IN} = V_{OUT(NOMINAL)}$		I_{LOAD} = 1.5 A	+25°C	01		335	mV
					260 typical		
			-55°C to +125°C			425	
		I_{LOAD} = 2.1 A	+25°C			415	
					330 typical		
			-55°C to +125°C			540	
GND pin current 6/ 9/ $V_{IN} = V_{OUT(NOMINAL)}$ + 0.55 V		I_{LOAD} = 0 μA	-55°C to +125°C	01		2.4	mA
					1.2 typical		
		I_{LOAD} = 1 mA				2.6	
					1.3 typical		
		I_{LOAD} = 100 mA				3.6	
					1.8 typical		
		I_{LOAD} = 500 mA				9	
					4.5 typical		
		I_{LOAD} = 1.5 A				46	
					23 typical		
		I_{LOAD} = 2.1 A				88	
					44 typical		
Quiescent current in shutdown		V_{IN} = 40 V, $V\overline{SHDN}$ = 0 V	+25°C	01		1	μA
					0.1 typical		
Output voltage noise		C_{SET} = 0.01 F, C_{OUT} = 10 μF, I_{LOAD} = 2.1 A, V_{OUT} = 5 V, BW = 10 Hz to 100 kHz	+25°C	01	40 typical		μVRMS

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Shutdown threshold		V_{OUT} = off to on	+25°C	01	1.12	1.32	V
					1.22 typical		
		V_{OUT} = on to off			0.85		
					1.03 typical		
$\overline{SHDN}$ pin current 10/		$V_{\overline{SHDN}}$ = 0 V	-55°C to +125°C	01		1	µA
1.55 < V_{IN} < 40 V		$V_{\overline{SHDN}}$ = 40 V				35	
					15 typical		
TEMP voltage 11/			T_J = +25°C	01	0.25 typical		V
			T_J = +125°C		1.25 typical		
TEMP error 11/		I_{TEMP} = 0	0°C < T_J < 125°C	01	-0.09	0.09	V
		I_{TEMP} = 0 µA to 80 µA			-0.1		
I_{TEMP} thermal limit current threshold			25°C < T_J < 125°C	01	95	105	µA
					100 typical		
I_{MON} output 12/ current		I_{LOAD} = 20 mA, R_{MON} = 1 kΩ	-55°C to +125°C	01	5	75	µA
					20 typical		
V_{IN} = $V_{OUT(NOMINAL)}$ + 0.55 V		I_{LOAD} = 500 mA, R_{MON} = 330 Ω			440	560	
					500 typical		
		I_{LOAD} = 1 A, R_{MON} = 330 Ω			0.95	1.05	mA
					1.00 typical		
		I_{LOAD} = 1.5 A, R_{MON} = 330 Ω			1.43	1.57	
					1.50 typical		
		I_{LOAD} = 2.1 A, R_{MON} = 330 Ω			2.02	2.18	
					2.10 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output current sharing error 13/		R_{MON} = 330 Ω, $I_{OUT(MASTER)}$ = 2.1 A	T_J = +25°C	01	-10 0 typical	10	%
TRACK pin pull up current		V_{TRACK} = 750 mV	-55°C to +125°C	01	7 15 typical	25	µA
R_{PWRGD} reference voltage		1.55 V < V_{IN} < 40 V	-55°C to +125°C	01	390 400 typical	410	mV
R_{PWRGD} reference current		1.55 V < V_{IN} < 40 V	-55°C to +125°C	01	48.75 50 typical	51.25	µA
R_{PWRGD} reference voltage hysteresis		1.55 V < V_{IN} < 40 V	+25°C	01	2.4 typical		mV
R_{PWRGD} reference current hysteresis		1.55 V < V_{IN} < 40 V	+25°C	01	300 typical		nA
PWRGD V_{OL}		I_{PWRGD} = 200 A (fault condition)	-55°C to +125°C	01	 55 typical	200	mV
PWRGD internal time delay		V_{OL} to V_{OH} (rising edge)	-55°C to +125°C	01	8 17 typical	25	µs
PWRGD pin leakage current		V_{PWGRD} = 32 V, V_{RPWGRD} = 500 mV	-55°C to +125°C	01		1	µA
CDC reference voltage		1.55 V < V_{IN} < 40 V, I_{MON} = 0 V	-55°C to +125°C	01	390 400 typical	410	mV
CDC/V_{IMON} voltage gain		1.55 V < V_{IN} < 40 V, 0 < I_{CDC} < 20 µA, V_{IMON} = 800 mV to 0	-55°C to +125°C	01	0.320 0.333 typical	0.343	V/V
Ripple rejection		V_{IN} = 1.9 V(AVG), V_{OUT} = 1 V, V_{RIPPLE} = 0.5 V_{PP}, f_{RIPPLE} = 120 Hz, I_{LOAD} = 2.1 A	-55°C to +125°C	01	65 80 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Internal current limit		V_{IN} = 1.55 V	-55°C to +125°C	01	2.2	2.9	A
					2.4 typical		
		$V_{IN} = V_{OUT(NOMINAL)} + 0.55$ V, ΔV_{OUT} = -5% 6/ 14/			2.2		
I_{LIM} threshold voltage		1.55 V < V_{IN} < 40 V	-55°C to +125°C	01	775	825	mV
					800 typical		
Input reverse leakage current		V_{IN} = -40 V, V_{OUT} = 0	-55°C to +125°C	01		2	mA
Reverse output 15/ current		V_{OUT} = 32 V, V_{IN} = 0, V_{SHDN} = 0	+25°C	01		10	µA
					1 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ The device is tested and specified for these conditions with the SET pin connected to the OUT pin, V_{OUT} = 0.4 V.

3/ The device is tested and specified under pulse load conditions such that TJ ≅ TA. The device is 100% tested over the –55°C to +125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than +125°C.

4/ Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. Limit the output current range if operating at large input to output voltage differentials. Limit the input to output voltage differential if operating at maximum output current. Current limit foldback limits the maximum output current as a function of input to output voltage. See Current Limit versus $V_{IN} – V_{OUT}$ in the manufacturer's datasheet.

5/ Load regulation is Kelvin-sensed at the package.

6/ To satisfy minimum input voltage requirements, the device is tested and specified for these conditions with a 32 kΩ resistor between OUT and SET for a 2 V output voltage

7/ The device requires a minimum load current to ensure proper regulation and stability.

8/ Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage equals: $(V_{IN} – V_{DROPOUT})$. For low output voltages and certain load conditions, minimum input voltage requirements limit dropout voltage. See the Minimum Input Voltage curve in the manufacturer's datasheet.

9/ GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ + 0.55 V and PWRGD pin floating. GND pin current increases in dropout. See GND pin current curves in the Typical Performance Characteristics section and the manufacturer's data sheet.

10/ $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

11/ The TEMP output voltage represents the average die temperature next to the power transistor while the center of the transistor can be significantly hotter during high power conditions. Due to power dissipation and temperature gradients across the die, the TEMP output voltage measurement does not guarantee that absolute maximum junction temperature is not exceeded.

12/ The device is tested and specified for these conditions with the I_{MON} and I_{LIM} pins tied together.

13/ Output current sharing error is the difference in output currents of a slave relative to its master when two device regulators are paralleled. The device is tested as a slave with V_{TRACK} = 0.693 V, R_{MON} = 330 Ω and V_{SET} = 0.4 V, conditions when an ideal master is outputting A. The specification limits account for the slave output tracking error from 2.1 A and the worst-case error that can be contributed by a master: the maximum deviation of V_{SET} from 0.4 V and I_{MON} from 2.1 mA.

14/ The integrated circuit (IC) includes overtemperature protection circuitry that protects the device during momentary overload conditions. Junction temperature exceeds +125°C when the over temperature circuitry is active unless thermal limit is externally set by loading the TEMP pin. Continuous operation above the specified maximum junction temperature may impair device reliability.

15/ Reverse-output current is tested with the IN pin grounded and the OUT pin forced to a voltage. The current flows into the OUT pin and out of the GND pin.

Case X

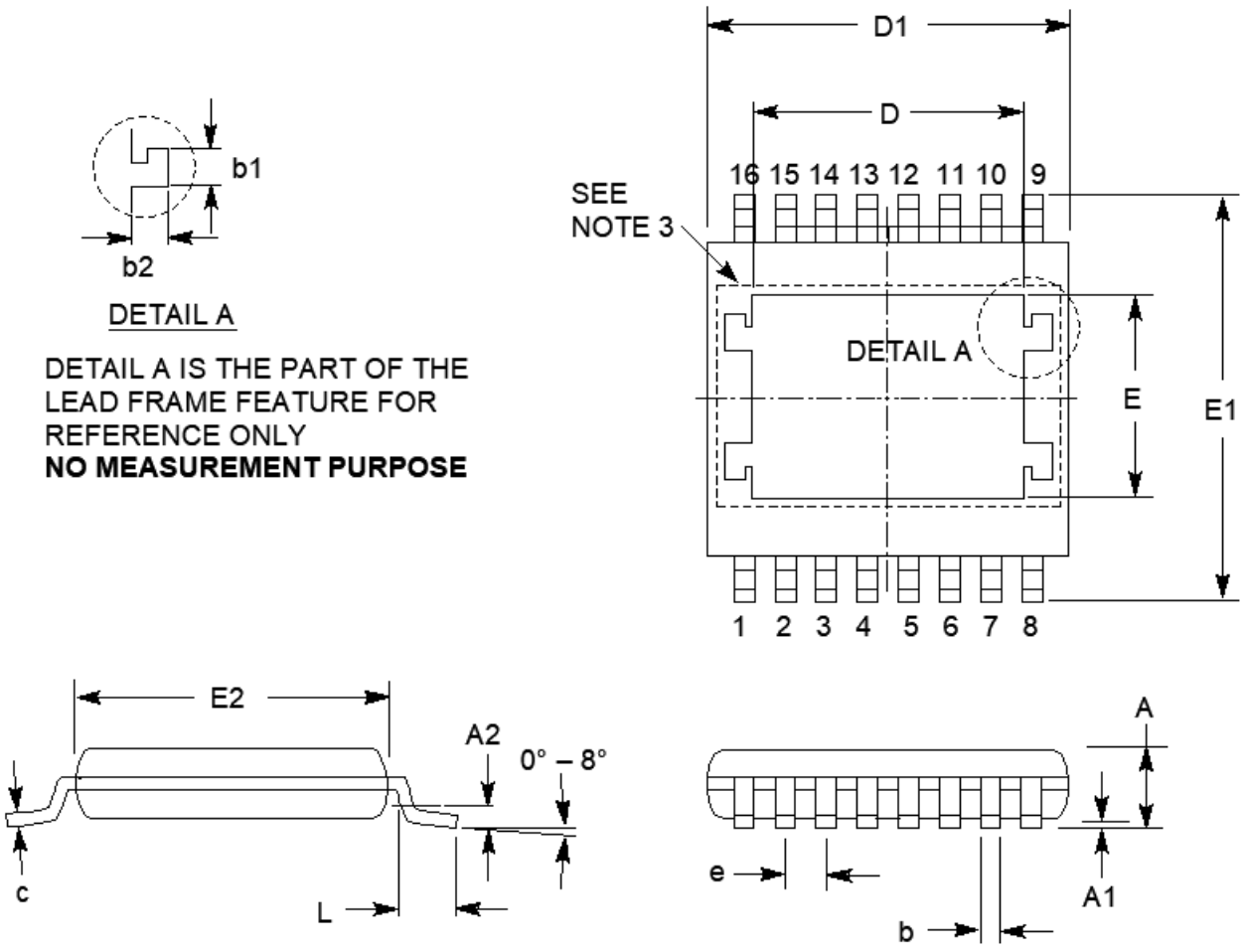

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/22602
		REV	PAGE 11

Symbol	Dimensions			
	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	---	.0433	---	1.10
A1	.002	.006	0.05	0.15
A2	.010 REF		0.25 REF	
b	.0077	.0118	0.195	0.30
b1	.022 REF		0.56 REF	
b2	.021 REF		0.53 REF	
c	.0035	.0079	0.09	0.20
D	---	.141	---	3.58
D1	.193	.201	4.90	5.10
E	---	.116	---	2.94
E1	.252 BSC		6.40 BSC	
E2	.169	.177	4.30	4.50
e	.0256 BSC		0.65 BSC	
L	.020	.030	0.50	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Recommended minimum printed circuit board (PCB) metal size for exposed pad attachment.
3. Bottom exposed paddle may have metal protrusion in this area. This region must be free of any exposed traces or vias on PCB layout.
4. D1 and E1 dimensions do not include mold flash. Mold flash shall not exceed 0.150 mm (.006 inch) per side.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	GND
2	I_{MON} / I_{LIM}
3	CDC
4	P_{PWRGD}
5	SET
6	OUT
7	OUT
8	GND
9	GND
10	IN
11	IN
12	$\overline{SHDN}$
13	TEMP
14	TRACK
15	PWRGD
16	GND
17	Exposed pad

FIGURE 2. Terminal connections.

Terminal symbol	Description
GND	Ground. The exposed pad of the TSSOP package is an electrical connection to GND. To ensure proper electrical and thermal performance, tie the exposed pad or tab directly to the remaining GND pins of the relevant package and the PCB ground. GND pin current is typically 1.2 mA at zero load and increases to about 44 mA at full load.
I_{MON} / I_{LIM}	I_{MON} is the Output monitor. This pin sources a current equal to 1/1000 of output load current. Connecting a resistor from I_{MON} to GND programs a load current dependent voltage for monitoring by an ADC. If I_{MON} connects to I_{LIM}, current limit is externally programmable. I_{LIM} is the External current limit programming. This pin externally programs current limit if connected to I_{MON} and a resistor to GND. Current limit activates if the voltage at I_{LIM} equals 0.8 V. Current limit equals: 1000 • (0.8 V / R_{MON}). An internal clamp typically limits the I_{LIM} voltage to 1 V. If external current limit is set to less than 1 A, connect a series 1 kΩ-10 nF network in parallel with the R_{MON} resistor for stability. Internal current limit foldback overrides externally programmed current limit if V_{IN} – V_{OUT} differential voltage is excessive. If external current limit programming is not used, then ground this pin.
CDC	Cable drop compensation. Connecting a single resistor (R_{CDC}) between the CDC and SET pins provides programmable cable drop compensation that cancels output voltage errors caused by resistive connections to the load. A resistor (R_{MON}) from I_{MON} to GND is also required to enable Cable Drop Compensation. Choose R_{MON} first based on required current limit. $R_{MON} = 0.8\ V \cdot 1000/I_{LIM}$ Calculate the value of RCDC with this formula: $R_{CDC} = (R_{MON} \cdot R_{SET}) / (3000 \cdot R_{WIRE})$ where R_{WIRE} is the total cable or wire resistance to and from the load. From a practical application standpoint, manufacturer recommends limiting cable drop compensation to 20% of V_{OUT} for applications needing good regulation. The limiting factor is variations in wire temperature as copper wire resistance changes about 19% for a 50°C temperature change. If output regulation requirements are loose (for example, when using a secondary regulator), cable drop compensation of up to 50% may be used.
P_{PWRGD}	Power good threshold voltage programming. This pin is the input to the power good comparator. Connecting a resistor between OUT and R_{PWRGD} programs an adjustable power good threshold voltage. The threshold voltage is 0.4 V on the R_{PWRGD} pin, and a 50 µA current source is connected from R_{PWRGD} to GND. If the voltage at R_{PWRGD} is less than 0.4 V, the PWRGD flag asserts and pulls low. If the voltage at R_{PWRGD} is greater than 0.4 V, the PWRGD flag de-asserts and becomes high impedance. For most applications, PWRGD is pulled high with a pull-up resistor. Calculate the value of R_{PWRGD} with this formula: $R_{PWRGD} = (X \cdot V_{OUT(NOMINAL)} – 0.4\ V) / 50\ \mu A$ where X is normally in the 85% to 95% range. A 17 µs deglitching filter suppresses false tripping of the PWRGD flag at the rising edge of PWRGD with instant reset. Hysteresis at the R_{PWRGD} pin is typically 0.6% on the 0.4 V threshold and the 50 µA current source.

FIGURE 2. Terminal connections. – continued.

Terminal symbol	Description
SET	Output voltage programming. This pin is the error amplifier's inverting terminal. It regulates to 0.4 V and a 50 µA current source is connected from SET to GND. Connecting a single resistor from OUT to SET programs output voltage. Calculate the value of the required resistor from the formula: RSET = (VOUT – 0.4 V) / 50 µA. Connecting a capacitor in parallel with R_{SET} provides output voltage soft start capability, improves transient response and decreases output voltage noise. The device error amplifier design is configured so that the regulator always operates in unity-gain.
OUT	Output. These pin(s) supply power to the load. Connect all OUT pins together on the package for proper operation. Stability requirements demand a minimum 10 µF ceramic output capacitor with an ESR less than 100 mΩ to prevent oscillations. Large load transients require larger output capacitance to limit peak voltage transients. Permissible output voltage range is 0.4 V to 32 V. The device requires a 1 mA minimum load current to ensure proper regulation and stability.
IN	Input. These pin(s) supply power to the device. Connect all IN pins together for proper operation. The device requires a local IN bypass capacitor if it is located more than a few inches from the main input filter capacitor. In general, battery output impedance rises with frequency, so adding a bypass capacitor in battery powered circuits is advisable. A 10 µF minimum input capacitor generally suffices. The IN pin(s) withstand a reverse voltage of 45 V. The device limits current flow and no negative voltage appears at OUT. The device protects itself and the load against batteries that are plugged in backwards
$\overline{\text{SHDN}}$	Shutdown/UVLO. Pulling the $\overline{\text{SHDN}}$ pin typically below 1 V puts the device into a low power state and turns the output off. Quiescent current in shut- down is typically less than 1 µA. The $\overline{\text{SHDN}}$ pin turn-on threshold is typically 1.22 V. This pin may either be used as a shutdown function or as an undervoltage lockout function. If using this pin as an undervoltage lockout function, use a resistor divider between IN and GND with the tap point tied to $\overline{\text{SHDN}}$. If using the pin as a shutdown function, drive the pin with either logic or an open-collector/drain with a pull-up resistor. The resistor supplies the pull-up current to the open-collector/drain logic, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically less than 10 µA at 6 V. If unused, connect the SHDN pin to IN.

FIGURE 2. Terminal connections. – continued.

Terminal symbol	Description
TEMP	Die junction temperature. This pin outputs a voltage indicating the device average die junction temperature. At 25°C, this pin typically outputs 250 mV. The TEMP pin slope equals 10 mV/°C so that at 125°C, this pin typically outputs 1.25 V. This pin does not read temperatures less than 0°C. The TEMP pin is not meant to be an accurate temperature sensor, but is useful for debug, monitoring and calculating thermal resistance of the package mounted to the PCB. The TEMP pin also incorporates the ability to program a thermal limit temperature lower than the internal typical thermal shutdown temperature of 165°C. Tying a resistor from TEMP to GND programs the thermal limit temperature with a 100 µA trip point. Calculate the value of the resistor from the formula: RTEMP = (TSHDN • (10 mV/°C)) / 100 µA. where T_{SHDN} is the desired die thermal limit temperature. There are several degrees of hysteresis in the thermal shutdown that cycles the regulator output on and off. Limit the capacitance on the TEMP pin to less than 100 pF. To prevent saturation in the TEMP output device, ensure that V_{IN} is higher than V_{TEMP} by 250 mV.
TRACK	Track pin for paralleling. The TRACK pin allows multiple device to be paralleled in a master/ slave(s) configuration for higher output current applications. This also allows heat to be spread out on the PCB. This circuit technique does not require ballast resistors and does not degrade load regulation. Tying the TRACK pin of the slave device(s) to the I_{MON}/I_{LIM} pins of the master device enables this function. If the TRACK function is unused, TRACK is in a default clamped high state. A TRACK pin voltage below 1.2 V on slave device (s) shuts off the internal 50 µA reference current at SET such that only the 50 µA reference current of the master device is active. All SET pins must be tied together in a master/ slave configuration.
PWRGD	Power good flag. The PWRGD pin is an open-collector logic pin connected to the output of the power good comparator. PWRGD asserts low if the R_{PWRGD} pin is less than 400 mV. The maximum low output level of 200 mV over temperature is defined for 200 µA of sink current. If R_{PWRGD} is greater than 400 mV, the PWRGD pin de-asserts and becomes high impedance. The PWRGD pin may be pulled to 36 V without damaging any internal circuitry regardless of the input voltage.

FIGURE 2. Terminal connections. – continued.

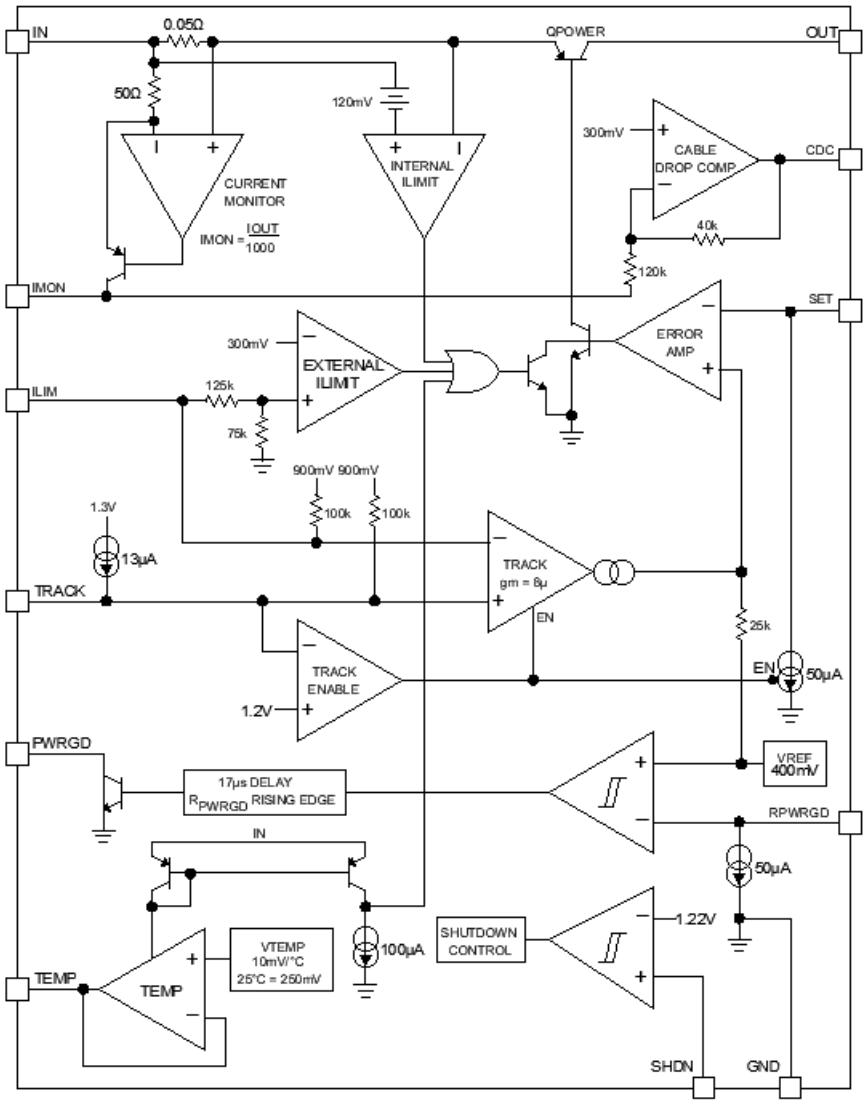

FIGURE 3. Block diagram.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/22602
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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/22602-01XE	24355	Tube, 95 units	3086FE-EP	LT3086FE#Z-EP
		Reel, 2,500 units	3086FE-EP	LT3086FE#TRZ-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123