

Low V_{IN} , High Efficiency 10A Step-Down DC/DC μ Module Regulator

FEATURES

- **Tiny Surface Mount, 4mm × 4mm × 4.32mm LGA and 4mm × 4mm × 4.62mm BGA Packages**
- **Silent Switcher[®]2 Architecture**
- **Ultralow EMI Noise**
- Input Voltage Range: 2.25V to 5.5V
- Output Voltage Range: 0.5V to V_{IN}
- 10A DC Output Current
- Current Mode Control, Fast Transient Response
- Multiphase Parallel Current Sharing with Multiple LTM4658s
- Output Soft-Start with Voltage Tracking
- External Frequency Synchronization
- Selectable Pulse-Skipping Mode
- Power Good Indicator
- Die Temperature Monitoring Output
- Overvoltage, Overcurrent and Overtemperature Protection

APPLICATIONS

- Telecom, Datacom, Networking System
- Optical Module
- Industrial Equipment
- Point-of-Load Regulation

DESCRIPTION

The **LTM[®]4658** is a complete 10A step-down switching mode μ Module[®] regulator in a tiny 4mm × 4mm × 4.32mm LGA and 4mm × 4mm × 4.62mm BGA packages. Included in the package are the switching controller, power MOSFETs, inductor and all support components. Operating over an input voltage range of 2.25V to 5.5V, the LTM4658 supports an output voltage range of 0.5V to V_{IN} set by external resistors. Its high efficiency design delivers 10A continuous output current. Only ceramic input and output capacitors are needed.

The LTM4658 employs a Silent Switcher 2 architecture with internal hot loop bypass capacitors to achieve both low EMI and high efficiency at high switching frequencies.

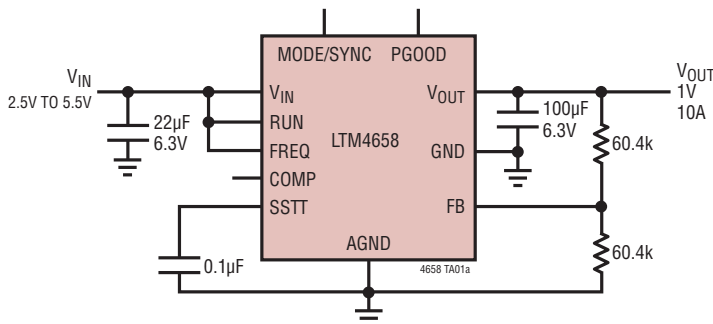
The LTM4658 also supports frequency synchronization, multiphase operation, selectable pulse-skipping mode operation, output voltage tracking for supply rail sequencing. Its high switching frequency and a current mode architecture enables a very fast transient response to line and load changes without sacrificing stability.

Fault protection features include overvoltage, overcurrent and overtemperature protection. The LTM4658 is Pb-Free and RoHS compliant.

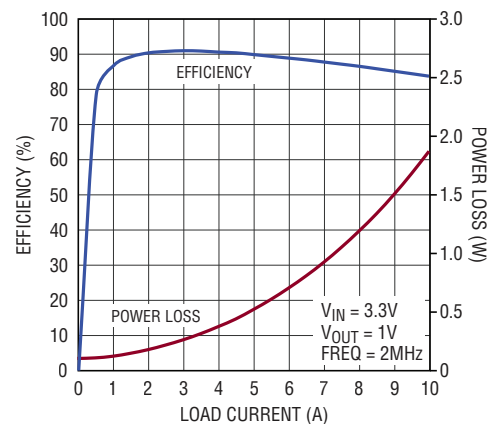
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TYPICAL APPLICATION

Single 10A, 1V Output DC/DC μ Module Regulator



Efficiency vs Load Current



4658 TA01b

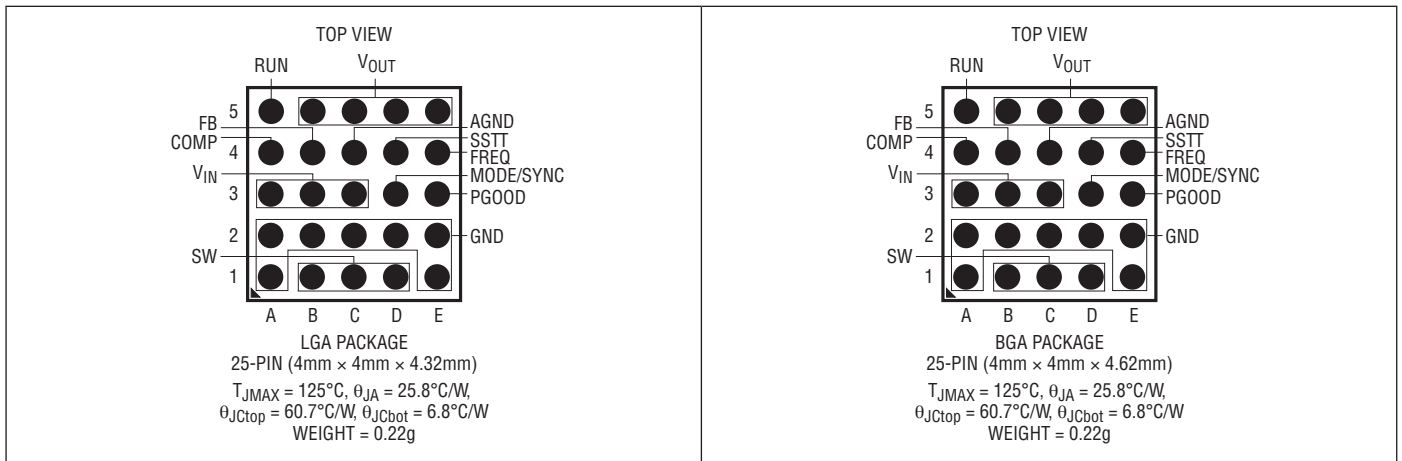
Rev. B

LTM4658

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}	-0.3V to 6V	Operating Junction Temperature	
V_{OUT}	-0.3V to V_{IN}	(Note 2).....	-40°C to 125°C
PGOOD.....	-0.3V to 6V	Storage Temperature Range	-55°C to 125°C
RUN, SSTT, MODE/SYNC,		Peak Solder Reflow Body Temperature	250°C
FB, COMP, FREQ	-0.3V to V_{IN}	Note that the peak reflow temperature must not exceed	
		250°C, including reworking process.	

PIN CONFIGURATION (See Pin Functions and Table 9)



ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4658EV#PBF	Au (RoHS)	4658	4	LGA	4	-40°C to 125°C
LTM4658IV#PBF	Au (RoHS)	4LTV		LGA	4	-40°C to 125°C
LTM4658EY#PBF	SAC305 (RoHS)	4658	1	BGA	4	-40°C to 125°C
LTM4658IY#PBF	SAC305 (RoHS)	1LTY		BGA	4	-40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- [Recommended LGA and BGA PCB Assembly and Manufacturing Procedures](#)
- [LGA and BGA Package and Tray Drawings](#)

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, (Note 2). $V_{IN} = 3.3\text{V}$ per the typical application.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V_{IN}	Input DC Voltage		● 2.25		5.5	V	
$V_{OUT(RANGE)}$	Output Voltage Range	MODE/SYNC = 1MHz, FREQ = V_{IN}	● 0.5		V_{IN}	V	
$V_{OUT(DC)}$	Output Voltage	MODE/SYNC = 1MHz, FREQ = V_{IN} , $V_{OUT} = 0.5\text{V}$	● 0.4925	0.5	0.5075	V	
V_{IN_UVLO}	V_{IN} Undervoltage Lockout	V_{IN} Rising		2.0	2.1	2.2	V
$V_{IN_UVLO_HYS}$	V_{IN} Undervoltage Lockout Hysteresis			150		mV	
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising		0.375	0.4	0.425	V
V_{RUN_HYS}	RUN Pin Hysteresis			60		mV	
I_{RUN}	RUN Pin Leakage Current	RUN = 0.4V			±200	nA	
$I_{Q(VIN)}$	Input Supply Bias Current Pulse-Skipping Mode Forced Continuous Mode Shutdown	MODE/SYNC = FREQ = V_{IN} , $V_{OUT} = 1.5\text{V}$ MODE/SYNC = 0V, FREQ = V_{IN} , $V_{OUT} = 1.5\text{V}$ RUN = 0V		1.6 70 1		mA mA μA	
$I_{S(VIN)}$	Input Supply Current	$V_{OUT} = 1.5\text{V}$, $I_{OUT} = 10\text{A}$		5.5		A	
$I_{OUT(DC)}$	Output Continuous Current Range	$V_{OUT} = 1.5\text{V}$ (Note 4)			10	A	
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	FREQ = V_{IN} , $V_{OUT} = 1.5\text{V}$, $V_{IN} = 2.25\text{V}$ to 5.5V , $I_{OUT} = 0\text{A}$	●	0.001	0.30	%/V	
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	$V_{IN} = \text{FREQ} = 3.3\text{V}$, MODE/SYNC = 1.0MHz, $V_{OUT} = 0.5\text{V}$ $I_{OUT} = 0\text{A}$ to 8A $I_{OUT} = 0\text{A}$ to 10A (Notes 3 and 4)	●	0.2	1.5 1.5	% %	
$V_{OUT(AC)}$	Output Ripple Voltage	$I_{OUT} = 0\text{A}$, $C_{OUT} = 100\mu\text{F} + 22\mu\text{F} \times 2$ Ceramic, (Notes 4)		100		mV	
$\Delta V_{OUT(START)}$	Turn-On Overshoot	$I_{OUT} = 0\text{A}$, $C_{OUT} = 100\mu\text{F} + 22\mu\text{F} \times 2$ Ceramic, (Notes 4)		5		mV	
t_{START}	Turn-On Time	$C_{OUT} = 100\mu\text{F} + 22\mu\text{F} \times 2$ Ceramic, No Load, SSTT = 0.1μF (Note 4)		5		ms	
I_{SSTT}	Track Pin Soft-Start Pull-Up Current	SSTT = 0.5V		7	10	13	μA
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load $C_{OUT} = 100\mu\text{F} + 2 \times 22\mu\text{F}$ Ceramic (Note 4)		157		mV	
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, $C_{OUT} = 100\mu\text{F} + 2 \times 22\mu\text{F}$ Ceramic, (Note 4)		15		μs	
I_{OUTPK}	Output Current Limit	$V_{IN} = 3.3\text{V}$, $V_{OUT} = 0.5\text{V}$		16		A	
V_{FB}	Voltage at V_{FB} Pin	$I_{OUT} = 0\text{A}$, $V_{OUT} = 1.5\text{V}$	● 0.495	0.50	0.505	V	
I_{FB}	Current at V_{FB} Pin				±20	nA	
V_{PGOOD}	PGOOD Trip Level Undervoltage Falling Threshold Overvoltage Rising Threshold	As a Percentage of Regulated V_{OUT} V_{FB} Ramping Negative V_{FB} Ramping Positive		-4 7	-3 10	-2 13	% %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, (Note 2). $V_{IN} = 3.3\text{V}$ per the typical application.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{PGOOD}	PGOOD Leakage	$V_{PGOOD} = 5.5\text{V}$			50	nA
f_{OSC}	Oscillator Frequency			2		MHz
SYNC_RANGE	Sync Frequency Range	$FREQ = V_{IN}$	1.0		2.6	MHz
SYNC_LEVEL	Clock Level High on SYNC Clock Level Low on SYNC		1.2		0.4	V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4658 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4658E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full -40°C to 125°C internal operating temperature range are assured by design, characterization and correlation

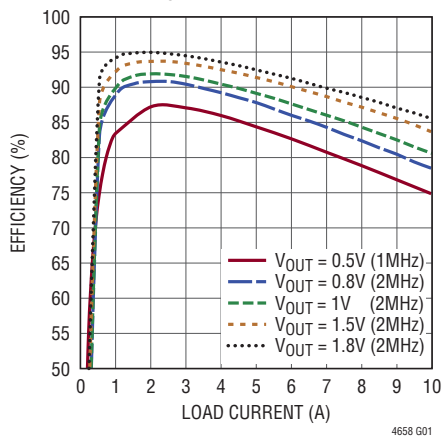
with statistical process controls. The LTM4658I is guaranteed to meet specifications over the full -40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: See output current derating curves for different V_{IN} , V_{OUT} and T_A .

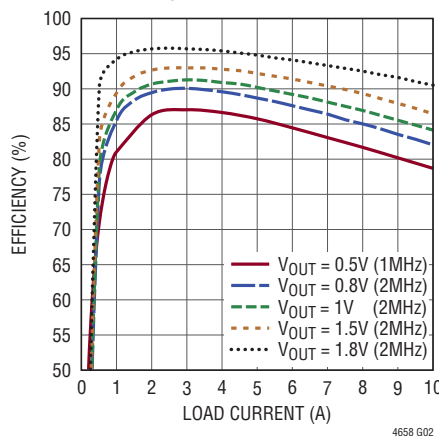
Note 4: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

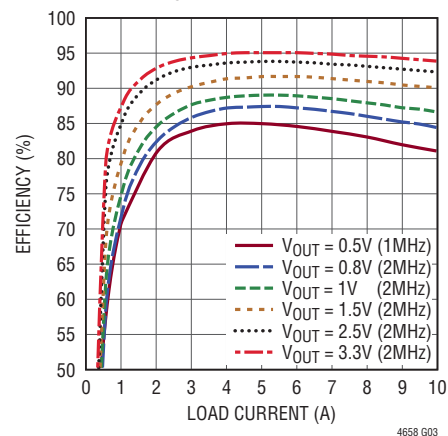
Efficiency vs Load Current at 2.5V_{IN}



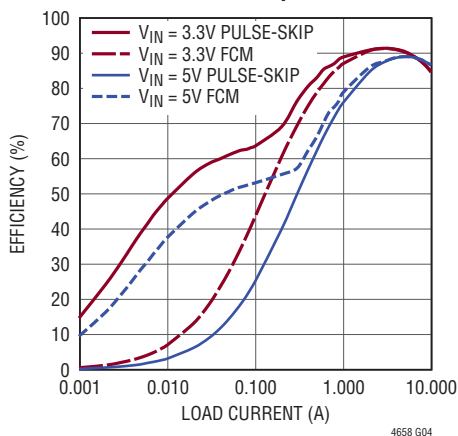
Efficiency vs Load Current at 3.3V_{IN}



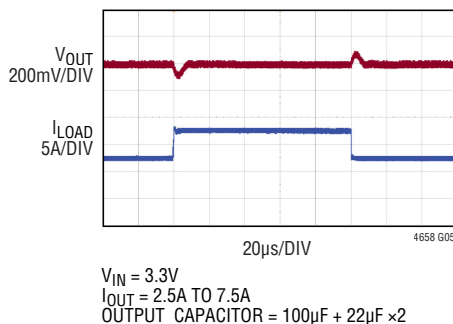
Efficiency vs Load Current at 5V_{IN}



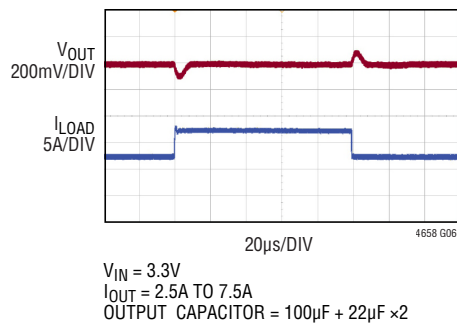
Efficiency vs Load Current at Different Mode of Operation



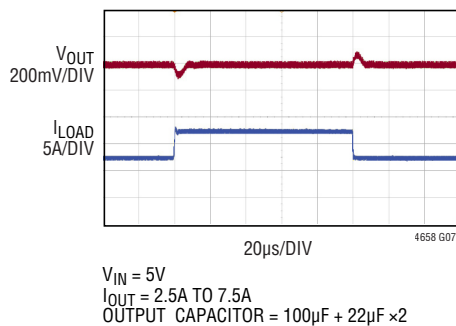
1.0V Output Transient Response, V_{IN} = 3.3V



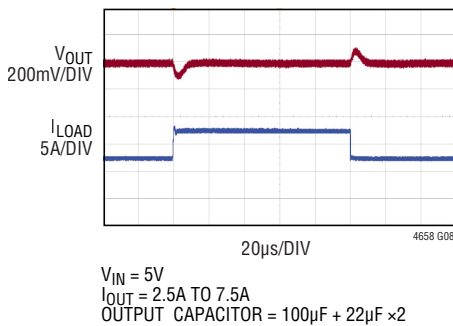
1.5V Output Transient Response, V_{IN} = 3.3V



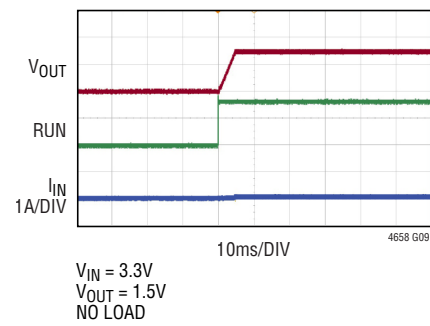
1.0V Output Transient Response, V_{IN} = 5V



1.5V Output Transient Response, V_{IN} = 5V

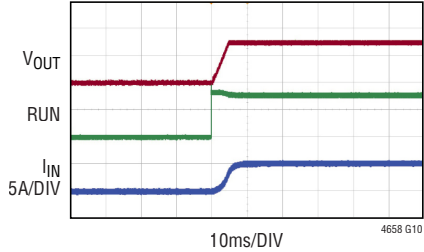


Start-Up with No Load



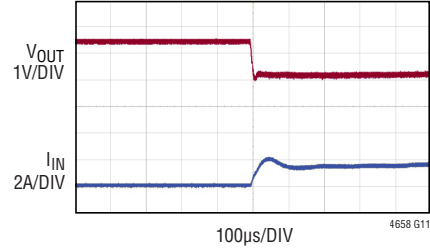
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up with 10A Load

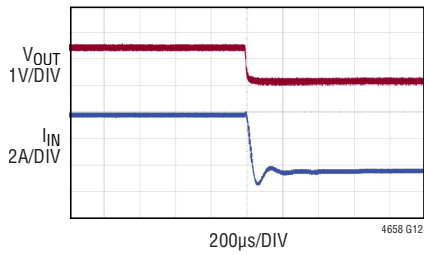


$V_{IN} = 3.3V$
 $V_{OUT} = 1.5V$
 $R_{LOAD} = 0.15\Omega$

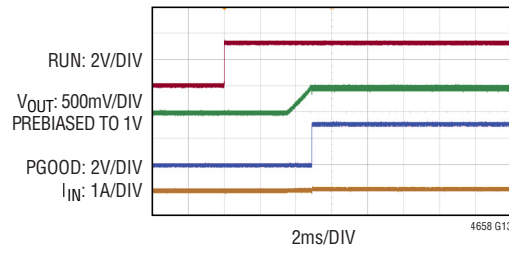
Short-Circuit with No Load



Short-Circuit with 10A Load



Start-Up with Prebiased Output



PIN FUNCTIONS

GND (Pins A1, A2, B2, C2, D2, E1, E2): Power Ground Pins for Both Input and Output Returns.

V_{IN} (Pins A3, B3, C3): The V_{IN} pins supply current to the internal circuitry and topside power switch. All of the V_{IN} pins must be connected together with short, wide traces and bypassed to PGND with low ESR capacitors located as close as possible to the pins.

COMP (Pin A4): Current Control Threshold and Error Amplifier Compensation Point of the Switching Mode Regulator Channel. The current comparator's trip threshold is linearly proportional to this voltage. Tie the COMP pins together for parallel operation. The device is internally compensated.

RUN (Pin A5): Run Control Input of Each Switching Mode Regulator Channel. Enables chip operation by tying RUN above 0.4V. Tying it to GND shuts down the part.

SW (Pins B1, C1, D1): Switching Node Internal High Current Path from MOSFET to Inductor. Connect with solid copper area or leave it floating.

FB (Pin B4): The negative input of the error amplifier for the switching mode regulator. The LTM4658 regulates the voltage between FB and AGND to 500mV. A resistor divider connecting to V_{OUT} sets the output voltage. In PolyPhase[®] operation, tying the FB pins of the subordinate channels to V_{IN} to disable the internal error amplifier. See the Applications Information of Switching Regulator section for details.

V_{OUT} (Pins B5, C5, D5, E5): Power Output Pins of Each Switching Mode Regulator. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

AGND (Pin C4): The AGND pin is the ground reference for the internal analog circuitry, including the bandgap voltage reference. To achieve good load regulation, connect

the AGND pin to the negative terminal of the output capacitor (C_{OUT}) at the load. A drop in the high current power ground return path will be compensated. All of the signal components, such as the FB resistor dividers and soft-start capacitor, should be referenced to the AGND node. The AGND node carries very little current and, therefore, can be a minimal size trace.

MODE/SYNC (Pin D3): The MODE/SYNC pin facilitates multiphase operation and synchronization to an external clock. Depending on the mode of operation, the MODE/SYNC pin either accepts an input clock pulse or outputs a clock pulse at its operating frequency. (see Multiphase Operation in Applications Information). The MODE/SYNC pin also programs the mode of operation: pulse-skipping or forced continuous.

SSTT (Pin D4): Soft-Start, Tracking and Temperature Monitor Pin. An internal 10 μ A current into an external capacitor on the soft-start pin programs the output voltage ramp rate during start-up. When SSTT is below 0.5V, the V_{FB} pin voltage will track the SSTT pin voltage. When SSTT is above 0.5V, the tracking function is disabled, the internal reference resumes control of the error amplifier and the SSTT pin serves to a voltage representative of junction temperature. For a clean recovery from an output short circuit condition, the SSTT pin is pulled down to approximately 140mV above the V_{FB} voltage and a new soft-start cycle is initiated. During shutdown and fault conditions, the SSTT pin is pulled to ground.

PGOOD (Pin E3): Output Power Good with Open-Drain Logic of the Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within $-3\%/10\%$ of the internal 0.5V reference.

FREQ (Pin E4): The FREQ pin sets the oscillator frequency with an external resistor to AGND or sets the phasing for multiphase operation. (See Multiphase Operation in Applications Information section).

OPERATION

The LTM4658 is a standalone nonisolated step-down μ Module regulator. It can deliver up to 10A of DC output current with a few external input and output capacitors. This module provides precisely regulated output voltage from 0.5V to 5.5V over 2.25V to 5.5V input voltage range. The typical application schematic is shown on page 1.

The LTM4658 has an integrated constant frequency peak current mode step-down regulator with power MOSFETs, inductor, and other supporting discrete components. The default switching frequency is 2MHz. It can be externally synchronized to a clock from 1MHz to 2.60MHz. See the Applications Information section.

Current mode control provides cycle-by-cycle fast current limiting, overcurrent protection. Internal feedback loop compensation provides sufficient stability margins and good transient performance with wide range of output capacitors, even with all ceramic output capacitors.

Internal undervoltage and overvoltage comparators pull the open-drain PGOOD output low if the feedback voltage exits a $-3\%/10\%$ window around the regulation point. Furthermore, in an overvoltage condition, internal top MOSFET is turned off and bottom MOSFET is turned on and held on until the overvoltage condition clears.

For systems with higher power requirements, multiphase operation can be easily employed with the synchronization and phase mode controls.

Pulling the RUN pin to GND forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, pulse-skipping mode operation can be enabled to achieve higher efficiency compared to forced continuous mode by setting MODE/SYNC pin to V_{IN} . The SSTT pin is used for power supply tracking, soft-start programming and die temperature monitoring. See the Applications Information section.

APPLICATIONS INFORMATION

The typical LTM4658 application circuit is shown on page 1. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. Refer to Table 8 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

The minimum V_{OUT} step-down ratio that can be achieved for a given input voltage is limited by minimum on-time of the regulator.

The minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated with Equation 1.

$$D_{MIN} = T_{ON(MIN)} \cdot f_{SW} \quad (1)$$

where $T_{ON(MIN)}$ is the minimum on-time, 45ns typical for the LTM4658. In the rare cases where the minimum duty cycle is surpassed, output will overvoltage and a slower switching frequency is needed to accommodate the high V_{IN}/V_{OUT} ratio.

The LTM4658 is capable of a maximum duty cycle of 100%, therefore, the V_{IN} -to- V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch, the inductor DCR and the load current.

It should be noted that the practical transconductance amplifier has a limited output voltage range, to stay in regulation, COMP voltage in the compensation loop must reflect the peak current value. If the output is set to below 0.7V and the switching frequency is 2MHz or above, due to the small ripple current, the output voltage may not be regulated at no load since the transconductance amplifier is running to its low output voltage limit. To avoid this issue, reduce to a lower frequency or change the operation mode to pulse-skipping mode.

Output Voltage Programming and Output Voltage Sensing

The PWM controller has an internal 0.5V reference voltage. Resistor divider from V_{OUT} remote sensing point to FB pin and from FB pin to AGND pin programs the output voltage (Equation 2). Refer to the Block Diagram.

$$V_{OUT} = 0.5V \cdot \frac{R_A + R_B}{R_B} \quad (2)$$

In high current operation, a ground offset may be present between the LTM4658 local ground and ground at the load. To overcome this offset, AGND should have a Kelvin connection to the load ground, and the lowest potential node of the resistor divider should be connected to AGND. The internal error amplifier senses the difference between this feedback voltage and a 0.5V AGND referenced voltage. This scheme overcomes any ground offsets between local ground and remote output ground, resulting in a more accurate output voltage. The LTM4658 allows for remote output ground deviations as much as $\pm 100mV$ with respect to the local ground.

Input Decoupling Capacitors

The LTM4658 module should be connected to a low AC-impedance DC source. All of the V_{IN} pins must be connected together with short, wide traces and bypassed to PGND with low ESR capacitors located as close as possible to the pins. For the regulator, one-piece 22 μF input ceramic capacitor is recommended for RMS ripple current decoupling. Bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor and polymer capacitor.

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated with Equation 3.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \cdot \sqrt{D \cdot (1-D)} \quad (3)$$

where $\eta\%$ is the estimated efficiency of the power module.

Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only two pieces of 47 μF low ESR output ceramic capacitor is required for LTM4658 to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 8 shows a matrix of different output voltages and output

APPLICATIONS INFORMATION

capacitors to minimize the voltage droop and overshoot during a 2.5A (25%) load-step transient.

Multiphase operation will reduce effective output ripple as a function of the number of phases. [Application Note 77](#) discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more a function of stability and transient response. The Analog Devices [LTpowerCAD](#)® design tool is available to download online for output ripple, stability and transient response analysis and calculating the output ripple reduction as the number of phases implemented increases by N times.

Modes of Operation

The MODE/SYNC pin either synchronizes the external switching frequency, or a clock output, to set the PWM mode. The PWM modes of operation are either pulse-skipping or forced continuous. See Table 1.

Table 1. LTM4658 Single Phase Configuration

FREQ PIN CONNECTION	MODE/SYNC PIN CONNECTION	MODE OF OPERATION	SWITCHING FREQUENCY
V _{IN}	Clock Input	Forced Continuous	External Clock
V _{IN}	AGND	Forced Continuous	2MHz Default
V _{IN}	V _{IN}	Pulse-Skip	2MHz Default
Resistor to AGND	Clock Output	Forced Continuous	R _{FREQ} Programmed

The LTM4658 operates in forced continuous mode for low noise or pulse-skipping mode for high efficiency at light load. The LTM4658 operates in pulse-skipping mode when both FREQ and MODE/SYNC pins are connected to V_{IN}. In pulse-skipping mode, switching cycles are skipped at light load to regulate the output voltage. The LTM4658 defaults to forced continuous in regulation and during synchronization. During forced continuous mode, the top switch turns on every cycle and light load regulation is achieved by allowing negative inductor current.

Setting the Operating Frequency

The operating frequency defaults to 2MHz when the FREQ pin is tied to V_{IN}. If any frequency higher than the default

frequency is required, the frequency can be programmed by tying a resistor from FREQ pin to AGND with Equation 4.

$$R_{\text{FREQ}} = 568 \cdot f_{\text{SW}}^{(-1.08)} \quad (4)$$

where R_{FREQ} is in kΩ and f_{SW} is the desired switching frequency in MHz.

The frequency can be programmed to switch from 1MHz to 3MHz. Table 2 shows the necessary R_{FREQ} value for a desired switching frequency.

Table 2. SW Frequency vs R_{FREQ} Value

f _{SW} (MHz)	R _{FREQ} (kΩ)
1	549
2	274
2.2	243
3	178

Synchronizing the Oscillator to an External Clock

The LTM4658 switching frequency can also be adjusted by synchronizing the internal PLL circuit to an external clock to the MODE/SYNC pin. The synchronization frequency range is 1MHz to 2.6MHz. The LTM4658 operates in forced continuous mode when synchronized to an external clock.

Tie the FREQ pin to V_{IN} configures the MODE/SYNC pin as a clock input. During synchronization, the top power switch turn-on is locked to the rising edge of the external frequency source. The slope compensation is automatically adapted to the external clock frequency.

At start-up, before the LTM4658 recognizes the external clock applied to MODE/SYNC, the LTM4658 will switch at its default frequency of 2MHz. Once the externally applied clock is recognized, the switching frequency will gradually transition from the default frequency to the applied frequency. If the external clock is removed, the LTM4658 will slowly transition back to the default frequency.

The synchronizing clock amplitude should be greater than 1.2V and less than 0.4V with a pulse width greater than 40ns. An internal 200k resistor on MODE/SYNC pin to AGND allows the MODE/SYNC to be floating. Please note

APPLICATIONS INFORMATION

that low switching frequency will increase the inductor peak current and the output voltage ripple.

Multiphase Operation

For output loads that demand more than 10A of current, multiple LTM4658s can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples. See Table 3.

To parallel multiple LTM4658 modules to achieve the same switching frequency, a perfect interleaved phase shift and an accurate current sharing between different modules, one of the LTM4658 will become the main module and the rest of LTM4658s need to be programmed to be subordinate modules. Refer to multiphase application circuits.

1. Connect a resistor from FREQ pin to AGND of the main phase will programs the frequency and configures the MODE/SYNC pin to become a clock output used to drive the MODE/SYNC pins of the subordinate phase(s).

Connecting the FREQ pin of the main phase to V_{IN} configures the MODE/SYNC pin to become an input capable of accepting an external clock. The switching frequency defaults to the nominal 2MHz internal

frequency when the external clock is unavailable, such as during start-up.

Connecting the FB pin to V_{IN} configures a phase as a subordinate. The MODE/SYNC becomes an input and the voltage control loop is disabled. The subordinate phase current control loop is still active and the peak current is controlled via the shared COMP node. Careful consideration should be taken when routing the COMP node between phases. Routing the COMP and AGND nodes together is recommended to create a low inductance path.

Connecting the PGOOD pins together and adding an external pull-up resistor allows the main phase to communicate with the subordinate phases on when start-up has been completed.

The pull-up voltage should be greater than 0.49V for subordinate channels on multiphase operations.

2. The phasing of a subordinate phase relative to the main phase is programmed with a resistor divider on the FREQ pin (see Figure 2). Use of 1% resistors is recommended. See Table 4 for more information.

Table 3. Multiphase Configuration

MAIN/SUBORDINATE	FREQ PIN	FB PIN	MODE/SYNC PIN	SWITCHING FREQUENCY (f_{SW})
Main	V_{IN}	V_{OUT} Divider	Clock Input	External Clock/2MHz Default
Main	Resistor to AGND	V_{OUT} Divider	Clock Output	FREQ Programmed
Subordinate	V_{IN} Divider	V_{IN}	Clock Input	External Clock

Table 4. Programming Subordinate Phase Angle

SYNC PHASE ANGLE	R3 RATIO	R4 RATIO	R3 EXAMPLE	R4 EXAMPLE
0°	0Ω	NA	0Ω	NA
90°	3 • R	R	301k	100k
120°	7 • R	5 • R	243k	174k
180°	NA	0Ω	NA	0Ω
240°	5 • R	7 • R	174k	243k
270°	R	3 • R	100k	300k

APPLICATIONS INFORMATION

When configured for main/subordinate operation, the subordinate phases operate in forced continuous modes.

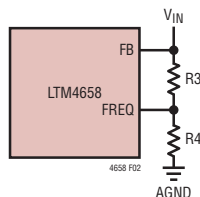


Figure 2. Phase Programming

The LTM4658 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Tie RUN, SSTT, FB and COMP pins of each paralleling channel together. Figure 17 through Figure 19 show examples of parallel operation and pin connections.

INPUT RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 3 shows this graph.

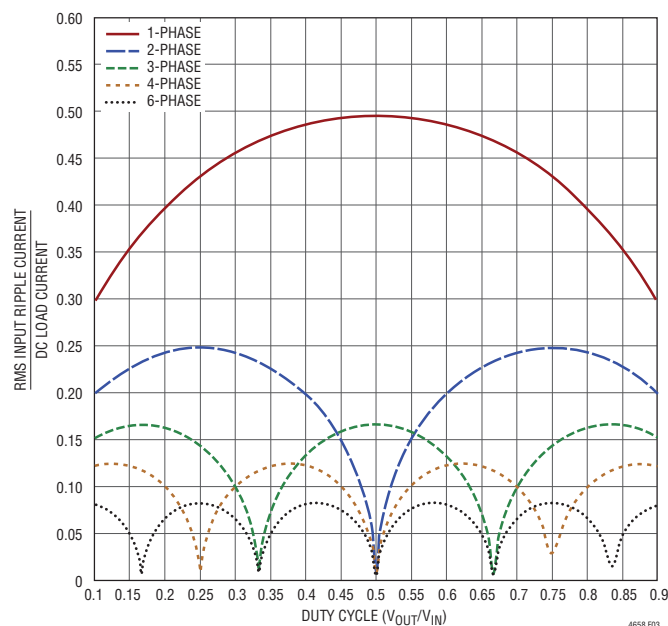


Figure 3. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

Soft-Start /Tracking/Temperature Monitor

The LTM4658 allows the user to program its output voltage ramp rate by means of the SSTT pin.

An internal 10 μ A pulls up the SSTT pin. Putting an external capacitor on SSTT enables soft-starting the output to prevent current surge on the input supply and output voltage overshoot. During the soft-start ramp, the output voltage will proportionally track the SSTT pin voltage. When the soft-start is complete, the pin will servo to a voltage proportional to the LTM4658 junction temperature. See Figure 4 showing the SSTT pin operating range.

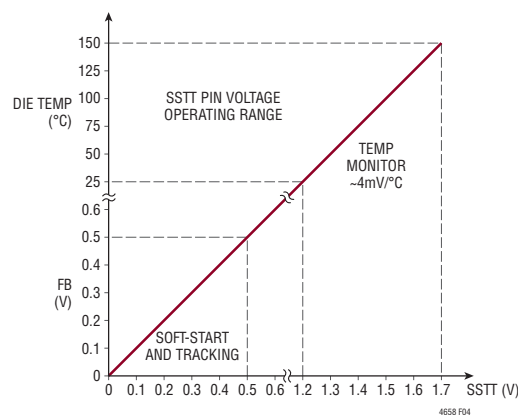


Figure 4. Soft-Start and Temperature Monitor Operation

The soft-start time is calculated with Equation 5.

$$T_{SS} = C_{SS} \cdot \frac{500\text{mV}}{10\mu\text{A}} \quad (5)$$

For output tracking applications, SSTT can be externally driven by another voltage source. From 0V to 0.5V, the SSTT voltage will override the internal 0.5V reference input to the error amplifier, thus regulating the FB pin voltage to that of SSTT pin. When SSTT is above 0.5V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

An active pull-down circuit is connected to the SSTT pin to discharge the external soft-start capacitor in the case of fault conditions. The ramp will restart when the fault is cleared. Fault conditions that clear the soft-start capacitor are the RUN/UV pin transitioning low, V_{IN} voltage falling too low or thermal shutdown.

APPLICATIONS INFORMATION

Once the soft-start cycle has completed and the output power good flag thrown, the SSTS pin reports the die junction temperature. The LTM4658 regulates the SSTS pin to a voltage proportional to the junction temperature. While reporting the temperature, the SSTS voltage is not valid below 1V. The junction temperature is calculated with Equation 6.

$$T_J (\text{°C}) = \frac{V_{SSTS}}{4\text{mV}} - 273 \quad (6)$$

The following procedure is used for a more accurate measurement of the junction temperature:

1. Measure the ambient temperature T_A .
2. Measure the SSTS voltage while in pulse-skipping mode with the V_{OUT} pulled up slightly higher than the regulated V_{OUT} .
3. Calculate the slope of the temperature sensing circuit using Equation 7.

$$\text{Slope} \left(\frac{\text{mV}}{\text{°C}} \right) = \frac{V_{SSTS}}{T_A + 273} \quad (7)$$

4. Calculate the junction temperature with the new calibrated slope.

When the output voltage goes out of regulation and the power good pin is pulled low, the soft-start pin no longer reports the temperature.

Power Good

The PGOOD pins are open drain pins that can be used to monitor valid output voltage regulation. This pin monitors a $-3/+10\%$ window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTM4658's PGOOD falling edge includes a blanking delay of approximately $100\mu\text{s}$. The PGOOD is also actively pulled low during fault conditions: RUN pin is low, V_{IN} is too low or in thermal shutdown.

Stability Compensation

The LTM4658 module's internal compensation loop is designed and optimized for low ESR ceramic output capacitors only application. A 10pF to 15pF phase boost cap between V_{OUT} and FB pins may be required to help maintaining a high phase margin. The [LTpowerCAD](#) design tool is available to download for control loop optimization.

RUN Threshold Programming

The LTM4658 has a precision threshold RUN pin to enable or disable switching. Pulling the RUN pin to ground forces the LTM4658 into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.4V will turn on the entire chip.

The rising threshold of the RUN comparator is 400mV with 60mV of hysteresis. Connect the RUN pin to V_{IN} if the shutdown feature is not used. Adding a resistor divider from V_{IN} to RUN programs the LTM4658 to regulate the output only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(RUN)}$, is used in situations where the input supply is current limited or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(RUN)}$ threshold prevents the regulator from operating at source voltages where problems may occur. This threshold can be adjusted by setting the values R1 and R2 such that they satisfy Equation 8.

$$V_{IN(RUN)} = \left(\frac{R_1}{R_2} + 1 \right) \cdot 400\text{mV} \quad (8)$$

where the LTM4658 will remain off until V_{IN} is above $V_{IN(RUN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(RUN)}$.

Alternatively, a resistor divider from an output of another regulator to the enable RUN pin of the LTM4658 provides event-based power up sequencing, enabling the LTM4658 when the output of the other regulator reaches a predetermined level.

APPLICATIONS INFORMATION

Output Overvoltage Protection

During an output overvoltage event, when the FB pin voltage is greater than 110% of nominal, the LTM4658 top power switch will be turned off. If the output remains out of regulation for more than 100 μ s, the PGOOD pin will be pulled low. An output overvoltage event should not happen under normal operating conditions.

Output Short-Circuit Protection and Recovery

The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the COMP pin. If the output current increases, the error amplifier raises the COMP pin voltage until the average inductor current matches the new load current. In normal operation, the LTM4658 clamps at the maximum COMP pin voltage.

When the output is shorted to ground, the inductor current decays very slowly during the switch off time because of the low voltage across the inductor. To keep the current in control, a secondary limit is also imposed on the valley inductor current. If the inductor current measured through the bottom power switch increases beyond $I_{\text{VALLEY(MAX)}}$, the top power switch will be held off and switching cycles will be skipped until the inductor current is reduced.

Recovery from a short circuit can be abrupt and because the output is shorted and below regulation the regulator is requesting the maximum current to charge the output. When the short circuit condition is removed, the inductor current could cause an extreme voltage overshoot in the output. The LTM4658 addresses this potential issue by regulating the SSTT voltage just above the FB voltage anytime the output is out of regulation. Therefore, a recovery from an output short circuit goes through a soft-start cycle. The output ramp is controlled and the overshoot is minimized.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the

outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a μ Module package mounted to a hardware test board—also defined by JESD51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”). The motivation for providing these thermal coefficients is found in JESD51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the μ Module regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA} , the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. $\theta_{J\text{Cbot}}$, the thermal resistance from junction to bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical module regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value maybe useful for comparing packages but the test conditions don’t generally match the user’s application.

APPLICATIONS INFORMATION

3. θ_{JCtop} , the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical μ Module are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot} , this value may be useful for comparing packages but the test conditions don't generally match the user's application.

A graphical representation of the aforementioned thermal resistances is given in Figure 5; blue resistances are contained within the μ Module regulator, whereas green resistances are external to the μ Module.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JEDEC 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a μ Module. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the μ Module—as the standard defines for θ_{JCtop} and θ_{JCbot} , respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the μ Module and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the μ Module with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet.

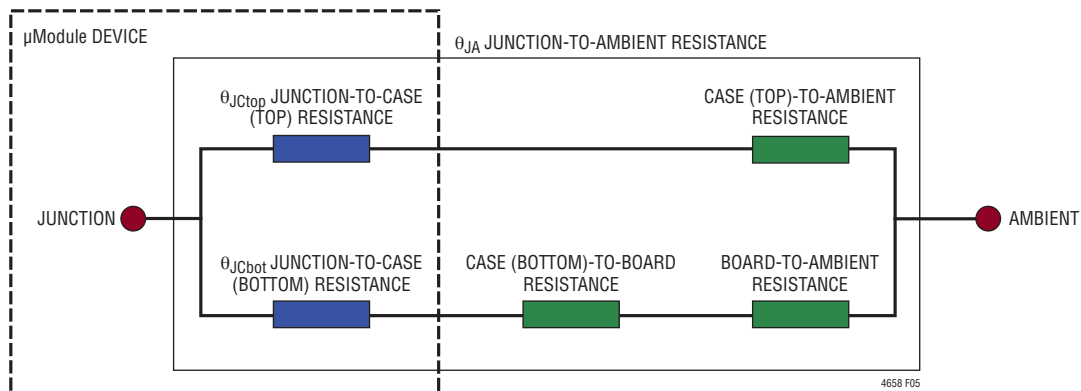


Figure 5. Graphical Representation of JEDEC 51-12 Thermal Coefficients

APPLICATIONS INFORMATION

The $2.5V_{IN}$, $3.3V_{IN}$ and $5V_{IN}$ power loss curves in Figure 6, Figure 7 and Figure 8 can be used in coordination with the load current derating curves in Figure 9 to Figure 14 for calculating an approximate θ_{JA} thermal resistance for the LTM4658 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors according to the junction temperature. This approximate factor is ~ 1.2 assuming the junction temperature is reaching 120°C . Maximum load current is achievable while increasing ambient temperature as long as the junction temperature is less than 120°C , which is 5°C guardband from maximum junction temperature of 125°C . When the ambient temperature reaches a point where the junction temperature is 120°C , then the load current is lowered to maintain the junction at 120°C while increasing ambient temperature up to 120°C . The derating curves are plotted with the output current starting at 10A and the ambient temperature at 30°C . The output voltages are 1.0V, 1.5V and 2.5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will

decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. For example, to determine the maximum ambient temperature allowable when $V_{IN} = 5\text{V}$, $V_{OUT} = 1\text{V}$ and 10A load current without a heat sink and airflow, simply find out the power loss from Figure 7 which equals to 1.54W in this case, then multiply by the 1.2 coefficient for 120°C junction temperature, If the 81.6°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 43°C divided by 1.85W equals a $21^{\circ}\text{C}/\text{W}$ for θ_{JA} the system equivalent thermal resistance. Table 5 specifies $20.8^{\circ}\text{C}/\text{W}$ value which is very close. Table 6 and Table 7 provide equivalent thermal resistances for 1.5V and 2.5V outputs with and without airflow. **The Pin Configuration section shows the simulation data for the worst case scenario.** Table 5 through Table 7 provide equivalent thermal resistances for 1.0V, 1.5V and 2.5V outputs with and without airflow. The derived thermal resistances in Table 5 through Table 7 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four-layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are $95\text{mm} \times 76\text{mm}$.

APPLICATIONS INFORMATION

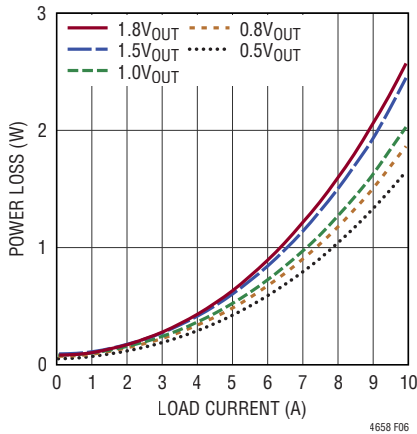


Figure 6. Power Loss vs Load Current at 2.5VIN

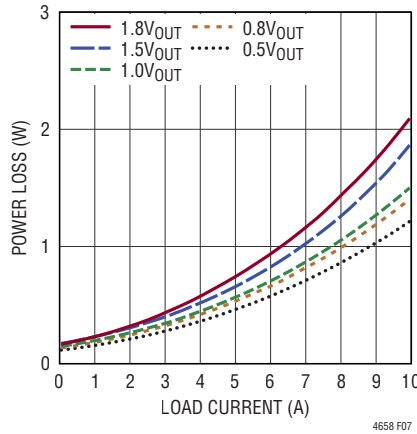


Figure 7. Power Loss vs Load Current at 3.3VIN

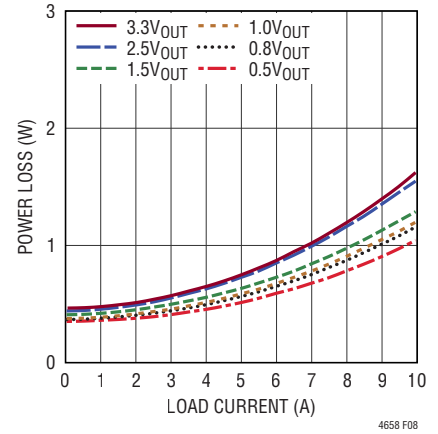


Figure 8. Power Loss vs Load Current at 5VIN

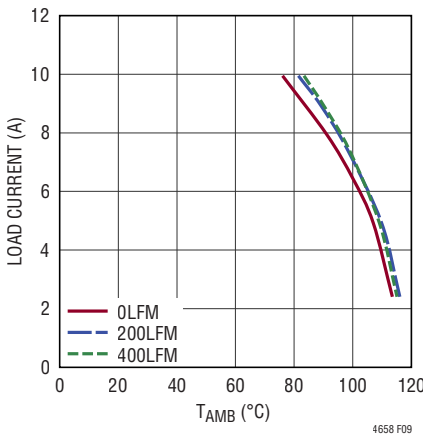


Figure 9. 3.3V to 1V Derating Curve, No Heat Sink

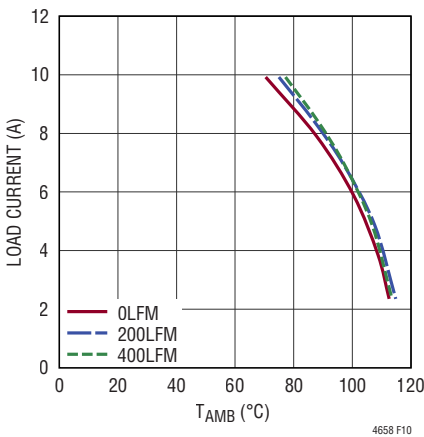


Figure 10. 3.3V to 1.5V Derating Curve, No Heat Sink

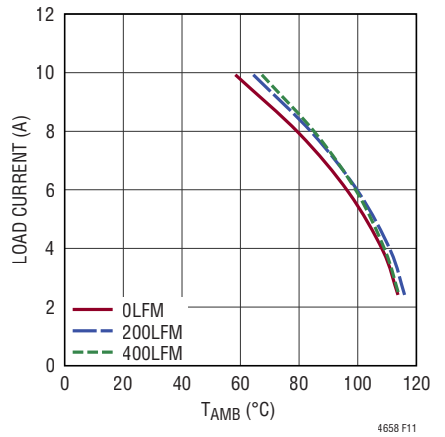


Figure 11. 3.3V to 2.5V Derating Curve, No Heat Sink

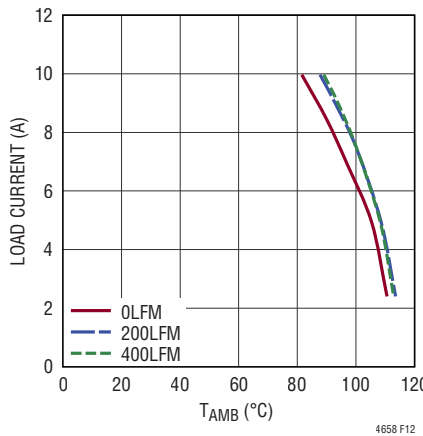


Figure 12. 5V to 1V Derating Curve, No Heat Sink

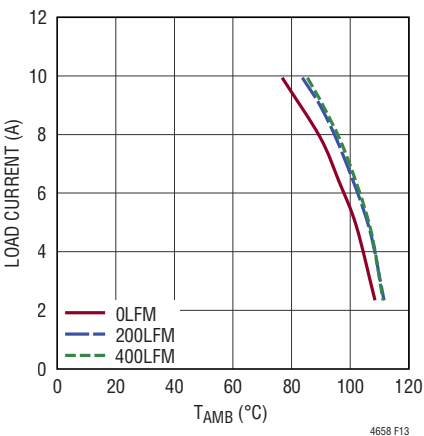


Figure 13. 5V to 1.5V Derating Curve, No Heat Sink

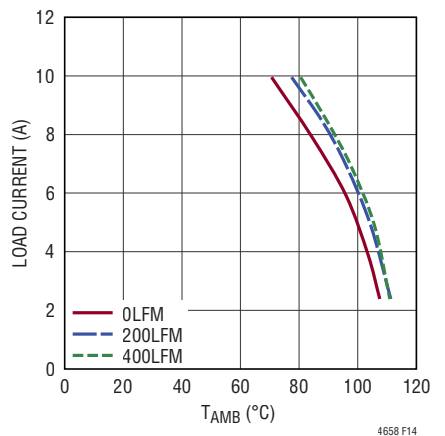


Figure 14. 5V to 2.5V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

Table 5. 1.0V Output

DERATING CURVE	V _{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ _{JA} (°C/W)
Figure 9, Figure 12	3.3, 5	Figure 7, Figure 8	0	None	20.6
Figure 9, Figure 12	3.3, 5	Figure 7, Figure 8	200	None	18.5
Figure 9, Figure 12	3.3, 5	Figure 7, Figure 8	400	None	17.4

Table 6. 1.5V Output

DERATING CURVE	V _{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ _{JA} (°C/W)
Figure 10, Figure 13	3.3, 5	Figure 7, Figure 8	0	None	20.5
Figure 10, Figure 13	3.3, 5	Figure 7, Figure 8	200	None	18.3
Figure 10, Figure 13	3.3, 5	Figure 7, Figure 8	400	None	17.5

Table 7. 2.5V Output

DERATING CURVE	V _{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ _{JA} (°C/W)
Figure 11, Figure 14	3.3, 5	Figure 7, Figure 8	0	None	21.2
Figure 11, Figure 14	3.3, 5	Figure 7, Figure 8	200	None	18.3
Figure 11, Figure 14	3.3, 5	Figure 7, Figure 8	400	None	17.5

Table 8. Output Voltage Response vs Component Matrix (Refer to Front Page Figure) 0A to 5A Load Step Typical Measured Values

C _{IN} CERAMIC VENDORS	VALUE (μF)	PART NUMBER	C _{OUT} VENDORS	VALUE (μF)	PART NUMBER
Taiyo Yuden	10	EMK212BB7106MG-T	Murata	22	GRM188R60J226MEA0D
Murata	22	GRM188R61A226ME15D	Murata	100	GRM21BR60J107ME15K

V _{OUT} (V)	C _{IN} (CERAMIC) (μF)	C _{IN} (BULK)	C _{OUT} (CERAMIC) (μF)	C _{OUT} (BULK) (μF)	C _{FF} (pF)	V _{IN} (V)	DROOP (mV)	P-P Deviation (mV)	RECOVERY TIME (μs)	LOAD STEP (A/μs)	LOAD STEP SLEW RATE (A/μs)	FREQ. (kHz)
0.5	2 × 10	150	100 + 2 × 22	Open	Open	3.3	40	78	5	5	5	1000
0.8	2 × 10	150	100 + 2 × 22	Open	Open	3.3	45	92	10	5	5	2000
0.8	2 × 10	150	100 + 2 × 22	Open	Open	5	45	90	10	5	5	2000
1	2 × 10	150	100 + 2 × 22	Open	Open	3.3	55	109	10	5	5	2000
1	2 × 10	150	100 + 2 × 22	Open	Open	5	55	105	10	5	5	2000
1.5	2 × 10	150	100 + 2 × 22	Open	Open	3.3	80	157	10	5	5	2000
1.5	2 × 10	150	100 + 2 × 22	Open	Open	5	80	156	10	5	5	2000
2.5	2 × 10	150	100 + 2 × 22	Open	Open	3.3	120	239	15	5	5	2000
2.5	2 × 10	150	100 + 2 × 22	Open	Open	5	120	241	15	5	5	2000
3.3	2 × 10	150	100 + 2 × 22	Open	Open	5	120	291	15	5	5	2000

APPLICATIONS INFORMATION

Safety Considerations

The LTM4658 modules do not provide galvanic isolation from V_{IN} to V_{OUT} . There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and over current protection.

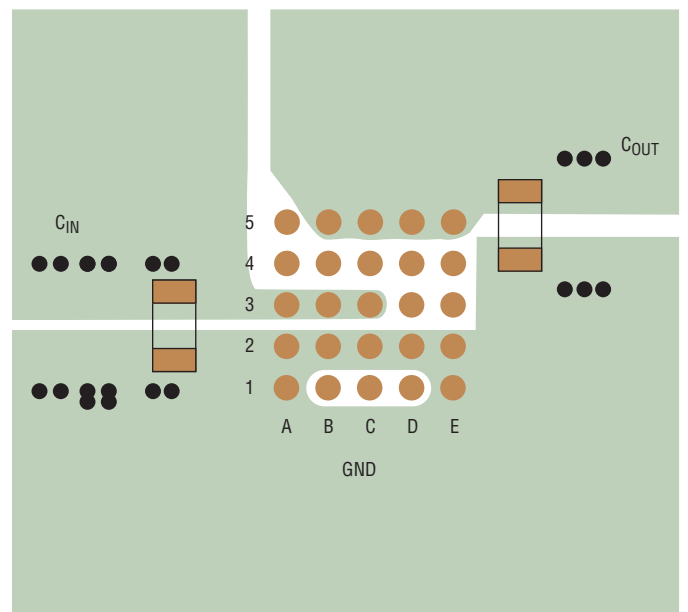
Layout Checklist/Example

The high integration of LTM4658 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN} , GND and V_{OUT} . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN} , GND and V_{OUT} pins as close as possible to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.

- Use a separated GND ground copper area for components connected to signal pins. Connect the AGND to GND underneath the unit.
- For parallel modules, tie the V_{OUT} , V_{FB} , and COMP pins together. Use an internal layer to closely connect these pins together. The SSTT pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 15 gives a good example of the recommended layout.



4658 F15

Figure 15. Recommended PCB Layout

TYPICAL APPLICATIONS

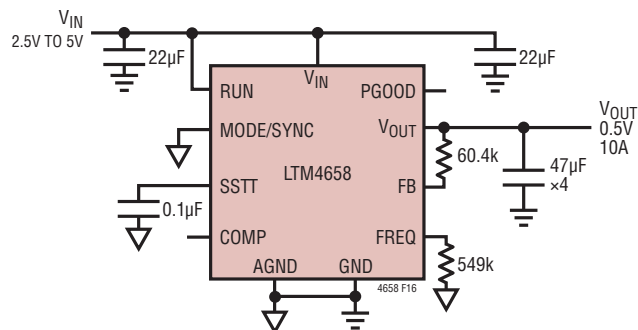


Figure 16. High Efficiency, 1MHz, 0.5V, 10A Forced Continuous Mode, Low Part Count

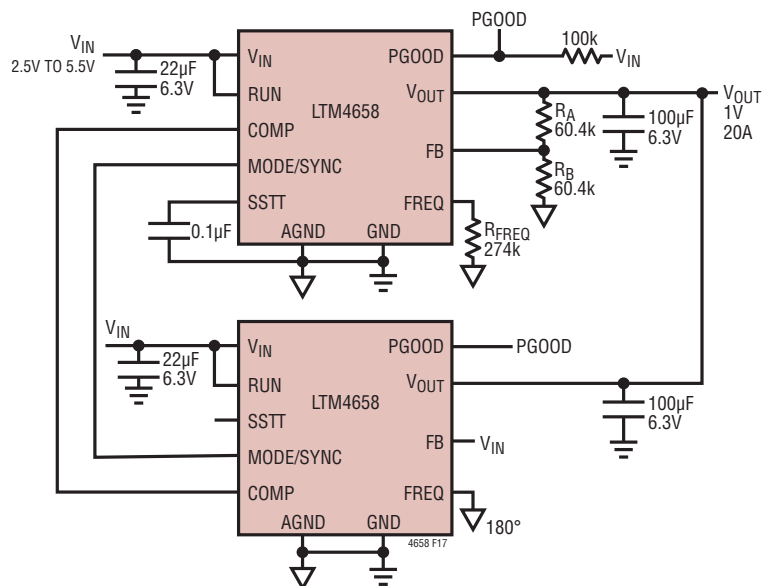


Figure 17. Dual-Phase Application with 180° Phase

TYPICAL APPLICATIONS

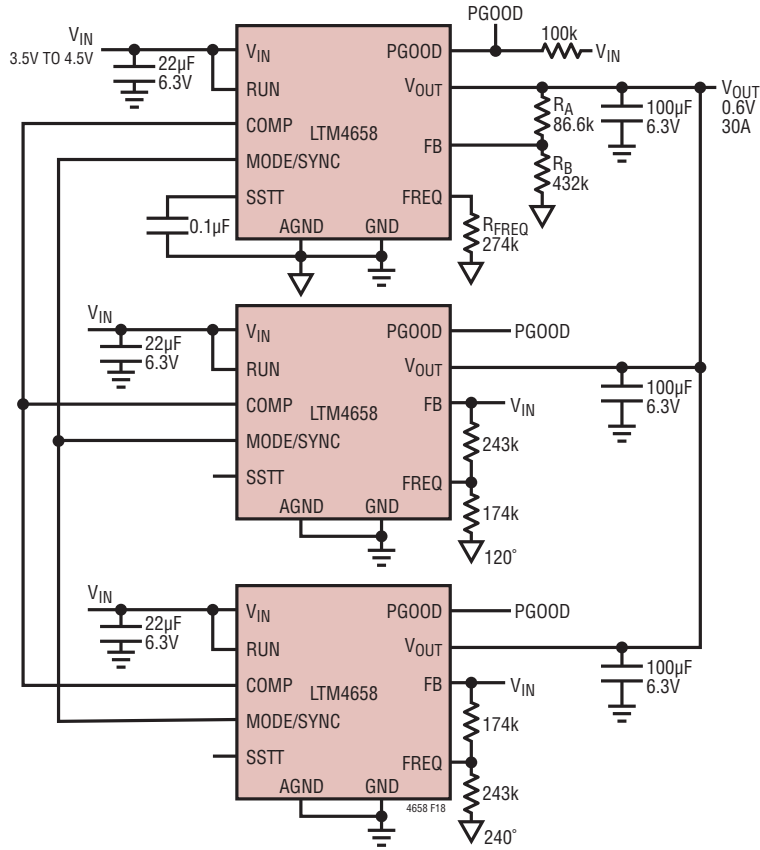


Figure 18. Three-Phase Application

TYPICAL APPLICATIONS

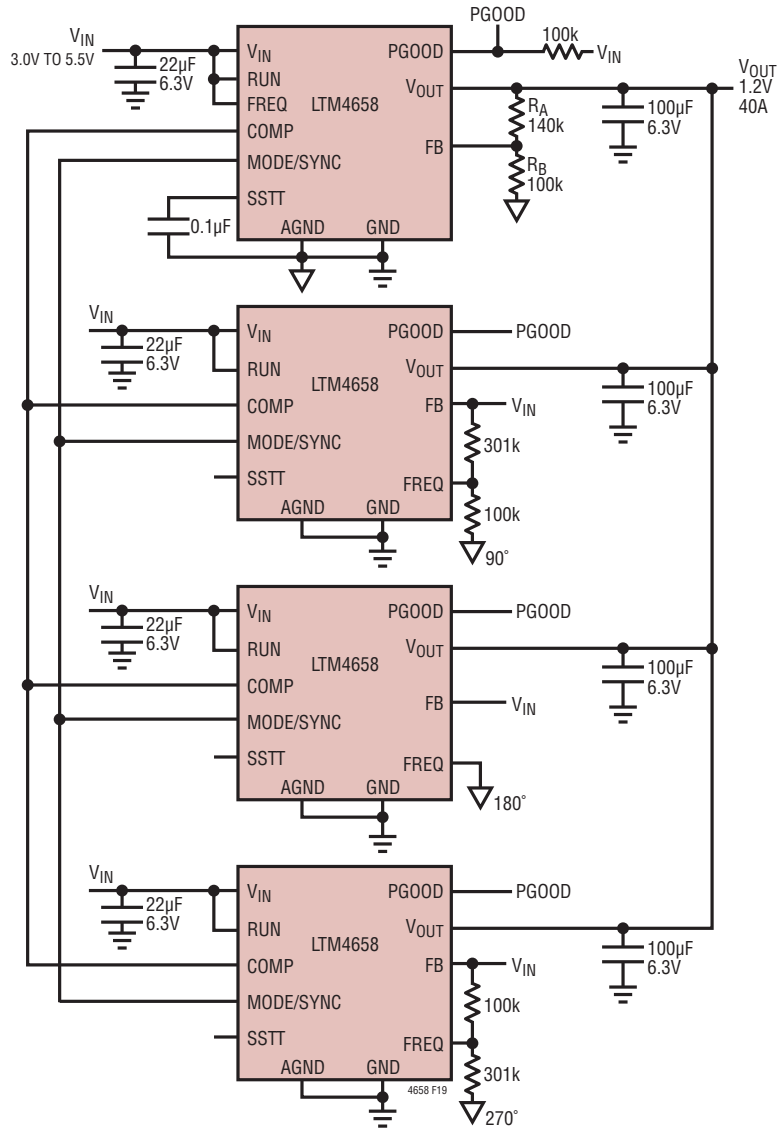


Figure 19. Four-Phase Application

PACKAGE DESCRIPTION



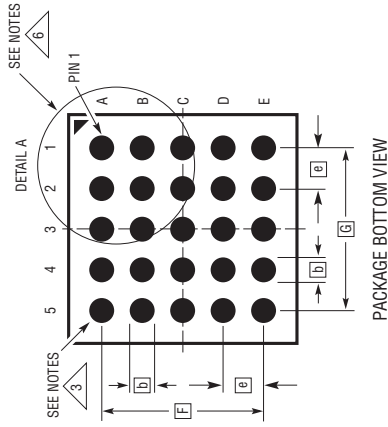
PACKAGE ROW AND COLUMN LABELING MAY VARY
AMONG μ Module PRODUCTS. REVIEW EACH PACKAGE
LAYOUT CAREFULLY.

Table 9. LTM4658 Component Pinout

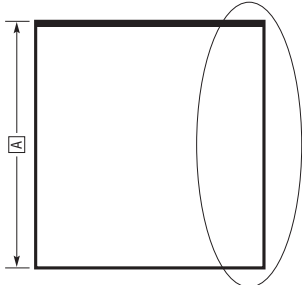
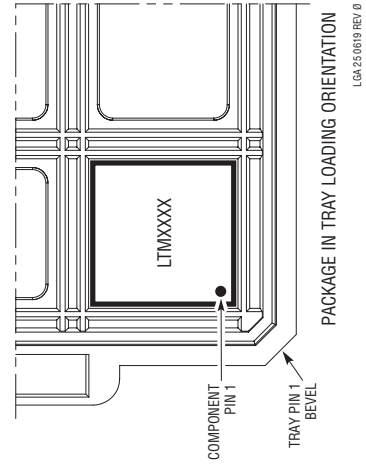
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	A2	GND	A3	V _{IN}	A4	COMP	A5	RUN
B1	SW	B2	GND	B3	V _{IN}	B4	FB	B5	V _{OUT}
C1	SW	C2	GND	C3	V _{IN}	C4	AGND	C5	V _{OUT}
D1	SW	D2	GND	D3	MODE/SYNC	D4	SSTT	D5	V _{OUT}
E1	GND	E2	GND	E3	PGOOD	E4	FREQ	E5	V _{OUT}

PACKAGE DESCRIPTION

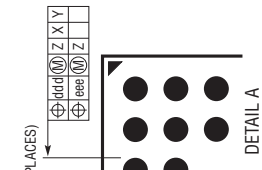
LGA Package
25-Lead (4mm × 4mm × 4.32mm)
 (Reference LTC DWG# 05-08-1830 Rev 0)



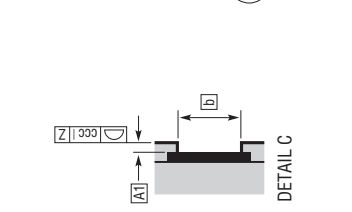
- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. ALL DIMENSIONS ARE IN MILLIMETERS
 3. LAND DESIGNATION PER JEP95
 4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
 5. PRIMARY DATUM -Z- IS SEATING PLANE
 6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG MODULE PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



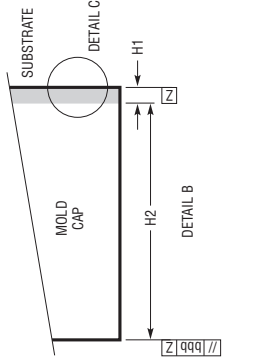
PACKAGE SIDE VIEW



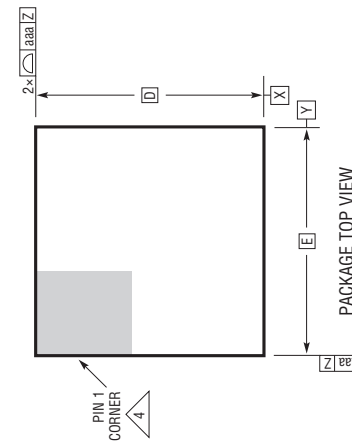
DIMENSIONS				NOTES
SYMBOL	MIN	NOM	MAX	
A	4.23	4.32	4.41	PAD DIMENSION
A1			0.03	
b	0.32	0.35	0.38	SUBSTRATE THK
D		4.00		
E		4.00		
e		0.65		
F		2.60		
G		2.60		MOLD CAP HT
H1		0.32 REF		
H2		4.00 REF		
aaa			0.15	
bbb			0.10	
ccc			0.10	
ddd			0.15	
eee			0.08	



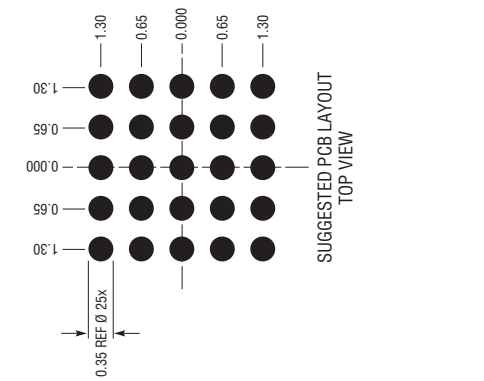
DETAIL C



DETAIL B



PACKAGE TOP VIEW

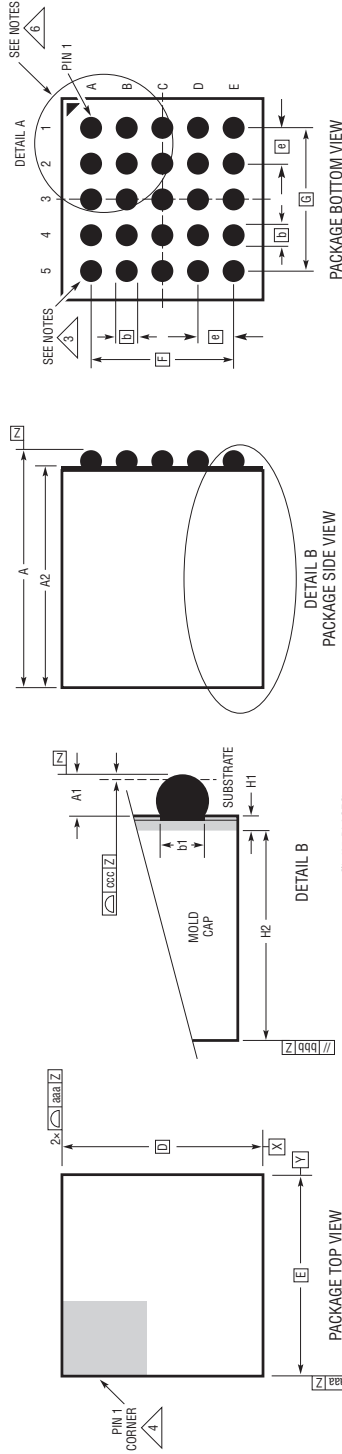


SUGGESTED PCB LAYOUT TOP VIEW

PACKAGE DESCRIPTION

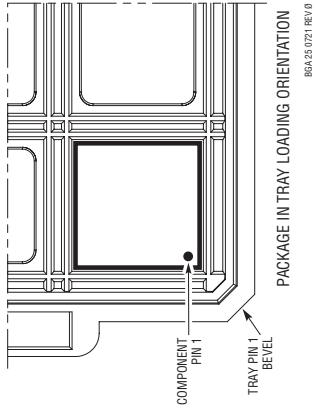
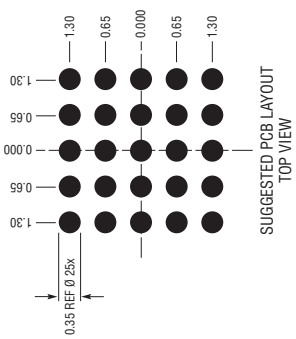


25-Ball Chip Scale Package Ball Grid Array [CSP_BGA] 4mm × 4mm × 4.62mm (BC-25-2)



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. ALL DIMENSIONS ARE IN MILLIMETERS
 3. LAND DESIGNATION PER JEP95
 4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
 5. PRIMARY DATUM -Z- IS SEATING PLANE
 6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG MODULE PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

SYMBOL	DIMENSIONS		NOTES
	MIN	NOM	
A	4.46	4.62	4.78
A1	0.23	0.30	0.37
A2	4.23	4.32	4.41
b	0.35	0.40	0.45
b1	0.32	0.35	0.38
D		4.00	
E		4.00	
e		0.65	
F		2.60	
G		2.60	
H1		0.32 REF	SUBSTRATE THK
H2		4.00 REF	MOLD CAP HT
aaa			0.15
bbb			0.10
ccc			0.10
ddd			0.15
eee			0.08
TOTAL NUMBER OF BALLS: 25			

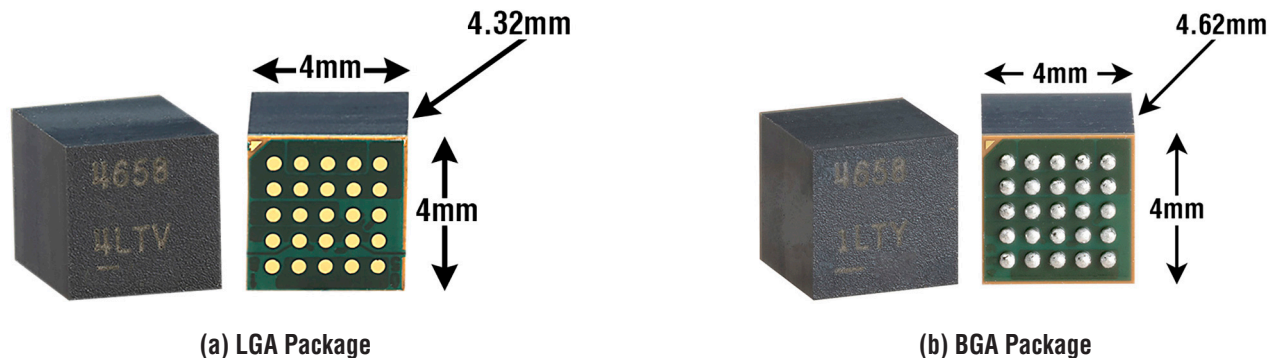


80A-25-071 REV 0

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/22	Changed master to main and slave to subordinate.	All
		Added BGA package option, updated peak reflow temperature.	2
		Added label on G11.	6
		Added pull-up voltage comment in Multiphase Operation section.	12
		Corrected Pin D4 to read SSTI.	24
		Updated Package Description.	26, 28
		Added ink marking statement to package photos.	28
B	9/23	Updated Order Information	2
		Updated in Electrical Characteristics (V_{RUN} parameter)	3
		Updated Setting the Operating Frequency section	11
		Updated Package Description	26

PACKAGE PHOTOS Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION
µModule Design and Manufacturing Resources	<p>Design:</p> <ul style="list-style-type: none"> • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools <p>Manufacturing:</p> <ul style="list-style-type: none"> • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	<ol style="list-style-type: none"> Sort table of products by parameters and download the result as a spread sheet. Search using the Quick Power Search parametric table. <div style="border: 1px solid #ccc; padding: 5px; margin-top: 10px;"> <p>Quick Power Search</p> <p>INPUT $V_{in}(\text{Min})$ <input type="text"/> V $V_{in}(\text{Max})$ <input type="text"/> V</p> <p>OUTPUT V_{out} <input type="text"/> V I_{out} <input type="text"/> A</p> <p>FEATURES <input type="checkbox"/> Low EMI <input type="checkbox"/> Ultrathin <input type="checkbox"/> Internal Heat Sink</p> <p style="text-align: center;">Multiple Outputs Search</p> </div>
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4670	Quad 10A Step-Down µModule Regulator	$2.25V \leq V_{IN} \leq 5.5V$, $0.5V \leq V_{OUT} \leq 5.5V$, 15mm × 7.50mm × 4.65mm BGA
LTM4691	Low V_{IN} , Ultrathin, Dual 2A Step-Down µModule Regulator	$2.25V \leq V_{IN} \leq 3.6V$, $0.5V \leq V_{OUT} \leq 2.5V$, 3mm × 4mm × 1.18mm LGA/BGA
LTM4668/ LTM4668A	Quad 1.2A Step-Down µModule Regulator	$2.7V \leq V_{IN} \leq 17V$, $0.6V \leq V_{OUT} \leq 1.8V$ (LTM4668A: $0.6V \leq V_{OUT} \leq 5.5V$, 2.25MHz) 6.25mm × 6.25mm × 2.1mm BGA
LTM4622	Ultrathin, Dual 2.5A or Single 5A Step-Down µModule Regulator	$3.6V \leq V_{IN} \leq 20V$, $0.6V \leq V_{OUT} \leq 5.5V$, 6.25mm × 6.25mm × 1.82mm LGA, 6.25mm × 6.25mm × 2.42mm BGA
LTM4626	12A µModule Regulator. Pin Compatible with LTM4657, LTM4638	$3.1V \leq V_{IN} \leq 20V$. $0.6V \leq V_{OUT} \leq 5.5V$, 6.25mm × 6.25mm × 3.87mm BGA
LTM4657	8A µModule Regulator. Pin Compatible with LTM4626, LTM4638	$3.1V \leq V_{IN} \leq 20V$, $0.5V \leq V_{OUT} \leq 5.5V$, 6.25mm × 6.25mm × 3.87mm BGA
LTM4638	15A µModule Regulator. Pin Compatible with LTM4657, LTM4626	$3.1V \leq V_{IN} \leq 20V$, $0.6V \leq V_{OUT} \leq 5.5V$, 6.25mm × 6.25mm × 5.02mm BGA
LTM4663	Ultrathin 1.5A µModule Thermoelectric Cooler (TEC) Regulator	$2.7V \leq V_{IN} \leq 5.5V$, 3.5mm × 4mm × 1.3mm LGA
LTM4693	Low V_{IN} , Ultrathin, 2A Buck-Boost µModule Regulator	$2.6V \leq V_{IN} \leq 5.5V$, $1.8V \leq V_{OUT} \leq 5.5V$, 3.5mm × 4mm × 1.25mm LGA