Click here to ask an associate for production status of specific part numbers.

MAX17615

4.25V to 60V, 250mA Current Limiter with OV, UV, Reverse Protection

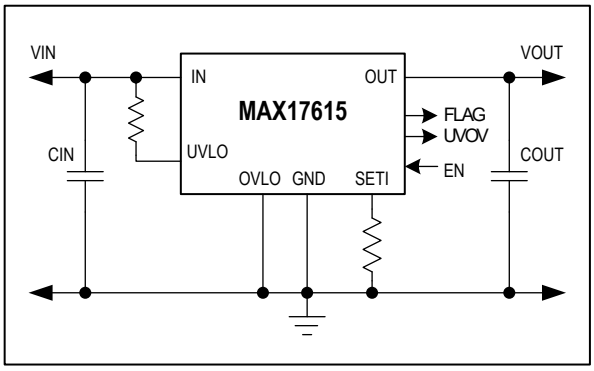
Product Highlights

- Robust Protection Reduces System Downtime
  - Wide Input Supply Range: +4.25V to +60V
  - Hot Plug-In Tolerant without TVS up to 35V Input Supply
  - Negative Input Tolerance to -65V
  - Negative Output Tolerance to -(65 - V_{IN})V
  - Low R_{ON} 1.42Ω (typ)
  - Reverse Current-Blocking Protection
  - Thermal Overload Protection
  - Extended -40°C to +125°C Temperature Range
- Flexible Design to Maximize Reuse and Minimize Requalification
  - Adjustable OVLO and UVLO Thresholds
  - Programmable Forward-Current Limit: 10mA to 20mA with ±6% Accuracy and 20mA to 250mA with ±5% Accuracy Over Full Temperature Range
  - Programmable Overcurrent Fault Response: Autoretry, Latch-Off, and Continuous Modes
  - Smooth Current-Transitions
- Reduced Solution Footprint
  - 10-Pin, 3mm x 3mm, TDFN Package
  - Integrated FETs

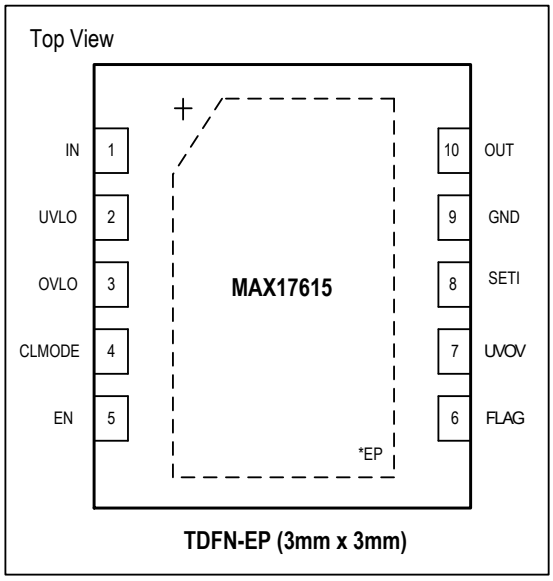
Key Applications

- Small Total Solution Size (Sensor Systems)
  Increased need for integrating more functionality in smaller form factors limits board space allocated for power and protection circuitry in factory automation and building automation applications. By integrating both forward and reverse MOSFETs, current sense, input/output reverse polarity protection, forward and reverse overcurrent protection, and UVLO/OVLO all into a single chip, the MAX17615 needs only 1/8th of the total solution size compared to solutions that use discrete components to implement the same protection features.
- Tight Current Limit Accuracy (Condition Monitoring, Battery Operated Modules)
  Battery operated electronics as well as battery chargers need tight current limit accuracy to protect against overcurrent faults. The MAX17615 with its ±5% tight current limit accuracy provides robust overcurrent protection in these applications.

Simplified Application Diagram



Pin Description



TDFN-EP (3mm x 3mm)

- Output Reverse Polarity Protection (Process Instrumentation, PLC, Network Modules)
  Factory automation applications that provide a 24V output to remote equipment are liable to experience a reverse polarity voltage applied across their output terminals due to cable wiring error. The MAX17615 offers robust protection for such scenarios and prevents expensive equipment failure and service costs.

See more *Who should use this part.*

***Ordering Information* appears at end of data sheet.**

19-101588; Rev 0; 8/22

Absolute Maximum Ratings

IN to GND ..... -65V to +65V

IN to OUT ..... -65V to +65V

OUT to GND ..... -65V to +65V

UVLO, OVLO to GND ..... -0.3V to MAX(V_{IN}, V_{OUT}) + 0.3V

$\overline{UVOV}$, $\overline{FLAG}$, EN, CLMODE to GND ..... -0.3V to +6.0V

IN Current (DC) 262.5mA

SETI to GND ..... -0.3V to 1.6V

Continuous Power Dissipation (10pin TDFN EP (T_A = +70°C, derate 24.4mW/°C above +70°C)) 1951.2mW

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature Range ..... -40°C to +150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10s) ..... +300°C

Note 1: SETI pin is internally clamped. Forcing more than 5mA current into the pin can damage the device.

Note 2: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 10 TDFN

Package Code	T1033+1C
Outline Number	*21-0137*
Land Pattern Number	*90-0003*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = +4.25 to +60V, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{IN} = +24V, T_A= +25°C, R_{SETI} = 1.2kΩ. (*Note 3*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Voltage Range	V_{IN}		4.25		60	V
Shutdown Input Current into IN pin	I_{SHDN}	V_{EN} = 0V		37	82	µA
Shutdown Output Current into OUT pin	I_{OFF}	V_{EN} = 0V, V_{OUT} = 0V			-5	µA
		V_{EN} = 0V, V_{OUT} = -60V, V_{IN} = 0V			-27	
Reverse Input Current into IN pin	I_{IN_RVS}	V_{IN} = -60V, V_{OUT} = 0V	-85	-50		µA
Reverse Shutdown Current into OUT pin	I_{OUT_RVS}	V_{IN} = 0V, V_{OUT} = +24V, V_{EN} = 0V		170	400	µA
Reverse Shutdown Current into IN pin		V_{IN} = 0V, V_{OUT} = +24V, V_{EN} = 0V, T_A= +25°C			-0.4	µA
Supply Current	I_{IN}	V_{IN} = +24V, V_{EN} = 5V		0.94	1.30	mA

(V_{IN} = +4.25 to +60V, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{IN} = +24V, T_A= +25°C, R_{SETI} = 1.2kΩ. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Undervoltage-Trip Level	$V_{INTUVLO}$	V_{IN} rising	4.080	4.160	4.225	V
		V_{IN} falling	3.950	4.000	4.100	
Undervoltage Threshold Level	V_{UVLOR}	V_{UVLO} rising	1.47	1.50	1.53	V
	V_{UVLOF}	V_{UVLO} falling	1.42	1.45	1.48	
Overvoltage Threshold Level	V_{OVLOR}	V_{OVLO} rising	1.47	1.50	1.53	V
	V_{OVLOF}	V_{OVLO} falling	1.42	1.45	1.48	
UVLO and OVLO Leakage Current	I_{LEAK}	V_{UVLO} = V_{OVLO} = 0 to 2V, T_A= +25°C	-100		100	nA
UVLO Adjustment Range		(Note 4)	4.25		59	V
OVLO Adjustment Range		(Note 4)	5.50		60	V
Internal POR	V_{PORR}	V_{IN} rising	3.3	3.7	4.0	V
	V_{PORF}	V_{IN} falling	3.1	3.5	3.8	
INTERNAL FET						
Internal FET On-Resistance	R_{ON}	I_{LOAD} = 100mA, V_{IN} > 8V		1.42	2.70	Ω
Current Limit Adjustment Range	I_{LIM}	(Note 5)	10		250	mA
Current Limit Accuracy		10mA < I_{LIM} < 20mA	-6		+6	%
		20mA ≤ I_{LIM} ≤ 250mA	-5		+5	
$\overline{FLAG}$ Assertion Drop-Voltage Threshold	V_{FA}	Increase (V_{IN} - V_{OUT}) drop until $\overline{FLAG}$ asserts, V_{IN} = +24V	430	500	570	mV
Reverse Current Blocking Slow-Threshold	V_{RIBS}	(V_{OUT} - V_{IN}), VIN = +24V	2	11	20	mV
Reverse Current Blocking Debounce Blanking Time	t_{DEBRIB}	V_{IN} = +24V	100	140	180	µs
Reverse Current-Blocking Powerup Blanking Time	t_{BLKRIB}		14.4	16.0	17.6	ms
Reverse Current-Blocking Fast Threshold	V_{RIBF}	(V_{OUT} - V_{IN}), V_{IN} = +24V	70	105	140	mV
Reverse Current-Blocking Fast Response Time	t_{RIB}	$I_{REVERSE}$ = 2.5A (Note 6)		150	230	ns
Reverse-Blocking Supply Current	I_{RBL}	Current into OUT when (V_{OUT} - V_{IN}) > 130mV		1.00	1.35	mA
SETI						
R_{SETI} x I_{LIM}	V_{RI}			1.5		V
Current-Mirror Output Ratio	C_{IRATIO}	10mA ≤ I_{OUT} ≤ 20mA	190	200	210	A/A
		20mA ≤ I_{OUT} ≤ 250mA	193	200	207	
Internal SETI Clamp		5mA into SETI	1.6		2.2	V
SETI Leakage Current		V_{SETI} = 1.6V, T_A= +25°C	-0.1		+0.1	µA
LOGIC INPUT						

(V_{IN} = +4.25 to +60V, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{IN} = +24V, T_A= +25°C, R_{SETI} = 1.2kΩ. (*Note 3*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN Input-Logic High	V_{IH}		1.4			V
EN Input-Logic Low	V_{IL}				0.4	V
EN Pullup Voltage		EN pin unconnected. V_{IN} = 60V		1.6	2.0	V
EN Input Current		V_{EN} = 5.5V		17	30	µA
EN Pullup Current		V_{EN} = 0.4V	1.0	3.0	8.0	µA
CLMODE Input-Logic High			2.0	3.8	4.9	V
CLMODE Input-Logic Low			0.15	0.60	0.95	V
CLMODE Pullup Input Current			8	10	12	µA
$\overline{FLAG}$, $\overline{UVOV}$ OUTPUT						
$\overline{FLAG}$, $\overline{UVOV}$ Output Logic-Low Voltage		I_{SINK} = 1mA			0.4	V
$\overline{FLAG}$, $\overline{UVOV}$ Output Leakage Current		V_{IN} = $V_{\overline{FLAG}}$ = $V_{\overline{UVOV}}$ = 5.5V. $\overline{FLAG}$ and $\overline{UVOV}$ pins are deasserted, T_A= +25°C			0.1	µA
TIMING CHARACTERISTICS						
Switch Turn-On Time	t_{ON_SWITCH}	R_{LOAD} = 1kΩ, C_{LOAD} = 0pF, V_{IN} = +24V		230	450	µs
Overvoltage Switch Turn-Off Time	t_{OFF_OVP}	V_{OVLO} exceeds V_{OVLOR} as a step; R_{LOAD} = 1kΩ, V_{IN} = +24V		1.0	1.3	µs
Overvoltage Falling Edge Debounce Time	t_{DEB_OVP}			20		µs
IN Debounce Time	t_{DEB}	From (V_{IN_UVLO} < V_{IN} < V_{IN_OVLO}) and EN = High, to V_{OUT} = 10% of V_{IN}. Elapses only at power-up.	14.4	16.0	17.6	ms
Current Limit Blanking Time	t_{BLANK}	(*Note 7*)	144	160	176	ms
Current Limit Autoretry Time	t_{RETRY}	After blanking time from I_{OUT} > I_{LIM} to $\overline{FLAG}$ deasserted. (*Note 8*)	1.08	1.20	1.32	s
THERMAL PROTECTION						
Thermal Shutdown Threshold	T_J			160		°C
Thermal Shutdown Hysteresis	$T_{J(HYS)}$			28		°C

Note 3: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design; not production tested.

Note 4: User settable. See the *Overvoltage Lockout (OVLO)* and *Undervoltage Lockout (UVLO)* sections for instructions.

Note 5: The current limit can be set below 10mA with a decreased accuracy.

Note 6: Guaranteed by design; not production tested.

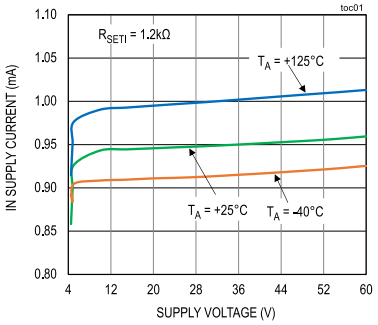
Note 7: During overload and short circuit conditions, the power dissipation in the device increases. The device enters thermal shutdown protection if the junction temperature exceeds thermal shutdown threshold (T_J).

Note 8: The ratio between autoretry time and blanking time is fixed and equal to 7.5.

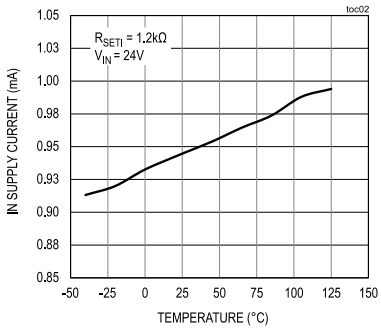
Typical Operating Characteristics

(C_{IN} = 0.47µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

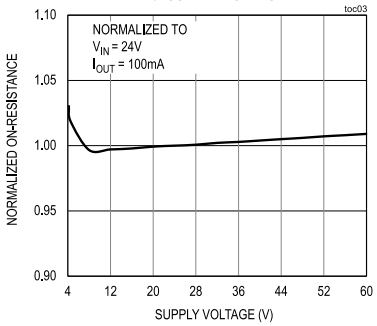
IN SUPPLY CURRENT vs. SUPPLY VOLTAGE



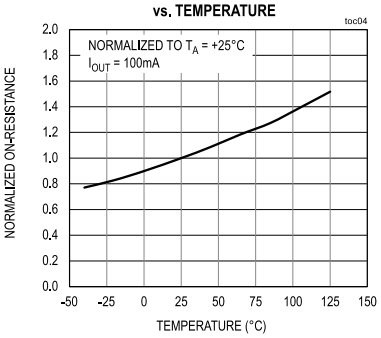
IN SUPPLY CURRENT vs. TEMPERATURE



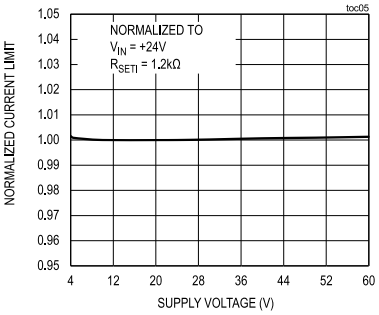
NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



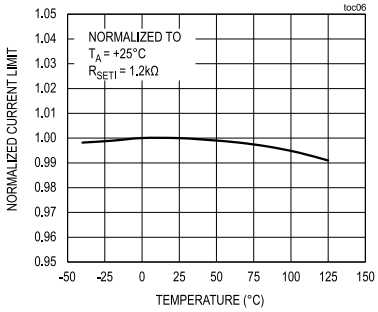
NORMALIZED ON-RESISTANCE vs. TEMPERATURE



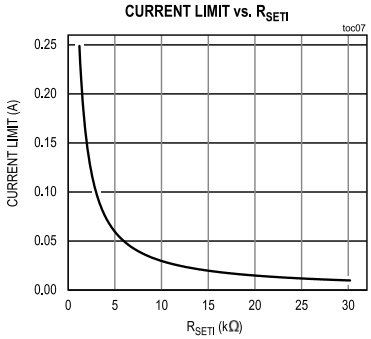
NORMALIZED CURRENT LIMIT vs. SUPPLY VOLTAGE



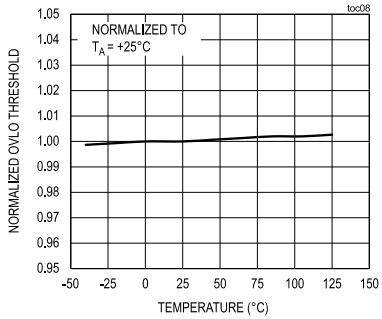
NORMALIZED CURRENT LIMIT vs. TEMPERATURE



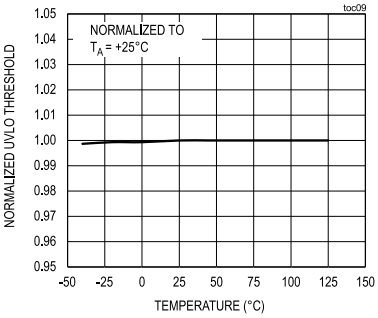
CURRENT LIMIT vs. R_{SETI}



NORMALIZED OVLO THRESHOLD vs. TEMPERATURE

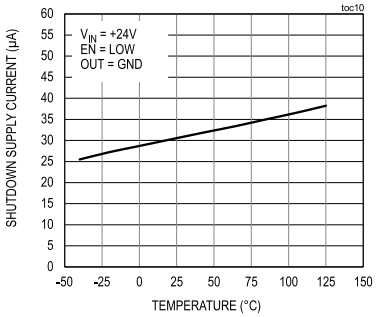


NORMALIZED UVLO THRESHOLD vs. TEMPERATURE

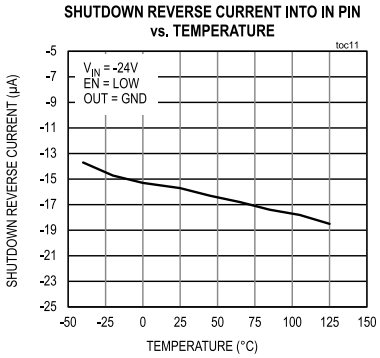


(C_{IN} = 0.47µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

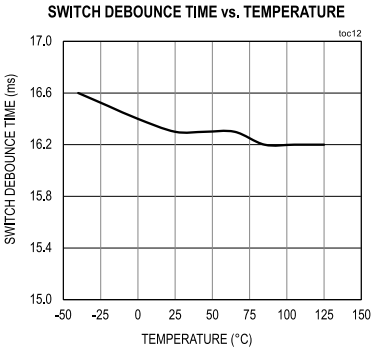
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



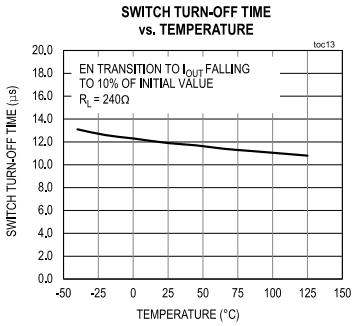
SHUTDOWN REVERSE CURRENT INTO IN PIN vs. TEMPERATURE



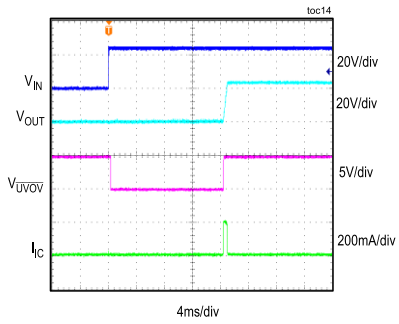
SWITCH DEBOUNCE TIME vs. TEMPERATURE



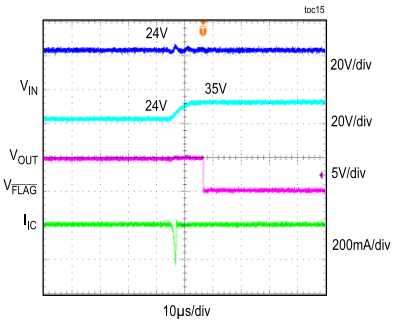
SWITCH TURN-OFF TIME vs. TEMPERATURE



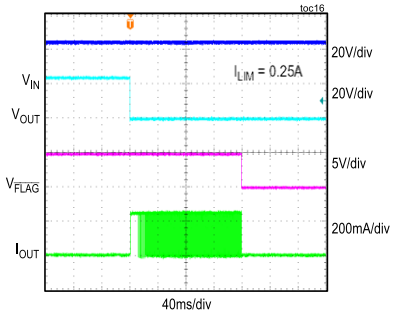
POWER-UP RESPONSE



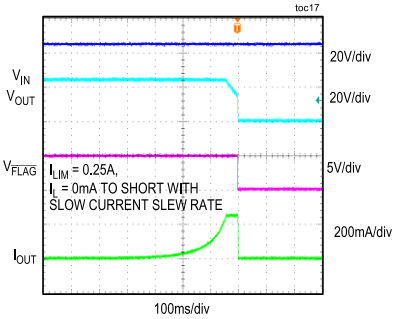
REVERSE-BLOCKING RESPONSE



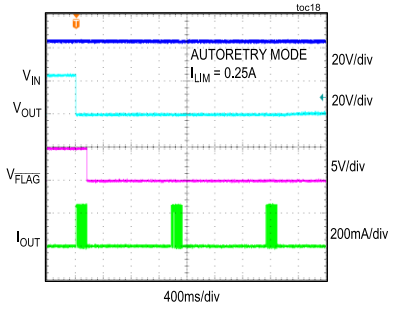
OUTPUT SHORT-CIRCUIT RESPONSE



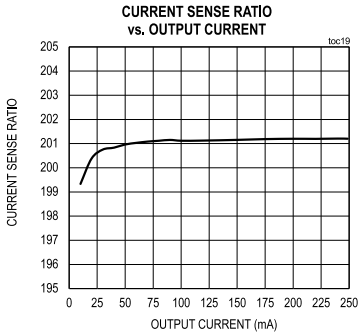
CURRENT-LIMIT RESPONSE

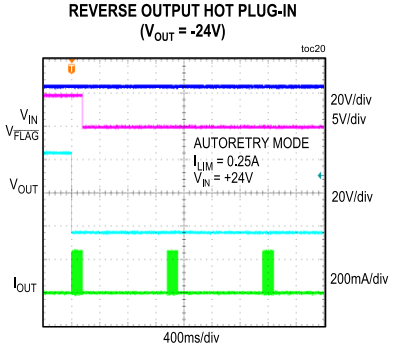


AUTORETRY TIME (t_{RETRY})

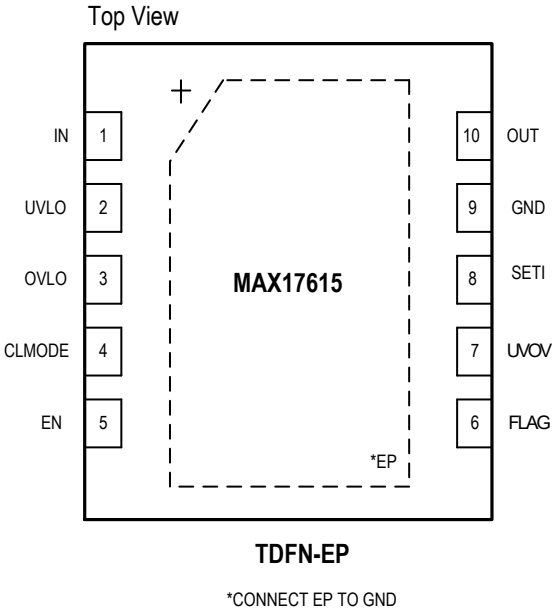


(C_{IN} = 0.47µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)





Pin Configuration



TDFN-EP

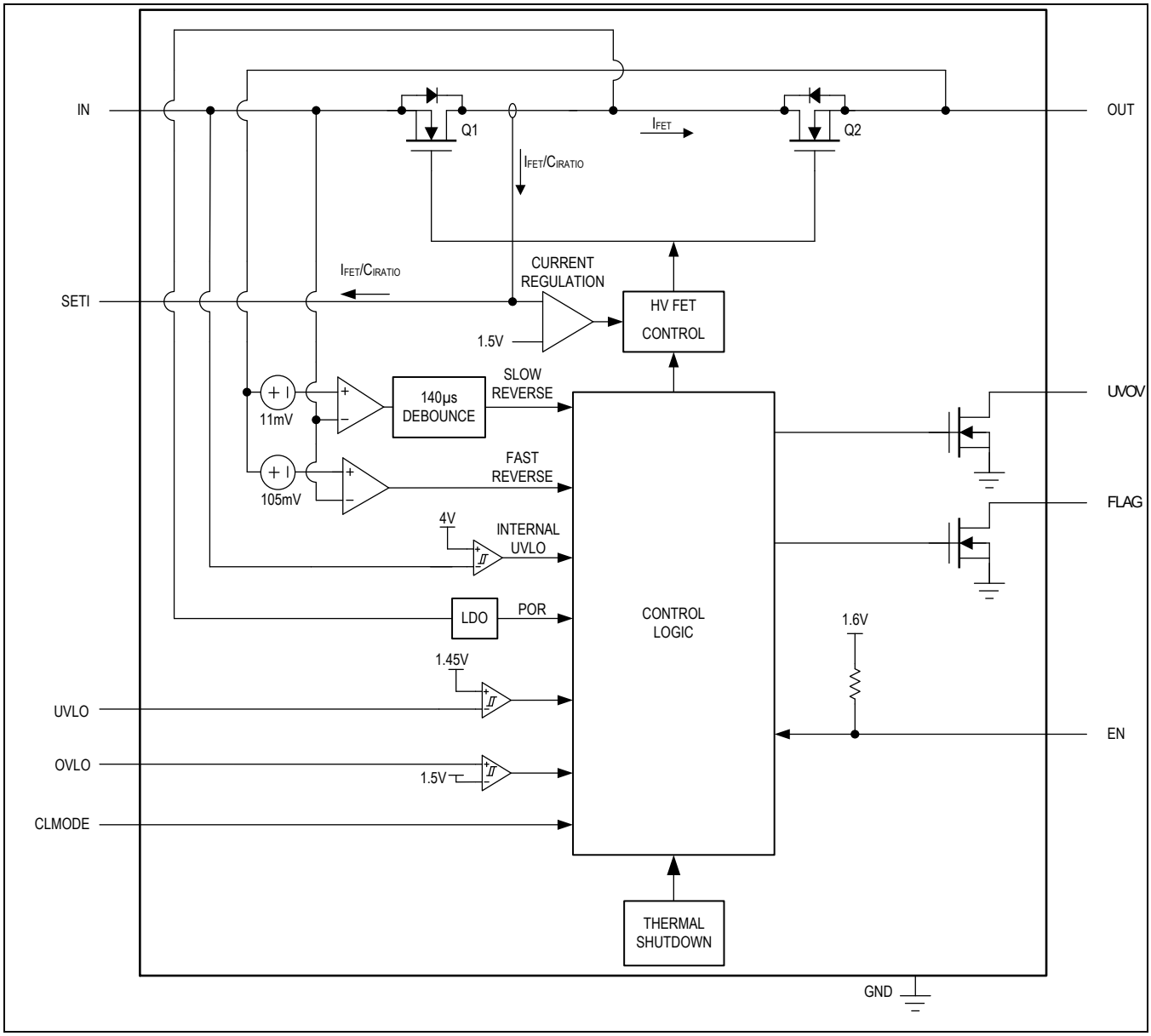
*CONNECT EP TO GND

Pin Description

PIN	NAME	FUNCTION
1	IN	Input Pin. Connect a low-ESR ceramic capacitor to GND. For hot plug-in applications, see the *Applications Information* section.
2	UVLO	UVLO Adjustment. Connect resistive potential divider from IN to GND to set the UVLO threshold.
3	OVLO	OVLO Adjustment. Connect resistive potential divider from IN to GND to set the OVLO threshold.
4	CLMODE	Current-Limit Mode Selector. Connect CLMODE to GND for Continuous mode. Connect a 150kΩ resistor between CLMODE and GND for Latch-off mode. Leave CLMODE unconnected for Autoretry mode.
5	EN	Active-High Enable Input. Internally pulled up to 1.6V.
6	$\overline{FLAG}$	Open-Drain, Fault Indicator Output. $\overline{FLAG}$ goes low when: • Overcurrent duration exceeds the blanking time. • Reverse current is detected. • R_{SETI} is less than 1kΩ (max). • Reverse polarity voltage is applied on OUT pin when voltage on IN pin is valid.
7	$\overline{UVOV}$	Open-Drain, Fault Indicator Output. $\overline{UVOV}$ goes low when: • Input voltage falls below UVLO falling threshold. • Input voltage rises above OVLO rising threshold.
8	SETI	Overcurrent Limit Adjustment Pin and Current Monitoring Output. Connect a resistor from SETI to GND to set overcurrent limit. See the Setting Current-Limit Threshold section. Do not connect more than 10pF to SETI.
9	GND	Ground.
10	OUT	Output Pin. For a long output cable or inductive load, see the *Applications Information* section.
—	EP	Exposed Pad. Connect EP to a large GND plane with several thermal vias for best thermal performance. Refer to the MAX17615 EV kit data sheet for a reference layout design.

Functional Diagram

MAX17615



Detailed Description

The MAX17615 overvoltage and overcurrent-protection device offers adjustable protection boundaries for systems against positive and negative input faults up to +60V and -65V, and output load current up to 250mA. The device features two internal MOSFETs connected in series with a low cumulative R_{ON} of 1.42Ω (typ).The device blocks out negative input voltages completely. The device withstands accidental reverse polarity output voltage connection, with magnitudes up to –(65 - V_{IN})V. Input undervoltage protection can be programmed between 4.25V and 59V, while the overvoltage protection can be independently programmed between 5.5V and 60V. Additionally, the device has an internal undervoltage lockout falling threshold set at 4V (typ).

The device is enabled or disabled through the EN pin by a master supervisory system. This in turn offers a switch operation to turn on or turn off power delivery to connected loads.

The current through the device is limited by setting a current limit, which is programmed by a resistor connected from SETI to GND. The current limit can be programmed between 10mA to 250mA. When the device current reaches or exceeds the set current limit, the on-resistance of the internal FETs are modulated to limit the current to set limit. The device offers three different behavioral modes when under current limited operations: Autoretry, Continuous, and Latch-Off modes. The SETI pin also presents a voltage with reference to GND, which under normal operation is proportional to the device current. The voltage appearing on the SETI pin might be read by an ADC in a monitoring system for recording instantaneous device current.

The MAX17615 offers $\overline{FLAG}$ and $\overline{UVOV}$ communication signals to indicate different operational and fault signals. The communication signal pins are open drain in nature and require external pullup resistors to appropriate system interface voltage.

MAX17615 blocks reverse current flow (from OUT to IN). The device offers internal thermal shutdown protection against excessive power dissipation.

Undervoltage Lockout (UVLO)

Connect an external resistive potential divider to the UVLO pin as shown in the Typical Operating Circuit to adjust the UVLO rising threshold. Use the following equation to adjust the UVLO threshold. The recommended value of R1 is 2.2MΩ.

$$V_{UVLO} = V_{UVLOR} \times \left[1 + \frac{R_1}{R_2}\right]$$

where

V_{UVLOR} is the UVLO rising threshold

V_{UVLO} is the input supply voltage at which the device exits the UVLO condition

When the voltage on the UVLO pin rises above V_{UVLOR}, the MAX17615 exits Undervoltage Lockout (UVLO) condition and turns ON. The device enters UVLO condition and turns OFF when the voltage on UVLO pin falls below V_{UVLOF}. The device also has a 4.16V (typ) internal UVLO rising threshold. The external resistor divider based UVLO setting should not be set lower than the internal UVLO rising threshold.

The MAX17615 has an internal power ON reset (POR) sensed at the middle of Q1 and Q2 FETs. The device turns off the internal FETs Q1 and Q2 when the IN pin voltage is below the internal POR falling threshold of 3.5V (typ). The $\overline{UVOV}$ pin is asserted high and the SETI pin is deactivated. When the IN pin voltage rises above the internal POR rising threshold of 3.7V (typ), the $\overline{UVOV}$ pin is asserted low and the SETI pin is activated. The internal FETs Q1 and Q2 remain turned off. The device also implements an internal UVLO sensed at the IN pin. The Q1 FET is turned on when the IN voltage rises above the internal UVLO rising threshold of 4.16V (typ). The Q2 FET is turned on after 16ms (t_{DEB}) from the instant IN voltage rises above the user defined external UVLO voltage rising threshold and the $\overline{UVOV}$ pin is asserted high.

Overvoltage Lockout (OVLO)

Connect an external resistive potential divider to the OVLO pin as shown in the Typical Operating Circuits to adjust the OVLO rising threshold. Use the following equation to adjust the OVLO threshold. The recommended value of R3 is 2.2MΩ.

$$V_{OVLO} = V_{OVLOR} \times \left[1 + \frac{R_3}{R_4}\right]$$

where V_{OVLOR} is the OVLO rising threshold

When the voltage on OVLO pin exceeds V_{OVLOR} for time equal to the overvoltage switch turn-off time (t_{OFF_OVP}), MAX17615 enters Overvoltage Lockout (OVLO) condition, turns OFF, and asserts $\overline{UVOV}$ low. When the OVLO condition is removed, the device takes the overvoltage falling-edge debounce time (t_{DEB_OVP}) to start the switch turn-on process. The switch turns back on after switch turn-on time (t_{ON_SWITCH}) and $\overline{UVOV}$ is asserted high. *Figure 1* depicts typical behavior in overvoltage condition.

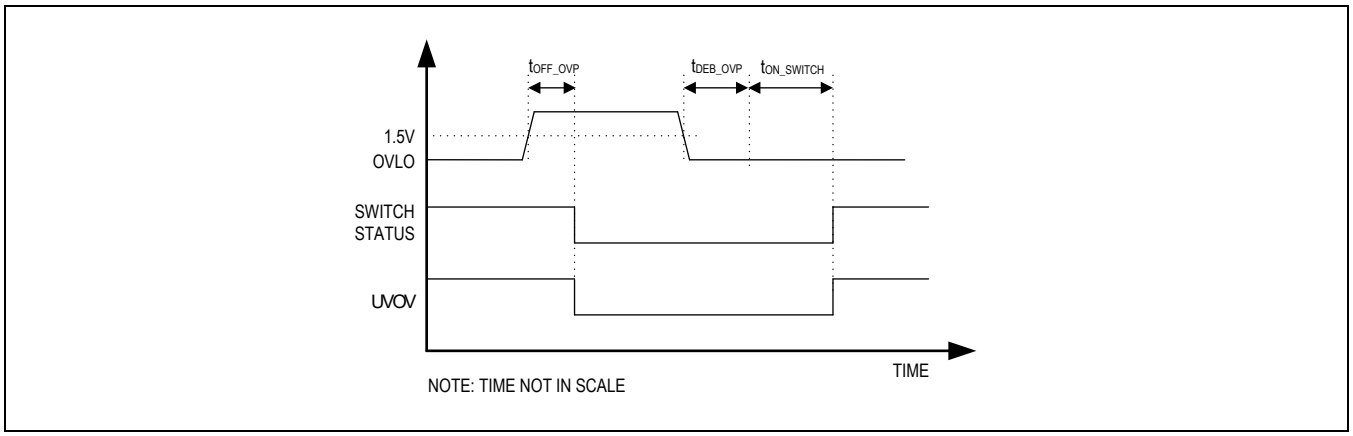


Figure 1. Overvoltage-Fault Timing Diagram

Input Voltage Reverse-Polarity Protection

The MAX17615 protects itself and downstream load circuits from accidental input voltage reverse-polarity conditions. In an input voltage reverse-polarity condition, the internal FETs remain off.

Output Voltage Reverse-Polarity Protection

The MAX17615 protects itself and input power supply connections from accidental output voltage reverse-polarity conditions. Reverse-polarity output voltage can appear across the OUT and GND pins due to miswiring of live load at the output terminals. If the device is enabled ($V_{EN} > V_{IH}$), the current at OUT is limited according to the current limit set by R_{SETI} resistor. If the device is in shutdown mode ($V_{EN} < V_{IL}$), the OUT current is limited to 27µA (max).

Input Debounce Protection

The device features input debounce protection. The device starts operation (turns on the internal FETs) only if the input voltage is higher than UVLO threshold for a period greater than the debounce time (t_{DEB}). The t_{DEB} elapses only at power-up of the device. This feature is intended for applications where the EN signal is present when the power supply ramps up. *Figure 2* depicts a typical debounce timing diagram.

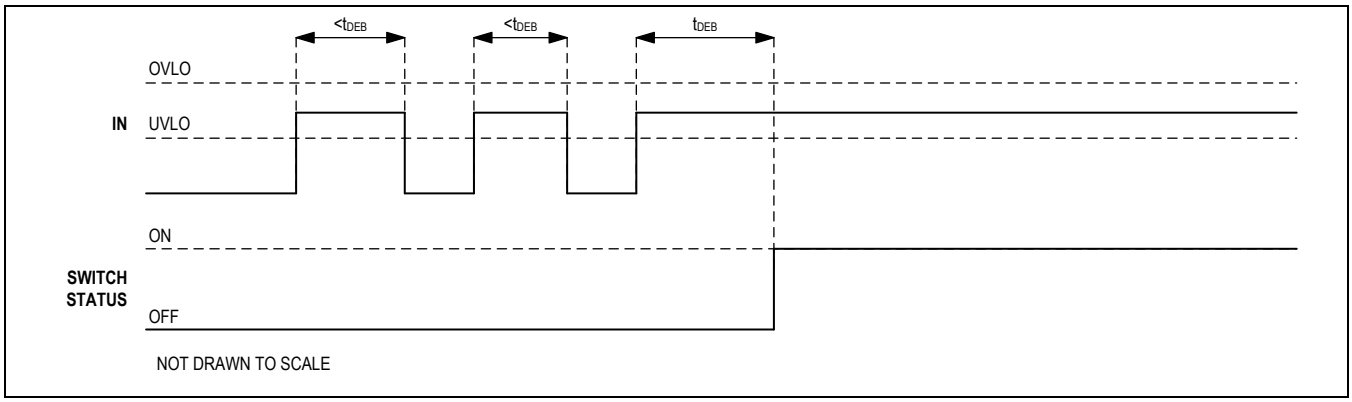


Figure 2. Debounce Timing Diagram

Enable

The MAX17615 is enabled or disabled through the EN pin by driving it above or below the EN threshold voltage; as such, the device can be used to turn power delivery to connected loads on or off using the EN pin. In Latch-Off Mode, toggling the EN pin for at least 15µs resets the fault condition and the device resumes operation. The EN pin is internally pulled up to 1.6V to have an always ON option when it is left open. Input debounce time (t_{DEB}) is present when the device is turned on through the EN pin.

Setting the Current Limit/Threshold

Connect a resistor between SETI and GND to program the current-limit threshold in the device. Use the following equation to calculate current-limit setting resistor:

$$R_{SETI}(k\Omega) = \frac{300}{I_{LIM}(mA)}$$

where I_{LIM} is the desired current limit in mA.

Do not use a R_{SETI} smaller than 1.2kΩ. *Table 1* shows current-limit thresholds for different resistor values.

The device features read-out of the current flowing into the IN pin. A current mirror with a ratio of C_{IRATIO} is implemented using a current-sense auto-zero operational amplifier. The mirrored current flows out of the SETI pin into the external current-limit resistor. The voltage on the SETI pin provides information about the IN current with the following relationship:

$$I_{IN-OUT}(A) = \frac{V_{SETI}(V)}{R_{SETI}(k\Omega)}$$

If SETI is left unconnected, V_{SETI} ≥ 1.5V. The Q2 FET is turned OFF and allows only a few µA current to flow due to internal circuitry. During startup, this causes the switches to remain off and $\overline{FLAG}$ to assert after t_{BLANK} elapses. During Startup, if R_{SETI} is lower than 350Ω, the switches remain off and $\overline{FLAG}$ asserts. For best damped measurement, the capacitance on the SETI pin should be limited to 10pF.

Table 1. Current-Limit Threshold vs. Resistor Values

R_{SETI} (kΩ)	CURRENT LIMIT (mA)
30	10
12	25
6	50
3	100
2	150
1.5	200
1.2	250

Current-Limit Type Select

The CLMODE pin is used to program the overcurrent response of the device in one of the following three modes: Autoretry mode (CLMODE pin is left unconnected), Continuous mode (CLMODE pin is connected to GND), and Latch-off mode (a 150kΩ resistor is connected between CLMODE and GND).

Autoretry Current Limit

In autoretry current-limit mode, when current through the device reaches the current-limit threshold, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ pin asserts if the overcurrent condition is present for more than t_{BLANK}. The timer resets if the overcurrent condition resolves before t_{BLANK} has elapsed. If the device enters thermal shutdown mode, the output Q2 FET turns off and it turns back on after the junction temperature cools down by $T_{J(HYS)}$. The thermal cycling continues until t_{BLANK} elapses. A retry time delay (t_{RETRY}) starts immediately after t_{BLANK} elapses. During the t_{RETRY} period, the switch remains off. Once t_{RETRY} has elapsed, the switch is turned back on again. If the fault still exists, the cycle is repeated and $\overline{FLAG}$ pin remains asserted. If the overcurrent condition is resolved, then the switch stays on.

The autoretry feature reduces system power in case of overcurrent or short-circuit conditions. When the switch is on during t_{BLANK} time, the supply current is held at the current limit. During t_{RETRY} time, there is no current through the switch. Thus, the average output current is much less than the programmed current limit. Calculate the average output current using the following equation:

$$I_{LOAD} = I_{LIM}\left[\frac{t_{BLANK}}{t_{RETRY} + t_{BLANK}}\right]$$

With a 160ms (typ) t_{BLANK} and 1200ms (typ) t_{RETRY}, the duty cycle is 11.8%, resulting in a 88.2% power reduction compared to the switch being on the entire time. *Figure 3* depicts typical behavior in the autoretry current-limit mode.

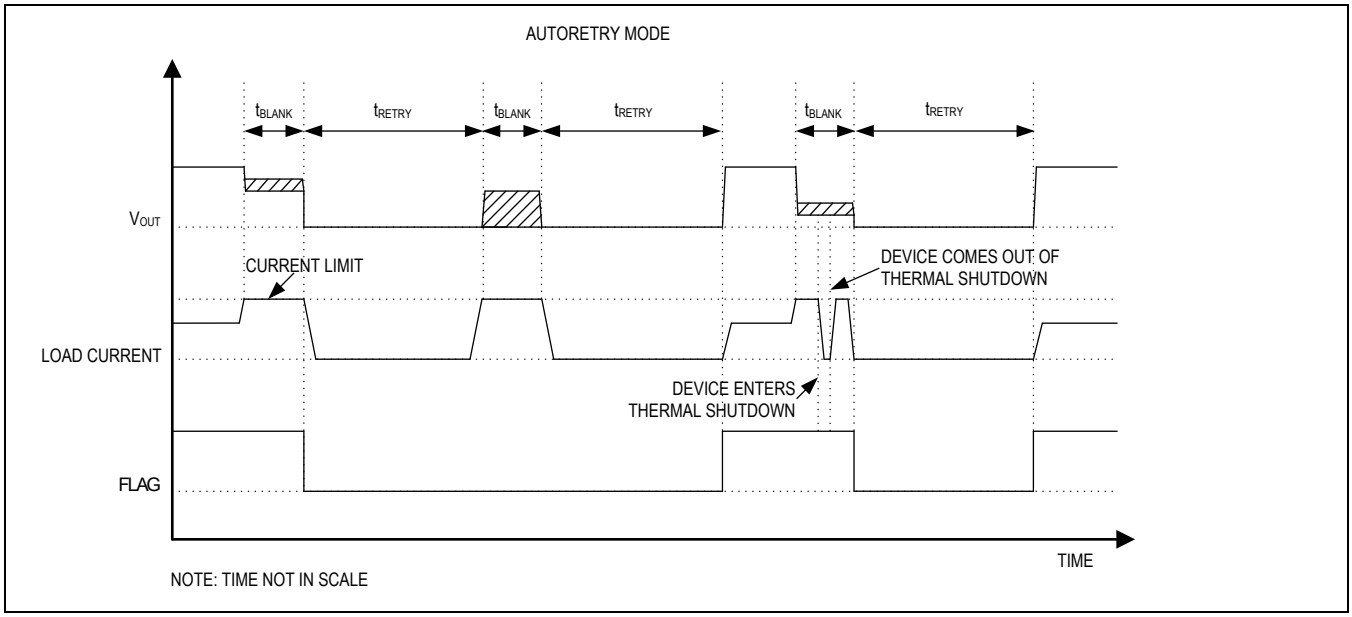


Figure 3. Autoretry Fault-Timing Diagram

Continuous Current Limit

In continuous current-limit mode, when current through the device reaches the current limit threshold, the device limits output current to the programmed current limit. If the device enters thermal shutdown mode, the output Q2 FET turns off and it turns back on after the junction temperature cools down by $T_{J(HYS)}$. The $\overline{FLAG}$ pin asserts if the overcurrent condition is present for a period more than t_{BLANK} and deasserts when the overcurrent condition is removed. *Figure 4* depicts typical behavior in the continuous current-limit mode.

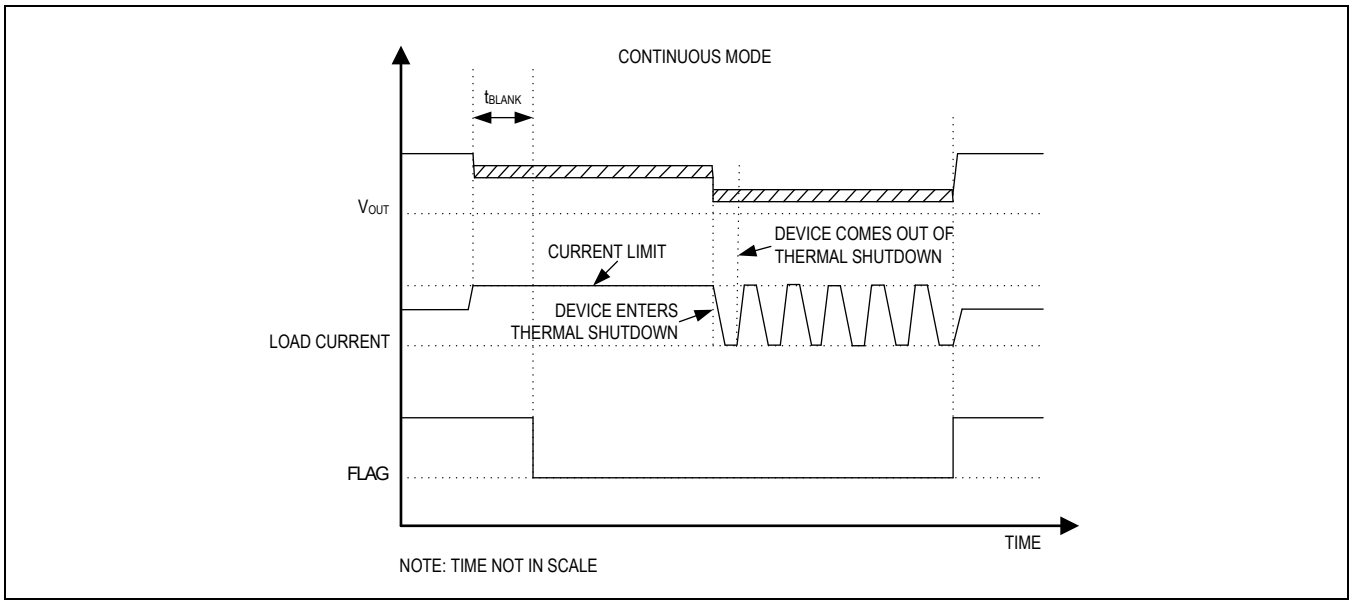


Figure 4. Continuous Fault-Timing Diagram

Latch-Off Current Limit

In latch-off current-limit mode, when current through the device reaches the current-limit threshold, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ pin asserts if an overcurrent condition is present for a period more than t_{BLANK}. The timer resets when the overcurrent condition disappears before t_{BLANK} has elapsed. If the device enters thermal shutdown mode, the output Q2 FET turns off and it turns back on after the junction temperature cools down by $T_{J(HYS)}$. The device turns off and stays off if the overcurrent condition continues beyond t_{BLANK}. To reset the device, either toggle the control logic (EN) or cycle the input voltage. *Figure 5* depicts typical behavior in latch-off current-limit mode.

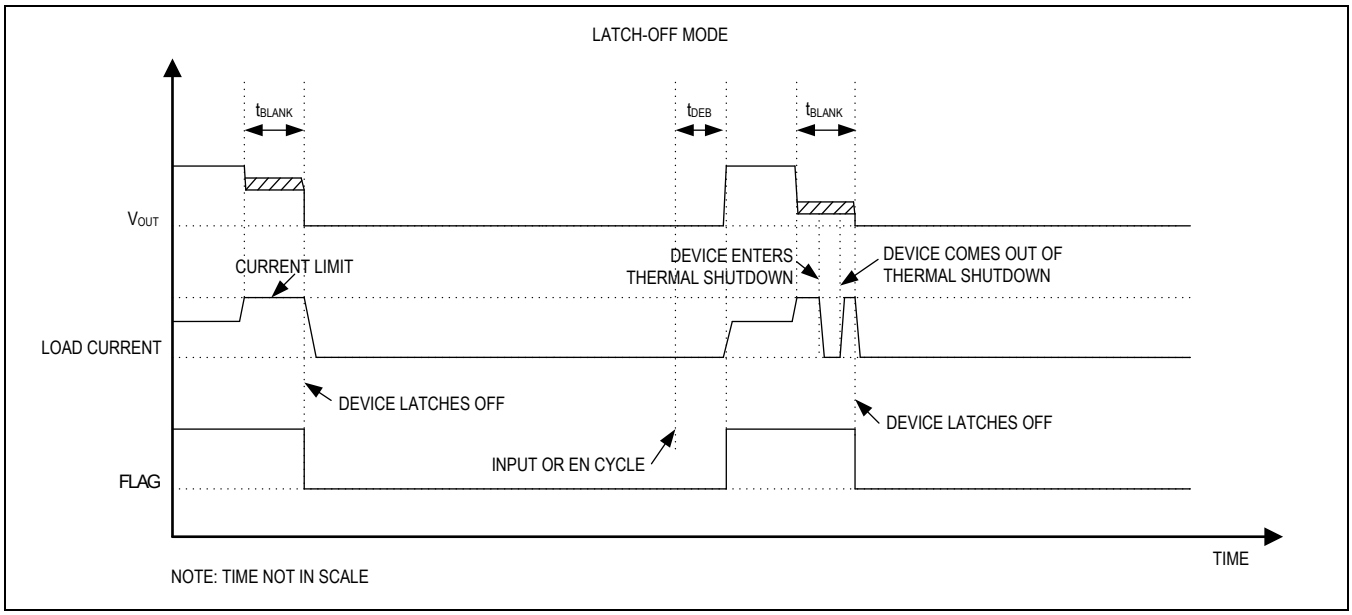


Figure 5. Latch-Off Fault-Timing Diagram

Short Circuit Protection

During a hard output short circuit event, the current through the device increases very rapidly. The device incorporates a fast-trip current comparator to limit the output short circuit peak current. The fast-trip current comparator turns off only the internal Q2 FET within 1µs (t_{DELAY1}), when the current through the FET exceeds I_{OCP}. The I_{OCP} is internally set to 300mA above the set current limit. After a time delay 100µs (t_{DELAY2}), the device turns back on and limits the output current to programmed current limit and operates as described in prior current limit mode sections. *Figure 6* illustrates the behavior of the system when the current exceeds the I_{OCP} threshold.

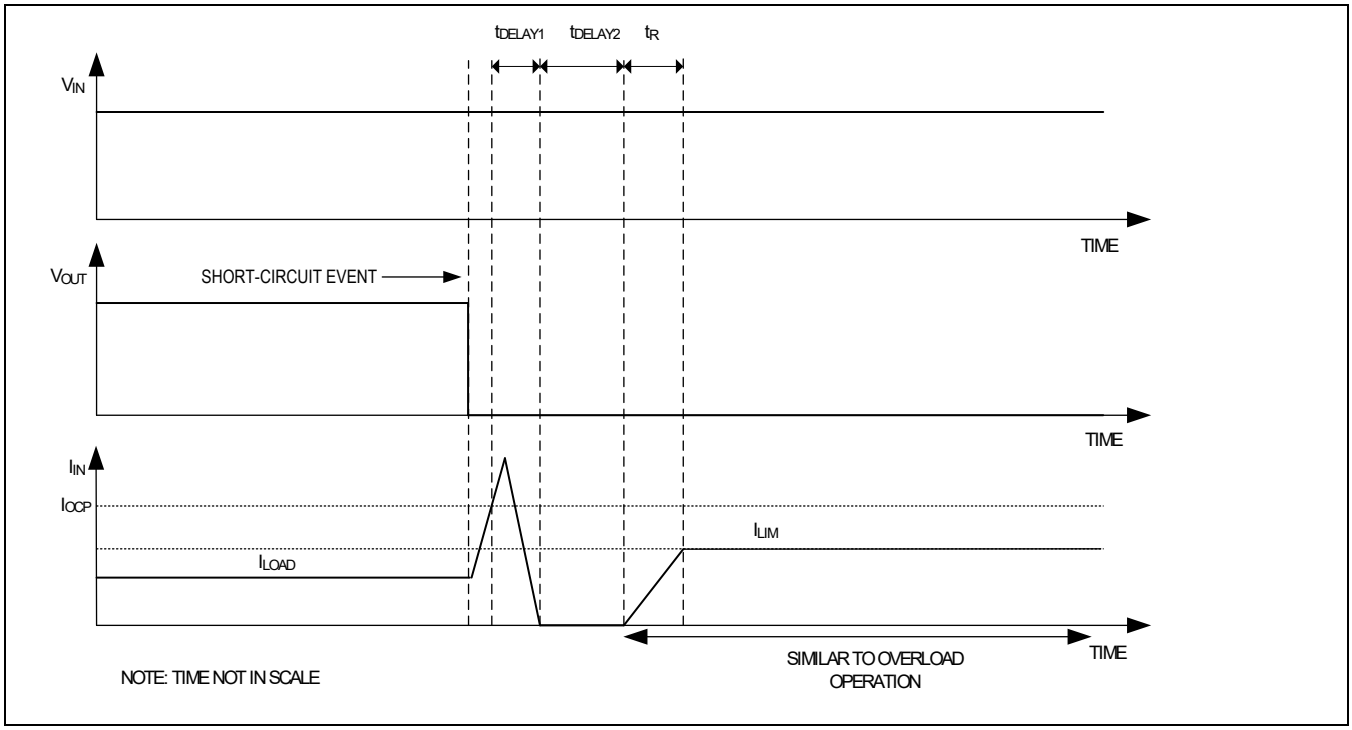


Figure 6. Fast Overcurrent Trip Timing Diagram

Reverse Current Protection

The MAX17615 prevents reverse current flow from the OUT pin to the IN pin. Two different reverse-current features are implemented.

A slow reverse-current condition is detected if (V_{IN} - V_{OUT}) < V_{RIBS} is present during reverse current-blocking debounce blanking time (t_{DEBRIB}). Only the input Q1 FET is turned off and the $\overline{FLAG}$ pin is asserted while the output Q2 FET is kept on. During and after this time, the device monitors the voltage difference between the OUT and IN pins to determine whether the reverse current is still present. Once the reverse current condition has been removed, Q1 FET is turned back on and the $\overline{FLAG}$ pin is deasserted. Q1 FET takes t_{Q1_ON} (~100µs) time to turn on. *Figure 7* depicts typical behavior in slow reverse current conditions.

A fast reverse-current condition is detected if (V_{IN} - V_{OUT}) < V_{RIBF} is present during reverse current blocking fast response time (t_{RIB}). Only the input Q1 FET is turned off and the $\overline{FLAG}$ pin is asserted while the output Q2 FET is kept on. During and after this time, the device monitors the voltage difference between the OUT and IN pins to determine whether the reverse current is still present. Once the reverse current condition has been removed, Q1 FET is turned back on and the $\overline{FLAG}$ pin is deasserted. Q1 FET takes t_{Q1_ON} (~100µs) time to turn on. *Figure 8* depicts typical behavior in fast reverse-current condition.

The device features two reverse-current thresholds with slow (<140µs) and fast (<150ns) response time for reverse current protection. The threshold for slow reverse protection is 11mV (typ), whereas it is 105mV (typ) for fast reverse. This feature results in robust operation in noisy environments, while still delivering fast protection under severe fault conditions such as input short-circuit or hot plug-in at the OUT pin.

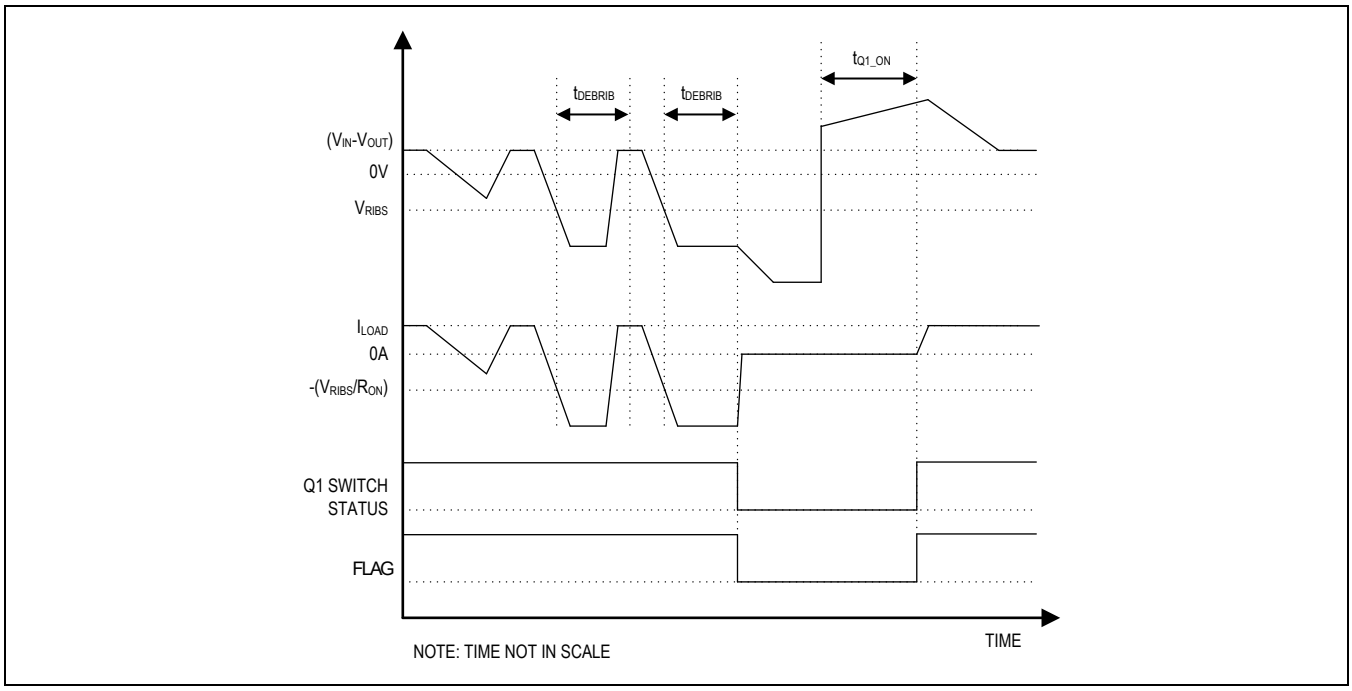


Figure 7. Slow Reverse-Current Fault-Timing Diagram

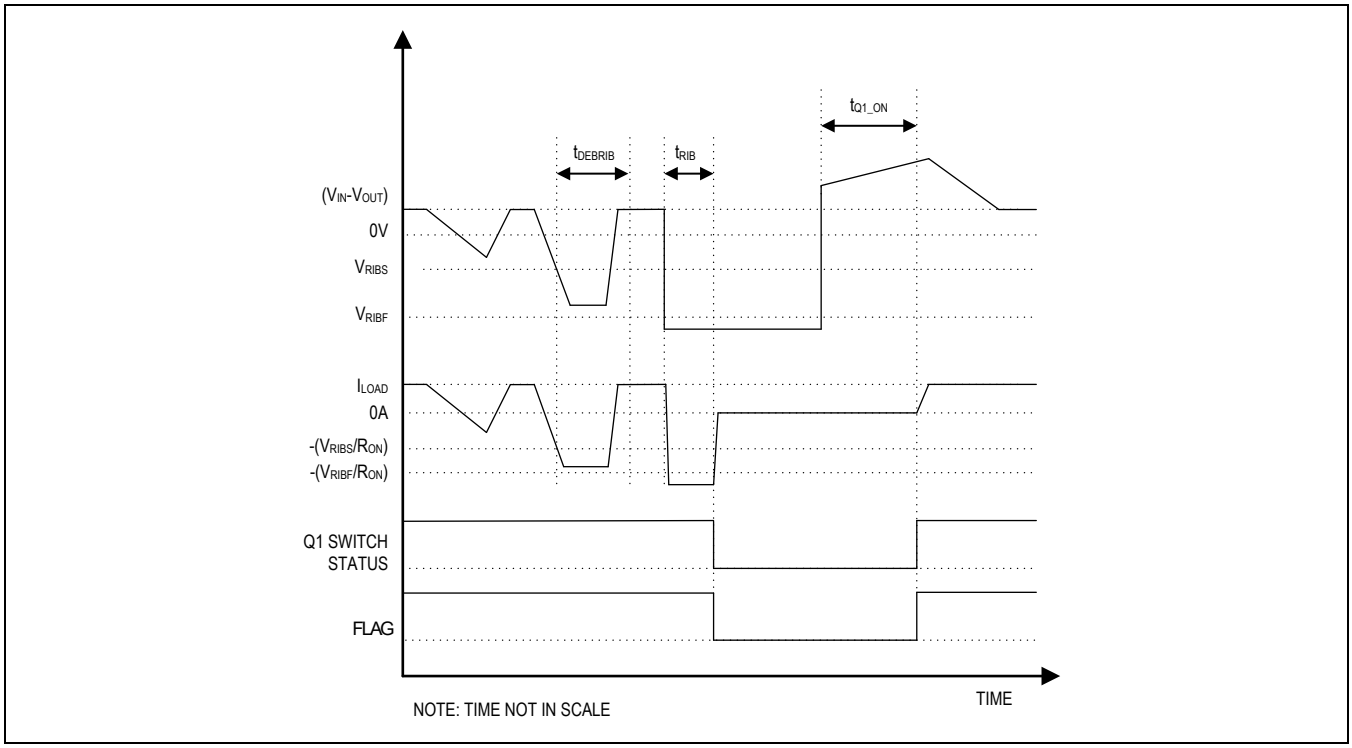


Figure 8. Fast Reverse-Current Fault-Timing Diagram

Fault Output

The device features two open-drain fault outputs, $\overline{FLAG}$ and $\overline{UVOV}$. They require external pullup resistors to a DC supply. The $\overline{FLAG}$ pin goes low when any of the following conditions occur:

- Overcurrent duration exceeds blanking time
- Reverse-current is detected
- R_{SETI} is less than 1kΩ (max)
- Reverse polarity on the OUT pin when the voltage on the IN pin is valid within the programmed UVLO and OVLO range

The $\overline{UVOV}$ fault output goes low when any of the following conditions occur:

- Input voltage falls below UVLO falling threshold
- Input voltage rises above OVLO rising threshold

During startup, the UVOV pin deasserts with a 16ms debounce time after the input voltage rises above the UVLO rising threshold.

Thermal Shutdown Protection

The device features a thermal shutdown function to protect itself against overheating. The device turns off when the junction temperature exceeds +160°C (typ). The device exits thermal shutdown and resumes normal operation after the junction temperature cools down by 28°C (typ).

Applications Information

IN Capacitor

A 0.47µF capacitor from the IN pin to GND is recommended to hold input voltage steady during sudden load-current changes.

Hot Plug-In at IN Terminal

In many system powering applications, an input-filtering capacitor is required to lower radiated emissions and enhance ESD capability. In hot plug-in applications, parasitic cable inductance along with the input capacitor causes overshoot and ringing when a live power cable is connected to the input terminal. This effect causes the protection device to experience almost twice the applied voltage. A transient voltage suppressor (TVS) is often used in industrial applications to protect the system from these conditions. A TVS that is capable of limiting surge voltage to maximum 60V should be placed close to the input terminal for enhanced protection. The maximum tolerated slew rate at the IN pin is 100V/µs.

Input Hard Short to Ground

In many system applications, input short-circuit protection is required. The device detects reverse current entering at the OUT pin and flowing out of the IN pin, and turns off the internal FETs. The magnitude of the reverse current depends on the inductance of input circuitry and any capacitance installed near the IN pin.

The device can be damaged in case V_{IN} goes so negative that (V_{OUT} - V_{IN}) > 60V.

OUT Capacitor

The maximum capacitive load (C_{MAX} in µF) that can be connected is a function of current-limit setting (I_{LIM} in mA), the blanking time (t_{BLANK} in ms), the input voltage (V_{IN} in V), and the programmed current limit mode.

In autoretry and latch-off current limit modes, C_{MAX} is calculated using the following relationship:

$$C_{MAX}(\mu F) = \frac{I_{LIM}(mA) \times t_{BLANK(TYP)}(ms)}{V_{IN}(V)}$$

For example, for V_{IN} = 24V, t_{BLANK} (typ) = 160ms, and I_{LIM} = 250mA, C_{MAX} is 1667µF.

In autoretry and latch-off current limit modes, output capacitor values in excess of C_{MAX} can trigger false overcurrent conditions. Note that the above expression assumes no load current is drawn. Any load current drawn would offset the capacitor charging current, which results in a longer charging period and thus the possibility of false overcurrent condition. Also, depending on the operating temperature and thermal impedance characteristics of the application PCB, the junction temperature might reach the thermal shutdown threshold (T_J) which causes the device to turn off the output Q2 FET and it turns back on after the junction temperature cools down by $T_{J(HYS)}$. In autoretry current limit mode, the thermal cycling continues until t_{BLANK} expires. t_{RETRY} starts immediately after t_{BLANK} elapses. During t_{RETRY} period, the switch remains off. Once t_{RETRY} has elapsed, the switch is turned back on again and continues charging the output capacitor. In latch-off current limit mode, the thermal cycling continues until t_{BLANK} expires. The device turns off and stays off until EN or input power is cycled.

In continuous current limit mode, larger output capacitors can be charged. Depending on the operating temperature and thermal impedance characteristics of the application PCB, if the junction temperature reaches the thermal shutdown threshold (T_J), the device operates in a cyclical manner with an operating junction temperature between the thermal shutdown hysteresis limits. Thus, continuous operation allows a large output capacitor to be charged.

Hot Plug-In at OUT Terminal

In some applications, there might be a possibility of applying a positive or negative external voltage at the OUT terminal of the device, with or without the presence of an input voltage. During these conditions, the device detects any reverse current entering at the OUT pin and flowing out of the IN pin and turns off the internal FETs. Parasitic cable inductance along with input and output capacitors cause overshoot and ringing when an external voltage is applied at the OUT terminal. This causes the protection device to see up to twice the applied voltage, which can damage the device. It is recommended to use voltage clamps such that the voltages at the pins do not exceed the *Absolute Maximum Ratings*. The maximum tolerated slew rate at OUT pin is 100V/µs.

OUT Clamping Diode for Inductive Hard Short to Ground

In applications that require protection from a sudden short to ground with an inductive load or a long cable, an output clamp is recommended. This clamp can be implemented with a TVS and a diode as shown in the *Typical Application Circuit*. This clamp is required to limit negative voltage spikes on the OUT pin due to the inductive kickback during an output shortcircuit event.

Layout and Thermal Dissipation

To optimize the switch response time to output short-circuit conditions, it is very important to keep all traces as short as possible to reduce the effect of undesirable parasitic inductance. Place input and output capacitors as close as possible to the device (no more than 5mm). IN and OUT must be connected with short, wide traces to the power bus. During normal operation, the power dissipation is small and the package temperature change is minimal.

Power dissipation under steady-state normal operation is calculated as:

$$P_{(SS)} = I_{OUT}^2 \times R_{ON}$$

See the *Electrical Characteristics* table and *Typical Operating Characteristics* for R_{ON} values at various operating temperatures.

If the output is continuously shorted to ground, the power dissipation is calculated as:

$$P = I_{OUT} \times V_{IN}$$

Attention must be given since the power dissipation during a short circuit fault condition can cause the device to reach the thermal-shutdown threshold. Thermal vias from the exposed pad to the ground plane are highly recommended to increase the system thermal capacitance while reducing the thermal resistance to the ambient.

In autoretry current-limit mode, the average power dissipation in the device is reduced as the device turns off during t_{RETRY} period. Power dissipation in the device is calculated using the following equation:

$$P_{(AVG)} = \frac{V_{IN} \times I_{OUT} \times t_{BLANK}}{t_{RETRY} + t_{BLANK}}$$

ESD Protection

The device is specified for ±15kV (Human body model (HBM) electrostatic discharge (ESD) model) ESD on IN when IN is bypassed to ground with a 0.47µF, low-ESR ceramic capacitor. No capacitor is required for ±2kV (HBM) (typ) ESD on IN. All the pins have a ±2kV (HBM) typical ESD protection. *Figure 9* shows the HBM, and *Figure 10* shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

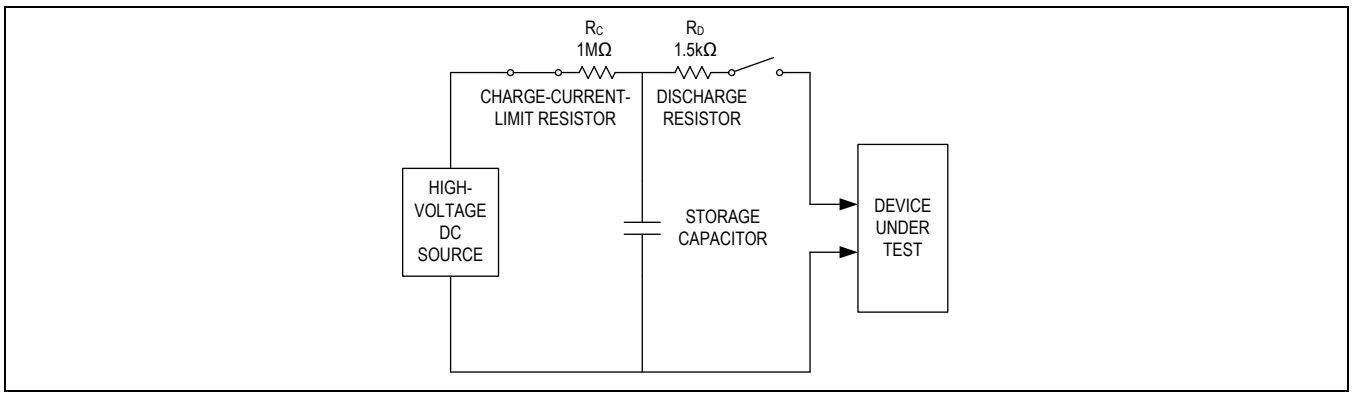


Figure 9. Human Body ESD Test Model

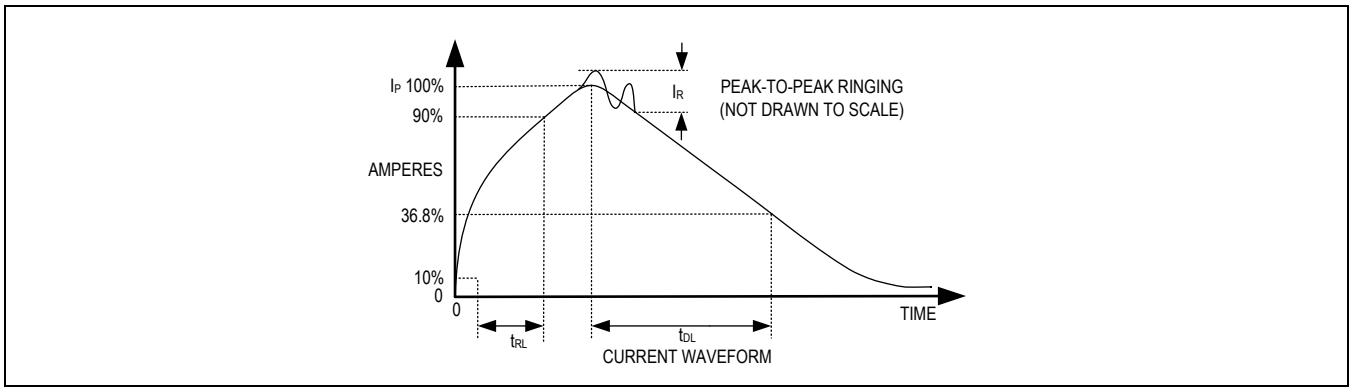
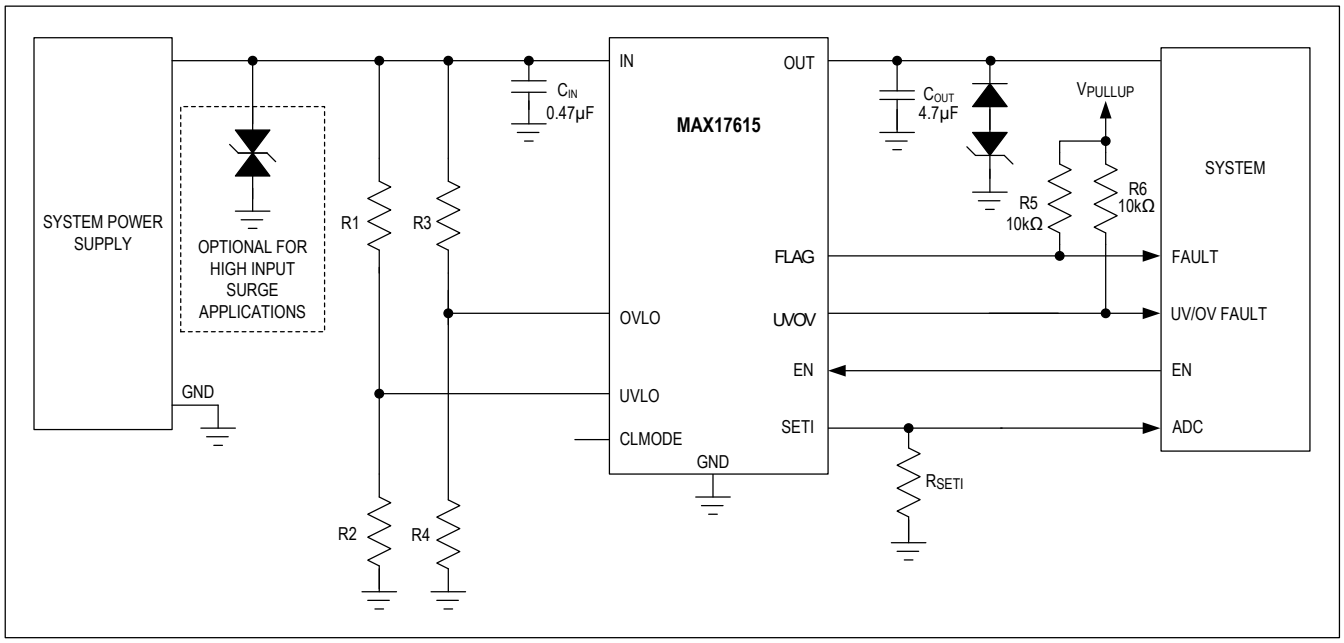


Figure 10. Human Body Current Waveform

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN PACKAGE
MAX17615ATB+	-40°C to +125°C	10 TDFN-EP*
MAX17615ATB+T	-40°C to +125°C	10 TDFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = tape and reel.

**EP = Exposed Pad*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/22	Release for Market Intro	—