MAX17690

60V, No-Opto Isolated Flyback Controller

General Description

The MAX17690 is a peak current mode, fixed-frequency switching controller specifically designed for the isolated flyback topology operating in Discontinuous Conduction Mode (DCM). The device senses the isolated output voltage directly from the primary-side flyback waveform during the off time of the primary switch. No auxiliary winding or optocoupler is required for output-voltage regulation.

The MAX17690 is designed to operate over a wide supply range from 4.5V to 60V. The switching frequency is programmable from 50kHz to 250kHz. A EN/UVLO pin allows the user to turn on/off the power supply precisely at the desired input voltage. The MAX17690 provides an input overvoltage protection through the OVI pin. The 7V internal LDO output of the MAX17690 makes it suitable for switching both logic-level and standard MOSFETs used in flyback converters. With 2A/4A source/sink currents, the MAX17690 is ideal for driving low $R_{DS(ON)}$ power MOSFETs with fast gate transition times. The MAX17690 provides an adjustable soft-start feature to limit the inrush current during startup.

The MAX17690 provides temperature compensation for the output diode forward voltage drop. The MAX17690 has robust hiccup-protection and thermal protection schemes, and is available in a space-saving 16-pin 3mm x 3mm TQFN package with a temperature range from -40°C to 125°C.

Benefits and Features

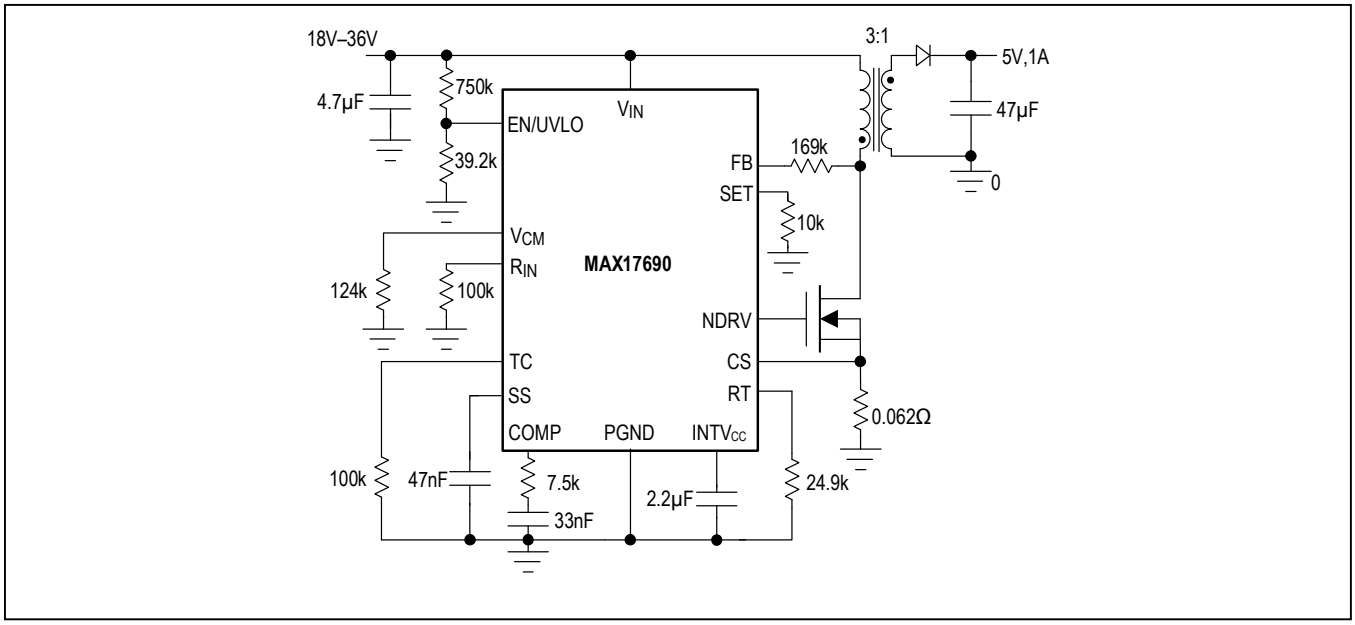
- 4.5V to 60V Input Voltage Range
- No Optocoupler or Third Winding Required to Derive Feedback Signal Across Isolation Boundary
- 2A/4A Peak Source/Sink Gate Drive Currents
- 50kHz to 250kHz Programmable Switching Frequency
- Input EN/UVLO Feature
- Input Overvoltage Protection
- Programmable Soft-Start
- Hiccup-Mode Short-Circuit Protection
- Thermal Shutdown Protection
- -40°C to 125°C Operating Temperature Range
- Space-Saving, 16-Pin 3 x 3 TQFN Package

Applications

- Isolated Flyback Converters
- Wide-Range DC-Input Isolated Power Supplies
- Industrial and Telecom Applications
- PLC I/O modules

Ordering Information **appears at end of data sheet.**

Application Circuit



maxim integrated™

Absolute Maximum Ratings

$INTV_{CC}$ to SGND .....-0.3V to +16V
V_{IN}, EN to SGND .....-0.3V to +70V
V_{IN} to FB .....-0.3V to +0.3V
OVI to SGND .....-0.3V to +6V
RIN, RT, V_{CM}, COMP, SS,
SET, TC and CS to SGND .....-0.3V to +6V
NDRV to PGND..... -0.3V to V_{INTVCC} + 0.3V

Continuous Power Dissipation (single-layer board)
(T_A = +70°C, derate 15.6mW/°C above +70°C).....1250mW
Continuous Power Dissipation (multilayer board)
(T_A = +70°C, Derate 20.8mW/°C above +70°C)....1666.7mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Single-Layer Board
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....64°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....7°C/W

Four-Layer Board
Junction-to-Ambient Thermal Resistance (θ_{JA}).....48°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 24V, $V_{EN/UVLO}$ = 2V, V_{OVI} = 0V, R_{RT} = 49.9kΩ, C_{INTVCC} = 2.2µF to GND; V_{PGND} = V_{SGND} = 0V, NDRV = SS = V_{CM} = COMP = OPEN, CS = GND, V_{IN} to FB = 0V, R_{SET} = 10kΩ, T_C = 27.5K, R_{IN} = 60kΩ,T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (V_{IN})						
V_{IN} Voltage Range	V_{IN}		4.5		60	V
Input Supply Shutdown Current	IIN_SH	$V_{EN/UVLO}$ = 0V (shutdown mode)		2.5	4	µA
		V_{IN} = 60V		3.5		µA
Input Switching Current	I_{SW}	No capacitor at NDRV		1.8		mA
ENABLE (EN/UVLO)						
EN/UNVO Threshold	V_{ENR}	V_{EN} rising	1.19	1.215	1.24	V
	V_{ENF}	V_{EN} falling	1.07	1.1	1.12	V
True Shutdown EN/UVLO Threshold	V_{ENSHDN}			0.7		V
EN/UVLO Input Leakage Current	I_{ENLKG}	$V_{EN/UVLO}$ = 2V, T_A = T_J = +25°C	-100		+100	nA
$INTV_{CC}$ LDO						
$INTV_{CC}$ Output Voltage Range	V_{INTVCC}	V_{IN} = 8V, 1mA ≤ I_{INTVCC} ≤ 25mA	6.65	7.0	7.35	V
		8V ≤ V_{IN} ≤ 60V, I_{INTVCC} = 1mA	6.65	7.0	7.35	V
$INTV_{CC}$ Current Limit	$I_{INTVCCMAX}$	V_{IN} = 8V, $INTV_{CC}$ = 6V	26	60		mA
$INTV_{CC}$ Dropout	$V_{INTVCC-DO}$	V_{IN} = 4.5V, I_{VCC} = 10mA	4.1			V
$INTV_{CC}$ ULVO	$V_{INTVCC-UVR}$	Rising	4.2	4.32	4.45	V
	$V_{INTVCC-UVF}$	Falling	3.9	4.03	4.15	V
OVI						
OVI Threshold	V_{OVIR}	V_{OVI} rising	1.19	1.215	1.24	V
	V_{OVIF}	V_{OVI} falling	1.07	1.1	1.12	V
OVI Input Leakage Current	I_{OVILKG}	V_{OVI} = 2V, T_A = T_J = +25°C	-100		+100	nA

Electrical Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = 2V, V_{OVI} = 0V, R_{RT} = 49.9kΩ, C_{INTVCC} = 2.2µF to GND; V_{PGND} = V_{SGND} = 0V, NDRV = SS = V_{CM} = COMP = OPEN, CS = GND, V_{IN} to FB = 0V, R_{SET} = 10kΩ, T_C = 27.5K, R_{IN} = 60kΩ,T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
NDRV						
RT Bias Voltage	V_{RT}			1.215		V
NDRV Switching Frequency Range	f_{SW}		50		250	kHz
NDRV Switching Frequency Accuracy			-6		+6	%
Maximum Duty Cycle			66	69	71	%
Minimum NDRV On-Time	T_{ON_MIN}			200	235	ns
Minimum NDRV Off-Time	T_{OFF_MIN}			430	490	ns
NDRV Pullup Resistance	R_{NDRV_P}	I_{NDRV} = 100mA (sourcing)		1.6	2.8	Ω
NDRV Pulldown Resistance	R_{NDRV_N}	I_{NDRV} = 100mA (sinking)		0.45	0.9	Ω
NDRV Peak Source Current	I-SOURCE			2		A
NDRV Peak Sink Current	I-SINK			4		A
NDRV Fall time	T_{NDRV_F}	C_{NDRV} = 3.3nF		11		ns
NDRV Rise Time	T_{NDRV_R}	C_{NDRV} = 3.3nF		16		ns
SOFT-START (SS)						
Soft-Start Charging current	I_{SS}	V_{SS} = 1V	4.75	5	5.25	µA
Soft-Start Done Threshold		V_{SS} rising		0.98		V
CURRENT SENSE (CS)						
Maximum CS Current-Limit Threshold	V_{CS_MAX}	V_{SET} = 0.8V	90	100	110	mv
Minimum CS Current-Limit Threshold	V_{CS_MIN}	V_{SET} = 1.2V		20		mv
CS Input Bias Current	I_{CS}	V_{CS} = 0V	7.5	10	13.5	µA
Runaway Current-Limit Threshold	$V_{CS\_RUNAWAY}$		108	120	132	mV
Overcurrent Hiccup Timeout		V_{SET} < 0.7V		16,384		cycles
SET						
SET Regulation Voltage	V_{SET}		0.988	1	1.012	V
SET Undervoltage Trip Level to Cause Hiccup	V_{SET_HICF}			0.7		V
TC						
TC Pin Bias Voltage	V_{TC}	T_A = T_J = +25°C		0.55		V
TC Current	I_{TC}	R_{TC} = 27.5kΩ		20		µA
COMP						
Error Amplifier Transconductance	Gm			1.6		mS

Electrical Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = 2V, V_{OVI} = 0V, R_{RT} = 49.9kΩ, C_{INTVCC} = 2.2µF to GND; V_{PGND} = V_{SGND} = 0V, NDRV = SS = V_{CM} = COMP = OPEN, CS = GND, V_{IN} to FB = 0V, R_{SET} = 10kΩ, T_C = 27.5K, R_{IN} = 60kΩ,T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

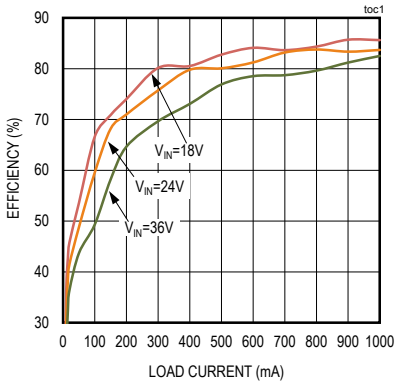
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
COMP Source Current	I_{COMP_SOURCE}	V_{COMP} = 2V and V_{SET} = 0.8V	95	136	190	µA
COMP Sink Current	I_{COMP_SINK}	V_{COMP} = 2V and V_{SET} = 1.2V	95	136	190	µA
MAX COMP Voltage	V_{COMPH}	R_{SET} = 8kΩ		2.9		V
MIN COMP Voltage	V_{COMPL}	R_{SET} = 12kΩ		1.55		V
COMP-to-CS Gain	ACS-PWM	ΔVCOMP/ΔVCS	10.0	10.3	10.7	V/V
V_{CM}						
V_{CM} Pullup Current		V_{CM} = GND	9.4	10	10.6	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	T_{SHDNR}	Temperature rising		+160		°C
Thermal-Shutdown Hysteresis	T_{SHDNHY}			+20		°C

Note 2: Limits are 100% tested at T_A = +25°C. Limits over the temperature range and relevant supply voltage range are guaranteed by design and characterization.

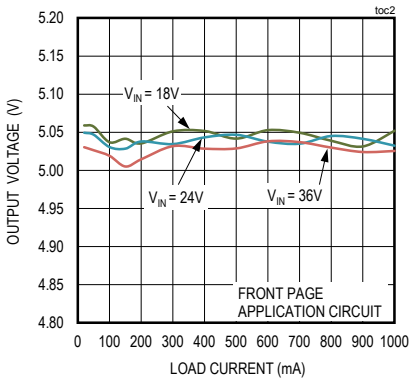
Typical Operating Characteristics

(V_{IN} = 24V, $V_{EN/UVLO}$ = +2V, V_{OVI} = SGND, C_{VIN} = 1uF, C_{INTVCC} = 2.2µF, T_A = +25°C, unless otherwise noted.)

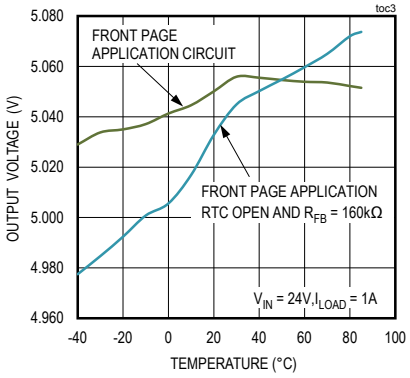
EFFICIENCY vs. LOAD CURRENT



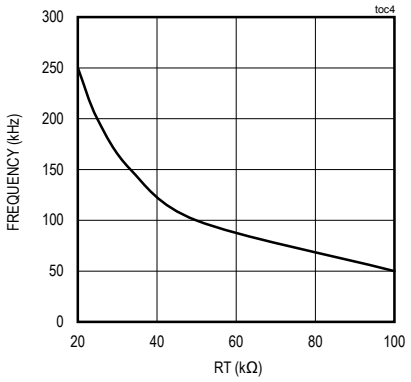
OUTPUT VOLTAGE vs. LOAD CURRENT



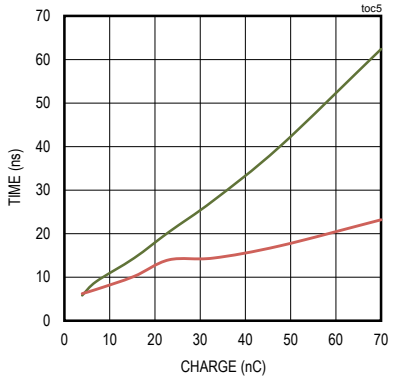
OUTPUT VOLTAGE vs. TEMPERATURE



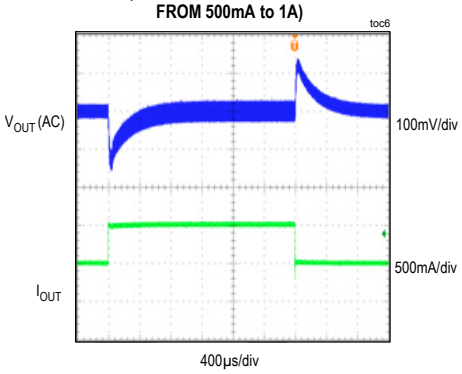
SWITCHING FREQUENCY vs. RT



CHARGE vs. NDRV RISE/FALL TIME



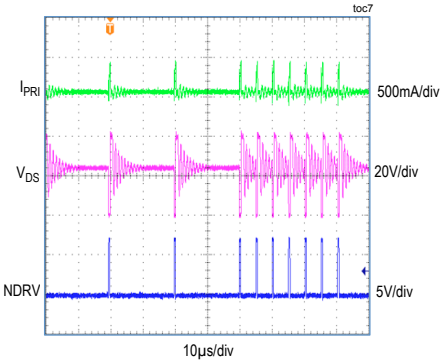
LOAD TRANSIENT RESPONSE (LOAD CURRENT STEPPED FROM 500mA to 1A)



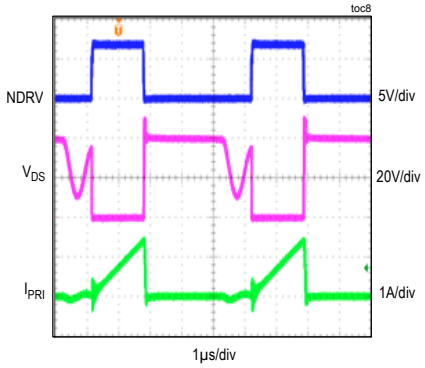
Typical Operating Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = +2V, V_{OVI} = SGND, C_{VIN} = 1uF, C_{INTVCC} = 2.2µF, T_A = +25°C, unless otherwise noted.)

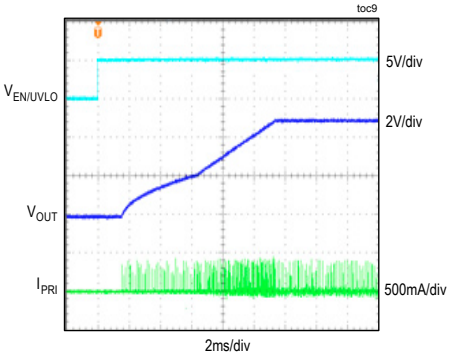
STEADY-STATE WAVEFORMS
LIGHT LOAD



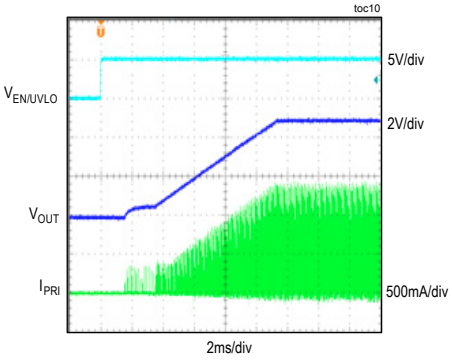
STEADY-STATE WAVEFORMS
FULL LOAD



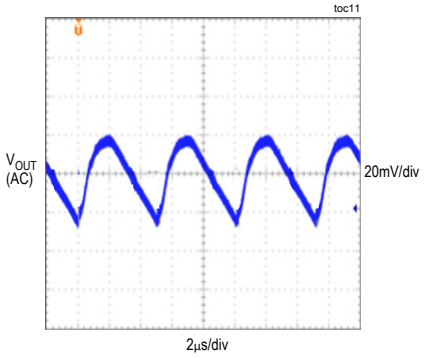
SOFT-START, LIGHT LOAD



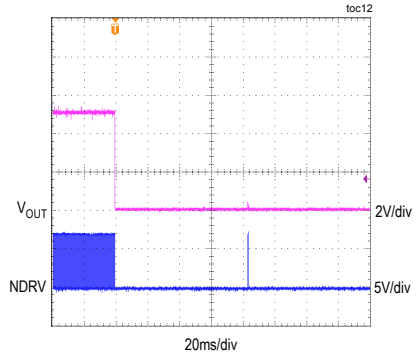
SOFT START, FULL LOAD



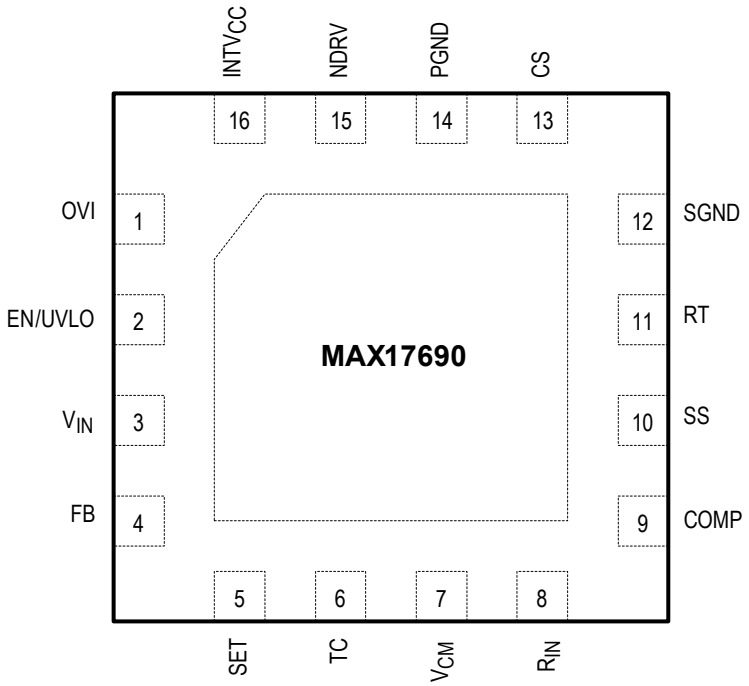
OUTPUT VOLTAGE RIPPLE
FULL LOAD



OVERLOAD PROTECTION



Pin Configuration



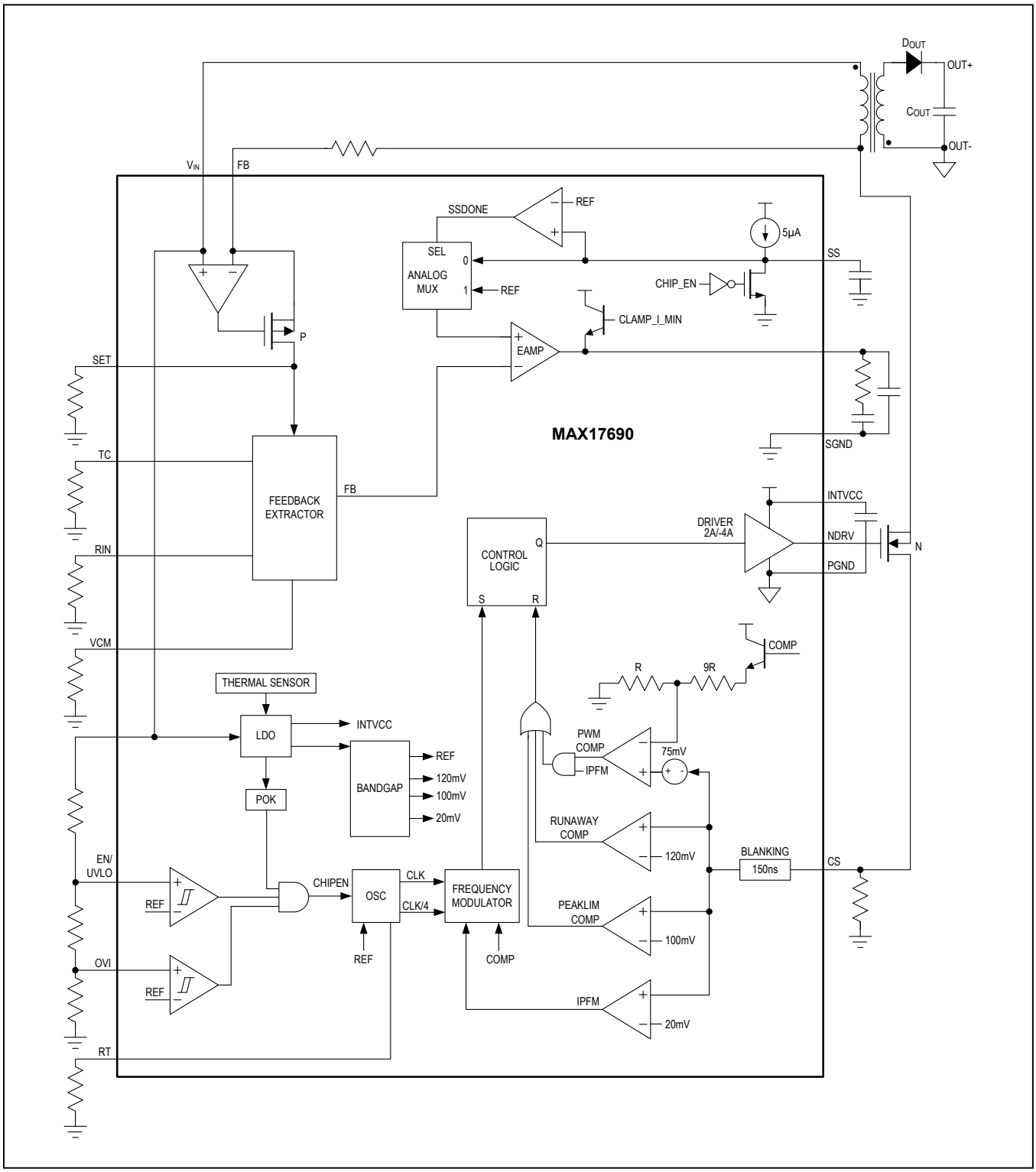
Pin Description

PIN	NAME	FUNCTION
1	OVI	Input Overvoltage Detection. Connect a resistive-divider between the input supply, OVI, and SGND to set the input overvoltage threshold. The MAX17690 stops switching when the voltage at the OVI pin exceeds 1.215V and resumes switching when the voltage at the OVI pin falls below 1.1V.
2	EN/UVLO	Input Voltage EN/UVLO. Connect a resistive-divider between the input supply, EN/UVLO, and SGND to set the input turn-on threshold. The MAX17690 starts switching when the voltage at the EN/UVLO pin exceeds 1.215V and stops switching when the voltage at the EN/UVLO pin falls below 1.1V.
3	V_{IN}	Input Supply Voltage. The input supply voltage range is 4.5V to 60V. This pin acts as a reference pin for the feedback circuitry connected to the FB pin. Connect a minimum of 1µF ceramic capacitor between the V_{IN} pin and SGND.
4	FB	Input for Deriving the Output Voltage Feedback During the Flyback Period. Connect a resistor R_{FB} between the primary MOSFET drain node and the FB pin to program the output voltage. The average current through this resistor during the flyback period should be approximately 100µA.
5	SET	Input for the External Ground-Referred Reference Resistor. Connect a 10kΩ resistor from the SET pin to SGND and place as close as possible to the MAX17690 IC.
6	TC	Output Voltage Temperature Compensation. Connect the resistor RTC from the TC pin to SGND to set the temperature compensation. Current through TC pin is given by $0.55/R_{TC}$.
7	V_{CM}	Common-Mode Voltage Selector for Internal Zero Current Detector Block. Connect a resistor R_{CM} from the V_{CM} pin to SGND. See the *Selection of VCM Resistor* section for selecting an appropriate R_{CM} resistor.

Pin Description (continued)

PIN	NAME	FUNCTION
8	RIN	Input Voltage Sense. Connect a resistor R_{IN} from the RIN pin to SGND.
9	COMP	Error Amplifier Output. Connect the frequency compensation network between COMP and SGND.
10	SS	Soft-Start. Connect a capacitor C_{SS} from the SS pin to SGND to program the soft-start time interval. Pullup current at this pin is 5µA.
11	RT	Switching Frequency Programming Resistor. Connect resistor R_{RT} from RT to SGND to set the PWM switching frequency. This pin is regulated to 1.215V. See the *Switching Frequency* section for selecting an appropriate R_{RT} resistor.
12	SGND	Signal Ground. Connect SGND to the signal ground plane.
13	CS	Current Sense Input. See the *Setting Peak Current Limit* section for selecting an R_{CS} resistor.
14	PGND	Power Ground. Connect PGND to the power ground plane.
15	NDRV	Driver Output. Connect this pin to the external MOSFET gate. Switches between $INTV_{CC}$ to PGND.
16	INTVCC	Linear Regulator Output and Driver Input. Connect a minimum of 2.2µF bypass capacitor from INTVCC pin to PGND as close as possible to the MAX17690 IC. This pin is typically regulated to 7V.
	EP	Exposed Pad. Connect this pin to the signal ground plane.

Functional Diagram



Detailed Description

For low and medium-power applications, the flyback converter is the preferred choice due to its simplicity and low cost. However, in isolated applications, the use of optocoupler or auxiliary winding for voltage feedback across the isolation boundary increases the number of components, and design complexity. The MAX17690 eliminates the optocoupler or auxiliary winding, and achieves ±5% output voltage regulation over line and load variations.

The MAX17690 implements an innovative algorithm to sample the output voltage by primary-side sensing when the secondary current is close to zero. This minimizes the errors due to transformer secondary parasitics and the diode forward voltage. When the primary MOSFET is turned-off, the interaction between the leakage inductance and the drain node capacitance creates a ringing at the drain node of the MOSFET. The device provides a blanking time of 150ns (typ) for the ringing to settle. The designer should limit this ringing to a time interval smaller than the blanking time using an RC snubber, RCD clamp, or both. The MAX17690 needs a minimum off time of 430ns (typ) to sample the output voltage, including the internal blanking time.

Supply Voltage

The IC has a wide input voltage range from 4.5V to 60V. Connect the positive terminal of the supply voltage to the V_{IN} pin of the IC. The voltage at this pin acts as reference voltage for the voltage measured at the drain node of the MOSFET during flyback period. Connect a minimum of 1µF ceramic capacitor between V_{IN} pin and SGND, as close to the IC as possible.

EN/UVLO and OVI

This device's EN/UVLO pin serves as an enable/disable input, as well as an accurate programmable input UVLO pin. The MAX17690 do not commence startup operation until the EN/UVLO pin voltage exceeds 1.215V (typ). The MAX17690 turns-off if the EN/UVLO pin voltage falls below 1.1V (typ). A resistor-divider from the input positive terminal to SGND can be used to divide and apply a fraction of the input voltage (V_{IN}) to the EN/UVLO pin. The values of the resistor-divider can be selected so that the EN/UVLO pin voltage exceeds the 1.215V (typ) turn-on threshold at the desired input bus voltage. The same resistor-divider can be modified with an additional resistor (R_{OVI}) to implement input overvoltage protection in addition to the EN/UVLO functionality, as shown in Figure 1. When the voltage at the OVI pin exceeds 1.215V (typ), the device stops switching. The device resumes switching operations only if the voltage at the OVI pin falls below 1.1V (typ). For given values of startup input voltage (V_{START}) and input overvoltage-protection voltage (V_{OVI}), the resistor values for the divider can be calculated as follows, assuming a 10kΩ resistor for R_{OVI}:

$$R_{EN} = R_{OVI} \times \left[\frac{V_{OVI}}{V_{START}} - 1 \right]$$

Where R_{OVI} is in kΩ, while V_{START} and V_{OVI} are in volts

$$R_{EN-TOP} = \left[R_{OVI} + R_{EN} \right] \times \left[\frac{V_{START}}{1.215} - 1 \right]$$

Where R_{EN} , R_{OVI} is in kΩ, while V_{START} is in volts.

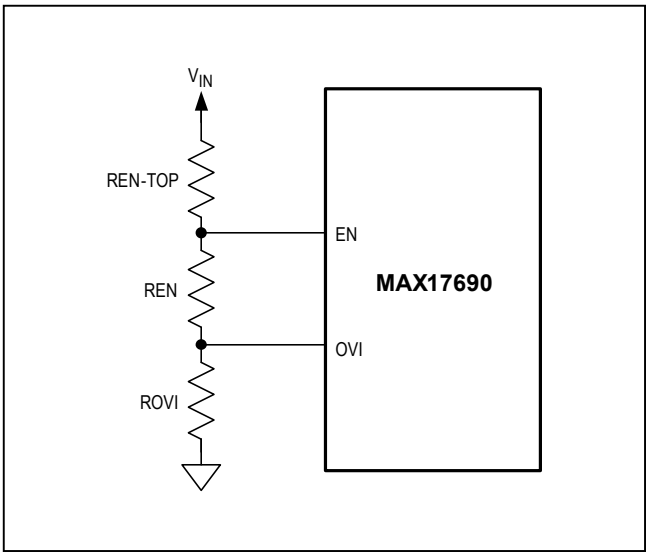


Figure 1. Programming EN/UVLO and OVI

$INTV_{CC}$

The V_{IN} powers internal LDO of the MAX17690. The regulated output of the LDO is connected to the $INTV_{CC}$ pin. The LDO output voltage is 7V (typ). Connect a 2.2µF (min) ceramic capacitor between the $INTV_{CC}$ and PGND pins for the stable operation over the full temperature range. Place this capacitor as close as close possible to the IC. Although there is no need for an auxiliary winding for the voltage feedback, for some applications with input voltages greater than 16V, an additional winding used to overdrive the $INTV_{CC}$ may improve overall system efficiency. The third winding should be designed to output a voltage between 8V and 16V. The typical circuit for overdriving the $INTV_{CC}$ is shown in Figure 2.

Programming Soft-start time

The capacitor connected between the SS pin to SGND programs the soft-start time. Internally generated 5µA of precise current source charges the soft-start capacitor. When the EN/UVLO voltage is above 1.215V (typ), the device initiates a soft-start sequence. During the soft-start time, the SS pin voltage is used as a reference for the internal error amplifier. The soft-start feature reduces the input inrush current during startup. The reference ramp-up allows the output voltage to increase monotonically from zero to the target output value.

$$C_{SS} = 5 \times t_{SS}$$

where,

C_{SS} is the soft-start capacitor in nF

t_{SS} is the soft-start time in ms

Switching Frequency

The MAX17690 switching frequency is programmable between 50kHz and 250kHz with a resistor R_{RT} connected between RT and SGND. Use the following formula to determine the appropriate value of R_{RT}:

$$R_{RT} = \frac{5 \times 10^9}{f_{SW}}$$

where, f_{SW} is the desired switching frequency

Selection of R_{IN}, R_{FB} and R_{SET} Resistor

In a flyback converter, during the turn-off time of the primary MOSFET, the voltage across the drain node of the MOSFET is the sum of the input voltage and the reflected secondary winding voltage on the primary. A resistor placed between FB pin and the drain node of the MOSFET is used to derive the output voltage during the turn-off time of Primary MOSFET. The device programs a 100µA current through the R_{FB} resistor. Use the following formula to calculate the R_{FB} resistor,

$$R_{FB} = \frac{(V_O + V_D) \times (N_P / N_S)}{100\mu A} \text{ Where,}$$

V_O is the output voltage in Volts

V_D is the forward voltage drop of the secondary diode

N_P/N_S is the primary-to-secondary turns ratio of the transformer.

The output voltage sampling instance is determined based on the input voltage, the resistor connected from R_{IN} to SGND and the reflected output voltage on the drain node of the MOSFET during flyback period. For sampling the output voltage when the secondary current is close to zero, use the following formula to select the R_{IN} resistor.

$$R_{IN} = 0.6 \cdot R_{FB}$$

The R_{SET} resistor is connected between the SET pin and SGND. The current proportional to V_O/R_{FB} flows through the R_{SET} resistor to generate a voltage proportional to output, referred to SGND. The Voltage across the R_{SET} is sampled when the secondary current is near zero and held at error amplifier's negative terminal till the next sampling. When the output is regulated, the voltage across the R_{SET} will be equal to 1V (typ) at the sampling instance. To regulate the output voltage, the value of R_{SET} should be 10kΩ.

$$R_{SET} = 10k\Omega$$

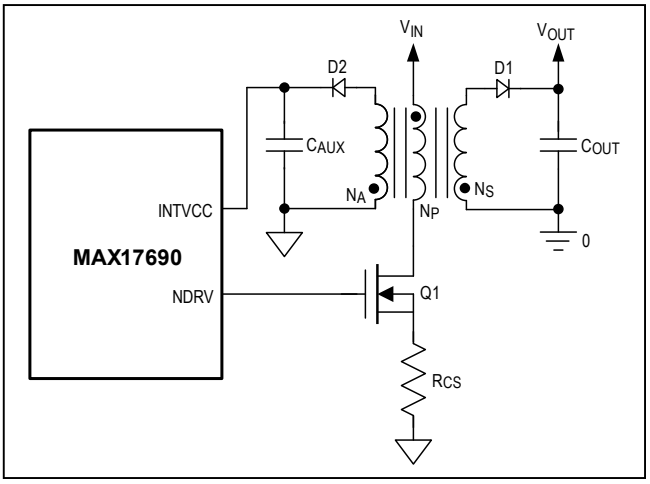


Figure 2. $INTV_{CC}$ Pin Configuration.

Setting Peak current Limit

A current-sense resistor, connected between the source of the MOSFET and PGND, sets the peak current limit. The current-limit comparator has a voltage trip point (V_{CS-MAX}) of 100mV. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{100mV}{I_{LIM}}$$

where I_{LIM} is the peak current through the MOSFET

Selection of V_{CM} Resistor

The device generates the voltage proportional to input voltage times the on-time to determine the sampling instance for the output voltage. The magnitude of this voltage depends on switching frequency (f_{SW}) and duty cycle. The resistor connected between the V_{CM} pin to SGND is used to scale the common-mode voltage of internal circuit within the operating range. Follow the below steps to select the R_{CM} resistor value,

1) Using the below formula, calculate the required internal capacitance (C_{INT})

$$C_{INT} = \frac{(100\mu \times (1 - D_{MAX})}{(f_{SW} \times 3)}$$

where D_{MAX} is the maximum operating duty cycle.

2) From Table 1, choose the nearest higher capacitance for the calculated C_{INT}.

3) Select the resistor value corresponding to the choice of capacitor, as the R_{CM}.

Table 1. R_{CM} Resistor Selection

S.NO	C_{INT} (PF)	R_{CM} (Ω)
1	640	0
2	320	85k
3	160	140k
4	80	220k
5	40	Float

Temperature Compensation

The diode forward drop (V_D) has a significant negative temperature coefficient. To compensate for this, a positive temperature coefficient current source is internally connected to the SET pin. Resistor RTC connected between the TC pin and SGND sets the current. The following equation is used to calculate the RTC:

$$\frac{\delta V_D}{\delta T} = -\frac{R_{FB}}{R_{TC}} \times \frac{N_S}{N_P} \times \frac{\delta V_{TC}}{\delta T} \text{ or}$$

$$R_{TC} = \frac{R_{FB}}{\delta V_D/\delta T} \times \frac{N_S}{N_P} \times \frac{\delta V_{TC}}{\delta T} \approx \frac{N_S}{N_P} \times R_{FB}$$

$\frac{\delta V_D}{\delta T}$ – Diode's forward voltage temperature coefficient

$$\frac{\delta V_{TC}}{\delta T} = 1.85mV/°C$$

V_{TC} = 0.55V

Due to additional proportional to absolute temperature (PTAT) currents into the SET pin, the R_{FB} needs to be adjusted to eliminate the systematic offset using the following equation:

$$R_{FB(NEW)} = \frac{(V_0 + V_D)}{\frac{N_S}{N_P} \times (100\mu - \frac{0.55}{R_{TC}})}$$

$$R_{IN(NEW)} = 0.6 \times R_{FB(NEW)}$$

Due to the non-idealities in the transformer and secondary diode, the measured output voltage may deviate from the target output voltage. For the desired output voltage, we need to adjust the R_{FB} resistor to:

$$R_{FB(adj)} = \frac{V_{0(TARGET)}}{V_{0(MEASURED)}} \times R_{FB(NEW)}$$

Transformer Magnetizing Inductance and Leakage Inductance

Designers can follow the standard flyback transformer design outlined in AN5504 for selecting the transformer magnetizing inductance. As the MAX17690 uses the sampling technique to derive the output voltage information, we arrive at a condition for the minimum magnetizing inductance as briefed below.

The MAX17690 sets the minimum voltage level of the CS pin at 20mV, to force the switching in every clock cycle. This switching is mandatory for the controller to sample the output voltage. The controller sets a min turn-on time of 200ns (typ), to avoid false triggering due to leakage inductance ringing. To sample the correct output voltage, the controller requires a minimum of-time of 430ns (typ). The above requirements impose the below conditions on the magnetizing inductance (L_{MAG}) of the transformer:

$$L_{MAG} \geq \frac{(V_{OUT} \times 430n)}{(K \times \frac{I_{LIM}}{5})}$$

$$L_{MAG} \geq \frac{(V_{INMAX} \times 200ns)}{(K \times \frac{I_{LIM}}{5})} \text{ where,}$$

V_{OUT} is the Regulated Output voltage

V_{INMAX} is the maximum operating input voltage

I_{LIM} is the peak current limit set by R_{CS} resistor

K is the ratio of the secondary-to-primary turns of the transformer.

To achieve ±5% voltage regulation over line, load, and temperature, suitable winding techniques should be used to limit the leakage inductance to 1.5% to 2% of the transformer magnetizing inductance.

Minimum Load Requirement

The MAX17690 samples the output voltage information using the flyback pulse that occurs once the external MOSFET is turned-off. The external MOSFET switching is mandatory to sample the output voltage. Thus, the MAX17690 needs to deliver a minimum amount of energy even during the no-load condition. At load currents less than 4% of the full load current, the device modulates the switching frequency discretely between $f_{SW}/4$ and f_{SW} to regulate the output voltage. This enables the device to limit the minimum load requirements to approximately 1.5% to 2% of full load.

Short-Circuit Protection/Hiccup

The device offers a hiccup scheme that protects and reduces power dissipation in the design under output short-circuit conditions. One occurrence of the runaway current limit or output voltage less than 70% of regulated voltage would trigger a hiccup mode that protects the converter by immediately suspending the switching for the period of 16,384 clock cycles. The runaway current limit is set at a $V_{CS-PEAK}$ of 120mV (typ).

Output Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of 50% of the rated output current so that the output voltage deviation is contained to 3% of the rated output voltage. The output capacitance can be calculated as follows

$$C_{OUT} = \frac{I_{STEP} \times T_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

$$T_{RESPONSE} \cong (\frac{0.33}{f_C} + \frac{1}{f_{SW}})$$

Table 2: Predesigned Transformers—Typical Specifications Unless Otherwise Noted

TRANSFORMER PART NUMBER	SIZE (W x L x H) (mm)	L_{PRI} (µH)	L_{LEAK} (nH)	NPS (NP:NS)	I_{SAT} (A)	R_{PRI} (mΩ)	R_{SEC} (mΩ)	MANUFACTURER	TARGET APPLICATION	
									INPUT (V)	OUTPUT
750343122	13.3 x 15.2 x 11.4	27	300	3:1	1.8	0.075	0.02	Wurth	18–36	5V/1A
750343077	13.4 x 17.7 x 12.7	6	150	1:2.4	6.5	0.021	0.22	Wurth	4.5–5.5	+15V/250mA -15V/150mA
750342975	13.3 x 15.2 x 11.4	27	300	3:1	1.8	0.075	0.02	Wurth	18–36	5V/1A
750343078	12.04 x 12.7 x 6.1	60	1500	1:1	1	0.25	0.32	Wurth	15–35	15V/0.17A

The output capacitor RMS current rating can be calculated as follows:

$$I_{COUTRMS} = I_{OUT} \times \sqrt{\frac{2 \times I_{PRIPEAK}}{3 \times K \times I_{OUT}} - 1}$$

Where I_{STEP} is the load step, $T_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage ripple, and f_C is the target closed-loop crossover frequency. f_C is chosen between 1/20 to 1/40 of the switching frequency (f_{SW}). For the flyback converter, the output capacitor supplies the load current when the main switch is on, and therefore the output voltage ripple is a function of load current and duty cycle. Use the following equation to calculate the output capacitor ripple:

$$\Delta V_{COUT} = \frac{I_{OUT} \times \left[I_{PRIPEAK} - (K \times I_{OUT})\right]^2}{I_{PRIPEAK}^2 \times f_{SW} \times C_{OUT}}$$

where I_{OUT} is load current.

The parameters $I_{PRIPEAK}$ and K are dependent on the transformer design parameters.

Loop Compensation

The MAX17690 is compensated using an external resistor capacitor network on the COMP pin. For no-opto flyback designs, the loop compensation network are connected as shown in Figure 3.

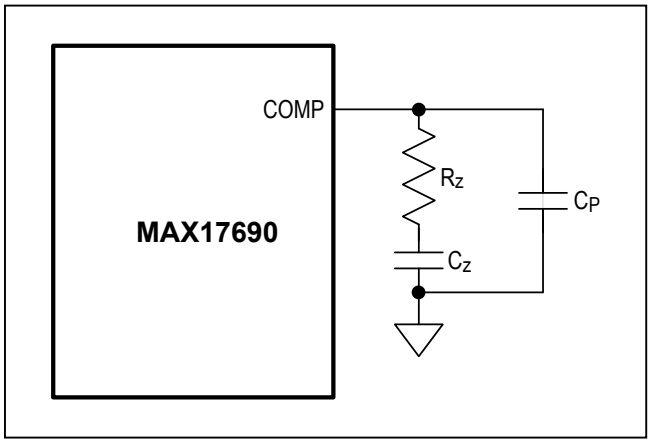


Figure 3. Loop Compensation Arrangement

The loop compensation values are calculated as follows:

$$R_Z = 12500 \times R_{CS} \times \left[\frac{f_C}{f_P}\right] \sqrt{\frac{V_{OUT} \times I_{OUT}}{2 \times L_{PRI} \times f_{SW}}} \ \Omega$$

$$C_Z = \frac{1}{2\pi \times R_Z \times f_P} \text{ Farad}$$

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}} \text{ Farad}$$

where:

$$f_P = \frac{1}{\pi \times \frac{V_{OUT}}{I_{OUT}} \times C_{OUT}} \text{ Hz}$$

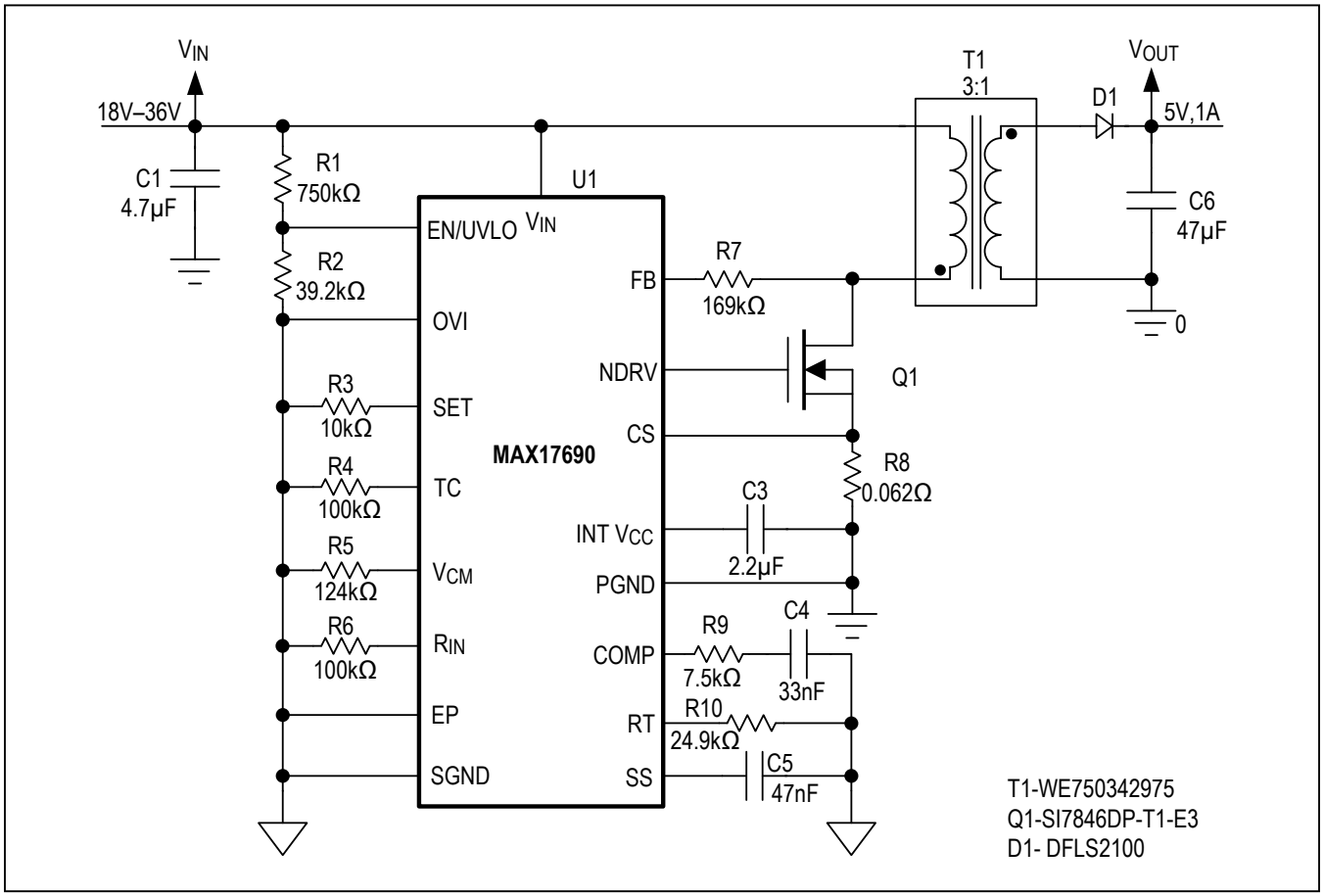
PCB Layout guidelines

Careful PCB layout is critical to achieve clean and stable operation. For a sample layout that ensures first-pass success, refer to the MAX17690 evaluation kit layouts available at www.maximintegrated.com.

Follow the below guidelines for good PCB layout:

1) Keep the loop area of paths carrying the pulsed currents as small as possible.
2) INTVCC and V_{IN} bypass capacitors should be connected close to the respective pins and returned to GND pin of the IC. This loop area should be as small as possible.
3) The proper sensing of Lx voltage is critical in sampling algorithm. The R_{FB} resistor trace length should be kept as small as possible.
4) The ground termination of the current sense resistor should be kelvin connected to the SGND of the IC.

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17690ATE+	-40°C to +125°C	16 TQFN

+Denotes a lead(pB)-free/RoHS-compliant package.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN	T1633+4C	21-0136	90-0031

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/16	Initial release	—

