±0.8% Accurate Quad UV/OV Positive/Negative Voltage Supervisor

Data Sheet

ADM12914

FEATURES

- Quad undervoltage/overvoltage (UV/OV) positive/negative supervisor
- Supervises up to two negative rails
- Adjustable UV and OV input thresholds
- Industry leading threshold accuracy over the extended temperature range: ±0.8%
- 1 V buffered reference output
- Open-drain $\overline{UV}$ and $\overline{OV}$ reset outputs
- Adjustable reset timeout with disable option
- Outputs guaranteed down to V_{CC} of 0.9 V
- Glitch immunity
- 62 µA supply current
- 16-lead QSOP package
- Specified from −40°C to +125°C

APPLICATIONS

- Server supply monitoring
- FPGA/DSP core and I/O voltage monitoring
- Telecommunications equipment
- Medical equipment

FUNCTIONAL BLOCK DIAGRAM

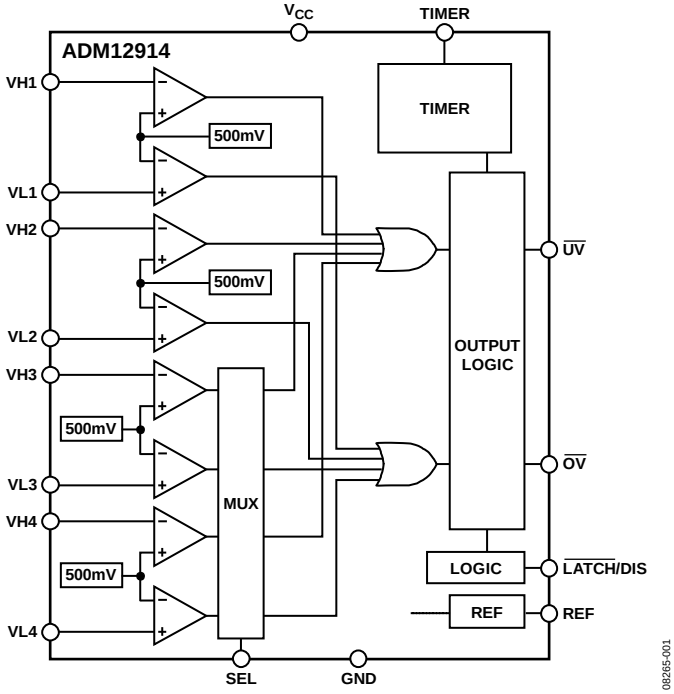

Figure 1.

GENERAL DESCRIPTION

The ADM12914 is a quad voltage supervisory IC ideally suited for monitoring multiple rails in a wide range of applications. Each monitored rail has two dedicated input pins, VHx and VLx, which allows each rail to be monitored for both undervoltage (UV) and overvoltage (OV) conditions with high threshold accuracy of ±0.8%. Common active low undervoltage ($\overline{UV}$) and overvoltage ($\overline{OV}$) pins are shared by each of the monitored voltage rails.

The ADM12914 includes a 1 V buffered reference output, REF, that acts as an offset when monitoring a negative voltage. The three-state SEL pin determines the polarity of the third and fourth inputs, that is, it configures the device to monitor positive or negative supplies.

The device incorporates an internal shunt regulator that enables the device to be used in higher voltage systems. This feature requires a resistor to be placed between the main supply rail and the V_{CC} pin to limit the current flow into the V_{CC} pin at a level no greater than 10 mA. The ADM12914 uses the internal shunt regulator to regulate V_{CC} if the supply line exceeds the absolute maximum ratings.

The ADM12914 is available in two models. The ADM12914-1 offers a latching overvoltage output that can be cleared by toggling the $\overline{LATCH}$ input pin. The ADM12914-2 has a disable pin that can override and disable both the $\overline{UV}$ and the $\overline{OV}$ output signals.

The ADM12914 is available in a 16-lead QSOP package. The device is specified over the extended temperature range of −40°C to +125°C.

Rev. F
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- ADM2914/ADM12914 Evaluation Board

DOCUMENTATION

Data Sheet

- ADM12914: ±0.8% Accurate Quad UV/OV Positive/ Negative Voltage Supervisor Data Sheet

User Guides

- UG-174: Evaluation Board User Guide for ADM2914 and ADM12914

REFERENCE MATERIALS

Product Selection Guide

- Supervisory Devices Complementary Parts Guide for Altera FPGAs
- Supervisory Devices Complementary Parts Guide for Xilinx FPGAs

DESIGN RESOURCES

- ADM12914 Material Declaration
- PCN-PDN Information
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REVISION HISTORY

2/2017—Rev. E to Rev. F
Change to Figure 25 ... 15

5/2015—Rev. D to Rev. E
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Added Figure 23, Renumbered Sequentially ... 13
Added Table 6, Renumbered Sequentially ... 14
Updated Outline Dimensions ... 16

8/2013—Rev. C to Rev. D
Changes to Figure 17 and Figure 18 ... 10
Deleted $\overline{UV}$ and $\overline{OV}$ Rise and Fall Times Section ... 13
Changes to Figure 24 and Figure 25 ... 15

6/2010—Rev. B to Rev. C
Changed V_{CC} of 1 V to V_{CC} of 0.9 V in Features Section ... 1

2/2010—Rev. A to Rev. B
Changes to Figure 17 and Figure 18 ... 10

12/2009—Rev. 0 to Rev. A
Changes to Shunt Regulator Section ... 13

9/2009—Revision 0: Initial Version

SPECIFICATIONS

T_A = −40°C to +125°C. Typical values at T_A = 25°C, unless otherwise noted. V_{CC} = 3.3 V, VLx = 0.45 V, VHx = 0.55 V, $\overline{LATCH}$ = V_{CC}, SEL = V_{CC}, DIS = open, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SHUNT REGULATOR						
V_{CC} Shunt Regulator Voltage	V_{SHUNT}	6.3	6.6	6.8	V	I_{CC} = 5 mA
V_{CC} Shunt Regulator Load Regulation	ΔV_{SHUNT}			150	mV	I_{CC} = 2 mA to 10 mA
SUPPLY						
Supply Voltage[1]	V_{CC}	2.3		V_{SHUNT}	V	
Minimum V_{CC} Output Valid	$V_{CCR(MIN)}$			0.9	V	DIS = 0 V
Supply Undervoltage Lockout	$V_{CC(UVLO)}$	1.94	2	2.06	V	DIS = 0 V, V_{CC} rising
Supply Undervoltage Lockout Hysteresis	$\Delta V_{CC(HYST)}$	15	25	35	mV	DIS = 0 V
Supply Current	I_{CC}		62	100	µA	V_{CC} = 2.3 V to 6.0 V
REFERENCE OUTPUT						
Reference Output Voltage	V_{REF}	0.994	1	1.008	V	I_{VREF} = ±1 mA
UNDERVOLTAGE/OVERVOLTAGE CHARACTERISTICS						
Undervoltage/Overvoltage Threshold	V_{UOT}	496	500	504	mV	V_{CC} = 2.3 V to 6.0 V
Undervoltage/Overvoltage Threshold to Output Delay	t_{UOD}	100	200	350	µs	VHx = V_{UOT} − 5 mV or VLx = V_{UOT} + 5 mV
VHx, VLx Input Current	I_{VHL}			±10	nA	
$\overline{UV}/\overline{OV}$ Timeout Period	t_{UOTO}	7.5	8.5	10.5	ms	C_{TIMER} = 1 nF
$\overline{OV}$ LATCH CLEAR INPUT						
$\overline{OV}$ Latch Clear Threshold Input High	$V_{\overline{LATCH}(IH)}$	1.2			V	
$\overline{OV}$ Latch Clear Threshold Input Low	$V_{\overline{LATCH}(IL)}$			0.8	V	
$\overline{LATCH}$ Input Current	I_{LATCH}			50	nA	$V_{\overline{LATCH}}$ > 0.5 V
DISABLE INPUT						
DIS Input High	$V_{DIS(IH)}$	1.2			V	
DIS Input Low	$V_{DIS(IL)}$			0.8	V	
DIS Input Current	I_{DIS}	1.25	2	2.75	µA	V_{DIS} > 0.5 V
TIMER CHARACTERISTICS						
TIMER Pull-Up Current	$I_{TIMER(UP)}$	−1.7	−2.1	−2.5	µA	V_{TIMER} = 0 V
TIMER Pull-Down Current	$I_{TIMER(DOWN)}$	1.7	2.1	2.5	µA	V_{TIMER} = 1.6 V
TIMER Disable Voltage	$V_{TIMER(DIS)}$	−180	−270		mV	Referenced to V_{CC}
OUTPUT VOLTAGE						
Output Voltage High $\overline{UV}/\overline{OV}$	V_{OH}	1			V	V_{CC} = 2.3 V; $I_{\overline{UV}/\overline{OV}}$ = −1 µA
Output Voltage Low $\overline{UV}/\overline{OV}$	V_{OL}		0.1	0.3	V	V_{CC} = 2.3 V; $I_{\overline{UV}/\overline{OV}}$ = 2.5 mA
			0.01	0.15	V	V_{CC} = 0.9 V; $I_{\overline{UV}}$ = 100 µA
THREE-STATE INPUT SEL						
Low Level Input Voltage	V_{IL}			0.4	V	
High Level Input Voltage	V_{IH}	1.4			V	
Pin Voltage when Left in High-Z State	V_Z	0.8	0.9	1.0	V	I_{SEL} = ±10 µA
SEL High, Low Input Current	I_{SEL}			±25	µA	
Maximum SEL Input Current	$I_{SEL(MAX)}$			±30	µA	SEL tied to V_{CC} or GND

[1] The maximum voltage on the V_{CC} pin is limited by the input current. The V_{CC} pin has an internal 6.5 V shunt regulator and, therefore, a low impedance supply exceeding 6 V may exceed the maximum allowable input current. When operating from a higher supply than 6 V, always use a dropper resistor.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
$\overline{UV}$, $\overline{OV}$	−0.3 V to +16 V
TIMER	−0.3 V to (V_{CC} + 0.3 V)
VLx, VHx, $\overline{LATCH}$, DIS, SEL	−0.3 V to +7.5 V
I_{CC}	10 mA
Reference Load Current (I_{REF})	±1 mA
$I_{\overline{UV}}$, $I_{\overline{OV}}$	10 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead QSOP	104	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

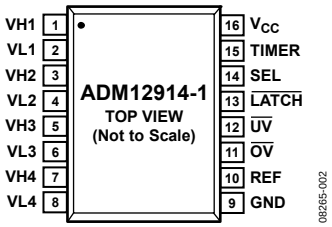


Figure 2. ADM12914-1 Pin Configuration

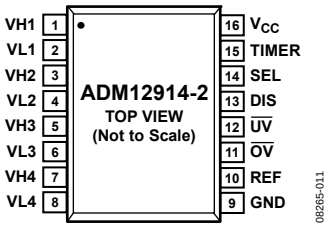


Figure 3. ADM12914-2 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.			
ADM12914-1	**ADM12914-2**	**Mnemonic**	**Description**
1, 3	1, 3	VH1, VH2	Voltage High Input 1 and Voltage High Input 2. If the voltage monitored by VH1 or VH2 drops below 0.5 V, an undervoltage condition is detected. Connect to V_{CC} when not in use.
2, 4	2, 4	VL1, VL2	Voltage Low Input 1. If the voltage monitored by VL1 or VL2 rises above 0.5 V, an overvoltage condition is detected. Tie to GND when not in use.
5, 7	5, 7	VH3, VH4	Voltage High Input 3 and Voltage High Input 4. The polarity of these inputs is determined by the state of the SEL pin (see Table 5). When the monitored input is configured as a positive voltage and the voltage monitored by VH3 and VH4 drops below 0.5 V, an undervoltage condition is detected. Conversely, when the input is configured as a negative voltage and the input drops below 0.5 V, an overvoltage condition is detected. Connect to V_{CC} when not in use.
6, 8	6, 8	VL3, VL4	Voltage Low Input 3 and Voltage Low Input 4. The polarity of these inputs is determined by the state of the SEL pin (see Table 5). When the monitored input is configured as a positive voltage and the voltage monitored by VL3 or VL4 rises above 0.5 V, an overvoltage condition is detected. Conversely, when the input is configured as a negative voltage and the input rises above 0.5 V, an undervoltage condition is detected. Tie to GND when not in use.
9	9	GND	Device Ground.
10	10	REF	Buffered Reference Output. This pin is a 1 V reference that is used as an offset when monitoring negative voltages. This pin can source or sink 1 mA, and drive loads up to 1 nF. Larger capacitive loads may lead to instability. Leave unconnected when not in use.
11	11	$\overline{OV}$	Overvoltage Reset Output. $\overline{OV}$ is asserted low if a negative polarity input voltage drops below its associated threshold or if a positive polarity input voltage exceeds its threshold. The ADM12914-1 allows $\overline{OV}$ to be latched low. The ADM12914-2 holds $\overline{OV}$ low for an adjustable timeout period determined by the timer capacitor. This pin has a weak pull-up to V_{CC} and can be pulled up to 16 V externally. Leave this pin unconnected when not in use
12	12	$\overline{UV}$	Undervoltage Reset Output. $\overline{UV}$ is asserted low if a negative polarity input voltage exceeds its associated threshold or if a positive polarity input voltage drops below its threshold. $\overline{UV}$ is held low for an adjustable timeout period set by the external capacitor tied to the TIMER pin. The $\overline{UV}$ pin has a weak pull-up to V_{CC} and can be pulled up to 16 V externally via an external pull-up resistor. Leave this pin unconnected when not in use.
13	N/A[1]	$\overline{LATCH}$	$\overline{OV}$ Latch Bypass Input/Clear Pin. When pulled high, the $\overline{OV}$ latch is cleared. When held high, the $\overline{OV}$ output has the same delay and output characteristics as the $\overline{UV}$ output. When pulled low, the $\overline{OV}$ output is latched when asserted. (Applies only to the ADM12914-1.)
N/A[1]	13	DIS	$\overline{OV}$ and $\overline{UV}$ Disable Input. When pulled high, the $\overline{OV}$ and $\overline{UV}$ outputs are held high irrespective of the state of the VHx and VLx input pins. However, if a UVLO condition occurs, the $\overline{OV}$ and $\overline{UV}$ outputs are asserted. This pin has a weak internal pull-down (2 µA) to GND. Leave this pin unconnected when not in use. (Applies only to the ADM12914-2.)
14	14	SEL	Input Polarity Select. This three-state input pin allows the polarity of VH3, VL3, VH4, and VL4 to be configured. Connect this pin to V_{CC} or GND, or leave it open to select one of three possible input polarity configurations (see Table 5).

Pin No.		Mnemonic	Description
ADM12914-1	ADM12914-2		
15	15	TIMER	Adjustable Reset Delay Timer. Connect an external capacitor to the TIMER pin to program the reset timeout delay. Refer to Figure 15 in the Typical Performance Characteristics section. Connect this pin to V_{CC} to bypass the timer.
16	16	V_{CC}	Supply Voltage. V_{CC} operates as a direct supply for voltages up to 6 V. For voltages greater than 6 V, it operates as a shunt regulator. A dropper resistor must be used in this configuration to limit the current to less than 10 mA. When used without the resistor, the voltage at this pin must not exceed 6 V. A 0.1 µF bypass capacitor or greater should be used.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

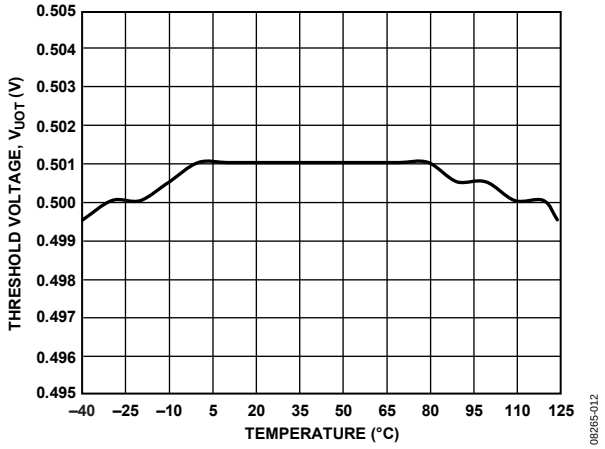


Figure 4. Input Threshold Voltage vs. Temperature

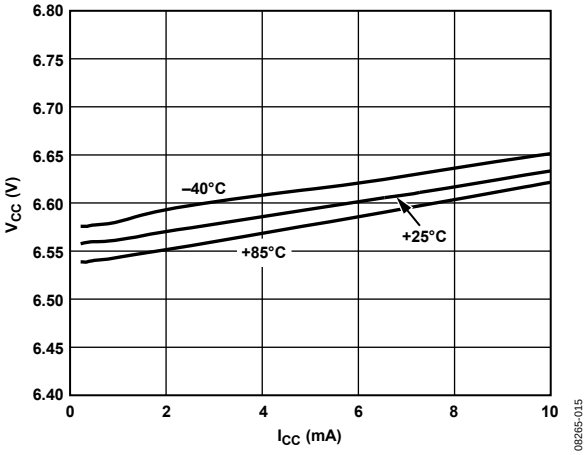


Figure 7. V_{CC} Shunt Voltage vs. I_{CC}

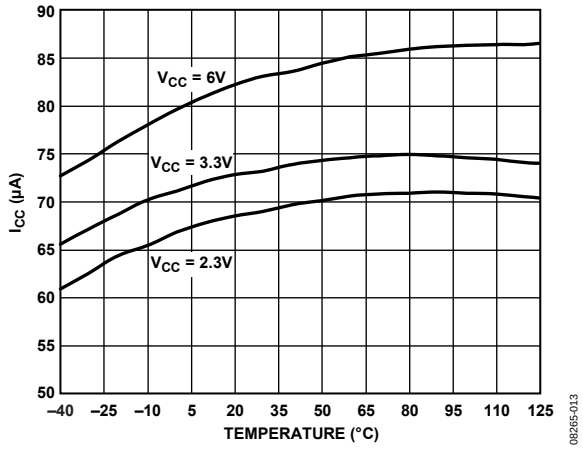


Figure 5. Supply Current vs. Temperature

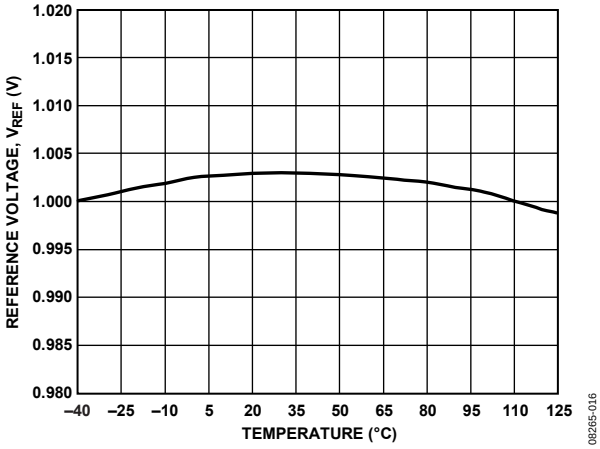


Figure 8. Buffered Reference Voltage vs. Temperature

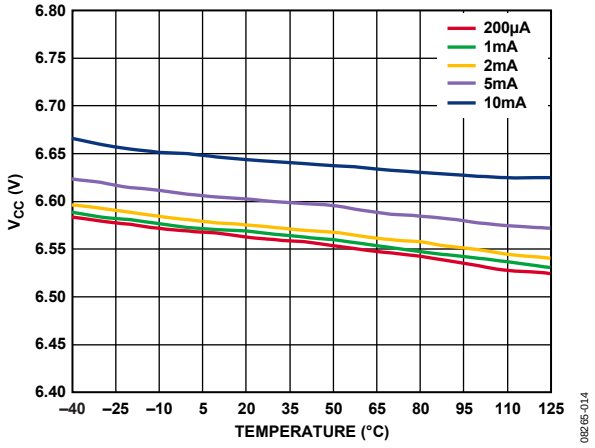


Figure 6. V_{CC} Shunt Voltage vs. Temperature

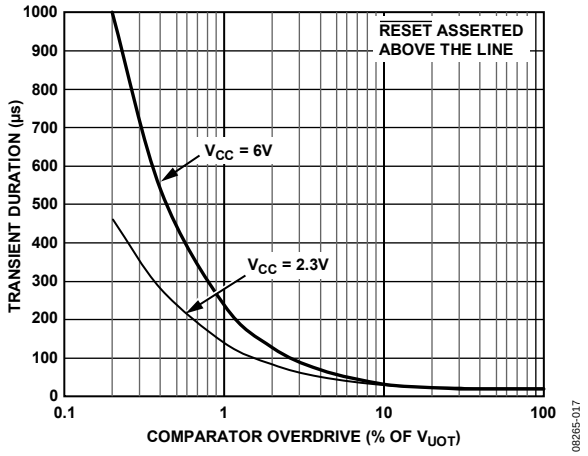


Figure 9. Transient Duration vs. Comparator Overdrive

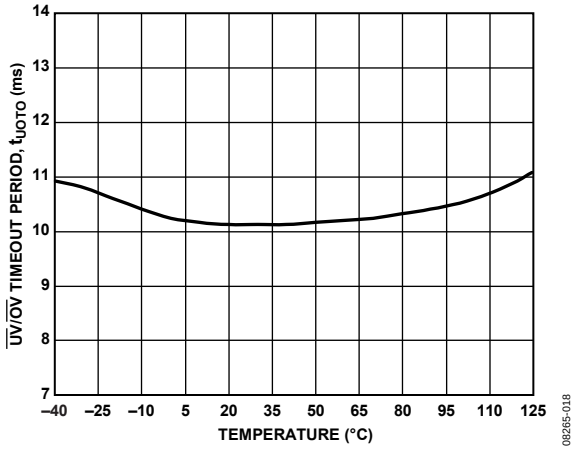


Figure 10. $\overline{UV}/\overline{OV}$ Timeout Period vs. Temperature

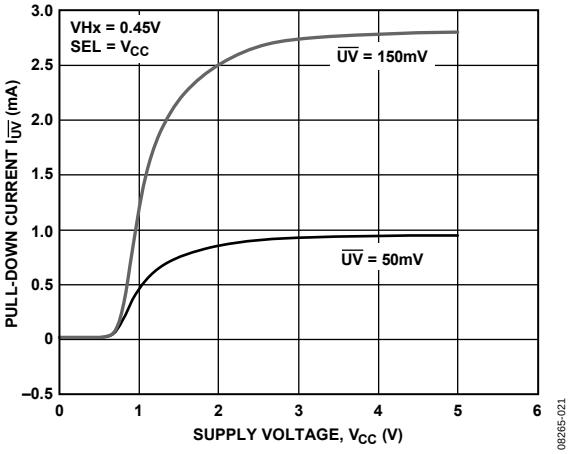


Figure 13. I_{SINK}, $I_{\overline{UV}}$ vs. V_{CC}

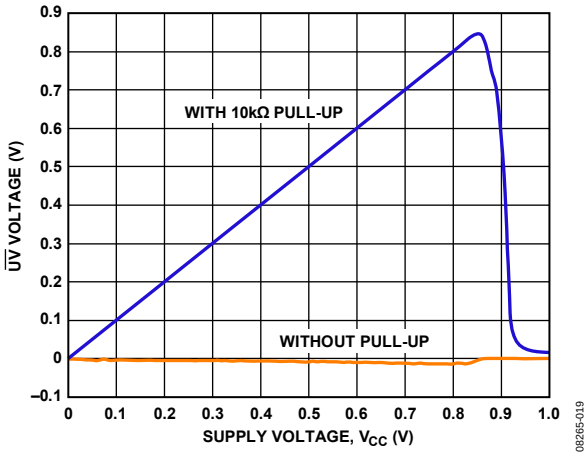


Figure 11. $\overline{UV}$ Output Voltage vs. V_{CC}

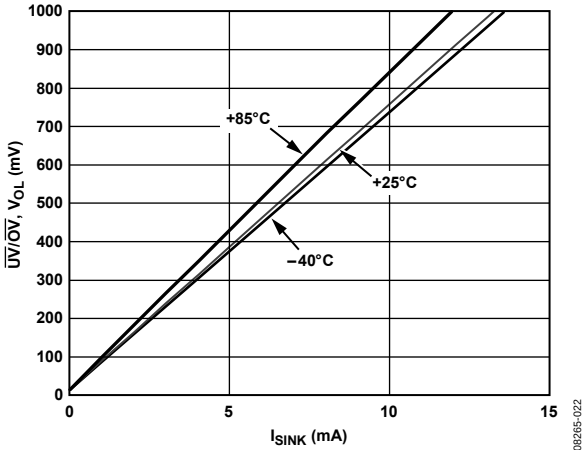


Figure 14. $\overline{UV}/\overline{OV}$ Voltage Output Low vs. Output Sink Current

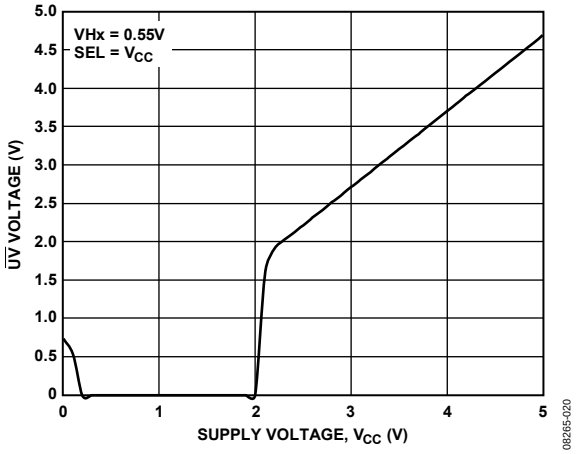


Figure 12. $\overline{UV}$ Output Voltage vs. V_{CC}

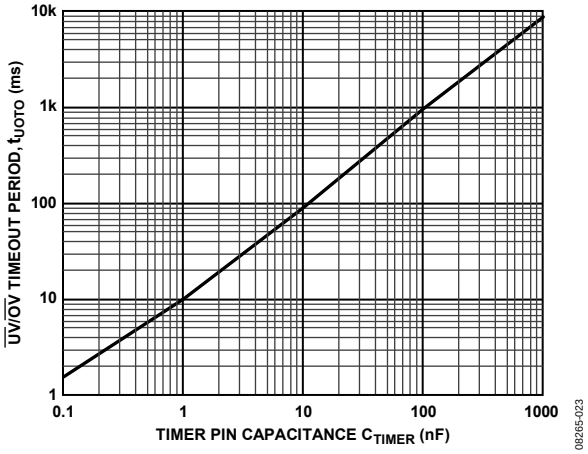


Figure 15. $\overline{UV}/\overline{OV}$ Timeout Period vs. Capacitance

THEORY OF OPERATION

VOLTAGE SUPERVISION

The ADM12914 supervises up to four voltage rails for undervoltage and overvoltage conditions. Two pins, VHx and VLx, are assigned to monitor each rail, one for overvoltage detection and the other for undervoltage detection. Each pin is connected to the input of an internal voltage comparator, and its voltage level is internally compared with a 0.5 V voltage reference with very high threshold accuracy of ±0.8%. The device is specified over the extended operating temperature range from −40°C to +125°C.

The output of each of the internal undervoltage comparators is tied to a common $\overline{UV}$ output pin. Likewise, the outputs of the internal overvoltage comparators are tied to a common $\overline{OV}$ output pin.

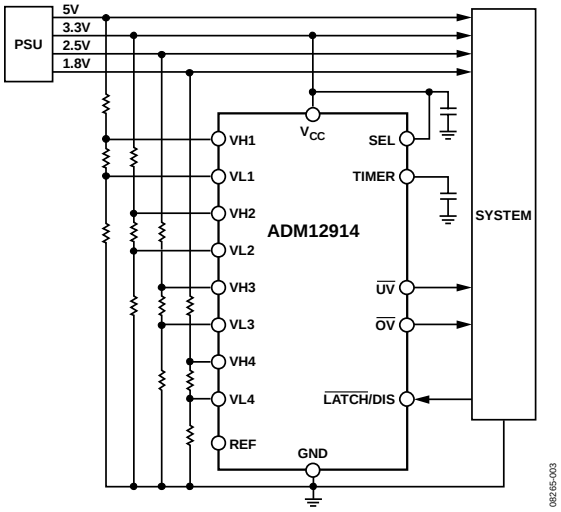


Figure 16. Typical Applications Diagram

POLARITY CONFIGURATION

The ADM12914 is capable of monitoring supply voltages of both positive and negative polarities. The SEL pin is a three-state pin that determines the polarity of Input 3 and Input 4. As summarized in Table 5, the SEL pin is connected to either GND or V_{CC}, or is not connected.

When an input is configured to monitor a positive voltage, using the three resistor scheme that is shown in Figure 17, VHx is connected to the high-side tap of the resistor divider and VLx is connected to the low-side tap of the resistor divider.

Conversely, when an input is configured to monitor a negative voltage, UVx and OVx are swapped internally. The negative voltage for monitoring is then connected as shown in Figure 18. VHx remains connected to the high-side tap and VLx remains connected to the low-side tap. Within this configuration, an undervoltage condition occurs when the monitored voltage is less negative than the programmed threshold, and an overvoltage condition occurs when the monitored voltage is more negative than the programmed threshold.

Table 5. Polarity Configuration

	Input 3			Input 4		
SEL Pin	**Polarity**	**UV Condition**	**OV Condition**	**Polarity**	**UV Condition**	**OV Condition**
Connected to V_{CC}	Positive	VH3 < 0.5 V	VL3 > 0.5 V	Positive	VH4 < 0.5 V	VL4 > 0.5 V
Left Unconnected	Positive	VH3 < 0.5 V	VL3 > 0.5 V	Negative	VL4 > 0.5 V	VH4 < 0.5 V
Connected to GND	Negative	VL3 > 0.5 V	VH3 < 0.5 V	Negative	VL4 > 0.5 V	VH4 < 0.5 V

MONITORING PIN CONNECTIONS

Positive Voltage Monitoring Scheme

When monitoring a positive supply, the desired nominal operating voltage for monitoring is denoted by V_M, I_M is the nominal current through the resistor divider, V_{OV} is the overvoltage trip point, and V_{UV} is the undervoltage trip point.

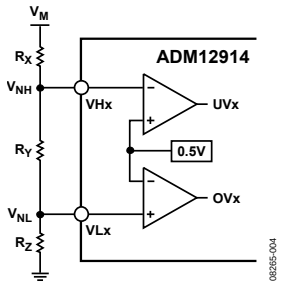


Figure 17. Positive Undervoltage/Overvoltage Monitoring Configuration

Figure 17 illustrates the positive voltage monitoring input connection. Three external resistors, R_X, R_Y, and R_Z, divide the positive voltage for monitoring,V_M, into high-side voltage, V_{PH}, and low-side voltage, V_{PL}. The high-side voltage is connected to the corresponding VHx pin and the low-side voltage is connected to the corresponding VLx pin.

To trigger an overvoltage condition, the low-side voltage (in this case, V_{PL}) must exceed the 0.5 V threshold on the VLx pin. The low-side voltage, V_{PL}, is given by the following equation:

$$V_{PL} = V_{OV}\left(\frac{R_Z}{R_X + R_Y + R_Z}\right) = 0.5\ \text{V}$$

Also,

$$R_X + R_Y + R_Z = \frac{V_M}{I_M}$$

Therefore, R_Z, which sets the desired trip point for the overvoltage monitor, is calculated using the following equation:

$$R_Z = \frac{(0.5)(V_M)}{(V_{OV})(I_M)} \quad (1)$$

To trigger the undervoltage condition, the high-side voltage, V_{PH}, must exceed the 0.5 V threshold on the VHx pin. The high-side voltage, V_{PH}, is given by the following equation:

$$V_{PH} = V_{UV}\left(\frac{R_Y + R_Z}{R_X + R_Y + R_Z}\right) = 0.5\ \text{V}$$

Because R_Z is already known, R_Y can be expressed as follows:

$$R_Y = \frac{(0.5)(V_M)}{(V_{UV})(I_M)} - R_Z \quad (2)$$

When R_Y and R_Z are known, R_X is calculated using the following formula:

$$R_X = \frac{(V_M)}{(I_M)} - R_Z - R_Y \quad (3)$$

If V_M, I_M, V_{OV}, or V_{UV} change, each step must be recalculated.

Negative Voltage Monitoring Scheme

Figure 18 shows the circuit configuration for negative supply voltage monitoring. To monitor a negative voltage, a 1 V reference voltage is required to connect to the end node of the voltage divider circuit. This reference voltage is generated internally and is output through the REF pin.

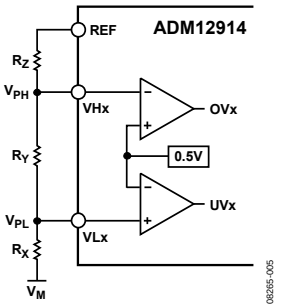


Figure 18. Negative Undervoltage/Overvoltage Monitoring Configuration

The equations described previously in the Positive Voltage Monitoring Scheme section need some minor modifications for use with negative voltage monitoring. The 1 V reference voltage is added to the overall voltage drop; it must therefore be subtracted from V_M, V_{UV}, and V_{OV} before using each in the previous equations.

To monitor a negative voltage level, the resistor divider circuit divides the voltage differential level between the 1 V reference voltage and the negative supply voltage into high-side voltage, V_{NH}, and low-side voltage, V_{NL}. Similar to the positive voltage monitoring scheme, the high-side voltage, V_{NH}, is connected to the corresponding VHx pin and the low-side voltage, V_{NL}, is connected to the corresponding VLx pin. Refer to the Voltage Monitoring Example section for further information.

THRESHOLD ACCURACY

The reset threshold accuracy is fundamental, especially at lower voltage levels. Consider an FPGA application that requires a 1 V core voltage input with a tolerance of ±5%, where the supply has a specified regulation, for example, ±2.6%. As shown in Figure 19, to ensure the supply is within the FPGA input voltage requirement range, its voltage level must be monitored for UV and OV conditions. The voltage swing on the supply itself causes the voltage band available for setting the monitoring threshold to be quite narrow. In this example, the threshold voltages, including the

tolerances, must fit within a monitor region of just 0.024 V. The ADM12914 device with 0.1% resistors can achieve this level of accuracy.

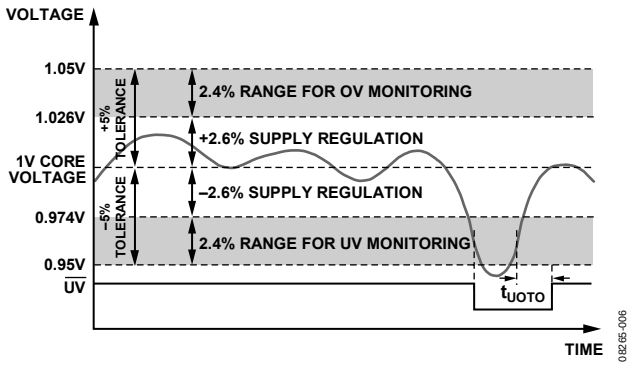


Figure 19. Monitoring Accuracy Example

VOLTAGE MONITORING EXAMPLE

To illustrate how the ADM12914 device works in a real-world application, consider the 1 V input example shown in Figure 19, with the addition of a −5 V rail.

The first step is to choose the current flow through both voltage divider circuits, for example, 5 µA.

For the 1 V ± 5% input, due to the specified ±2.6% regulation of the supply, the UV and OV threshold should be set in the middle of the undervoltage and overvoltage monitoring bands, respectively; in this case, on the ±3.8% points of the supply, which are 0.962 V for the UV threshold and 1.038 V for OV threshold.

Input these values into Equation 1 to Equation 3 as follows:

$$R_Z = \frac{(0.5)(1)}{(1.038)(5\times10^{-6})} \approx 96.5\ \text{k}\Omega \quad (1)$$

Insert the value of R_Z into Equation 2.

$$R_Y = \frac{(0.5)(1)}{(0.962)(5\times10^{-6})} - 96.5\ \text{k}\Omega \approx 7.41\ \text{k}\Omega \quad (2)$$

Then substitute the calculated values for R_Z and R_Y into Equation 3.

$$R_X = \frac{1}{5\times10^{-6}} - 96.5\ \text{k}\Omega - 7.41\ \text{k}\Omega \approx 96.5\ \text{k}\Omega \quad (3)$$

This design approach meets the application specifications. As described previously, the 1 V rail is specified with an input requirement of ±5% and a supply tolerance of ±2.6%. This effectively means the OV threshold of the monitoring device, including all the tolerance factors, must fit within the 1.026 V to 1.05 V range. Similarly, the UV threshold range must be between 0.95 V and 0.974 V.

The four worst-case scenarios of minimum and maximum undervoltage and overvoltage thresholds are calculated as follows:

Minimum overvoltage threshold

$$V_{OV\_MIN} = (0.5\,V - 0.8\%)\left(1 + \frac{(R_X - 0.1\%) + (R_Y - 0.1\%)}{(R_Z + 0.1\%)}\right)$$

$$= 0.496\left(1 + \frac{(96{,}500 + 7410)(0.999)}{(96{,}500)(1.001)}\right)$$

$$= 1.029\ \text{V} > 1.026\ \text{V}$$

Maximum overvoltage threshold

$$V_{OV\_MAX} = (0.5\,V + 0.8\%)\left(1 + \frac{(R_X + 0.1\%) + (R_Y + 0.1\%)}{(R_Z - 0.1\%)}\right)$$

$$= 1.047\ \text{V} < 1.05\ \text{V}$$

The maximum and minimum overvoltage threshold values reside within the 1.026 V to 1.05 V range specified.

The minimum and maximum undervoltage thresholds are calculated as follows:

Minimum undervoltage threshold

$$V_{UV\_MIN} = (0.5\,\text{V} - 0.8\%)\left(1 + \frac{(R_X - 0.1\%)}{(R_Y + 0.1\%) + (R_Z + 0.1\%)}\right)$$

$$= 0.9557\ \text{V} > 0.95\ \text{V}$$

Maximum undervoltage threshold

$$V_{UV\_MAX} = (0.5\,\text{V} + 0.8\%)\left(1 + \frac{(R_X + 0.1\%)}{(R_Y - 0.1\%) + (R_Z - 0.1\%)}\right)$$

$$= 0.9729\ \text{V} < 0.974\ \text{V}$$

These values fit within the specified undervoltage monitoring range. All four worst-case scenarios satisfy the tolerance requirement; therefore, the design approach is valid.

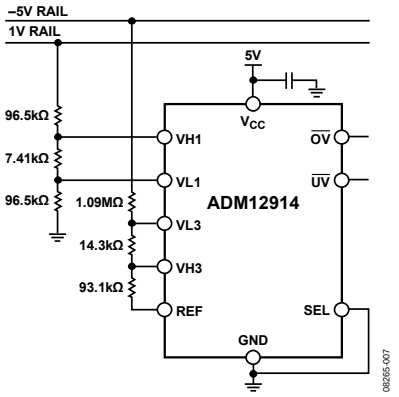


Figure 20. Positive and Negative Supply Monitor Example

Next, consider a −5 V input, which is specified with a ±12% input. The threshold accuracy required by the supply is chosen to be within ±5% of the −5 V rail. The UV and OV threshold should be set in the middle of the undervoltage and overvoltage monitoring bands, respectively. In this case, on the ±8.5% points of the supply, which is −4.575 V for the UV threshold and −5.425 V for the OV threshold.

The negative voltage scheme configuration requires that the 1 V reference voltage be accounted for in Equation 1 to Equation 3. The 1 V reference voltage is subtracted from V_M, V_{UV}, and V_{OV}, and the absolute value of the result is taken.

Equation 1 becomes

$$R_Z = \frac{(0.5)(|-5-1|)}{(|-5.425-1|)(5\times10^{-6})} \approx 93.1\,\text{k}\Omega$$

Insert the value of R_Z into Equation 2

$$R_Y = \frac{(0.5)(|-5-1|)}{(|-4.575-1|)(5\times10^{-6})} - 93.1\,\text{k}\Omega \approx 14.3\,\text{k}\Omega$$

To calculate R_X, insert the value of R_Z and R_Y into Equation 3.

$$R_X = \frac{(|-5-1|)}{5\times10^{-6}} - (14.3\,\text{k}\Omega) - (93.1\,\text{k}\Omega) \approx 1.09\,\text{M}\Omega$$

POWER-UP AND POWER-DOWN

On power-up, when V_{CC} reaches 1 V, the active low $\overline{UV}$ output asserts and the $\overline{OV}$ output pulls up to V_{CC}. When the voltage on the V_{CC} pin reaches 1 V, the ADM12914 is guaranteed to assert $\overline{UV}$ low and $\overline{OV}$ high. When V_{CC} exceeds 1.9 V (minimum), the VHx and VLx inputs take control. When V_{CC} and each of the VHx inputs are valid, an internal timer begins. Subsequent to an adjustable time delay, $\overline{UV}$ weakly pulls high.

$\overline{UV}$/$\overline{OV}$ TIMING CHARACTERISTICS

$\overline{UV}$ is an active low output. It asserts when any of the four monitored voltages is below its associated threshold. When the voltage on the V_{CC} pin is greater than 2 V, an internal timer holds $\overline{UV}$ low for an adjustable period, t_{UOTO}, after the voltages on all the monitoring rails rise above their thresholds. This allows time for all monitored power supplies to stabilize after power-up. Similarly, any monitored voltage that falls below its threshold initiates a timer reset, and the internal timer restarts once all the monitoring rails rise above their thresholds.

The $\overline{UV}$ and $\overline{OV}$ outputs are held asserted after all faults have cleared for an adjustable timeout period, determined by the value of the external capacitor attached to the TIMER pin.

TIMER CAPACITOR SELECTION

The $\overline{UV}$ and $\overline{OV}$ timeout period on the ADM12914 is programmable via the external timer capacitor, C_{TIMER}, placed between the TIMER pin and ground. The timeout period, t_{UOTO}, is calculated using the following equation:

$$C_{TIMER} = (t_{UOTO})(115)(10^{-9})\ \text{F/sec}$$

Refer to Figure 15 in the Typical Performance Characteristics section, which illustrates the delay time as a function of the timer capacitor value. A minimum capacitor value of 10 pF is required. The chosen timer capacitor must have a leakage current that is less than the 1.7 µA TIMER pin charging current. To bypass the timeout period, connect the TIMER pin to V_{CC}.

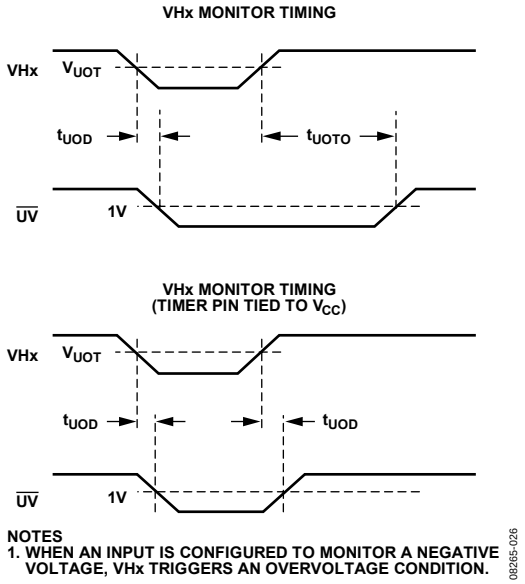


Figure 21. VHx Positive Voltage Monitoring Timing Diagrams

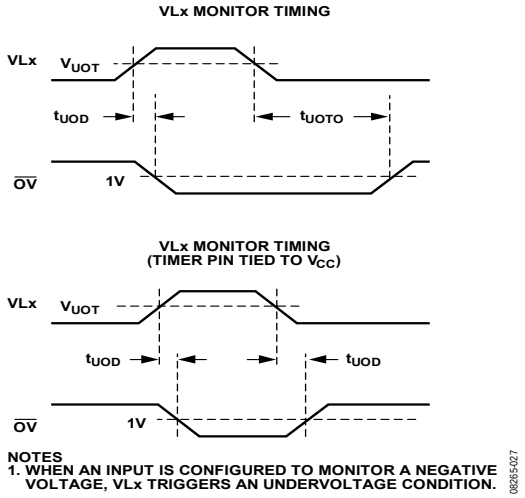


Figure 22. VLx Positive Voltage Monitoring Timing Diagrams

$\overline{UV}/\overline{OV}$ OUTPUT CHARACTERISTICS

Both the $\overline{OV}$ and $\overline{UV}$ outputs have strong pull-down to ground and weak internal pull-up to V_{CC}. This permits the pins to behave as open-drain outputs. When the rise time on the pin is not critical, the weak pull-up removes the requirement for an external pull-up resistor. The open-drain configuration allows for wire-OR'ing of outputs, which is particularly useful when more than one signal needs to pull down on the output.

At V_{CC} = 1 V, a maximum V_{OL} = 0.15 V at $\overline{UV}$ is guaranteed. At V_{CC} = 1 V, the weak pull-up current on $\overline{OV}$ is almost turned on. Consequently, if the state and pull-up strength of the $\overline{OV}$ pin is important at very low V_{CC}, an external pull-up resistor of no more than 100 kΩ is advised. By adding an external pull-up resistor, the pull-up strength on the $\overline{OV}$ pin is greater. Therefore, if it is connected in a wire-OR'ed configuration, the pull-down strength of any single device must account for this additional pull-up strength.

GLITCH IMMUNITY

The ADM12914 is immune to short transients that may occur on the monitored voltage rails. The device contains internal filtering circuitry that provides immunity to fast transient glitches. Figure 9 illustrates glitch immunity performance by showing the maximum transient duration without causing a reset pulse. Glitch immunity makes the ADM12914 suitable for use in noisy environments.

UNDERVOLTAGE LOCKOUT (UVLO)

The ADM12914 has an undervoltage lockout circuit that monitors the voltage on the V_{CC} pin. When the voltage on V_{CC} drops below 1.94 V (minimum), the circuit activates. The $\overline{UV}$ output is asserted and the $\overline{OV}$ output is cleared and is not allowed to assert. When V_{CC} recovers, $\overline{UV}$ exhibits the same timing characteristics as though an undervoltage condition had occurred on the inputs.

SHUNT REGULATOR

The ADM12914 is powered via the V_{CC} pin. The V_{CC} pin can be directly connected to a voltage rail of up to 6 V. In this mode, the supply current of the device does not exceed 100 µA. An internal shunt regulator allows the ADM12914 to operate at voltage levels greater than 6 V by simply placing a dropper resistor in series between the supply rail and the V_{CC} pin to limit the input current to less than 10 mA.

Once the supply voltage, V_{IN}, has been established, an appropriate value for the dropper resistor can be calculated. Begin by determining the maximum supply current required, $I_{CCtotal}$, by adding the current drawn from the reference and/or the pull resistors between the outputs and the V_{CC} pin to the maximum specified supply current. The minimum and maximum shunt regulator voltage specified in Table 1, $V_{SHUNT\ min}$ and $V_{SHUNT\ max}$, are also required in the following calculations.

Calculate the maximum and minimum dropper resistor values

$$R_{MAX} = \frac{V_{INmin} - V_{SHUNTmax}}{I_{CCtotal}}$$

$$R_{MIN} = \frac{V_{INmax} - V_{SHUNTmin}}{100\,\mu A}$$

Based on these values, choose a real-world resistor value within this range. Then, given the specified accuracy of this resistor, calculate the minimum and maximum real resistor value variation, $R_{REALmin}$ and $R_{REALmax}$, respectively.

The maximum device power is calculated as follows:

$$P_{DeviceMax} = V_{SHUNTmax}\left[\frac{\left(V_{IN\,max} - V_{SHUNTmax}\right)}{R_{REAL\,min}} - Icc_{TOTAL}\right] + V_{SHUNTmax} I_{CCtotal}$$

To check that the calculated value of the resistor will be acceptable, calculate the maximum device temperature rise

$$Temp_{RISEmax} = \theta_{JA} P_{DeviceMax}$$

Add this value to the ambient operating temperature. If the resistor value is acceptable, the result will lie within the specified operating temperature range of the device.

$\overline{OV}$ LATCH (ADM12914-1)

If an overvoltage condition occurs when the $\overline{LATCH}$ pin is pulled low, the $\overline{OV}$ pin latches low. Pulling the $\overline{LATCH}$ pin high clears the latch. If an overvoltage condition clears while the $\overline{LATCH}$ pin is high, the latch is bypassed and the $\overline{OV}$ pin behaves in the same way as the $\overline{UV}$ pin, with an identical timeout period. If the $\overline{LATCH}$ pin is pulled low while the timeout period is active, the $\overline{OV}$ pin latches low, as in normal operation.

If the $\overline{LATCH}$ pin is kept low during the device power up, a false positive overvoltage condition is reported by the IC. This is due to uncertainties between the rising internal reference voltage and the voltages being monitored and is more evident if the device is configured for negative voltage monitoring. It is recommended to add a delay circuit shown in Figure 23 to temporarily pull the $\overline{LATCH}$ pin high during the device power up period until the supply and reference voltage stabilize.

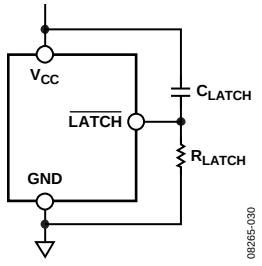


Figure 23. $\overline{LATCH}$ Pin Delay Circuit

Calculate the component values using the following equation:

$$C_{LATCH} = \frac{-t_{DELAY}}{\ln\left(\frac{0.8}{V_{CC}}\right) \times R_{LATCH}}$$

where:
V_{CC} is the final supply voltage on the VCC pin.
t_{DELAY} is the estimated delay between the VCC pin power up to the $\overline{\text{LATCH}}$ pin voltage dropping below threshold low voltage.

The exact delay time required, depending on the VCC power up profile and ramping rate, is always longer than the VCC rise time plus a few milliseconds for margin. Some component value combinations are shown in Table 6.

Table 6. Standard Component Values of the Latch Delay Circuit

V_{CC} (V)	t_{DELAY} (ms)	R_{LATCH} (kΩ)	C_{LATCH} (µF)
3.3	10	10.5	0.68
	100	105	0.68
5	10	12	0.47
	100	120	0.47
6.6	10	10	0.47
	100	10	0.47

DISABLE (ADM12914-2)

Pulling the DIS pin high disables both the $\overline{\text{UV}}$ and $\overline{\text{OV}}$ outputs, and forces both outputs to remain weakly pulled high, regardless of any faults that are detected at the inputs. If a UVLO condition is detected, the $\overline{\text{UV}}$ output is asserted and pulls low; however, the timeout function is bypassed. As soon as the UVLO condition clears, the $\overline{\text{UV}}$ output pulls high. To guarantee normal operation when the pin is left unconnected, DIS has a weak 2 µA internal pull-down current.

TYPICAL APPLICATIONS

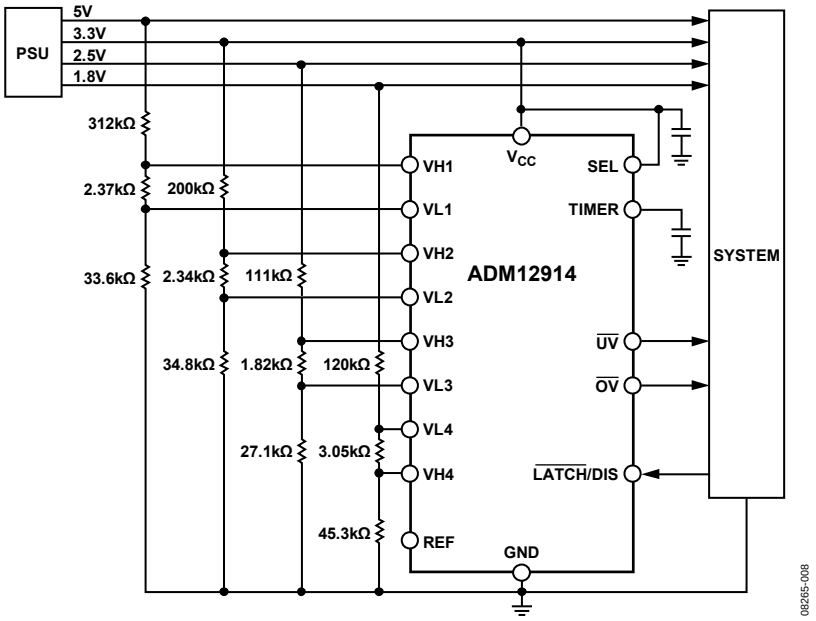


Figure 24. Typical Application Diagram for Monitoring 5 V, 3.3 V, 2.5 V, and 1.8 V with 1.5% Supply Tolerance and 5% Input Tolerance Requirement

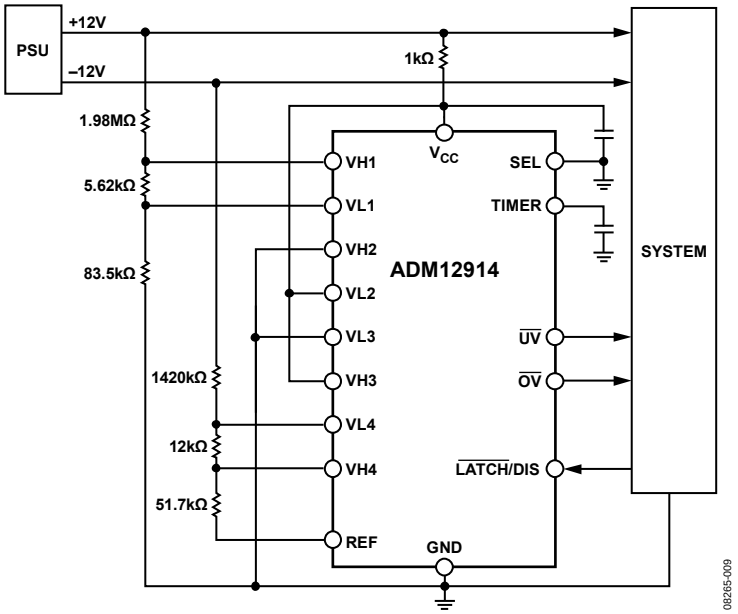
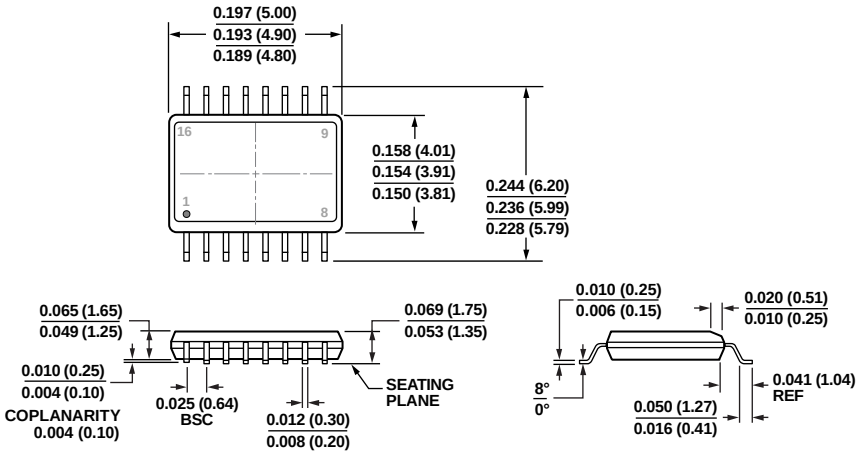


Figure 25. Typical Application Diagram for Monitoring 12 V with 1.5% Supply Tolerance and 5% Input Tolerance Requirement; –12 V with 3% Supply Tolerance and 15% Input Tolerance Requirement

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

09-12-2014-A

Figure 26. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM12914-1ARQZ	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADM12914-1ARQZ-RL7	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADM12914-2ARQZ	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADM12914-2ARQZ-RL7	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16

[1] Z = RoHS Compliant Part.

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