Click here for production status of specific part numbers.

MAX20014

2.2MHz Sync Boost and Dual Step-Down Converters

General Description

The MAX20014 is a high-efficiency three-output low-voltage DC-DC converter. OUT1 boosts the input supply up to 8.5V at up to 750mA, while two synchronous step-down converters operate from a 3.0V to 5.5V input voltage range and provides a 0.8V to 3.8V output voltage range at up to 3A. The boost converter achieves ±2% and the buck converters achieve ±1.5% output error over load, line, and temperature range.

The device features a 2.2MHz fixed-frequency pulse-width modulation (PWM) mode for better noise immunity and load transient response, and a pulse-frequency modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows for the use of all-ceramic capacitors and minimizes external components footprint. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions.

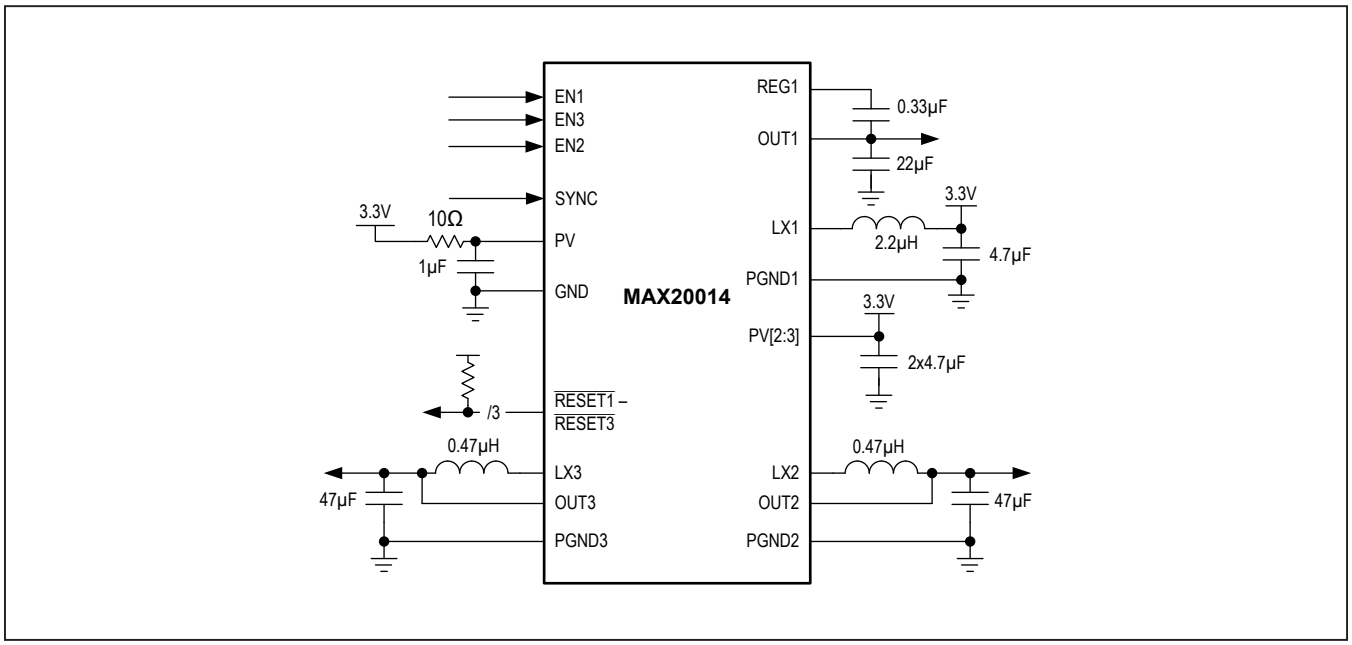
The device is offered with factory-preset output voltages or resistor-adjustable output voltages. Other features include soft-start, overcurrent, and overtemperature protections.

Benefits and Features

- Multiple Functions for Small Size
  - Synchronous 750mA Boost Converter
    - Fixed from 3.8V to 8.5V in 100mV Steps
  - Dual Synchronous Buck Converters Up to 3A
    - Factory-Configurable Output Voltages from 0.8V to 3.8V in 25mV Steps
    - Resistor Adjustable
  - 3.0V to 5.5V Operating Supply Voltage
  - 2.2MHz Operation
  - Undervoltage Threshold of 93% ±3%
  - Overvoltage Threshold of 107% ±3%
  - Individual $\overline{\text{RESET}}$_ Outputs
- High-Precision
  - ±1.5% Output-Voltage Accuracy
  - Good Load Transient Performance for Buck Converters
- Robust for the Automotive Environment
  - Current Mode, Forced-PWM, and Skip Operation
  - Overtemperature and Short-Circuit Protection
  - 4mm x 4mm 24-Pin TQFN
  - -40°C to +125°C Automotive Temperature Range

***Ordering Information/Selector Guide* appears at end of data sheet.**

Typical Operating Circuit



maxim integrated™

Absolute Maximum Ratings

PV2, PV3 to PGND_ ..... -0.3V to +6V
PV to GND ..... -0.3V to +6V
REG1 to GND ..... -0.3V to V_{OUT1} + 0.3V
EN1–EN3, SYNC to GND ..... -0.3V to V_{PV} + 0.3V
$\overline{RESET1}$–$\overline{RESET3}$, GND ..... -0.3V to +6V
OUT1 to PGND1 ..... -0.3V to +10V
OUT2 to PGND2 ..... -0.3V to V_{PV2} + 0.3V
OUT3 to PGND3 ..... -0.3V to V_{PV3} + 0.3V
LX1 to PGND1 ..... -0.3V to V_{OUT1} + 0.3V
LX2 to PGND2 ..... -0.3V to V_{PV2} + 0.3V
LX3 to PGND3 ..... -0.3V to V_{PV3} + 0.3V
GND to PGND ..... -0.3V to +0.3V
LX1 Continuous RMS Current 2A
LX2, LX3 Continuous RMS Current 3A
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
TQFN-EP (derate 30.3 mW/°C > +70°C) 2222mW
Operating Temperature ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Range ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{PV} = V_{PV2} = V_{PV3} = 3.3V, EN1 = EN2 = EN3 = 3.3V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}	Fully operational	3.0		5.5	V
Undervoltage Lockout (UVLO)	$UVLO_R$	Rising		2.7	2.9	V
	$UVLO_F$	Falling	2.4	2.6		
Shutdown Supply Current	$I_{IN-SHDN}$	EN1–EN3 = low	1	2.2	5	µA
Supply Current	I_{IN1}	EN1 = high, I_{OUT1} = 0mA, skip, V_{OUT1} 2% above regulation point	70	135	210	µA
	I_{IN2}	EN2 = high, I_{OUT2} = 0mA, skip, V_{OUT2} 2% above regulation point	40	80	160	
	I_{IN3}	EN3 = high, I_{OUT3} = 0mA, skip, V_{OUT3} 2% above regulation point	40	80	160	
PWM Switching Frequency	f_{SW}	Internally generated	2.0	2.2	2.4	MHz
Spread Spectrum	SS	Factory option enabled		±3		%
OUT1 SYNCHRONOUS DC-DC BOOST CONVERTER						
Voltage Accuracy	V_{OUT1}	I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{IN} ≤ 3.6V	-2		+2	%
pMOS On-Resistance	R_{HS1}	V_{PV} = V_{PV2} = 3.3V, I_{LX1} = 0.1A	125	250	500	mΩ
nMOS On-Resistance	R_{LS1}	V_{PV} = V_{PV2} = 3.3V, I_{LX1} = 0.1A	75	150	300	mΩ
nMOS Current-Limit Threshold	I_{LIM1}		1.6	2		A
pMOS Turn-Off Threshold	I_{ZX1}		15	50	90	mA

Electrical Characteristics (continued)

(V_{PV} = V_{PV2} = V_{PV3} = 3.3V, EN1 = EN2 = EN3 = 3.3V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX1 Leakage Current	I_{LX1LKG}	V_{PV} = V_{PV2} = 6V, LX1 = PGND1 or OUT1, T_A = 25°C	-1	+0.1	+1	µA
Maximum Duty Cycle	DC_{MAX1}			75		%
OUT1 Discharge Resistance	R_{DIS1}	V_{EN1} = 0V, V_{OUT1} = 1V	200	440	700	Ω
OUT1 Discharge Current	I_{DIS1}	V_{EN1} = 0V, V_{OUT1} = regulation point	4	10	18	mA
Switching Phase	PH_{LX1}	With respect to LX3 rising edge		20		deg
REG1 to OUT1	V_{REG1}	V_{OUT1} > 4.5V	-5.1	-4.5	-3.9	V
Skip Threshold	$SKIP_1$	Percentage of nMOS current-limit threshold	5	15	30	%
Soft-Start Time	t_{SS1}			1.9		ms
OUT2 SYNCHRONOUS STEP-DOWN CONVERTER						
Voltage Accuracy	V_{OUT2}	I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{PV} ≤ 5.5V, PWM mode selected	-1.5		+1.5	%
pMOS On-Resistance	R_{HS2}	V_{PV} = V_{PV2} = 3.3V, I_{LX2} = 0.2A	35	82	150	mΩ
nMOS On-Resistance	R_{LS2}	V_{PV} = V_{PV2} = 3.3V, I_{LX2} = 0.2A	20	50	100	mΩ
pMOS Current-Limit Threshold	I_{LIM2-1}	Factory option 1 (1A)	1.4	1.9		A
	I_{LIM2-2}	Factory option 2 (2A)	2.8	3.8		
	I_{LIM2-3}	Factory option 3 (3A)	4.5	5.8		
	I_{LIM2-4}	Factory option 4 (3.6A)	5.1	6.5		
nMOS Zero-Crossing Threshold	I_{ZX2}			150		mA
Maximum Duty Cycle	DC_{MAX2}				100	%
Minimum On-Time	$t_{MINTON2}$		25	44	68	ns
LX2 Discharge Resistance	R_{DIS2}	V_{EN2} = 0V (connected to LX2)	20	40	80	Ω
Switching Phase	PH_{LX2}			180		deg
Skip Threshold	$SKIP_2$	Percentage of pMOS current-limit threshold	4	12	20	%
Soft-Start Time	t_{SS2}			2.5		ms
OUT3 SYNCHRONOUS STEP-DOWN CONVERTER						
Voltage Accuracy	V_{OUT3}	I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{PV} ≤ 5.5V, PWM mode selected	-1.5		+1.5	%
pMOS On-Resistance	R_{HS3}	V_{PV} = V_{PV3} = 3.3V, I_{LX3} = 0.2A	35	82	150	mΩ
nMOS On-Resistance	R_{LS3}	V_{PV} = V_{PV3} = 3.3V, I_{LX3} = 0.2A	20	50	100	mΩ
pMOS Current-Limit Threshold	I_{LIM3-1}	Option 1 (1A)	1.4	1.9		A
	I_{LIM3-2}	Option 2 (2A)	2.8	3.8		
	I_{LIM3-3}	Option 3 (3A)	4.5	5.8		
	I_{LIM3-4}	Factory option 4 (3.6A)	5.1	6.5		
nMOS Zero-Crossing Threshold	I_{ZX3}			150		mA

Electrical Characteristics (continued)

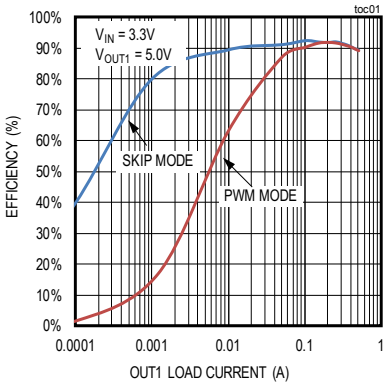
(V_{PV} = V_{PV2} = V_{PV3} = 3.3V, EN1 = EN2 = EN3 = 3.3V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Duty Cycle	DC_{MAX3}				100	%
Minimum On-Time	$t_{MINTON3}$		25	44	68	ns
LX3 Discharge Resistance	R_{DIS3}	V_{EN3} = 0V (connected to LX3)	20	40	80	Ω
Switching Phase	PH_{LX3}	With respect to LX3 rising edge		0		deg
Skip Threshold	$SKIP_3$	Percentage of pMOS current-limit treshold	4	12	20	%
Soft-Start Time	t_{SS3}			2.5		ms
THERMAL OVERLOAD						
Thermal-Shutdown Temperature	T_{SHDN}	T_J rising		165		°C
Hysteresis	T_{HYST}			15		°C
OUT1–OUT3 OPEN-DRAIN RESET OUTPUTS ($\overline{RESET1}$–$\overline{RESET3}$)						
Overvoltage Threshold	OV	Rising, % of nominal output	104	107	110	%
Undervoltage Threshold	UV	Falling, % of nominal output	90	93	96	%
Active Hold Period	t_{HOLD}			7.4		ms
Delay Filter	t_{PVDEL}	10% below/above threshold		10		µs
RESET1–RESET3 High-Leakage Current	$I_{PVOVLKG}$		-0.5	+0.1	+0.5	µA
Output Low Level	V_{PVOL}	3.0V ≤ V_{PV} ≤ 5.5V, sinking 2mA			0.2	V
EN1–EN3 AND SYNC INPUTS						
Input High Level	V_{IH}		1.5			V
Input Low Level	V_{IL}				0.5	V
Input Hysteresis	V_{ENHYST}			0.1		V
EN1–EN3 Input Pulldown Current	I_{EN_PD}	V_{PV} = 5.0V, T_A = +25°C	0.2	0.5		µA
EN1–EN3 Leakage Current	I_{ENLKG}	0 ≤ V_{PV} ≤ 5.5V, T_A = +25°C	-1	0.1	+1	µA
SYNC Input Pulldown	R_{SYNCPD}		50	100	200	kΩ
SYNC Input Frequency Range	f_{SYNC}		1.8		2.6	MHz
SYNC OUTPUT						
Output Low	V_{OL}	V_{PV} = 3.3V, I_{SINK} = 2mA			0.4	V
Output High	V_{OH}	V_{PV} = 3.3V, I_{SOURCE} = 2mA	2.7			V

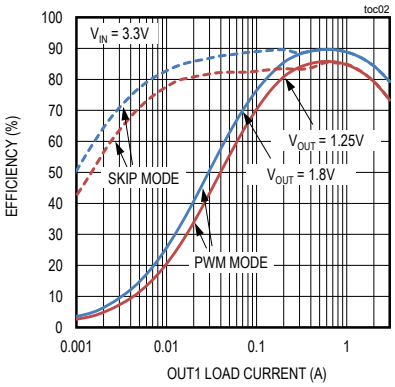
Note 2: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design.

Typical Operating Characteristics

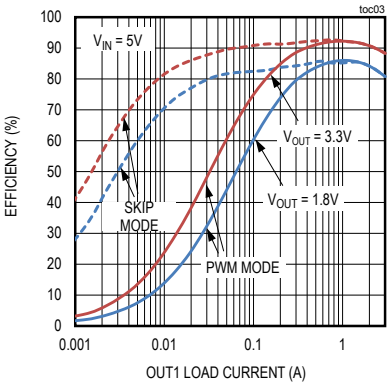
OUT1 EFFICIENCY



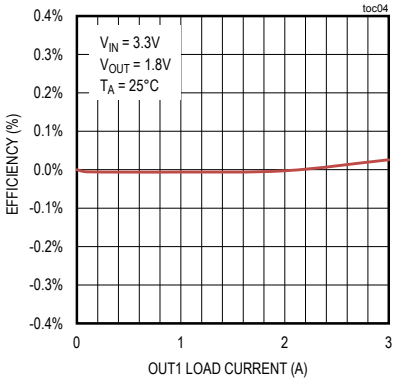
OUT2/3 EFFICIENCY



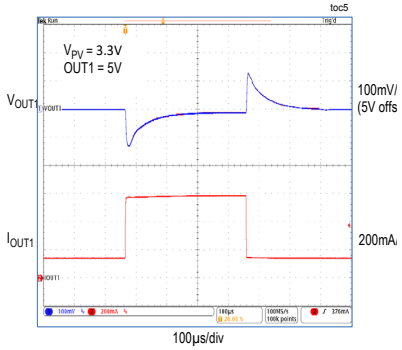
OUT2/3 EFFICIENCY



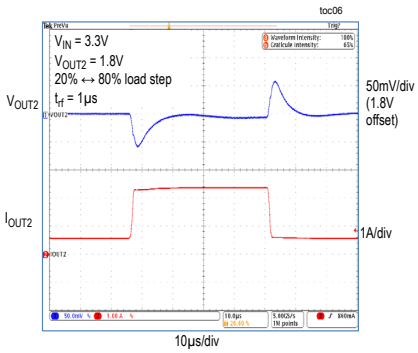
OUT2/3 LOAD REGULATION



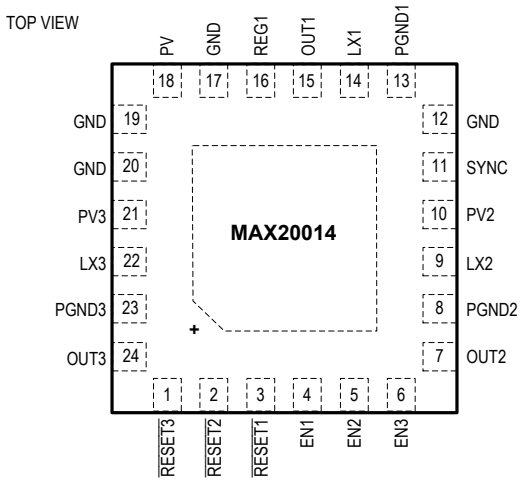
OUT1 LOAD TRANSIENT (PWM MODE)



OUT2/3 LOAD TRANSIENT (PWM MODE)



Pin Configurations



TQFN
4mm x 4mm

Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{RESET3}}$	Open-Drain RESET Output for OUT3. To obtain a logic signal, pull up $\overline{\text{RESET3}}$ with an external resistor.
2	$\overline{\text{RESET2}}$	Open-Drain RESET Output for OUT2. To obtain a logic signal, pull up $\overline{\text{RESET2}}$ with an external resistor.
3	$\overline{\text{RESET1}}$	Open-Drain RESET Output for OUT1. To obtain a logic signal, pull up $\overline{\text{RESET1}}$ with an external resistor.
4	EN1	Active-High Enable Input for OUT1. Drive EN1 high for normal operation.
5	EN2	Active-High Enable Input for OUT2. Drive EN2 high for normal operation.
6	EN3	Active-High Enable Input for OUT3. Drive EN3 high for normal operation.
7	OUT2	OUT2 Voltage Sense Input/Feedback Pin
8	PGND2	Power Ground for OUT2. Connect all PGND pins together.
9	LX2	Inductor Connection. Connect LX2 to the switched side of the inductor.
10	PV2	Power Input Supply for OUT2. Connect a 4.7µF ceramic capacitor from PV2 to PGND2.
11	SYNC	SYNC I/O. When configured as an input, connect SYNC to GND or leave unconnected to enable skip-mode operation under light loads. Connect SYNC to PV or an external clock to enable fixed-frequency forced-PWM-mode operation. When configured as an output (factory-configured), connect SYNC to other devices SYNC inputs.
12	GND	Unused. Connect to ground.
13	PGND1	Power Ground. Connect all PGND pins together.
14	LX1	Inductor Connection. Connect LX1 to the switched side of the inductor.
15	OUT1	OUT1 Voltage Output
16	REG1	Floating Supply for OUT1. Connect a 0.33µF ceramic capacitor from REG1 to OUT1.
17	GND	Analog Ground
18	PV	Analog Input Supply. Connect a 1µF or larger ceramic capacitor from PV to GND with a 10Ω resistor in series to the supply voltage.

Pin Description (continued)

PIN	NAME	FUNCTION
19, 20	GND	Unused. Connect to ground.
21	PV3	Power Input Supply for OUT3. Connect a 4.7µF ceramic capacitor from PV3 to PGND3.
22	LX3	Inductor Connection. Connect LX3 to the switched side of the inductor.
23	PGND3	Power Ground for OUT3. Connect all PGND pins together.
24	OUT3	OUT3 Voltage Sense Input/Feedback
—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Detailed Description

The MAX20014 is a high-efficiency three-output low-voltage DC-DC converter. OUT1 is a 750mA (typ) synchronous DC-DC boost converter that boosts the 3.0V to 5.5V input supply to a factory-set fixed-output voltage between 3.8V and 8.5V in 100mV steps. The boost converter has true shutdown so the output voltage is 0V when off. The two synchronous step-down converters (OUT2, OUT3) operate from a 3.0V to 5.5V input voltage and provide a 0.8V to 3.80V output voltage at up to 3A. OUT2 and OUT3 can be factory set to a fixed voltage or resistor adjustable. The boost converter achieves ±2% and the buck converters achieve ±1.5% output error over load, line, and temperature range.

The device features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response, and a pulse-frequency modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows for the use of all-ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. The spread modulation can be factory set to pseudorandom. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions.

The device contains high-accuracy overvoltage/undervoltage thresholds for each output that is mapped to the $\overline{RESET1}$–$\overline{RESET3}$] pins. There are diagnostics on $\overline{RESET1}$–$\overline{RESET3}$] and OUT1–OUT3 to guarantee high reliablilty and fail-safe operation.

In light-load applications, a logic input (SYNC) allows the devices to operate either in skip mode for reduced current consumption, or fixed-frequency, forced-PWM mode to eliminate frequency variation, and help minimize EMI. Protection features include cycle-by-cycle current limit, and thermal shutdown with automatic recovery.

Enable Inputs (EN1–EN3)

The enable control inputs (EN1–EN3) activate the device channel from their low-power shutdown state. EN1–EN3 have an input threshold of 1.0V (typ) with hysteresis of 100mV (typ). EN1–EN3 are fully independent with no timing restrictions between each other. When an enable input goes high, the associated output voltage ramps up with the programmed soft-start time.

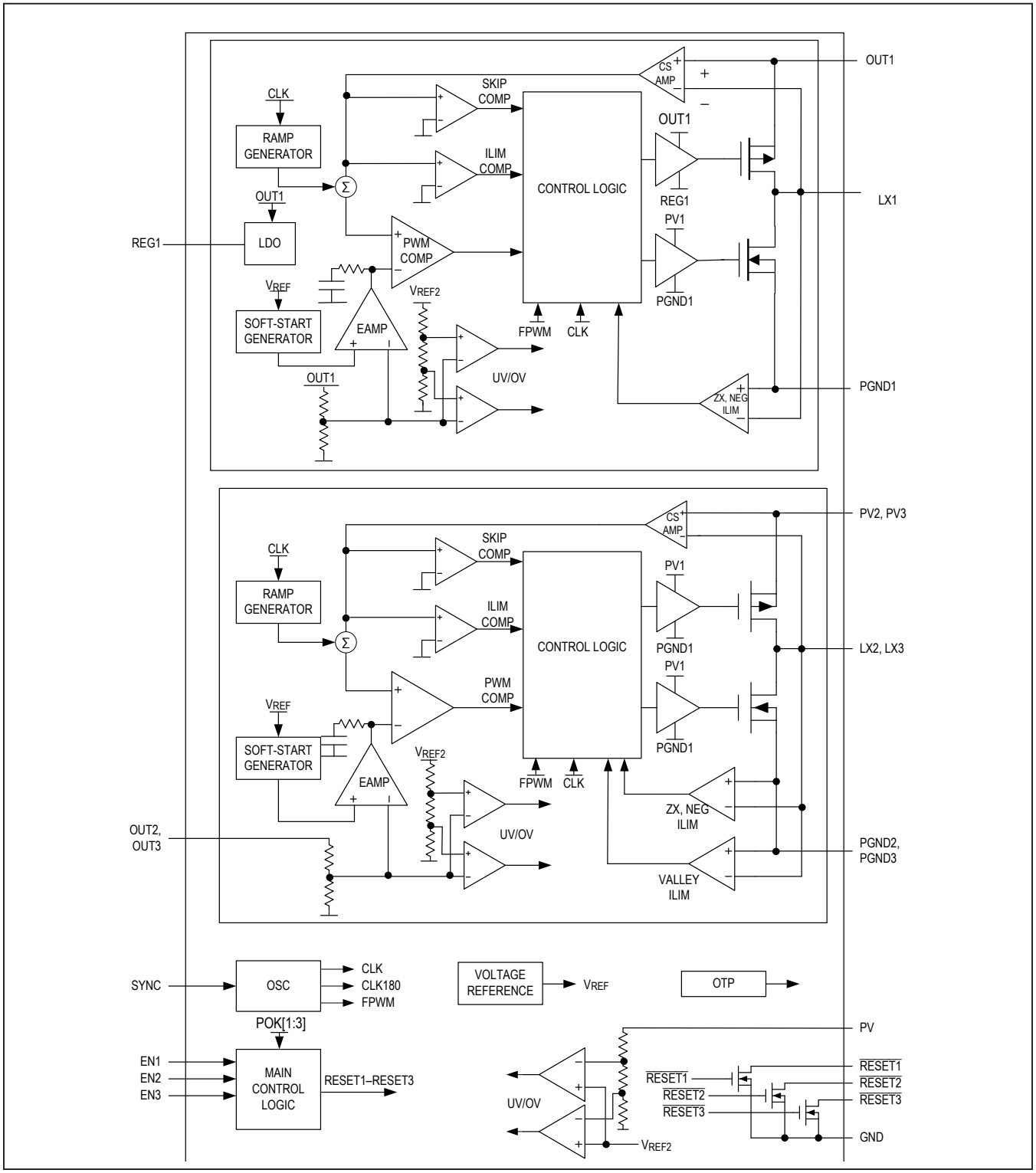
Reset Outputs ($\overline{RESET1}$–$\overline{RESET3}$)

The device features individual open-drain reset outputs for each output that asserts low when the corresponding output voltage is outside of the UV/OV window. $\overline{RESET1}$–$\overline{RESET3}$ remain asserted for a fixed timeout period after the output rises up to its regulated voltage. The fixed timeout period is selectable between 0.8ms, 3.7ms, 7.4ms (default), or 14.9ms. See the *Ordering Information/Selector Guide* table. To obtain a logic signal, place a pullup resistor between the $\overline{RESET1}$–$\overline{RESET3}$ pins to the system I/O voltage.

Feedback Pins (OUT1–OUT3)

The output voltage is fed back to the coresponding OUT_ feedback pin to close the regulation loop. If this connection is open, the output turns off to prevent open-loop operation that would normally result in the output being driven to the input supply voltage. For a fixed-output voltage, connect OUT_ directly to the output. For an adjustable-output voltage, connect a resistor-divider to the output and connect OUT_ to the midpoint. The boost converter output is not resistor adjustable.

Internal Block Diagram



Internal Oscillator

The device has a spread-spectrum oscillator that varies the internal operating frequency up by ±3% relative to the internally generated operating frequency of 2.2MHz (typ). This function does not apply to externally applied oscillation frequency. The spread frequency generated is pseudorandom, with a repeat rate well below the audio band.

Synchronization (SYNC)

SYNC is factory-programmable I/O. See the *Ordering Information/Selector Guide* table for available options. When configured as an input, a logic-high on SYNC enables fixed-frequency, forced-PWM mode. Apply an external clock on the SYNC input to synchronize the internal oscillator to an external clock. The SYNC input accepts signal frequencies in the range of 1.8MHz < f_{SYNC} < 2.6MHz. When the pin is open or logic-low, the SYNC input enables the device to enter a low-power skip mode under light-load conditions. When configured as an output, SYNC outputs the internally generated 2.2MHz clock that switches from PV to GND. All converters operate in forced-PWM mode when SYNC is configured as an output.

Soft-Start

The device includes a fixed soft-start of 1.9ms for OUT1 and 2.5ms for OUT2/OUT3. Soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

OUT3 Load-Switch Option

OUT3 of the device can be factory trimmed to operate as a load switch. In this configuration, LX3 becomes the output and OUT3 must be connected to GND. When EN3 goes high, the high-side pMOS current ramps from 0 to I_{MAX} in 500µs (typ) to limit the inrush current. The pMOS switch is also protected from short circuit. When a short circuit is detected, the pMOS turns off and reinitiates a soft-start sequence. For proper operation, the peak current through the pMOS switch must be kept below 4.2A during soft-start. This limits the maximum output capacitor value depending on the output voltage and load conditions. It is recommended that the output capacitor does not exceed 47µF.

When configured as a load switch, the $\overline{\text{RESET3}}$ output indicates when the pMOS switch is fully closed and not the actual voltage on the output. The normal hold time still applies.

Current Limit/Short-Circuit Protection

The device features current limit that protects the device against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current crosses below the low-side MOSFET current-limit threshold, the converter turns on the high-side MOSFET again. This cycle repeats until the short or overload condition is removed.

PWM and Skip Modes

The device features a SYNC input that puts the converter either in skip mode for forced-PWM mode of operation. See the *Pin Description* table for more details. In PWM mode, the converter switches at a constant frequency with variable on-time. In skip mode of operation, the converter's switching frequency is load dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off as often as is the case in PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the MAX20014. When the junction temperature exceeds +165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the device to cool. The thermal sensor turns on the device again after the junction temperature cools by 15°C.

Applications Information

Input Capacitors

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. A 4.7µF X7R ceramic capacitor is recommended for the PV2 and PV3 pins, as well as the supply side pin of the boost inductor. A 1.0µF X7R ceramic capacitor is recommended for the PV pin, with a 10Ω resistor in series to the input supply.

Boost Inductor Selection and Output Current

Proper choice of inductor for the boost converter is based on ripple current and slope compensation. Ripple current (I_{PK-PK}) is usually specified as a percentage of the average input current. 33% peak-to-peak ripple provides a reasonable balance between inductor size, DCR, and core losses.

The peak boost input current limit is 1.6A (min), so the average current as a function of I_{PK-PK} is shown below.

Equation 1:

$$I_{IN} = 1.6/(1 + I_{PK-PK}/2)$$

For 33% ripple, this equates to 1.37A for I_{IN} and 0.45A ripple current (denoted I_{Δ}, which has a unit of A, as opposed to I_{PK-PK}, which is a percentage). With the maximum average current I_{IN} known, the maximum output current for a given duty cycle (D) is shown below.

Equation 2:

$$I_{OUT-MAX} = (1-D) \times I_{IN}$$

where (see Equation 3):

Equation 3:

$$D = 1 - \eta \times V_{IN}/V_{OUT}$$

If η (efficiency) is not known, it must be measured or estimated. A good efficiency estimate is 0.9 (90%) for V_{OUT}/V_{IN} ratios of 1.5 or less, and 0.8 for V_{OUT}/V_{IN} ratios near 2.5.

The approximate minimum inductance necessary to achieve a given ripple current I_{Δ} is shown below.

Equation 4:

$$L_{MIN1} = (V_{IN} \times D)/(f_{SW} \times I_{\Delta})$$

The second factor in inductor selection is slope compensation. The inductor current down-slope (m2) must be less than twice the internal slope compensation down-ramp (m1) to dampen oscillations in the inductor current waveform. Perfect deadbeat control occurs when the two downslopes are equal. The inductor current downslope is given by the formula below.

Equation 5:

$$m2 = (V_{OUT} - V_{IN})/L$$

The internal slope compensation ramp for the boost channel is set at 0.630 V/µs, and the R_{CS} for the boost channel is fixed at 0.330Ω. This provides a compensation ramp downslope of:

Equation 6:

$$m1 = 0.630/R_{CS}$$

Setting the inequality, adding in a margin factor of 1.3 for device and component variation, and rearranging for inductance gives the following.

Equation 7:

$$L_{MIN2} \geq 1.3 \cdot R_{CS} \times (V_{OUT} - V_{IN})/(0.630 \times 2)$$

This gives the minimum inductance necessary for satisfying slope compensation (half inductor downslope). The minimum inductance acceptable for use is the greater of the two calculated minimum values.

Equation 8:

$$L_{MIN} = \max(L_{MIN1}, L_{MIN2})$$

The maximum recommended inductance is twice the minimum value.

Equation 9:

$$L_{MIN} < L_{NOM} < 2 \times L_{MIN}$$

Soft-saturation type inductors are recommended, as they maintain a measure of effective inductance even when driven past their saturation points during fault conditions. If a ferrite-based inductor is used, then the saturation current must be higher than the maximum current limit in order to help protect the part during continuous output short-circuit events.

Buck Inductor Selection

Three key inductor parameters must be specified for operation with the MAX20014: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the maximum output current capability of the output. A lower inductor value minimizes size and cost, improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels especially when the inductance is increased without also allowing for larger inductor dimensions. The MAX20014 is designed for ΔI_{P-P} equal to ~30% of the full load current. Use the following equation to calculate the inductance.

Equation 10:

$$L_{MIN1} = \frac{(V_{IN} - V_{OUT\_}) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{MAX} \times 30\%}$$

V_{IN}	The nominal input voltage (3.3V or 5V, typ).
$V_{OUT\_}$	The nominal output voltage.
I_{MAX}	1A, 2A, or 3A depending on part number and channel. Use the maximum output capability of the output channel for the channel being used.
f_{SW}	The operating frequency. This value is 2.2MHz unless externally synchronized to a different frequency.

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency (f_{SW}) is 2.2MHz. The maximum output capability (I_{MAX}) is 1A, 2A, or 3A based on the specific part number of the device. See the *Boost Output Capacitor* section to verify that the worst-case output ripple is acceptable. The inductor saturation current is also important to avoid runaway current during continuous output short circuit.

The next equation ensures that the inductor current downslope is less than the internal slope compensation. For this to be the case, the following equation needs to be satisfied.

Equation 11:

$$-m \geq \frac{m2}{2}$$

where:

m2	The inductor current downslope. $\frac{V_{OUT}}{L} \times R_{CS}$
-m	Slope compensation. $\left[0.940 \frac{V}{\mu s}\right]$ for V_{OUT} > 3.2V fixed output. $\left[0.535 \frac{V}{\mu s}\right]$ for $V_{OUT} \leq$ 3.2V fixed output or adjustable output version.
R_{CS}	0.378Ω for 1A channel 0.263Ω for 2A channel 0.176Ω for 3A channel

Solving for L and adding a 1.3 multiplier to account for tolerances in the system, is shown below.

Equation 12:

$$L_{MIN2} = V_{OUT\_} \times \frac{R_{CS}}{2 \times m} \times 1.3$$

To satisfy both L_{MIN1} and L_{MIN2}, L_{MIN} must be set to the larger of the two.

Equation 13:

$$L_{MIN} = \text{Max}\ (L_{MIN1}, L_{MIN2})$$

The maximum inductor value recommended is 2 times the chosen value from the above formula.

Equation 14:

$$L_{MAX} = 2 \times L_{MIN}$$

Select a nominal inductor value based on the following formula. For optimal performance select the first standard inductor value greater than L_{MIN}.

Equation 15:

$$L_{MIN} < L_{NOM} < L_{MAX}$$

Boost Output Capacitor

The MAX20014 is designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended as the ESR zero can affect stability of the device. The output capacitor calculations below are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify proper stability is achieved.

Equation 16:

$$C_{OUT\_MIN} = \frac{50 \times A \times \mu s}{V_{OUT}}$$

$$C_{OUT1\_NOM} = \frac{100 \times A \times \mu s}{V_{OUT}}$$

Buck Output Capacitors

The MAX20014 is designed to be stable with low ESR ceramic capacitors. Other capacitor types are not recommended as the ESR zero can affect stability of the device. The output capacitor calculations below are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify that proper stability is achieved.

Equation 17:

$$C_{OUT23\_MIN} = 10.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

$$C_{OUT23\_NOM} = 27.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

$C_{OUT23-MIN}$	The minimum fully-derated output capacitance needed for a stable output.
$C_{OUT23-NOM}$	The nominal output capacitance.
I_{MAX}	The maximum DC current capability. Either 1A, 2A, or 3A. depending on the part number (see the *Ordering Information/Selector Guide*).
V_{OUT}	Nominal output voltage.

with C_{OUT23_MIN} defining the minimum fully derated output capacitance required for a stable output, and C_{OUT23_NOM} defining the nominal output capacitance for maximum phase margin. I_{MAX} is the maximum DC current capability of the associated output, as defined in the *Ordering Information/Selector Guide* table. V_{OUT} is the output voltage for the associated channel.

Adjustable Output-Voltage Option

The MAX20014 adjustable output-voltage version allows the customer to set the buck outputs to any voltage between 0.8V and approximately PV - 0.5V (see the *Ordering Information/Selector Guide*). The actual maximum output-voltage setting is limited by the specific application conditions and components. Connect a resistive divider from the output capacitor (V_{OUT}) to OUT_ to GND to set the output voltage (Figure 1). Select R_2 (OUT_ to GND resistor) ≤ 100kΩ. Calculate R_1 (V_{OUT} to OUT_ resistor) with the equation below.

Equation 18:

$$R_1 = R_2\left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]$$

where V_{FB} = 800mV (see the *Electrical Characteristics*).

The external feedback resistive divider must be frequency compensated for proper operation. Place a capacitor across R1 in the resistive-divider network. Use Equation 20 to determine the value of the capacitor.

Equation 19:

$$C_1 = 50\frac{R_2}{R_1}pF$$

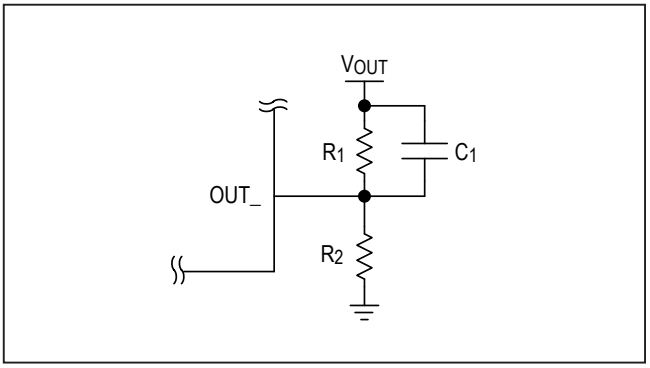


Figure 1. Adjustable Output-Voltage Configuration

PCB Layout Guidelines

For each converter, place the capacitor with the highest current ripple closest to the IC. For a buck converter, this is the input capacitor; for the boost converter, it is the output capacitor. Route the LX trace out from the IC underneath that capacitor (use a larger-package capacitor, such as 3.2mm x 1.6mm). Lastly, place the other capacitors close by with their ground pins very close to both the IC's ground pins and the other capacitor's ground pins. This configuration results in a closely-routed DC/DC converter that helps maintain performance and reduces EMI.

The layer directly below the IC and power components should be a continuous ground plane. Use multiple vias to provide good connections between that plane and component ground pins/pads. Split grounding should not be used.

The exposed pad (EP) of the IC is attached to the die with epoxy, providing a good way to dissipate thermal energy from the die. Connect the EP to all available ground planes below it using a grid of small vias in the EP land (3x3 grid of 0.3mm diameter vias is recommended).

Ordering Information/Selector Guide

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	V_{OUT1} (V)	V_{OUT2} (V)	I_{OUT2} (A)	V_{OUT3} (V)	I_{OUT3} (A)	t_{HOLD} (ms)	SS
MAX20014ATGA/V+	-40°C to +125°C	24 TQFN-EP*	5.0	ADJ	3	ADJ	3	7.4	Off
MAX20014ATGB/V+**	-40°C to +125°C	24 TQFN-EP*	6.5	ADJ	3	ADJ	3	7.4	Off
MAX20014ATGC/V+**	-40°C to +125°C	24 TQFN-EP*	5.0	1.2	3	1.8	3	7.4	Off
MAX20014ATGD/V+**	-40°C to +125°C	24 TQFN-EP*	7.5	ADJ	2	ADJ	1	7.4	On
MAX20014ATGE/V+**	-40°C to +125°C	24 TQFN-EP*	5.0	1.4	3	1.5	3	7.4	On
MAX20014ATGF/V+	-40°C to +125°C	24 TQFN-EP*	5.0	ADJ	3	ADJ	3	7.4	On

For variants with different options, contact factory.

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
***Future product—contact factory for availability.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP*	T2444+4C	21-0139	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/16	Initial release	—
1	5/18	Various updates	1–12
2	12/18	Added MAX20014ATGF/V+ to *Ordering Information/Selector Guide* table	13
3	3/19	Updated *Ordering Information/Selector Guide*	13

