40V Full-Bridge or Dual Half-Bridge Controller

FEATURES

- **Full-Bridge or Dual Half-Bridge Controller**
- **Dual Bidirectional, Rail-to-Rail Precision Current Monitors (200µV V_{OS})**
- **Dual On-Chip 16-Bit Monotonic DACs**
- **4-Wire SPI with Error Detection and Correction**
- **Quad N-Channel MOSFET 5.3V Gate Drivers**
- **V_{IN} Range: 5.5V to 40V**
- Configurable Output Current or Voltage Regulation
- Configurable PWM Control Methods for Loop Stability
- 100kHz to 1MHz Fixed Switching Frequency with SYNC and Spread Spectrum
- System Monitor and Fault Report via SPI Interface

APPLICATIONS

- Solenoid and Inductive Load Regulation
- Active or Semi-Active Damping Control
- Thermoelectric Cooler (TEC) Control
- Vibration Control

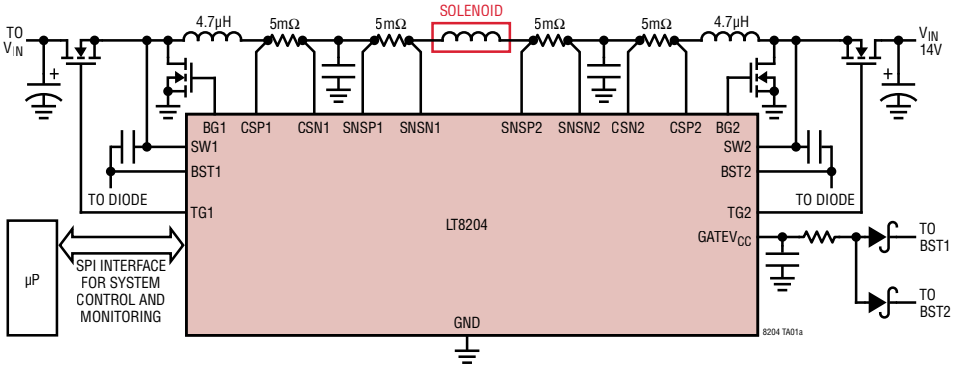
DESCRIPTION

The LT®8204 is a 40V full-bridge or dual half-bridge controller. It can be configured as either a four-switch full-bridge controller or dual two-switch half-bridge controllers to regulate either the output voltage or the output current. The LT8204 provides two selectable PWM control methods (i.e., peak current mode control and voltage mode control) to ease loop frequency compensation for applications with different load types (inductive, resistive, or capacitive loads).

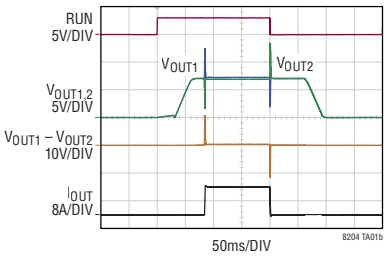
The LT8204 features dual bidirectional rail-to-rail precision (200µV V_{OS}) load current monitors, output voltage monitors, and dual on-chip 16-bit monotonic digital-to-analog converters (DACs). Together with the serial peripheral interface (SPI), the output current or voltage can be programmed precisely on-the-fly. The LT8204 also monitors the system operation status and reports via SPI interface in case of failure (e.g., loss of load connection, failure of external MOSFET devices).

TYPICAL APPLICATION

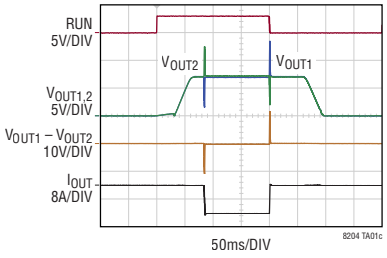
14V, ±8A Solenoid Driver



Soft Start Up and Shutdown with I_{OUT} = 8A



Soft Start Up and Shutdown with I_{OUT} = –8A



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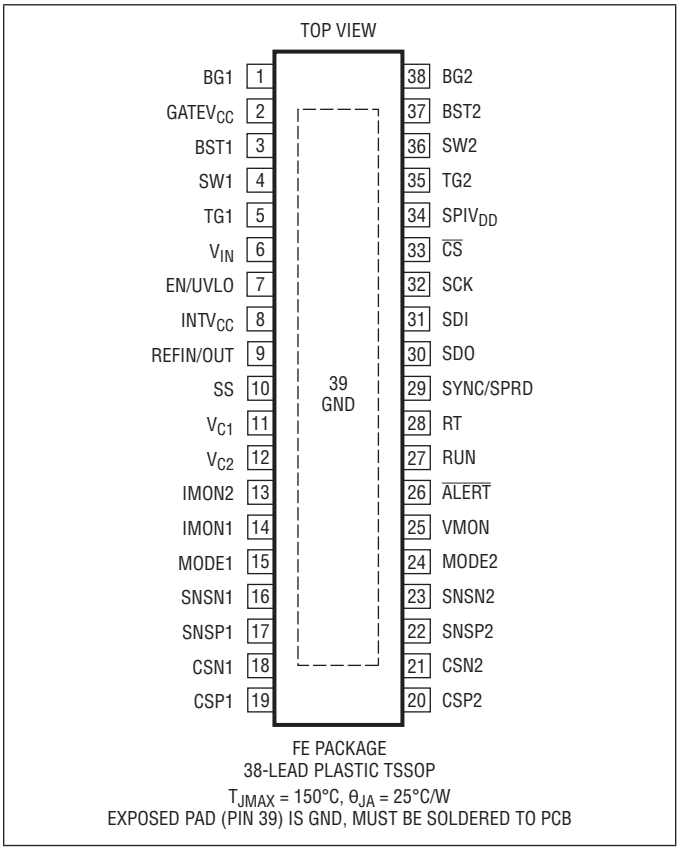
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UVLO ..... –0.3V to 40V
BST1, BST2 ..... –0.3V to 46V
BST1–SW1, BST2–SW2 ..... –0.3V to 6V
SW1, SW2 ..... –5V to 40V
CSP1, CSN1, CSP2, CSN2 ..... –5V to 40V
CSP1–CSN1, CSP2–CSN2 ..... ±0.3V
CSN1–CSN2 ..... ±40V
CSN1–SNSP1, CSN2–SNSP2 ..... ±0.3V
CSN1–SNSN1, CSN2–SNSN2 ..... ±0.3V
SNSP1, SNSN1, SNSP2, SNSN2 ..... –5V to 40V
SNSP1–SNSN1, SNSP2–SNSN2 ..... ±0.3V
REFIN/OUT, RUN, SS ..... –0.3V to 6V
$SPIV_{DD}$, $\overline{CS}$, SCK, SDI ..... –0.3V to 6V
SDO ..... –0.3V to Min ($SPIV_{DD}$ + 0.3V, 6V)
SYNC/SPRD, MODE1, MODE2, $\overline{ALERT}$ ..... –0.3V to 6V
$GATEV_{CC}$ ..... –0.3V to 6V
$INTV_{CC}$, RT, IMON1, IMON2, VMON, V_{C1}, V_{C2} ..... (Note 2)
TG1, TG2, BG1, BG2 ..... (Note 2)
Operating Junction Temperature (Notes 3, 4)
  LT8204R ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
  FE Package ..... 300°C

PIN CONFIGURATION



FE PACKAGE
38-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8204RFE#PBF	LT8204RFE#TRPBF	LT8204FE	38-Lead Plastic TSSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

For more information on lead free part marking, go to: http://www.adi.com/leadfree/
For more information on tape and reel specifications, go to: http://www.adi.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 14V, $V_{EN/UVLO}$ = V_{RUN} = 3V, V_{MODE1} = V_{MODE2} = GND, External $V_{REFIN/OUT}$ = 5V, V_{CSNX} = V_{CSPX} = V_{SNSNX} = V_{SNSPX} = 7V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Supplies and Regulators						
V_{IN} Operating Range		●	5.5		40	V
V_{IN} Quiescent Current (Not Switching)	V_{RUN} = 0.4V			5	10	mA
V_{IN} Standby Current	$V_{EN/UVLO}$ = 1.1V, V_{RUN} = 0.4V			500		µA
V_{IN} Shutdown Current	$V_{EN/UVLO}$ = 0.3V, V_{RUN} = 0.4V			1	2	µA
$INTV_{CC}$ Current Limit	$INTV_{CC}$ = 2.5V			60		mA
$INTV_{CC}$ Voltage	5.5V ≤ V_{IN} ≤ 40V, I_{INTVCC} = 10mA	●	5.148	5.200	5.226	V
$INTV_{CC}$ Load Regulation	I_{INTVCC} = 0mA to 20mA	●			0.2	%
$INTV_{CC}$ Undervoltage Lockout (UVLO)	$INTV_{CC}$ Falling		4.7	4.8	4.9	V
$INTV_{CC}$ UVLO Hysteresis				120		mV
$GATEV_{CC}$ Voltage			5.1	5.3	5.5	V
$GATEV_{CC}$ UVLO	$GATEV_{CC}$ Falling		4.3	4.4	4.5	V
$GATEV_{CC}$ UVLO Hysteresis				250		mV
$GATEV_{CC}$ Current Limit	$GATEV_{CC}$ = 4V			100		mA
REFIN/OUT Output Voltage	Internal 2.048V REF Mode	●	2.018	2.048	2.078	V
REFIN/OUT Output Voltage	Internal 4.096V REF Mode	●	4.036	4.096	4.156	V
REFIN/OUT Short-Circuit Current	Internal REF Mode, Forcing REFIN/OUT to GND			2.5		mA
REFIN/OUT Load Regulation	Internal REF Mode, I_{OUT} = 500µA			10		mV/mA
REFIN/OUT Input Voltage Range	External REF Mode	●	1.5		$INTV_{CC}$	V
REFIN/OUT Input Current	External REF Mode, $V_{REFIN/OUT}$ = 5V			300		µA
$SPIV_{DD}$ Voltage Range		●	1.80		5.25	V
$SPIV_{DD}$ Quiescent Current	$V_{\overline{CS}}$ = $SPIV_{DD}$ = 5.25V			6		µA
$SPIV_{DD}$ Shutdown Current	$V_{EN/UVLO}$ = 0.3V			0	1	µA
Switching Regulation Control						
EN/UVLO Shutdown Threshold	EN/UVLO Falling, Part Disabled, I_{VIN} < 10µA	●	0.3	0.6	1.0	V
EN/UVLO Threshold	EN/UVLO Falling, Part Stop Switching	●	1.17	1.20	1.23	V
EN/UVLO Hysteresis				25		mV
EN/UVLO Pin Current	$V_{EN/UVLO}$ = 0.3V $V_{EN/UVLO}$ = 1.2V, EN/UVLO Rising $V_{EN/UVLO}$ = 1.3V	●	1.6	0.5 2.0 0	2.6	µA µA µA
RUN High Level Input Voltage		●	1.30			V
RUN Low Level Input Voltage		●			0.55	V
RUN Resistance to GND				100		kΩ
SS Hard Pull-Down Resistance	V_{RUN} = 0.4V			250		Ω
SS Charging Current	V_{SS} = 1.5V		9	10	11	µA
SS Discharging Current	V_{SS} = 1.5V, V_{RUN} = 0.4V		9	10	11	µA
CSPx, CSNx Common Mode Operating Voltage Range		●	0		40	V
CSNx + CSPx + SNSPx + SNSNx Pin Current	$V_{EN/UVLO}$ = 0.3V, V_{RUN} = 0.4V, 0V < V_{CSPx} = V_{CSNx} = V_{SNSPx} = V_{SNSNx} < 40V	●		0.5	2	µA
CSNx Pin Current	V_{CSPx} = V_{CSNx} = 7V, V_{RUN} = 0.4V V_{CSPx} = V_{CSNx} = 0V, V_{RUN} = 0.4V			300 –10		µA µA

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CSPx Pin Current	V_{CSPx} = V_{CSNx} = 7V, V_{RUN} = 0.4V V_{CSPx} = V_{CSNx} = 0V, V_{RUN} = 0.4V	● ●	–1.5 –1.5	–1.0 –1.0	0 0	µA µA
Maximum Current Sense Threshold (V_{CSPx} – V_{CSNx})	Full-Bridge Configuration Positive Negative		 55 –95	 75 –75	 95 –55	 mV mV
	Dual Half-Bridge Configuration, Load-To-GND Positive		 55	 75	 95	 mV
	Dual Half-Bridge Configuration, Load-To-V_{IN} Negative		 –95	 –75	 –55	 mV
Error Amp g_m	V_{VC1} = V_{VC2} = 2V			1.2		mS
Maximum V_{C1} and V_{C2} Pin Current	Source Sink			–180 180		µA µA
Output Current Monitor						
SNSPx, SNSNx Common Mode Operating Voltage Range		●	0		40	V
SNSPx, SNSNx Pin Bias Current I_{Bx} I(SNSPx) = I(SNSNx) (Note 4)	V_{SNSPx} = V_{SNSNx} = 7V V_{SNSPx} = V_{SNSNx} = 0V	● ●	4.2 –8.4	6.3 –6.3	8.4 –4.2	µA µA
SNSPx, SNSNx Pin Offset Current I_{OSx}, I_{OSx} = I(SNSPx) – I(SNSNx) (Note 4)	V_{SNSPx} = V_{SNSNx} = 7V V_{SNSPx} = V_{SNSNx} = 0V	● ●	–1 –1		1 1	µA µA
SNSPx, SNSNx Differential Operating Voltage Range		●	–45		45	mV
V_{SNSPx} – V_{SNSNx} to IMONx Voltage Gain	V_{SNSPx} = 0V, V_{SNSPx} – V_{SNSNx} = ±45mV V_{SNSPx} = 40V, V_{SNSPx} – V_{SNSNx} = ±45mV	● ●	49.8 49.8	50 50	50.2 50.2	mV/mV mV/mV
V_{SNSPx} – V_{SNSNx} Input Referred Offset Voltage for IMONx	V_{SNSPx} = V_{SNSNx} = 0V V_{SNSPx} = V_{SNSNx} = 40V 	 ● ●	–120 –200 –150 –200	0 0 0 0	120 200 150 200	µV µV µV µV
IMONx Short-Circuit Current	IMONx = 0V			2		mA
IMONx Overcurrent Threshold				1.8		mA
IMONx Undervoltage Threshold	IMONx Falling, External REFIN/OUT Mode $V_{REFIN/OUT}$ = 5V $V_{REFIN/OUT}$ = 3V $V_{REFIN/OUT}$ = 1.5V		 135 75 30		 mV mV mV
IMONx Undervoltage Hysteresis				15		mV
IMONx Overvoltage Threshold	IMONx Rising, External REFIN/OUT Mode $V_{REFIN/OUT}$ = 5V $V_{REFIN/OUT}$ = 3V $V_{REFIN/OUT}$ = 1.5V		 4.85 2.91 1.455		 V V V
IMONx Overvoltage Hysteresis				15		mV
Output Current Regulation Loop						
V_{SNSPx} – V_{SNSNx} Regulation Voltage for Output Current Control	DAC Code = 7FFFH, V_{SNSPx} = 0V, 7V DAC Code = 0000H, V_{SNSPx} = 0V, 7V DAC Code = 8000H, V_{SNSPx} = 0V, 7V	● ● ●	44.00 –0.25 –44.88	44.44 0 –44.44	44.88 0.25 –44.00	mV mV mV
Output Voltage Monitor and Differential Regulation Loop						
V_{CSN1} – V_{CSN2} Operating Voltage Range		●	–40		40	V
V_{CSN1} – V_{CSN2} to VMON Voltage Gain	V_{CSN1} – V_{CSN2} = 40V	●	49	50	51	mV/V
VMON Short-Circuit Current	VMON = 0V			2		mA
V_{CSN1} – V_{CSN2} Regulation Voltage	DAC Code = 0000H			0		V

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
External NMOS Gate Drive						
TG1, TG2 Rise Time	C_{LOAD} = 3300pF (Note 5)			20		ns
TG1, TG2 Fall Time	C_{LOAD} = 3300pF (Note 5)			20		ns
BG1, BG2 Rise Time	C_{LOAD} = 3300pF (Note 5)			20		ns
BG1, BG2 Fall Time	C_{LOAD} = 3300pF (Note 5)			20		ns
TG1 Off to BG1 On Delay	C_{LOAD}(TG1) = C_{LOAD}(BG1) = 3300pF (Note 5)			50		ns
BG1 Off to TG1 On Delay	C_{LOAD}(BG1) = C_{LOAD}(TG1) = 3300pF (Note 5)			30		ns
TG2 Off to BG2 On Delay	C_{LOAD}(TG2) = C_{LOAD}(BG2) = 3300pF (Note 5)			50		ns
BG2 Off to TG2 On Delay	C_{LOAD}(BG2) = C_{LOAD}(TG2) = 3300pF (Note 5)			30		ns
Minimum On-Time for TG1, BG2	C_{LOAD}(TG1) = C_{LOAD}(BG2) = 3300pF			150		ns
Minimum Off-Time for TG1, BG2	C_{LOAD}(TG1) = C_{LOAD}(BG2) = 3300pF			150		ns
MT1, MT2, MB1 and MB2 V_{DS} Fault Threshold	Positive Negative			1.5 –1.0		V V
Oscillator						
Switch Frequency Range	SYNCing or Free Running		100		1000	kHz
Switching Frequency	RT = 90.9k RT = 22.6k RT = 13.0k	 ●	90 280 475	100 300 500	110 320 525	kHz kHz kHz
SYNC/SPRD High Level Input Voltage		●	1.30			V
SYNC/SPRD Low Level Input Voltage		●			0.55	V
Spread Spectrum Above Oscillator Frequency	$V_{SYNC/SPRD}$ = 3V			23		%
Switching Phase Between Two Half Bridges	In Dual Half-Bridge Mode, RT = 13.0k		160	180	200	Deg
Digital to Analog Conversion						
Resolution	(Note 6)	●	16			Bits
Monotonicity		●	16			Bits
Differential Nonlinearity (DNL)		●		±0.5	±1	LSB
Integral Nonlinearity (INL)		●		±20	±40	LSB
DAC Min Output Voltage				1/18 • $V_{REFIN/OUT}$		V
DAC Max Output Voltage	(Note 7)			17/18 • $V_{REFIN/OUT}$ – 1 • LSB		V
Logic I/O						
$\overline{ALERT}$ Output Low Voltage	$I_{\overline{ALERT}}$ = 1mA	●			0.3	V
$\overline{ALERT}$ Output High to Low Delay Time				1		µs
$\overline{ALERT}$ Leakage Current	$V_{\overline{ALERT}}$ = 5.25V	●			2	µA
$\overline{CS}$, SCK, SDI High Level Input Voltage		●	0.8 • $SPIV_{DD}$			V
$\overline{CS}$, SCK, SDI Low Level Input Voltage		●			0.2 • $SPIV_{DD}$	V
$\overline{CS}$, SCK, SDI Input Leakage	$V_{\overline{CS}}$ = V_{SCK} = V_{SDI} = $SPIV_{DD}$ = 5.25V	●			±2	µA
$\overline{CS}$, SCK, SDI Input Capacitance	(Note 6)			10		pF

ELECTRICAL CHARACTERISTICS

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PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
SDO High Level Output Voltage		I_{SDO} = –500µA	●	$SPIV_{DD}$ – 0.2			V
SDO Low Level Output Voltage		I_{SDO} = 500µA	●			0.2	V
SDO Hi-Z Output Leakage Current		V_{SDO} = 0V to $SPIV_{DD}$	●			±1	µA
SPI Timing (See SPI Timing Diagram in Figure 1) (Note 5)							
t_1	SDI Valid to SCK Setup		●	5			ns
t_2	SDI Valid to SCK Hold		●	5			ns
t_3	SCK Pulse Width High		●	15			ns
t_4	SCK Pulse Width Low		●	15			ns
t_5	$\overline{CS}$ Pulse Width High		●	25			ns
t_6	Last Bit SCK High to $\overline{CS}$ High		●	10			ns
t_7	$\overline{CS}$ Low to SCK High		●	10			ns
t_8	SDO Data Valid Delay from SCK Low	C_L = 20pF $SPIV_{DD}$ = 3.3V to 5.25V $SPIV_{DD}$ = 1.80V to 3.3V	 ● ●			 20 45	 ns ns
t_9	SDO Data Valid Delay from $\overline{CS}$ Low	C_L = 20pF $SPIV_{DD}$ = 3.3V to 5.25V $SPIV_{DD}$ = 1.80V to 3.3V	 ● ●			 20 45	 ns ns
t_{10}	$\overline{CS}$ High to SCK High		●	10			ns
	SCK Frequency (Note 8)	50% Duty Cycle $SPIV_{DD}$ = 3.3V to 5.25V $SPIV_{DD}$ = 1.80V to 3.3V	 ● ●			 25 10	 MHz MHz
	EN/UVLO High to Part Responsive to $\overline{CS}$ Low (Power-Up Delay)	C_{INTVCC} = 2.2µF			500		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not apply a voltage or current source to these pins. They must be connected to resistive/capacitive loads only, otherwise permanent damage may occur.

Note 3: The LT8204 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

LT8204R is specified over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperature greater than 125°C. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors.

Note 4: $I_{B1(2)}$ is defined as the average of the input bias currents to the SNSP1(2) and SNSN1(2) pins. A positive current indicates current flowing into the pin. $I_{OS1(2)}$ is defined as the difference of the input bias currents. $I_{OS1(2)} = I_{SNSP1(2)} - I_{SNSN1(2)}$.

Note 5: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 6: Guaranteed by design and not production tested.

Note 7: LSB voltage value is defined as 8/9 • $V_{REFIN/OUT}/2^{16}$.

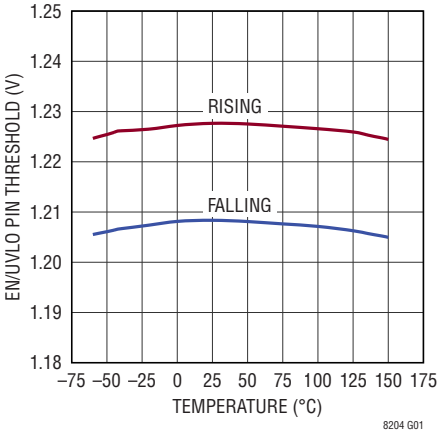
Note 8: When using SDO, the maximum SCK frequency f_{MAX} is limited by SDO propagation delay as following:

$$f_{MAX} = \frac{1}{2 \bullet (t_8 + t_S)}$$

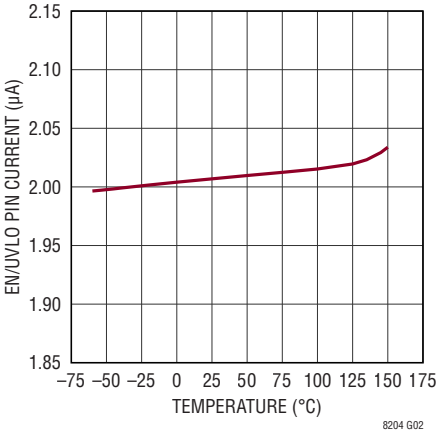
where t_8 is SDO data valid delay time from $\overline{CS}$ low, and t_S is the setup time of the receiving device.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

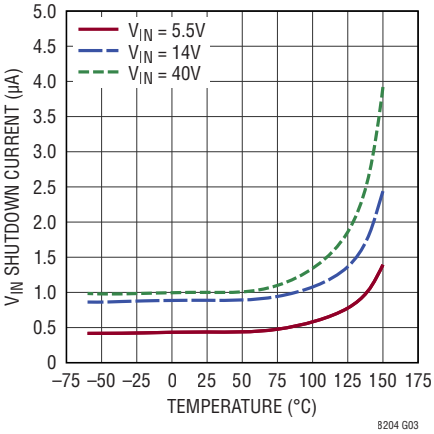
EN/UVLO Pin Threshold



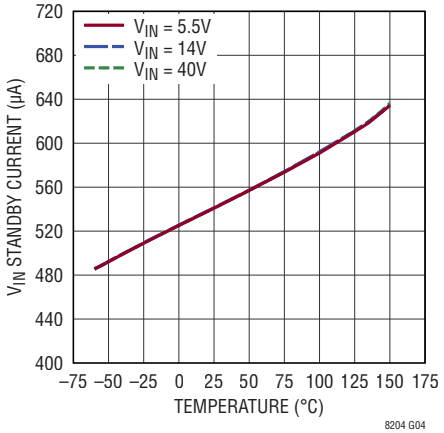
EN/UVLO Pin Current



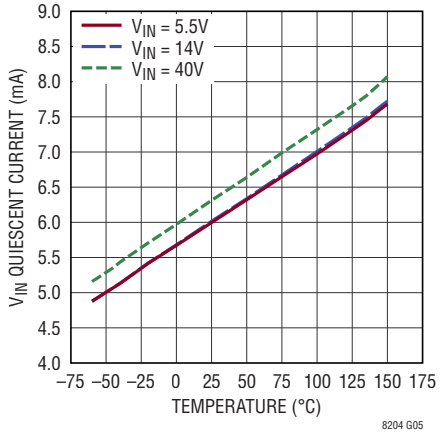
V_{IN} Shutdown Current



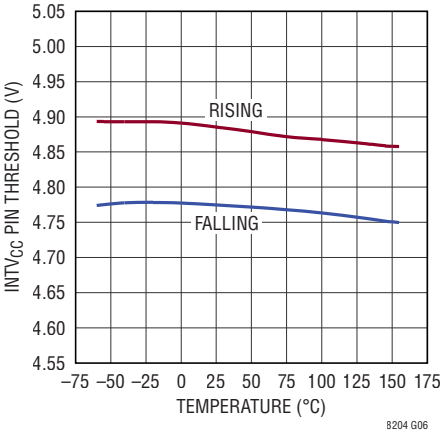
V_{IN} Standby Current



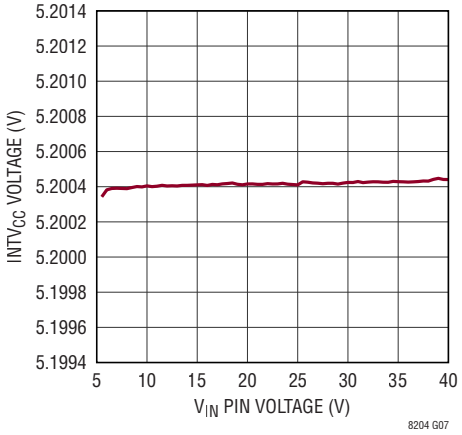
V_{IN} Quiescent Current



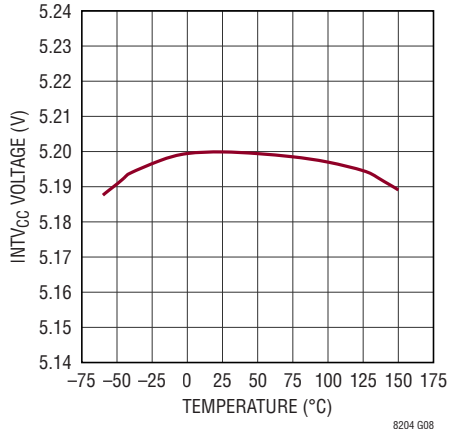
$INTV_{CC}$ Pin Threshold



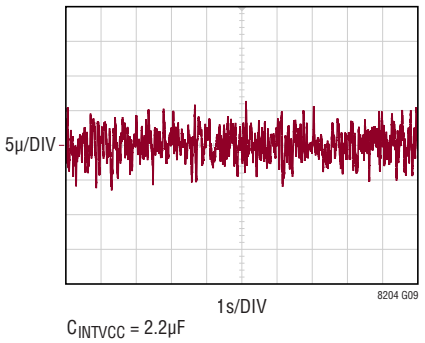
$INTV_{CC}$ Voltage vs V_{IN}



$INTV_{CC}$ Voltage vs Temperature



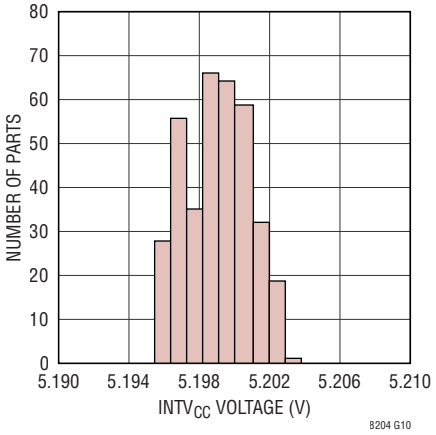
$INTV_{CC}$ Low Frequency 0.1Hz to 10Hz Noise



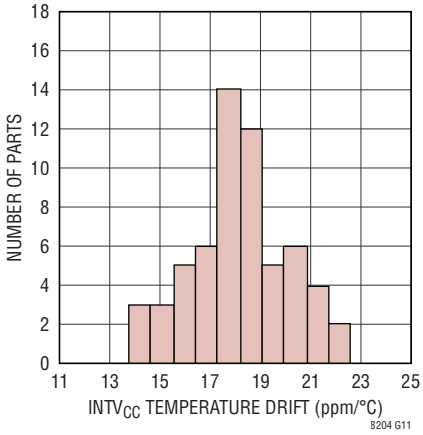
C_{INTVCC} = 2.2µF

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

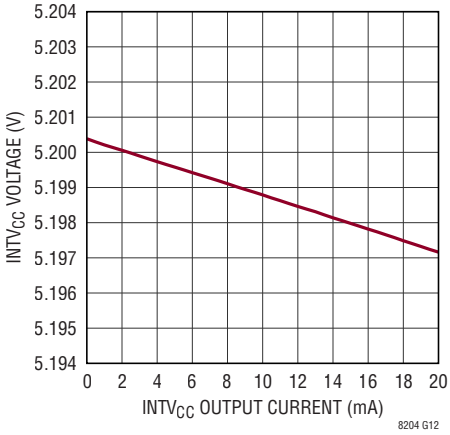
$INTV_{CC}$ Voltage Distribution



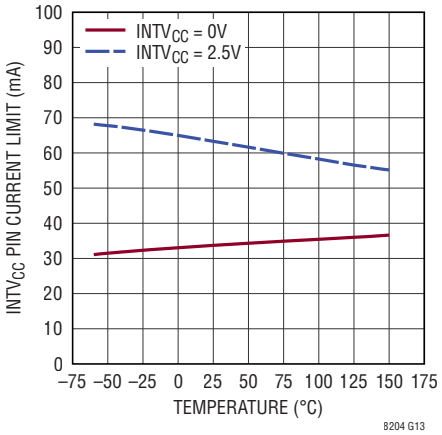
$INTV_{CC}$ Temperature Drift Distribution



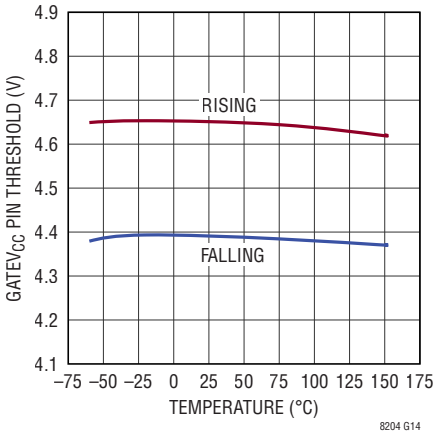
$INTV_{CC}$ Load Regulation



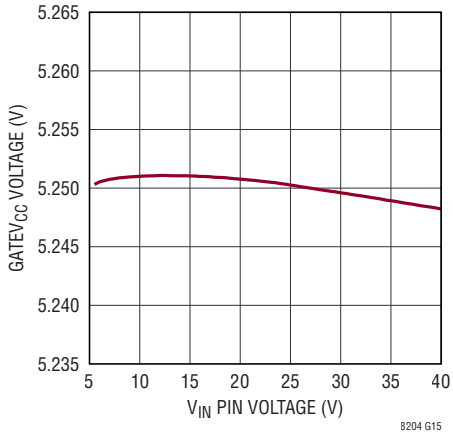
$INTV_{CC}$ Pin Current Limit



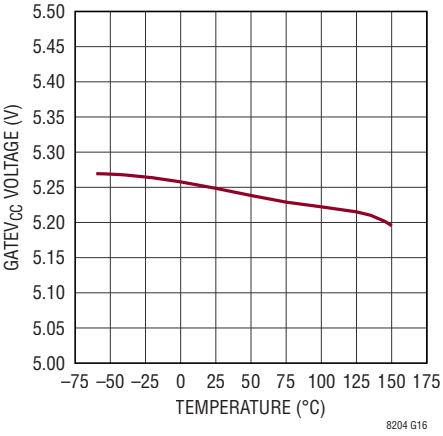
$GATEV_{CC}$ Pin Threshold



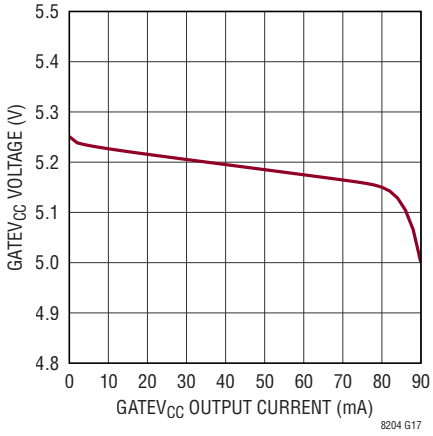
$GATEV_{CC}$ Voltage vs V_{IN}



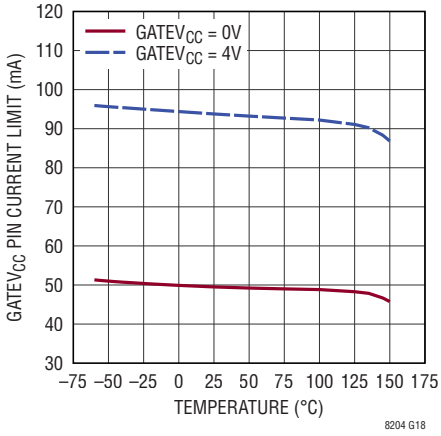
$GATEV_{CC}$ Voltage vs Temperature



$GATEV_{CC}$ Load Regulation

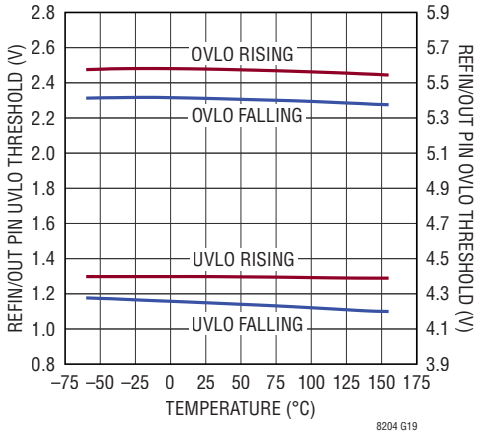


$GATEV_{CC}$ Pin Current Limit

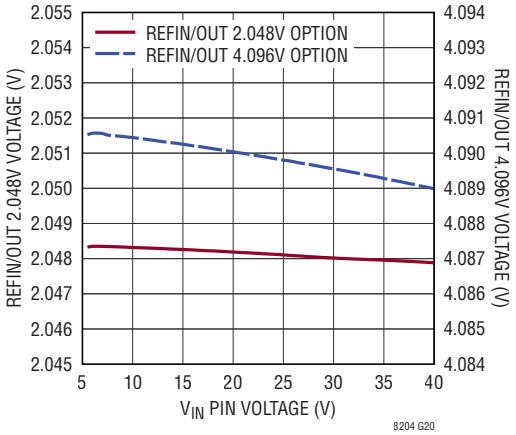


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

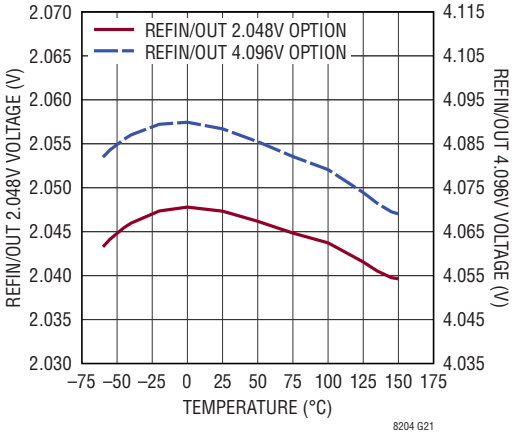
REFIN/OUT Pin Threshold External REFIN/OUT Option



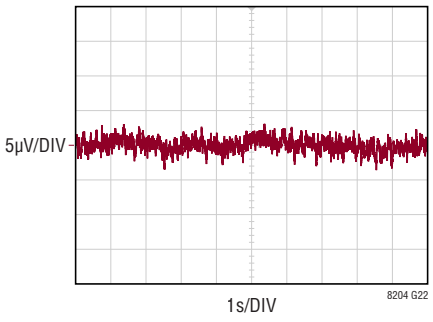
Internal REFIN/OUT Voltage vs V_{IN}



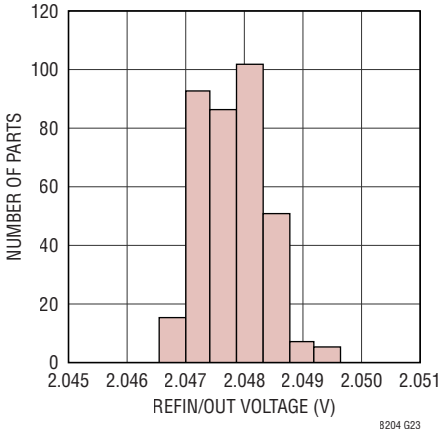
Internal REFIN/OUT Voltage vs Temperature



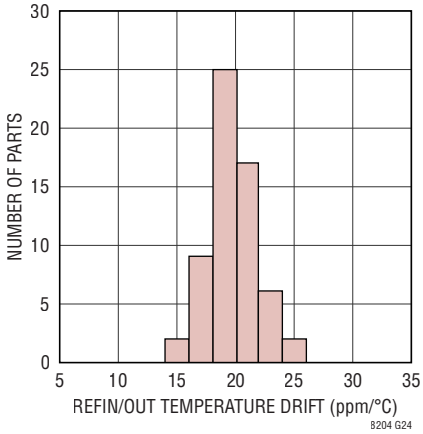
Internal 2.048V REFIN/OUT Low Frequency 0.1Hz to 10Hz Noise



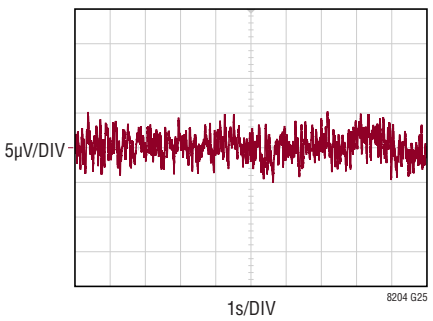
Internal 2.048V REFIN/OUT Voltage Distribution



Internal 2.048V REFIN/OUT Temperature Drift Distribution

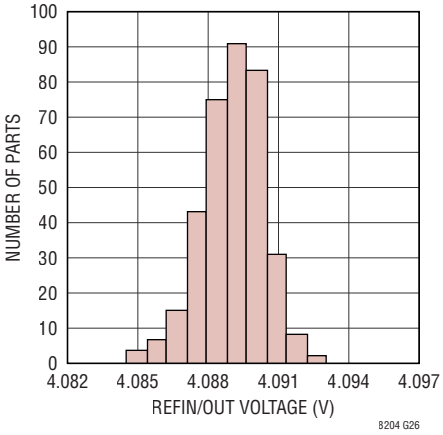


Internal 4.096V REFIN/OUT Low Frequency 0.1Hz to 10Hz Noise

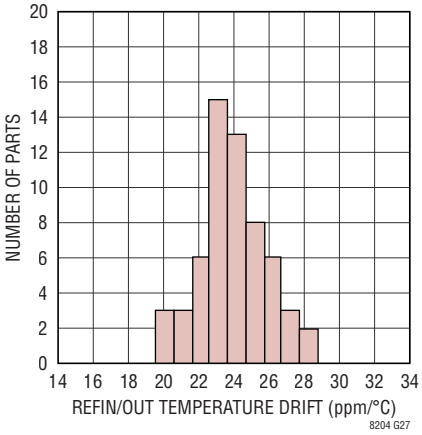


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

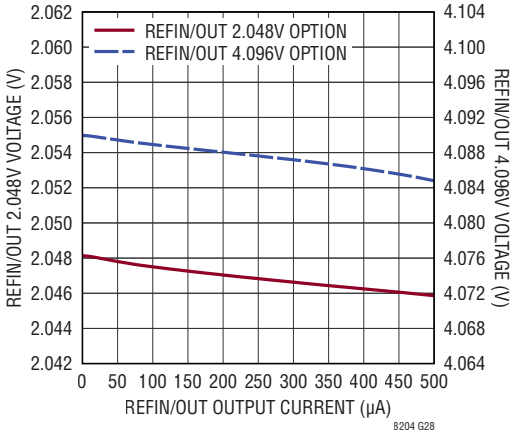
Internal 4.096V REFIN/OUT Voltage Distribution



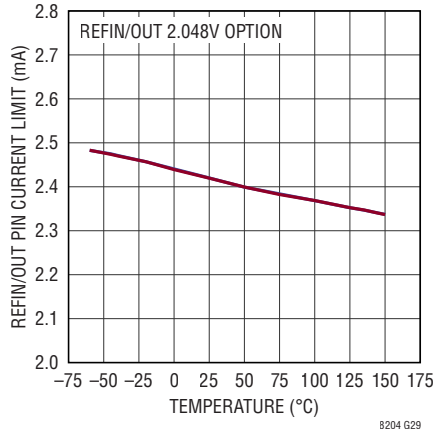
Internal 4.096V REFIN/OUT Temperature Drift Distribution



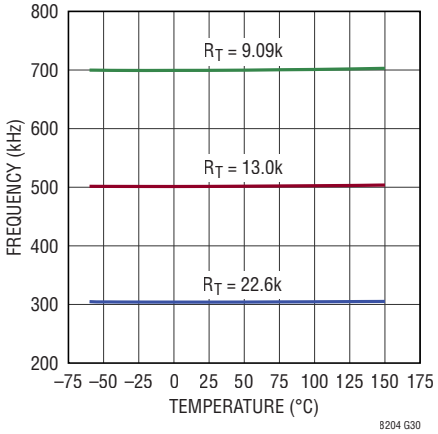
Internal REFIN/OUT Load Regulation



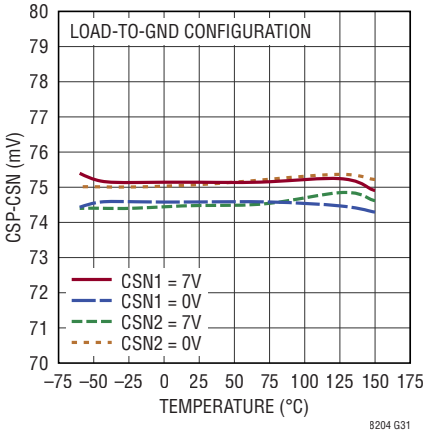
REFIN/OUT Pin Current Limit



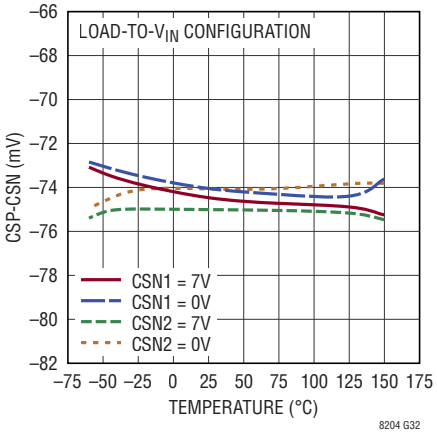
Oscillator Frequency



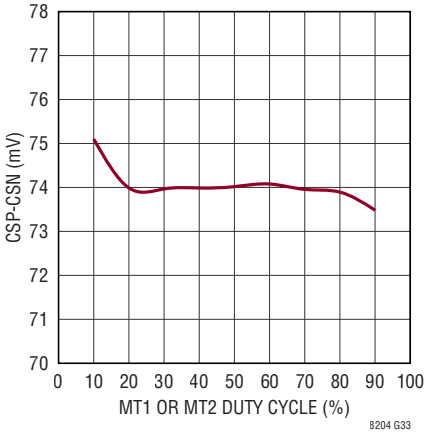
Maximum Positive Inductor Current Sense Voltage vs Temperature



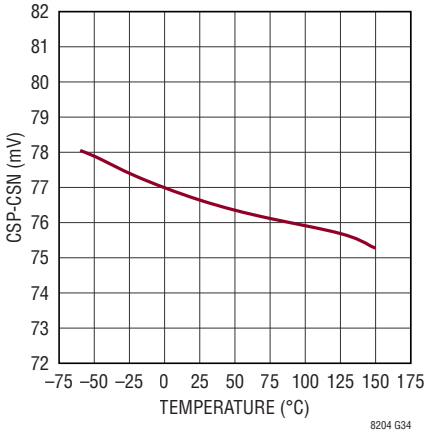
Maximum Negative Inductor Current Sense Voltage vs Temperature



Maximum Inductor Current Sense Voltage vs Duty Cycle

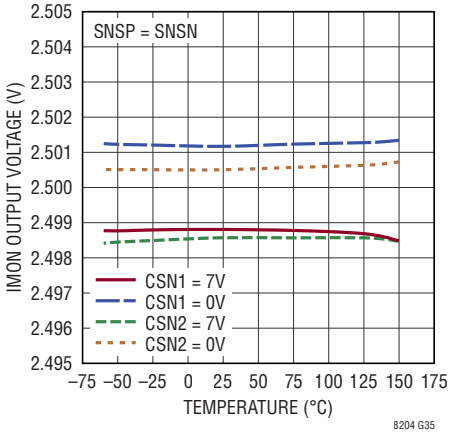


Maximum Inductor Current Sense Voltage at Minimum Duty Cycle

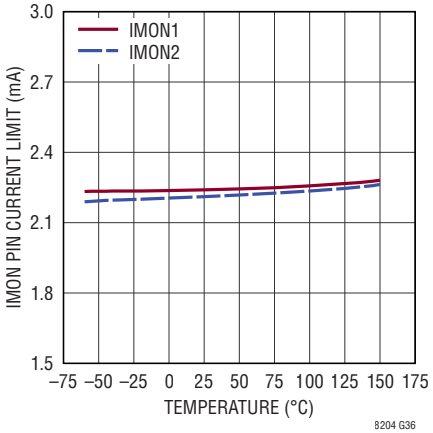


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

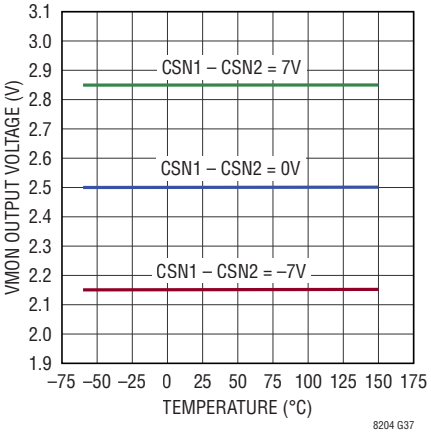
IMON Output Voltage



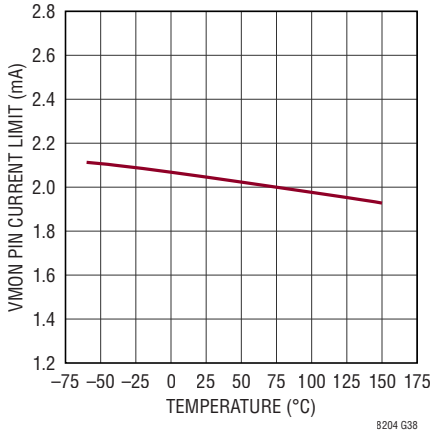
IMON Pin Current Limit



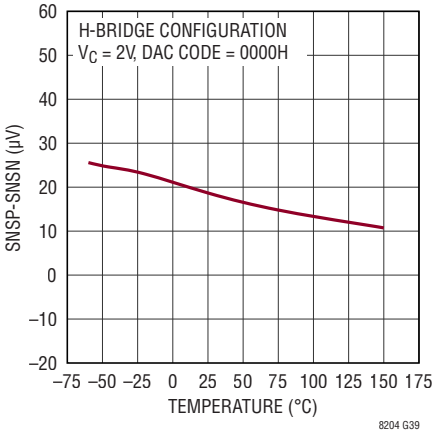
VMON Output Voltage



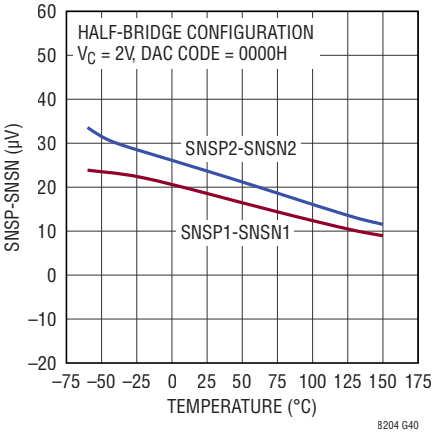
VMON Pin Current Limit



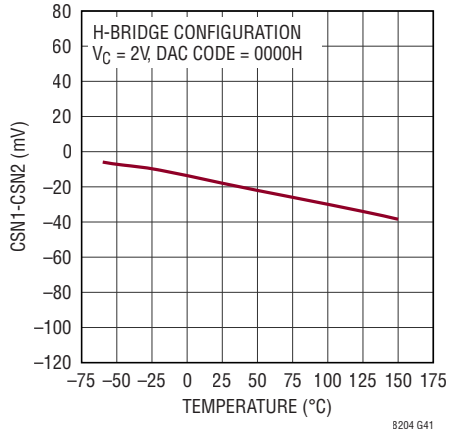
SNSP-SNSN Voltage Regulation



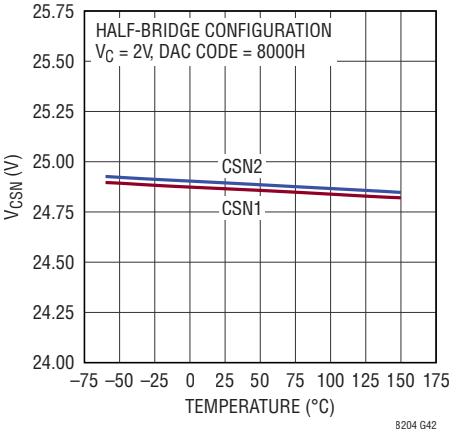
SNSP-SNSN Voltage Regulation



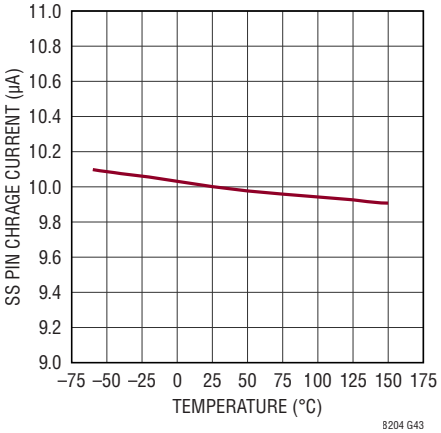
CSN1-CSN2 Voltage Regulation



CSN Voltage Regulation

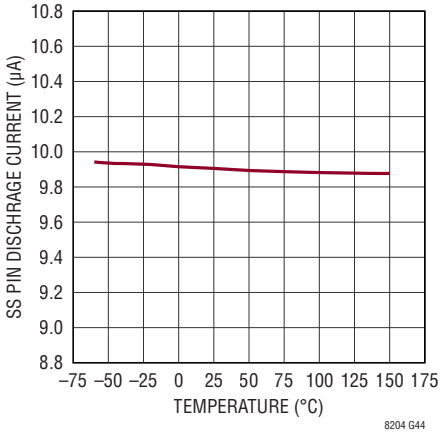


SS Pin Charge Current

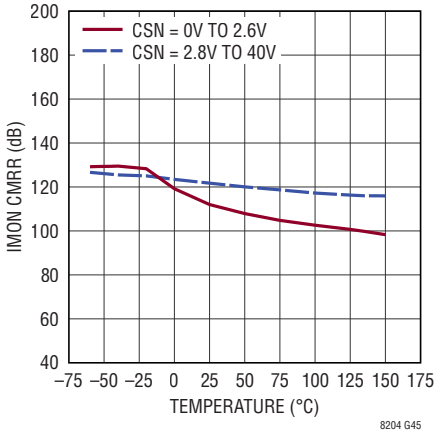


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

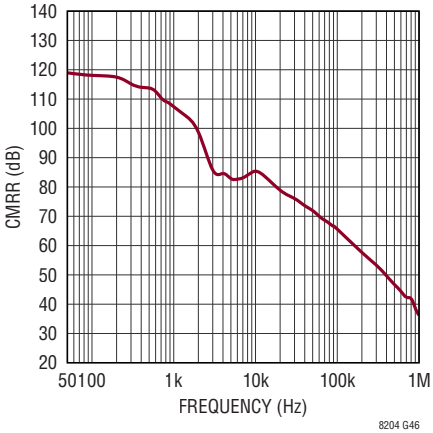
SS Pin Discharge Current



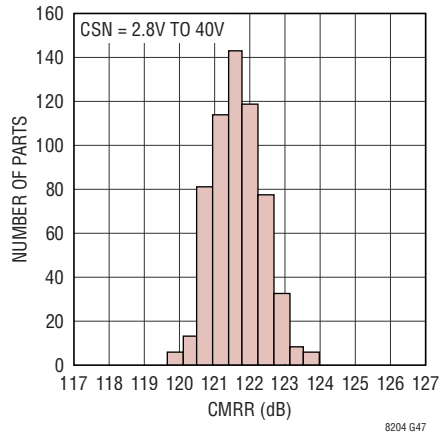
IMON CMRR vs Temperature



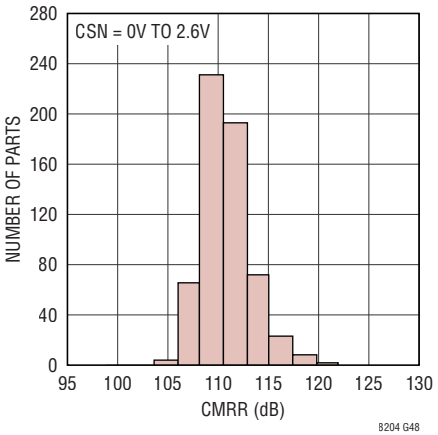
IMON CMRR vs Frequency



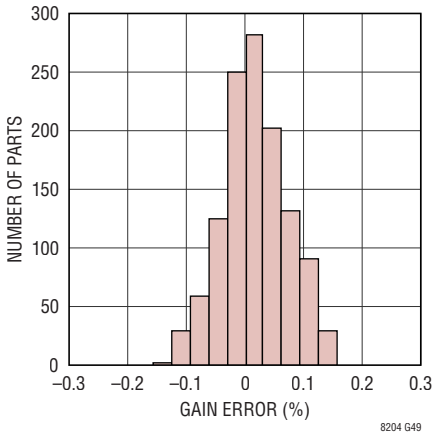
Typical Distribution of IMON CMRR



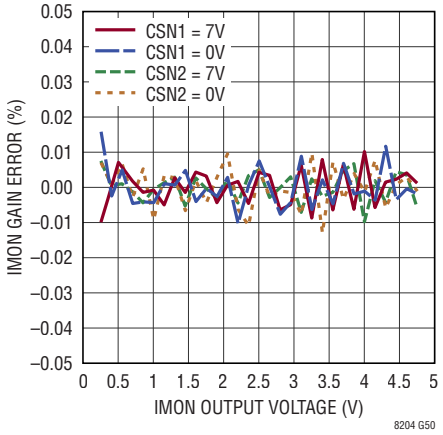
Typical Distribution of IMON CMRR



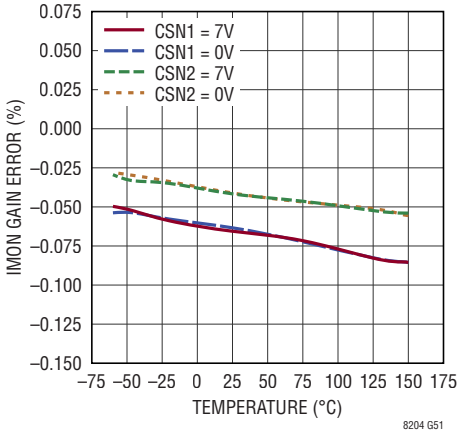
Typical Distribution of IMON Gain Error



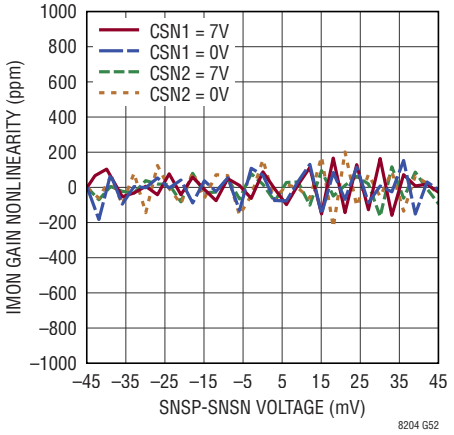
IMON Gain Error vs IMON Output Voltage



IMON Gain Error vs Temperature

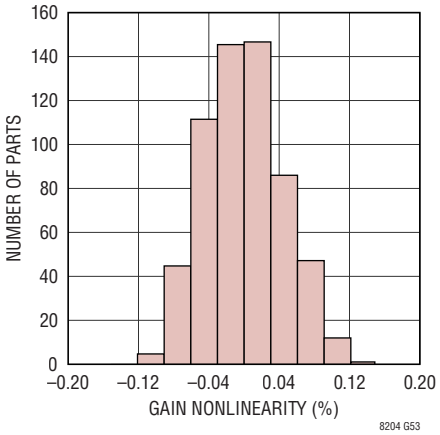


IMON Gain Nonlinearity

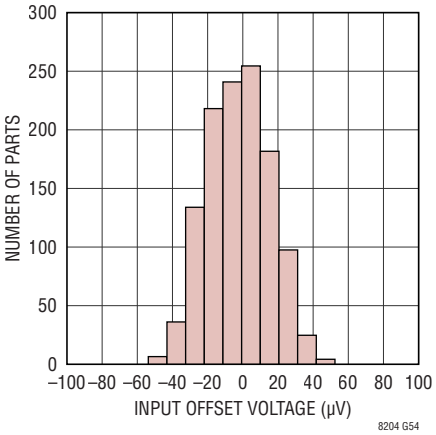


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

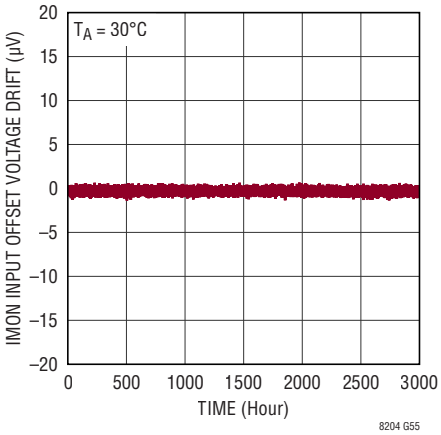
Typical Distribution of IMON Gain Nonlinearity



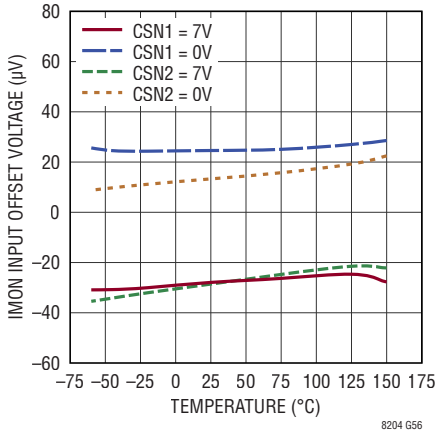
Typical Distribution of IMON Input Offset Voltage



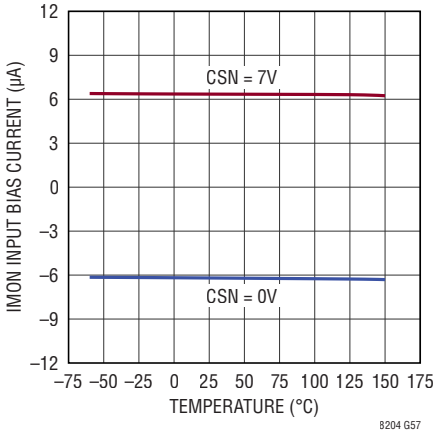
IMON Input Offset Voltage Long Term Drift



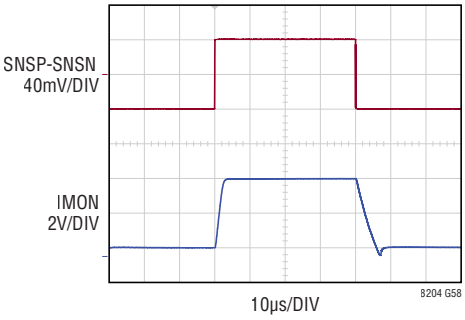
IMON Input Offset Voltage vs Temperature



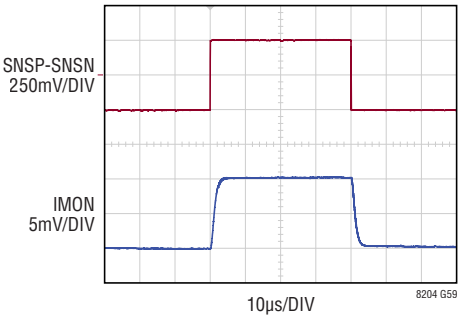
IMON Input Bias Current



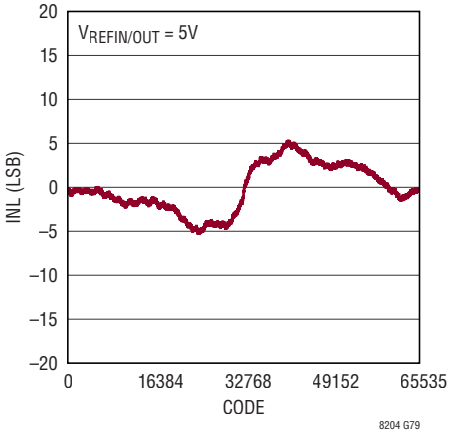
IMON Large-Signal Step Response



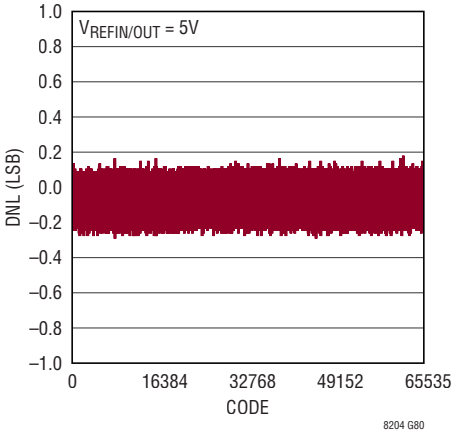
IMON Small-Signal Step Response



Integral Nonlinearity (INL)

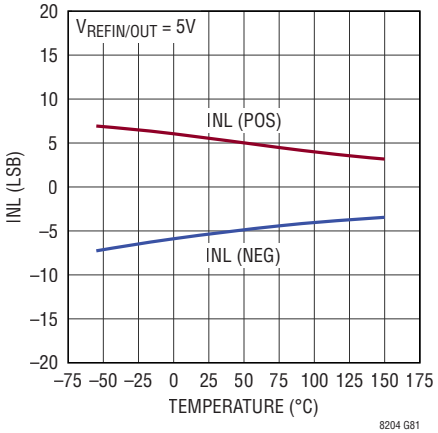


Differential Nonlinearity (DNL)

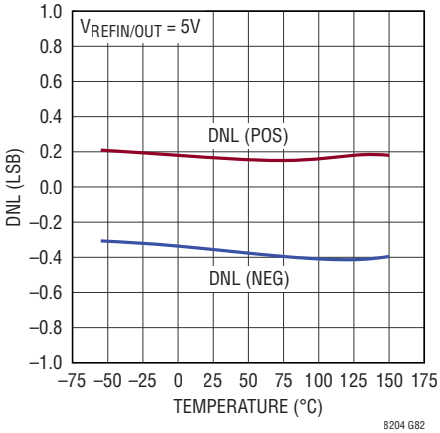


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

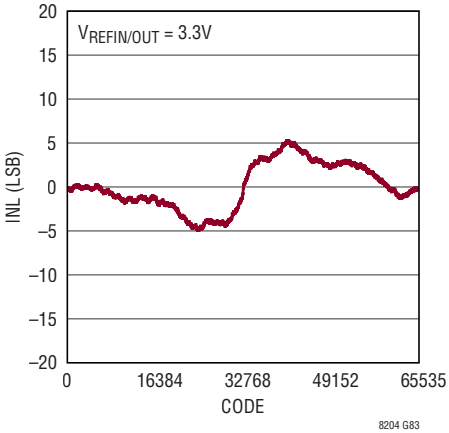
INL vs Temperature



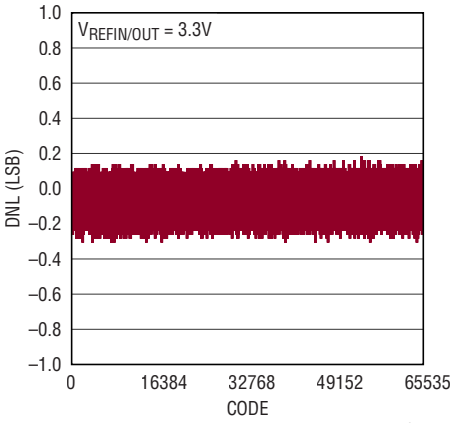
DNL vs Temperature



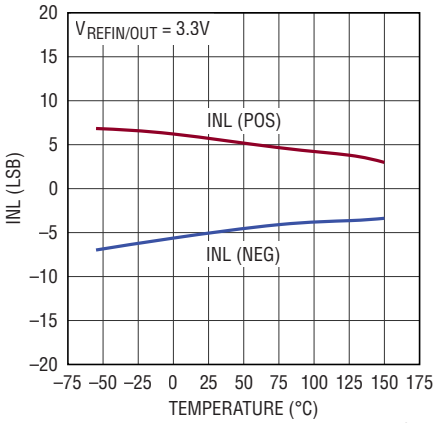
Integral Nonlinearity (INL)



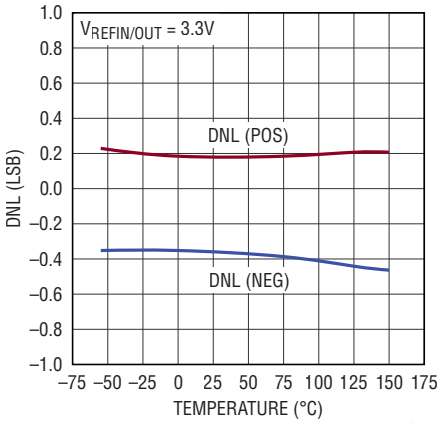
Differential Nonlinearity (DNL)



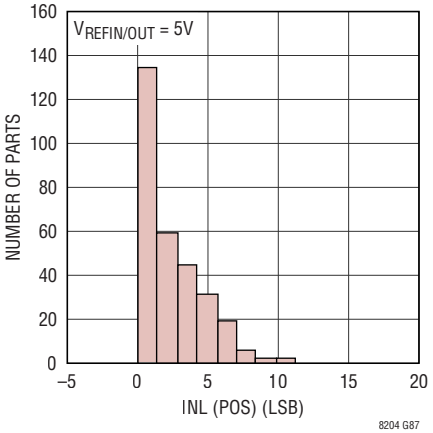
INL vs Temperature



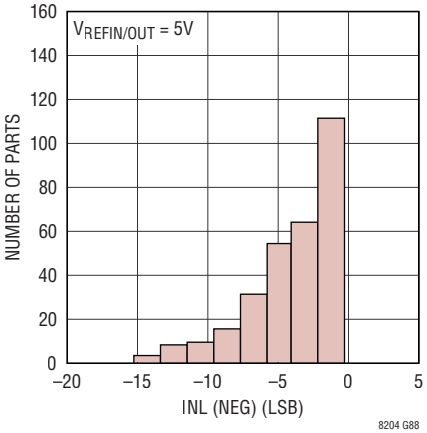
DNL vs Temperature



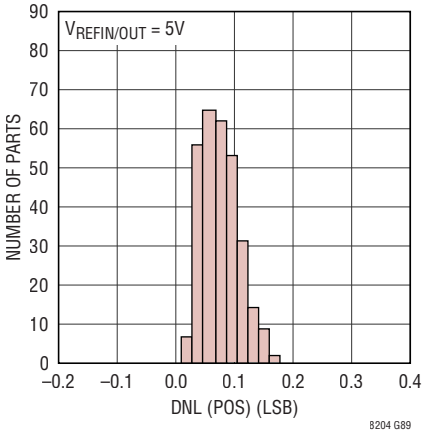
Typical Distribution of INL (POS)



Typical Distribution of INL (NEG)

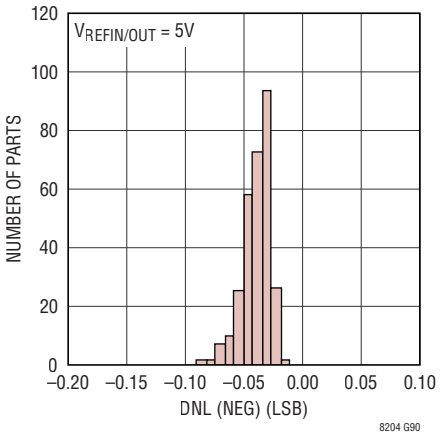


Typical Distribution of DNL (POS)

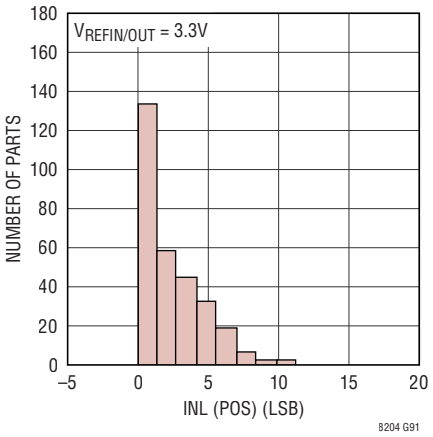


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

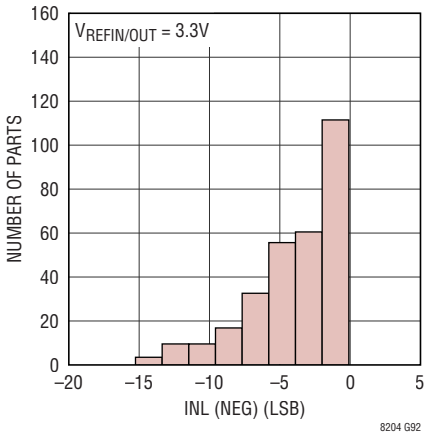
Typical Distribution of DNL (NEG)



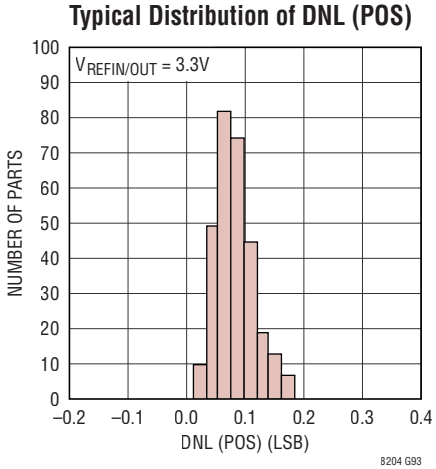
Typical Distribution of INL (POS)



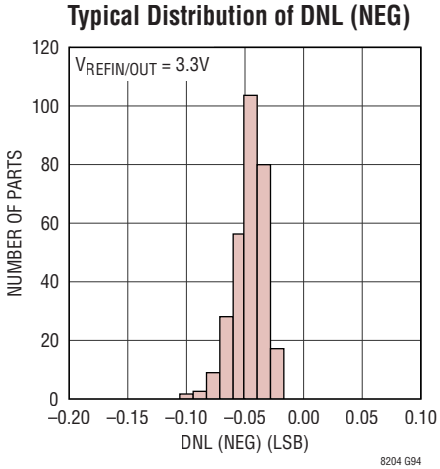
Typical Distribution of INL (NEG)



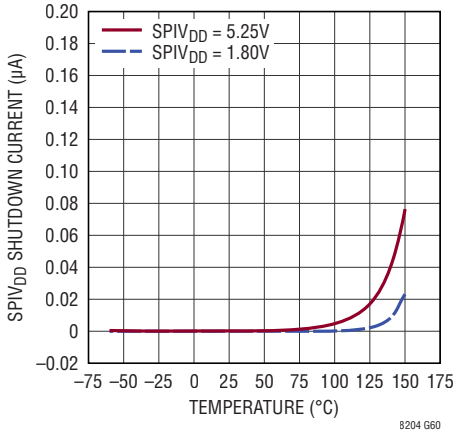
Typical Distribution of DNL (POS)



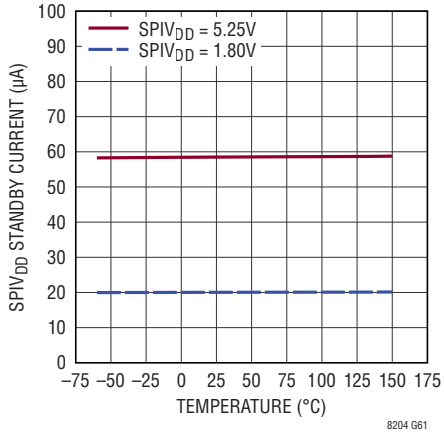
Typical Distribution of DNL (NEG)



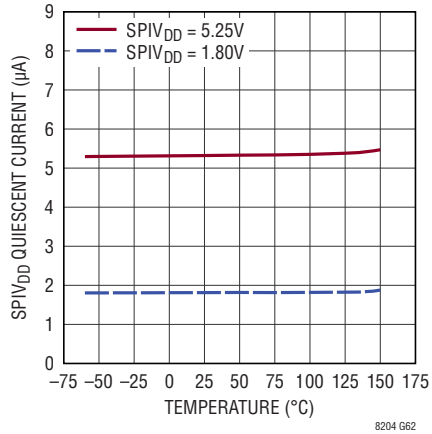
$SPIV_{DD}$ Shutdown Current EN/UVLO = 0.3V



$SPIV_{DD}$ Standby Current EN/UVLO = 1.1V

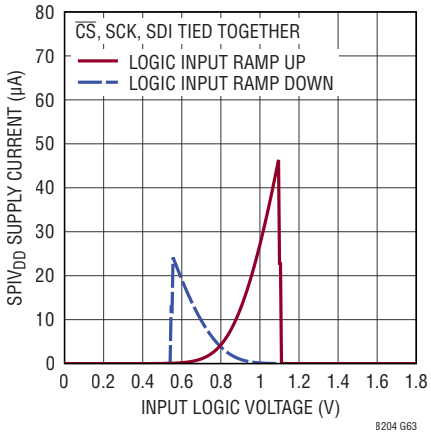


$SPIV_{DD}$ Quiescent Current EN/UVLO = 3V

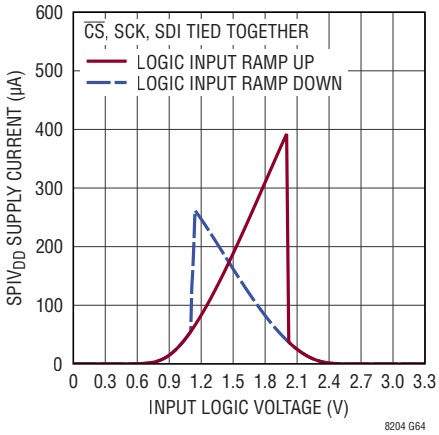


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

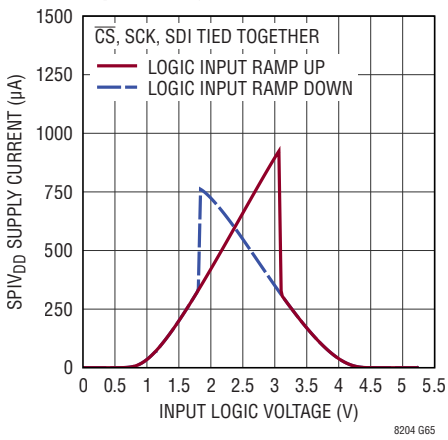
$SPIV_{DD}$ Supply Current vs Logic Input Voltage, $SPIV_{DD}$ = 1.8V



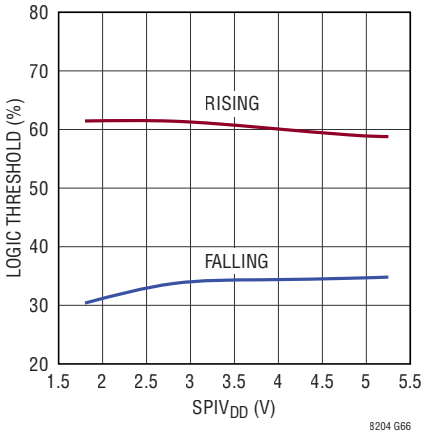
$SPIV_{DD}$ Supply Current vs Logic Input Voltage, $SPIV_{DD}$ = 3.3V



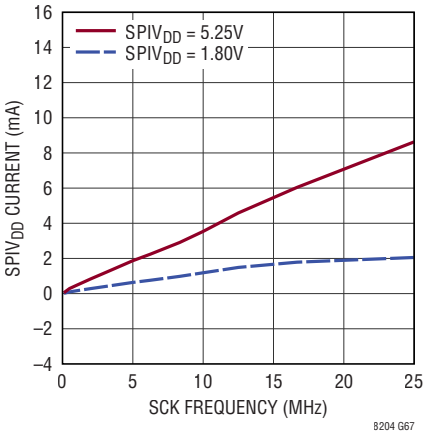
$SPIV_{DD}$ Supply Current vs Logic Input Voltage, $SPIV_{DD}$ = 5.25V



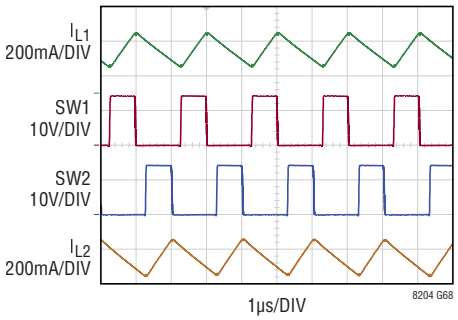
$\overline{CS}$, SCK, SDI Logic Threshold vs $SPIV_{DD}$



$SPIV_{DD}$ Supply Current of Update Frequency

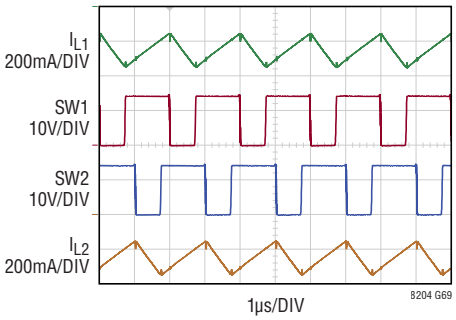


Switching Waveforms (Half-Bridge Configuration)



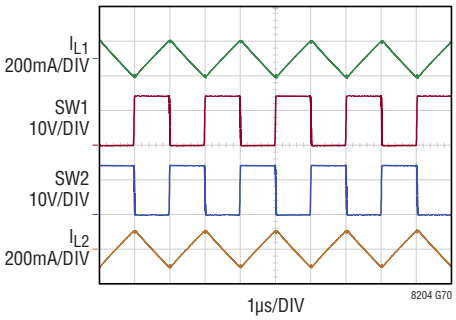
LOAD-TO-GND
I_{OUT1} = 250mA, I_{OUT2} = 250mA

Switching Waveforms (Half-Bridge Configuration)



LOAD-TO-V_{IN}
I_{OUT1} = 250mA, I_{OUT2} = 250mA

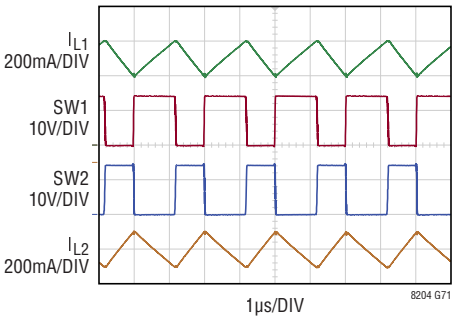
Switching Waveforms (H-Bridge Configuration)



I_{OUT} = 0A

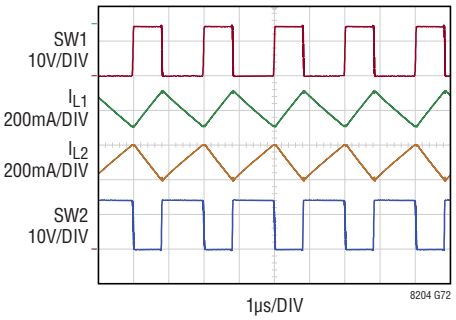
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Switching Waveforms (H-Bridge Configuration)



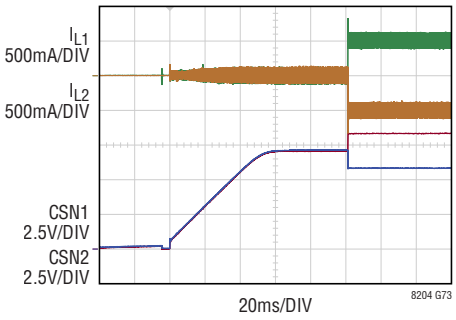
I_{OUT} = 500mA

Switching Waveforms (H-Bridge Configuration)



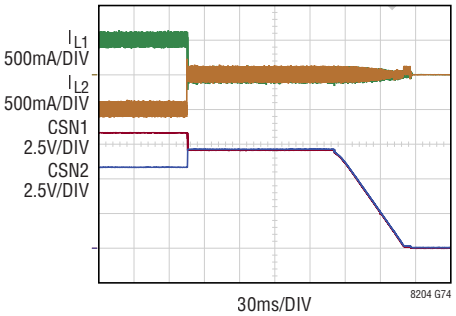
I_{OUT} = –500mA

Soft Start-Up Waveforms (H-Bridge Configuration)



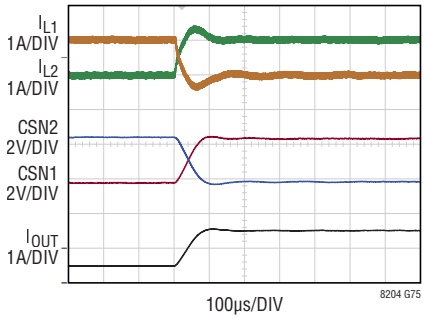
SOFT-START TO I_{OUT} = 500mA
CURRENT MODE CONTROL
5Ω RESISTIVE LOAD

Soft Startdown Waveforms (H-Bridge Configuration)



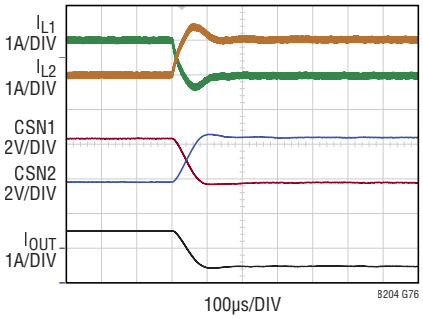
SOFT SHUTDOWN FROM I_{OUT} = 500mA
CURRENT MODE CONTROL
5Ω RESISTIVE LOAD

I_{OUT} Step Response to DAC (H-Bridge Configuration)



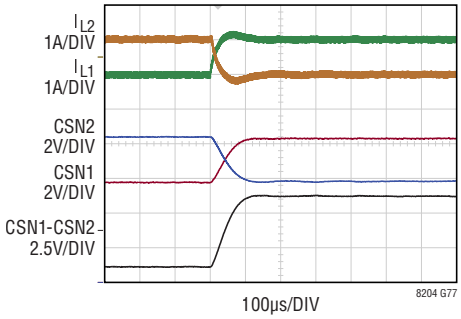
I_{OUT} TRANSITION FROM –500mA TO 500mA
CURRENT MODE CONTROL
5Ω RESISTIVE LOAD

I_{OUT} Step Response to DAC (H-Bridge Configuration)



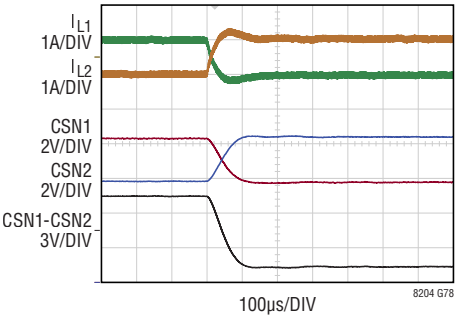
I_{OUT} TRANSITION FROM 500mA TO –500mA
CURRENT MODE CONTROL
5Ω RESISTIVE LOAD

V_{OUT} Step Response to DAC (H-Bridge Configuration)



V_{OUT} TRANSITION FROM –2.5V TO 2.5V
CURRENT MODE CONTROL
5Ω RESISTIVE LOAD

V_{OUT} Step Response to DAC (H-Bridge Configuration)



V_{OUT} TRANSITION FROM 2.5V TO –2.5V
CURRENT MODE CONTROL
5Ω RESISTIVE LOAD

PIN FUNCTIONS

BG1, BG2 (Pins 1, 38): Bottom N-Channel MOSFET Gate Driver Output Pin. BG1 and BG2 are the gate drive signals for the external N-channel MOSFET devices connected between the SW1 and SW2 pins and power ground. The BG1 and BG2 voltage swings between $GATEV_{CC}$ and ground.

$GATEV_{CC}$ (Pin 2): Internal 5.3V Regulator Bypass Pin. The internal bottom gate drivers are powered from this voltage. Decouple this pin to power ground with at least 4.7µF low ESR ceramic capacitor placed close to the IC.

BST1, BST2 (Pins 3, 37): Boosted Floating Gate Driver Supply Pin. The positive (+) terminals of the bootstrap capacitors connect to these pins. The BST1 and BST2 pin voltages swing from a diode voltage below $GATEV_{CC}$ to (V_{IN} + $GATEV_{CC}$).

SW1, SW2 (Pins 4, 36): Switch Pins. The negative (–) terminals of the bootstrap capacitors connect to these pins.

TG1, TG2 (Pins 5, 35): Top N-Channel MOSFET Gate Driver Output Pin. TG1 and TG2 are the gate drive signals for the external N-channel MOSFET connected between V_{IN} and the SW1 and SW2 pins. The voltage swing on the TG1 and TG2 pins equals $GATEV_{CC}$ superimposed onto the SW1 and SW2 pin voltages.

V_{IN} (Pin 6): Input Supply Pin. Must be locally bypassed with a capacitor to ground.

EN/UVLO (Pin 7): Enable and Undervoltage Lockout Pin. Pull the pin below 0.3V to shut down the LT8204 for lowest V_{IN} current. This pin has an accurate 1.2V (typical) falling threshold and programs V_{IN} undervoltage lockout (UVLO) threshold with an external resistor divider from V_{IN} to ground. A 2µA pin current hysteresis programs V_{IN} UVLO hysteresis. If neither function is used, tie this pin directly to V_{IN}.

$INTV_{CC}$ (Pin 8): Internal 5.2V Regulator Bypass Pin. The internal control circuits are powered from this voltage. Decouple this pin to signal ground with at least 2.2µF low ESR ceramic capacitor placed close to the IC. The 5.2V output voltage on this pin features high accuracy over a wide range of V_{IN} voltage, load current and temperature, and thus can be used as $V_{REFIN/OUT}$ (tied to the REFIN/OUT pin), if no external precise voltage reference is available.

REFIN/OUT (Pin 9): Reference Input/Output Pin. This pin provides the voltage reference for the on-chip DACs and the precision current monitors. It acts as the internal reference output in internal reference mode and acts as the reference input pin in external reference mode. In internal reference mode, two voltage options (2.048V or 4.096V) can be selected via the SPI interface. Decouple this pin to signal ground with a low ESR ceramic capacitor placed close to the IC, for best noise performance.

SS (Pin 10): Soft Start-Up/Soft Shutdown Pin. Connect a capacitor between the SS pin and ground for soft start-up and soft shutdown controls. See more details in the Applications Information section.

V_{C1}, V_{C2} (Pins 11, 12): Error Amplifier Output Pins. Connect the external closed-loop frequency compensation network to these pins.

IMON1, IMON2 (Pins 14, 13): Load Current Monitor 1 and 2 Output Pin. The voltage on IMON1(2) pin is 50 times the voltage ($V_{SNSP1(2)} – V_{SNSN1(2))}$, plus an offset of $V_{REFIN/OUT}$/2. A pin voltage above $V_{REFIN/OUT}$/2 indicates a current flow from SNSP1 pin to SNSN1 pin, while a voltage below $V_{REFIN/OUT}$/2 for the opposite current flow direction.

MODE1, MODE2 (Pins 15, 24): Mode Pins. The voltage applied to these pins sets the system architecture of the LT8204. See more details in Table 1.

SNSN1, SNSN2 (Pins 16, 23): Load Current Monitor Negative (–) Input Pins.

SNSP1, SNSP2 (Pins 17, 22): Load Current Monitor Positive (+) Input Pins. These two pins and the SNSN1, SNSN2 pins measure the voltage across the sense resistors, to monitor the load current.

CSN1, CSN2 (Pins 18, 21): Inductor Current Sense Negative (–) Input Pins. See more details in the Applications Information section.

CSP1, CSP2 (Pins 19, 20): Inductor Current Sense Positive (+) Input Pins. The V_C pin voltage and built-in offsets between CSP1(2) and CSN1(2), in conjunction with the current sense resistor value, set the current trip threshold. Short these pins to V_{CSN1} and V_{CSN2} respectively if not used. See more details in the Applications Information section.

PIN FUNCTIONS

VMON (Pin 25): Differential Load Voltage Monitor Output Pin. The pin voltage is 1/20 of the differential voltage ($V_{CSN1} – V_{CSN2}$) plus an offset of $V_{REFIN/OUT}/2$. A pin voltage above $V_{REFIN/OUT}/2$ indicates a higher voltage on the CSN1 pin than the CSN2 pin, while a voltage below $V_{REFIN/OUT}/2$ for the opposite voltage direction.

$\overline{\text{ALERT}}$ (Pin 26): Alert Pin. Connect a pull-up resistor from this pin to $SPIV_{DD}$ or an external voltage source. Limit the current into the pin to no more than 1mA. This pin is active low when the LT8204 has an alert. Connect this pin to a microprocessor's interrupt pin for system diagnosis.

RUN (Pin 27): System Run Pin. This pin is used to disable/enable the switching action of the LT8204. Pull this pin low to disable the switching action. If a soft shutdown command is programmed through the SPI interface (by default, the LT8204 commands a soft shutdown), the LT8204 performs the soft shutdown to discharge the output voltages of the bridge/s to near zero voltage, before stopping switching; If a hold command is programmed through the SPI interface, the LT8204 first performs the soft shutdown and then turns on both bottom MOSFETs. (See more details in the Operation section). If the function is not used, tie this pin directly to $INTV_{CC}$.

RT (Pin 28): Timing Resistor Input Pin. The RT pin adjusts the LT8204 switching frequency. Place a resistor from this pin to the ground to set the free-running frequency. If floated or disconnected from the resistor at any time, LT8204 will default to a 30kHz switching frequency and notify the host of this abnormal frequency in a fault status register. Similarly, if the RT pin is shorted to ground, it will default to a 1.4MHz switching frequency and notify the host.

SYNC/SPRD (Pin 29): External Synchronization Input or Spread Spectrum Control Pin. To synchronize the switching frequency to an external clock, simply drive this pin with a clock. Connect this pin to $INTV_{CC}$ to use the internal oscillator frequency with a +23% triangle spread spectrum. If spread spectrum is not needed, tie this pin to the ground to use the fixed internal oscillator frequency.

SDO (Pin 30): Tri-State Serial Data Output Pin. The SDO pin is the SPI digital communication port from the LT8204 to the host microprocessor. During the data output period, this pin is used as serial data output. When the $\overline{\text{CS}}$ pin is HIGH, the SDO pin is in a high impedance state. This allows sharing of the serial interface with other devices.

SDI (Pin 31): Serial Data Input Pin. The SDI pin is the SPI digital communication port from the host microprocessor to the LT8204. SDI sends the 32-bit command instruction to the LT8204 at the rising edge of SCK. The input word is encoded with Hamming code to allow for error detection and correction by the LT8204. The LT8204 accepts input word lengths of 32 bits. See Figure 8.

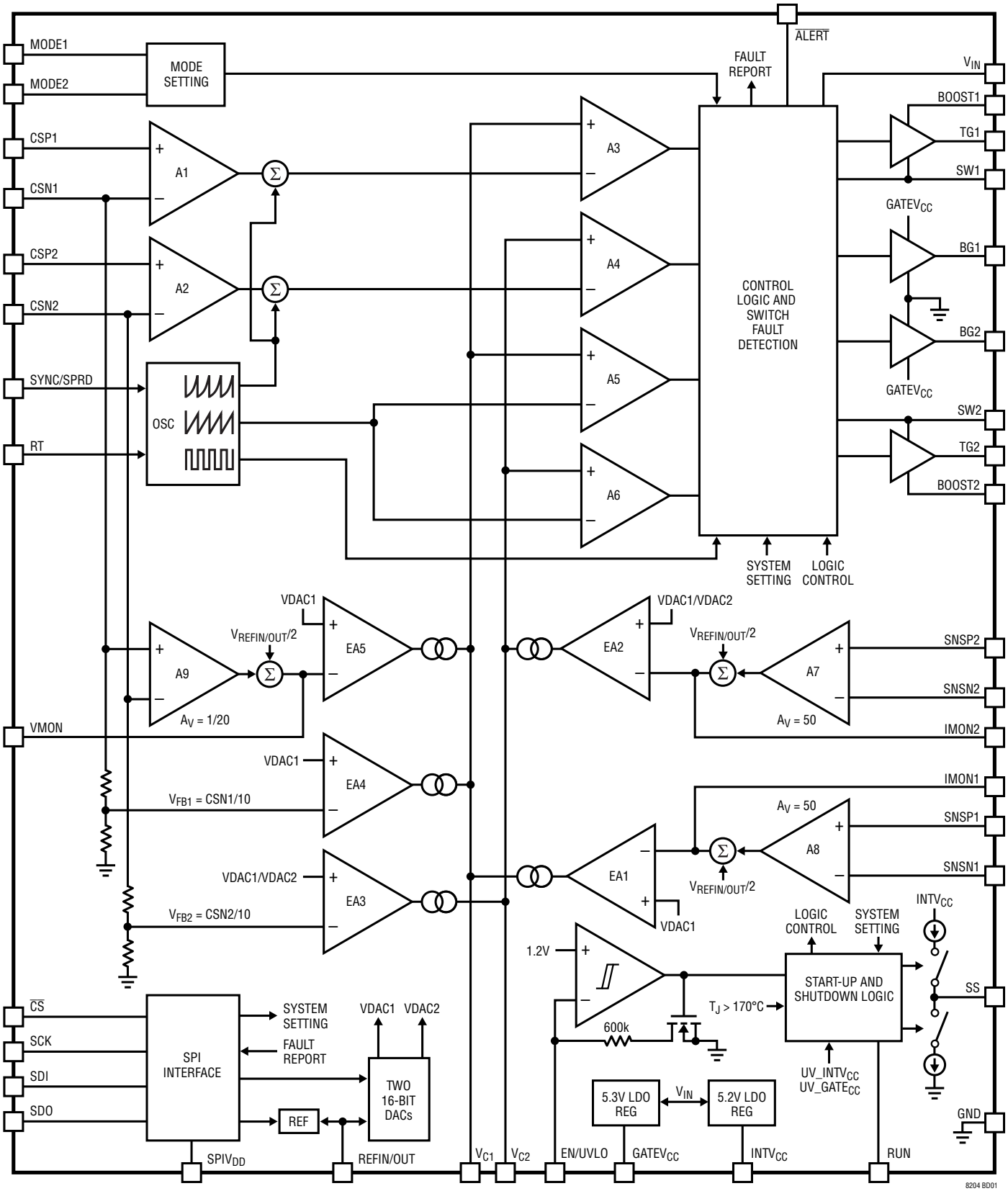
SCK (Pin 32): Serial Clock Input Pin. The SCK pin is the clock input for the SPI digital communication between the host and the LT8204. The SCK pin is used to synchronize the data transfer. Each bit of data is shifted into the SDI pin on the rising edge of the serial clock, while each bit of data is shifted out of the SDO pin on the falling edge of the serial clock.

$\overline{\text{CS}}$ (Pin 33): SPI Chip Select Pin. The $\overline{\text{CS}}$ pin is the chip select input for the SPI digital communication between the host microprocessor and the LT8204. When $\overline{\text{CS}}$ is active low, SCK is enabled, and the selected LT8204 is allowed to receive and transmit data across a shared SPI communication bus. When $\overline{\text{CS}}$ is high, SCK is disabled, and the specified command (See Figure 1) is executed.

$SPIV_{DD}$ (Pin 34): External SPI Interface Supply Voltage Pin. Connect this pin to the same voltage potential as the host microprocessor to make sure the output voltage level of the SDO pin is compatible with the host microprocessor. Decouple this pin to ground with a low ESR ceramic capacitor placed close to the IC.

GND (Exposed Pad Pin 39): Ground Pin. The exposed pad of the TSSOP package is an electrical connection to GND. To ensure proper electrical and thermal performance, tie the exposed pad directly to the local ground plane.

BLOCK DIAGRAM



TIMING DIAGRAM

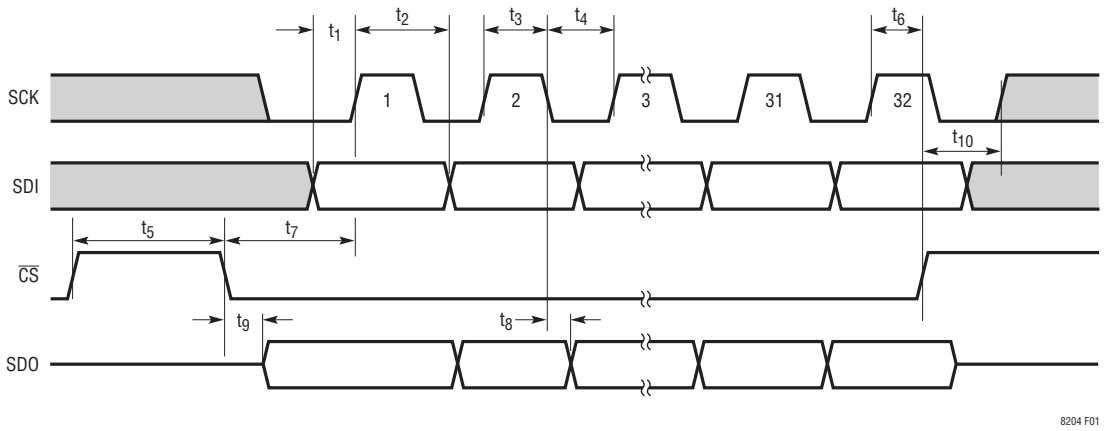


Figure 1. SPI Timing Diagram

OPERATION

The LT8204 integrates quad N-channel MOSFET gate drivers. It can be configured as either a four-switch full-bridge controller or a dual two-switch half-bridge controller. In terms of output regulation, it can be either the output current regulation or the output voltage regulation. The LT8204 provides two selectable PWM control methods, i.e., voltage mode control or peak current mode control, to ease loop compensation for applications with different load types. Operation is best understood by referring to the typical application circuit on the front page and the Block Diagram.

SYSTEM CONFIGURATION

The LT8204 configures the system architecture based on the MODE1 and MODE2 pin connections, as shown in Table 1. Note that configurations #1 and #9 are the same.

Topology

The LT8204 can be configured as a four-switch full-bridge controller, as shown in Figure 2, with the power switches controlled as shown in Figure 3. At the beginning of every cycle, switches MT1 and MB2 are turned on, and both the L1 and L2 inductor current ramps up. When switches MT1 and MB2 are commanded to be turned off by the control loop, switches MB1 and MT2 are turned on for the rest of the cycle, and both L1 and L2 inductor current ramps down. V_{OUT1} and V_{OUT2} voltages are regulated at $D \bullet V_{IN}$ and $(1 - D) \bullet V_{IN}$, respectively, and therefore the voltage across the load is $V_{OUT1} - V_{OUT2} = (2D - 1) \bullet V_{IN}$.

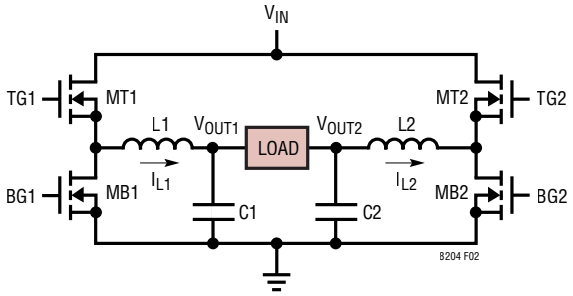


Figure 2. Simplified Diagram of the Four-Switch Full-Bridge

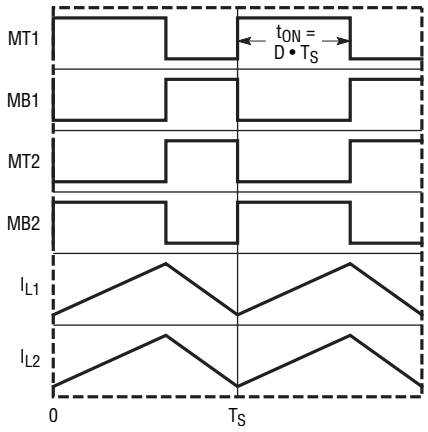


Figure 3. Operation of the Four-Switch H-Bridge

The LT8204 can also be configured as a dual two-switch half-bridge controller, as shown in Figure 4, with the power switches controlled as shown in Figure 5. The two half bridges operate 180° out of phase with each other to minimize the power loss and noise. At the beginning of every clock cycle, switch MT1 is turned on, and L1

Table 1. System Configuration Based on MODE1 and MODE2 Pin Connection (0 = Low (Tie to GND), Z = Float, 1 = High (Tie to $INTV_{CC}$))

No.	MODE2	MODE1	SYSTEM CONFIGURATION					
			TOPOLOGY		OUTPUT REGULATION		PWM CONTROL METHOD	
			SINGLE H-BRIDGE	DUAL HALF-BRIDGE	OUTPUT CURRENT	OUTPUT VOLTAGE	VOLTAGE MODE	CURRENT MODE
1	0	0	X		X		X	
2	0	1	X		X			X
3	1	0		X	X		X	
4	1	1		X	X			X
5	0	Z	X			X	X	
6	Z	0	X			X		X
7	1	Z		X		X	X	
8	Z	1		X		X		X
9	Z	Z	X		X		X	

OPERATION

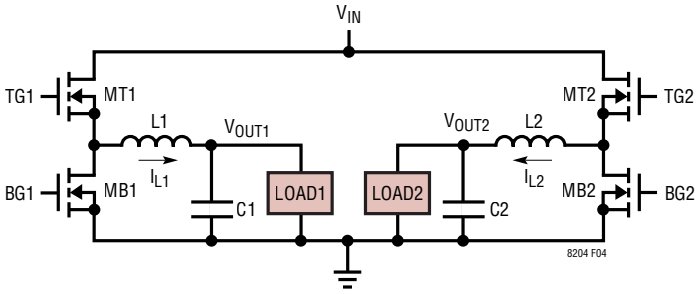


Figure 4. Simplified Diagram of the Dual Two-Switch Half-Bridge

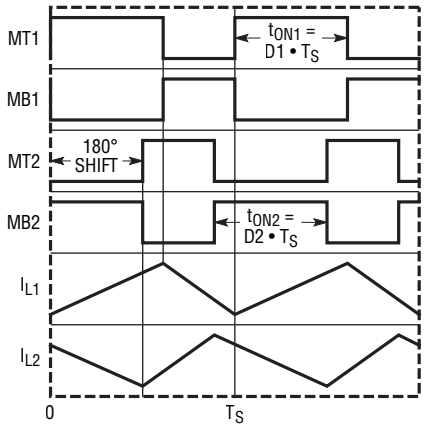


Figure 5. Operation of the Dual Two-Switch Half-Bridge

inductor current ramps up. When switch MT1 is commanded to be turned off by the control loop, switch MB1 is turned on for the rest of the cycle, and L1 inductor current ramps down. The turn-on of the switch MT2 in the second half-bridge is 180° out of phase to the clock. There is a second separate control loop to command the switch MT2 to turn off and then turn on switch MB2. V_{OUT1} and V_{OUT2} voltages are regulated at D1 • V_{IN} and D2 • V_{IN}, respectively.

Output Regulation

The LT8204 regulates either the output voltage or the output current. For the full-bridge configuration, the output regulation can be bidirectional, either the output voltage or the output current. For the dual half-bridge configuration, the output voltage regulation can only be a positive value reference to GND, while the output current regulation can be either direction depending on the state of bit SS10 in the system setup register (see Internal Registers section). In Figure 6, at SS10 = 0, the output current flows out of the LC filter, and the half-bridge operates as a current source for a load reference to GND (Load-to-GND). In Figure 7, at SS10 = 1, the output current flows into the LC filter, and the half-bridge operates as a current sink for a load reference to V_{IN} (Load-to-V_{IN}).

PWM Control Method

The LT8204 features two PWM control methods: voltage mode control and peak current mode control.

In the voltage mode control, the V_C pin voltage compares with an internal voltage ramp (see the PWM comparators A5 and A6 in the block diagram) and hence determines the duty cycle of the SW pin switching waveform.

In the peak current mode control, the V_C pin voltage determines the peak current in the inductor (see the inductor current sense amplifiers A1 and A2 and the PWM comparators A3 and A4 in the block diagram) and hence the duty cycle of the SW pin switching waveform.

OPERATION

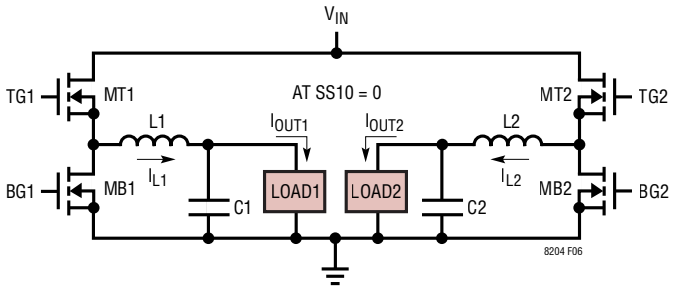


Figure 6. Dual Half-Bridge as Current Sources with Load-to-GND

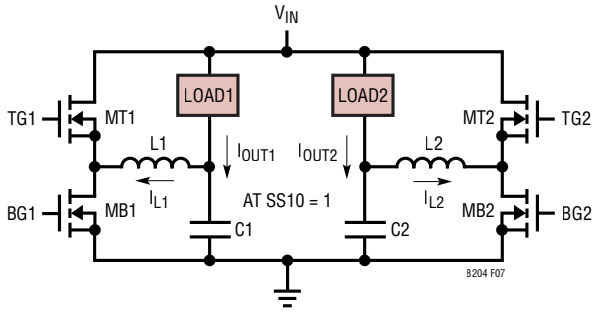


Figure 7. Dual Half-Bridge as Current Sources with Load-to-V_{IN}

SERIAL PERIPHERAL INTERFACE (SPI)

The LT8204 uses SPIV_{DD}, $\overline{CS}$, SCK, SDI, and SDO pins for SPI communication. When the $\overline{CS}$ pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock (SCK pin). The 5-bit header, HD4 to HD0 = 10110, is loaded first, followed by the 5-bit command word, C4 to C0, and then the 16-bit data word, D15 to D0, and finally the 6-bit hamming code, H5 to H0, in straight binary format. Data can only be transferred to the LT8204 when the $\overline{CS}$ signal is low. The rising edge of $\overline{CS}$ ends the data transfer and causes the device to carry out the action specified in the 32-bit input word.

The LT8204 also shifts out data on the SDO pin when the $\overline{CS}$ pin is low. At the falling edge of $\overline{CS}$, a 1-bit acknowledgement ACK, is presented on the SDO pin, and then on the falling edges of the clock (SCK pin), the 4-bit system run status word, SR3 to SR0, is shifted out, followed by the 5-bit command, C4 to C0, and then the 16-bit data word, D15 to D0, and finally the 6-bit hamming code, H5 to H0, in straight binary format. Data can only be transferred from the LT8204 when the $\overline{CS}$ signal is low. The rising edge of $\overline{CS}$ ends the data transfer and causes the SDO pin to be in high impedance mode.

The complete sequence for SPI data transfer to and from the LT8204 is shown in Figure 8.

Null SPI Transaction

The LT8204 allows a null SPI transaction, in which the $\overline{CS}$ pin can be pulsed low without a clock on the SCK pin. With this feature, the host microprocessor (µP) can check if the previous transaction was acknowledged by the first data bit shown on the SDO pin, i.e., the ACK bit, after the $\overline{CS}$ pin is low. The µP can then make a decision on the next SDI input word while the $\overline{CS}$ pin is pulled high without clocking the SCK pin. After the null SPI transaction, the ACK bit is set to 1.

Error Detection and Correction

During the SPI transaction, both the 32-bit input word for the SDI data and the 32-bit output word for the SDO data incorporate a 6-bit hamming code for error detection and correction.

Table 2 shows the parity bit coverage map provided by the 6-bit hamming code, and Table 3 shows the equations to generate the 6-bit hamming code (with an example provided). With 6 parity bits for 26 data bits, the hamming code used in the LT8204 features the capability of single-error correction and double-error detection.

SPI Transaction Acknowledgement

The ACK bit is set to 1 when the previous SPI transaction was accepted by the LT8204. It is set to 0 when any of the following conditions happen: number of SCK clock not equal to 0 or 32 within a $\overline{CS}$ pin low pulse; double errors detected in the transaction; misuse of command codes (see SPI Command Codes section). In addition to set the ACK bit to 0 in case of a fault in the transaction, the $\overline{ALERT}$ pin is also pulled low until the next $\overline{CS}$ pin falling edge.

System Run Status Word, SR3 to SR0

The 4-bit system run status word, SR3 to SR0, reports the system run status of the LT8204 right before the falling edge of the $\overline{CS}$ pin, shown in Table 4. Note that only the seven codes shown in Table 4 are valid for system run status. If any one of the other codes not listed in Table 4 is received by the µP, it indicates either a SPI transaction error

OPERATION

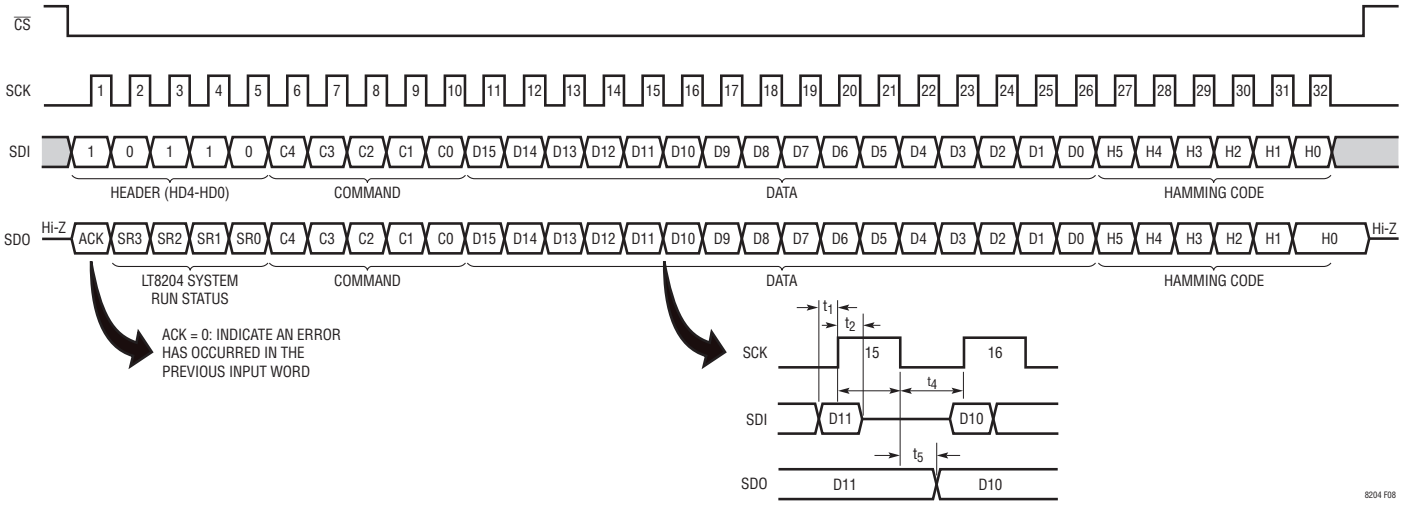


Figure 8. SPI 32-Bit Load Sequence

Table 2. Parity Bit Coverage Map by the Hamming Code (Note: the data on the 1st SCK period is defined as B25, followed by B24 on the 2nd SCK period, and finally B0 on the 26th SCK period.)

26-Bit Data Bit				B25		B24	B23	B22		B21	B20	B19	B18	B17	B16	B15		B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Corresponding SDI Data		**H0**	**H1**	HD4	**H2**	HD3	HD2	HD1	**H3**	HD0	C4	C3	C2	C1	C0	D15	**H4**	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	**H5**
Corresponding SDO Data		**H0**	**H1**	ACK	**H2**	S3	S2	S1	**H3**	S0	C4	C3	C2	C1	C0	D15	**H4**	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	**H5**
Parity Bit Coverage	**H0**	x		x		x		x		x		x		x		x		x		x		x		x		x		x		x		x		
	H1		x	x			x	x			x	x			x	x			x	x			x	x			x	x			x	x		
	H2				x	x	x	x					x	x	x	x					x	x	x	x					x	x	x	x		
	H3								x	x	x	x	x	x	x	x									x	x	x	x	x	x	x	x		
	H4																x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
	H5	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	

Table 3. Hamming Code Generation

PARITY BIT	BIT GENERATION
H0	XOR (B25, B23, B21, B19, B17, B15, B13, B11–B10, B8, B6, B4–B3, B1–B0)
H1	XOR (B25–B24, B21–B20, B17–B16, B13–B12, B10–B9, B6–B5, B3, B2, B0)
H2	XOR (B25 to B22, B17 to B14, B10 to B7, B3 to B1)
H3	XOR (B25 to B18, B10 to B4)
H4	XOR (B25 to B11)
H5	XOR (B25 to B0, H4 to H0)
Example: For B25 to B0 = 1011 0001 0110 1010 1010 1010 10, H5 to H0 = 001101	

OPERATION

Table 4. System Run Status Word

SR3 TO SR0	SYSTEM RUN STATUS
0000	Switching stopped; waiting for the µP to set up the system setup register
0001	Switching stopped; waiting for $GATEV_{CC}$, REFIN/OUT, V_C or SS pin voltage to be ready, or thermal shutdown to be cleared
0010	Switching stopped; waiting for RUN pin to go high
0011	In Hold Mode; waiting for RUN pin to go high
0100	In soft shutdown
0101	In soft start-Up
0111	Running
1100	Running at IMON1 with PMOS input pair and IMON2 with PMOS input pair
1101	Running at IMON1 with NMOS input pair and IMON2 with PMOS input pair
1110	Running at IMON1 with PMOS input pair and IMON2 with NMOS input pair
1111	Running at IMON1 with NMOS input pair and IMON2 with NMOS input pair

due to $\overline{CS}$ pin connection or sequence error (if SR3 to SR0 = 0110) or a system setup issue (if SR3 to SR0 = 10xx).

The last four codes, SR3–SR0 = 11xx, shown in the table indicate the operation modes of the dual IMON current monitors during system running. To achieve rail-to-rail operation, the LT8204 IMON design detects the input common mode and selects different input pairs accordingly. When the current sense pins, SNSP and SNSN pins, have a common mode voltage of higher than 2.7V (typical), the IMON current monitor selects the NMOS input pair; when the common mode voltage is lower than 2.3V (typical), the IMON current monitor selects the PMOS input pair.

INTERNAL REGISTERS

The LT8204 has six internal registers: system setup register, DAC1 register, DAC2 register, $\overline{AlertMask}$ register, bit flip register and fault status register. These registers are initialized to all 0 when the EN/UVLO pin voltage is lower than its rising threshold.

System Setup Register

The system setup register maintains the commands to set up the LT8204 system operation, as shown in Table 5.

SS15 to SS13: These three bits, HBRIDGE, VMODE, and IFB, indicate the system configuration as shown in Table 1, and they are read only through the SPI transaction. The µP can utilize these bits to confirm the system configuration before starting switching.

SS12, SS11: The SS12 bit, REF_INT, selects internal REFIN/OUT mode at 1 and external REFIN/OUT mode at 0. In the internal REFIN/OUT mode with SS12 = 1, the SS11 bit, REF_INT_LOW, further defines the voltage value at the REFIN/OUT pin: 2.048V at 1 and 4.096V at 0. For the µP to write into SS12–SS11 bits, the LT8204 should be in non-switching mode, i.e., when the SR3, SR2 bits in the system run status word are not 11 and the RUN pin is low.

SS10: The SS10 bit, LOAD_TO_VIN, is used only in the dual half-bridge configuration with output current

Table 5. System Setup Register

SS15	SS14	SS13	SS12	SS11	SS10	SS9	SS8
HBRIDGE 1: in H-Bridge 0: in Half-Bridge	VMODE 1: in Voltage Mode Control 0: in Peak Current Mode Control	IFB 1: in Output Current Regulation 0: in Output Voltage Regulation	REF_INT 1: Internal REFIN/OUT Mode 0: External REFIN/OUT Mode	REF_INT_LOW 1: 2.048V Internal REFIN/OUT 0: 4.096V Internal REFIN/OUT	LOAD_TO_VIN 1: Load-to-V_{IN} 0: Load-to-GND	LOW_ILIM 1: 25mV Threshold 0: 75mV Threshold	IN_PHASE 1: in Phase Control 0: out of Phase Control
SS7	**SS6**	**SS5**	**SS4**	**SS3**	**SS2**	**SS1**	**SS0**
DCM 1: in DCM Mode 0: in CCM Mode	TWODAC 1: use DAC2 for the Second Bridge 0: use DAC1 for the Second Bridge	SSDB 1: without Soft Shutdown Control 0: with Soft Soft Shutdown Control	HOLD 1: with Hold Mode 0: without Hold Mode	Must be 0	Must be 0	SETUP_DONE1 11: setup Done 10: setup Not Done	SETUP_DONE0 01: setup Not Done 00: setup Not Done

OPERATION

regulation. It needs to be set at 1 for application with load referenced to V_{IN} (Load-to-V_{IN}) and at 0 for application with load referenced to GND (Load-to-GND). For the µP to write into the SS10 bit, the LT8204 should be in non-switching mode, i.e., when the SR3–SR2 bits in the system run status word are not 11 and the RUN pin is low.

SS9: The SS9 bit, LOW_ILIM, defines the maximum inductor current sense threshold as 25mV at 1 and 75mV at 0. For the µP to write into the SS10 bit, the LT8204 should be in non-switching mode, i.e., when the SR3–SR2 bits in the system run status word are not 11 and the RUN pin is low.

SS8: The SS8 bit, IN_PHASE, provides an option to choose between 180° out of phase and 0° in phase operation in dual half-bridge configuration. By default, the LT8204 operates the dual half-bridge at 180° out of phase with SS8 = 0, and 0° in phase operation is selected with SS8 = 1. For the µP to write into the SS8 bit, the LT8204 should be in non-switching mode, i.e., when the SR3-SR2 bits in the system run status word are not 11 and the RUN pin is low.

SS7: The SS7 bit, DCM, sets the operation mode in a dual half-bridge configuration with Load-to-GND. At 1, the LT8204 operates with DCM mode to prevent reverse inductor current from the output to the input. At 0, the LT8204 operates with CCM mode to allow reverse inductor current.

SS6: The SS6 bit, TWODAC, determines which DAC's output voltage is used for the second half-bridge in the dual half-bridge configuration. At 1, DAC2 output voltage is used for the second half-bridge, and at 0, DAC1 output voltage is used for both the first and second half bridges. The µP is able to write and read the SS6 at all times after both EN/UVLO and $INTV_{CC}$ pin voltages are higher than their respective rising UVLO thresholds.

SS5: The SS5 bit, SSDB, determines whether the LT8204 has soft shutdown control. At 0, the LT8204 has soft shutdown control, and at 1 and when the SS4 bit is 0, the LT8204 does not have soft shutdown control. The µP is able to write and read the SS5 at all times after both EN/UVLO and $INTV_{CC}$ pin voltages are higher than their respective rising UVLO thresholds, but the LT8204 will not react to he transition of 0 to 1 when the system is already in soft shutdown mode, i.e., when the SR3 to SR0 bits in the system run status word are 0100.

SS4: The SS4 bit, HOLD, determines whether the LT8204 has hold mode during shutdown. At 0, the LT8204 does not have hold mode, and at 1, the LT8204 has hold mode. The µP is able to write and read the SS4 bit at all times after both EN/UVLO and $INTV_{CC}$ pin voltages are higher than their respective rising UVLO thresholds.

SS3, SS2: These two bits must be set to 00 for proper LT8204 system operation.

SS1, SS0: The SETUP_DONE1 and SETUP_DONE0 bits are used to indicate that the µP has finished setting up the system setup register. When the SS1–SS0 bits are set to 11 and the RUN pin is high, the LT8204 is ready to start switching. The µP is able to write and read the SS1–SS0 bits at all times after both EN/UVLO and $INTV_{CC}$ pin voltages are higher than their respective rising UVLO thresholds. However, the LT8204 will not respond to the transition of 11 to 10 or 01 or 00 when the system is already in soft shutdown mode, i.e., when the SR3 to SR0 bits in the system run status word are 0100.

DAC1, DAC2 Registers

The DAC1 register and DAC2 register maintain the 16-bit input codes to control the DAC1 and DAC2 output voltages, respectively. The µP is able to write and read the DAC1 register and the DAC2 register at all times after both EN/UVLO and $INTV_{CC}$ pin voltages are higher than their respective rising UVLO thresholds.

$\overline{\text{AlertMask}}$ Register

The $\overline{\text{AlertMask}}$ register maintains the commands on whether to mask a certain fault condition from triggering the $\overline{\text{ALERT}}$ pin low, as shown in Table 6. The µP is able to write and read AM15 to AM3 at all times after both EN/UVLO and $INTV_{CC}$ pin voltages are higher than their respective rising UVLO thresholds.

AM15: The AM15 bit, when at 0, masks the fault in the IMON1 and IMON2 pin voltage differences in full-bridge configuration to the $\overline{\text{ALERT}}$ pin.

AM14: The AM14 bit, when at 0, masks the fault in IMON1 regulation referenced to the DAC output voltage to the $\overline{\text{ALERT}}$ pin.

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Table 6. $\overline{\text{AlertMask}}$ Register

AM15	AM14	AM13	AM12	AM11	AM10	AM9	AM8
IMON1 and IMON2 Pin Voltage Difference in Full-Bridge Configuration	IMON1 Regulation Referenced to the DAC Output Voltage	IMON2 Regulation Referenced to the DAC Output Voltage	Switches MT1 and MB1	Switches MT2 and MB2	IMON1 Positive Maximum Regulation	IMON1 Negative Maximum Regulation	IMON2 Positive Maximum Regulation
AM7	**AM6**	**AM5**	**AM4**	**AM3**	**AM2**	**AM1**	**AM0**
IMON2 Negative Maximum Regulation	RT Pin	IMON1 Pin Current Limit	IMON2 Pin Current Limit	Load Short	Not Writable, Internally Latched at 0	Not Writable, Internally Latched at 0	Not Writable, Internally Latched at 0

AM13: The AM13 bit, when at 0, masks the fault in IMON2 regulation referenced to the DAC output voltage to the $\overline{\text{ALERT}}$ pin.

AM12: The AM12 bit, when at 0, masks the fault in switches MT1 and MB1 to the $\overline{\text{ALERT}}$ pin.

AM11: The AM12 bit, when at 0, masks the fault in switches MT2 and MB2 to the $\overline{\text{ALERT}}$ pin.

AM10: The AM10 bit, when at 0, masks the fault in IMON1 positive maximum regulation to the $\overline{\text{ALERT}}$ pin.

AM9: The AM9 bit, when at 0, masks the fault in IMON1 negative maximum regulation to the $\overline{\text{ALERT}}$ pin.

AM8: The AM8 bit, when at 0, masks the fault in IMON2 positive maximum regulation to the $\overline{\text{ALERT}}$ pin.

AM7: The AM7 bit, when at 0, masks the fault in IMON2 negative maximum regulation to the $\overline{\text{ALERT}}$ pin.

AM6: The AM6 bit, when at 0, masks the fault in the RT pin to the $\overline{\text{ALERT}}$ pin.

AM5: The AM5 bit, when at 0, masks the fault in the IMON1 pin current limit to the $\overline{\text{ALERT}}$ pin.

AM4: The AM4 bit, when at 0, masks the fault in the IMON2 pin current limit to the $\overline{\text{ALERT}}$ pin.

AM3: The AM3 bit, when at 0, masks the fault in load short to the $\overline{\text{ALERT}}$ pin.

AM2 to AM0: These bits are latched at 0 in the LT8204 design.

Bit Flip Register

The bit flip register reports a bit flip fault in the system setup register, DAC1 register, DAC2 register, and $\overline{\text{AlertMask}}$ register, as shown in Table 7. The bits in this register are read only via SPI transaction.

BF15: The BF15 bit is set to 1 if one or all three SS15 to SS13 bits in the system setup register flip after both EN/UVLO and $INTV_{CC}$ pin voltages are higher than their respective rising UVLO thresholds.

BF14: The BF14 bit is set to 1 if odd numbers of SS12 to SS8 bits in the system setup register flip when the LT8204 is in switching mode, i.e., when the SR3-SR2 bits in the system run status word are 01 or 11.

BF13: The BF13 bit is set to 1 if odd numbers of SS7 to SS0 bits in the system setup register flip after the bits are written.

BF12: The BF12 bit is set to 1 if odd numbers of bits in the DAC1 register flip after the bits are written.

BF11: The BF11 bit is set to 1 if odd numbers of bits in the DAC2 register flip after the bits are written.

BF10: The BF10 bit is set to 1 if odd numbers of bits in the $\overline{\text{AlertMask}}$ register flip after the bits are written.

Fault Status Register

The fault status register reports various system operation status/faults, as shown in Table 8. The µP can read and clear the states of all FS15 to FS0 bits. With the clear fault status register command code, all FS15 to FS0 bits are reset to 0000H.

FS15: The FS15 bit is set and latched to 1 if there is a fault in the IMON1 and IMON2 pin voltage difference in full-bridge configuration.

OPERATION

Table 7. Bit Flip Register

BF15	BF14	BF13
Set 1 When SS15 to 13 in System Setup Register Has Odd Number Bit Flip	Set 1 When SS12 to 8 in System Setup Register Has Odd Number Bit Flip	Set 1 When SS7 to 0 in System Setup Register Has Odd Number Bit Flip
BF12	**BF11**	**BF10**
Set 1 When DAC1 Register Has Odd Number Bit Flip	Set 1 When DAC2 Register Has Odd Number Bit Flip	Set 1 When $\overline{\text{AlertMask}}$ Register Has Odd Number Bit Flip

Table 8. Fault Status Register

FS15	FS14	FS13	FS12	FS11	FS10	FS9	FS8
IMON1 and IMON2 Pin Voltage Difference in Full-Bridge Configuration	IMON1 Regulation Referenced to the DAC Output Voltage	IMON2 Regulation Referenced to the DAC Output Voltage	Switches MT1 and MB1	Switches MT2 and MB2	IMON1 Positive Maximum Regulation	IMON1 Negative Maximum Regulation	IMON2 Positive Maximum Regulation
FS7	**FS6**	**FS5**	**FS4**	**FS3**	**FS2**	**FS1**	**FS0**
IMON2 Negative Maximum Regulation	RT Pin	IMON1 Pin Current Limit	IMON2 Pin Current Limit	Load Short	Bit Flip	Temp1	Temp0

FS14: The FS14 bit is set and latched to 1 if there is a fault in IMON1 regulation referenced to the DAC output voltage.

FS13: The FS13 bit is set and latched to 1 if there is a fault in IMON2 regulation referenced to the DAC output voltage.

FS12: The FS12 bit is set and latched to 1 if there is a fault in switches MT1 and MB1.

FS11: The FS11 bit is set and latched to 1 if there is a fault in switches MT2 and MB2.

FS10: The FS10 bit is set and latched to 1 if there is a fault in IMON1 positive maximum regulation.

FS9: The FS9 bit is set and latched to 1 if there is a fault in IMON1 negative maximum regulation.

FS8: The FS8 bit is set and latched to 1 if there is a fault in IMON2 positive maximum regulation.

FS7: The FS7 bit is set and latched to 1 if there is a fault in IMON2 negative maximum regulation.

FS6: The FS6 bit is set and latched to 1 if there is a fault in the RT pin.

FS5: The FS5 bit is set and latched to 1 if there is a fault in the IMON1 pin current limit.

FS4: The FS4 bit is set and latched to 1 if there is a fault in the IMON2 pin current limit.

FS3: The FS3 bit is set and latched to 1 if there is a fault in the load short.

FS2: The FS2 bit is set and latched to 1 if there is a bit flip fault, i.e., any one of the BF15 to BF10 bits is 1. Once the FS2 bit is 1, the $\overline{\text{ALERT}}$ pin is pulled low.

FS1, FS0: The FS1–FS0 bits report the die temperature range. If the die temperature is T_J < 130°C, FS1–FS0 = 01; at 130°C < T_J < 155°C, FS1–FS0 = 00; at 155°C < T_J < 170°C, FS1–FS0 = 10; T_J > 170°C, FS1–FS0 = 11, where 170°C is the thermal shutdown threshold. Once FS1–FS0 bits are set to 11 as T_J > 170°C, they are latched at 11 until receiving the clear FAULT STATUS register command. Once the FS1-FS0 bits are 11, the $\overline{\text{ALERT}}$ pin is pulled low. The 130°C, 155°C, and 170°C thresholds are not production tested.

SPI COMMAND CODES

Table 9 shows the LT8204 SPI command codes. Codes #1 to #17 are used to read, write, and clear various internal registers. For SPI transactions with command codes #1 to #17, the C4 to C0 word in the SDO data is set to the same word as in the SDI data during the previous SPI transaction. Command codes other than #1 to #17 are invalid. In case of receiving invalid command codes from

OPERATION

Table 9. SPI Command Codes

No.	COMMAND WORD					COMMAND
	C4	C3	C2	C1	C0	
1	0	0	0	0	0	Read $\overline{\text{AlertMask}}$ register in the next SPI transaction
2	0	0	0	0	1	Write $\overline{\text{AlertMask}}$ register with D15 to D3; read $\overline{\text{AlertMask}}$ register in the next SPI transaction
3	0	0	0	1	0	Write $\overline{\text{AlertMask}}$ register with D15 to D3; read system setup register in the next SPI transaction
4	0	0	0	1	1	Write $\overline{\text{AlertMask}}$ register with D15 to D3; read fault status register in the next SPI transaction
5	0	0	1	0	0	Read DAC1 register in the next SPI transaction
6	0	0	1	0	1	Write DAC1 register with D15 to D0; read DAC1 register in the next SPI transaction
7	0	0	1	1	0	Write DAC1 register with D15 to D0; read system setup register in the next SPI transaction
8	0	0	1	1	1	Write DAC1 register with D15 to D0; read fault status register in the next SPI transaction
9	0	1	0	0	0	Read DAC2 register in the next SPI transaction
10	0	1	0	0	1	Write DAC2 register with D15 to D0; read DAC2 register in the next SPI transaction
11	0	1	0	1	0	Write DAC2 register with D15 to D0; read system setup register in the next SPI transaction
12	0	1	0	1	1	Write DAC2 register with D15 to D0; read fault status register in the next SPI transaction
13	0	1	1	0	0	Read system setup register in the next SPI transaction
14	0	1	1	0	1	Write system setup register with D12 to D0; read system setup register in the next SPI transaction
15	0	1	1	1	0	Read fault status register in the next SPI transaction
16	0	1	1	1	1	Clear fault status register (the data word on SDO will be 0000H in the next SPI transaction)
17	1	0	0	0	0	Read bit flip register in the next SPI transaction

Note: Command codes other than No.1 to No.17 are invalid. In case of receiving invalid command codes from the SPI transaction, the LT8204 ignores the command code, and sets the ACK and C4 to C0 bits in the SDO data to 0 and 11111 respectively, to notify the µP of the code misuse.

the SPI transaction, the LT8204 ignores the command code and sets ACK and C4 to C0 bits in the SDO data to 0 and 11111, respectively, to notify the µP of the code misuse. Once the FS1–FS0 bits are 11, the $\overline{\text{ALERT}}$ pin is pulled low.

FIRST SPI TRANSACTION

After the LT8204 is ready for SPI transaction, when the µP initiates the first SPI transaction, the SDI pin on the LT8204 receives data from the µP. At the same time, the LT8204 sends out data on the SDO pin, and the command word and the data word shown on the SDO pin are 01100 (command code #13) and system setup register data, respectively.

POWER-UP SEQUENCE

The LT8204 enters shutdown mode and drains less than 2µA quiescent current when the EN/UVLO pin is below its shutdown threshold (0.3V minimum). Once the EN/UVLO pin is above its shutdown threshold (0.6V typical, 1V maximum), the LT8204 wakes up start-up circuitry, generates a bandgap reference, and powers up the internal $INTV_{CC}$ LDO. The $INTV_{CC}$ LDO supplies the internal control circuitry. Now the LT8204 enters undervoltage lockout (UVLO) mode with a hysteresis current (2µA typical) pulled into the EN/UVLO pin.

When the $INTV_{CC}$ pin is charged above its rising UVLO threshold (4.95V typical) and the EN/UVLO pin passes its rising enable threshold (1.225V typical), the LT8204 enters enable mode, in which the EN/UVLO hysteresis current is turned off. In enable mode, the LT8204 is going through the following procedures:

1. The internal $GATEV_{CC}$ LDO, which supplies the gate drivers, is being charged up from the ground.
2. The $\overline{\text{ALERT}}$ pin is asserted low to notify the µP that the LT8204 is ready to start SPI transaction and the system setup register needs to be programmed.
3. When internal REFIN/OUT mode is selected, the REFIN/OUT pin voltage is being charged up from the ground.

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When the following conditions are satisfied, the LT8204 finishes the power-up sequence:

1. $GATEV_{CC}$ voltage exceeds its rising UVLO threshold (4.65V typical);
2. REFIN/OUT pin voltage exceeds its rising UVLO threshold (1.7V typical in 2.048V internal REFIN/OUT mode, 3.5V typical in 4.096V internal REFIN/OUT mode, and 1.3V typical in external REFIN/OUT mode);
3. The junction temperature is less than its thermal shutdown threshold (170°C typical).

From the time of entering enable mode to the time of finishing the power-up sequence, the LT8204 initiates a power-on-reset (POR), waking up the entire internal control circuitry and settling to the right initial conditions. Meanwhile, the LT8204 is waiting for an internal signal, SWON, to go from low level to high level, in order to initiate the start-up of the switching actions. The SWON signal goes high after the following conditions are satisfied:

1) Software Switch Enable: The µP finishes setting up system setup register through SPI transactions (i.e., SS1 and SS0 bits are set to 11). At this time, the LT8204 pulls the $\overline{ALERT}$ pin high.

2) Hardware Switch Enable: RUN pin goes high and stays high for a certain time (40µs typical).

Figure 9 summarizes the LT8204 power-up sequence.

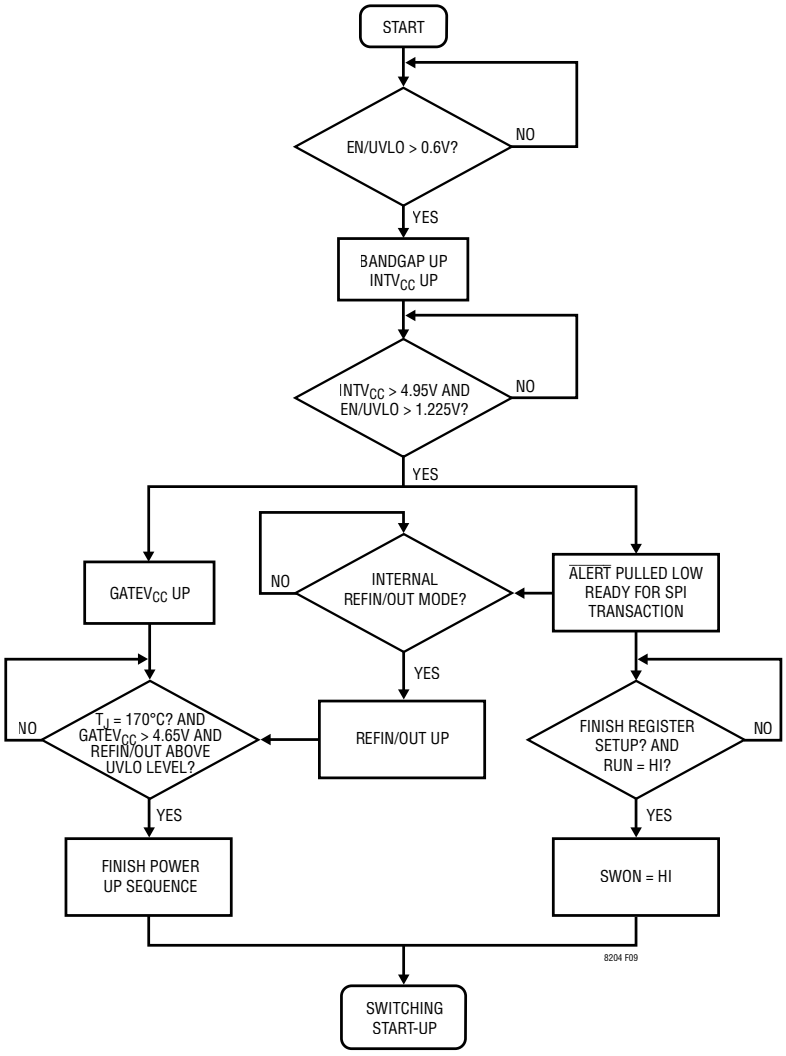

Figure 9. LT8204 Power-Up Sequence

OPERATION

START-UP AND SHUTDOWN: FULL-BRIDGE CONFIGURATION

Figure 10 shows the switching start-up and shutdown sequence for the LT8204 in the single H-Bridge configuration.

During the POR state, the SS pin is hard pulled down with an internal 200Ω resistor to ground. When the SWON signal goes high, the LT8204 enters the UP/INIT state, in which the SS pin is kept pulled down with the 200Ω resistor to ground. At the same time, the LT8204 also pulls down the $V_{C1(2)}$ pin with an internal 20kΩ resistor to ground. When the SS pin is pulled below 0.63V (typical) and also the $V_{C1(2)}$ pin is pulled below 0.8V (typical), the LT8204 enters the UP/VOUT state.

During the UP/VOUT state, the SS pin is charged up by a 10µA pull-up current. In this state, the LT8204 enables the switching action and controls power switches MT1–MB1 and MT2–MB2 with two individual control loops, as dual half bridges. Therefore, V_{OUT1} and V_{OUT2} are controlled separately. As the SS pin voltage ramps up, it controls the V_{OUT1} and V_{OUT2} voltages to soft start from 0V to $V_{IN}/2$. The V_{OUT1} and V_{OUT2} voltages are controlled as 12 • (V_{SS} – 0.7V) with a minimum and maximum value at 0V and $V_{IN}/2$, respectively.

When the SS pin is charged above 0.7V + $V_{IN}/19$, the LT8204 enters the UP/PRE state, where it controls the power switches, as shown in Figure 3. In the UP/PRE state, the SS pin is charged up with the 10µA pull-up current, and the LT8204 regulates the output differential voltage $V_{OUT1} – V_{OUT2}$ (output voltage regulation configuration) or the output current (output current regulation configuration) to be zero.

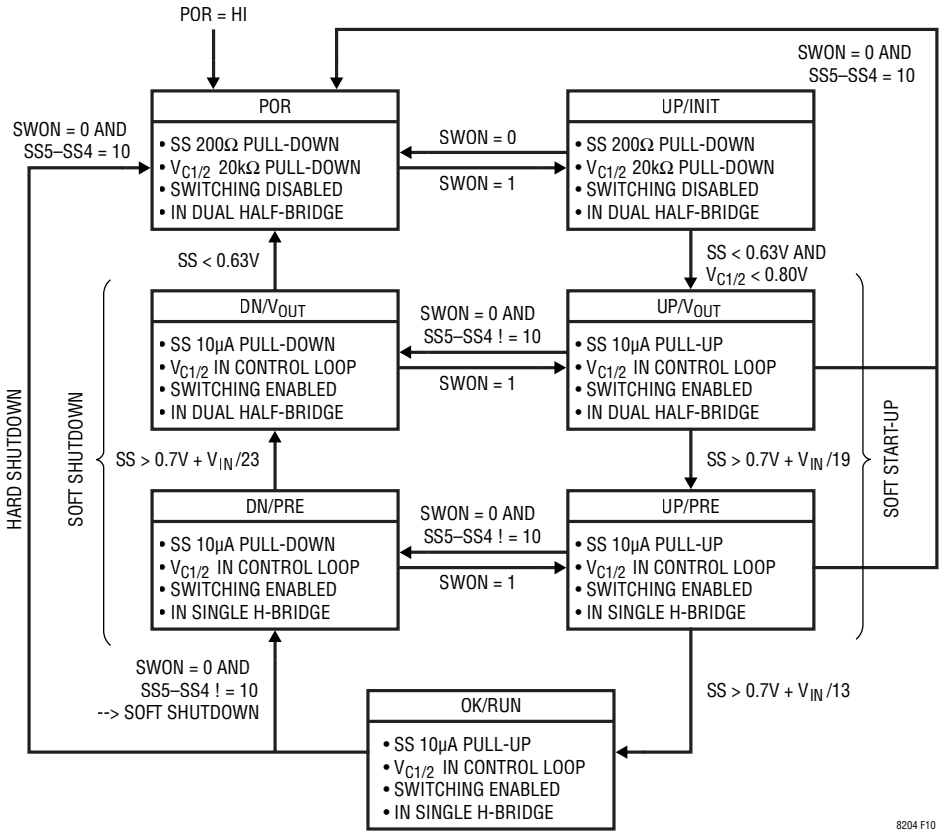

Figure 10. Start-Up and Shutdown Sequence in H-Bridge Configuration

OPERATION

When the SS pin is charged above 0.7V + V_{IN}/13, the LT8204 enters the OK/RUN state, where the output differential voltage V_{OUT1} – V_{OUT2} (output voltage regulation configuration) or the output current (output current regulation configuration) is controlled by the internal DAC1's output voltage, which is programmed via the SPI transaction.

The internal SWON signal goes low when the RUN pin goes low or the SS1–SS0 bits, SETUP_DONE1 and SETUP_DONE0, in the system setup register are no longer set to 11. Once the SWON signal goes low, the LT8204 starts the shutdown procedure based on the state of the SS5 bit, SSDB, and the SS4 bit, HOLD. The shutdown method is summarized in Table 10.

Soft Shutdown: With the soft shutdown method, the LT8204 transits from the OK/RUN state to the DN/PRE state, where it operates as in the UP/PRE state, except that the SS pin is discharged with a 10µA pull-down current. The LT8204 regulates the output differential voltage V_{OUT1} – V_{OUT2} (output voltage regulation configuration) or the output current (output current regulation configuration) to be zero.

When the SS pin is discharged below 0.7V + V_{IN}/23, the LT8204 enters the DN/V_{OUT} state, where it operates similar to the UP/V_{OUT} state, except that the SS pin is discharged with a 10µA pull-down current. As the SS pin voltage ramps down, it controls the V_{OUT1} and V_{OUT2} voltages to soft shutdown from V_{IN}/2 to 0V. The V_{OUT1} and V_{OUT2} voltages are controlled as 12 • (V_{SS} – 0.7V) with a maximum and minimum value at V_{IN}/2 and 0V, respectively.

Table 10. System Shutdown Methods in Full-Bridge Configuration

SS5–SS4	SYSTEM SHUTDOWN METHOD
00	**Soft Shutdown + No Hold:** Soft shutdown using the SS pin and then turn off all power switches after the SS pin voltage is below 0.63V
10	**Hard Shutdown + No Hold:** Stop switching and turn off all power switches instantly
01	**Soft Shutdown + Hold:** Soft shutdown using the SS pin and then turn off MT1 and MT2 power switches, but turn on MB1 and MB2 power switches after the SS pin voltage is below 0.63V
11	

When the SS pin is discharged below 0.63V, the LT8204 goes back to the POR state, where it stops switching. Then, depending on the state of the SS4 bit, HOLD, the power switches are in either Hold mode or No Hold mode.

Hard Shutdown: With the hard shutdown method, the LT8204 transitions directly from the OK/RUN state to the POR state, and turns off all power switches MT1, MB1, MT2, and MB2 immediately.

Figure 10 also shows that the LT8204 can transition among the states when the SWON signal changes during the soft start-up and soft shutdown procedure.

START-UP AND SHUTDOWN: DUAL HALF-BRIDGE CONFIGURATION

Figure 11 shows the start-up and shutdown sequence for the LT8204 in the dual half-bridge configuration.

During the POR state, the SS pin is hard pulled down with an internal 200Ω resistor to the ground. When the SWON signal goes high, the LT8204 enters the UP/INIT state, in which the SS pin is kept pulled down with the 200Ω resistor to ground. At the same time, the LT8204 also pre-positions the $V_{C1(2)}$ pin voltage based on the SS10 bit, Load-to-V_{IN}, in the system setup register. At SS10 = 0, the $V_{C1(2)}$ pin is pulled down with an internal 20kΩ resistor to the ground. At SS10 = 1 and in the output current regulation configuration, the $V_{C1(2)}$ pin is pulled up with an internal 20kΩ resistor to $INTV_{CC}$. When the SS pin is pulled below 0.63V (typical) and the $V_{C1(2)}$ pin is pulled below 0.8V (typical) at SS10 = 0 or above 2.63V (typical) at SS10 = 1, and in the output current regulation configuration, the LT8204 enters the OK/RUN state.

During the OK/RUN state, the LT8204 enables the switching action and controls power switches, as shown in Figure 5. The SS pin is charged up by a 10µA pull-up current, and its voltage controls the output voltage V_{OUT1} (V_{OUT2}) (output voltage regulation configuration) or the output current (output current regulation configuration) to gradually ramp up to the desired level commanded by the internal DAC's output voltage, which is programmed via the SPI transaction.

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The internal SWON signal goes low when the RUN pin goes low or the SS1–SS0 bits, SETUP_DONE1 and SETUP_DONE0, in the system setup register are no longer set to 11. Once the SWON signal goes low, the LT8204 starts the shutdown procedure based on the state of the SS5 bit, SSDB, and the SS4 bit, HOLD. The shutdown method is summarized in Table 11.

Table 11. System Shutdown Methods in Dual Half-Bridge Configuration

SS5–SS4	SYSTEM SHUTDOWN METHOD
00	**Soft Shutdown + No Hold:** Soft shutdown using the SS pin and then turn off all power switches after the SS pin voltage is below 0.63V
10	**Hard Shutdown + No Hold:** Stop switching and turn off all power switches instantly
01	**Soft Shutdown + Hold:** Soft shutdown using the SS pin and then turn off MT1 and MT2 power switches, but turn on MB1 and MB2 power switches after the SS pin voltage is below 0.63V
11	

Soft Shutdown: With the soft shutdown method, the LT8204 transits from the OK/RUN state to the DN/SS state, where the SS pin is discharged with a 10µA pull-down current. The pin voltage is then used to control the output voltage V_{OUT1} (V_{OUT2}) (output voltage regulation configuration) or the output current (output current regulation configuration) to gradually ramp down to zero.

When the SS pin is discharged below 0.63V, the LT8204 goes back to the POR state, where it stops switching. Then, depending on the state of the SS4 bit, HOLD, the power switches are in either Hold mode or No Hold mode.

Hard Shutdown: With the hard shutdown method, the LT8204 transits directly from the OK/RUN state to the POR state, and turns off all power switches MT1, MB1, MT2, and MB2 immediately.

Figure 11 also shows that the LT8204 can transit among the states when the SWON signal changes during the soft start-up and soft shutdown procedure.

IMON OUTPUT CURRENT MONITORING

The IMON1(2) pin provides an amplified and buffered monitor of the voltage between the SNSP1(2) and SNSN1(2) pins (see A7 and A8 in the block diagram). The IMON1(2) pin voltage is defined as:

$$V_{IMON1(2)} = 0.5 \bullet V_{REFIN/OUT} + 50 \bullet (V_{SNSP1(2)} - V_{SNSN1(2)})$$

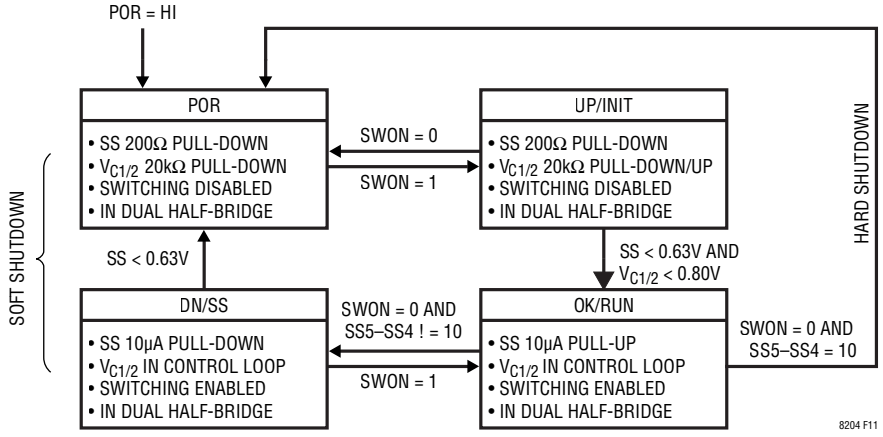

Figure 11. Start-Up and Shutdown Sequence in H-Bridge Configuration

OPERATION

The IMON1(2) pin voltage has a common mode value of 0.5 • $V_{REFIN/OUT}$ to identify a bidirectional current flow operation. $V_{IMON1(2)}$ = 0.5 • $V_{REFIN/OUT}$ represents a zero voltage across the SNSP1(2) and SNSN1(2) pins, i.e., a zero current flow through the SNSP1(2) and SNSN1(2) pins. $V_{IMON1(2)}$ > 0.5 • $V_{REFIN/OUT}$ represents a positive voltage across the SNSP1(2) and SNSN1(2) pins, i.e., a positive current flow through the SNSP1(2) and SNSN1(2) pins. $V_{IMON1(2)}$ < 0.5 • $V_{REFIN/OUT}$ represents a negative voltage across the SNSP1(2) and SNSN1(2) pins, i.e., a negative current flow through the SNSP1(2) and SNSN1(2) pins.

VMON DIFFERENTIAL OUTPUT VOLTAGE MONITORING

The VMON pin provides an attenuated and buffered monitor of the voltage between V_{OUT1} and V_{OUT2}, i.e., between the CSN1 and CSN2 pins (see A9 in the block diagram). The VMON pin voltage is defined as:

$$V_{VMON} = 0.5 \bullet V_{REFIN/OUT} + (V_{CSN1} - V_{CSN2}) / 20$$

The VMON pin voltage has a common mode value of 0.5 • $V_{REFIN/OUT}$ to identify a bidirectional voltage differential operation. V_{VMON} = 0.5 • $V_{REFIN/OUT}$ represents a zero voltage across the CSN1 and CSN2 pins. V_{VMON} > 0.5 • $V_{REFIN/OUT}$ represents a positive voltage across the CSN1 and CSN2 pins. V_{VMON} < 0.5 • $V_{REFIN/OUT}$ represents a negative voltage across the CSN1 and CSN2 pins.

REFIN/OUT REFERENCE MODES

The LT8204 has two reference modes for the REFIN/OUT pin: internal and external modes, with which the reference source can be selected.

The LT8204 has a precision 2.048V or 4.096V integrated reference with a typical temperature drift of 30ppm/°C. To use the internal reference, set the SS12 bit, REF_INT, in the system setup register to 1. The SS11 bit, REF_INT_LOW, in the system setup register defines the internal reference value: 1 for 2.048V and 0 for 4.096V. A buffer is needed if the internal reference is to drive external circuitry. For reference stability and low noise, a 6.3V or higher rated 2.2µF low ESR, X7R or X5R ceramic capacitor should be tied between REFIN/OUT and GND.

To use an external reference, set the SS12 bit, REF_INT, in the system setup register to 0. In this mode, the $INTV_{CC}$ LDO output voltage can be used as an external reference by connecting the $INTV_{CC}$ pin to the REFIN/OUT pin. The $INTV_{CC}$ LDO provides 1% output voltage accuracy.

DUAL 16-BIT DACS

The LT8204 has dual on-chip 16-bit DACs with guaranteed monotonicity to generate two voltage references for the error amplifiers and hence control the output voltage (output voltage regulation configuration) or the output current (output current regulation configuration).

Both DACs have an output voltage range from 1/18 • $V_{REFIN/OUT}$ to (17/18 • $V_{REFIN/OUT}$ – 1 • LSB). With 16 bits, the least significant bit (LSB) value of the output voltage is defined as 8/9 • $V_{REFIN/OUT}/2^{16}$.

The transfer function from the input code to the output voltage for both DACs is shown in Figure 12 and Figure 13. Note that in the dual half-bridge output voltage regulation configuration, the 16-bit input code is in straight binary format (Figure 12), and by default the output voltage is initialized to 1/18 • $V_{REFIN/OUT}$ after power-up. In other configurations, the binary two's complement format is used for the 16-bit input code (Figure 13), and by default, the output voltage is initialized to 1/2 • $V_{REFIN/OUT}$ after power-up.

FAULT DETECTION AND REPORT

The LT8204 monitors the system operation for various faults and reports them in the fault status register. Also, based on the setting in the $\overline{\text{AlertMask}}$ register, if a certain

OPERATION

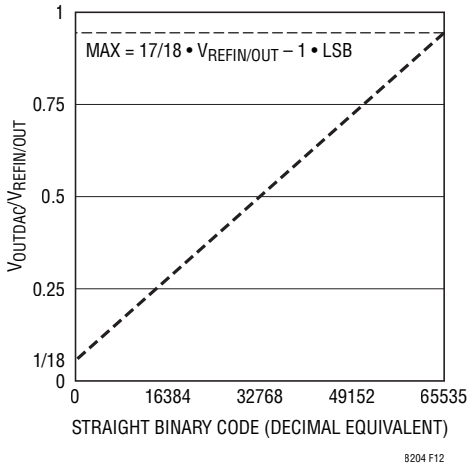

Figure 12. DAC Transfer Function in Dual Half-Bridge, Output Voltage Regulation Configuration

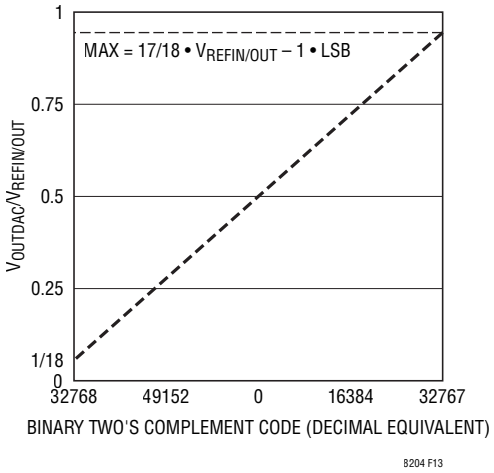

Figure 13. DAC Transfer Function in Configurations Other Than the Dual Half-Bridge, Output Voltage Regulation Configuration

fault is set to trigger the $\overline{\text{ALERT}}$ pin, it asserts the $\overline{\text{ALERT}}$ pin to a low state to interrupt the µP.

Output Current Regulation Fault Detection and Report

The LT8204 monitors the IMON1 and IMON2 pins to detect any fault in the output current regulation.

In the full-bridge output current regulation configuration, if the IMON1 and IMON2 pin voltage differences are larger than ±200mV between each other, this indicates a fault in the output current regulation. When this condition lasts for 31 consecutive switching cycles, the FS15 bit is latched in the fault status register to 1. This feature can be used to identify a load open fault.

In the output current regulation configuration, if the IMON1(2) pin voltage is < $V_{OUTDAC1(2)}$ – 200mV or > $V_{OUTDAC1(2)}$ + 200mV, this indicates a fault in the output current regulation. When this condition lasts for 31 consecutive switching cycles, the FS14(13) bit is latched in the fault status register to 1.

In the output current regulation configuration, if the IMON1(2) pin voltage is > 97% • $V_{REFIN/OUT}$, this indicates an out-of-max-range fault in the output current regulation. When this condition lasts for 31 consecutive switching cycles, the FS10(8) bit is latched in the fault status register to 1. If the IMON1(2) pin voltage is < 3% • $V_{REFIN/OUT}$, this indicates an out-of-min-range fault in the output current regulation. When this condition lasts for 31 consecutive switching cycles, the FS9(7) bit is latched in the fault status register to 1.

Power Switch Fault Detection and Report

The LT8204 monitors the SW1(2) pin to detect any short or open fault in the external power switches, regardless of the direction of the inductor current flow.

When the LT8204 commands switch MT1(2) to turn on, it monitors SW1(2) pin voltage versus V_{IN} pin voltage. If V_{SW1} is > V_{IN} + 1V or < V_{IN} – 1.5V, this indicates either a short or open fault in the switches MT1 and MB1. When this condition lasts for seven consecutive switching cycles, the LT8204 latches the FS12 bit in the fault status register to 1. If V_{SW2} is > V_{IN} + 1V or < V_{IN} – 1.5V, this indicates either a short or open fault in the switches MT2 and MB2. When this condition lasts for seven consecutive switching cycles, the FS11 bit is latched in the fault status register to 1.

When the LT8204 commands switch MB1(2) to turn on, it monitors SW1(2) pin voltage versus GND pin voltage. If V_{SW1} is >1.5V or < –1V, it indicates either a short or open

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fault in the switches MT1 and MB1. When this condition lasts for seven consecutive switching cycles, the FS12 bit is latched in the fault status register to 1. If V_{SW2} is > 1.5V or < – 1V, this indicates either a short or open fault in the switches MT2 and MB2. When this condition lasts for seven consecutive switching cycles, the FS11 bit is latched in the fault status register to 1.

IMON Pin Short Detection and Report

The LT8204 monitors the IMON1(2) pin to detect any short pin fault.

If the LT8204 detects the IMON pin current $I_{IMON1(2)}$ is >1.75mA, this indicates a short fault in the IMON1(2) pin. When this condition lasts for 31 consecutive switching cycles, the FS5(4) bit is latched in the fault status register to 1.

In case the IMON1(2) pin is shorted or a resistor with a low resistance value is connected between the IMON pin and the ground, the LT8204 reports the fault in the fault status register and also limits the IMON1(2) pin current at 2mA (typical).

RT Pin Fault Detection and Report

The LT8204 monitors the RT pin to detect any short or open pin fault.

If the LT8204 detects the current out of the RT pin, I_{RT} is > 221.5625µA or < 2.8125µA, i.e., R_T < 4.4kΩ or > 356kΩ, this indicates either a short or open fault in the RT pin connection. In this condition, the FS6 bit is latched in the fault status register to 1.

If the RT pin is floated or disconnected from the R_T resistor at any time (i.e., an open fault), the LT8204 will default the RT switching frequency to 30kHz. Similarly, if the RT pin is shorted to the ground, it will default to 1.4MHz. If the RT pin connection has a fault when the frequency synchronization is used with an external clock on the SYNC/SPRD pin, the LT8204 will still operate with a switching frequency based on the synchronized clock on the SYNC/SPRD pin and also reports the fault in the fault status register.

Load Short Fault Detection and Report

The LT8204 monitors the CSN1 and CSN2 pins to detect any short fault in the load.

In the full-bridge configuration, when the internal DAC1 output voltage is set to be < $V_{REFIN/OUT}$/2 – 150mV or >$V_{REFIN/OUT}$/2 + 150mV, if the VMON pin voltage is between $V_{REFIN/OUT}$/2 – 20mV and $V_{REFIN/OUT}$/2 + 20mV, this indicates a short fault in the load. When this condition lasts for 31 consecutive switching cycles, the FS3 bit is latched in the fault status register to 1.

In the dual half-bridge output current regulation configuration, when the internal DAC1(2) output voltage is set to be >$V_{REFIN/OUT}$/2 + 150mV, if the CSN1(2) pin voltage is < 400mV in Load-to-GND configuration or > V_{IN} – 400mV in Load-to-V_{IN} configuration, this indicates a short fault in the load. When this condition lasts for 31 consecutive switching cycles, the FS3 bit is latched in the fault status register to 1.

APPLICATIONS INFORMATION

The front page shows a typical LT8204 application circuit. This Applications Information section serves as a guideline of selecting external components for typical applications.

SHUTDOWN AND PROGRAMMING UNDERVOLTAGE LOCKOUT

The LT8204 has an accurate 1.2V shutdown threshold at the EN/UVLO pin. This threshold can be used in conjunction with a resistor divider from the system input supply to define an accurate undervoltage lockout (UVLO) threshold for the system (Figure 14). An internal hysteresis voltage (25mV) and current (2µA) at the EN/UVLO pin allow programming of the hysteresis voltage for this UVLO threshold. Calculation of the turn on/off thresholds for a system input supply using the LT8204 EN/UVLO pin is as follows:

$$V_{SUPPLY\ OFF} = 1.2V \bullet \left(1 + \frac{R1}{R2}\right)$$

$$V_{SUPPLY\ ON} = 1.225V \bullet \left(1 + \frac{R1}{R2}\right) + (2\mu A \bullet R1)$$

An open-drain transistor can be added to the resistor divider network at the EN/UVLO pin to independently control the turn-off of the LT8204.

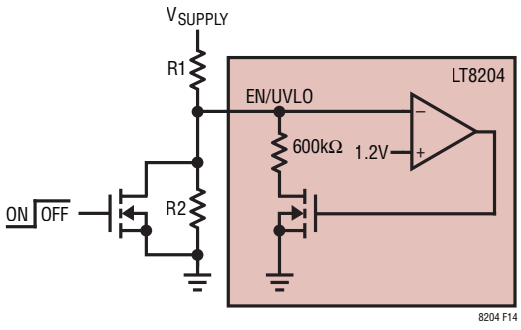

Figure 14. Programming Undervoltage Lockout with Hysteresis

$INTV_{CC}$ REGULATOR BYPASSING AND OPERATION

The $INTV_{CC}$ pin is the output of an internal linear regulator driven from V_{IN} and is the supply for the internal control circuits. The $INTV_{CC}$ pin should be bypassed with a 6.3V or higher rated 2.2µF low ESR, X7R or X5R ceramic capacitor to ensure stability. The $INTV_{CC}$ regulator has an undervoltage lockout that shuts down the internal control circuits until $INTV_{CC}$ reaches 4.95V and maintains circuit operation until $INTV_{CC}$ falls below 4.80V.

The $INTV_{CC}$ regulator can be used for MODE1 and MODE2 pin connections, SYNC/SPRD pin connection and supply for the pull-up resistor at the $\overline{ALERT}$ pin. With 1% output voltage accuracy, the $INTV_{CC}$ pin can also be connected to the REFIN/OUT pin for an application that can tolerate 1% reference for the internal DAC. Other than these three applications, the $INTV_{CC}$ regulator is not intended to supply other external circuitry.

$GATEV_{CC}$ REGULATOR BYPASSING AND OPERATION

The $GATEV_{CC}$ pin is the output of an internal linear regulator driven from V_{IN} and is the supply for the internal gate driver. The $GATEV_{CC}$ pin should be bypassed with a 6.3V or higher rated 4.7µF low ESR, X7R, or X5R ceramic capacitor to ensure stability and provide charge for the gate driver. The $GATEV_{CC}$ regulator has an undervoltage lockout that prevents gate driver switching until $GATEV_{CC}$ reaches 4.65V and maintains switching until $GATEV_{CC}$ falls below 4.4V.

The $GATEV_{CC}$ regulator is intended only to supply the internal gate driver, including the low side gate driver for power switches MB1 and MB2, and the high side gate driver for power switches MT1 and MT2, through the external Schottky diodes connected between the $GATEV_{CC}$ pin and BST1/BST2 pin.

MODE1 AND MODE2 PIN CONNECTION

The LT8204 configures the system architecture based on the MODE1 and MODE2 pin connections, as shown in Table 1. Connect the MODE1 and MODE2 pins to the $INTV_{CC}$ pin to set as high; connect to the GND pin to set as low; and float the pin to set as float.

To set the MODE1 and MODE2 pin connections, the EN/UVLO pin voltage should be below its shutdown threshold (0.3V minimum). When the EN/UVLO pin is above its shutdown threshold (1V maximum) and then the $INTV_{CC}$ pin voltage is charged above its rising UVLO threshold (4.95V typical), the LT8204 latches the system configuration based on the MODE1 and MODE2 pin connections.

APPLICATIONS INFORMATION

PWM CONTROL METHOD SELECTION

The LT8204 features two PWM control methods: voltage mode control and peak current mode control. Choose the voltage mode control for applications with an inductive load and the peak current mode control for applications with a resistive load or a capacitive load.

SWITCHING FREQUENCY SELECTION

The LT8204 uses a constant frequency control scheme between 100kHz and 1MHz. The selection of the switching frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductor and capacitor values. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. For low power applications, consider operating at higher frequencies to minimize the total solution size. In addition, the specific application also plays an important role in switching frequency selection. In a noise-sensitive system, the switching frequency is usually selected to keep the switching noise out of a sensitive frequency band.

SWITCHING FREQUENCY SETTING

The switching frequency of the LT8204 can be set by the internal oscillator. With the SYNC/SPRD pin pulled to the ground, the switching frequency is set by a resistor from the RT pin to the ground. Table 12 shows R_T resistor values for common switching frequencies.

SPREAD SPECTRUM FREQUENCY MODULATION

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve the EMI performance, the LT8204 implements a triangle spread spectrum frequency modulation scheme. With the SYNC/SPRD pin tied to $INTV_{CC}$, the LT8204 starts to spread its switching frequency 23% above the internal oscillator frequency. Figure 15 demonstrates the noise spectrum comparison of the front page application between spread spectrum frequency modulation enabled and disabled. Figure 16 shows the switching waveforms with the spread spectrum feature enabled.

Table 12. Switching Frequency vs R_T Value (1% Resistor)

f_{OSC} (kHz)	R_T (k)
100	90.9
200	36.5
300	22.6
400	16.5
500	13.0
600	10.7
700	9.09
800	7.87
900	6.81
1000	6.19

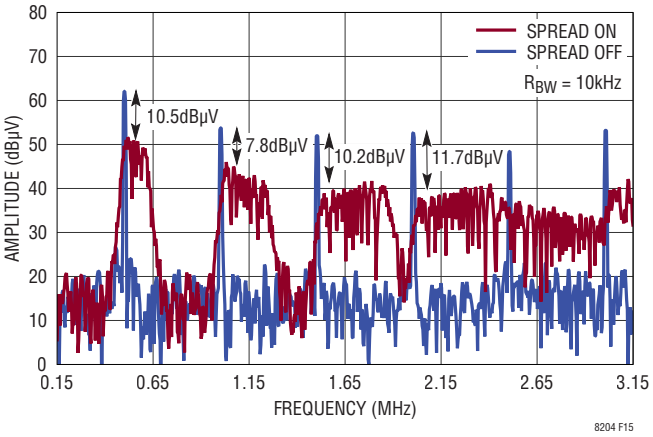

Figure 15. Conducted Average EMI Comparison (AM Band) Example

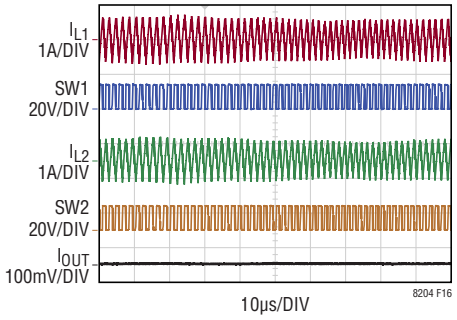

Figure 16. Switching Waveforms with Spread Spectrum Feature

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FREQUENCY SYNCHRONIZATION

The LT8204 switching frequency can be synchronized to an external clock using the SYNC/SPRD pin. Driving the SYNC/SPRD pin with a 50% duty cycle waveform is always a good choice; otherwise, maintain the duty cycle between 10% and 90%. Due to the use of a phase-locked loop (PLL) inside, there is no restriction between the synchronization frequency and the internal oscillator frequency set by the RT pin.

The rising edge of the synchronization clock represents the beginning of a switching cycle. In the full-bridge configuration, switches MT1 and MB2 are turned on at the beginning of a switching cycle. In the dual half-bridge configuration, switch MT1 is turned on at the beginning of a switching cycle, while switch MT2 is turned on after a 180° phase delay from the beginning of a switching cycle.

MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LT8204 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit, and care should be taken to ensure that:

$$t_{ON(MIN)} > \frac{\frac{V_{CSN1} - V_{CSN2}}{V_{IN}} + 1}{2 \bullet f_{SW}} \text{ for Single H-Bridge;}$$

$$t_{ON(MIN)} > \frac{V_{CSN1(2)}}{V_{IN} \bullet f_{SW}} \text{ in Dual Half-Bridge}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase. The minimum on-time for the LT8204 is approximately 150ns. However, as the peak sense voltage for the inductor current decreases, the minimum on-time gradually increases up to about 200ns.

INDUCTOR CURRENT LIMIT PROGRAMMING

The SS9 bit, LOW_ILIM, in the system setup register is used to set the maximum inductor current limit of the controller. When SS9 = 1, the maximum inductor current limit threshold of the current comparator is programmed to be 25mV. When SS9 = 0, the maximum inductor current limit threshold is 75mV.

In the full-bridge configuration, the maximum inductor current limit threshold is 75mV or 25mV for both directions, i.e., ±75mV or ±25mV across the CSP1(2) and CSN1(2) pins. In the dual half-bridge configuration, if it is the output current regulation with Load-to-V_{IN}, the maximum inductor current limit threshold is 25mV or 8.33mV for positive direction and –75mV or –25mV for negative direction across the CSP1(2) and CSN1(2) pins; for other output regulation types in the dual half-bridge configuration, the maximum inductor current limit threshold is 75mV or 25mV for positive direction, and –22mV or –7.33mV in CCM Mode with SS7 = 1 and 5mV or 1.67mV in DCM Mode with SS7 = 0 for negative direction across the CSP1(2) and CSN1(2) pins. Table 13 summarizes the inductor current limit in different system configurations.

Table 13. Inductor Current Limit in Different System Configurations

CONFIGURATION		POSITIVE LIMIT		NEGATIVE LIMIT	
		SS9 = 1	SS9 = 0	SS9 = 1	SS9 = 0
H-Bridge		25mV	75mV	–25mV	–75mV
Half-Bridge, Output Current Regulation with Load-to-V_{IN}		8.33mV	25mV	–25mV	–75mV
Half-Bridge, Other Configurations	SS7 = 0	25mV	75mV	–7.33mV	–22mV
	SS7 = 1	25mV	75mV	1.67mV	5mV

CSP AND CSN PINS

The CSP1(2) and CSN1(2) pins are the inputs to the current comparators. Always tie the CSP1(2) pin to the LC filter side and the CSN1(2) pin to the load side. The common mode input voltage range of the current comparators is 0V to 40V. The CSP1(2) pin is a high impedance input with small bias currents of less than 1µA. When the CSP1(2) pin ramps up from 0V to 2.9V, the small bias current flows out of the CSP1(2) pin. When the CSP1(2) pin ramps down from 40V to 2.5V, the small bias current flows into the CSP1(2) pin. The high impedance on the CSP1(2) input to the current comparator allows accurate DCR sensing. However, care must be taken not to float these pins during a normal operation.

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LOW VALUE RESISTORS INDUCTOR CURRENT SENSING

A typical sensing circuit using a discrete resistor is shown in Figure 17. R_{CS} is chosen based on the required output current.

The current comparator has a maximum threshold, V_{MAX}, determined by the SS9 bit state. The current comparator threshold sets the maximum peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the maximum peak value less half the peak-to-peak ripple current, ΔI_L. Allowing a margin of 20% for variations in the IC and external component values yields:

$$R_{CS} = 0.8 \bullet \frac{V_{MAX}}{I_{MAX} + \Delta I_L / 2}$$

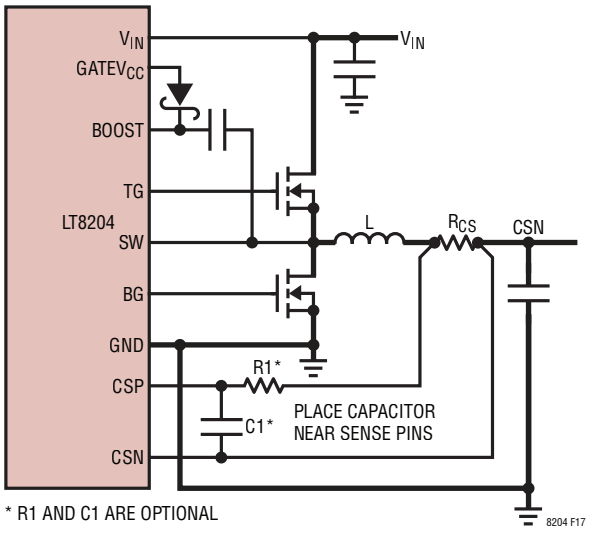

Figure 17. Using a Resistor to Sense Current with the LT8204

INDUCTOR DCR SENSING

For applications requiring the highest possible efficiency, the LT8204 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 18. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. If the external R1||R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the voltage drop across the inductor DCR multiplied by R2/(R1 + R2). Therefore, R2 may be used to scale the voltage across the sense terminals when the DCR is greater than the target sense resistance. Check the manufacturer's data sheet for specifications regarding the inductor DCR in order to properly dimension the external filter components. The DCR of the inductor can also be measured using a good RLC meter.

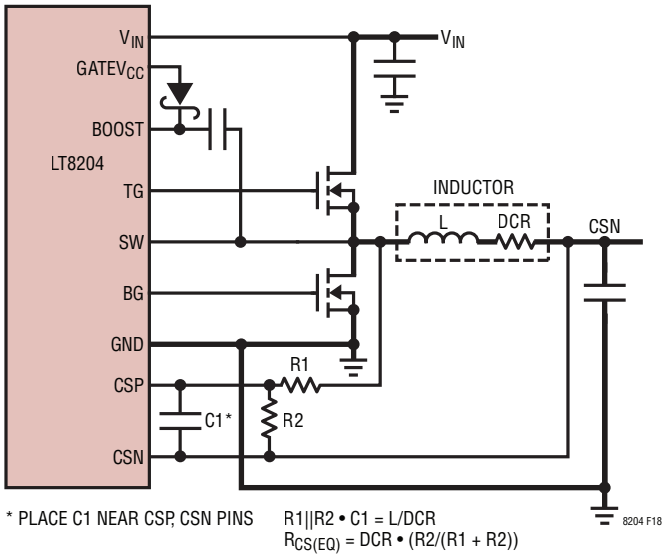

Figure 18. Using the Inductor DCR to Sense Current with the LT8204

SLOPE COMPENSATION AND INDUCTOR PEAK CURRENT

In the PWM peak current mode control method, slope compensation provides stability in constant-frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, this results in a reduction of the maximum inductor peak current for duty cycles higher than 40%. However, the LT8204 uses a novel scheme that allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

INDUCTOR SELECTION

The switching frequency and inductor selection are interrelated in that higher switching frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on the ripple current. The highest inductor current ripple happens at $V_{IN(MAX)}$. For both PWM voltage mode control and peak current mode

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control methods, and for any given ripple allowance set by customers, the minimum inductance can be calculated as:

$$L > \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{f_{SW} \bullet I_{OUT(MAX)} \bullet \Delta I_L\% \bullet V_{IN(MAX)}}$$

where:

f_{SW} is switching frequency

$\Delta I_L\%$ is allowable inductor current ripple $\Delta I_L/I_{OUT(MAX)}$

$V_{IN(MAX)}$ is maximum input voltage

V_{OUT} is output voltage on CSN1(2) pin

I_{OUT} is maximum output current

For the PWM peak current mode control method, the inductor also needs to satisfy the following requirement due to the slope compensation used. Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at certain duty cycles. The minimum inductance required for stability can be calculated as:

$$L > \frac{380 \bullet R_{CS}}{f_{SW}}$$

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

INDUCTOR CORE SELECTION

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. The actual core loss is independent of the core size for a fixed inductor value, but it is very dependent on the inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire, and therefore, copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

POWER MOSFET SELECTION

The LT8204 requires four external N-channel power MOSFETs: two for the top switches (switches MT1 and MT2) and two for the bottom switches (switches MB1 and MB2). The gate drive voltage is set by the 5.3V $GATEV_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LT8204 applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well.

Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage, and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis, while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Top Switch Turn-On Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Bottom Switch Turn-On Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

where V_{OUT} is the voltage at the CSN1 and CSN2 pins. For top switch MT1 and bottom switch MB1, V_{OUT} is the voltage at the CSN1 pin; for top switch MT2 and bottom switch MB2, V_{OUT} is the voltage at the CSN2 pin.

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The power dissipation due to I^2R losses at maximum output current is given by:

$$P_{TOP-I^2R} = \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

$$P_{BOT-I^2R} = \frac{V_{IN}-V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

where ρ_T is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically 0.4%/°C as shown in Figure 19. For a maximum junction temperature of 125°C, using a value of $\rho_T = 1.5$ is reasonable. $I_{OUT(MAX)}$ is the maximum absolute value of the output current.

Besides the I^2R losses, both top and bottom MOSFETs have transition losses based on the direction of the inductor current. For the top MOSFETs, when the inductor current flows from the SW pin to the inductor, the transition loss at maximum positive output current is given by:

$$P_{TOP-TRAN} = V_{IN}^2 \bullet \frac{I_{OUT(POS-MAX)}}{2} \bullet R_{DR} \bullet C_{MILLER} \bullet \left[\frac{1}{V_{GATEVCC}-V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right] \bullet f_{SW}$$

where $I_{OUT(POS-MAX)}$ is the maximum positive output current, R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. $V_{TH(MIN)}$ is the typical MOSFET minimum threshold voltage.

For the bottom MOSFETs, when the inductor current flows from the inductor to the SW pin, the transition loss at maximum negative output current is given by:

$$P_{TOP-TRAN} = V_{IN}^2 \bullet \frac{I_{OUT(NEG-MAX)}}{2} \bullet R_{DR} \bullet C_{MILLER} \bullet \left[\frac{1}{V_{GATEVCC}-V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right] \bullet f_{SW}$$

where $I_{OUT(POS-MAX)}$ is the maximum positive output current.

The transition losses are highest at high input voltages. For V_{IN} < 20V, the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

The junction-to-ambient thermal resistance $R_{TH(JA)}$ includes the junction-to-case thermal resistance $R_{TH(JC)}$ and the case-to-ambient thermal resistance $R_{TH(CA)}$. This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

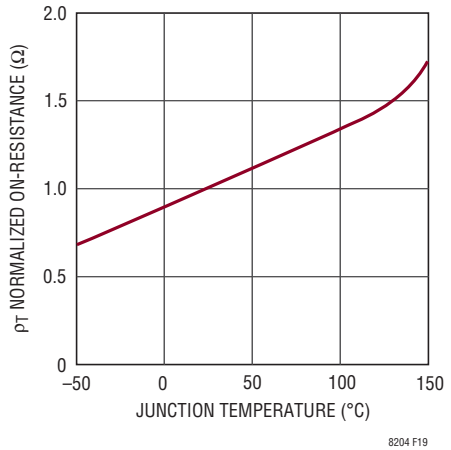

Figure 19. Normalized $R_{DS(ON)}$ vs Temperature

POWER MOSFET GATE RESISTORS

In some cases, it can be beneficial to add 1Ω to 10Ω of resistance between some of the NMOS gate pins and their respective gate driver pins on the LT8204 (i.e., TG1, BG1, TG2, BG2). Due to parasitic inductance and capacitance, ringing can occur on SW1 or SW2 when low capacitance MOSFETs are turned on/off too quickly. The ringing can be of greatest concern when operating the MOSFETs for the LT8204 near the rated voltage limits. Additional gate resistance slows the switching speed, minimizing the ringing.

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Excessive gate resistance can have two negative side effects on performance:

1. Slowing the switch transition times can also increase power dissipation in the switch.
2. Capacitive coupling from the SW1 or SW2 pin to the switch gate node can turn it on when it's supposed to be off, thus increasing power dissipation. With too much gate resistance, this would most commonly happen to the MB1(2) switch when SW1(2) is rising.

Careful board evaluation should be performed when optimizing the gate resistance values. SW1 and SW2 pin ringing can be affected by the inductor current levels. Therefore, board evaluation should include measurements at a wide range of load currents. When performing PCB measurements of the SW1 and SW2 pins, be sure to use a very short ground post from the PCB ground to the scope probe ground sleeve in order to minimize false inductive voltages readings.

OPTIONAL SCHOTTKY DIODE (D_{T1}, D_{B1}, D_{T2}, D_{B2}) SELECTION

The optional Schottky diodes D_{T1} (in parallel with switch MT1), D_{B1} (in parallel with switch MB1), D_{T2} (in parallel with switch MT1), and D_{B2} (in parallel with switch MB1) conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of switches MT1, MB1, MT2, and MB2 from turning on and storing charge during the dead time. In particular, D_{T1} significantly reduces the reverse recovery current between the switch MT1 turnoff and switch MB1 turn-on, D_{B1} significantly reduces the reverse recovery current between the switch MB1 turnoff and switch MT1 turn-on, D_{T2} significantly reduces the reverse recovery current between the switch MT2 turnoff and switch MB2 turn-on, and D_{B2} significantly reduces the reverse recovery current between the switch MB2 turnoff and switch MT2 turn-on. They improve converter efficiency and reduce switch voltage stress. In order for the diode to be effective, the inductance between it and the switch must be as small as possible, mandating that these components be placed adjacently.

TOP GATE MOSFET DRIVER SUPPLY (C_{BST1}, C_{BST2})

The top MOSFET drivers, TG1 and TG2, are driven between their respective SW and BST pin voltages. The boost voltages are biased from floating bootstrap capacitors C_{BST1} and C_{BST2}, which are normally recharged through the external bootstrap diodes when the respective top MOSFET is turned off. Both capacitors are charged to the same voltage as the $GATEV_{CC}$ voltage. The bootstrap capacitors, C_{BST1} and C_{BST2} need to store about 100 times the gate charge required by the top switches, MT1 and MT2. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

OPTIONAL SCHOTTKY DIODE (D_{LT1}, D_{LB1}, D_{LT2}, D_{LB2}) SELECTION

Figure 20 and Figure 21 show the optional Schottky diodes: D_{LT1} between the CSN1 pin and V_{IN}, D_{LB1} between GND and the CSN1 pin, D_{LT2} between the CSN2 pin and V_{IN}, and D_{LB2} between GND and the CSN2 pin. These optional Schottky diodes can be used to prevent the CSN1 and CSN2 pins from going above V_{IN} and below GND, especially when the load is inductive.

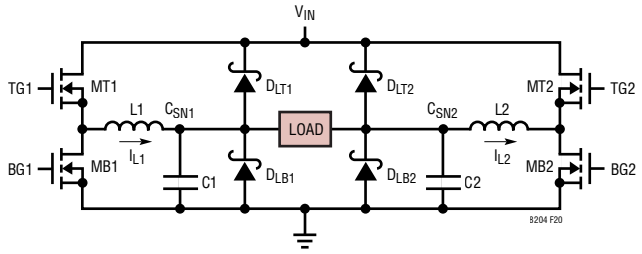

Figure 20. Optional Schottky Diodes (D_{LT1}, D_{LB1}, D_{LT2}, D_{LB2}) in H-Bridge Configuration

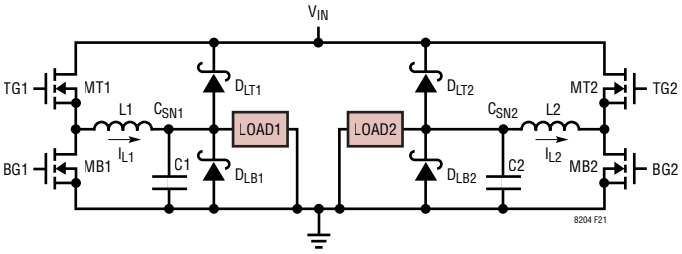

Figure 21. Optional Schottky Diodes (D_{LT1}, D_{LB1}, D_{LT2}, D_{LB2}) in Half-Bridge Configuration

APPLICATIONS INFORMATION

C_{IN} AND C_{OUT} SELECTION

The selection of C_{IN} is usually based off the worst-case RMS input current. The highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula shown in Equation 1 to determine the maximum RMS capacitor current requirement.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \left(\frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2} \quad (1)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there are any questions.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LT8204, is also suggested. A small (≤10Ω) resistor placed between C_{IN} and the V_{IN} pin provides further isolation.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (V_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \bullet \left(ESR + \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} \right)$$

where f_{SW} is the operating frequency, C_{OUT} is the output capacitance, and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

SOFT START-UP AND SOFT SHUTDOWN

As shown in Figure 10 and Figure 11 and explained in the Operation section, the SS pin can be used to program soft start-up and soft shutdown by connecting an external capacitor C_{SS} from the SS pin to the ground. During the soft start-up period, the internal 10µA pull-up current charges up the capacitor, creating a voltage ramp-up on the SS pin. During the soft shutdown period, the internal 10µA pull-down current discharges the capacitor, creating a voltage ramp-down on the SS pin.

H-Bridge: In the UP/V_{OUT} state during the soft start-up, as the SS pin voltage rises linearly from 0.63V to 0.7V + V_{IN}/19, the output voltages, V_{CSN1} and V_{CSN2}, rise smoothly and settle down to $V_{IN}/2$. The output voltage soft start-up time in the UP/V_{OUT} state can be calculated as:

$$t_{SS\text{-}H\text{-}UP/VOUT} = \frac{(V_{IN}/19 + 70mV) \bullet C_{SS}}{10\mu A}$$

After the UP/V_{OUT} state, the LT8204 enters the UP/PRE state, where it transits from individual output voltage regulation to H-bridge operation. The system regulates the output differential voltage $V_{CSN1} - V_{CSN2}$ (output voltage regulation configuration) or the output current (output current regulation configuration) to be zero. The SS pin voltage rises linearly from 0.7V + V_{IN}/19 to 0.7V + V_{IN}/13, creating a time delay to allow the transition to be settled down. The delay time in the UP/PRE state can be calculated as:

$$t_{SS\text{-}H\text{-}UP/PRE} = \frac{(6 \bullet V_{IN}/247) \bullet C_{SS}}{10\mu A}$$

After the UP/PRE state, the LT8204 enters the OK/RUN state and regulates the output differential voltage $V_{CSN1} - V_{CSN2}$ (output voltage regulation configuration) or the output current (output current regulation configuration) based on the internal DAC1 output voltage. The SS pin voltage rises linearly above 0.7V + V_{IN}/13 and finally clamps at around 1V + V_{IN}/11.

In the DN/PRE state during the soft shutdown, the system regulates the output differential voltage $V_{CSN1} - V_{CSN2}$ (output voltage regulation configuration) or the output current (output current regulation configuration) to be

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zero. The SS pin voltage falls linearly from 1V + V_{IN}/11 to 0.7V + V/15, creating a time delay to allow the zero output regulation to be settled down. The delay time in the DN/PRE state can be calculated as:

$$t_{SS-H-DN/PRE} = \frac{(4 \bullet V_{IN}/165 + 300mV) \bullet C_{SS}}{10\mu A}$$

After the DN/PRE state, the output voltages, V_{CSN1} and V_{CSN2}, are at V_{IN}/2. The LT8204 then enters the DN/V_{OUT} state, and the SS pin voltage falls linearly from 0.7V + V_{IN}/15 to 0.7V + V_{IN}/23. The output voltages, V_{CSN1} and V_{CSN2}, fall smoothly and settle down to 0V. The output voltage soft shutdown time in the DN/V_{OUT} state can be calculated as:

$$t_{SS-H-UP/VOUT} = \frac{(8 \bullet V_{IN}/345) \bullet C_{SS}}{10\mu A}$$

Half-Bridge: After the SS pin voltage rises above 0.63V, the LT8204 enters the OK/RUN state. As the SS pin voltage continues to rise linearly above 0.7V, the output voltage (output voltage regulation configuration) or the output current (output current regulation configuration) rises smoothly and settles down to the regulation point based on the internal DACs' output voltage. The soft start-up range is defined to be the voltage from 0V to V_{OUTDAC} (output voltage of the internal DAC). The soft start-up time can be calculated as:

$$t_{SS-HALF-UP} = \frac{V_{DAC} \bullet C_{SS}}{10\mu A}$$

The SS pin voltage is finally clamped at around 1V + 3/5 • $V_{REFIN/OUT}$. During soft shutdown, the LT8204 enters the DN/SS state, and the SS pin voltage falls linearly from 1V + 3/5 • $V_{REFIN/OUT}$ to 0V. The output voltage (output voltage regulation configuration) or the output current (output current regulation configuration) falls smoothly and settles down to zero. The soft shutdown range is defined to be the voltage from 1V + 3/5 • $V_{REFIN/OUT}$ to 0V. The soft shutdown time can be calculated as:

$$t_{SS-HALF-DN} = \frac{(3/5 \bullet V_{REFIN/OUT} + 1V) \bullet C_{SS}}{10\mu A}$$

For both full-bridge and dual half-bridge configurations, choose C_{SS} to be at least five to ten times larger than the compensation capacitor on the V_C pin.

OUTPUT CURRENT MONITORING AND PROGRAMMING

The output current is monitored by placing an appropriate value current sense resistor, R_{SNS}, in series with the load. The voltage drop across R_{SNS} is (Kelvin) sensed by the SNSP and SNSN pins, and it is amplified and buffered to the IMON pin.

With close-loop regulation, the LT8204 regulates the IMON pin voltage to be equal to the output voltage of the internal DAC (see EA1 and EA2 in the Block Diagram). Hence, in the output current regulation configuration, the output current is:

$$I_{OUT} = \frac{V_{DAC} - V_{REFIN/OUT}/2}{50 \bullet R_{SNS}}$$

In the full-bridge output current regulation configuration, the LT8204 regulates I_{OUT1} (from the SNSP1 pin to the SNSN1 pin) to be I_{OUT} (see EA1 in the Block Diagram). The output current regulation can be bidirectional, and so the full range of DAC output voltage can be used.

In the dual half-bridge output current regulation configuration, the LT8204 regulates I_{OUT1} (from the SNSP1 pin to the SNSN1 pin) for the first bridge and I_{OUT2} (from the SNSP2 pin to the SNSN2 pin) for the second bridge, respectively (see EA1 and EA2 in the Block Diagram). The output current regulation in a dual half-bridge is unidirectional, although the full range of DAC output voltage can still be used, which provides capability for calibration to achieve 0A output current regulation in Load-to-GND condition. In Load-to-V_{IN} condition, due to the maximum duty cycle limitation, there is a minimum output current level.

OUTPUT CURRENT SENSE RESISTOR R_{SNS} SELECTION

The external output current sense resistor, R_{SNS}, has a significant effect on the output current monitoring and must be chosen with care. First, the power dissipation in the resistor should be considered. The output current

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will cause both heat and voltage loss in R_{SNS}. As a result, the sense resistor should be as small as possible while still providing the input dynamic range required by the measurement. Note that the input dynamic range is the difference between the maximum input signal and the minimum accurately reproducible signal (which is limited primarily by the input DC offset of the internal IMON amplifier of the LT8204). In addition, R_{SNS} must be small enough that V_{SNS} does not exceed the maximum input voltage specified by the LT8204, even under peak load conditions.

As an example, an application may require that the maximum sense voltage be ±40mV. If this application is expected to draw ±2A at peak load, R_{SNS} should be no more than 20mΩ.

$$V_{SNS(MAX)} = \frac{\left(\frac{17 \bullet V_{REFIN/OUT}}{18} - 1 \bullet LSB - \frac{V_{REFIN/OUT}}{2}\right)}{50} \approx$$

$$\frac{\left(\frac{17 \bullet 4.5V}{18} - \frac{4.5V}{2}\right)}{50} = 40mV$$

$$R_{SNS(MAX)} = \frac{V_{SNS(MAX)}}{I_{OUT(MAX)}} = \frac{40mV}{2A} = 20m\Omega$$

Once the maximum R_{SNS} value is determined, the minimum sense resistor value will be set by the resolution or dynamic range required. The minimum signal that can be accurately represented by the IMON amplifier is limited by the input offset. As an example, the LT8204 has a typical input offset of ±50µV. If the minimum current is ±25mA, a sense resistor of 2mΩ will set V_{SNS} to ±50µV. This is the same value as the input offset. A larger sense resistor will reduce the error due to offset by increasing the sense voltage for a given load current. Choosing a 20mΩ R_{SNS} will maximize the dynamic range and provide a system that has ±40mV across the sense resistor at peak load (±2A), while input offset causes an error equivalent to only ±2.5mA of output current. Peak dissipation in the sense resistor is 80mW in this example. If instead a 2.5mΩ sense resistor is employed, then the effective current error is ±20mA, while the peak sense voltage is reduced to ±5mV at ±2A, dissipating only 10mW.

OUTPUT CURRENT SENSE RESISTOR R_{SNS} CONNECTION

Kelvin connection of the SNSP and SNSN inputs to the sense resistor should be used in all but the lowest power applications. Solder connections and PC board interconnections that carry high current can cause significant error in measurement due to their relatively large resistances. One 10mm × 10mm square trace of one-ounce copper is approximately 0.5mΩ. A 1mV error can be caused by as little as 2A flowing through this small interconnect. This will cause a 1% error in a 100mV signal. A 10A load current in the same interconnect will cause a 5% error for the same 100mV signal. By isolating the sense traces from the high current paths, this error can be reduced by orders of magnitude. A sense resistor with integrated Kelvin sense terminals will give the best results.

Figure 22 to Figure 24 illustrate the required connection methods in different configurations.

OUTPUT CURRENT SENSE ERROR SOURCES

The IMON amplifier in the LT8204 causes output current sense error due to its gain error, input offset voltage, and input bias current.

Gain Error: The IMON amplifier has a fixed voltage gain between the IMON pin voltage and the SNSP and SNSN pins' voltage difference. This fixed voltage gain is 50, with a worst-case error of ±0.4%.

Input Offset Voltage: The DC input offset voltage of the IMON amplifier adds directly to the value of the sense voltage, V_{SNS}. The input offset voltage induced error limits the available dynamic range of the output current sense.

Input Bias Current: When the current sense pins, SNSP and SNSN pins, have a common mode voltage of higher than 2.7V (typical), the bias current I_B^+ flows into the positive input, SNSP, of the IMON amplifier, and I_B^- flows into the negative input, SNSN, of the IMON amplifier. When the common mode voltage is lower than 2.3V (typical), the bias current I_B^+ flows out of the positive input, SNSP, of the IMON amplifier, and I_B^- flows out of the negative input, SNSN, of the IMON amplifier.

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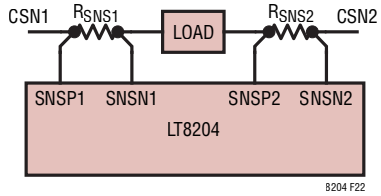

Figure 22. Output Current Sense Resistors Connection in Full-Bridge Configuration

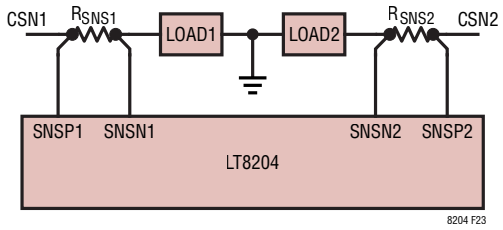

Figure 23. Output Current Sense Resistors Connection in Dual Half-Bridge Configuration with Load-to-GND

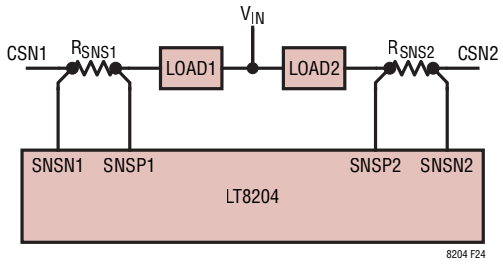

Figure 24. Output Current Sense Resistors Connection in Dual Half-Bridge Configuration with Load-to-V_{IN}

With $I_B^+ \approx I_B^- = I_{BIAS}$, $R_{SNS1} = R_{SNS2} = R_{SNS}$, the IMON amplifier output error in the full-bridge configuration is:

$$E_{IMON1} = 50 \bullet I_{BIAS} \bullet R_{SNS}, E_{IMON2} = -50 \bullet I_{BIAS} \bullet R_{SNS}$$

In the dual half-bridge configuration with Load-to-GND, the IMON amplifier output error is:

$$E_{IMON1} = E_{IMON2} = 50 \bullet I_{BIAS} \bullet R_{SNS}$$

In the dual half-bridge configuration with Load-to-GND, the IMON amplifier output error is:

$$E_{IMON1} = E_{IMON2} = -50 \bullet I_{BIAS} \bullet R_{SNS}$$

The input bias current induced error becomes significant when a large value of the current sense resistor is used. As an example, with a typical bias current I_{BIAS} = 6µA, a current sense resistor R_{SNS} = 1Ω, the IMON output error is 0.3mV.

To eliminate this error, a resistor R_C equal in value to R_{SNS} can be added in series with the SNSP or SNSN pin, based on the system configuration. Figure 25 to Figure 27 illustrate the connection of the R_C resistor.

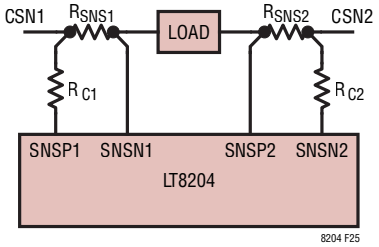

Figure 25. R_C Resistor Connection in Full-Bridge Configuration

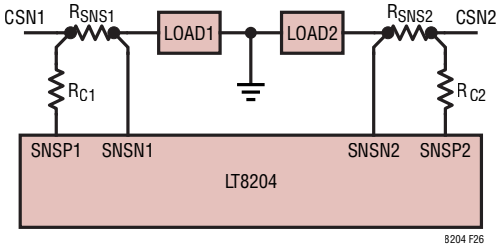

Figure 26. R_C Connection in Dual Half-Bridge Configuration with Load-to-GND

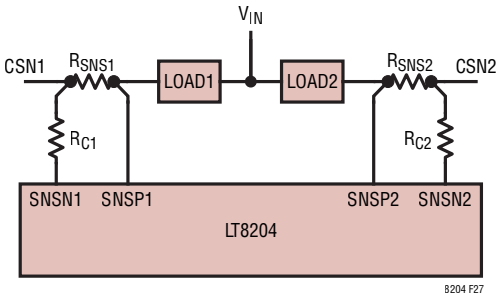

Figure 27. R_C Connection in Dual Half-Bridge Configuration with Load-to-V_{IN}

OUTPUT VOLTAGE MONITORING AND PROGRAMMING

The output voltages, V_{CSN1} and V_{CSN2}, are monitored by internal resistor dividers, and the LT8204 generates internal feedback voltages as V_{FB1} and V_{FB2}:

$$V_{FB1} = \frac{V_{CSN1}}{10},\ V_{FB2} = \frac{V_{CSN2}}{10}$$

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The voltage difference between V_{CSN1} and V_{CSN2} is also monitored in both full-bridge and dual half-bridge configurations. The VMON pin provides an attenuated and buffered monitor of the voltage difference between the V_{CSN1} and V_{CSN2}.

With close-loop regulation, the LT8204 regulates the V_{FB1} and V_{FB2} voltages, or VMON pin voltage to be equal to the output voltage of the internal DAC.

In the full-bridge output voltage regulation configuration, the LT8204 regulates the VMON pin voltage (see EA5 in the block diagram) and hence the voltage difference between the V_{CSN1} and V_{CSN2} as:

$$V_{CSN1} - V_{CSN2} = 20 \bullet (V_{DAC} - V_{REFIN/OUT}/2)$$

The voltage difference regulation can be bidirectional, and so the full range of DAC output voltage can be used. However, the minimum and maximum $V_{CSN1} - V_{CSN2}$ can be regulated is limited by the LT8204 minimum and maximum on-time $t_{ON(MIN)}$ (150ns typical) and off-time $t_{OFF(MIN)}$ (150ns typical) as shown below:

$$(V_{CSN1} - V_{CSN2})_{MAX} = (1 - 2 \bullet t_{OFF(MIN)} \bullet f_{SW}) \bullet V_{IN}$$

$$(V_{CSN1} - V_{CSN2})_{MIN} = (2 \bullet t_{ON(MIN)} \bullet f_{SW} - 1) \bullet V_{IN}$$

In the dual half-bridge configuration, the LT8204 regulates V_{FB1} and hence V_{CSN1} for the first bridge and V_{FB2} and hence V_{CSN2} for the second bridge, respectively (see EA3 and EA4 in the block diagram). The V_{CSN1} and V_{CSN2} are regulated as:

$$V_{CSN1} = 10 \bullet V_{DAC}$$

$$V_{CSN2} = 10 \bullet V_{DAC}$$

The V_{CSN1} and V_{CSN2} regulation in dual half-bridge is unidirectional. However, the straight binary coding scheme is used for the DAC input code, and so the full range of DAC output voltage can be used. However, the minimum and maximum V_{CSN1} and V_{CSN2} can be regulated is limited by the LT8204 minimum and maximum on-time $t_{on(min)}$ (150ns typical) and off-time $t_{off(min)}$ (150ns typical), as shown below:

$$V_{CSN1(MAX)} = V_{CSN2(MAX)} = (1 - t_{OFF(MIN)} \bullet f_{SW}) \bullet V_{IN}$$

$$V_{CSN1(MIN)} = V_{CSN2(MIN)} = t_{ON(MIN)} \bullet f_{SW} \bullet V_{IN}$$

CSN, CSP, SNSP, AND SNSN PINS

The connection of CSN1, CSP1, SNSP1, and SNSN1 pins should make sure the voltage difference between each two of them is less than the ABSMAX rating (±0.3V for LT8204). The connection of CSN2, CSP2, SNSP2, and SNSN2 pins has the same requirement.

LOOP COMPENSATION

The loop stability is affected by a number of factors, including the inductor value, output capacitance, load type (inductive, resistive, or capacitive), load current, V_{IN}, V_{OUT}, and the V_C resistor and capacitors. The LT8204 uses internal transconductance error amplifiers driving V_C to help compensate the control loop. In full-bridge configuration, the compensation networks on V_{C1} and V_{C2} should be the same, while in dual half-bridge configuration, the compensation networks on V_{C1} and V_{C2} can be independent based on the two bridges' different operation conditions.

For applications with resistive or capacitive loads, the peak current mode PWM control method should be selected. Then, for most applications, a 3.3nF series capacitor at V_C is a good value. The parallel capacitor (from V_C to GND) is typically 1/10th the value of the series capacitor to filter high frequency noise. A larger V_C series capacitor value may be necessary if the output capacitance is reduced. A good starting value for the V_C series resistor is 20kΩ. Lower resistance will improve stability but will slow the loop response. Use a trim pot instead of a fixed resistor for initial bench evaluation to determine the optimum value.

For applications with inductive loads, the voltage mode PWM control method should be selected. With voltage mode control, there are three poles in the power stage. The load contributes one pole based on its inductance L_{LOAD} and equivalent series resistance R_{LOAD} at the frequency of:

$$f_{P-LOAD} = \frac{R_{LOAD}}{2\pi \bullet L_{LOAD}}$$

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The output LC filter, i.e., the inductor L and the output capacitor C_{OUT}, also contributes double poles at the frequency of:

$$f_{P-LC} = \frac{1}{2\pi \bullet \sqrt{L \bullet C_{OUT}}}$$

The selection of the series capacitor, C_C, at V_C should be able to achieve a system bandwidth less than 1/10th of f_{P-LC}, which yields:

$$C_C > \frac{10 \bullet g_m}{f_{P-LC}}$$

where g_m is the transconductance (typical 1.2mS) of the error amplifiers (EA1 through EA5 in the block diagram).

The selection of the series capacitor, R_C, at V_C should be able to achieve a zero location around 10 • f_{P-LOAD}, which yields:

$$R_C \approx \frac{1}{2\pi \bullet C_C \bullet 10 \bullet f_{LOAD}}$$

DAC OUTPUT RANGE

Both DACs inside the LT8204 have an output voltage range from 1/18 • $V_{REFIN/OUT}$ to (17/18 • $V_{REFIN/OUT}$ – 1 • LSB). In order to achieve the maximum output of (17/18 • $V_{REFIN/OUT}$ – 1 • LSB), the V_{IN} voltage needs to be 3V above $V_{REFIN/OUT}$. Otherwise, the DAC maximum output voltage is limited at V_{IN} – 3V.

REFIN/OUT VOLTAGE REFERENCE CONSIDERATIONS

Selecting a precision voltage reference on the REFIN/OUT pin for use with the LT8204 is critical to the performance of the system. The output voltage of the LT8204 on-chip DAC is directly affected by the voltage reference. Therefore, any voltage reference error will appear as a DAC output voltage error.

There are three primary error sources to consider when selecting a precision voltage reference for 16-bit applications: output voltage initial tolerance, output voltage temperature coefficient, and output voltage noise.

Initial reference output voltage tolerance, if uncorrected, generates a full-scale error term. Choosing a reference with a low output voltage initial tolerance, like the LT1236 (±0.05%), minimizes the gain error caused by the reference.

A reference's output voltage temperature coefficient affects not only the full-scale error, but can also affect the circuit's INL and DNL performance. If a reference is chosen with a loose output voltage temperature coefficient, then the DAC output voltage along its transfer characteristic will be very dependent on ambient conditions. Minimizing the error due to the reference temperature coefficient can be achieved by choosing a precision reference with a low output voltage temperature coefficient and/or tightly controlling the ambient temperature of the circuit to minimize temperature gradients.

As precision DAC applications move to 16-bit performance, reference output voltage noise may contribute a dominant share of the system's noise floor. This, in turn, can degrade the system's dynamic range and signal-to-noise ratio. Care should be exercised in selecting a voltage reference with as low an output noise voltage as practical for the system resolution desired. Precision voltage references like the LT1236 or LTC6655 produce low output noise in the 0.1Hz to 10Hz region, well below the 16-bit LSB level.

Table 14 is a partial list of LTC precision references recommended for use with the LT8204 with relevant specifications.

Table 14. Partial List of LTC Precision References Recommended for Use with the LT8204 with Relevant Specifications

REFERENCE	INITIAL TOLERANCE	TEMPERATURE DRIFT	0.1Hz TO 10Hz NOISE
LT1019A-2.5 LT1019A-5	±0.05% Max	5ppm/°C Max	$12\mu V_{P-P}$
LT1236A-5	±0.05% Max	5ppm/°C Max	$3\mu V_{P-P}$
LT1460A-2.5 LT1460A-5	±0.075% Max	10ppm/°C Max	$20\mu V_{P-P}$
LT1790A-2.5 LT1790A-5	±0.05% Max	10ppm/°C Max	$12\mu V_{P-P}$
LTC6652A-2.5 LTC6652A-5	±0.05% Max	5ppm/°C Max	$2.8ppm_{P-P}$
LTC6655A-2.5 LTC6655A-5	±0.025% Max	2ppm/°C Max	$0.25ppm_{P-P}$
LT6657A-2.5 LT6657A-5	±0.1% Max	1.5ppm/°C Max	$0.5ppm_{P-P}$

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For applications requiring less precision of the DAC reference, the three options that the LT8204 provides can be considered: $INTV_{CC}$ LDO output voltage (tie $INTV_{CC}$ pin to REFIN/OUT pin and set SS12 bit in the system setup register to 0), internal 2.048V REFIN/OUT output voltage (set SS12–SS11 bits in the system setup register to 11), internal 4.096V REFIN/OUT output voltage (set SS12 to SS11 bits in the system setup register to 10). The specifications of these three reference options are summarized in Table 15.

Table 15. LT8204 Reference Specifications

REFERENCE	INITIAL TOLERANCE	TEMPERATURE DRIFT	0.1Hz TO 10Hz NOISE
$INTV_{CC}$	±0.5% Max	50ppm/°C Max	$15\mu V_{P-P}$
2.048V REFIN/OUT	±0.5% Max	20ppm/°C Max	$10\mu V_{P-P}$
4.096V REFIN/OUT	±0.5% Max	40ppm/°C Max	$15\mu V_{P-P}$

$\overline{ALERT}$ PIN

The LT8204 provides an open-drain status pin, $\overline{ALERT}$, which is pulled low during fault conditions. Connect a pull-up resistor at the $\overline{ALERT}$ pin, and select a resistance value to make sure the current flowing into the pin does not exceed 1mA when pulled low.

To summarize, the following conditions pull the $\overline{ALERT}$ pin low:

1. The LT8204 powers up and is ready to start SPI transaction, and the system setup register needs to be programed (see Power-Up Sequence section);
2. The LT8204 has a SPI transaction error (see SPI Transaction Acknowledgement section);
3. The LT8204 has a system operational fault condition (see $\overline{ALERT}$MASK Register and Fault Status Register sections).

EFFICIENCY CONSIDERATIONS

The power efficiency of a switching regulator is equal to the output power divided by the input power times 100%.

It is often useful to analyze individual losses to determine what is limiting efficiency and which change would produce the most improvement. Although all dissipative elements in circuits produce losses, four main sources account for most of the losses in LT8204 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.
2. Transition loss. This loss arises from the brief amount of time switches MT1, MB1, MT2, and MB2 spend in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors.
3. $INTV_{CC}$ current. This is the internal control circuitry currents.
4. $GATEV_{CC}$ current. This is the quad MOSFET drivers' currents.
5. C_{IN} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. C_{IN} is required to have a low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.
6. Other losses. Schottky diodes D_{T1}, D_{B1}, D_{T2}, and D_{B2} are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominately at light loads. Switches MT1 and MT2 cause reverse recovery current loss when the inductor current flows from the SW pin to the inductor, and switches MB1 and MB2 cause reverse recovery current loss when the inductor current flows from the inductor to the SW pin.

When making adjustments to improve efficiency, the input current is the best indicator of the changes of efficiency. If a change is made and the input current decreases, then the efficiency has increased. If there is no change in the input current, then there is no change in efficiency.

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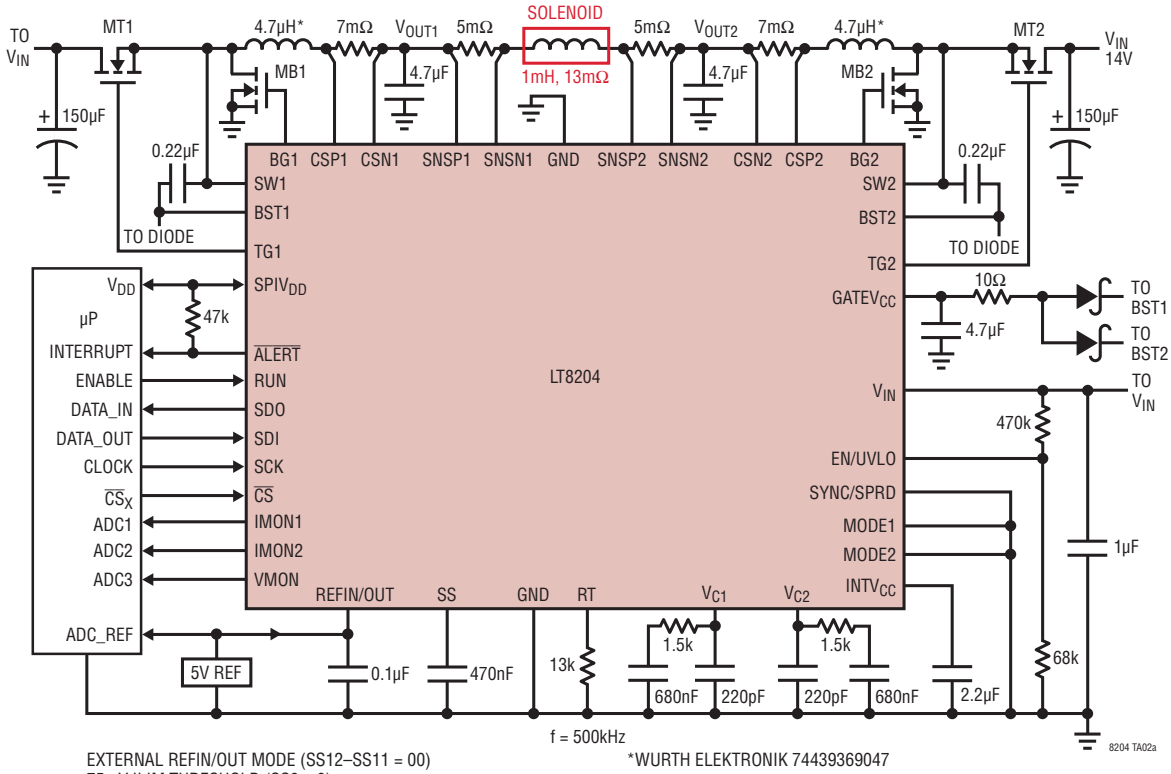
PC BOARD LAYOUT CHECKLIST

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

- The ground plane layer should not have any traces, and it should be as close as possible to the layer with power MOSFETs.
- Use immediate vias to connect the components to the ground plane. Use several large vias for each power component.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or GND).
- Separate the signal and power grounds. All small signal components should return to the exposed GND pad from the bottom, which is then tied to the power GND close to the sources of power switches MB1 and MB2.
- Place switches MT1 and MT2 as close to the controller as possible, keeping the power GND, BG, and SW traces short.
- Keep the high dV/dT SW1, SW2, BST1, BST2, TG1, and TG2 nodes away from sensitive small-signal nodes.
- The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor.
- Connect the top driver bootstrap capacitor C_{BST1} closely to the BST1 and SW1 pins. Connect the top driver bootstrap capacitor C_{BST2} closely to the BST2 and SW2 pins.
- Connect the input capacitors C_{IN} closely to the power switches MT1 and MT2. These capacitors carry the MOSFET AC current.
- Route SNSP and SNSN traces together with minimum PCB trace spacing. Avoid sense lines that pass through noisy areas, such as switch nodes. The filter capacitor between the SNSP and SNSN pins should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the R_{SNS} resistor. A low ESL sense resistor is recommended.
- Route CSP and CSN traces together with minimum PCB trace spacing. Avoid sense lines that pass through noisy areas, such as switch nodes. The filter capacitor between the CSP and CSN pins should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the R_{CS} resistor. A low ESL sense resistor is recommended.
- Connect the V_C pin compensation network close to the IC, between V_C and the signal ground. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ bypass capacitor, C_{INTVCC}, close to the IC, between the $INTV_{CC}$ and the signal ground.
- Connect the $GATEV_{CC}$ bypass capacitor, $C_{GATEVCC}$, close to the IC, between the $GATEV_{CC}$ and the power ground. This capacitor carries the gate drivers' current peaks.

TYPICAL APPLICATIONS

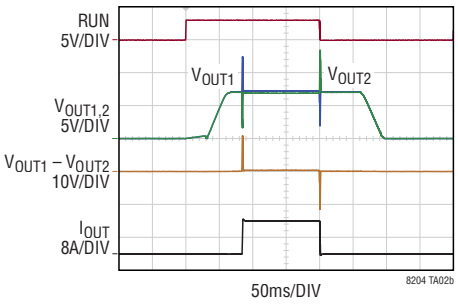
14V, ±8A Solenoid Driver



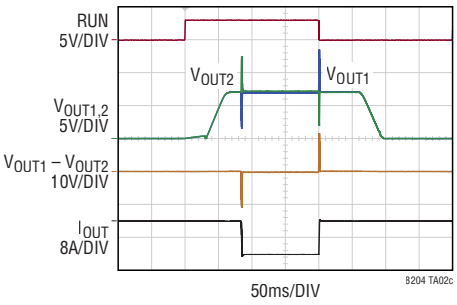
EXTERNAL REFIN/OUT MODE (SS12–SS11 = 00)
75mV ILIM THRESHOLD (SS9 = 0)
WITH SOFT SHUTDOWN CONTROL AND HOLD MODE (SS5–SS4 = 01)

*WURTH ELEKTRONIK 74439369047

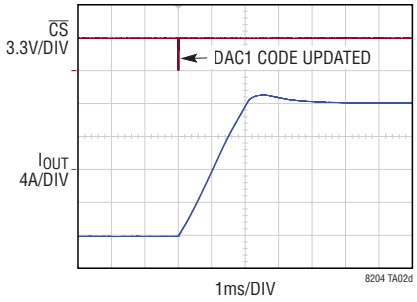
Soft Start Up and Shutdown with I_{OUT} = 8A



Soft Start Up and Shutdown with I_{OUT} = –8A

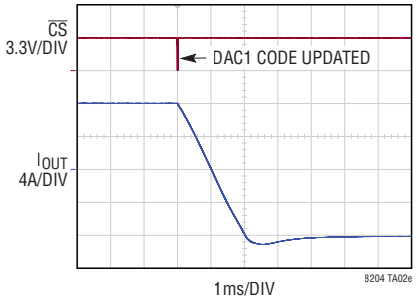


I_{OUT} Commanded to Step Up



I_{OUT} STEPS UP FROM –8A TO 8A

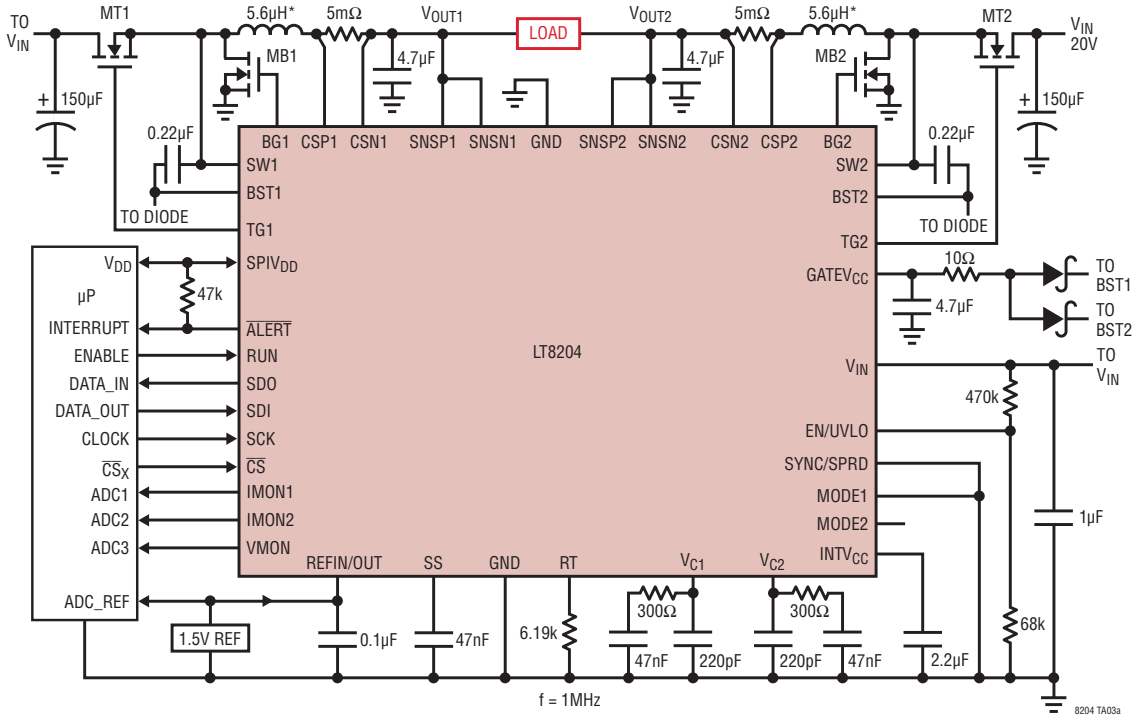
I_{OUT} Commanded to Step Down



I_{OUT} STEPS DOWN FROM 8A TO –8A

TYPICAL APPLICATIONS

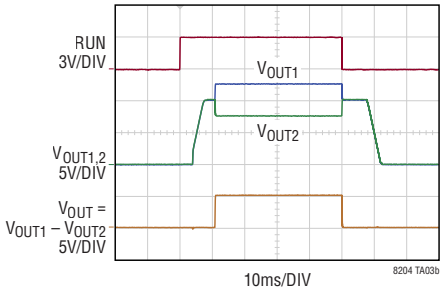
20V V_{IN} Bipolar –12V to 12V Output Range Voltage Source



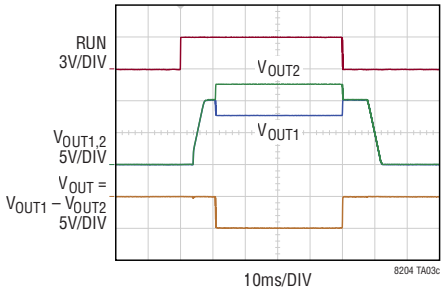
EXTERNAL REFIN/OUT MODE (SS12–SS11 = 00)
75mV ILIM THRESHOLD (SS9 = 0)
WITH SOFT SHUTDOWN CONTROL AND HOLD MODE (SS5–SS4 = 01)

*WURTH ELEKTRONIK 7443556560

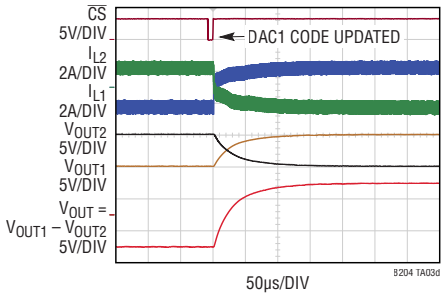
Soft Start Up and Shutdown for V_{OUT} = 5V



Soft Start Up and Shutdown for V_{OUT} = –5V

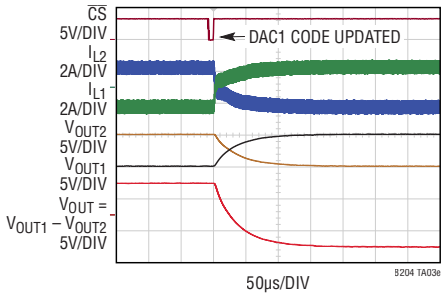


V_{OUT} Commanded to Step Up



$V_{OUT} = V_{OUT1} – V_{OUT2}$ STEPS UP
FROM –5V TO 5V
LOAD = 4Ω

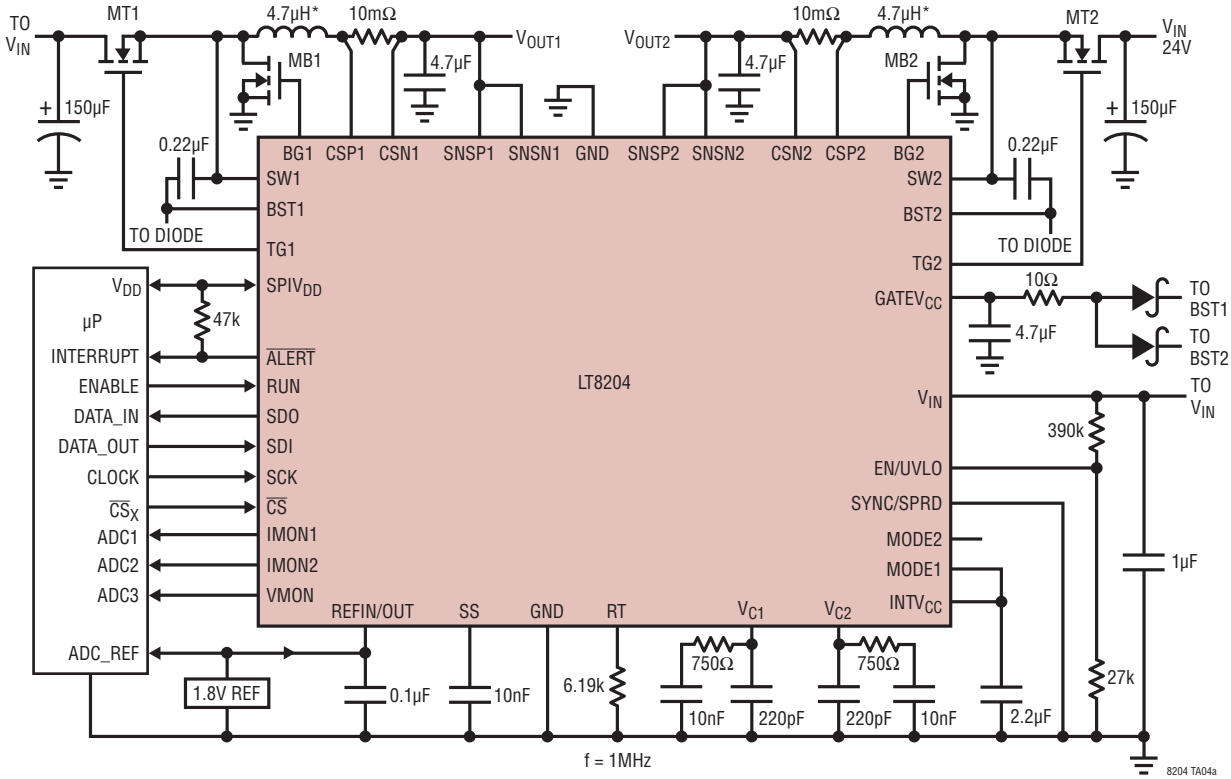
V_{OUT} Commanded to Step Down



$V_{OUT} = V_{OUT1} – V_{OUT2}$ STEPS DOWN
FROM 5V TO –5V
LOAD = 4Ω

TYPICAL APPLICATIONS

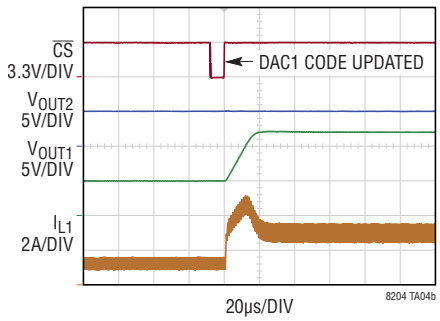
24V V_{IN} Dual-Channel 6A Output Voltage Regulator



EXTERNAL REFIN/OUT MODE (SS12–SS11 = 00)
75mV ILIM THRESHOLD (SS9 = 0)
WITHOUT SOFT SHUTDOWN CONTROL NOR HOLD MODE (SS5–SS4 = 10)
DCM MODE (SS7 = 1)
TWODAC (SS6 = 1)

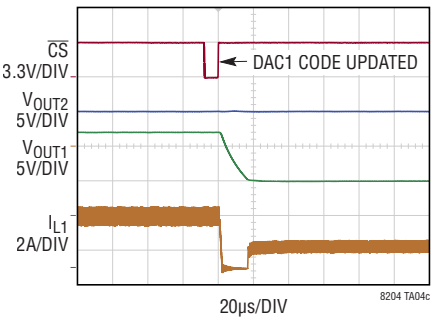
*COILCRAFT XAL1010-472ME

V_{OUT1} Commanded to Step Up



V_{OUT1} STEPS UP FROM 5V TO 12V
V_{OUT2} = 5V
LOAD1 = 4Ω, LOAD2 = 5Ω

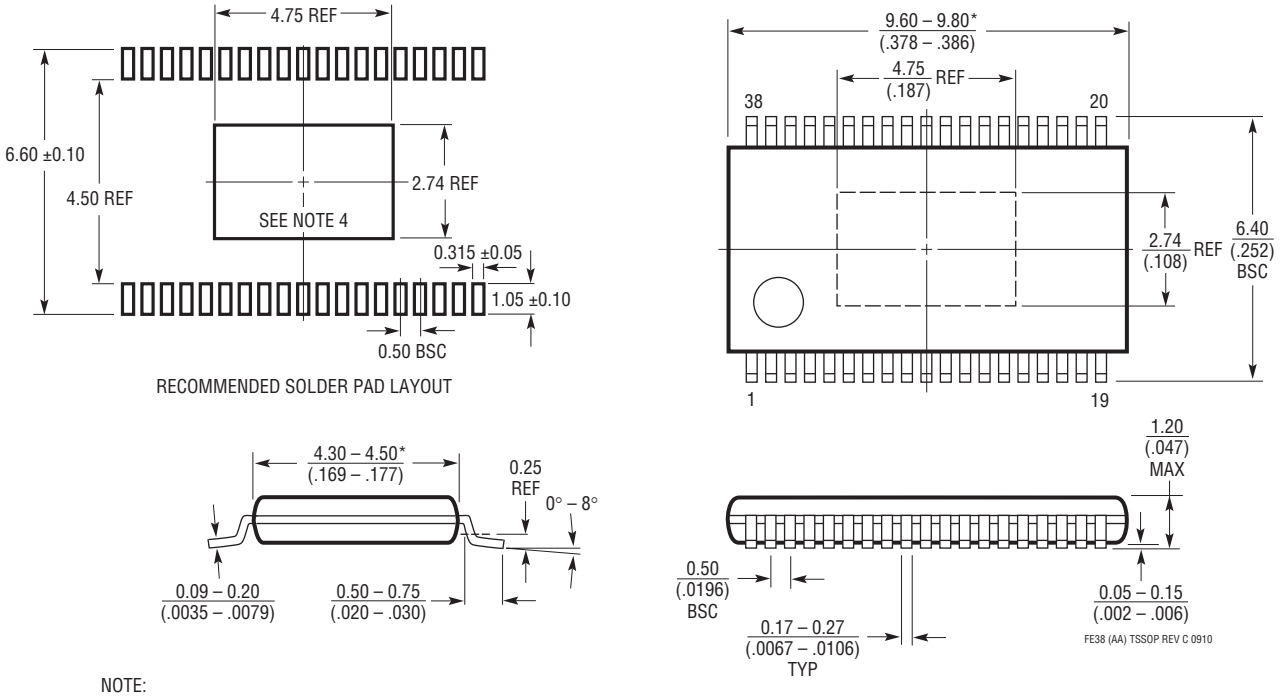
V_{OUT1} Commanded to Step Down



V_{OUT1} STEPS DOWN FROM 12V TO 5V
V_{OUT2} = 5V
LOAD1 = 4Ω, LOAD2 = 5Ω

PACKAGE DESCRIPTION

FE Package
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1772 Rev C)
Exposed Pad Variation AA

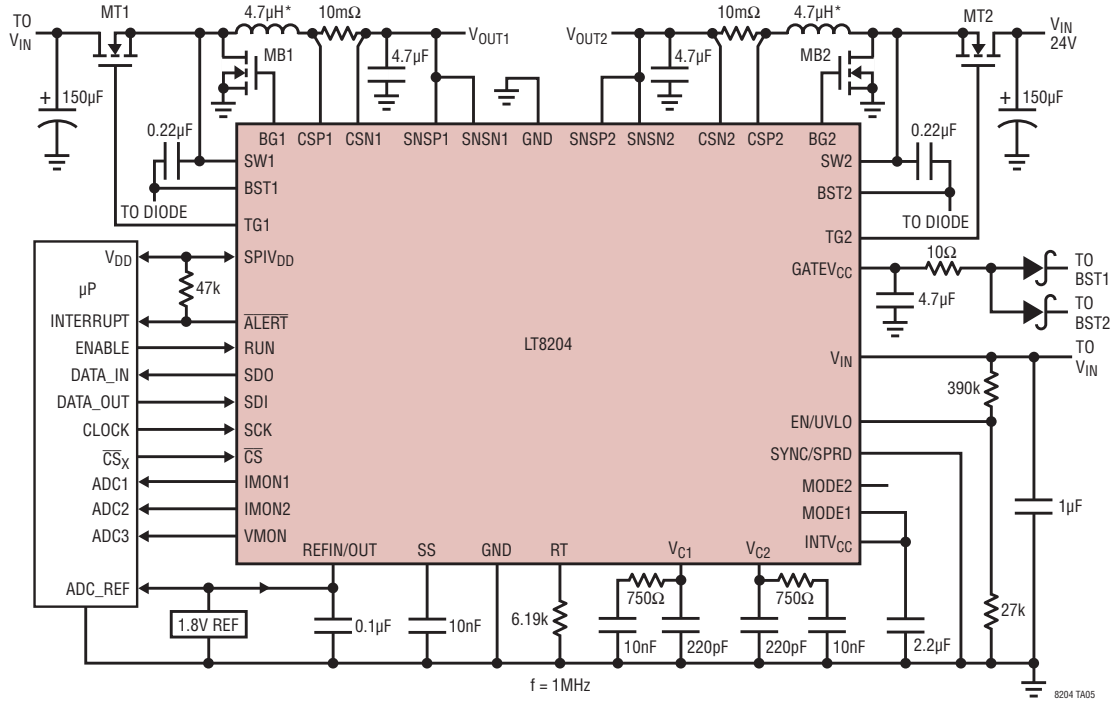


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

24V V_{IN} Dual-Channel 6A Output Voltage Regulator



EXTERNAL REFIN/OUT MODE (SS12–SS11 = 00)
75mV ILIM THRESHOLD (SS9 = 0)
WITHOUT SOFT SHUTDOWN CONTROL NOR HOLD MODE (SS5–SS4 = 10)
DCM MODE (SS7 = 1)
TWODAC (SS6 = 1)

*COILCRAFT XAL1010-472ME

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1923	High Efficiency Thermoelectric Cooler Controller	2.7V ≤ V_{IN} ≤ 5.5V, Full-Bridge Controller for Bidirectional Current Control, 5mm × 5mm QFN-28
LTC3838	Dual, Fast, Accurate Step-Down DC/DC Controller with Differential Output Sensing	4.5V ≤ V_{IN} ≤ 38V, 0.5V ≤ V_{OUT} ≤ 5.5V, I_{SD} < 15µA, 5mm × 7mm QFN-38
LTC3860	Dual, Multiphase Step-Down Voltage Mode DC/DC Controller with Current Sharing	3V ≤ V_{IN} ≤ 24V, 0.6V ≤ V_{OUT} ≤ 5V, I_{SD} < 50µA, 5mm × 5mm QFN-32
LTC3884	Dual Output PolyPhase® Step-Down Controller with Sub-mΩ DCR Sensing and Digital Power System Management	4.5V ≤ V_{IN} ≤ 38V, 0.5V ≤ V_{OUT} ≤ 5.5V, PMBus/I^2C Compliant Serial Interface, 7mm × 7mm QFN-48
LTC3886	60V Dual Output Step-Down Controller with Digital Power System Management	3V ≤ V_{IN} ≤ 60V, 0.5V ≤ V_{OUT} ≤ 13.8V, PMBus/I^2C Compliant Serial Interface, 7mm × 8mm QFN-52
LTC3892/ LTC3892-1	60V Low I_Q, Dual, 2-Phase Step-Down DC/DC Controller with 99% Duty Cycle	4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 99% • V_{IN}, Fixed Frequency 50kHz to 900kHz, Adjustable 5V to 10V Gate Drive, 5mm × 5mm QFN-32
References		
LT1236	Precision Reference	0.05% Max Tolerance, 5ppm/°C Max, 3µV_{P-P} 0.1Hz to 10Hz Noise
LT1460	Micropower Precision Series Reference	0.075% Max Tolerance, 10ppm/°C Max, 20µV_{P-P} 0.1Hz to 10Hz Noise
LT1790	Micropower Low Dropout Reference	0.05% Max Tolerance, 10ppm/°C Max, 12µV_{P-P} 0.1Hz to 10Hz Noise
LTC6652	Precision Low Drift Low Noise Buffered Reference	0.05% Max Tolerance, 5ppm/°C Max, 2.8ppm$_{P-P}$ 0.1Hz to 10Hz Noise
LTC6655	Low Drift Precision Buffered Reference	0.025% Max Tolerance, 2ppm/°C Max, 0.25ppm$_{P-P}$ 0.1Hz to 10Hz Noise