

# High-Efficiency, 6A, Current-Mode Synchronous Step-Down Switching Regulator

**MAX15106A/  
MAX15106B/  
MAX15106C**

## General Description

The MAX15106A/MAX15106B/MAX15106C family of high-efficiency, current-mode, synchronous step-down switching regulators with integrated power switches deliver up to 6A of output current. The regulators operate from 2.7V to 5.5V and provide an output voltage from 0.6V up to 95% of the input voltage, making the devices ideal for distributed power systems, portable devices, and pre-regulation applications.

The ICs utilize a current-mode control architecture with a high-gain transconductance error amplifier. The current-mode control architecture facilitates easy compensation design and ensures cycle-by-cycle current limit with fast response to line and load transients.

The low  $R_{DS(ON)}$  integrated switches ensure high efficiency at heavy loads while minimizing critical inductance, making the layout design a much simpler task with respect to discrete solutions. The ICs' simple layout and footprint assures first-pass success in new designs.

The regulator features 0.9MHz (MAX15106A), 1.0MHz (MAX15106B), and 1.1MHz (MAX15106C) factory-trimmed fixed frequency PWM-mode operation. The high-switching frequency, along with the PWM current-mode architecture allows for a compact, all-ceramic capacitor design.

The IC features a capacitor-programmable soft-start to reduce input inrush current. Internal control circuitry ensures safe startup into a prebiased output. Power sequencing is controlled with the enable input and power-good output.

The IC is available in a 20-bump (4 x 5 array), 2.5mm x 2mm WLP package and is fully specified over the -40°C to +105°C temperature range.

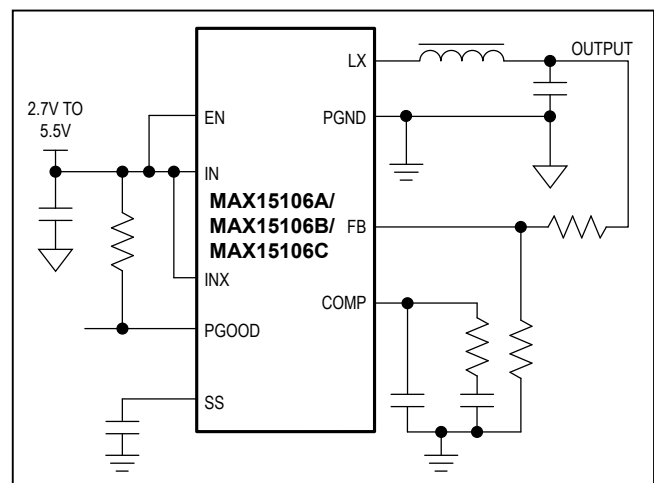
## Applications

- Distributed Power Systems
- DDR Memory
- Base Stations
- Portable Devices
- Notebook Power
- Server Power

## Features

- Continuous 6A Output Current
- Efficiency Up to 96%
- $\pm 1\%$  Accuracy Over Load, Line, and Temperature
- Operates from a 2.7V to 5.5V Supply
- Adjustable Output from 0.6V to  $0.95 \times V_{IN}$
- Programmable Soft-Start
- Safe Startup into Prebiased Output
- External Reference Input
- 0.9MHz, 1.0MHz, and 1.1MHz Switching Frequency Options
- Stable with Low-ESR Ceramic Output Capacitors
- Forced PWM Mode
- Enable Input and Power-Good Output for Power-Supply Sequencing
- Cycle-by-Cycle Overcurrent Protection
- Fully Protected Features Against Overcurrent and Overtemperature
- Input Undervoltage Lockout
- 20-Bump (4 x 5 Array), 2.5mm x 2mm, WLP Package

## Typical Operating Circuit



[Ordering Information](#) appears at end of data sheet.

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**Absolute Maximum Ratings**

IN, PGOOD to PGND.....	-0.3V to +6V	Continuous Power Dissipation (T <sub>BOARD</sub> = +70°C)
LX to PGND.....	-0.3V to (V <sub>IN</sub> + 0.3V)	WLP (derate 21.3mW/°C above T <sub>BOARD</sub> = +70°C).....
LX to PGND.....	-1V to +8V for 50ns	1.704W
EN, COMP, FB, SS to PGND.....	-0.3V to (V <sub>IN</sub> + 0.3V)	Operating Temperature Range.....
Continuous LX Current (Note 1).....	-12A to +12A	-40°C to +105°C
Output Short-Circuit Duration.....	Continuous	Operating Junction Temperature (Note 2).....
		+125°C
		Storage Temperature Range.....
		-65°C to +150°C
		Soldering Temperature (reflow) (Note 3).....
		+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Note 1:** LX has internal clamp diodes to PGND and IN. Do not exceed the power dissipation limits of the device when forward biasing these diodes.
- Note 2:** Limit the junction temperature to +125°C for continuous operation at full current.
- Note 3:** The WLP package is constructed using a unique set of package techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

**Package Information**

<b>PACKAGE TYPE: 20 WLP</b>	
Package Code	W202D2Z+1
Outline Number	<a href="#">21-0505</a>
Land Pattern Number	Refer to <a href="#">Application Note 1891</a>
<b>THERMAL RESISTANCE, FOUR-LAYER BOARD</b>	
Junction to Ambient (θ <sub>JA</sub> )	47°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

**Electrical Characteristics**

(V<sub>IN</sub> = 5V, C<sub>SS</sub> = 4.7nF, T<sub>A</sub> = T<sub>J</sub> = -40°C to +105°C. Typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.) (See the [Package Information](#) section for package thermal considerations.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Voltage Range	V <sub>IN</sub>		2.7		5.5	V
IN Shutdown Supply Current		V <sub>EN</sub> = 0V		0.3	3	µA
IN Supply Current	I <sub>IN</sub>	V <sub>EN</sub> = 5V, V <sub>FB</sub> = 0.75V, not switching		3.4	6	mA
V <sub>IN</sub> Undervoltage Lockout Threshold		LX starts switching, V <sub>IN</sub> rising		2.6	2.7	V
V <sub>IN</sub> Undervoltage Lockout Hysteresis		LX stops switching, V <sub>IN</sub> falling		200		mV
<b>ERROR AMPLIFIER</b>						
Transconductance	g <sub>MV</sub>			1.4		mS
Voltage Gain	A <sub>VEA</sub>			90		dB
FB Set-Point Accuracy	V <sub>FB</sub>	Over line, load, and temperature	594	600	606	mV
FB Input Bias Current	I <sub>FB</sub>		-100		+100	nA
COMP to Current-Sense Transconductance	G <sub>MOD</sub>			25		A/V
COMP Clamp Low		V <sub>FB</sub> = 0.75V		0.93		V
Compensation RAMP Valley				1		

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**Electrical Characteristics (continued)**

( $V_{IN} = 5V$ ,  $C_{SS} = 4.7nF$ ,  $T_A = T_J = -40^{\circ}C$  to  $+105^{\circ}C$ . Typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.) (See the [Package Information](#) section for package thermal considerations.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SWITCHES</b>						
High-Side Switch Current-Limit Threshold	$I_{HSCL}$		7.5	9	12.5	A
Low-Side Switch Sink Current-Limit Threshold				7		
Low-Side Switch Source Current-Limit Threshold				9		
LX Leakage Current		$V_{EN} = 0V$			10	$\mu A$
RMS LX Output Current				6		A
<b>OSCILLATOR</b>						
Switching Frequency	$f_{SW}$	MAX15106A	750	900	1050	kHz
		MAX15106B	850	1000	1150	
		MAX15106C	950	1100	1250	
Maximum Duty Cycle	$D_{MAX}$			94		%
Minimum Controllable On-Time				100		ns
<b>ENABLE</b>						
EN Input High-Threshold Voltage		$V_{EN}$ rising	1.3			V
EN Input Low-Threshold Voltage		$V_{EN}$ falling			0.4	
EN Input-Leakage Current		$V_{EN} = 5V$			1	$\mu A$
<b>SOFT-START, PREBIAS</b>						
Soft-Start Current	$I_{SS}$	$V_{SS} = 0.45V$ , sourcing		10		$\mu A$
SS Discharge Resistance	$R_{SS}$	$I_{SS} = 10mA$ , sinking		8.5		$\Omega$
SS Prebias Mode Stop Voltage		SS rising		0.58		V
<b>HICCUP</b>						
Number of Consecutive Current-Limit Events to Hiccup				8		Events
Timeout				1024		Clock Cycles
<b>POWER-GOOD OUTPUT</b>						
PGOOD Threshold		FB rising	0.54	0.56	0.585	V
PGOOD Threshold Hysteresis		FB falling		25		mV
PGOOD $V_{OL}$		$I_{PGOOD} = 5mA$ , $V_{FB} = 0.5V$		22	100	
PGOOD Leakage		$V_{PGOOD} = 5V$ , $V_{FB} = 0.75V$			1	$\mu A$
<b>THERMAL SHUTDOWN</b>						
Thermal Shutdown Threshold				+160		$^{\circ}C$
Thermal Shutdown Hysteresis		Temperature falling		+25		

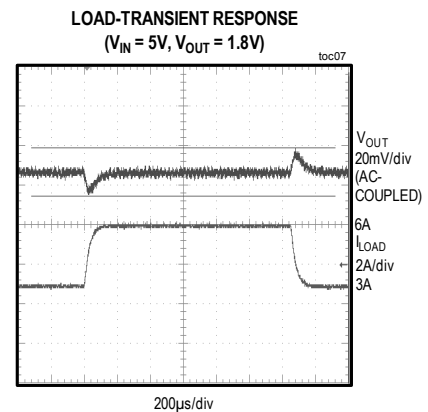
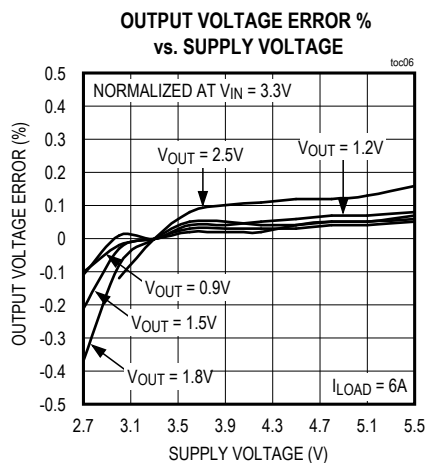
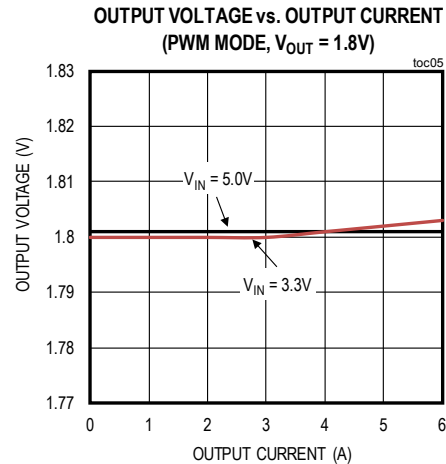
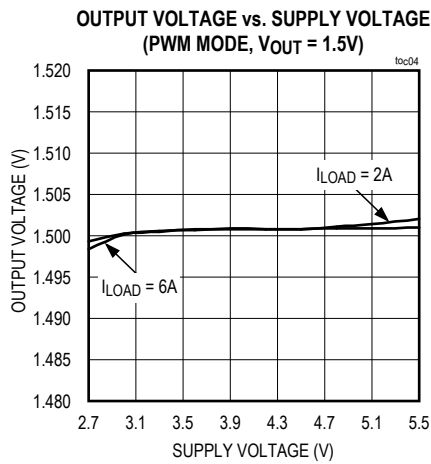
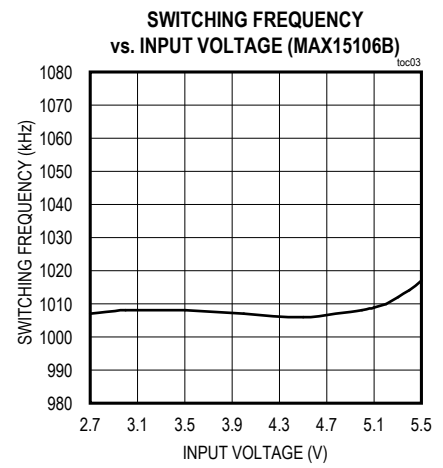
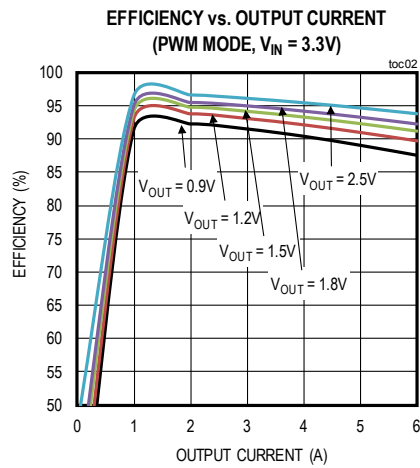
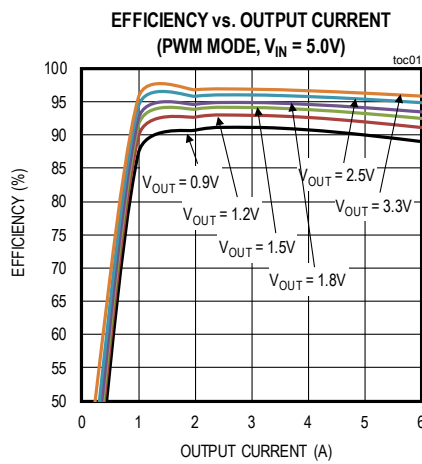
**Note 5:** Specifications are 100% production tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design and characterization.

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**Typical Operating Characteristics**

(Circuit of [Typical Application Circuit](#),  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

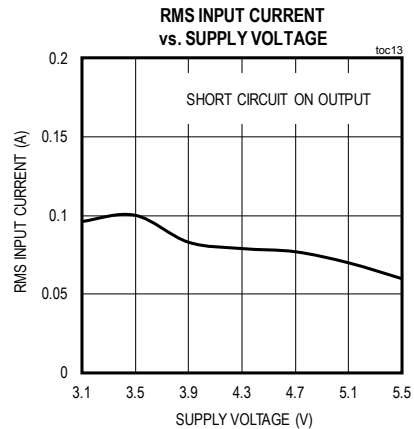
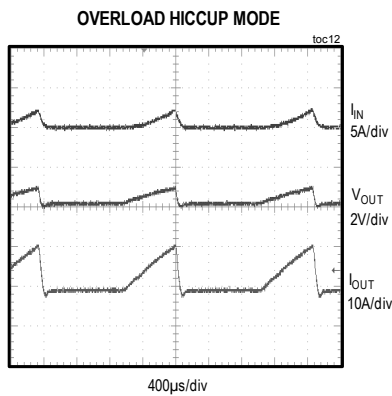
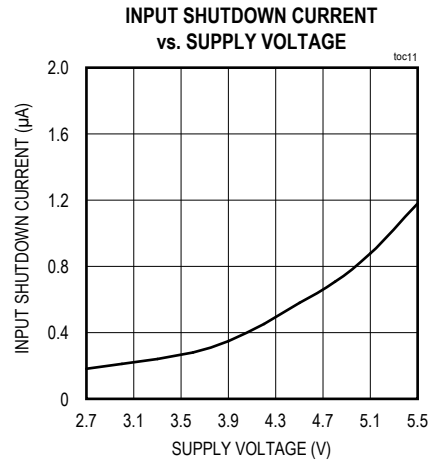
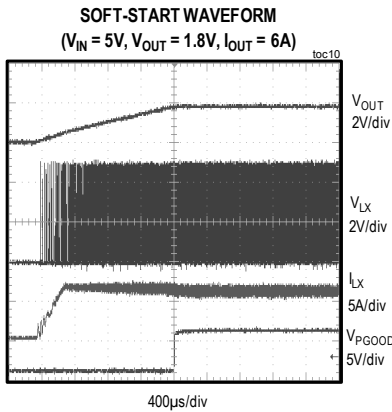
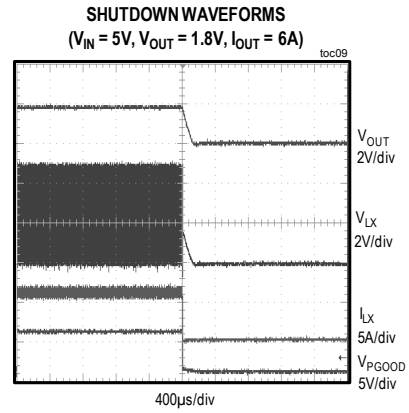
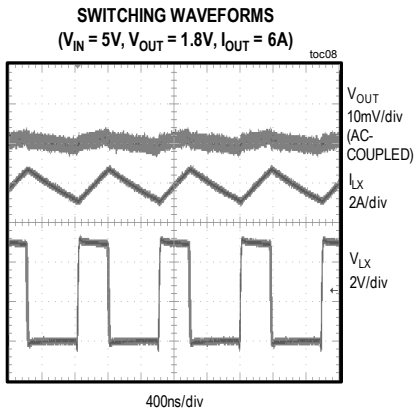


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**Typical Operating Characteristics (continued)**

(Circuit of [Typical Application Circuit](#),  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

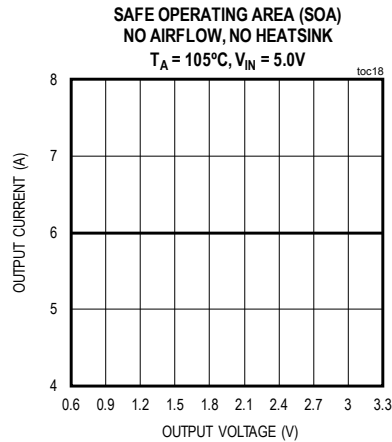
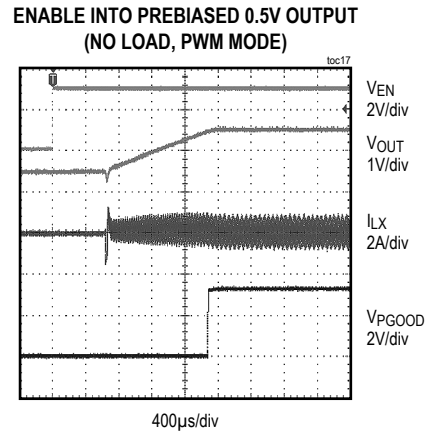
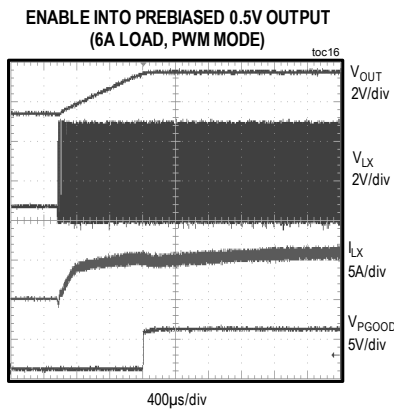
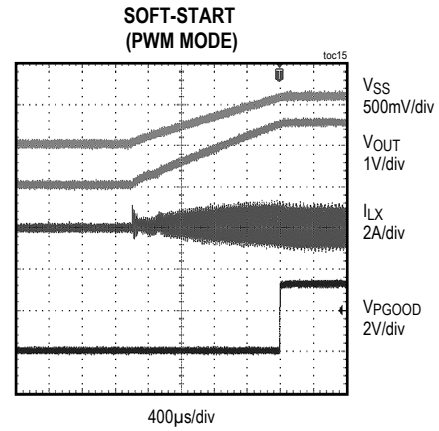
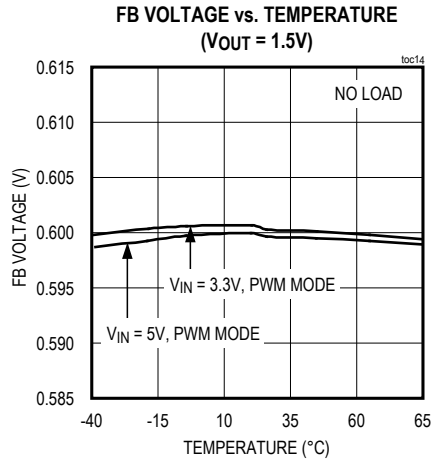


**MAX15106A/  
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**Typical Operating Characteristics (continued)**

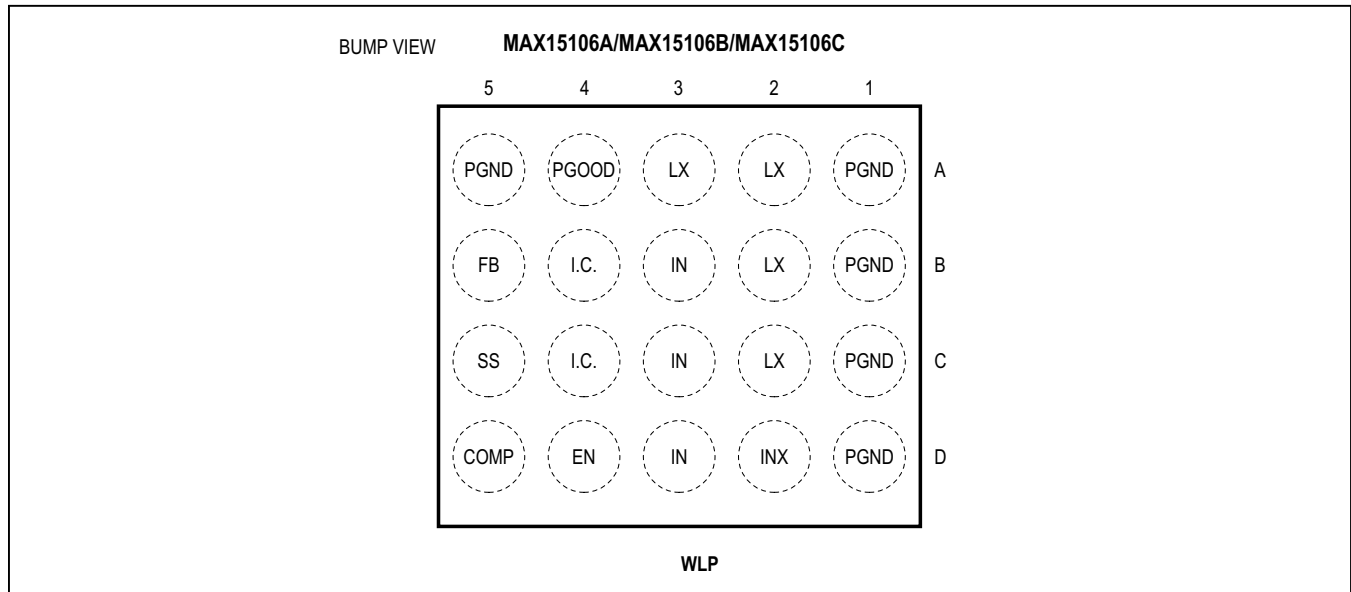
(Circuit of [Typical Application Circuit](#),  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



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**Pin Configuration**



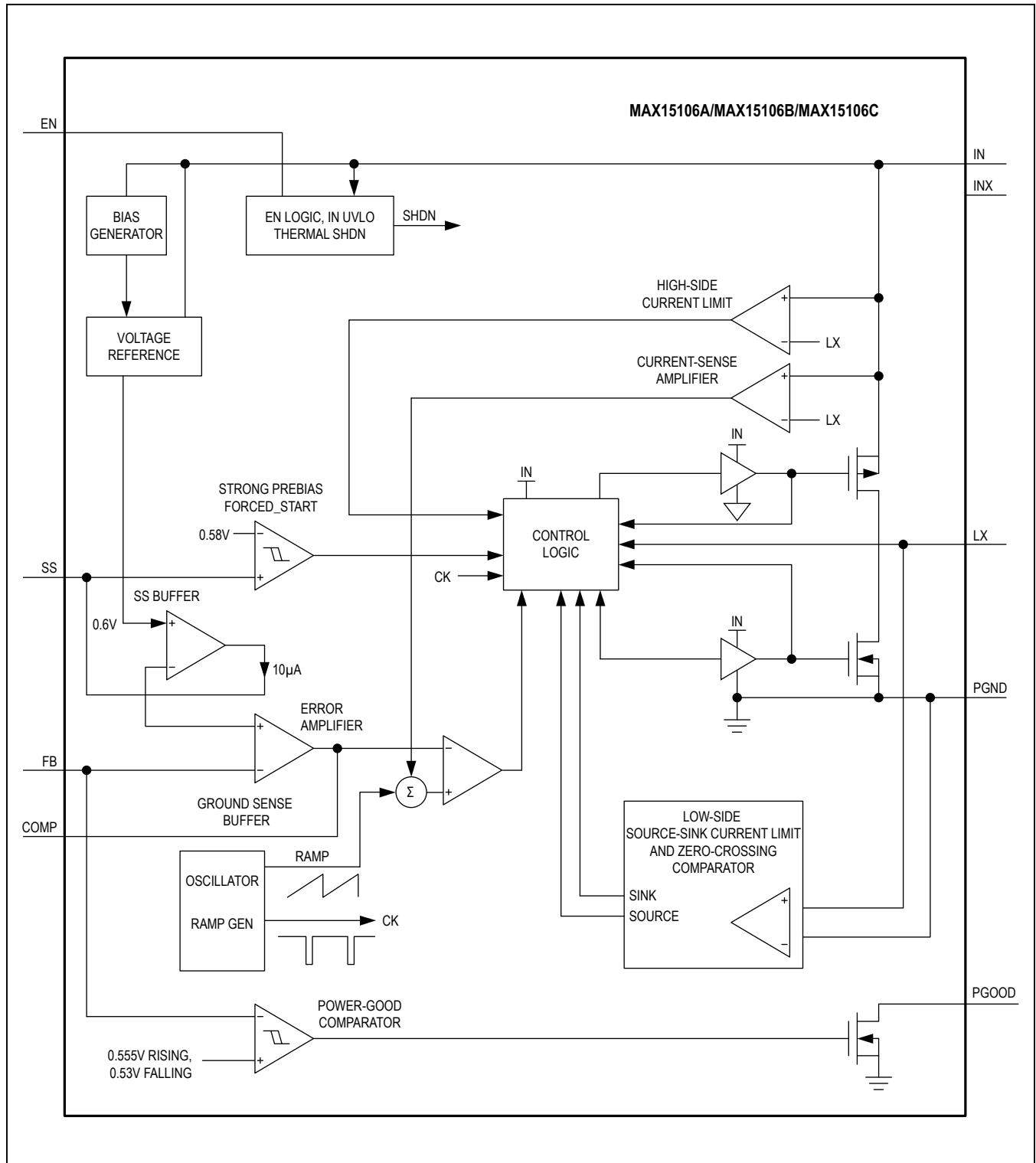
**Pin Description**

BUMP	NAME	FUNCTION
A1, A5, B1, C1, D1	PGND	Power Ground. Low-side switch source terminal. Connect PGND and the return terminals of input and output capacitors to the power ground plane.
A2, A3, B2, C2	LX	Inductor Connection. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown mode.
A4	PGOOD	Open-Drain Power-Good Output. PGOOD goes low when $V_{FB}$ is below 530mV.
B3, C3, D3	IN	Input Power Supply. Input supply range is 2.7V to 5.5V. Bypass IN with a minimum 10 $\mu$ F ceramic capacitor to PGND. See the <a href="#">Typical Application Circuit</a> .
B4, C4	I.C.	Internally Connected. Leave unconnected.
B5	FB	Feedback Input. Connect FB to the center tap of an external resistive voltage-divider from the output to PGND to set the output voltage from 0.6V to 95% of $V_{IN}$ .
C5	SS	Soft-Start. Connect a capacitor from SS to PGND to set the startup time. See the <a href="#">Setting the Soft-Start Startup Time</a> section for details on setting the soft-start time. SS is also an external reference input. Apply an external voltage reference from 0V to $V_{IN} - 1.5V$ to drive soft-start externally.
D2	INX	Input Bump for Control Section. Connect to IN.
D4	EN	Enable Input. EN is a digital input that turns the regulator on and off. Drive EN high to turn on the regulator. Connect to IN for always-on operation.
D5	COMP	Error Amplifier Output. Connect compensation network from COMP to signal ground (SGND). See the <a href="#">Compensation Design Guidelines</a> section.

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**Functional Diagram**





## Detailed Description

The MAX15106A/MAX15106B/MAX15106C high-efficiency, current-mode switching regulators deliver up to 6A of output current. The regulators provide output voltages from 0.6V to  $(0.95 \times V_{IN})$  with 2.7V to 5.5V input supplies, making the device ideal for on-board point-of-load applications.

The IC delivers current-mode control architecture using a high-gain transconductance-error amplifier. The current-mode control architecture facilitates easy compensation design and ensures cycle-by-cycle current limit with fast response to line and load transients.

The regulator features 0.9MHz (MAX15106A), 1.0MHz (MAX15106B), and 1.1MHz (MAX15106C) fixed switching frequencies, allowing for all-ceramic capacitor designs with fast transient responses. The high operating frequency minimizes the size of external components. The IC is available in a 2.5mm x 2mm (4 x 5 array), 0.5mm pitch WLP package.

The low  $R_{DS(ON)}$  integrated switches ensure high efficiency at heavy loads while minimizing critical inductance, making the layout design a much simpler task than that of discrete solutions. The ICs' simple layout and footprint assure first-pass success in new designs.

The ICs feature PWM current-mode control, allowing for an all-ceramic capacitor solution. The regulators offer capacitor-programmable soft-start to reduce input inrush current. The device safely starts up into a prebiased output. The IC includes an enable input and open-drain PGOOD output for sequencing with other devices.

### Controller Function—PWM Logic

The controller logic block determines the duty cycle of the high-side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current-limit and temperature protection are not triggered, the controller logic block takes the output from the PWM comparator to generate the driver signals for both high-side and low-side MOSFETs. The control logic block controls the break-before-make logic and all the necessary timing.

The high-side MOSFET turns on at the beginning of the oscillator cycle and turns off when the COMP voltage

crosses the internal current-mode ramp waveform. The internal ramp is the sum of the compensation ramp and the current-mode ramp derived from the inductor current (current sense block). The high-side MOSFET also turns off if the maximum duty cycle exceeds 95%, or when the current limit is reached. The low-side MOSFET turns on for the remainder of the switching cycle.

### Starting into a Prebiased Output

The ICs can soft-start into a prebiased output without discharging the output capacitor. In safe prebiased startup, both low-side and high-side MOSFETs remain off to avoid discharging the prebiased output. PWM operation starts when the voltage on SS crosses the voltage on FB.

The ICs can start into a prebiased voltage higher than the nominal set point without abruptly discharging the output. Forced PWM operation starts when the SS voltage reaches 0.58V, forcing the converter to start. When the low-side sink current-limit threshold of 1A is reached, the low-side switch turns off before the end of the clock period. The low-side sink current limit is 1A. The high-side switch turns on until one of the following conditions is satisfied:

- High-side source current hits the reduced high-side current limit (1A). The high-side switch turns off for the remaining time of clock period.
- The clock period ends.

Reduced high-side current limit is activated in order to recirculate the current into the high-side power switch rather than into the internal high-side body diode, which can cause damage to the device.

Low-side sink current limit protects the low-side switch from excessive reverse current during prebiased operation.

### Enable Input

The IC features independent device enable control and power-good signal that allow for flexible power sequencing. Drive the enable input (EN) high to enable the regulator, or connect EN to IN for always-on operation. Power-good (PGOOD) is an open-drain output that deasserts when  $V_{FB}$  is above 555mV, and asserts low if  $V_{FB}$  is below 530mV.

### Programmable Soft-Start (SS)

The ICs utilize a soft-start feature to slowly ramp up the regulated output voltage to reduce input inrush current during startup. Connect a capacitor from SS to SGND to set the startup time. See the [Setting the Soft-Start Startup Time](#) section for capacitor selection details.

### Error Amplifier

A high-gain error amplifier provides accuracy for the voltage feedback loop regulation. Connect a compensation network between COMP and SGND. See the [Compensation Design Guidelines](#) section. The error amplifier transconductance is 1.4mS. COMP clamp low is set to 0.93V, just below the PWM ramp compensation valley, helping COMP to rapidly return to the correct set point during load and line transients.

### PWM Comparator

The PWM comparator compares COMP voltage to the current-derived ramp waveform (LX current to COMP voltage transconductance value is 25A/V). To avoid instability due to subharmonic oscillations when the duty cycle is around 50% or higher, a compensation ramp is added to the current-derived ramp waveform. The compensation ramp slope ( $0.3V \times 1MHz = 0.3V/\mu s$ ) is equivalent to half of the inductor current down-slope in the worst case (load 2A, current ripple 30% and maximum duty-cycle operation of 95%). The compensation ramp valley is set to 1V.

### Overcurrent Protection and Hiccup

When the converter output is connected to ground or the device is overloaded, each high-side MOSFET current-limit event (9A) turns off the high-side MOSFET and turns on the low-side MOSFET. A 3-bit counter increments on each current-limit event. The counter is reset after three consecutive events of high-side MOSFET turn-on without reaching the current limit. If the current limit condition persists, the counter fills up reaching eight events. The control logic then discharges SS, stops both high-side and low-side MOSFETs and waits for a hiccup period (1024 clock cycles) before attempting a new soft-start sequence. The hiccup-mode also operates during soft-start.

### Thermal Shutdown Protection

The ICs contain an internal thermal sensor that limits the total power dissipation to protect it in the event of an extended thermal fault condition. When the die temperature exceeds +160°C, the thermal sensor shuts down the device, turning off the DC-DC converter to allow the die to cool. After the die temperature falls by 25°C, the device restarts, following the soft-start sequence.

## Applications Information

### Setting the Output Voltage

Connect a voltage-divider (R1 and R2, see [Figure 1](#)) from OUT to FB to PGND to set the DC-DC converter output voltage. Choose R1 and R2 so that the DC errors due to the FB input bias current do not affect the output-voltage precision. With lower value resistors, the DC error is reduced, but the amount of power consumed in the resistive divider increases. A typical tradeoff value for R2 is 5kΩ, but values between 1kΩ and 20kΩ are acceptable. Once R2 is chosen, calculate R1 using:

$$R_1 = R_2 \times \left( \frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where the feedback threshold voltage ( $V_{FB}$ ) = 0.6V.

### Inductor Selection

A large inductor value results in reduced inductor ripple current, leading to a reduced output ripple voltage. A high-value inductor is of a larger physical size with a higher series resistance (DCR) and a lower-saturation current rating. Choose inductor values to produce a ripple current equal to 30% of the load current.

Choose the inductor with the following formula:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where  $f_{SW}$  is the internally fixed 1MHz switching frequency, and  $\Delta I_L$  is the estimated inductor ripple current (typically set to  $0.3 \times I_{LOAD}$ ). In addition, the peak inductor current,  $I_{L\_PK}$ , must always be below the high-side current-limit value,  $I_{HSCL}$ , and the inductor saturation current rating,  $I_{L\_SAT}$ .

Ensure that the following relationship is satisfied:

$$I_{L\_PK} = I_{LOAD} + \frac{1}{2} \times \Delta I_L < \text{MIN}(I_{HSCL}, I_{L\_SAT})$$

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## High-Efficiency, 6A, Current-Mode Synchronous Step-Down Switching Regulator

### Input Capacitor Selection

For a step-down converter, the input capacitor  $C_{IN}$  helps to keep the DC input voltage steady, in spite of discontinuous input AC current. Use low-ESR capacitors to minimize the voltage ripple due to ESR.

Size  $C_{IN}$  using the following formula:

$$C_{IN} = \frac{I_{LOAD}}{f_{SW} \times \Delta V_{IN\_RIPPLE}} \times \frac{V_{OUT}}{V_{IN}}$$

Make sure that the selected capacitance can accommodate the input ripple current given by:

$$I_{RMS} = I_O \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

If necessary, use multiple capacitors in parallel to meet the RMS current rating requirement.

### Output Capacitor Selection

Use low-ESR ceramic capacitors to minimize the voltage ripple due to ESR. Use the following formula to estimate the total output voltage peak-to-peak ripple:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR\_COUT} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right)$$

Select the output capacitors to produce an output-ripple voltage that is less than 2% of the set output voltage.

### Setting the Soft-Start Startup Time

The soft-start feature ramps up the output voltage slowly, reducing input inrush current during startup. Size the  $C_{SS}$  capacitor to achieve the desired soft-start time,  $t_{SS}$ , using:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{FB}}$$

$I_{SS}$ , the soft-start current, is  $10\mu A$ , and  $V_{FB}$ , the output feedback voltage threshold, is  $0.6V$ . When using large  $C_{OUT}$  capacitance values, the high-side current limit can trigger during the soft-start period. To ensure the correct soft-start time,  $t_{SS}$ , choose  $C_{SS}$  large enough to satisfy:

$$C_{SS} \gg C_{OUT} \times \frac{V_{OUT} \times I_{SS}}{(I_{HSCL\_MIN} - I_{OUT}) \times V_{FB}}$$

$I_{HSCL\_MIN}$  is the minimum high-side switch current-limit value.

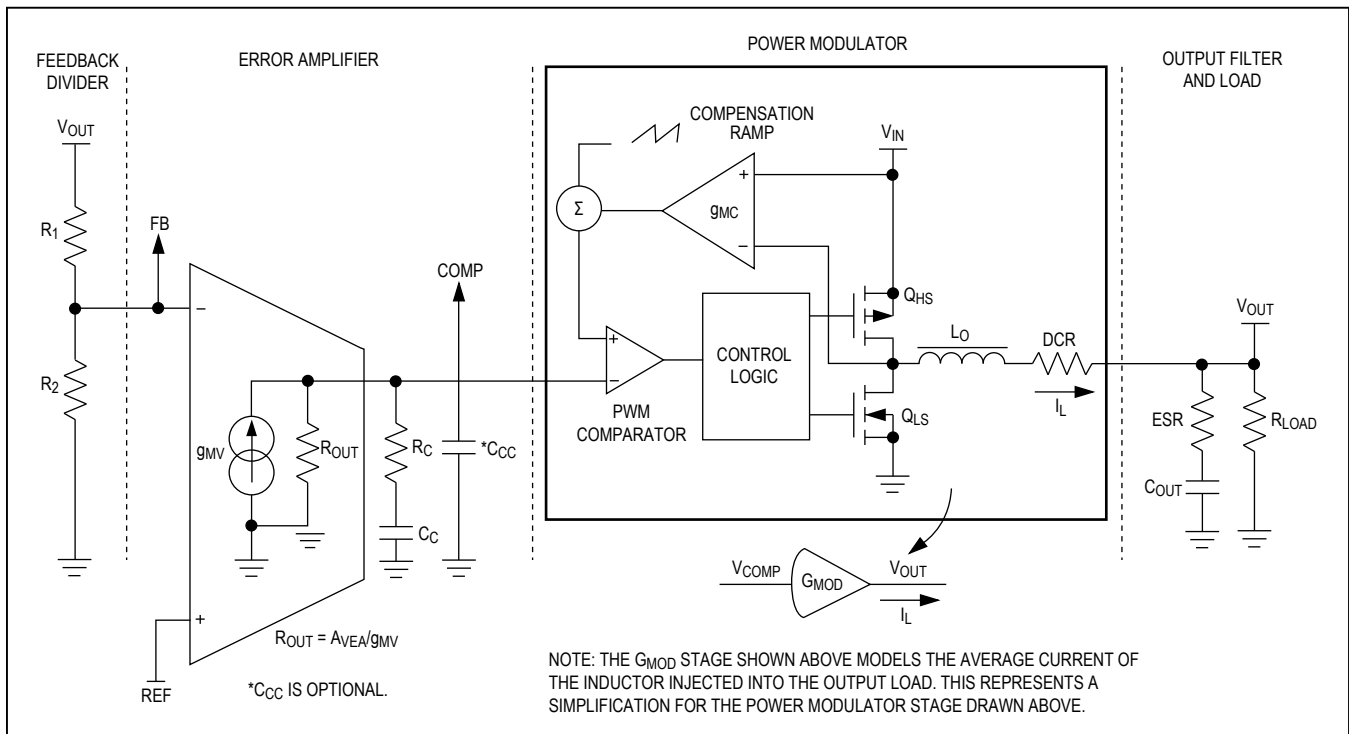


Figure 1. Peak Current-Mode Regulator Transfer Model

**MAX15106A/  
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**High-Efficiency, 6A, Current-Mode  
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An external tracking reference with steady-state value between 0V and  $V_{IN} - 1.5V$  can be applied to SS. In this case, connect an RC network from external tracking reference and SS as in [Figure 2](#). Set  $R_{SS}$  to approximately 1kΩ. In this application,  $R_{SS}$  is needed to ensure that, during hiccup period, SS can be internally pulled down. When an external reference is connected to SS, the soft-start must be provided externally.

**Compensation Design Guidelines**

The IC uses a fixed-frequency, peak-current-mode control scheme to provide easy compensation and fast transient response. The inductor peak current is monitored on a cycle-by-cycle basis and compared to the COMP voltage (output of the voltage error amplifier). The regulator's duty cycle is modulated based on the inductor's peak current value. This cycle-by-cycle control of the inductor current emulates a controlled current source. As a result, the inductor's pole frequency is shifted beyond the gain bandwidth of the regulator. System stability is provided with the addition of a simple series capacitor-resistor from COMP to PGND. This pole-zero combination serves to tailor the desired response of the closed-loop system. The basic regulator loop consists of a power modulator (comprising the regulator's pulse-width modulator, compensation ramp, control circuitry, MOSFETs, and inductor), the capacitive output filter and load, an output feedback divider, and a voltage-loop error amplifier with its associated compensation circuitry (see [Figure 1](#)).

The average current through the inductor is expressed as:

$$\bar{I}_L = G_{MOD} \times \bar{V}_{COMP}$$

where  $\bar{I}_L$  is the average inductor current and  $G_{MOD}$  is the power modulator's transconductance.

For a buck converter:

$$\bar{V}_{OUT} = R_{LOAD} \times \bar{I}_L$$

where  $R_{LOAD}$  is the equivalent load resistor value. Combining the above two relationships, the power modulator's transfer function in terms of  $\bar{V}_{OUT}$  with respect to  $\bar{V}_{COMP}$  is:

$$\frac{\bar{V}_{OUT}}{\bar{V}_{COMP}} = \frac{R_{LOAD} \times \bar{I}_L}{\bar{I}_L} = R_{LOAD} \times G_{MOD}$$

Having defined the power modulator's transfer function gain, the total system loop gain can be written as follows (see [Figure 1](#)):

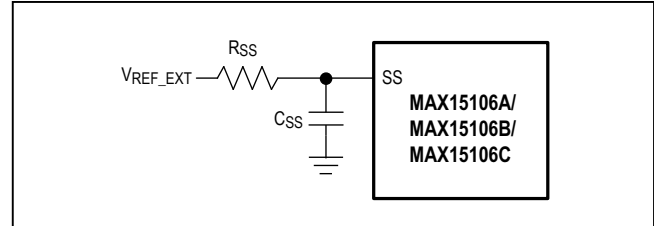


Figure 2. Setting Soft-Start Time

$$\alpha = \frac{R_{OUT} \times (sC_C R_C + 1)}{[s(C_C + C_{CC})(R_C + R_{OUT}) + 1] \times [s(C_C \parallel C_{CC})(R_C \parallel R_{OUT}) + 1]}$$

$$\beta = G_{MOD} \times R_{LOAD} \times \frac{(sC_{OUT} ESR + 1)}{[sC_{OUT}(ESR + R_{LOAD}) + 1]}$$

$$\text{Gain} = \frac{R_2}{R_1 + R_2} \times \frac{A_{VEA}}{R_{OUT}} \times \alpha \times \beta$$

where  $R_{OUT}$  is the quotient of the error amplifier's DC gain,  $A_{VEA}$ , divided by the error amplifier's transconductance,  $g_{MV}$ ;  $R_{OUT}$  is much larger than  $R_C$ .

$$\frac{R_2}{R_1 + R_2} = \frac{V_{FB}}{V_{OUT}}$$

Also,  $C_C$  is much larger than  $C_{CC}$ , therefore:

$$C_C + C_{CC} \approx C_C$$

and

$$C_C \parallel C_{CC} \approx C_{CC}$$

Rewriting:

$$\text{Gain} = \frac{V_{FB}}{V_{OUT}} A_{VEA} \times \frac{(sC_C R_C + 1)}{[sC_C \left(\frac{A_{VEA}}{g_{MV}}\right) + 1] \times (sC_{CC} R_C + 1)} \times$$

$$G_{MOD} R_{LOAD} \times \frac{(sC_{OUT} ESR + 1)}{[sC_{OUT}(ESR + R_{LOAD}) + 1]}$$

The dominant poles and zeros of the transfer loop gain are shown below:

$$f_{P1} = \frac{g_{MV}}{2\pi \times 10^{AVEA\_dB/20} \times C_C}$$

$$f_{P2} = \frac{1}{2\pi \times C_{OUT}(ESR + R_{LOAD})}$$

$$f_{P3} = \frac{1}{2\pi \times C_{CC}R_C}$$

$$f_{Z1} = \frac{1}{2\pi \times C_C R_C}$$

$$f_{Z2} = \frac{1}{2\pi \times C_{OUT}ESR}$$

The order of pole-zero occurrence is:

$$f_{P1} < f_{P2} < f_{Z1} < f_{Z2} \leq f_{P3}$$

Under heavy load,  $f_{P2}$ , approaches  $f_{Z1}$ . A graphical representation of the asymptotic system closed-loop response, including dominant pole and zero locations, is shown in [Figure 3](#).

If  $C_{OUT}$  is large, or exhibits a lossy equivalent series resistance (large ESR), the circuit's second zero might come into play around the crossover frequency ( $f_{CO} = \omega/2\pi$ ). In this case, a third pole can be induced by a second (optional) small compensation capacitor ( $C_{CC}$ ), connected from COMP to PGND. The loop response's fourth asymptote (in bold, [Figure 3](#)) is the one of interest in establishing the desired crossover frequency (and determining the compensation component values). A lower crossover frequency provides for stable closed-loop operation at the expense of a slower load and line transient response. Increasing the crossover frequency improves the transient response at the (potential) cost of system instability. A standard rule of thumb sets the crossover frequency  $\leq 1/10$ th of the switching frequency. First, select the passive and active power components that meet the application's requirements. Then, choose the small-signal compensation components to achieve the desired closed-loop response and phase margin as outlined in the [Closing the Loop: Designing the Compensation Circuitry](#) section.

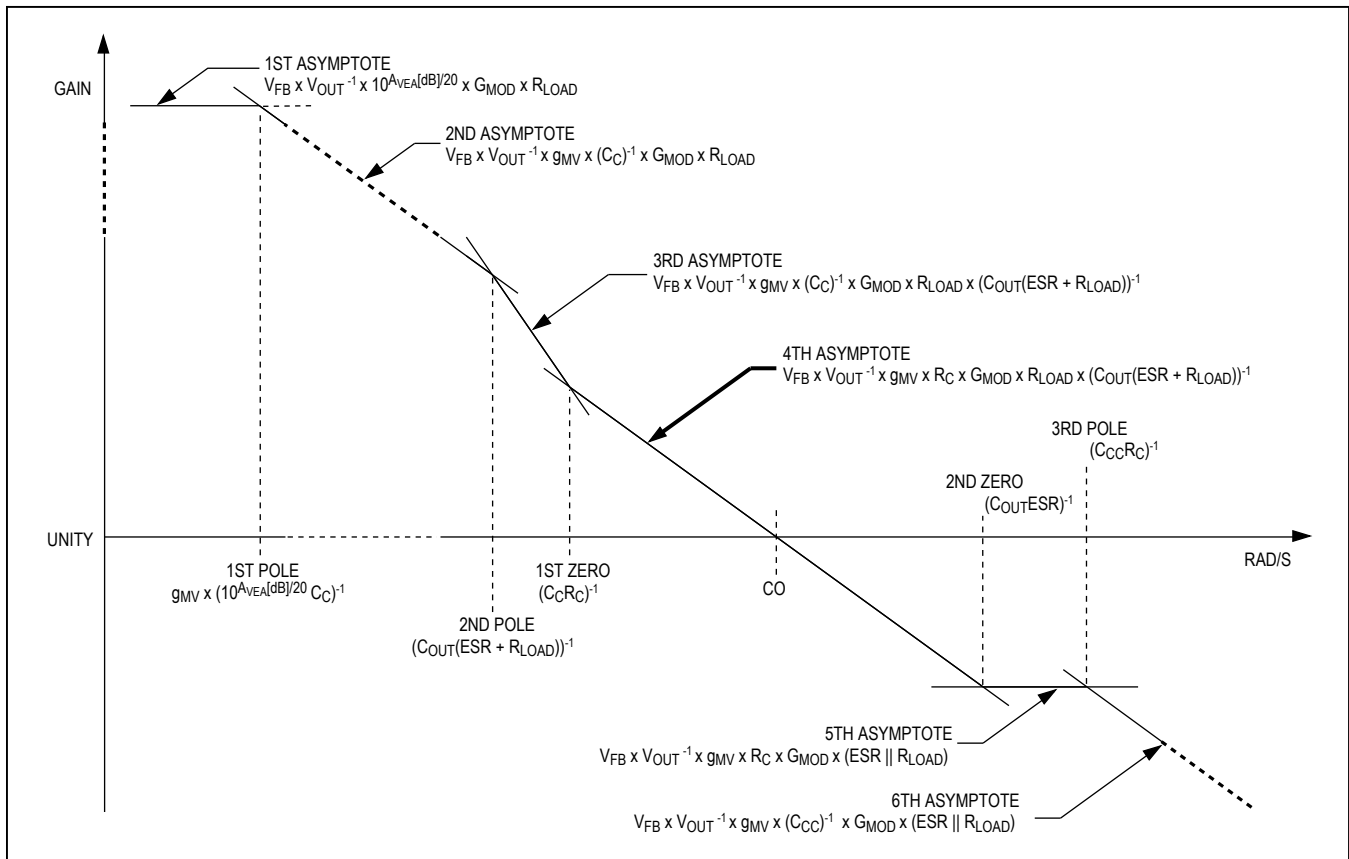


Figure 3. Asymptotic Loop Response of Peak Current-Mode Regulator

**Closing the Loop:  
Designing the Compensation Circuitry**

Select the desired crossover frequency. Choose  $f_{CO}$  approximately 1/10th of the switching frequency  $f_{SW}$ , or  $f_{CO} \approx 100\text{kHz}$ .

Select  $R_C$  using the transfer-loop's fourth asymptote gain (assuming  $f_{CO} > f_{P1}$ ,  $f_{P2}$ , and  $f_{Z1}$  and setting the overall loop gain to unity) as follows:

$$1 = \frac{V_{FB}}{V_{OUT}} \times g_{MV} \times R_C \times G_{MOD} \times R_{LOAD} \times \frac{1}{2\pi \times f_{CO} \times C_{OUT} \times (ESR + R_{LOAD})}$$

Therefore:

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times f_{CO} \times C_{OUT} \times (ESR + R_{LOAD})}{g_{MV} \times G_{MOD} \times R_{LOAD}}$$

For  $R_{LOAD}$  much greater than ESR, the equation can be further simplified as follows:

$$R_C = \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times f_{CO} \times C_{OUT}}{g_{MV} \times G_{MOD}}$$

where  $V_{FB}$  is equal to 0.6V.

Determine  $C_C$  by selecting the desired first system zero,  $f_{Z1}$ , based on the desired phase margin. Typically, setting  $f_{Z1}$  below 1/5th of  $f_{CO}$  provides sufficient phase margin.

$$f_{Z1} = \frac{1}{2\pi \times C_C R_C} \leq \frac{f_{CO}}{5}$$

Therefore:

$$C_C \geq \frac{5}{2\pi \times f_{CO} \times R_C}$$

If the ESR output zero is located at less than one-half the switching frequency, use the (optional) secondary compensation capacitor,  $C_{CC}$ , to cancel it, as follows:

$$\frac{1}{2\pi \times C_{CC} R_C} = f_{P3} = f_{Z2} = \frac{1}{2\pi \times C_{OUT} ESR}$$

Therefore:

$$C_{CC} = \frac{C_{OUT} \times ESR}{R_C}$$

If the ESR zero exceeds 1/2 the switching frequency, use the following equation:

$$f_{P3} = \frac{1}{2\pi \times C_{CC} R_C} = \frac{f_{SW}}{2}$$

Therefore:

$$C_{CC} = \frac{2}{2\pi \times f_{SW} \times R_C}$$

Overall  $C_{CC}$  detracts from the overall system phase margin. Place this third pole well beyond the desired crossover frequency to minimize the interaction with the system loop response at crossover. Ignore  $C_{CC}$  in these calculations if  $C_{CC}$  is smaller than 10pF.

**Power Dissipation**

The IC is available in a 20-bump WLP package and can dissipate up to 1.704W at +70°C board temperature. When the die temperature exceeds +160°C, the thermal-shutdown protection is activated. See the [Thermal Shutdown Protection](#) section.

**Layout Procedure**

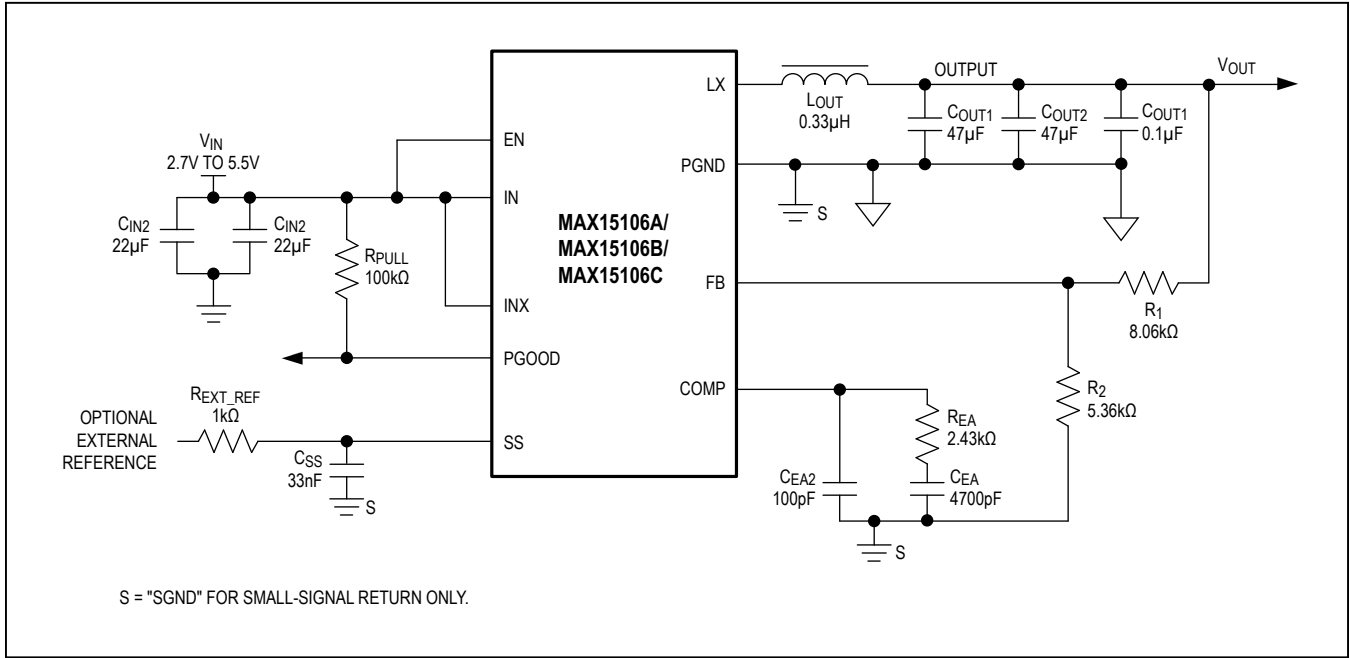
Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the MAX15106A/MAX15106B/MAX15106C evaluation kit layout for optimum performance. If deviation is necessary, follow these guidelines for good PCB layout:

- 1) Connect input and output capacitors to the power ground plane.
- 2) Place bypass capacitors as close to IN and the soft-start capacitor as close to SS as possible.
- 3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
- 4) Connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency.
- 5) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close as possible to the IC.
- 6) Route high-speed switching nodes (such as LX) away from sensitive analog areas (such as FB, COMP, SGND, and SS). See the EV kit layout for a tested layout example.

**MAX15106A/  
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MAX15106C**

**High-Efficiency, 6A, Current-Mode  
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**Typical Application Circuit**



**Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE	SWITCHING FREQUENCY (MHz)
<b>MAX15106AGWP+</b>	-40°C to +105°C	20 WLP	0.9
<b>MAX15106BGWP+</b>	-40°C to +105°C	20 WLP	1.0
<b>MAX15106CGWP+</b>	-40°C to +105°C	20 WLP	1.1

+Denotes a lead(Pb)-free/RoHS-compliant package.

**Chip Information**

PROCESS: BiCMOS

**MAX15106A/  
MAX15106B/  
MAX15106C**

High-Efficiency, 6A, Current-Mode  
Synchronous Step-Down Switching Regulator

**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/17	Initial release	—
1	7/17	Removed Future Product designation for MAX15106AGWP+ and MAX15106CGWP+	15
2	1/20	Updated <i>Absolute Maximum Ratings</i> section and <i>Power Dissipation</i> section	2, 14
3	6/21	Updated <i>Package Information</i> table	2



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