

Evaluation of the ADRF5023 Silicon SPDT Switch, Nonreflective , 9 kHz to 45 GHz

FEATURES

- ▶ Full-featured evaluation board for the [ADRF5023](#)
- ▶ Easy connection to the test equipment
- ▶ Thru line for calibration

EQUIPMENT NEEDED

- ▶ DC power supplies
- ▶ Network analyzer

GENERAL DESCRIPTION

The ADRF5023 is a single-pole, double-throw (SPDT) switch manufactured in the silicon process.

This user guide describes the ADRF5023-EVALZ evaluation board, designed to evaluate the features and performance of the ADRF5023. [Figure 1](#) shows a photograph of the evaluation board.

The [ADRF5023](#) data sheet provides full specifications for the ADRF5023. Refer to the [ADRF5023](#) data sheet with this user guide when using the ADRF5023-EVALZ.

ADRF5023-EVALZ EVALUATION BOARD PHOTOGRAPH

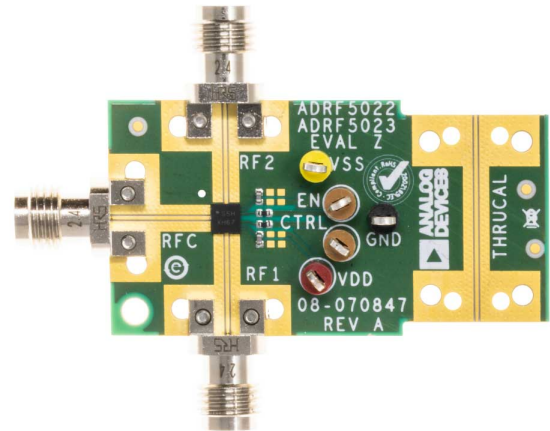


Figure 1. Evaluation Board Photograph

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REVISION HISTORY**1/2023—Revision 0: Initial Version**

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5023-EVALZ is a connectorized board, assembled with the ADRF5023 and its application circuitry. All components are placed on the primary side of ADRF5023-EVALZ. An assembly drawing for the ADRF5023-EVALZ is shown in Figure 6, and an evaluation board schematic is shown in Figure 5.

BOARD LAYOUT

The ADRF5023-EVALZ is designed using RF circuit design techniques on a 4-layer printed circuit board (PCB). The PCB stack-up is shown in Figure 2.

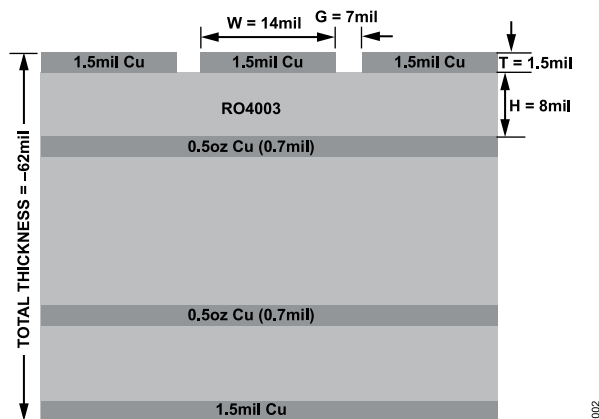


Figure 2. Evaluation Board Stack-Up

The outer copper layers are 1.5 mil thick and the inner layers are 0.7 mil thick.

All RF and DC traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 8 mil Rogers RO4003, offering optimal high-frequency performance. The middle and bottom dielectric materials provide mechanical strength. The total board thickness is 62 mil, which allows 2.4 mm RF edge launch connectors to be placed at the board edges.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 14 mil and ground spacing of 7 mil to have a characteristic impedance of 50 Ω . Ground via fences is arranged on both sides of a CPWG to improve isolation between nearby RF lines and other signal lines.

POWER-SUPPLY AND CONTROL INPUTS

The ADRF5023-EVALZ has two power-supply inputs, two control inputs, and a ground, as shown in Table 1. The DC test points are populated on V_{DD} , V_{SS} , CTRL, and GND. A 3.3 V supply is connected to the DC test points on V_{DD} , and a -3.3 V supply is connected to the DC test points on V_{SS} . Ground reference can be connected to GND. Connect the control input, CTRL, to 3.3 V or 0 V. The typical total current consumption for the ADRF5023 is 670 μA .

The V_{DD} and V_{SS} supply pin of the ADRF5023 are decoupled with 100 pF capacitors.

Table 1. Power-Supply and Control Inputs

Test Points	Description
V_{DD}	Positive supply voltage
V_{SS}	Negative supply voltage
CTRL	CONTROL input voltage
EN	EN input voltage
GND	Ground

EVALUATION BOARD HARDWARE

RF INPUTS AND OUTPUTS

The ADRF5023-EVALZ has five edge-mounted, 2.4 mm connectors for the RF inputs and outputs, as shown in [Table 2](#).

Table 2. RF Inputs and Outputs

2.4 mm Connectors	Description
RFC	RF common port
RF1	RF Throw Port 1
RF2	RF Throw Port 2
THRU1	Thru line input and output
THRU2	Thru line input and output

The through calibration line, connecting the THRU1 and THRU2 RF connectors, calibrates out the board loss effects from the measurements of the ADRF5023-EVALZ to determine the device performance at the pins of the IC. [Figure 3](#) shows the typical board loss for the ADRF5023-EVALZ at room temperature, as well as the embedded and de-embedded insertion loss for the [ADRF5023](#).

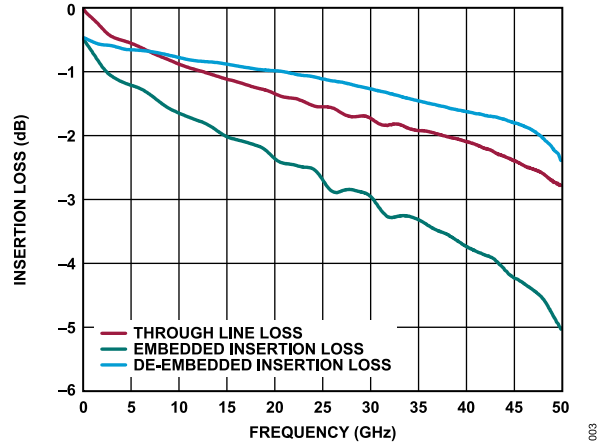


Figure 3. Insertion Loss vs. Frequency

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5023-EVALZ, perform the following steps:

1. Ground the GND test point.
2. Bias up the V_{DD} test point.
3. Bias up the V_{SS} test point.
4. Bias up the CTRL test point.
5. Bias up the EN test point.
6. Apply an RF input signal.

The ADRF5023-EVALZ is shipped fully assembled and tested. Figure 4 provides a basic test setup diagram to evaluate the s-parameters using a network analyzer. Perform the following steps to complete the test setup and verify the operation of the ADRF5023-EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the V_{DD} test point to the voltage-output terminal of the 3.3 V supply.
3. Connect the V_{SS} test point to the voltage-output terminal of the -3.3 V supply.
4. Connect the CTRL test point to the voltage-output terminal of the 3.3 V supply. The ADRF5023 can be configured in different modes by connecting the CTRL test point to 3.3 V or 0 V, as shown in Table 3.
5. Connect the EN test point to the voltage-output terminal of the 3.3 V supply. The ADRF5023 can be configured in different modes by connecting the EN test point to 3.3 V or 0 V, as shown in Table 3.
6. Connect a calibrated network analyzer to the RFC, RF1, and RF2 2.4 mm connectors. If the network analyzer port count is not enough, terminate unused RF ports with 50 Ω . Sweep the frequency from 10 MHz to 50 GHz and set the power to -10 dBm.

Additional test equipment is needed to fully evaluate the device's functions and performance.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high-isolation power combiner is also recommended.

For power compression and power handling evaluations, use a 2-channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

Note that the measurements performed at the 2.4 mm connectors of the ADRF5023-EVALZ include the losses of the 2.4 mm connectors and the PCB. The thru line must be measured to calibrate out the effects on the ADRF5023-EVALZ. The thru line is the summation of an RF input line and an RF output line that are connected to the device and equal in length.

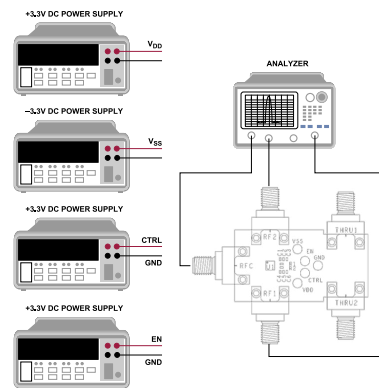


Figure 4. Test Setup Diagram

Table 3. Control Voltage Truth Table

Digital Control Inputs		RF Paths	
EN	CTRL	RF1 to RFC	RF2 to RFC
Low	Low	Isolation (off)	Insertion loss (on)
Low	High	Insertion loss (on)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)
High	High	Isolation (off)	Isolation (off)

EVALUATION BOARD SCHEMATIC AND ASSEMBLY DIAGRAM

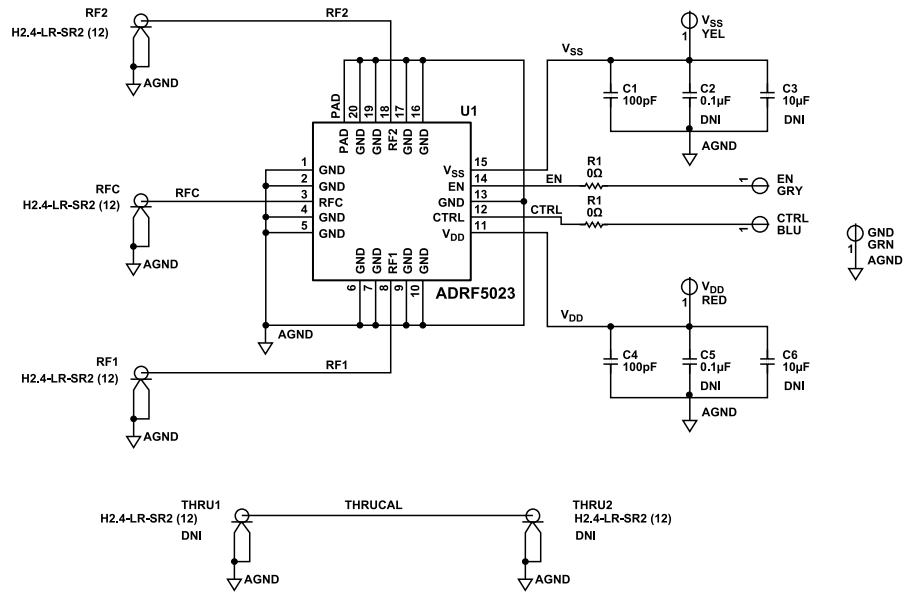


Figure 5. ADRF5023-EVALZ Evaluation Board Schematic

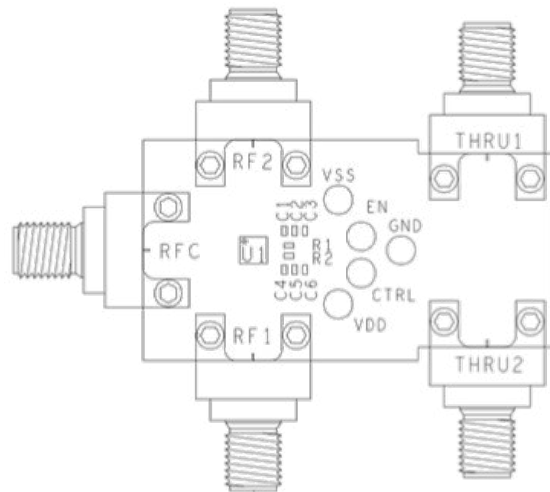


Figure 6. ADRF5023-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials for ADRF5023-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
2	C1, C4	Capacitors, 100 pF, 50 V, C0402 package	TDK	C1005NP01H101J050BA
2	C2, C5	Capacitors, 0.1 μ F, 16 V, C0402 package (do not insert, DNI)	SAMSUNG	CL05B104KO5NNNC
2	C3, C6	Capacitors, 10 μ F, 10 V, C0402 package (DNI)	SAMSUNG	CL05A106MP5NUNC
2	R1, R2	Resistors, 0 Ω , 0.1 W, 0402 package	Panasonic	ERJ-2GE0R00X
5	RFC, RF1, RF2, THRU1, and THRU2	Edge-mount 2.4 mm connectors	Hirose Electric CO.	H2.4-LR-SR2(12)
5	GND, CTRL, EN, V _{DD} , and V _{SS}	Surface-mount test points	Components Corporation	TP104-01
1	U1	Silicon SPDT switch, 9 kHz to 45 GHz	Analog Devices, Inc.	ADRF5023BCCZN
1	PCB	ADRF5023-EVALZ	Analog Devices, Inc.	BR-070847

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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