

MAX32675

Ultra-Low-Power Arm Cortex-M4F with Precision Analog Front-End for Industrial and Medical Sensors

General Description

The MAX32675 is a highly integrated, mixed-signal, ultra-low-power microcontroller for industrial applications and is especially suitable for 4-20mA loop-powered sensors and transmitters. It is based on an ultra-low-power Arm[®] Cortex[®]-M4 with Floating Point Unit (FPU) and includes 384KB of flash and 160KB of SRAM. Error correction coding (ECC), capable of single error correction, double error detection (SEC-DED), is implemented over the entire flash, SRAM, and cache to ensure ultra-reliable code execution for demanding applications. An analog front-end (AFE) provides two 12-channel delta-sigma (Δ - Σ) ADCs with features and specifications optimized for precision sensor measurement. Each Δ - Σ ADC can digitize external analog signals as well as system temperature. A PGA with gains of 1x to 128x precedes each ADC. ADC outputs can be optionally converted on the fly from integer to single-precision floating-point format. A 12-bit DAC is also included. The device also provides robust security features such as an AES Engine, TRNG, and secure boot.

Applications

- 4-20mA Industrial Sensors and Transmitters
- Industrial Pressure, Temperature, Flow, and Level Sensors/Transmitters
- Medical Pressure, Temperature, and Flow Sensors

Benefits and Features

- Low-Power, High-Performance for Industrial Applications
 - 100MHz Arm Cortex-M4 with FPU
 - 384KB Internal Flash
 - 160KB SRAM
 - 128kB ECC Enabled
 - 44.1 μ A/MHz ACTIVE Mode at 0.9V up to 12MHz CoreMark[®]
 - 64.5 μ A/MHz ACTIVE Mode at 1.1V up to 100MHz CoreMark
 - 2.84 μ A Full Memory Retention Current in BACKUP Mode at $V_{DDIO} = 3.3V$
 - Ultra-Low-Power Analog Peripherals
- Smart Integration Reduces BOM, Cost, and PCB Size
 - Two Δ - Σ ADCs
 - 12 Channels, Assignable to Either ADC
 - Flexible Resolution and Sample Rates
 - 24 Bits at 0.4ksps
 - 16 Bits at 4ksps
 - 12-Bit DAC
 - On-Die Temperature Sensor
 - Digital Peripherals
 - SPI (M/S)
 - Up to Two I²C
 - Up to Two UARTs
 - Up to 23 GPIOs
 - Timers
 - Up to Five 32-Bit Timers
 - Two Windowed Watchdog Timers
 - 8-Channel Standard DMA Controller
 - One I²S Slave for Digital Audio Interface
- Robust Security and Reliability
 - TRNG Compliant to SP800-90B
 - Secure Nonvolatile Key Storage and AES-128/192/256
 - Secure Bootloader to Protect IP/Firmware
 - Wide, -40°C to +105°C Operating Temperature Range

[Ordering Information](#) appears at end of data sheet.

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Simplified Block Diagram

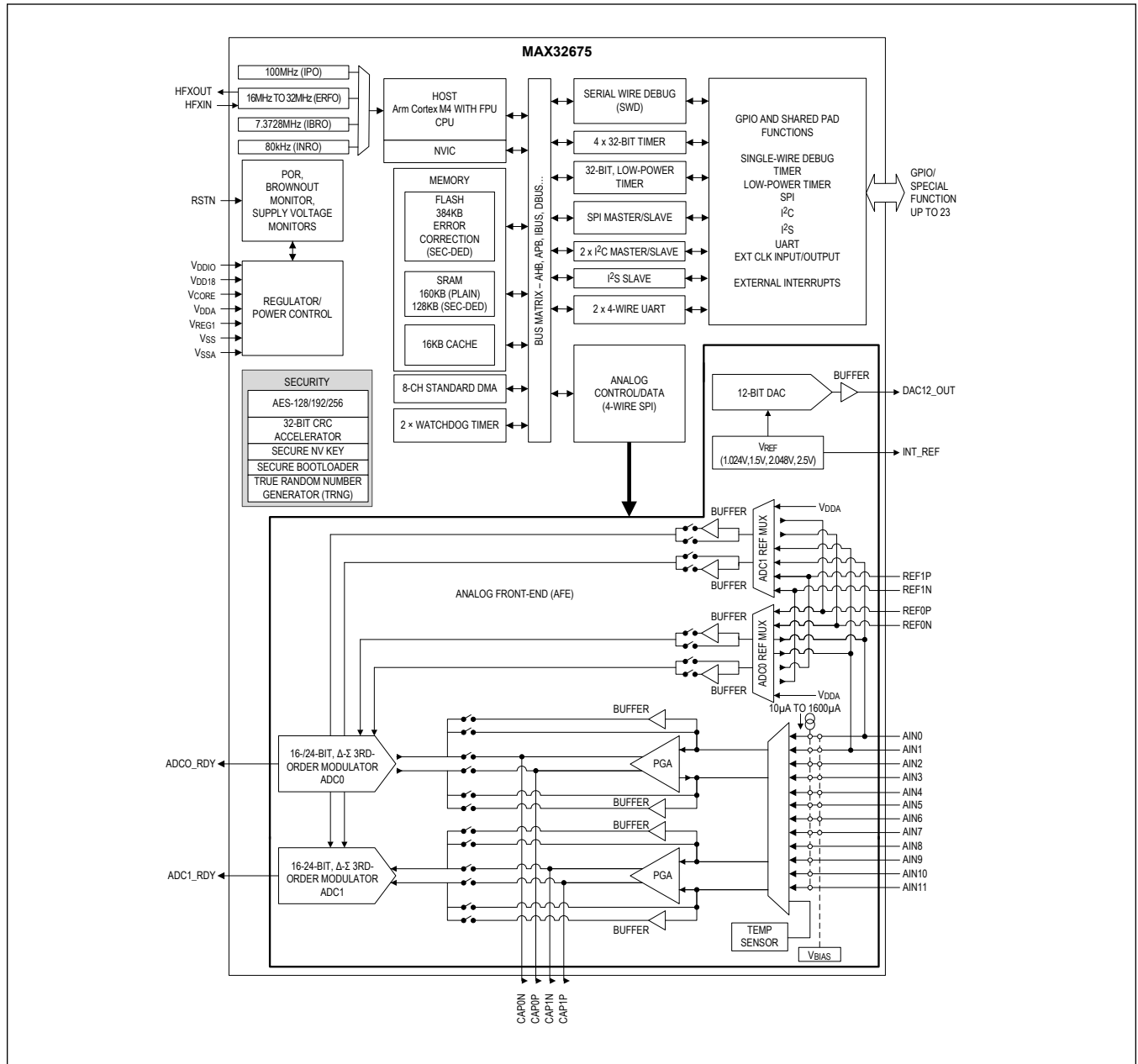


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Absolute Maximum Ratings

| | | |
|---|----------------------------|---|
| (All voltages with respect to V_{SS} , unless otherwise noted.) | V_{SS}, V_{SSA} | 100mA |
| V_{CORE} | -0.3V to +1.21V | Output Current (sink) by Any GPIO Pin |
| V_{DD18} | -0.3V to +1.98V | 25mA |
| $AIN[0-11]$ | -0.3V to $V_{DDA} + 0.3V$ | Output Current (source) by Any GPIO Pin |
| V_{DDIO}, V_{DDA} | -0.3V to +3.63V | -25mA |
| $HFXIN, HFXOUT$ | -0.3V to $V_{DDIO} + 0.3V$ | Continuous Package Power Dissipation 68 TQFN (multilayer board) $T_A = +70^{\circ}C$ (derate 45.21mW/ $^{\circ}C$ above +70 $^{\circ}C$) |
| $RSTN, GPIO, ADC0_RDY, ADC1_RDY$ | -0.3V to $V_{DDIO} + 0.3V$ | 3616.64mW |
| $REF1P, REF1N, REF0P, REF0N, VREG1, CAP1N, CAP1P, CAP0N, CAP0P, DAC12_OUT$ | -0.3V to $V_{DDA} + 0.3V$ | Operating Temperature Range |
| Total Current into All GPIO Combined (sink) | 100mA | -40 $^{\circ}C$ to +105 $^{\circ}C$ |
| | | Storage Temperature Range |
| | | -65 $^{\circ}C$ to +150 $^{\circ}C$ |
| | | Soldering Temperature (reflow) |
| | | +260 $^{\circ}C$ |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

68 TQFN

| | |
|--|-------------------------|
| Package Code | T6888MK+2 |
| Outline Number | 21-0510 |
| Land Pattern Number | 90-0354 |
| Thermal Resistance, Four-Layer Board: | |
| Junction to Ambient (θ_{JA}) | 22.12 $^{\circ}C/W$ |
| Junction to Case (θ_{JC}) | 0.7 $^{\circ}C/W$ |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(Limits are 100% tested at $T_A = +25^{\circ}C$ and $T_A = +105^{\circ}C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|--|-------|-----|-------|-------|
| POWER / BOTH SINGLE-SUPPLY AND MULTISUPPLY OPERATION | | | | | | |
| Supply Voltage, Digital | V_{DDIO} | The V_{DDIO} device pin must be connected to the V_{DDA} device pin. | 2.7 | 3.3 | 3.63 | V |
| | V_{DD18} | | 1.71 | 1.8 | 1.98 | |
| Supply Voltage, Core | V_{CORE} | OVR = [00] | 0.855 | 0.9 | 0.945 | V |
| | | OVR = [01] | 0.95 | 1.0 | 1.05 | |
| | | Default OVR = [10] | 1.045 | 1.1 | 1.155 | |
| Supply Voltage, Analog | V_{DDA} | The V_{DDIO} device pin must be connected to the V_{DDA} device pin. | 2.7 | 3.3 | 3.63 | V |
| Power-Fail Reset Voltage | V_{RST} | Monitors V_{DDIO} | 1.55 | | 2.4 | V |
| | | Monitors V_{CORE} during multisupply operation | 0.76 | | 0.86 | |
| Power-On-Reset (POR) Voltage | V_{POR} | Monitors V_{DDIO} | | 1.4 | | V |
| | | Monitors V_{CORE} during multisupply operation | | 0.6 | | |

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------|---|---|-----|------|-------------------|
| POWER / SINGLE-SUPPLY OPERATION (V_{DDIO} ONLY) | | | | | | |
| V_{DDIO} Current ACTIVE Mode | I_{DD_DACTS} | Dynamic, IPO enabled, total current into V_{DDIO} pin, $V_{DDIO} = 3.3\text{V}$, CPU in ACTIVE mode, executing Coremark, ECC disabled, inputs tied to V_{SS} or V_{DDIO} , outputs source/sink 0mA | OVR = [10], internal regulator set to 1.1V, $f_{SYS_CLK(MAX)} = 100\text{MHz}$ | | 64.5 | $\mu\text{A/MHz}$ |
| | | | OVR = [01], internal regulator set to 1.0V, $f_{SYS_CLK(MAX)} = 50\text{MHz}$ | | 62.5 | |
| | | | OVR = [00], internal regulator set to 0.9V, $f_{SYS_CLK(MAX)} = 12\text{MHz}$ | | 59.5 | |
| | | Dynamic, IPO enabled, total current into V_{DDIO} pin, $V_{DDIO} = 3.3\text{V}$, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DDIO} , outputs source/sink 0mA | OVR = [10], internal regulator set to 1.1V, $f_{SYS_CLK(MAX)} = 100\text{MHz}$ | | 49.4 | |
| | | | OVR = [01], internal regulator set to 1.0V, $f_{SYS_CLK(MAX)} = 50\text{MHz}$ | | 47 | |
| | | | OVR = [00], internal regulator set to 0.9V, $f_{SYS_CLK(MAX)} = 12\text{MHz}$ | | 44.1 | |
| | I_{DD_FACTS} | Fixed, IPO enabled, total current into V_{DDIO} pin, $V_{DDIO} = 3.3\text{V}$, CPU in ACTIVE mode, 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DDIO} , outputs source/sink 0mA | OVR = [10], internal regulator set to 1.1V | | 796 | μA |
| | | | OVR = [01], internal regulator set to 1.0V | | 647 | |
| | | | OVR = [00], internal regulator set to 0.9V | | 475 | |

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|---|--|--------------------------|------|--------|
| V _{DDIO} Current SLEEP Mode | I _{DD_DSLPS} | Dynamic, IPO enabled, total current into V _{DDIO} pin, V _{DDIO} = 3.3V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [10], internal regulator set to 1.1V | | 39.2 | μA/MHz |
| | | | OVR = [01], internal regulator set to 1.0V, f _{SYS_CLK(MAX)} = 50MHz | | 37.5 | |
| | | | OVR = [00], internal regulator set to 0.9V, f _{SYS_CLK(MAX)} = 12MHz | | 36.1 | |
| | | Dynamic, IPO enabled, total current into V _{DDIO} pin, V _{DDIO} = 3.3V, CPU in SLEEP mode, ECC disabled, DMA disabled, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [10], internal regulator set to 1.1V, f _{SYS_CLK(MAX)} = 100MHz | | 21.1 | |
| | | | OVR = [01], internal regulator set to 1.0V, f _{SYS_CLK(MAX)} = 50MHz | | 19 | |
| | | | OVR = [00], internal regulator set to 0.9V, f _{SYS_CLK(MAX)} = 12MHz | | 17.2 | |
| | I _{DD_FSLPS} | Fixed, IPO enabled, total current into V _{DDIO} pin, V _{DDIO} = 3.3V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [10], internal regulator set to 1.1V | | 796 | μA |
| | | | OVR = [01], internal regulator set to 1.0V | | 647 | |
| | | | OVR = [00], internal regulator set to 0.9V | | 475 | |
| | V _{DDIO} Fixed Current, DEEPSLEEP Mode | I _{DD_FDLSL} | Standby state with full data retention and 160KB SRAM retained | V _{DDIO} = 3.3V | | 4.0 |
| V _{DDIO} Fixed Current, BACKUP Mode | I _{DD_FBKUS} | V _{DDIO} = 3.3V | 0KB SRAM retained, retention regulator disabled | | 0.32 | μA |

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|-----------------------|--|------------------------|-----|-------|-----|-------|
| V _{DDIO} Fixed Current, BACKUP Mode | I _{DD_FBKUS} | V _{DDIO} = 3.3V | 20KB SRAM retained | | 1.04 | | μA |
| | | | 40KB SRAM retained | | 1.37 | | |
| | | | 80KB SRAM retained | | 1.90 | | |
| | | | 160KB SRAM retained | | 2.84 | | |
| V _{DDIO} Fixed Current, STORAGE Mode | I _{DD_FSTOS} | V _{DDIO} = 3.3V | | | 0.362 | | μA |
| SLEEP Mode Resume Time | t _{SLP_ONS} | | | | 2.1 | | μs |
| DEEPSLEEP Mode Resume Time | t _{DSL_ONS} | fast_wk_en = 1 | | | 89 | | us |
| | | fast_wk_en = 0 | | | 129 | | |
| BACKUP Mode Resume Time | t _{BKU_ONS} | Includes system initialization and ROM execution time | | | 1.25 | | ms |
| STORAGE Mode Resume Time | t _{STO_ONS} | Includes system initialization and ROM execution time | | | 1.5 | | ms |

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------------|---|--|-----|------|-------------------|
| POWER / MULTISUPPLY OPERATION | | | | | | |
| V_{CORE} Current, ACTIVE Mode | $I_{\text{CORE_DACTD}}$ | Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing Coremark, ECC disabled, inputs tied to V_{SS} or V_{DDIO} , outputs source/sink 0mA | OVR = [10], $V_{\text{CORE}} = 1.1\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 100\text{MHz}$ | | 63.7 | $\mu\text{A/MHz}$ |
| | | | OVR = [01], $V_{\text{CORE}} = 1.0\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 50\text{MHz}$ | | 61.9 | |
| | | | OVR = [00], $V_{\text{CORE}} = 0.9\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 12\text{MHz}$ | | 59.4 | |
| | | Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DDIO} , outputs source/sink 0mA | OVR = [10], $V_{\text{CORE}} = 1.1\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 100\text{MHz}$ | | 48.9 | |
| | | | OVR = [01], $V_{\text{CORE}} = 1.0\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 50\text{MHz}$ | | 46.6 | |
| | | | OVR = [00], $V_{\text{CORE}} = 0.9\text{V}$, $f_{\text{SYS_CLK(MAX)}} = 12\text{MHz}$ | | 44.5 | |
| | $I_{\text{CORE_FACTD}}$ | Fixed, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DDIO} , outputs source/sink 0mA | OVR = [10], $V_{\text{CORE}} = 1.1\text{V}$ | | 362 | μA |
| | | | OVR = [01], $V_{\text{CORE}} = 1.0\text{V}$ | | 217 | |
| | | | OVR = [00], $V_{\text{CORE}} = 0.9\text{V}$ | | 109 | |

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|---|---|------|--------|--------|
| V _{DDIO} Current, ACTIVE Mode | I _{DD_DACTD} | Dynamic, IPO enabled, total current into V _{DDIO} pin, V _{DDIO} = 3.3V, CPU in ACTIVE mode, executing Coremark, ECC disabled, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [10], f _{SYS_CLK(MAX)} = 100MHz | | 0.51 | μA/MHz |
| | | | OVR = [01], f _{SYS_CLK(MAX)} = 50MHz | | 0.51 | |
| | | | OVR = [00], f _{SYS_CLK(MAX)} = 12MHz | | 0.51 | |
| | | Dynamic, IPO enabled, total current into V _{DDIO} pin, V _{DDIO} = 3.3V, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [10], f _{SYS_CLK(MAX)} = 100MHz | | 0.51 | |
| | | | OVR = [01], f _{SYS_CLK(MAX)} = 50MHz | | 0.51 | |
| | | | OVR = [00], f _{SYS_CLK(MAX)} = 12MHz | | 0.51 | |
| | I _{DD_FACTD} | Fixed, IPO enabled, total current into V _{DDIO} pin, V _{DDIO} = 3.3V, CPU in ACTIVE mode, 0MHz execution, ECC disabled, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [10], V _{CORE} = 1.1V | | 367 | μA |
| | | | OVR = [01], V _{CORE} = 1.0V | | 367 | |
| | | | OVR = [00], V _{CORE} = 0.9V | | 307 | |
| I _{CORE_DSLPD} | Dynamic, IPO enabled, total current into V _{CORE} pin, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [10], V _{CORE} = 1.1V, f _{SYS_CLK(MAX)} = 100MHz | | 39.2 | μA/MHz | |

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|---------------------------------------|-------------------------|---|--|-----|------|--------|----|
| V _{CORE} Current, SLEEP Mode | I _{CORE_DSLPD} | Dynamic, IPO enabled, total current into V _{CORE} pin, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [01], V _{CORE} = 1.0V, f _{SYS_CLK(MAX)} = 50MHz | | 37.5 | μA/MHz | |
| | | | OVR = [00], V _{CORE} = 0.9V, f _{SYS_CLK(MAX)} = 12MHz | | 37 | | |
| | | Dynamic, IPO enabled, total current into V _{CORE} pin, CPU in SLEEP mode, ECC disabled, DMA disabled, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [10], V _{CORE} = 1.1V, f _{SYS_CLK(MAX)} = 100MHz | | 21.1 | | |
| | | | OVR = [01], V _{CORE} = 1.0V, f _{SYS_CLK(MAX)} = 50MHz | | 19.2 | | |
| | I _{CORE_FSLPD} | Fixed, IPO enabled, total current into V _{CORE} pin, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR [10], V _{CORE} = 1.1V | | 362 | | μA |
| | | | OVR [01], V _{CORE} = 1.0V | | 217 | | |
| | | | OVR [00], V _{CORE} = 0.9V | | 109 | | |
| | | | | | | | |

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|--------------------------|---|--|-------|-------|--------|----|
| V _{DDIO} Current, SLEEP Mode | I _{DD_DSLPD} | Dynamic, IPO enabled, total current into V _{DD} pin, V _{DDIO} = 3.3V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | | 0.001 | | μA/MHz | |
| | | Dynamic, IPO enabled, total current into V _{DDIO} pin, V _{DDIO} = 3.3V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [10], V _{CORE} = 1.1V, f _{SYS_CLK(MAX)} = 100MHz | | | | |
| | | Dynamic, IPO enabled, total current into V _{DDIO} pin, V _{DDIO} = 3.3V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [01], V _{CORE} = 1.0V, f _{SYS_CLK(MAX)} = 50MHz | | 0.001 | | |
| | I _{DD_FSLPD} | Fixed, IPO enabled, total current into V _{DDIO} pin, V _{DDIO} = 3.3V, CPU in SLEEP mode, ECC disabled, inputs tied to V _{SS} or V _{DDIO} , outputs source/sink 0mA | OVR = [00], V _{CORE} = 0.9V, f _{SYS_CLK(MAX)} = 12MHz | | 0.001 | | μA |
| | | | OVR = [10], V _{CORE} = 1.1V | | 367 | | |
| | | | OVR = [01], V _{CORE} = 1.0V | | 367 | | |
| V _{CORE} Fixed Current, DEEPSLEEP Mode | I _{CORE_FDSLPD} | V _{DDIO} = 3.3V, V _{CORE} = 1.1V | | 10 | | μA | |
| | | V _{DDIO} = 3.3V, V _{CORE} = 0.855V | | 3.8 | | | |
| V _{DD} Fixed Current, DEEPSLEEP Mode | I _{DD_FDSLPD} | V _{DDIO} = 3.3V, V _{CORE} = 1.1V | | 0.34 | | μA | |
| | | V _{DDIO} = 3.3V, V _{CORE} = 0.855V | | 0.34 | | | |

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | | | |
|--|---|--|---|--|---|---------------|-------|---------------|---------------|
| V_{CORE} Fixed Current, BACKUP Mode | $I_{\text{CORE_FBKUD}}$ | 0KB SRAM retained, retention regulator disabled | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 1.1\text{V}$ | | 0.225 | μA | | | |
| | | | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 0.855\text{V}$ | | 0.13 | | | | |
| | | 20KB SRAM retained | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 1.1\text{V}$ | | 1.256 | | | | |
| | | | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 0.855\text{V}$ | | 0.507 | | | | |
| | | 40KB SRAM retained | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 1.1\text{V}$ | | 2.243 | | | | |
| | | | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 0.855\text{V}$ | | 0.877 | | | | |
| | | 80KB SRAM retained | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 1.1\text{V}$ | | 3.97 | | | | |
| | | | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 0.855\text{V}$ | | 1.49 | | | | |
| | | 160KB SRAM retained | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 1.1\text{V}$ | | 7.22 | | | | |
| | | | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 0.855\text{V}$ | | 2.61 | | | | |
| | | V_{DDIO} Fixed Current, BACKUP Mode | $I_{\text{DD_FBKUD}}$ | 0KB SRAM retained, retention regulator disabled | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 1.1\text{V}$ | | | 0.34 | μA |
| | | | | | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 0.855\text{V}$ | | | 0.34 | |
| 20KB SRAM retained | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 1.1\text{V}$ | | | | 0.32 | | | | |
| | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 0.855\text{V}$ | | | | 0.32 | | | | |
| 40KB SRAM retained | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 1.1\text{V}$ | | | | 0.32 | | | | |
| | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 0.855\text{V}$ | | | | 0.108 | | | | |
| 80KB SRAM retained | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 1.1\text{V}$ | | | | 0.32 | | | | |
| | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 0.855\text{V}$ | | | | 0.32 | | | | |
| 160KB SRAM retained | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 1.1\text{V}$ | | | | 0.32 | | | | |
| | $V_{\text{DDIO}} = 3.3\text{V},$ $V_{\text{CORE}} = 0.855\text{V}$ | | | | 0.32 | | | | |
| V_{CORE} Fixed Current, STORAGE Mode | $I_{\text{CORE_FSTOD}}$ | | | $V_{\text{DDIO}} = 3.3\text{V}, V_{\text{CORE}} = 1.1\text{V}$ | | | 0.226 | μA | |
| | | | | $V_{\text{DDIO}} = 3.3\text{V}, V_{\text{CORE}} = 0.855\text{V}$ | | | 0.112 | | |
| V_{DDIO} Fixed Current, STORAGE Mode | $I_{\text{DD_FSTOD}}$ | $V_{\text{DDIO}} = 3.3\text{V}; V_{\text{CORE}} = 1.1\text{V}$ | | | 0.335 | μA | | | |
| | | $V_{\text{DDIO}} = 3.3\text{V}; V_{\text{CORE}} = 0.855\text{V}$ | | | 0.335 | | | | |

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------------|--|------------------------------|------|------------------------------|---------------|
| SLEEP Mode Resume Time | $t_{\text{SLP_OND}}$ | | | 2.1 | | μs |
| DEEPSLEEP Mode Resume Time | $t_{\text{DSL_OND}}$ | fast_wk_en = 1 | | 81 | | μs |
| | | fast_wk_en = 0 | | 129 | | |
| BACKUP Mode Resume Time | $t_{\text{BKU_OND}}$ | Includes system initialization and ROM execution time | | 1.25 | | ms |
| STORAGE Mode Resume Time | $t_{\text{STO_OND}}$ | Includes system initialization and ROM execution time | | 1.5 | | ms |
| GENERAL-PURPOSE I/O | | | | | | |
| Input Low Voltage for All GPIO, RSTN | $V_{\text{IL_GPIO}}$ | Pin configured as GPIO | | | $0.3 \times V_{\text{DDIO}}$ | V |
| Input High Voltage for All GPIO, RSTN | $V_{\text{IH_GPIO}}$ | Pin configured as GPIO | $0.7 \times V_{\text{DDIO}}$ | | | V |
| Output Low Voltage for All GPIO Except P0.6, P0.7, P0.13, P0.18, P0.19 | $V_{\text{OL_GPIO}}$ | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OL}} = 1\text{mA}$, DS[1:0] = 00 | | 0.2 | 0.4 | V |
| | | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OL}} = 2\text{mA}$, DS[1:0] = 10 | | 0.2 | 0.4 | |
| | | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OL}} = 4\text{mA}$, DS[1:0] = 01 | | 0.2 | 0.4 | |
| | | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OL}} = 6\text{mA}$, DS[1:0] = 11 | | 0.2 | 0.4 | |
| Output Low Voltage for GPIO P0.6, P0.7, P0.13, P0.18, P0.19 | $V_{\text{OL_I2C}}$ | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OL}} = 2\text{mA}$, DS = 0 | | 0.2 | 0.4 | V |
| | | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OL}} = 10\text{mA}$, DS = 1 | | 0.2 | 0.4 | |
| Output High Voltage for All GPIO Except P0.6, P0.7, P0.13, P0.18, P0.19 | $V_{\text{OH_GPIO}}$ | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OH}} = -1\text{mA}$, DS[1:0] = 00 | $V_{\text{DDIO}} - 0.4$ | | | V |
| | | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OH}} = -2\text{mA}$, DS[1:0] = 10 | $V_{\text{DDIO}} - 0.4$ | | | |
| | | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OH}} = -4\text{mA}$, DS[1:0] = 01 | $V_{\text{DDIO}} - 0.4$ | | | |
| | | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OH}} = -6\text{mA}$, DS[1:0] = 11 | $V_{\text{DDIO}} - 0.4$ | | | |
| Output High Voltage for GPIO P0.6, P0.7, P0.13, P0.18, and P0.19 | $V_{\text{OH_I2C}}$ | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OH}} = -2\text{mA}$, DS = 0 | $V_{\text{DDIO}} - 0.4$ | | | V |
| | | $V_{\text{DDIO}} = 2.7\text{V}$, $I_{\text{OH}} = -10\text{mA}$, DS = 1 | $V_{\text{DDIO}} - 0.4$ | | | |
| Combined I_{OL} , All GPIO | $I_{\text{OL_TOTAL}}$ | | | | 100 | mA |
| Combined I_{OH} , All GPIO | $I_{\text{OH_TOTAL}}$ | | -100 | | | mA |
| Input Hysteresis (Schmitt) | V_{IHYS} | | | 300 | | mV |
| Input/Output Pin Capacitance for All Pins | C_{IO} | | | 4 | | pF |
| Input Leakage Current Low | I_{IL} | $V_{\text{IN}} = 0\text{V}$, internal pullup disabled | -500 | | +500 | nA |
| Input Leakage Current High | I_{IH} | $V_{\text{IN}} = 3.6\text{V}$, internal pulldown disabled | -500 | | +500 | nA |

Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ\text{C}$ and $T_A = +105^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|----------------------|--|-----|------------------------|-----|---------|
| Input Pullup Resistor to RSTN | R _{PU_VDD} | Pullup to V _{DDIO} = V _{RST} , RSTN at V _{IH} | | 18.7 | | kΩ |
| | | Pullup to V _{DDIO} = 3.63V, RSTN at V _{IH} | | 10.0 | | |
| Input Pullup Resistor for All GPIO | R _{PU} | Device pin configured as GPIO, pullup to V _{DDIO} = V _{RST} , device pin at V _{IH} | | 18.7 | | kΩ |
| | | Device pin configured as GPIO, pullup to V _{DDIO} = 3.63V, device pin at V _{IH} | | 10.0 | | |
| Input Pulldown Resistor for All GPIO | R _{PD} | Device pin configured as GPIO, pulldown to V _{SS} , V _{DDIO} = V _{RST} , device pin at V _{IL} | | 17.6 | | kΩ |
| | | Device pin configured as GPIO, pulldown to V _{SS} , V _{DDIO} = 3.63V, device pin at V _{IL} | | 8.8 | | |
| CLOCKS | | | | | | |
| System Clock Frequency | f _{SYS_CLK} | | | | 100 | MHz |
| System Clock Period | t _{SYS_CLK} | | | 1/f _{SYS_CLK} | | μs |
| Internal Primary Oscillator (IPO) | f _{IPO} | Default OVR = [10] | | 100 | | MHz |
| External RF Oscillator (ERFO) | f _{ERFO} | Required crystal characteristics: C _L = 12pF, ESR ≤ 50Ω, C ₀ ≤ 7pF, temperature stability ±20ppm, initial tolerance ±20ppm | 16 | | 32 | MHz |
| Internal Baud Rate Oscillator (IBRO) | f _{IBRO} | | | 7.3728 | | MHz |
| Internal NanoRing Oscillator (INRO) | f _{INRO} | Measured at V _{DDIO} = 2.7V | | 70 | | kHz |
| External Clock | f _{EXT_CLK} | External clock selected (P0.10) | | | 25 | MHz |
| FLASH MEMORY | | | | | | |
| Flash Erase Time | t _{M_ERASE} | Mass erase | | 30 | | ms |
| | t _{P_ERASE} | Page erase | | 30 | | |
| Flash Programming Time Per Word | t _{PROG} | 32-bit programming mode, f _{FLC_CLK} = 1MHz | | 42 | | μs |
| Flash Endurance | | | 10 | | | kcycles |
| Data Retention | t _{RET} | T _A = +125°C | 10 | | | years |

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA

(V_{DDA} = +3.3V, REFP - REFN = V_{DDA}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|--------|------------|-----|-----------------------------|-----|-------|
| ANALOG INPUTS | | | | | | |
| Full-Scale Input Voltage | FS | | | ±V _{REF} / Gain | | |

Electrical Characteristics—16-/24-Bit Δ - Σ ADC with PGA (continued)

($V_{DDA} = +3.3V$, $REFP - REFN = V_{DDA}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------|----------|--|------------------------------------|----------|------------------------------------|-----------|
| Absolute Input Voltage | | Buffers disabled | $V_{SSA} - 30mV$ | | $V_{DDA} + 30mV$ | V |
| Input Voltage Range | | Unipolar | 0 | | V_{REF} | V |
| | | Bipolar | $-V_{REF}$ | | V_{REF} | |
| Common-Mode Voltage Range | V_{CM} | AIN buffers/PGA disabled | V_{SSA} | | V_{DDA} | V |
| | | Buffers enabled | $V_{SSA} + 0.1$ | | $V_{DDA} - 0.1$ | |
| | | PGA gain = 1 to 16 | $V_{SSA} + 0.1 + (V_{IN})(Gain)/2$ | | $V_{DDA} - 0.1 - (V_{IN})(Gain)/2$ | |
| | | PGA gain = 32 to 128 | $V_{SSA} + 0.2 + (V_{IN})(Gain)/2$ | | $V_{DDA} - 0.2 - (V_{IN})(Gain)/2$ | |
| Differential Input Current | | Buffer disabled | | ± 1 | | $\mu A/V$ |
| | | Buffer enabled | | 0 to 50 | | nA |
| | | PGA enabled | | ± 1 | | |
| Absolute Input Current | | Buffer disabled | | ± 1 | | $\mu A/V$ |
| | | Buffer enabled | | 20 to 80 | | nA |
| | | PGA enabled, $-40^\circ C$ to $+105^\circ C$ | -2 | | 2 | |
| Input Capacitance | | Bypass mode | | 10 | | pF |
| SYSTEM PERFORMANCE | | | | | | |
| Resolution | | | | 24 | | bits |

Electrical Characteristics—16-/24-Bit Δ - Σ ADC with PGA (continued)

($V_{DDA} = +3.3V$, $REFP - REFN = V_{DDA}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------|--|-----|---|-----|----------------|
| Data Rate | | 50hZ/60Hz FIR filter, single-cycle conversions | | 1, 2, 4, 8, 16 | | sps |
| | | 50Hz FIR filter, single-cycle conversions | | 1.3, 2.5, 5, 10, 20, 35.6 | | |
| | | 60Hz FIR filter, single-cycle conversions | | 1.3, 2.5, 5, 10, 20, 36.5 | | |
| | | SINC4 filter, single-cycle conversions | | 1, 2.5, 5, 10, 15, 30, 60, 120, 240, 480, 960, 1920 | | |
| | | SINC4 filter, continuous conversions | | 4, 10, 20, 40, 60, 120, 240, 480, 960, 1920, 3840, 7680 | | |
| | | SINC4 filter, duty cycle conversions | | 0.25, 0.0625, 1.25, 2.5, 3.75, 7.7, 15, 30, 60, 120, 240, 480 | | |
| Data Rate Tolerance | | Determined by internal clock accuracy | -6 | | 6 | % |
| Integral Nonlinearity (Note 2) | INL | Differential input, reference buffer enabled, PGA = 1, tested at 16sps, measured at $+25^\circ C$, $V_{DDA} = 3.3V$ | -12 | +2 | +12 | ppmFS |
| | | Differential input, PGA = 2 - 16 | | 6 | | |
| | | Differential input, PGA = 32 - 64 | | 11 | | |
| | | Differential input, PGA = 128 | | 15 | | |
| Offset Error | | Referred to modulator input. After self and system calibration; $V_{REFP} - V_{REFN} = 2.5V$, tested at 16sps, $V_{DDA} = 3.3V$ | -25 | ± 0.5 | +25 | μV |
| Offset Error Drift | | | | ± 50 | | nV/ $^\circ C$ |

Electrical Characteristics—16-/24-Bit Δ - Σ ADC with PGA (continued)

($V_{DDA} = +3.3V$, $REFP - REFN = V_{DDA}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------|--|-----------------|--------------------------------------|-----------------|----------------------|
| PGA Gain Settings | | | | 1, 2, 4, 8, 16, 32, 64, 128 | | |
| Digital Gain Settings | | | | 2, 4 | | |
| PGA Gain Error (<i>Note 1</i>) | | No calibration | | ± 0.3 | | % |
| | | Gain = 1, after calibration | -0.012 | | +0.012 | |
| PGA Gain Drift | | | | 32 | | ppmFS/ $^\circ C$ |
| Input Noise | V_n | FIR50Hz/60Hz, 16.8sps, PGA = 128 | | 208 | | nV _{RMS} |
| Noise-Free Resolution | NFR | FIR50Hz/60Hz, 16.8sps, PGA = 1 | | 17.3 | | bits |
| Normal-Mode Rejection (Internal Clock) | NMR | 50Hz/60Hz FIR filter, 50Hz $\pm 1\%$, 16sps conversion, GBD | | 88 | | dB |
| | | 50Hz/60Hz FIR filter, 60Hz $\pm 1\%$, 16sps single-cycle conversion, GBD | | 88 | | |
| | | 50Hz FIR filter, 50Hz $\pm 1\%$, 35.6sps single-cycle conversion, GBD | | 49 | | |
| | | 60Hz FIR filter, 60Hz $\pm 1\%$, 35.6sps single-cycle conversion, GBD | | 55.6 | | |
| | | SINC4 filter, 50Hz $\pm 1\%$, 10sps single-cycle conversion, GBD | | 88 | | |
| | | SINC4 filter 60Hz $\pm 1\%$, 10sps single-cycle conversion, GBD | | 91 | | |
| Normal-Mode Rejection (External Clock) | NMR | 50Hz/60Hz FIR filter, 50Hz or 60Hz $\pm 1\%$, 16sps single-cycle conversion | | 91 | | dB |
| | | 50Hz FIR filter, 50Hz $\pm 1\%$, 35.6sps single-cycle conversion | | 49.4 | | |
| | | 60Hz FIR filter, 60Hz $\pm 1\%$, 35.6sps single-cycle conversion | | 55.6 | | |
| | | SINC4 filter, 50Hz $\pm 1\%$, 10sps single-cycle conversion | | 92.4 | | |
| | | SINC4 filter, 60Hz $\pm 1\%$, 10sps single-cycle conversion | | 92.6 | | |
| Common-Mode Rejection | CMR | DC rejection, any PGA gain | | 100 | | dB |
| Common-Mode Rejection | CMR60 | 50Hz/60Hz rejection, PGA enabled | 104 | | | |
| Power Supply Rejection | PSRRA | | | 94 | | dB |
| REFERENCE INPUTS | | | | | | |
| Reference Voltage Range | | Reference buffer(s) disabled | $V_{SSA} - 30m$ | | $V_{DDA} + 30m$ | V |
| | | Reference buffer(s) enabled | $V_{SSA} + 0.1$ | | $V_{DDA} - 0.1$ | |

Electrical Characteristics—16-/24-Bit Δ - Σ ADC with PGA (continued)

($V_{DDA} = +3.3V$, $REFP - REFN = V_{DDA}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------|---|------|---|-----------------|-----------|
| Reference Voltage Input | | $V_{REF} = V_{REFP} - V_{REFN}$ | 0.75 | 2.5 | V_{DDA} | V |
| Reference Input Current | | Reference buffer disabled | | 2.1 | | $\mu A/V$ |
| | | Reference buffer enabled | -200 | 61 | +200 | nA |
| Reference Input Capacitance | | Reference buffers disabled | | 15 | | pF |
| MATCHED CURRENT SOURCES | | | | | | |
| Matched Current Source Outputs | | | | 10, 50, 75, 100, 125, 150, 175, 200, 225, 250, 300, 400, 600, 800, 1200, 1600 | | μA |
| Current Source Output Voltage Compliance | | IDAC $\leq 250\mu A$ | 0 | | $V_{DDA} - 0.7$ | V |
| | | IDAC = 1.6mA | 0 | | $V_{DDA} - 1.2$ | |
| Initial Tolerance | | $T_A = +25^\circ C$, GBD | -5 | ± 1 | +5 | % |
| Current Matching | | Between IDACs | | ± 0.1 | | % |
| Temperature Drift Matching | | Between IDACs | | 10 | | ppm/C |
| Current Source Output Noise | I_N | Output current = 250 μA ; SINC4 filter, 60sps continuous; noise is referred to input | | 0.47 | | pA rms |
| V_{BIAS} OUTPUTS | | | | | | |
| V _{BIAS} Voltage | | | | $V_{DDA}/2$ | | V |
| V _{BIAS} Voltage Output Impedance | | | | 125k (active), 20k (passive), 125k (passive) | | Ω |
| SYSTEM TIMING | | | | | | |
| Power-On Wake-Up Time | | From $V_{DDA} > V_{POR}$ | | 240 | | μs |
| PGA Power-Up Time | | $C_{FILTER} = 0$ | | 0.25 | | ms |
| | | $C_{FILTER} = 20nF$ | | 2 | | |
| | | $C_{FILTER} = 100nF$ | | 10 | | |

Electrical Characteristics—16-/24-Bit Δ - Σ ADC with PGA (continued)

($V_{DDA} = +3.3V$, $REFP - REFN = V_{DDA}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------|---|-----|------|-----|---------|
| PGA Settling Time | | After changing gain settings to Gain = 1, $C_{FILTER} = 0$ | | 0.25 | | ms |
| | | After changing gain settings to Gain = 1, $C_{FILTER} = 100nF$ | | 10 | | |
| | | After changing gain settings to Gain = 128, $C_{FILTER} = 0$ | | 2 | | |
| Input Multiplexer Power-Up Time | | Settled to 21 bits with 10pF load | | 2 | | μs |
| Input Multiplexer Channel-to-Channel Settling Time | | Settled to 21 bits with 2k Ω external source resistor | | 2 | | μs |
| V_{BIAS} Power-Up Time | | Active generator; settled within 1% of final value; $C_{LOAD} = 1\mu F$ | | 10 | | ms |
| | | 125K passive generator; settled within 1% of final value; $C_{LOAD} = 1\mu F$ | | 575 | | |
| | | 20K passive generator; settled within 1% of final value; $C_{LOAD} = 1\mu F$ | | 90 | | |
| V_{BIAS} Settling Time | | Active generator; settled within 1% of final value; $C_{LOAD} = 1\mu F$ | | 10 | | ms |
| | | 125K passive generator; settled within 1% of final value; $C_{LOAD} = 1\mu F$ | | 605 | | |
| | | 20K passive generator; settled within 1% of final value; $C_{LOAD} = 1\mu F$ | | 100 | | |
| Matched Current Source Startup Time | | | | 110 | | μs |
| Matched Current Source Settling Time | | | | 12.5 | | μs |

Electrical Characteristics—16-/24-Bit Δ - Σ ADC with PGA (continued)

($V_{DDA} = +3.3V$, $REFP - REFN = V_{DDA}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------|--------|--|--|-----|-----|---------|
| POWER SPECIFICATIONS | | | | | | |
| V_{DDA} Current | | ADC0 only | Standby mode, $V_{DDA} = V_{REF} =$ $V_{IN} = 3.3V$ | | 92 | μA |
| | | | Bypass mode, IDAC, V_{BIAS} sources off, V_{DDA} $= V_{REF} = V_{IN} =$ 3.3V, SINC4 filter, continuous conversions at 60sps | | 166 | |
| | | | Buffered mode, IDAC, V_{BIAS} sources off, V_{DDA} $= V_{REF} = V_{IN} =$ 3.3V, SINC4 filter, continuous conversions at 60sps | | 193 | |
| | | | PGA enabled, IDAC, V_{BIAS} sources off, V_{DDA} $= V_{REF} = V_{IN} =$ 3.3V, SINC4 filter, continuous conversions at 60sps | | 292 | |
| | | ADC1. ADC0 must be in Standby mode | Bypass mode, IDAC, V_{BIAS} sources off, V_{DDA} $= V_{REF} = V_{IN} =$ 3.3V, SINC4 filter, continuous conversions at 60sps | | 167 | |
| | | | Buffered mode, IDAC, V_{BIAS} sources off, V_{DDA} $= V_{REF} = V_{IN} =$ 3.3V, SINC4 filter, continuous conversions at 60sps | | 193 | |

Electrical Characteristics—16-/24-Bit Δ - Σ ADC with PGA (continued)

($V_{DDA} = +3.3V$, $REFP - REFN = V_{DDA}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------|--------|--|-----|-----|-----|-------|
| | | PGA enabled, IDAC, V_{BIAS} sources off, V_{DDA} $= V_{REF} = V_{IN} =$ 3.3V, SINC4 filter, continuous conversions at 60sps | | 292 | | |

Electrical Characteristics—16-/24-Bit Δ - Σ ADC with PGA (continued)

($V_{DDA} = +3.3V$, $REFP - REFN = V_{DDA}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---------------------------------|--------|--|--|-----|-----|-----|---------|
| V_{DDA} Duty Cycle Power Mode | | ADC0 only | Bypass mode, IDAC, V_{BIAS} sources off, $V_{DDA} = V_{REF} = V_{IN} = 3.3V$, SINC4 filter, continuous conversions at 15sps | | 74 | | μA |
| | | | Buffered mode, IDAC, V_{BIAS} sources off, $V_{DDA} = V_{REF} = V_{IN} = 3.3V$, SINC4 filter, continuous conversions at 15sps | | 89 | | |
| | | | PGA enabled, IDAC, V_{BIAS} sources off, $V_{DDA} = V_{REF} = V_{IN} = 3.3V$, SINC4 filter, continuous conversions at 15sps | | 196 | | |
| | | ADC1. ADC0 must be enabled in Standby mode | Bypass mode, IDAC, V_{BIAS} sources off, $V_{DDA} = V_{REF} = V_{IN} = 3.3V$, SINC4 filter, continuous conversions at 15sps | | 74 | | |
| | | | Buffered mode, IDAC, V_{BIAS} sources off, $V_{DDA} = V_{REF} = V_{IN} = 3.3V$, SINC4 filter, continuous conversions at 15sps | | 89 | | |
| | | | PGA enabled, IDAC, V_{BIAS} sources off, $V_{DDA} = V_{REF} = V_{IN} = 3.3V$, SINC4 filter, continuous conversions at 15sps | | 196 | | |

Electrical Characteristics—16-/24-Bit Δ - Σ ADC with PGA (continued)

($V_{DDA} = +3.3V$, $REFP - REFN = V_{DDA}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|--------|------------------------------------|------|-----|------|-------|
| LDO | | | | | | |
| V_{DD18} Output Capacitance | | | 100 | | | nF |
| V_{DD18} Output Voltage | | V_{DD18} configured as an output | 1.71 | 1.8 | 1.98 | V |

Electrical Characteristics—12-Bit DAC

($V_{DDA} = 3.3V$, $R_L = 10k\Omega$ and $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. $V_{REF} = 1.5V$. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------|-----------|--|-----------------|---------|-----------------|------------|
| Resolution | DAC_R | | 12 | | | bits |
| Differential Nonlinearity | DNL | Power mode = 2 or 3, noise filter enabled GBD | | ± 1 | | LSB |
| Integral Nonlinearity | INL | Power mode = 2 or 3, noise filter enabled GBD | | ± 1 | | LSB |
| Offset Error | E_O | Measure at $V_{DDA} = 3.3V$ | | 4 | | mV |
| Output Voltage Range | V_O | DAC12_OUT device pin; min code to max code, GBD | $V_{SSA} + E_O$ | | $V_{DDA} - 0.5$ | V |
| Output Impedance | | Power mode = 3 | | 6.1 | | k Ω |
| | | Power mode = 2 | | 8.9 | | |
| | | Power mode = 1 | | 16.3 | | |
| | | Power mode = 0 | | 97.7 | | |
| Voltage Output Settling Time | t_{SFS} | Noise filter enabled, code 400h to C00h, rising or falling, to ± 0.5 LSB | | 4 | | ms |
| | | Noise filter disabled, code 400h to C00h, rising or falling, to ± 0.5 LSB | | 0.03 | | |
| Glitch Energy | | Power mode = 0, 1, or 2 | | 12 | | V x ns |
| | | Power mode = 3, code 000h to A50h | | 12 | | |

Electrical Characteristics—12-Bit DAC (continued)

($V_{DDA} = 3.3V$, $R_L = 10k\Omega$ and $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. $V_{REF} = 1.5V$. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|----------------|-------------|-----------------------------|----------------|-----|-----|---------|---------|
| Active Current | I_{DAC12} | Static, $V_{REF} = 2.5V$ | Power mode = 3 | | 680 | | μA |
| | | | Power mode = 2 | | 570 | | |
| | | | Power mode = 1 | | 458 | | |
| | | | Power mode = 0 | | 347 | | |
| | | Static, $V_{REF} = 2.0V$ | Power mode = 3 | | 601 | | |
| | | | Power mode = 2 | | 509 | | |
| | | | Power mode = 1 | | 418 | | |
| | | | Power mode = 0 | | 327 | | |
| | | Static, $V_{REF} = 1.5V$ | Power mode = 3 | | 497 | | |
| | | | Power mode = 2 | | 431 | | |
| | | | Power mode = 1 | | 364 | | |
| | | | Power mode = 0 | | 297 | | |
| | | Static, $V_{REF} = 1.0V$ | Power mode = 3 | | 407 | | |
| | | | Power mode = 2 | | 361 | | |
| | | | Power mode = 1 | | 304 | | |
| | | | Power mode = 0 | | 284 | | |
| Power-On Time | | Excluding reference | | 10 | | μs | |

Electrical Characteristics—Internal Voltage Reference

($V_{DDA} = 3.3V$, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Internal reference mode, $4.7\mu F$ at INT_REF; $V_{REF} = 1.5V$. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|----------------|--|----------------|-----|---------------------------------|----------|-----------------|
| Output Voltage at INT_REF | V_{INT_REF} | $T_A = +25^\circ C$ | INT_REF 1.024V | | 1.024 | | V |
| | | | INT_REF 1.50V | | 1.500 | | |
| | | | INT_REF 2.048V | | 2.048 | | |
| | | | INT_REF 2.50V | | 2.500 | | |
| Internal Reference Temperature Coefficient | T_{CREF} | $T_A = -40^\circ C$ to $+105^\circ C$ | | | | ± 50 | ppm/ $^\circ C$ |
| Turn-On Time | t_{ON} | GBD | | | $0.1 + (INT_VR EF \times 1.8)$ | 10 | ms |
| Leakage Current with INT_REF Output Disabled | I_{INT_REF} | GBD | | | 15 | 50 | nA |
| INT_REF Line Regulation | | | | | ± 50 | | $\mu V/V$ |
| INT_REF Load Regulation | INT_Load | $I_{SOURCE} = 0$ to $500\mu A$, $T_A = +25^\circ C$ | | | 10 | | $\mu V/\mu A$ |

Electrical Characteristics—Internal Voltage Reference (continued)

($V_{DDA} = 3.3V$, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Internal reference mode, $4.7\mu F$ at INT_REF; $V_{REF} = 1.5V$. $T_A = +25^\circ C$ for typical specifications, unless otherwise noted. Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|--------|----------------|-----|-----|-----|---------|
| Reference Supply Current | | Buffer enabled | | 270 | | μA |

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------|--|-------------|-------------|-----|---------|
| MASTER MODE | | | | | | |
| SPI Master Operating Frequency | f_{MCK} | $f_{SYS_CLK} = 100MHz$, $f_{MCK(MAX)} = f_{SYS_CLK}/2$ | | | 50 | MHz |
| SPI Master SCK Period | t_{MCK} | | | $1/f_{MCK}$ | | ns |
| SCK Output Pulse-Width High/Low | t_{MCH} , t_{MCL} | | $t_{MCK}/2$ | | | ns |
| MOSI Output Hold Time After SCK Sample Edge | t_{MOH} | | $t_{MCK}/2$ | | | ns |
| MOSI Output Valid to Sample Edge | t_{MOV} | | $t_{MCK}/2$ | | | ns |
| MOSI Output Hold Time After SCK Low Idle | t_{MLH} | | | $t_{MCK}/2$ | | ns |
| MISO Input Valid to SCK Sample Edge Setup | t_{MIS} | | | 5 | | ns |
| MISO Input to SCK Sample Edge Hold | t_{MIH} | | | $t_{MCK}/2$ | | ns |
| SLAVE MODE | | | | | | |
| SPI Slave Operating Frequency | f_{SCK} | | | | 50 | MHz |
| SPI Slave SCK Period | t_{SCK} | | | $1/f_{SCK}$ | | ns |
| SCK Input Pulse-Width High/Low | t_{SCH} , t_{SCL} | | | $t_{SCK}/2$ | | |
| SSx Active to First Shift Edge | t_{SSE} | | | 10 | | ns |
| MOSI Input to SCK Sample Edge Rise/Fall Setup | t_{SIS} | | | 5 | | ns |
| MOSI Input from SCK Sample Edge Transition Hold | t_{SIH} | | | 1 | | ns |
| MISO Output Valid After SCLK Shift Edge Transition | t_{SOV} | | | 5 | | ns |
| SCK Inactive to SSx Inactive | t_{SSD} | | | 10 | | ns |
| SSx Inactive Time | t_{SSH} | | | $1/f_{SCK}$ | | μs |

Electrical Characteristics—SPI (continued)

(Timing specifications are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|-----------|------------|-----|-----|-----|-------|
| MISO Hold Time After SSx Deassertion | t_{SLH} | | | 10 | | ns |

Electrical Characteristics—I²C

(Timing specifications are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------------|--|------|-----|-----|---------|
| STANDARD MODE | | | | | | |
| Output Fall Time | t_{OF} | Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ | | 150 | | ns |
| SCL Clock Frequency | f_{SCL} | | 0 | | 100 | kHz |
| Low Period SCL Clock | t_{LOW} | | 4.7 | | | μ s |
| High Time SCL Clock | t_{HIGH} | | 4.0 | | | μ s |
| Setup Time for Repeated Start Condition | $t_{SU;STA}$ | | 4.7 | | | μ s |
| Hold Time for Repeated Start Condition | $t_{HD;STA}$ | | 4.0 | | | μ s |
| Data Setup Time | $t_{SU;DAT}$ | | | 300 | | ns |
| Data Hold Time | $t_{HD;DAT}$ | | | 10 | | ns |
| Rise Time for SDA and SCL | t_R | | | 800 | | ns |
| Fall Time for SDA and SCL | t_F | | | 200 | | ns |
| Setup Time for a Stop Condition | $t_{SU;STO}$ | | 4.0 | | | μ s |
| Bus Free Time Between a Stop and Start Condition | t_{BUS} | | 4.7 | | | μ s |
| Data Valid Time | $t_{VD;DAT}$ | | 3.45 | | | μ s |
| Data Valid Acknowledge Time | $t_{VD;ACK}$ | | 3.45 | | | μ s |
| FAST MODE | | | | | | |
| Output Fall Time | t_{OF} | From $V_{IH(MIN)}$ to $V_{IL(MAX)}$ | | 150 | | ns |
| Pulse Width Suppressed by Input Filter | t_{SP} | | | 75 | | ns |
| SCL Clock Frequency | f_{SCL} | | 0 | | 400 | kHz |
| Low Period SCL Clock | t_{LOW} | | 1.3 | | | μ s |
| High Time SCL Clock | t_{HIGH} | | 0.6 | | | μ s |
| Setup Time for Repeated Start Condition | $t_{SU;STA}$ | | 0.6 | | | μ s |
| Hold Time for Repeated Start Condition | $t_{HD;STA}$ | | 0.6 | | | μ s |

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------------|---|------|-----|------|-------|
| Data Setup Time | t _{SU;DAT} | | | 125 | | ns |
| Data Hold Time | t _{HD;DAT} | | | 10 | | ns |
| Rise Time for SDA and SCL | t _R | | | 30 | | ns |
| Fall Time for SDA and SCL | t _F | | | 30 | | ns |
| Setup Time for a Stop Condition | t _{SU;STO} | | 0.6 | | | μs |
| Bus Free Time Between a Stop and Start Condition | t _{BUS} | | 1.3 | | | μs |
| Data Valid Time | t _{VD;DAT} | | 0.9 | | | μs |
| Data Valid Acknowledge Time | t _{VD;ACK} | | 0.9 | | | μs |
| FAST MODE PLUS | | | | | | |
| Output Fall Time | t _{OF} | From V _{IH(MIN)} to V _{IL(MAX)} | | 80 | | ns |
| Pulse Width Suppressed by Input Filter | t _{SP} | | | 75 | | ns |
| SCL Clock Frequency | f _{SCL} | | 0 | | 1000 | kHz |
| Low Period SCL Clock | t _{LOW} | | 0.5 | | | μs |
| High Time SCL Clock | t _{HIGH} | | 0.26 | | | μs |
| Setup Time for Repeated Start Condition | t _{SU;STA} | | 0.26 | | | μs |
| Hold Time for Repeated Start Condition | t _{HD;STA} | | 0.26 | | | μs |
| Data Setup Time | t _{SU;DAT} | | | 50 | | ns |
| Data Hold Time | t _{HD;DAT} | | | 10 | | ns |
| Rise Time for SDA and SCL | t _R | | | 50 | | ns |
| Fall Time for SDA and SCL | t _F | | | 30 | | ns |
| Setup Time for a Stop Condition | t _{SU;STO} | | 0.26 | | | μs |
| Bus Free Time Between a Stop and Start Condition | t _{BUS} | | 0.5 | | | μs |
| Data Valid Time | t _{VD;DAT} | | 0.45 | | | μs |
| Data Valid Acknowledge Time | t _{VD;ACK} | | 0.45 | | | μs |

Electrical Characteristics—I²S

(Timing specifications are guaranteed by design and not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|--------------------|------------|---------------|-----|-----|---------------|
| Bit Clock Frequency | f_{BCLKS} | | | | 25 | MHz |
| Bit Clock Period | t_{BCLKS} | | $1/f_{BCLKS}$ | | | ns |
| BCLK High Time | $t_{WBCLKHS}$ | | | 0.5 | | $1/f_{BCLKS}$ |
| BCLK Low Time | $t_{WBCLKLS}$ | | | 0.5 | | $1/f_{BCLKS}$ |
| LRCLK Setup Time | t_{LRCLK_BCLKS} | | | 25 | | ns |
| Delay Time, BCLK to SD (Output) Valid | t_{BCLK_SDOS} | | | 12 | | ns |
| Setup Time for SD (Input) | t_{SU_SDIS} | | | 6 | | ns |
| Hold Time SD (Input) | t_{HD_SDIS} | | | 3 | | ns |

Note 1: Gain error does not include zero-scale errors. It is calculated as (full-scale error – offset error).

Note 2: ppmFS is parts per million of full scale.

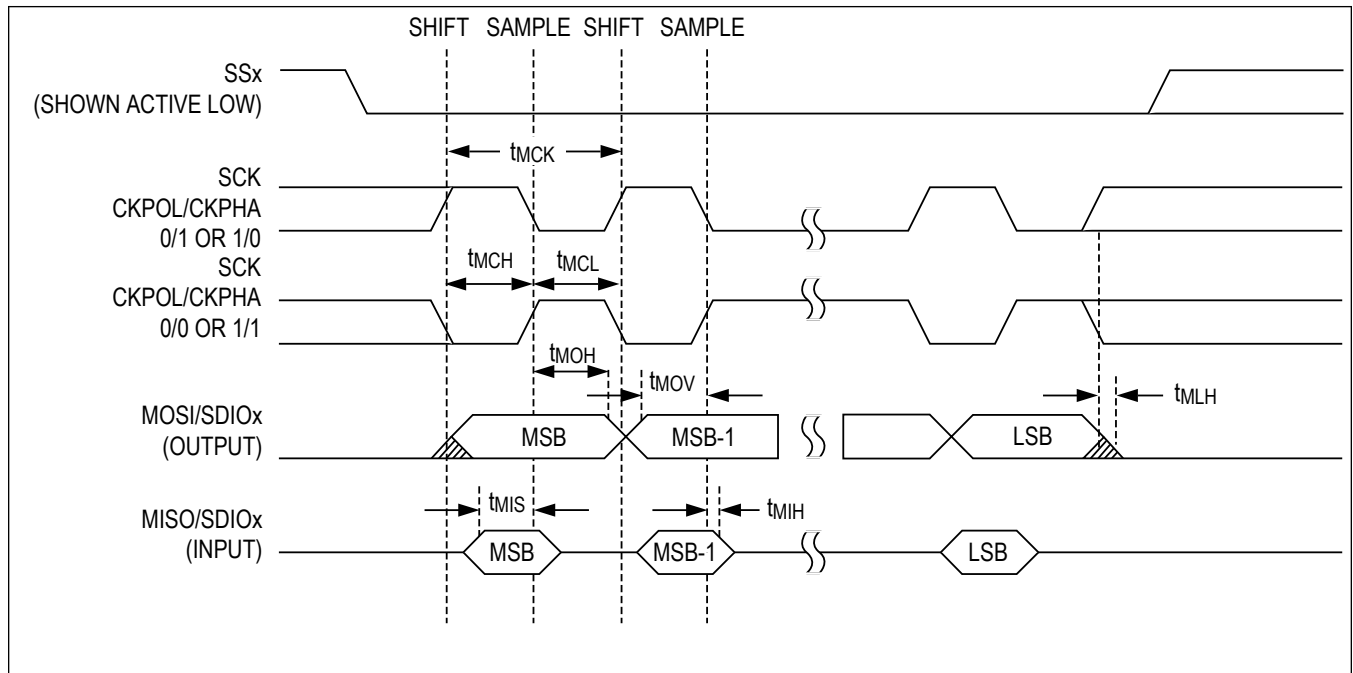


Figure 1. SPI Master Mode Timing Diagram

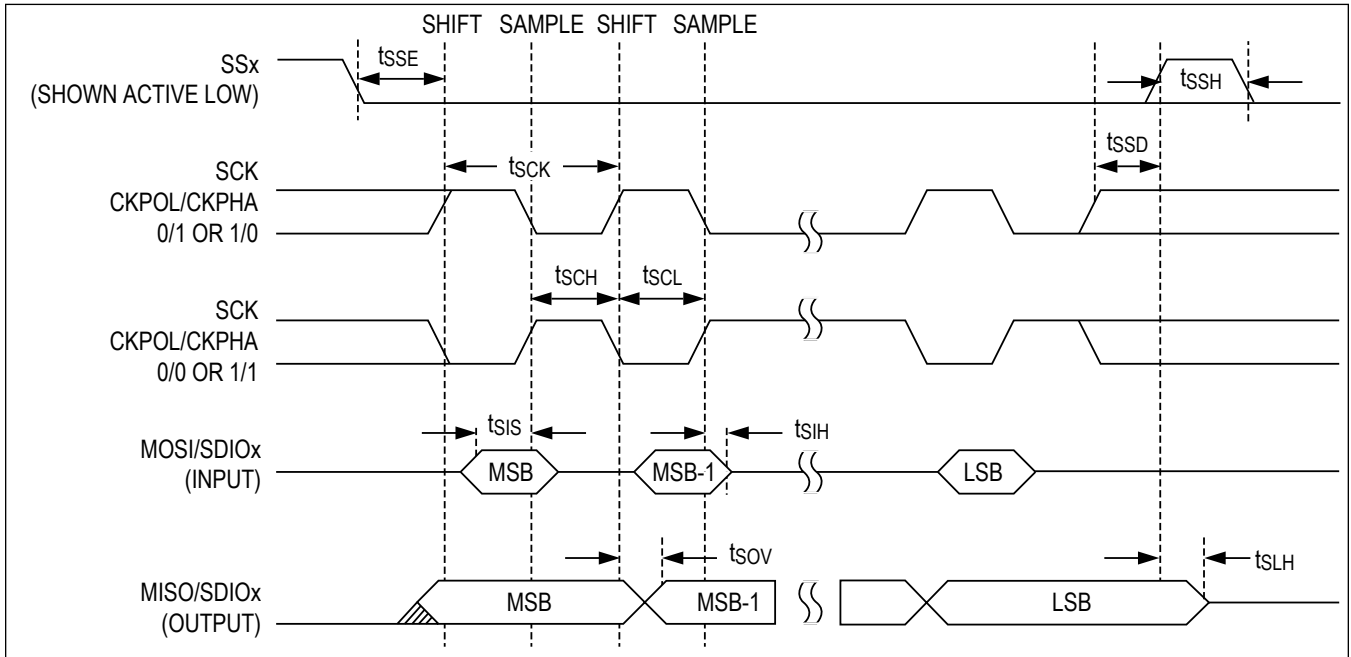


Figure 2. SPI Slave Mode Timing Diagram

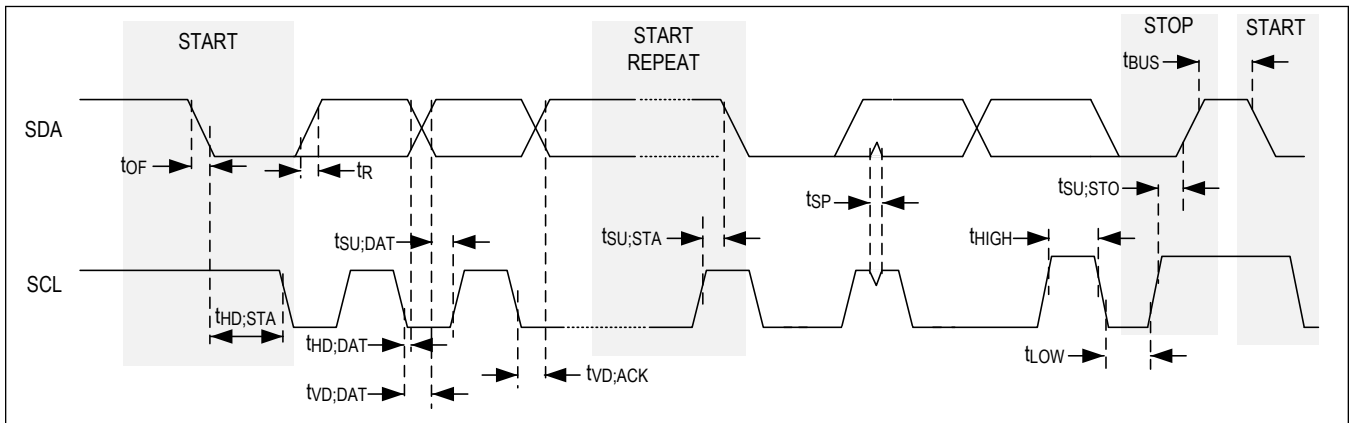


Figure 3. I²C Timing Diagram

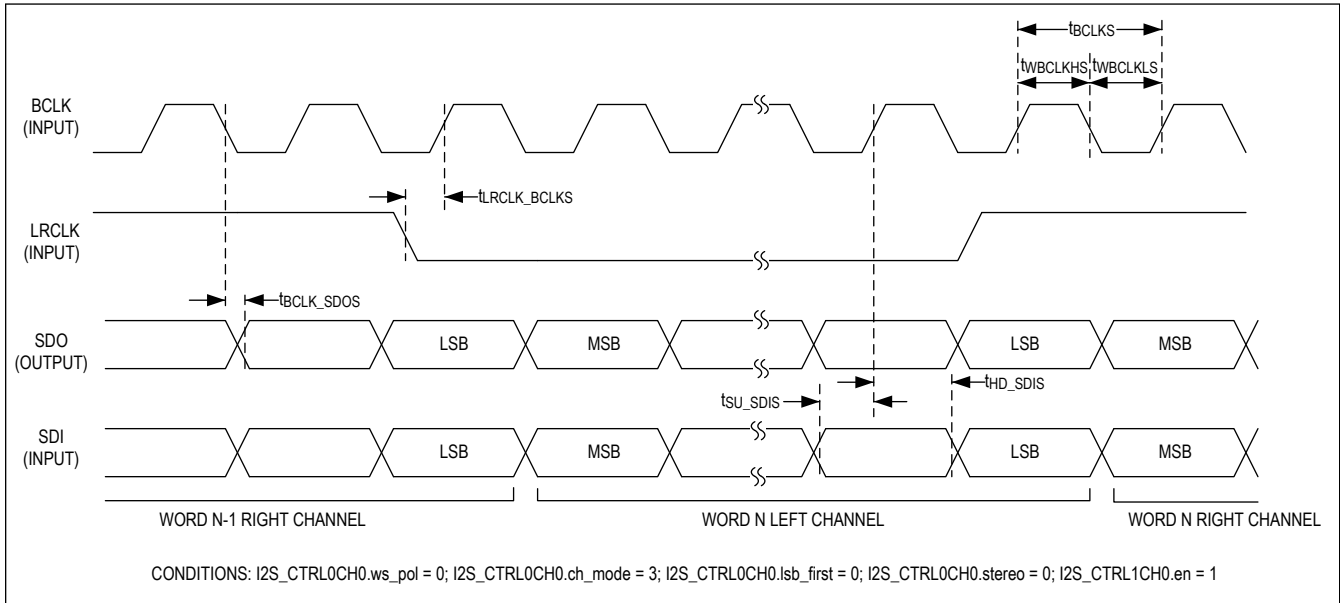
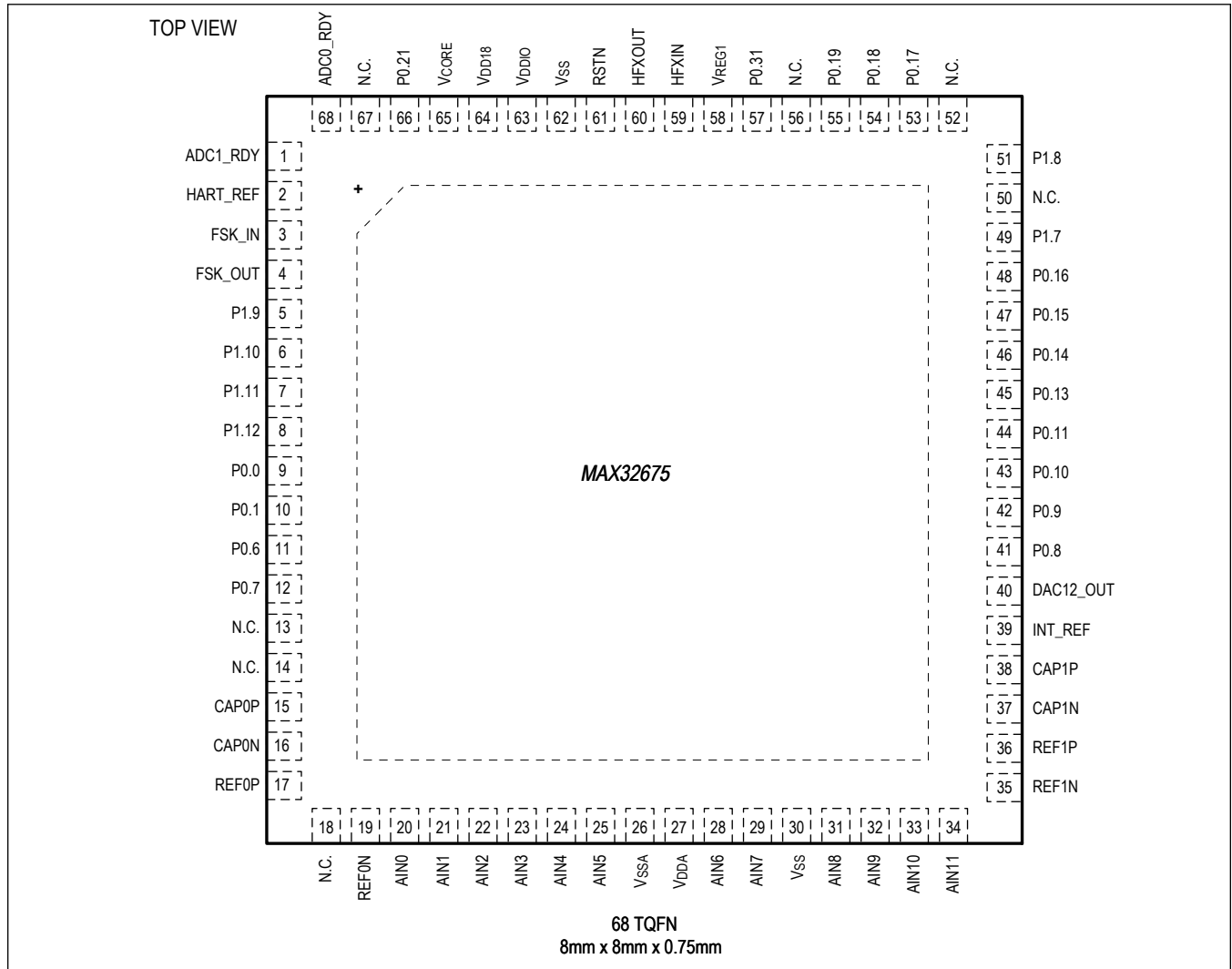


Figure 4. I²S Timing Diagram

Pin Configuration

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Pin Description

| PIN | NAME | FUNCTION MODE | | | | | FUNCTION |
|---|-------------------|--------------------------|----------------------|----------------------|----------------------|----------------------|--|
| | | Primary Signal (Default) | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Alternate Function 4 | |
| POWER (See the Applications Information section for bypass capacitor recommendations.) | | | | | | | |
| 65 | V _{CORE} | — | — | — | — | — | Digital Power-Supply Input. Bypass with 100nF to V _{SS} and 1µF with 10mΩ to 150mΩ ESR to V _{SS} . |

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| PIN | NAME | FUNCTION MODE | | | | | FUNCTION |
|--------------------------|-------------------|--------------------------|----------------------|----------------------|----------------------|----------------------|--|
| | | Primary Signal (Default) | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Alternate Function 4 | |
| 64 | V _{DD18} | — | — | — | — | — | This device pin can be configured as a LDO output or a voltage supply input. Bypass with 100nF to V _{SS} . Do not connect this device pin to any other external circuitry. |
| 63 | V _{DDIO} | — | — | — | — | — | Power Supply Input. This pin must always be connected to the V _{DDA} device pin at the PCB level. Bypass this pin with 100nF to V _{SS} and 1μF with 10mΩ to 150mΩ ESR to V _{SS} . |
| 27 | V _{DDA} | — | — | — | — | — | Analog Supply Voltage. This pin must always be connected to the V _{DDIO} device pin at the PCB level. Bypass this pin to V _{SSA} with 1.0μF and 0.01μF capacitors as close as possible to the package. |
| 58 | V _{REG1} | — | — | — | — | — | Bypass with 4.7nF to V _{SS} . Do not connect this device pin to any other external circuitry. |
| 30, 62 | V _{SS} | — | — | — | — | — | Digital Ground |
| 26 | V _{SSA} | — | — | — | — | — | Analog Ground |
| EP | Exposed Pad | — | — | — | — | — | Exposed Pad. This pad must be connected to V _{SS} . Refer to Application Note 3273: Exposed Pads: A Brief Introduction for additional information. |
| RESET AND CONTROL | | | | | | | |
| 61 | RSTN | — | — | — | — | — | Active-Low, External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies) and begins execution. This pin has an internal pullup to the V _{DDIO} supply. |
| CLOCK | | | | | | | |
| 59 | HFXIN | — | — | — | — | — | RF Crystal Oscillator Input. Connect the crystal between HFXIN and HFXOUT. Optionally, this pin can be configured as the input for an external square-wave source. See the Electrical Characteristics table for details of the crystal requirements. |

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| PIN | NAME | FUNCTION MODE | | | | | FUNCTION |
|--|----------|--------------------------|----------------------|----------------------|----------------------|----------------------|--|
| | | Primary Signal (Default) | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Alternate Function 4 | |
| 60 | HFXOUT | — | — | — | — | — | RF Crystal Oscillator Output. Connect the crystal between HFXIN and HFXOUT. See the Electrical Characteristics table for details of the crystal requirements. |
| N.A. | EXT_CLK | — | — | — | — | — | See Pin Description P0.10 for details. |
| 16-/24-BIT DELTA-SIGMA ADC WITH PGA | | | | | | | |
| 68 | ADC0_RDY | — | — | — | — | — | ADC0 Ready |
| 1 | ADC1_RDY | — | — | — | — | — | ADC1 Ready |
| 17 | REF0P | — | — | — | — | — | Positive Differential Reference 0 Input. REF0P must be more positive than REF0N. |
| 19 | REF0N | — | — | — | — | — | Negative Differential Reference 0 Input. REF0P must be more positive than REF0N. |
| 36 | REF1P | — | — | — | — | — | Positive Differential Reference 1 Input. REF1P must be more positive than REF1N. |
| 35 | REF1N | — | — | — | — | — | Negative Differential Reference 1 Input. REF1P must be more positive than REF1N. |
| 15 | CAP0P | — | — | — | — | — | ADC0 PGA Positive Output. Connect 1nF capacitor across CAP0P and CAP0N. |
| 16 | CAP0N | — | — | — | — | — | ADC0 PGA Negative Output. Connect 1nF capacitor across CAP0P and CAP0N. |
| 38 | CAP1P | — | — | — | — | — | ADC1 PGA Positive Output. Connect 1nF capacitor across CAP1P and CAP1N. |
| 37 | CAP1N | — | — | — | — | — | ADC1 PGA Negative Output. Connect 1nF capacitor across CAP1P and CAP1N. |
| 20 | AIN0 | — | — | — | — | — | Channel 0 Analog Input/Positive Differential Reference Input. When used as an analog input, may serve as either the positive or negative differential input. May also serve as current source output. When used as a reference input paired with AIN1, AIN0 must be more positive than AIN1. |

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| PIN | NAME | FUNCTION MODE | | | | | FUNCTION |
|-----|------|--------------------------|----------------------|----------------------|----------------------|----------------------|--|
| | | Primary Signal (Default) | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Alternate Function 4 | |
| 21 | AIN1 | — | — | — | — | — | Channel 1 Analog Input/Negative Differential Reference Input. When used as an analog input, may serve as either the positive or negative differential input. May also serve as current source output. When used as a reference input paired with AIN0, AIN0 must be more positive than AIN1. |
| 22 | AIN2 | — | — | — | — | — | Channel 2 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output. |
| 23 | AIN3 | — | — | — | — | — | Channel 3 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output. |
| 24 | AIN4 | — | — | — | — | — | Channel 4 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output. |
| 25 | AIN5 | — | — | — | — | — | Channel 5 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output. |
| 28 | AIN6 | — | — | — | — | — | Channel 6 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output. |
| 29 | AIN7 | — | — | — | — | — | Channel 7 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output. |
| 31 | AIN8 | — | — | — | — | — | Channel 8 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output. |
| 32 | AIN9 | — | — | — | — | — | Channel 9 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output. |

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| PIN | NAME | FUNCTION MODE | | | | | FUNCTION |
|------------------------------------|-----------|--------------------------|----------------------|----------------------|----------------------|----------------------|--|
| | | Primary Signal (Default) | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Alternate Function 4 | |
| 33 | AIN10 | — | — | — | — | — | Channel 10 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output. |
| 34 | AIN11 | — | — | — | — | — | Channel 11 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output. |
| 12-BIT DAC | | | | | | | |
| 40 | DAC12_OUT | — | — | — | — | — | 12-Bit DAC Analog Voltage Output |
| INTERNAL REFERENCE | | | | | | | |
| 39 | INT_REF | — | — | — | — | — | Internal Reference Output. It must be bypassed to V _{SSA} with a 4.7µF capacitor. |
| GPIO AND ALTERNATE FUNCTION | | | | | | | |
| 9 | P0.0 | P0.0 | SWDIO | — | TMR0C_IA | — | Single-Wire Debug I/O; Timer 0 Port Map C Input |
| 10 | P0.1 | P0.1 | SWDCLK | — | TMR0C_OA | — | Single-Wire Debug Clock; Timer 0 Port Map C Output |
| 11 | P0.6 | P0.6 | I2C0A_SCL | LPTMR0B_IA | TMR3C_IA | — | I ² C 0 Port Map A Serial Clock; Low-Power Timer 0 Port Map B Input 2 Bits or Lower 16 Bits; Timer 3 Port Map C Input 32 Bits or Lower 16 Bits |
| 12 | P0.7 | P0.7 | I2C0A_SDA | LPTMR0B_OA | TMR3C_OA | — | I ² C 0 Port Map A Serial Data; Low-Power Timer 0 Port Map B Output 32 Bits or Lower 16 Bits; Timer 3 Port Map C Output 32 Bits or Lower 16 Bits |
| 41 | P0.8 | P0.8 | UART0A_RX | I2S0B_SDO | TMR0C_IA | — | UART 0 Port Map A Rx; I ² S 0 Port Map B Serial Data Output; Timer 0 Port Map C Input 32 Bits or Lower 16 Bits |
| 42 | P0.9 | P0.9 | UART0A_TX | I2S0B_LRC_LK | TMR0C_OA | — | UART 0 Port Map A Tx; I ² S 0 Port Map B Left/Right Clock; Timer 0 Port Map C Output 32 Bits or Lower 16 Bits |

68 TQFN

| PIN | NAME | FUNCTION MODE | | | | | FUNCTION |
|-------------------|----------|--------------------------|----------------------|----------------------|----------------------|----------------------|---|
| | | Primary Signal (Default) | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Alternate Function 4 | |
| 43 | P0.10 | P0.10 | UART0A_CTS | I2S0B_BCLK | TMR1C_IA | EXT_CLK | UART 0 Port Map A CTS; I ² S 0 Port Map B Bit Clock; Timer 1 Port Map C Input 32 Bits or Lower 16 Bits. This pin can be used to source a clock signal. It can also be used to receive a clock signal. This clock signal can be used for the 16-/24-bit delta-sigma converters. See the Electrical Characteristics table for the External_Clock parameters. |
| 46 | P0.14 | P0.14 | SPI1A_MISO | UART2B_RX | TMR3C_IA | — | SPI 1 Port Map A Master In Slave Out; UART 2 Port Map B Rx; Timer 3 Port Map C Input 32 Bits or Lower 16 Bits |
| 47 | P0.15 | P0.15 | SPI1A_MOSI | UART2B_TX | TMR3C_OA | — | SPI 1 Port Map A Master Out Slave In; UART 2 Port Map B Tx; Timer 3 Port Map B Output 32 Bits or Lower 16 Bits |
| 48 | P0.16 | P0.16 | SPI1A_SCK | UART2B_CTS | TMR0C_IA | — | SPI 1 Port Map A Serial Clock; UART 2 Port Map B CTS; Timer 0 Port Map C Input 32 Bits or Lower 16 Bits |
| 51 | P1.8 | P1.8 | UART2A_RX | UART2B_RTS | — | — | UART2 Port Map A Rx; UART2 Port Map B RTS |
| 5 | P1.9 | P1.9 | UART2A_TX | — | — | — | UART 2 Port Map A Tx |
| 6 | P1.10 | P1.10 | UART2A_CTS | — | — | — | UART 2 Port Map A CTS |
| 7 | P1.11 | P1.11 | UART2A_RTS | — | TMR2C_OA | — | UART 2 Port Map A RTS; Timer 2 Port Map C Output 32 Bits or Lower 16 Bits |
| NO CONNECT | | | | | | | |
| 3 | FSK_IN | — | — | — | — | — | Do Not Connect. Internally connected. Do not make any electrical connection to this pin, including power supply grounds. |
| 4 | FSK_OUT | — | — | — | — | — | Do Not Connect. Internally connected. Do not make any electrical connection to this pin, including power supply grounds. |
| 2 | HART_REF | — | — | — | — | — | This pin must be connected to a 0.1μF capacitor. |

68 TQFN

| PIN | NAME | FUNCTION MODE | | | | | FUNCTION |
|--|------|--------------------------|----------------------|----------------------|----------------------|----------------------|--|
| | | Primary Signal (Default) | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Alternate Function 4 | |
| 13, 14, 18, 50, 52, 56, 67 | N.C. | — | — | — | — | — | No Connection. Not internally connected. |

Functional Diagrams

Power Supply Operational Modes

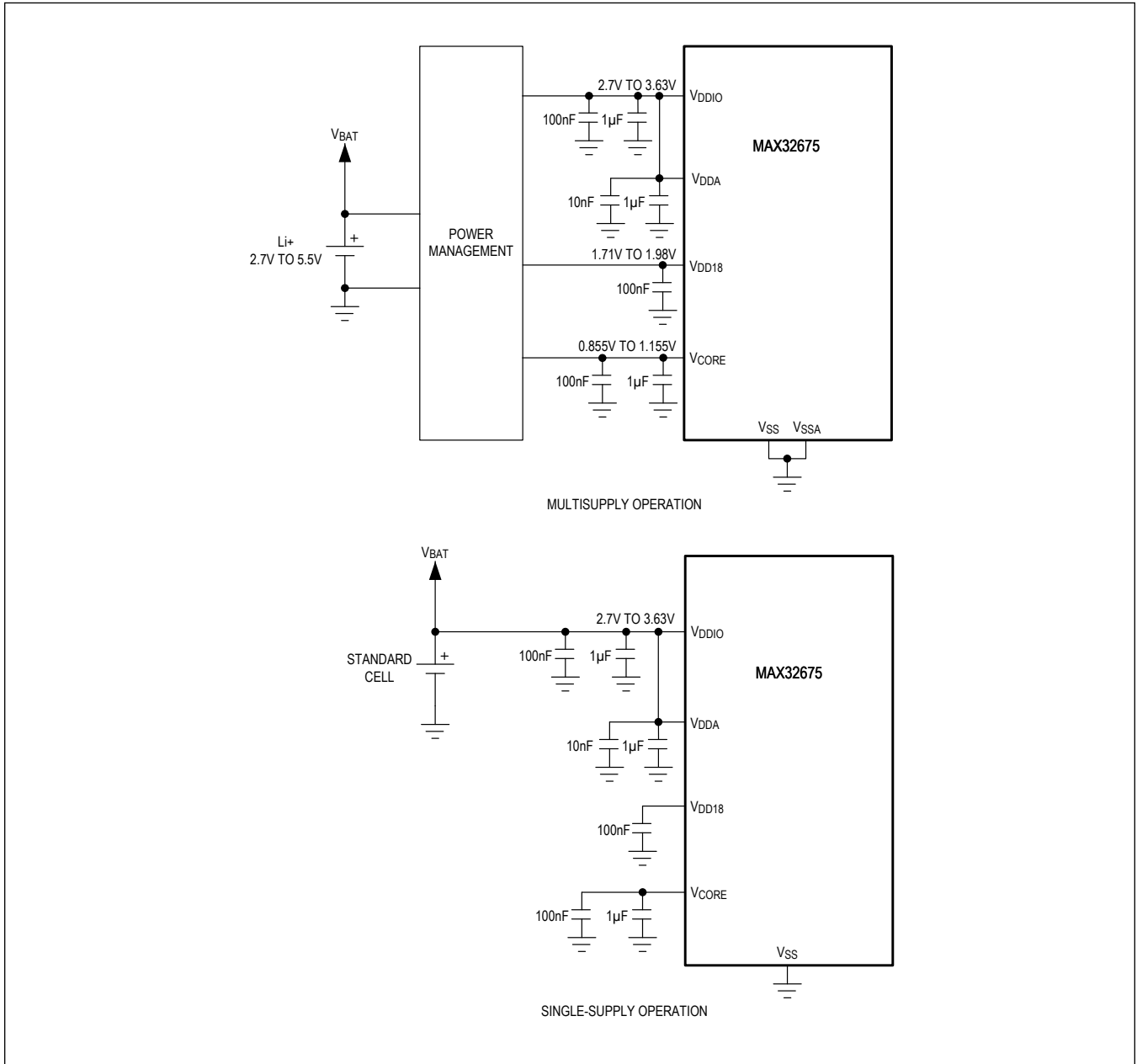


Figure 5. Power Supply Operation Modes

Detailed Description

The MAX32675 is a highly integrated, mixed-signal, ultra-low-power microcontroller for industrial applications and is especially suitable for 4-20mA loop-powered sensors and transmitters. It is based on an ultra-low-power Arm Cortex-M4 with FPU and includes 384KB of flash and 160KB of SRAM. ECC, capable of SEC-DED, is implemented over the entire flash, SRAM, and cache to ensure ultra-reliable code execution for demanding applications.

An AFE provides two 12-channel Δ - Σ ADCs with features and specifications that are optimized for precision sensor measurement. Each Δ - Σ ADC can digitize external analog signals as well as system temperature and supplies. A PGA with gains of 1x to 32x precedes each ADC. ADC outputs can be optionally converted on the fly from integer to single-precision floating-point format. A 12-bit DAC is also included. The integrated temperature sensor can be used with the internal sense element or an external diode for temperature compensation of sensor outputs.

The device also includes a trust protection unit (TPU), providing robust security features such as an AES engine, TRNG, and secure boot.

Arm Cortex-M4 Processor with FPU Engine

The Arm Cortex-M4 processor with FPU combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 processor with FPU supports single instruction multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed, unsigned, data with or without saturation

Memory

Internal Flash Memory

384KB of internal flash memory with error correction provides nonvolatile storage of program and data memory.

Internal SRAM

The internal 160KB SRAM provides low-power retention of application information in all power modes except STORAGE. For enhanced system reliability, the SRAM can be configured as 128KB with ECC single error correction, double error detection (SEC-DED). The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data retention feature is optional, and is configurable. This granularity allows the application to minimize its power consumption by only retaining the most essential data.

Clocking Scheme

Multiple clock sources can be selected as the system clock:

- Internal primary oscillator (IPO) at a nominal frequency of 100MHz
- Internal nanoring oscillator at 80kHz
- Internal baud rate oscillator at 7.3728MHz (IBRO)
- External RF oscillator at 16MHz to 32MHz (ERFO) (external crystal required)

The AFE is configured by SPIO and is clocked by the built-in Δ - Σ clock generation or the EXT_CLK signal. The APB clock or the INRO can clock the LPTMR0 in the AOD.

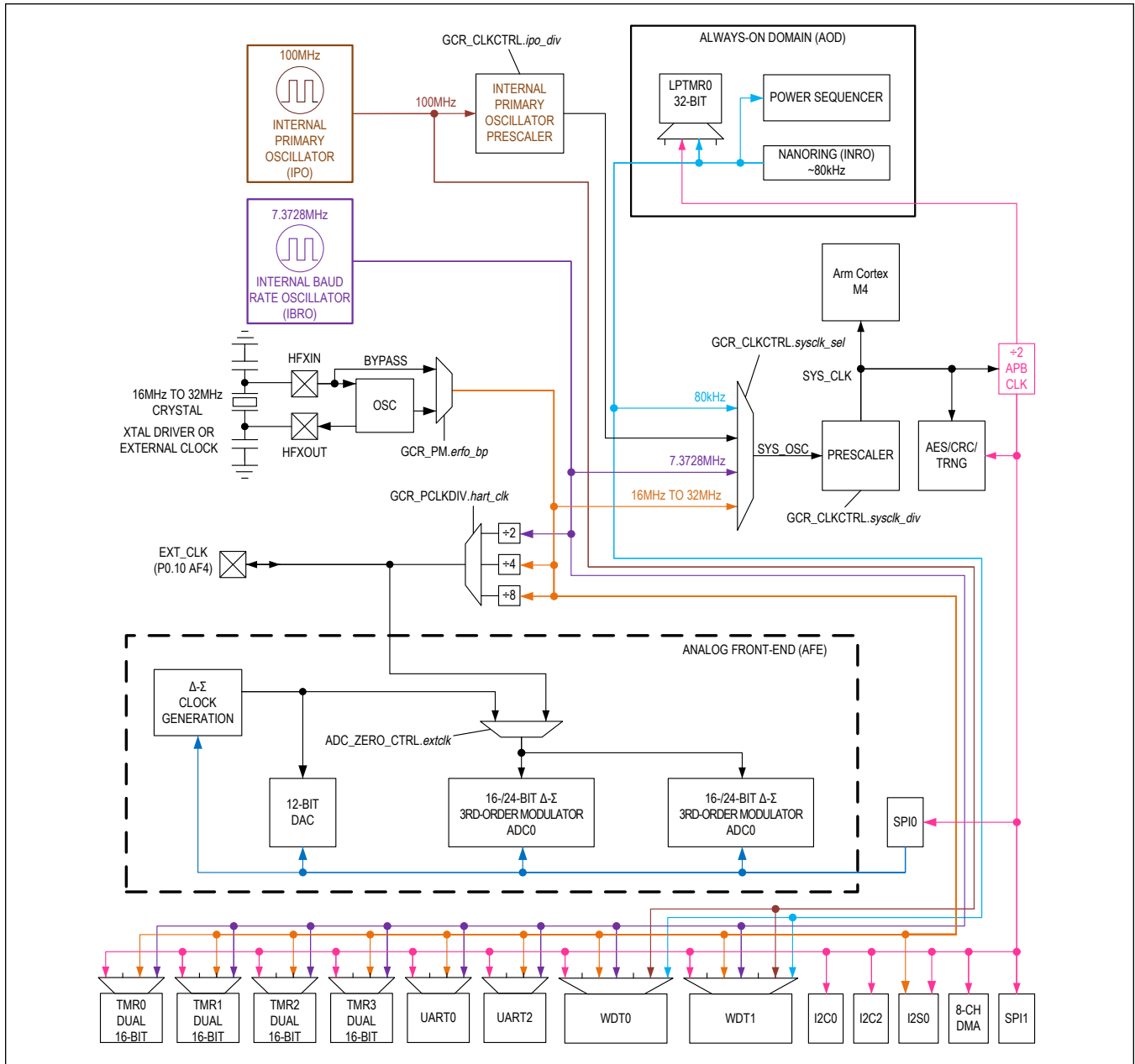


Figure 6. Clocking Scheme Diagram

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share both a firmware-controlled I/O function and one or more special function signals associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a firmware-controlled I/O. Though this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the [Electrical Characteristics](#) tables.

In GPIO mode, each pin of a port has an interrupt function that can be independently enabled and configured as a level-

or edge-sensitive interrupt. All GPIOs share the same interrupt vector. Some packages do not have all of the GPIOs available.

When configured as GPIOs, the following features are provided. These features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high-impedance
- Optional internal pullup resistor or internal pulldown resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32675 provides up to 23 GPIOs.

Power Management

Power Management Unit (PMU)

The PMU provides the optimal mix of high-performance and low-power consumption. It exercises intelligent, precise control of power distribution to the CPU and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple clock domains
- Fast wakeup of powered-down peripherals when activity detected

ACTIVE Mode

In this mode, the CPU is executing application code and all digital and analog peripherals are available on demand. Dynamic clocking disables local clocks in peripherals not in use. This mode corresponds to the Arm Cortex-M4 processor with FPU Active mode. The power mode of the AFE is software-controlled.

SLEEP Mode

This mode allows for lower power consumption operation than active mode. The CPU is asleep, peripherals are on, and the standard DMA block is available. The GPIO or any active peripheral can be configured to interrupt and cause transition to the ACTIVE mode. This mode corresponds to the Arm Cortex-M4 processor with FPU Sleep mode. The power mode of the AFE is software-controlled.

DEEPSLEEP Mode

In this mode, CPU and critical peripheral configuration settings and all volatile memory are preserved.

The device status is as follows:

- CPU is powered down. System state and all SRAM is retained.
- The GPIO pins retain their state.
- The transition from DEEPSLEEP to ACTIVE mode is faster than the transition from BACKUP mode because system initialization is not required.
- The system oscillators are all disabled to provide additional power savings over SLEEP mode.
- LPTMR0 can be active and are optional wake-up sources

This mode corresponds to the Arm Cortex-M4 with FPU DeepSleep mode. The power mode of the AFE is software-controlled.

BACKUP Mode

This mode places the CPU in a static, low-power state. The BACKUP mode supports the same wake-up sources as the DEEPSLEEP mode.

The device status is as follows:

- CPU is powered down.
- SRAM retention as per [Table 1](#). Each of the RAM blocks can be retained.

- LPTMR0 can be active and is an optional wake-up source.

The power mode of the AFE is software-controlled.

Table 1. BACKUP Mode RAM Retention

| RAM BLOCK | RAM SIZE WITHOUT ECC (KB) | RAM SIZE WITH ECC (KB) |
|-----------|---------------------------|------------------------|
| SYSRAM0 | 20 | 16 |
| SYSRAM1 | 20 | 16 |
| SYSRAM2 | 40 | 32 |
| SYSRAM3 | 80 | 64 |

STORAGE Mode

The device status is as follows:

- CPU is powered off.
- All peripherals are powered off.
- Wake-up from GPIO interrupt.
- No SRAM retention.

The power mode of the AFE is software-controlled.

Standard DMA Controller

The standard direct memory access (DMA) controller provides a means to offload the CPU for memory/peripheral data transfer leading to a more power-efficient system. It allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 8 channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

Windowed Watchdog Timer (WDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the windowed watchdog timer (WDT), which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WDT must be periodically reset by the application software. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution. The windowed timeout period feature provides more detailed monitoring of system operation, requiring the WDT to be reset within a specific window of time.

The WDT supports multiple clock option:

- 100MHz IPO
- 16MHz to 32MHz ERFO (external crystal required)
- 7.3728MHz IBRO
- 80kHz INRO
- PCLK

The MAX32675 provides two instances of the windowed watchdog timer (WDT0, WDT1).

32-Bit Timer/Counter/PWM (TMR, LPTMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generate pulse-width modulated (PWM) signals with minimal software interaction.

The timers provide the following features:

- 32-bit up/down auto-reload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating, or capture
- Timer output pin
- TMR0–TMR3 can be configured as 2 × 16-bit general-purpose timers
- Timer interrupt

The MAX32675 provides timer instances as shown in [Table 2](#). LPTMRx is capable of operation in the Low Power, SLEEP, DEEPSLEEP, and BACKUP modes.

I/O functionality is supported for all of the timers. Note that the function of a port can be multiplexed with other functions on the GPIO pins, so it might not be possible to use all the ports depending on the device configuration.

Table 2. Timer Configuration Options

| INSTANCE | SINGLE 32 BIT | DUAL 16 BIT | POWER MODE | CLOCK SOURCE | | | | |
|----------|---------------|-------------|------------------|--------------|------|------|------|------|
| | | | | AOD_PCLK | PCLK | IBRO | ERFO | INRO |
| TMR0 | Yes | Yes | ACTIVE SLEEP | No | Yes | Yes | Yes | No |
| TMR1 | Yes | Yes | ACTIVE SLEEP | No | Yes | Yes | Yes | No |
| TMR2 | Yes | Yes | ACTIVE SLEEP | No | Yes | Yes | Yes | No |
| TMR3 | Yes | Yes | ACTIVE SLEEP | No | Yes | Yes | Yes | No |
| LPTMR0 | Yes | No | ACTIVE SLEEP | Yes | No | No | No | Yes |
| | | | DEEPSLEEP BACKUP | No | | | | |

Serial Peripherals**I²C Interface (I2C)**

The I²C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many, or many-to-many communications medium. These engines support standard-mode, fast-mode, fast-mode plus, and high-speed mode I²C speeds. It provides the following features:

- Master or slave mode operation
 - Supports up to four different slave addresses in slave mode
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Transmit FIFO preloading
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates
 - Standard mode: 100kbps
 - Fast mode: 400kbps
 - Fast mode plus: 1000kbps

- High-speed mode: 3400kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

The MAX32675 provides I²C instances as shown in [Table 3](#).

Table 3. I²C Configuration Options

| INSTANCE |
|------------|
| I2C0, I2C2 |

Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a highly configurable, flexible, and efficient synchronous interface among multiple SPI devices on a single bus. The bus uses a single clock signal and multiple data signals and one or more slave select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either slave or master mode and provide the following features:

- SPI modes 0, 1, 2, 3 for single-bit communication
- 3- or 4-wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Multimaster mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Slave select assertion and de-assertion timing with respect to leading/trailing SCK edge

The MAX32675 provides SPI instances as shown in [Table 4](#).

Table 4. SPI Configuration Options

| INSTANCE | DATA | SLAVE SELECT LINES | MAXIMUM FREQUENCY MASTER MODE (MHz) | MAXIMUM FREQUENCY SLAVE MODE (MHz) |
|----------|----------------|--------------------|-------------------------------------|------------------------------------|
| SPI1 | 3 wire, 4 wire | 1 | 50 | 50 |

I²S Interface (I2S)

The I²S interface is a bidirectional, four-wire serial bus that provides serial communications for codecs and audio amplifiers compliant with the I²S Bus Specification, June 5, 1996. It provides the following features:

- Master and slave mode operation
- Support for 4 channels
- 8, 16, 24, and 32 bit frames
- Receive and transmit DMA support
- Wakeup on FIFO status (full/empty/threshold)
- Pulse density modulation support for receive channel
- Word-select polarity control
- First bit position selection
- Interrupts generated for FIFO status
- Receiver FIFO depth of 32 bytes
- Transmitter FIFO depth of 32 bytes

The MAX32675 provides one instance of the I²S peripheral (I2S0).

UART

The universal asynchronous receiver-transmitter (UART) interface supports full-duplex asynchronous communication

with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request to send (RTS) and clear to send (CTS) flow control signaling. Each instance is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 8-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun, and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th-bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The MAX32675 provides UART instances as shown in [Table 5](#).

Table 5. UART Configuration Options

| INSTANCE | POWER MODE | CLOCK SOURCE | | | | |
|--------------|------------|--------------|------|------|------|------|
| | | AOD_PCLK | PCLK | IBRO | ERFO | INRO |
| UART0, UART2 | ACTIVE | No | Yes | Yes | Yes | No |

16-/24-Bit Δ - Σ Analog-to-Digital Converter with Programmable Gain Amplifier

A low-power, multichannel, 24-bit Δ - Σ ADC has features and specifications optimized for the precision measurement of sensors and other analog signal sources. The architecture includes a low-noise programmable gain amplifier (PGA), low-power input buffers, programmable matched current sources, differential/single-ended input multiplexer, and integrated on-chip oscillator.

- PGA with Available Gains 1x to 128x
 - Very High Input Impedance
 - Optimizes Overall Dynamic Range
- Low-Power Input Buffers
 - Provide Input Isolation
- Selectable Reference
 - Internal Differential (V_{REF})
 - External Differential
- Programmable Current Sources
 - Bias for Resistive Sensors
 - 16 Current Levels Available
 - Detection of Broken Sensor Wires
- 12 Analog Inputs
 - 6 Differential or 12 Single Ended
- Sample Rates up to 61440 Samples per Second
- FIR Digital Filters
 - Provides Single-Cycle Settling in 16ms
 - 90dB of Noise Rejection at 50Hz and 60Hz
- On-Chip Clock Source
 - No External Components Required
- External Clock Capable
- Sample Ready Interrupts
 - ADC0_RDY and ADC1_RDY

The MAX32675 provides two instances of this ADC (ADC_ZERO, ADC_ONE) that share the multiplexed 12 analog inputs (AIN0–AIN11).

12-Bit Digital-to-Analog Converter

The 12-bit digital-to-analog (DAC) outputs a single-ended voltage. It can be set independently to generate either a static output voltage or to generate a series of preloaded sample outputs at a specified sample rate.

The 12-Bit DAC peripheral support the following features:

- Configurable clock rate and output sample rate.
- Selectable output voltage reference.
- Can be set to output a static voltage level, a preset number of samples at a configurable sample rate, or samples continuously at a configurable sample rate.
- Interpolation filter allows for linearly interpolated output samples to be generated between each pair of output samples (2 to 1, 4 to 1, or 8 to 1).
- DAC output samples are pulled from a FIFO allow continuous sample output generation.

Security

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in a dedicated flash to protect against tampering. Key generation and storage are transparent to the user.

True Random Number Generator (TRNG)

Random numbers are a vital part of a secure application. The TRNG provides random numbers for use as cryptographic seeds or strong encryption keys to ensure data privacy.

Software can use random numbers to trigger asynchronous events that result in nondeterministic behavior. This helps thwart replay attacks or key search approaches. A high-entropy source must continuously update an effective true random number generator (TRNG).

A physically unpredictable entropy source continuously drives the provided TRNG. It generates a 128-bit true random number in 128 system clock cycles.

The TRNG can support the system-level validation of many security standards such as FIPS 140-2, PCI-PED, and Common Criteria. Contact Maxim for details of compliance with specific standards.

CRC Module

A cyclic redundancy check (CRC) hardware module provides fast calculations and data integrity checks by application software. The CRC module supports the following polynomials:

- CRC-16-CCITT
- CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$)

Bootloader

The bootloader allows loading and verification of program memory through a serial interface. Features include:

- Bootloader interface through UART
- Program loading of Motorola™ SREC format files
- Permanent lock state prevents altering or erasing program memory
- Access to the USN for device or customer application identification
- Disable SWD interface to block debug access port functionality

Secure Boot

Following every reset, the device performs a secure boot to confirm that the root of trust has not been compromised. The secure boot verifies the integrity of the program memory to confirm it has not been modified or corrupted, ensuring the trustworthiness of the application software. An HMAC SHA-256 hash is performed over program memory and compared against a loaded value during the bootloader configuration process. If the two values match, the application software is considered valid, and the device begins code execution. Programs that fail the integrity check indicate intentionally or unintentionally corrupted or modified program memory. The device then transitions to safe mode, which prevents the execution of the customer code. During the development phase, the bootloader can be reactivated and a new, trusted program memory loaded. Devices with the secure boot feature also provide an optional challenge/response that authenticates before executing bootloader commands.

Debug and Development Interface (SWD)

The serial wire debug interface is used for code loading and ICE debug activities. All devices in mass production have the debugging/development interface enabled.

Applications Information

Bypass Capacitors

The proper use of bypass capacitors reduces noise generated by the IC into the ground plane. The [Pin Description](#) table indicates which pins should be connected to bypass capacitors, and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each pin/ball of the IC package. For example, if the pin description table shows four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Capacitors should be placed as close as possible to their corresponding device pins. Pins which recommend more than one value of capacitor per pin should place them in parallel with the lowest value capacitor first, closest to the pin.

Bootloader Activation

The device automatically tests the bootloader stimulus pins on any reset. If the stimulus pins are in the states shown in [Table 6](#), the device activates the bootloader and waits for the host to initiate communication. Once the bootloader is activated, the stimulus pins can be changed to any state. The bootloader is deactivated by performing another reset with the stimulus pins in their inactive state.

Table 6. Bootloader Activation Summary

| PART NUMBER | BOOTLOADER COMMUNICATION PORT | | ACTIVATION PINS |
|--------------|-------------------------------|------------------|------------------------|
| | RECEIVE | TRANSMIT | |
| All Versions | UART0A_RX (P0.8) | UART0A_TX (P0.9) | P0.8 (Low), P0.1 (Low) |

Ordering Information

| PART | FLASH (KB) | SRAM (KB) | BOOTLOADER | SECURE BOOT | DEFAULT OSCILLATOR AFTER POR | PIN-PACKAGE |
|---------------|------------|-----------|------------|-------------|------------------------------|-------------|
| MAX32675ATK+ | 384 | 160 | YES | YES | IPO | 68 TQFN |
| MAX32675ATK+T | 384 | 160 | YES | YES | IPO | 68 TQFN |

T = Tape and reel.

MAX32675

Ultra-Low-Power Arm Cortex-M4F with Precision
Analog Front-End for Industrial and Medical
Sensors

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|-----------------|---------------|
| 0 | 8/21 | Initial release | — |

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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