MAX22200

36V, 1A Octal Integrated Serial-Controlled Solenoid and Motor Driver

General Description

The MAX22200 is an octal 36V serial-controlled solenoid driver. Each channel features a low impedance (200mΩ typ) push-pull output stage with sink-and-source driving capability and up to $1A_{RMS}$ driving current. A serial interface (SPI) that also supports daisy-chain configurations is provided to individually control each channel.

The device half-bridges can be configured as low-side drivers or as high-side drivers. Moreover, pairs of half-bridges can be paralleled to double the driving current or can be configured as full-bridges to drive up to four latched valves (bi-stable valves) or four brushed DC motors.

Two control methods are supported: voltage drive regulation (VDR) and current drive regulation (CDR). In VDR, the device outputs a PWM voltage in which the duty cycle is programmed using SPI. For a given supply voltage and solenoid resistor, the output current is proportional to the programmed duty cycle. In CDR, an internal integrated lossless current sensing (ICS) circuit senses the output current and compares it with an internal programmable reference current.

For optimal power management in solenoid drive applications, the excitation drive level (I_{HIT}), the hold drive level (I_{HOLD}), and the excitation drive time (t_{HIT}) can be individually configured for each channel.

The MAX22200 features a full set of protections and diagnostic functions. This includes overcurrent protection (OCP), thermal shutdown (TSD), undervoltage Lockout (UVLO), open-load detection (OL), and detection of plunger movement (DPM). A fault indication pin ($\overline{FAULT}$) signals fault events and diagnostic information is stored in the FAULT register.

Due to the flexibility of use, the serial interface control, the high efficiency, and the small package, the MAX22200 is particularly well-suited for solenoid driver applications (valve control, relays control etc.) in which low power consumption and high level of integration are required.

The MAX22200 is available in a compact 5mm x 5mm, 32-pin TQFN package and operates over the temperature -40ºC to +85ºC range.

Applications

- Relays Driver
- Solenoid, Valves, Electromagnetic Drivers
- Generic Low-Side and High-Side Switch Applications
- Latched (Bi-Stable) Solenoid Valve Drivers
- Brushed DC Motor Driver

Benefits and Features

- Eight Half-Bridges Up To +36V
- High Performances:
  - Low On-Resistance: $R_{DS(on)}$: 200 mΩ typical (T_A = +25°C)
  - Continuous Output Current Up To $1A_{RMS}$ per Half-Bridge (T_A = +25°C)
  - Current-Drive Regulation (CDR)
  - Voltage-Drive Regulation (VDR)
  - Integrated Lossless Current Sensing (ICS)
- High Flexibility:
  - Independent Programmable HIT and HOLD Currents for Each Channel (I_{HIT}, I_{HOLD})
  - Independent Programmable HIT Current Timing for Each Channel (t_{HIT})
  - Full-Bridge Configuration Supported
  - Parallel Mode Supported
- High Speed Serial Interface (SPI)
  - 5MHz Daisy-Chain Configuration
  - 10MHz without Daisy Chain
- Protections and Diagnostic
  - Overcurrent Protection (OCP)
  - Open-Load Detection (OL)
  - Detection of Plunger Movement (DPM)
  - Undervoltage Lockout (UVLO)
  - HIT Current Not Reached (HHF)
  - Thermal Shutdown T = +145°C (TSD)
  - Fault Registers for Diagnostic purposes
- Integration:
  - 32 TQFN 5mm x 5mm Package

***Ordering Information* appears at end of datasheet.**

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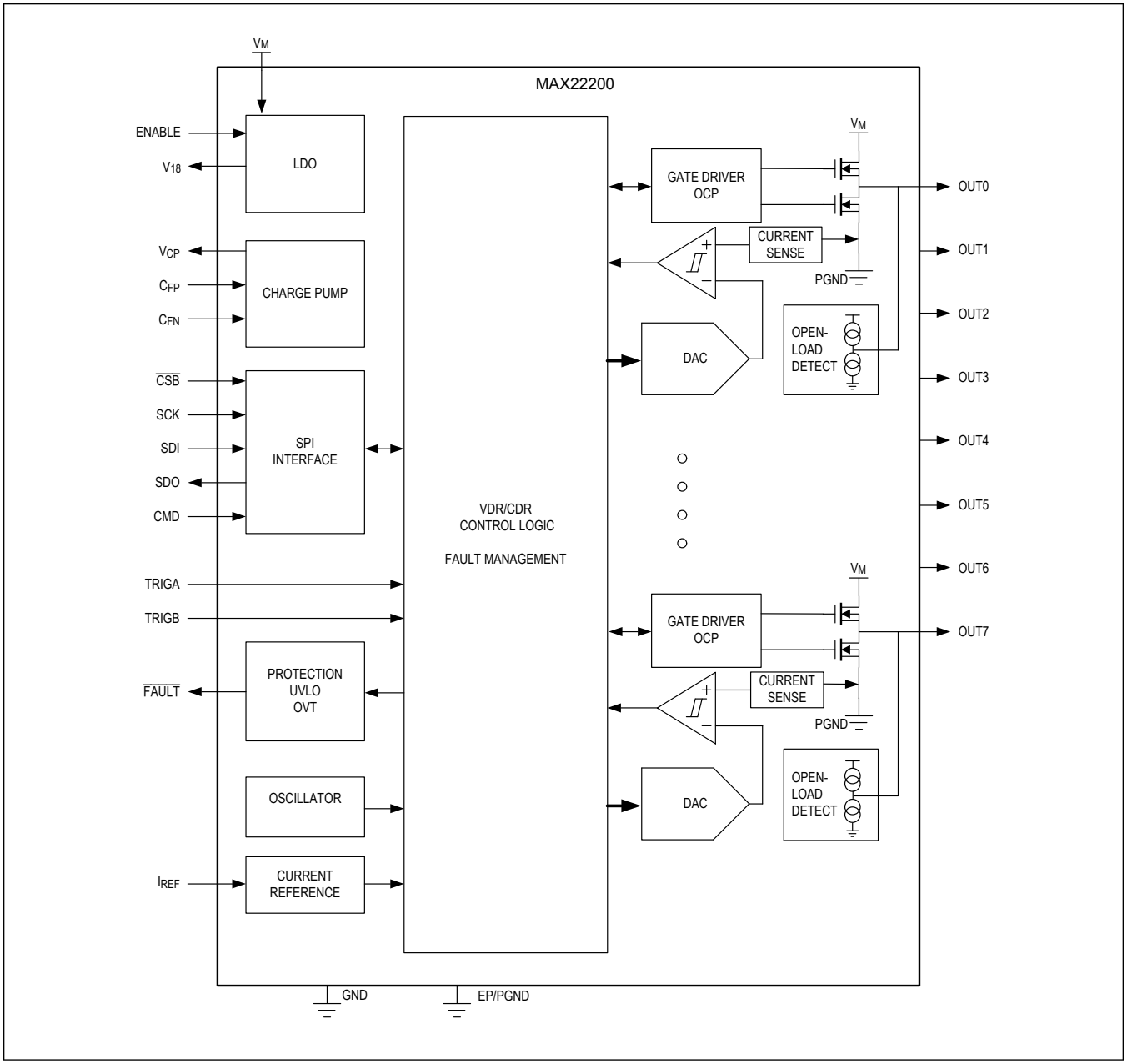
Simplified Block Diagram



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Absolute Maximum Ratings

PGND to GND ..... -0.6V to +0.6V
V_M to GND ..... -0.3V to +40V
V_{CP} to GND..... (V_M - 0.3V) to min(+42V, V_M + 6V)
C_{FP} to GND.....(V_M - 0.3V) to (V_{CP} + 0.3V)
C_{FN} to GND.....-0.3V to (V_M + 0.3V)
$\overline{CMD}$ to GND ..... -0.3V to +6V
$\overline{CSB}$ to GND ..... -0.3V to +6V
SDI to GND..... -0.3V to +6V
ENABLE to GND .....-0.3V to (V_M + 0.3V)
SCK to GND ..... -0.3V to +6V
$\overline{SDO}$ to GND .....-0.3V to +6V
$\overline{FAULT}$ to GND.....-0.3V to +6V
TRIGA, TRIGB to GND .....-0.3V to +6V
I_{REF} to GND..... -0.3V to min(+2.2V, V_{18} + 0.3V)
V_{18} to GND ..... -0.3V to min(+2.2V, V_M + 0.3V)
OUT_ to PGND ..... -0.3V to (V_M + 0.3V)
Continuous Power Dissipation TQFN (Multilayer Board) (T_A = +70°C, derate 34.5mW/°C above +70°C.)..... 0mW to 2758mW
Operating Temperature Range .....-40°C to +85°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 TQFN

Package Code	T3255+8C
Outline Number	21-0140
Land Pattern Number	90-0013
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	47°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.7°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	29°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.7°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

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Electrical Characteristics

(V_M = +4.5V to +36V, T_A = -40°C to +85°C. ENABLE = V_M, C_F = 22nF, C_{B18} = 2.2µF, C_T = 1µF. Typical values are at V_M = +24V and T_A = +25°C, unless otherwise noted. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
Supply-Voltage Range	V_M		4.5		36	V
Disable Current Consumption	I_{SDN}	ENABLE = 0, V_M = OUT_ = +24V			11	µA
Inactive Current Consumption	I_{NA}	ACTIVE = 0		200	400	µA

Electrical Characteristics (continued)

(V_M = +4.5V to +36V, T_A = -40°C to +85°C. ENABLE = V_M, C_F = 22nF, C_{B18} = 2.2µF, C_T = 1µF. Typical values are at V_M = +24V and T_A = +25°C, unless otherwise noted. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current Consumption–All Drivers Off	I_{Q1}	All drivers set in VDR Mode–Off			2.5	5	mA
Quiescient Current–All Drivers VDR Mode	I_{Q2}	All drivers set in VDR Mode–Continuous On, low-side, no load.			3.5	5	mA
Quiescent Current Consumption–CDR Mode	I_{Q3}	All drivers set in CDR Mode–Continuous On, no load			5.2	7.5	mA
LDO (V_{18})							
V_{18} Output Voltage Range	V_{18}	I_{V18} < 20mA		1.728	1.8	1.872	V
V_{18} Current Limit	$I_{V18(LIM)}$			20			mA
V_{18} UVLO Rising	$UVLO_{V18(R)}$	V_{18} rising			1.65		V
V_{18} UVLO Hysteresis	$UVLO_{V18(H)}$				70		mV
CHARGE PUMP (V_{CP}, C_{PF}, C_{NF})							
V_{CP} Operating Voltage	V_{VCP}	Internal Regulator			V_M + 2.7		V
Charge Pump Frequency	f_{PMP}				100		kHz
LOGIC INPUTS-OUTPUTS							
Input-Voltage Level High	V_{IH}			1.2			V
Input-Voltage Level Low	V_{IL}					0.65	V
Hysteresis on Logic Inputs	HYS				110		mV
Open-Drain Low-Level Output Voltage	V_{OL}	I_{OUT} = 10mA				0.4	V
Pulldown Current on Logic Inputs	I_{PD}	V_{PIN} = +5V			33	70	µA
Pullup Current $\overline{CSB}$/SDI	I_{PU}	$\overline{CSB}$/SDI = 0V		-15	-7.5		µA
ENABLE Voltage Level High	$V_{IH(EN)}$			0.9			V
ENABLE Voltage Level Low	$V_{IL(EN)}$					0.6	V
ENABLE Pulldown Input Resistance	$R_{PD(EN)}$			0.8	1.5		MΩ
OUTPUT CHARACTERISTICS							
Low-Side On Resistance	R_{ONLS}	0.5A	HFS_ = 0		0.2	0.4	Ω
			HFS_ = 1		0.4	0.8	
High-Side On resistance	R_{ONHS}	0.3A			0.21	0.4	Ω
Driver Output Leakage	I_{LEAK}	Open load detector disabled (OL_EN_ = 0), output three-stated (ONCH_ = 0)		-2		+2	µA

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Electrical Characteristics (continued)

(V_M = +4.5V to +36V, T_A = -40°C to +85°C. ENABLE = V_M, C_F = 22nF, C_{B18} = 2.2µF, C_T = 1µF. Typical values are at V_M = +24V and T_A = +25°C, unless otherwise noted. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PROTECTIONS							
Overcurrent Protection Threshold	OCP			1.1			A
Overcurrent Protection Deglitch Time	t_{OCP}	SRC = 0, FREQM = 0, FREQ_CFG = 00			1.2		µs
UVLO Threshold on V_M	UVLO	V_M rising		3.75	4	4.25	V
UVLO Threshold on V_M Hysteris	$UVLO_{HYS}$				0.12		V
Thermal Shutdown Threshold	T_{SDN}				145		°C
Thermal Shutdown Hysteresis	T_{HYS}				20		°C
Open-Load Detection Current	I_{OL_LS}	OL_EN_ = 1	HSnLS_ = 0, Pulldown current		16	30	µA
	I_{OL_HS}		HSnLS_ = 1, Pullup current	-30	-16		
Open-Load Detection Voltage	V_{OL_LS}	OL_EN_ = 1	HSnLS = 0		1.2	1.8	V
	V_{OL_HS}		HSnLS = 1	V_M - 1.8	V_M - 1.2		
Open-Load Detect Deglitch Time	t_{OL}				200		µs
HALF-BRIDGE CONTROL							
Chopping Frequency	f_{CHOP}	FREQ_CFG[1:0] = 11	FREQ_M = 0	80	100	120	kHz
			FREQ_M = 1	64	80	96	
Output Rise-Time in Slew Rate Controlled Mode	t_{RISE}	SRC_ = 1, 10% to 90% of the swing, V_M = +24V, no load			0.2		µs
Output Fall-Time in Slew Rate Controlled Mode	t_{FALL}	SRC_ = 1, 10% to 90% of the swing, V_M = +24V, no load			0.2		µs
Current Drive Regulation Accuracy	ITR_{ERR1}	Current Drive Regulation mode, I_{FS} at 1A, R_{REF} 1% tolerance LSnHS_ = 0, HFS_ = 0 (*Note 3*)	I_{TRIG} from 71% to 100%	-6		+6	%
	ITR_{ERR2}		I_{TRIG} from 20% to 70%	-10		+10	
	ITR_{ERR3}		I_{TRIG} from 10% to 20%	-15		+15	
	ITR_{ERR4}		I_{TRIG} from 5% to 10%	-25		+25	
Full-Scale Current Reference Constant	K_{FS1}	CDR, LS drive only. R_{REF} from 15kΩ to 100kΩ	HFS_ = 1		7.5k		A/A

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Electrical Characteristics (continued)

(V_M = +4.5V to +36V, T_A = -40°C to +85°C. ENABLE = V_M, C_F = 22nF, C_{B18} = 2.2µF, C_T = 1µF. Typical values are at V_M = +24V and T_A = +25°C, unless otherwise noted. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Full Scale Current Reference Constant	K_{FS0}	CDR, LS drive only. R_{REF} from 15kΩ to 100kΩ	HFS_ = 0		15k		A/A
IREF Pin Regulator Voltage Reference Voltage	V_{IREF}				1		V
Enable Time	t_{EN}	From Enable rising edge to SPI ready				0.5	ms
Wake-Up Time	t_{WU}	From ACTIVE = 1 to Normal operation OUT_ active				2.5	ms
Disable Time	t_{DIS}	From ENABLE falling edge to OUT_ tristate				2.5	ms
Dead Time	t_{DEAD}	Dead zone is inserted to prevent Current Feed through			200		ns
Blanking Time	t_{BLANK}	FREQ_CFG = 11, FREQM = 0	SRC_ = 0		0.8		µs
			SRC_ = 1		1.4		
		FREQ_CFG = 11, FREQM = 1	SRC_ = 0		1		
			SRC_ = 1		1.75		
SPI SPECIFICATIONS (Figure 1)							
SCK Clock Period	t_{CLK}			100			ns
SCK Pulse-Width High	t_{CH}			30			ns
SCK Pulse-Width Low	t_{CL}			30			ns
$\overline{CSB}$ Fall-to-CLK Rise Time	t_{CSS}			30			ns
$\overline{CSB}$ Hold Time	t_{CSH}			30			ns
$\overline{CSB}$ Pulse-Width High	t_{CSPW}			30			ns
SDI Setup Time	t_{DS}			10			ns
SDI Hold Time	t_{DH}			10			ns
SDO Propagation Delay	t_{DO}	310Ω // 20pF connected to 3.3V supply (Note 2)				40	ns
CMD Setup Time	t_{CMS}			20			ns

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: The rising edge on the SDO pin depends on the pullup resistor connected to the pin and on the parasitic stray capacitance. The RC time constant can limit the SPI maximum speed. For fast SPI, the stray capacitance must be minimized and a low-value resistive pullup must be selected.

Note 3: Guaranteed by design, not production tested.

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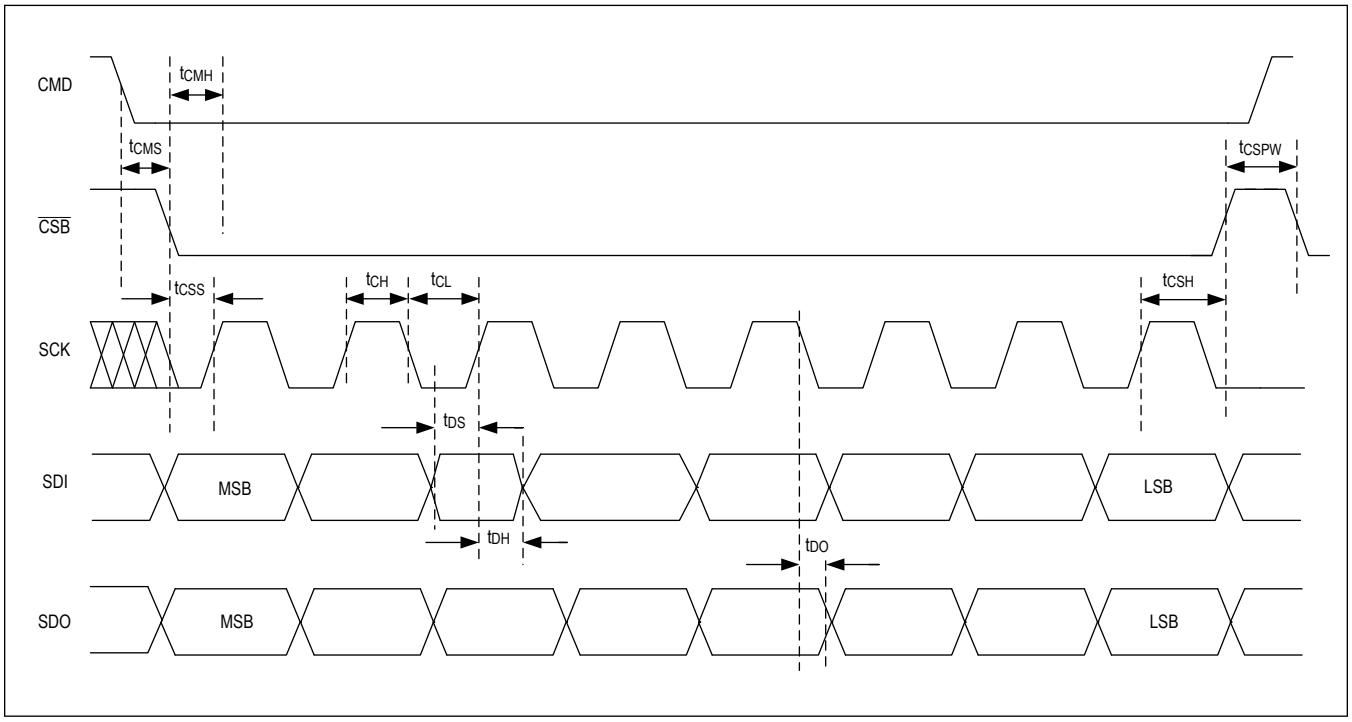

Figure 1. SPI Timing Diagram

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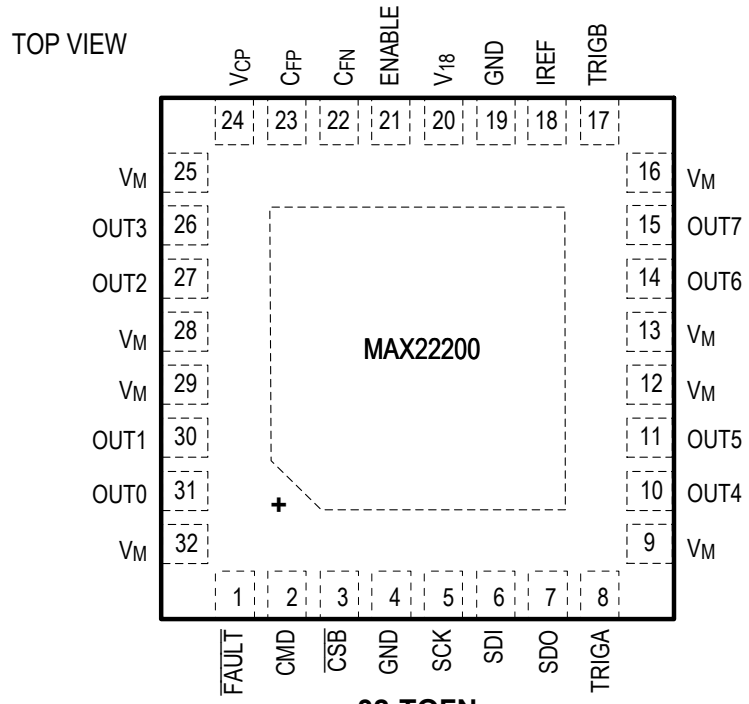
Pin Configuration

MAX22200



32-TQFN
5mm x 5mm

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Pin Description

PIN	NAME	FUNCTION	TYPE
1	$\overline{\text{FAULT}}$	Open Drain Output. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.	OD
2	CMD	Command Logic Input. Drive this pin High to write the Command Register. Drive this pin Low to Write/Read all the other registers. Internal pulldown.	INP
3	$\overline{\text{CSB}}$	SPI Chip Select–Active Low. Internal pullup current.	INP
4, 19	GND	Signal Ground	GND GND
5	SCK	SPI Clock Input. Rising edge clocks data into part for write operations. Falling edge clocks data out of part for read operations. Internal pulldown.	INP
6	SDI	SPI Data In from controller. Internal pulldown.	INP
7	SDO	SPI Data Output. Pulled logic low SPI logic output; open-drain output requires an external pullup resistor.	OD
8	TRIGA	Trigger Logic Input Pin. Half Bridges 0, 2, 4, 6 asynchronous trigger input. Internal pulldown.	INP

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
17	TRIGB	Trigger Logic Input Pin. Half Bridges 1, 3, 5, 7 asynchronous trigger input. Internal pulldown.	INP
9, 12, 13, 16, 25, 28, 29, 32	V_M	Supply Voltage Input. Bypass all V_M pins to GND with two 0.1µF local ceramic capacitors close to pins 12, 13 and pins 28, 29, respectively plus a 10µF electrolytic capacitor.	PWR
			PWR
			PWR
			PWR
			PWR
			PWR
			PWR
			PWR
18	IREF	Current Regulation Reference. Connect a 15kΩ to 100kΩ resistor from IREF to GND to set the full-scale current for all the channels in CDR Mode.	INP
20	V_{18}	1.8V LDO Regulator Output. Bypass to GND with a 2.2µF ceramic capacitor.	PWR
21	ENABLE	Enable Pin. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.	INP
22	C_{FN}	Charge Pump Capacitor–N side. Connect a 22nF, V_M-rated ceramic capacitor from C_{FN} to C_{FP}.	PWR
23	C_{FP}	Charge Pump Capacitor–P side. Connect a 22nF, V_M-rated ceramic capacitor from C_{FN} to C_{FP}.	PWR
24	V_{CP}	Charge Pump Output. Connect a 1µF, 5V or greater ceramic capacitor to V_M.	PWR
31	OUT0	Driver Output Channel 0	OUT
30	OUT1	Driver Output Channel 1	OUT
27	OUT2	Driver Output Channel 2	OUT
26	OUT3	Driver Output Channel 3	OUT
10	OUT4	Driver Output Channel 4	OUT
11	OUT5	Driver Output Channel 5	OUT
14	OUT6	Driver Output Channel 6	OUT
15	OUT7	Driver Output Channel 7	OUT
—	EP	Exposed Pad–Power GND. The exposed pad (thermal pad) is the Power GND of the device and must be electrically connected to the board GND. For good thermal dissipation, use large ground planes on multiple layers and multiple nearby vias connecting those planes.	GND

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Detailed Description

The MAX22200 is an octal 36V serial-controlled solenoid driver. Each channel features a low-impedance (200mΩ typ) push-pull output stage with sink and source driving capability and up to $1A_{RMS}$ driving current. A serial interface (SPI) that supports daisy chaining is provided to individually control each channel.

The MAX22200 half bridges can be configured as low-side drivers or as high-side drivers. Moreover, pairs of half-bridges can be paralleled to double the driving current or can be configured as full-bridges to drive up to four latched valves (bi-stable valves) or four brushed DC motors.

The device supports two control modes: voltage-drive regulation (VDR) and current-drive regulation (CDR) (low-side driver only). In VDR mode, the device outputs a PWM voltage in which the duty cycle is programmed through SPI. For a given supply voltage and solenoid resistor, the output current is proportional to the programmed duty cycle. In CDR mode, an internal integrated lossless current sensing (ICS) circuit senses the output current and compares it with an internal programmable reference current. The CDR loop modifies the PWM duty cycle so that the output current peak matches the programmed reference current. This function is available for low-side drive operation only.

For optimal power management in solenoid drive applications, the excitation drive level (I_{HIT}), the hold drive level (I_{HOLD}), and the excitation drive time (t_{HIT}) can be individually configured for each channel. If multiple channels are active simultaneously, care should be taken to ensure that the junction temperature does not exceed the maximum operating temperature.

The MAX22200 also features a full set of protections and diagnostic functions. This includes overcurrent protection (OCP), thermal shutdown (TSD), undervoltage lockout (UVLO), open-load detection (OL), and detection of plunger movement (DPM). A fault indication pin ($\overline{FAULT}$) is provided to signal fault events. In addition, diagnostic information are stored into the Fault register for further interrogations.

Due to the flexibility of use, the serial interface control, the high efficiency, and the small package size, the MAX22200 is particularly well-suited for solenoid driver applications (valves control, relays control, etc.) in which low-power consumption and a high-level of integration are required.

Enable Logic Input

Drive the ENABLE pin logic High to enable the device. Drive the ENABLE pin logic Low to disable the device. A pulldown resistor (1.5 MΩ typ) ensures the part is disabled if the ENABLE is not driven. When ENABLE is low, the device power consumption is minimized and the current consumption from V_M is less than 11µA. It takes 0.5ms to enable the device SPI communication from the ENABLE pin rising.

Functional Description - Two Levels Drive Sequence for Solenoid Valves

The MAX22200 features a two-level drive sequence for optimal control of solenoid valves. Figure 2 and Figure 3 show typical voltage and current waveforms of the MAX22200 when driving a solenoid with the VDR and CDR, respectively. Both figures refer to low-side driving applications in which the solenoid is tied to the positive rail (V_M). For high-side driving, only VDR is supported.

HIT current (I_{HIT}), HOLD current (I_{HOLD}), and HIT time (t_{HIT}) can be configured for each channel by writing to the correspondent 32-bit configuration register (CFG_CHx). The HOLD Time (t_{HOLD}) is not internally programmable and must be externally controlled. Each driver can be individually controlled independently from the others.

Depending on the content of the TRGnSPI bit in the configuration register of that specific channel, the driver channels can be activated/deactivated either through SPI (ONCH_ bits of the Status Register) or through a logic input signal on pins TRIGA and TRIGB. In the latter case, one (or more) among channels 0, 2, 4, 6 can be triggered by the logic input TRIGA. Similarly, one (or more) among channels 1, 3, 5, 7 can be triggered by using the logic input TRIGB.

With reference to Figure 2 and Figure 3, the excitation starts (point 1) when the channel driver is activated either through SPI or through the TRIG_ logic input. After a short analog delay, the driver is enabled and the current ramps up to I_{HIT}. Moreover, the t_{HIT} counter begins to count. The dip occurring in both the figures between point 1 and point 2 represents the effect of the back electromotive force (BEMF) when the plunger moves. Notice that when CDR is used, the current

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ramps up faster since the driver duty cycle is set to a maximum until the I_{HIT} level is reached. The current stabilizes around the target current level I_{HIT} (point 2).

As soon as the t_{HIT} time elapses (point 3), the driver automatically changes the target current to I_{HOLD}, which is normally set significantly lower than I_{HIT}. The current starts decreasing until it reaches the regulated value (point 4). Notice that when CDR is used, the current decreases faster since the driver duty cycle is set to minimum t_{ON} until the I_{HOLD} level is reached. Finally, the sequence ends as soon as the channel is deactivated either through SPI or through the TRIG_.

When the VDR is used, the output current slightly decreases both during the HIT and the HOLD time intervals. This behavior is representative of possible droops on the voltage supplies and/or of the increase of the solenoid resistance due to overheating during the excitation period. Due to the feedback close loop approach, CDR is less sensitive to this kind of environmental change and results in a more stable and constant current control.

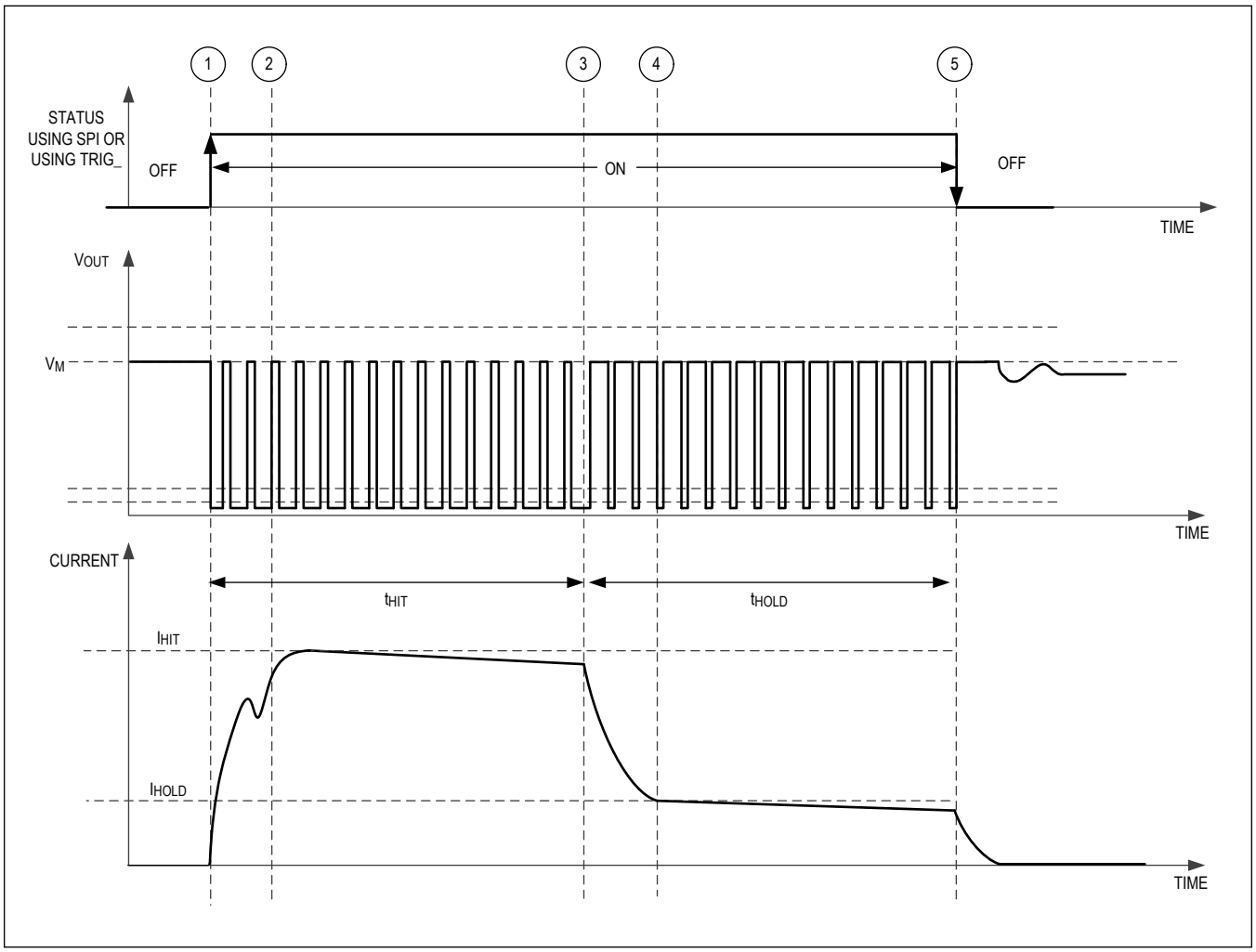

Figure 2. Timing Diagram VDR

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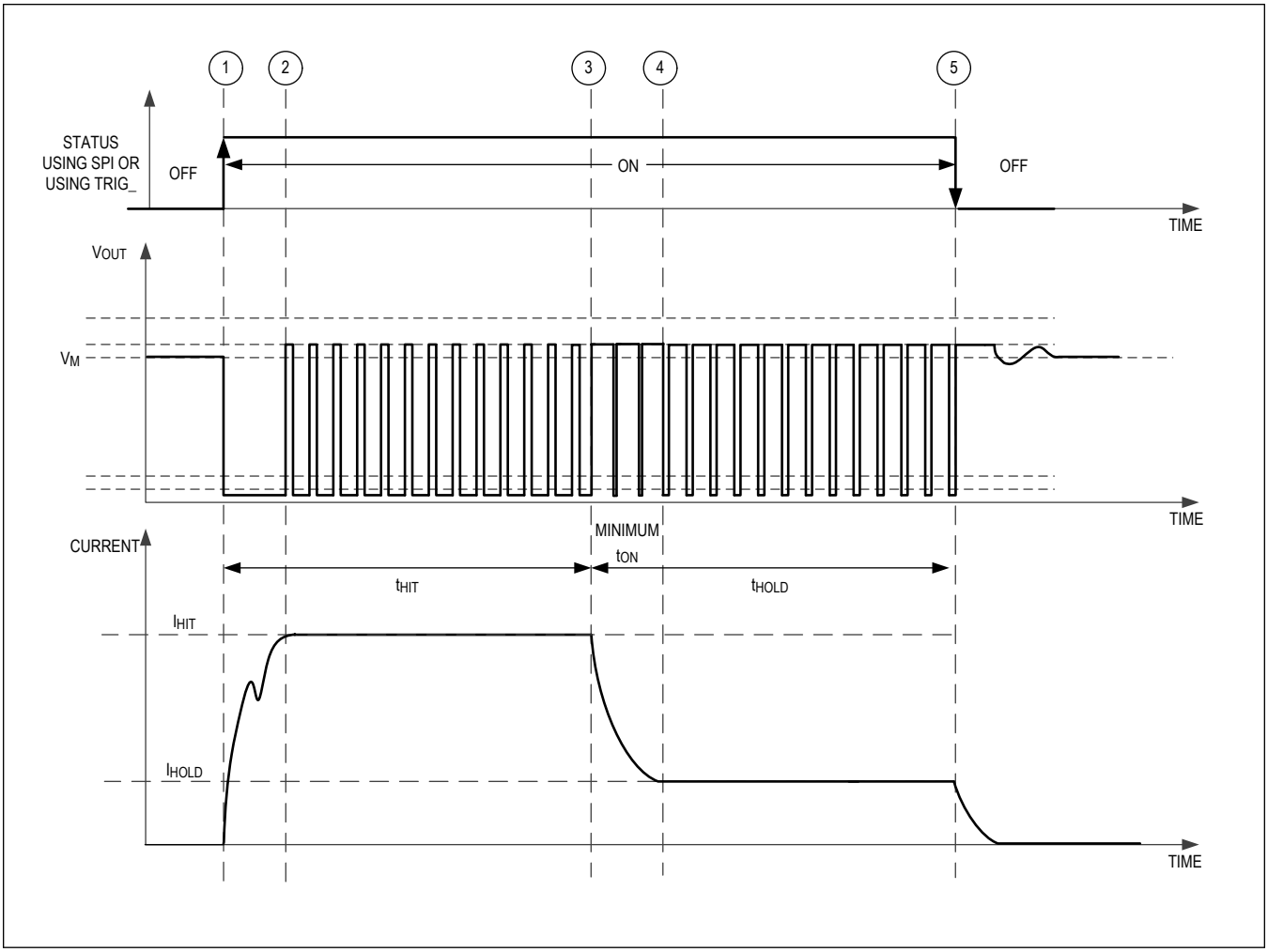

Figure 3. Timing Diagram CDR

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Chopping Frequency (FREQM, FRQ_CFG_)

The MAX22200 features an integrated oscillator, which sets the time base of the device and determines the chopping frequency both in VDR and in CDR. The oscillator frequency can be set either at 100kHz or at 80kHz depending on the FREQM bit in the STATUS register (global for all the channels).

In addition, two bits (FREQ_CFG_[1:0]) in the Configuration Register allows the user to configure the chopping frequency of each individual channel dividing down the oscillator frequency as shown in the Table 1.

Table 1. Chopping Frequency

CHOPPING FREQUENCY		CHOPPING FREQUENCY f_{CHOP} (kHz)
FREQM = 0	FREQ_CFG[1:0] = 11	100
	FREQ_CFG[1:0] = 10	50
	FREQ_CFG[1:0] = 01	33.3
	FREQ_CFG[1:0] = 00	25
FREQM = 1	FREQ_CFG[1:0] = 11	80

Table 1. Chopping Frequency (continued)

	FREQ_CFG[1:0] = 10	40
	FREQ_CFG[1:0] = 01	26.6
	FREQ_CFG[1:0] = 00	20

Slew-Rate Controlled Mode (SRC)

Both in CDR and VDR modes, rise and fall edges can be slowed down to reduced electromagnetic emissions (EME). To configure one half-bridge in slew-rate controlled (SRC) mode, the SRC bit in the Configuration Register (CFG_CH_) must be set high. When SRC mode is enabled, the rise/fall edges are limited to about 200ns (typ) and OCP deglitch time is doubled. SRC mode is only available for low-side driver configurations and for switching frequencies less than 50kHz.

Min and Max Duty cycle

In both CDR and VDR mode, the duty cycle is constrained as described in Table 2. The minimum and maximum duty cycles depend on the selected switching frequency and on the slew-rate configuration (SRC bit).

Table 2. Min and Max Duty Cycle

CHOPPING FREQUENCY SRC = 0		CHOPPING FREQUENCY f_{CHOP} (kHz)	VDR/CDR MIN DUTY δ_{MIN}	VDR/CDR MAX DUTY δ_{MAX}
FREQM = 0	FREQ_CFG[1:0] = 11	100	**8%**	**92%**
	FREQ_CFG[1:0] = 10	50	**4%**	**96%**
	FREQ_CFG[1:0] = 01	33.33	**4%**	**96%**
	FREQ_CFG[1:0] = 00	25	**4%**	**96%**
FREQM = 1	FREQ_CFG[1:0] = 11	80	**8%**	**92%**
	FREQ_CFG[1:0] = 10	40	**4%**	**96%**
	FREQ_CFG[1:0] = 01	26.66	**4%**	**96%**
	FREQ_CFG[1:0] = 00	20	**4%**	**96%**
CHOPPING FREQUENCY SRC = 1		**CHOPPING FREQUENCY f_{CHOP} (kHz)**	**VDR/CDR MIN DUTY δ_{MIN}**	**VDR/CDR MAX DUTY δ_{MAX}**
FREQM = 0	FREQ_CFG[1:0] = 01	33.33	**7%**	**93%**
	FREQ_CFG[1:0] = 00	25	**7%**	**93%**
FREQM = 1	FREQ_CFG[1:0] = 10	40	**7%**	**93%**
	FREQ_CFG[1:0] = 01	26.66	**7%**	**93%**
	FREQ_CFG[1:0] = 00	20	**7%**	**93%**

Voltage Drive Regulation (VDR)

To operate in VDR the VDRnCDR_ bit in the Configuration Register must be set High (see the Register Map). When VDR is used, each individual channel can be programmed to output the desired PWM waveform during HIT and HOLD phases. The user can program the HIT and HOLD duty cycles ($\delta = t_{ON} / t_{CHOP}$) with steps of 1% resolution.

The HIT and HOLD target duty cycles are preprogrammed in the Configuration Register for each channel as shown in Table 3. The duty cycle minimum and maximum values (δ_{MIN}, δ_{MAX}) are determined by the chopping frequency settings and by the SRC configuration bits as shown in Table 2.

Table 3. VDR Duty Cycle

HIT CURRENT PROGRAMMING CONDITION	OUTPUT DUTY CYCLE

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Table 3. VDR Duty Cycle (continued)

$HIT[6:0]_{DEC}$	= 0	0 duty cycle
	> 0, < δ_{MIN}	δ_{MIN}
	≥ δ_{MIN}, < δ_{MAX}	$HIT[6:0]_{DEC}$
	≥ δ_{MAX}, < 100	δ_{MAX}
	≥ 100	100% duty cycle
HOLD CURRENT PROGRAMMING CONDITION		**OUTPUT DUTY CYCLE**
$HOLD[6:0]_{DEC}$	= 0	0 duty cycle
	> 0, < δ_{MIN}	δ_{MIN}
	≥ δ_{MIN}, < δ_{MAX}	$HOLD[6:0]_{DEC}$
	≥ δ_{MAX}, < 100	δ_{MAX}
	≥ 100	100% duty cycle

Current Drive Regulation (CDR)

To operate in CDR, the VDRnCDR_ bit in the Configuration Register must be set Low (see the Register Map). This is also the default setting at power up. CDR is supported in low-side configurations only.

HIT and HOLD Current Setting (CDR)

When the CDR mode is used, the current can be controlled with 7-bit resolution. Because of the feedback approach, CDR results in more efficient power management when compared to VDR. In fact, unlike VDR, CDR requires no design margin for environmental parameter changes such as temperature, solenoid resistance variations, and droops on the supply. For a battery-powered system, this ultimately results in longer battery lifetime. The current loop of CDR regulates the coil current cycle-by-cycle. A non-dissipative accurate current sense is integrated so that no external sense resistors are needed.

The HIT and HOLD currents are configurable in the Configuration Register for each channel and the following equations apply as in Table 4.

Table 4. HIT and HOLD Current Setting (CDR)

HIT CURRENT PROGRAMMING CONDITION		**I_{TRIG} PEAK CURRENT**
$HIT[6:0]_{DEC}$	0	HS Switch ON, LS Switch OFF
	0 < $HIT[6:0]_{DEC}$ < 127	$I_{HIT} = HIT\_[6:0]_{DEC} / 2^7 \times I_{FS}$
	127	HS Switch OFF, LS Switch ON
HOLD CURRENT PROGRAMMING CONDITION		**I_{TRIG} PEAK CURRENT**
$HOLD[6:0]_{DEC}$	0	HS Switch ON, LS Switch OFF
	0 < $HOLD[6:0]_{DEC}$ < 127	$I_{HOLD} = HOLD\_[6:0]_{DEC} / 2^7 \times I_{FS}$
	127	HS Switch OFF, LS Switch ON

where, I_{FS} is the full-scale current.

The CDR loop regulates the peak current (I_{TRIG}). The average current (both for the HIT and HOLD currents) would be lower due to the current ripple.

Full-Scale Current Setting (I_{FS})

I_{FS} is user configurable by setting the resistor connected between pin IREF and Ground per the following equation:

$$I_{FS} = K_{FS} \times \frac{1(V)}{RREF(\Omega)}$$

where, K_{FS} is a constant (gain factor) and RREF is the resistor connected between the IREF pin and GND.

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The Gain factor K_{FS} depends on the HFS bit value in the configuration register (see the *Half Full-Scale (HFS)* section). If HFS_ = 0 then K_{FS} = 15k, whereas if HFS = 1 then K_{FS} = 7.5k. The recommended operating range for RREF is from 15kΩ to 100kΩ.

Half Full-Scale Setting (HFS bit)

Whenever low driver-current levels are needed, it is possible to improve the current control accuracy and resolution by setting high the HFS bit in the Configuration Register. This can be done individually for each half-bridge. (This function is available for low-side applications only.)

When the HFS bit is set low (default), the driver On resistance is R_{ON} = 0.2Ω, the full-scale current can be set up to I_{FS} = 1A. The current control accuracy is shown in the *Electrical Characteristics* section.

When the HFS bit is set high, the driver On resistance is doubled (R_{ON} = 0.4Ω) whereas the maximum full-scale and RMS currents are halved (I_{FS} = 0.5A).

For solenoids or brushed DC motors requiring less than 0.5A peak, the half full-scale setting results in a more accurate current sensing and hence better control accuracy and resolution. As a drawback, the efficiency of the driver worsens because of the higher driver On resistance.

Fixed Frequency Current Control

The current control loop regulates, cycle-by-cycle, the driver current by using a fixed-frequency topology and an integrated non-dissipative current-sensing. CDR is available only in low-side drive mode.

At the beginning of the chopping clock period, the low side FET is On and the current builds up in the coil at a rate dependent on the supply voltage and on the inductance of the winding. When the current hits the current regulation threshold, the low-side FET is turned Off, whereas the high-side FET is turned On and the winding current decays. This status lasts until the next On-cycle is triggered by the internal chopping clock. Refer to the *Chopping Frequency* section for information about the setting of the chopping frequency.

The current ripple is inversely proportional to the chopping frequency. In order to reduce the ripple and improve the average current control, a high chopping frequency should be considered. A first order approximation of the ripple can be achieved assuming that the OFF time is significantly shorter than the solenoid time constant ($\tau = \frac{L}{R}$) so that the ripple is small compared with the average current. Under this assumption, it can be found that the peak to peak ripple is given by:

$$\Delta I \cong \frac{1}{\frac{L}{R} \times f_{CHOP}} \times \left(1 - \frac{I_{TRIG}}{\frac{V_M}{R}}\right)$$

where,

ΔI = Peak-to-peak ripple,

I_{TRIG} = Threshold current,

V_M = Supply voltage,

L = Coil inductance,

R = Resistance.

Blanking delays and filters are integrated to prevent false triggers due to switching noise. They have not been accounted in the above equations .

HIT Excitation Time (t_{HIT})

The excitation time can be programmed among 256 different values by programming bits HIT_T_[7:0] in the configuration register (see the Register Map).

The HIT time (t_{HIT}) is inversely proportional to the chopping frequency (see the *Chopping Frequency* section) and can be calculated according to Table 5 in which f_{CHOP} is the oscillator frequency (in Hertz). For instance, with the oscillator

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running at f_{CHOP} = 20KHz, the t_{HIT} ranges from t_{MIN} = 0ms to t_{MAX} = 508ms with 2ms time resolution. As explained in the *Functional Description* paragraph, the t_{HIT} counter can be triggered either by the SPI programming command or by an external trigger signal.

Table 5. HIT Excitation Time (t_{HIT})

CONFIGURATION BITS	t_{HIT} VALUE	COMMENTS
$HIT\_T\_[7:0]_{DEC}$ = 0	t_{HIT} = 0	No Hit Time
$HIT\_T\_[7:0]_{DEC}$ from 1 to 254	$t_{HIT} = HIT\_T\_[7:0]_{DEC} \times 40 / f_{CHOP}$	
$HIT\_T\_[7:0]_{DEC}$ = 255	$t_{HIT} = \infty$	Continuous I_{HIT}

Supported Driver Configurations

The MAX22200 provides for flexibility. Its eight independent half bridges can be configured in different ways to address different applications.

1. It is possible to set each half-bridge as a low-side driver or as an high-side driver
2. It is possible to use a pair of half-bridges in parallel to double the driving current capability.
3. It is possible to use a pair of half-bridges to make a full-bridge and drive latched valves or brushed DC motors

These configurations must be set just after the power-up by writing the status register.

Low-Side/High-Side Operations (HSnLS)

The MAX22200 supports either low-side or high-side drive modes corresponding to loads connected to the positive rail or to ground respectively. The Bit HSnLS in the Configuration Register must be set low (default) for low-side drive operation or high for high-side drive operations. For high-side drive operations, CDR is not supported and channels are controlled in VDR mode only. Moreover, SRC and HFS functions are not supported in high-side operations.

Half-Bridge Parallelization

The user can possibly connect pairs of channels in parallel in order to double the driving current. The pairs 0–1, 2–3, 4–5, and 6–7 can be used in parallel by connecting the corresponding output pins together (refer to the *Application Diagram*

). To configure the pair x–y in Parallel mode, the user must write bit CMxy[10] = 01 into the STATUS[15:8] register (see the Register Map).

When one pair of half bridges is used in Parallel mode, the Configuration Register setting of the half-bridge with the lower identification number control both the half-bridges and the other one is ignored. For instance, considering the pair 0–1 in Parallel mode, all the settings are taken from the configuration register of Channel 0 while the configuration register of Channel 1 is ignored.

The activation/deactivation (On/Off command) of the two half-bridges in Parallel mode remains independent. The TRGnSPI bits in the Configuration Register enables/disables the drivers as shown in Table 6:

Table 6. TRGnSPI in Half-Bridge Parallel Mode

TRGnSPIy	TRGnSPIx	CONTROL MODE
0	0	Channels controlled by SPI (both ONCHx and ONCHy set logic high)
0	1	Channels controlled by TRIGA
1	0	Channels controlled by TRIGB
1	1	Channels controlled by SPI (both ONCHx and ONCHy set logic high)

Full-Bridge Configuration

It is possible to configure the half-bridges pairs 0–1, 2–3, 4–5, and 6–7 to make full-bridges and drive latched (bistable) solenoid valves or even brushed-bipolar DC motors. One pair x–y is declared as a full-bridge by setting bits CMxy_[1:0] = 10 in the Status Register (refer to the Register Map)

When in Full-Bridge mode, the full-bridge operates in 4 different statuses depending on the content of bits ONCHy and

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ONCHx in the Status Register as described in Table 7:

Table 7. Full-Bridge Configuration

(x,y) = (0,1), (2,3), (4,5), (6,7)				
ONCHy	**ONCHx**	**OUTx**	**OUTy**	**DESCRIPTION**
0	0	Hi Z	Hi Z	Hi Z
0	1	VM	VDR/CDR Y settings	Forward
1	0	VDR/CDR X settings	VM	Reverse
1	1	GND	GND	Brake

In Table 7, the setting parameters for the control are taken from the configuration register of Channel Y in Forward mode and from the configuration register of Channel X in Reverse mode. For instance, considering the pair 0–1 in Full-Bridge mode, when [ONCHy, ONCHx] = [0,1] (forward), the control parameters depend on the content of the Configuration Register of Channel Y. Vice versa, when [ONCHy, ONCHx] = [1,0] (reverse), then the control depends on the content of the Configuration Register of Channel X. In this way, it is possible to use different currents levels or timings for latch/unlatch operations of a latched valve. Notice that the HSnLS bit is ignored for full-bridge operations.

Finally, in Full Bridge Operations, the TRGnSPI bits in the Configuration register enables/disable the drivers as shown in Table 8:

Table 8. TRGnSPI in Full-Bridge Mode

TRGnSPIy	TRGnSPIx	CONTROL MODE
0	0	Channels controlled by SPI
0	1	Channels controlled by SPI
1	0	Channels controlled by SPI
1	1	Channels controlled by TRIGA/TRIGB

Protection Circuits

The MAX22200 features a full set of protections including undervoltage (UVLO), overcurrent (OCP), and overtemperature (OVT). The device also features diagnostic functions such as open-load detection (OL), detection of plunger movement (DPM), "hit current not reached" detection (HHF), and communication error detection (COMF). An open-drain fault indication pin ($\overline{FAULT}$) is provided to signal detected faults out to the controller. Each of the above mentioned failures (with the exception of the COMF) are by default signaled out to the $\overline{FAULT}$ pin. Fault indication can be masked by setting high the corresponding bits into the Status registers (STATUS[15:8]). When a Fault is masked, a Fault event does not activate the $\overline{FAULT}$ pin.

Overcurrent Protection (OCP)

The overcurrent protection protects the device from short-circuits of the driver outputs to the rails (V_M and GND) or among each other. When the output exceeds OCP trigger levels, the corresponding channel is automatically turned Off and the $\overline{FAULT}$ output is asserted (active low). Moreover, the corresponding OCP flag in the Fault register is set high for diagnostic purposes. Reading the Fault register clears the Flag and deasserts the $\overline{FAULT}$ output, but does not turn on the failed channel. Once the flag is cleared, the normal operations are resumed by turning the failed channel Off in the Status Register.

Open-Load Detection (OL)

One bit in the configuration register is used to either enable or disable the OL detection function. Provided that this function is enabled, whenever the load is disconnected, a small source/sink current pulls the output node up/down depending on low-/high-side operation mode set for the channel. If the voltage on the output pin is sensed to be less than +2V for low-side configuration or greater than V_M - 2V for high-side configuration, then an open-load condition is

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reported. Consequently, the corresponding flag in the Fault register is set high and the $\overline{FAULT}$ output is asserted (if this fault is not masked). Open-load faults are automatically cleared and the $\overline{FAULT}$ pin released if the corresponding output is turned on or if the Fault register is read.

Detection of Plunger Movement (DPM)

The MAX22200 features a novel diagnostic function which detects whether the plunger inside the armature successfully moves once the valve is activated. This function is referred as detection of plunger movement (DPM) and it is a useful tool to identify malfunctioning valves and allow a prompt repair or replacement of the defective valve.

Figure 4 shows the typical current profile exhibited by a working valve (blue curve) and a stuck valve (black curve). When the valve is actuated the solenoid current ramps up from zero to the programmed excitation current level I_{HIT}. If the valve works properly, the current profile is not monotonic but shows a drop due to the BEMF generated by the movement of the plunger inside the solenoid.

The amplitude of the drop is characteristic of each valve and is almost independent from external variables such as supply voltage and temperature. When enabled, the DPM function detects the presence of the drop during the excitation phase. If the drop is not revealed a fault indication is output on $\overline{FAULT}$ pin (if not masked) and a fault bit is asserted in the fault register.

The DPM starts monitoring the current above a user-programmable initial current (I_{START}). The search ends as soon as the programmed excitation level (I_{HIT}) is reached. The user can program the DPM threshold (I_{DPM_TH}) as a fraction of the full-scale current. Finally, it is possible to program a debounce time to avoid false detection caused by environmental noise. Refer to the *CFG_DPM* section for further details about DPM configuration.

The detection can fail if the drop is not pronounced enough or if the currents ramps up too quickly. The DPM function is activated by setting logic high for one bit in the configuration register for each individual channel.

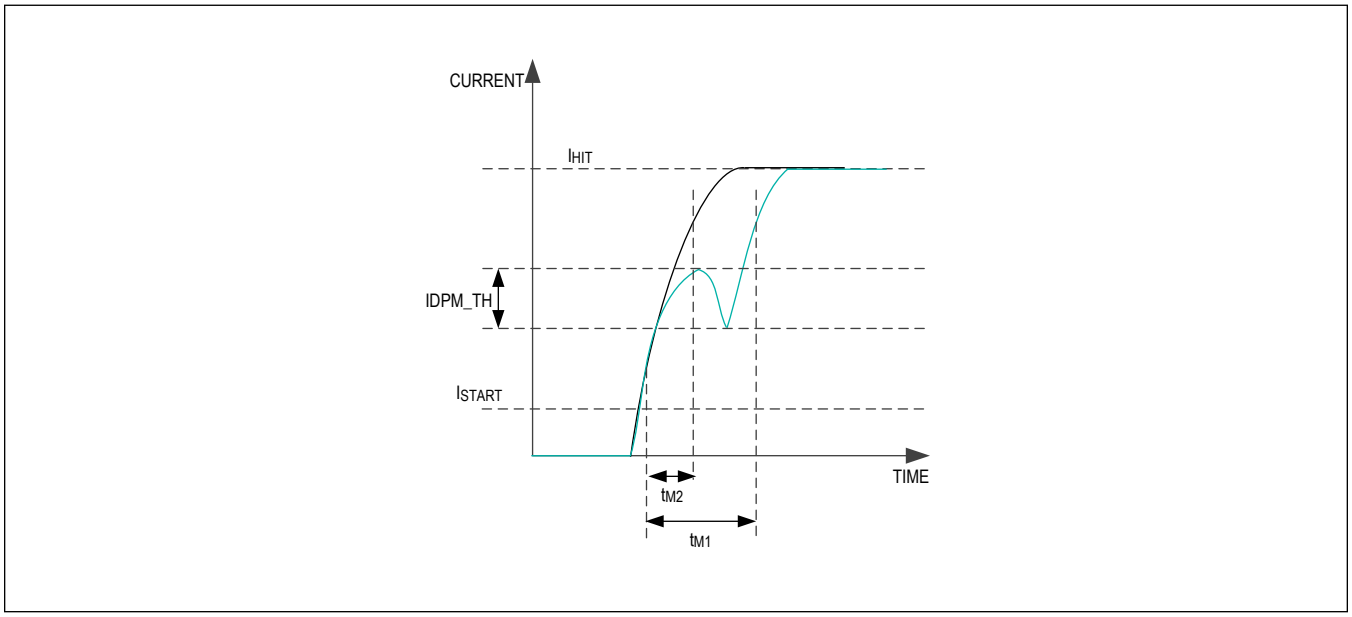

Figure 4. Detection of Plunger Movement

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all outputs are disabled. One flag bit in the Fault register is set high and the $\overline{FAULT}$ pin is driven low. Once the die temperature has fallen to a safe level, operation automatically resumes. The $\overline{FAULT}$ pin is released but the flag bit remains set to '1' until the fault register is read.

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Undervoltage Lockout (UVLO)

If at any time the voltage on the V_M pin falls below the undervoltage lockout threshold (about +4V typ), all channels are three-stated and the internal charge pump is disabled. The content of the logic registers is preserved until the V_{18} regulator, which operates under V_M, loses the regulation and V_{18} falls below the digital power-on reset (POR) threshold. When this happens (typically at V_{18} = 1.0V), all registers are reset to the default values.

A UVLO event that has not resulted in any POR, activates the fault indication pin if the corresponding mask bit (M_UVM) is set logic low (default). The MAX22200 resumes normal operation as soon as the V_M rises back above the UVLO threshold.

A UVLO event that has caused a POR event, always activates the $\overline{FAULT}$ pin and requires the user to reconfigure the device and reactivate the part normal operation. In particular, $\overline{FAULT}$ is always asserted at power-up.

"HIT Current not reached" Flag (HHF)

In CDR mode, the user can monitor whether the preprogrammed HIT current level is reached. This diagnostic tool can be enabled by setting the bit HHF_EN_ to "1." If the target current is not reached at the end of t_{HIT}, then the corresponding flag bit in the Fault register is set high. If the fault mask bit M_HHF is set to "0," the $\overline{FAULT}$ indication pin is activated, the driver is not disabled, and the flag bit is cleaned up when the fault register is read or every time the channel initiates a new cycle.

Programming Information

SPI Detailed Description

During normal operation (ENABLE = logic high), the MAX22200 is controlled using SPI. The interface has five signals: clock (SCK), chip select ($\overline{CSB}$), command (CMD), serial data in (SDI), and serial data out (SDO). The SPI interface logic complies with SPI clock polarity CPOL = 0 and clock phase CPHA = 0. The SPI supports daisy-chain configurations and can operate up to 5MHz. Figure 5 shows a typical daisy-chain configuration.

The MAX22200 features 10x 32-bit data registers (1x Status Register, 8x Configuration Register, 1x Fault Register) plus an 8-bit Command Register. The Command Register (Write Only) must be written first since its content determines the interpretation of the follow-on SPI cycles.

Status Register, Configuration Registers, and Fault Register are 32-bits long. However, by setting high the "8bit/nr32" bit in the Command Register, the user can address the first Most Significant Byte only with just one-byte long SPI transfer.

- The MSB of the Status Register allows the user to enable/disable each individual half-bridge. Therefore, activation/deactivation operations can be done with just one-byte long SPI transfer minimizing the system latency.
- The MSB of the Configuration Register, allows the user to program the HOLD current and the HFS bit. Therefore, updating the HOLD current can be done with just one-byte long SPI transfer allowing a quick update in applications in which such a current must be controlled dynamically.
- The MSB of the Fault Register reports the OCP information. The user can read the OCP register information with just one-byte-read operation.

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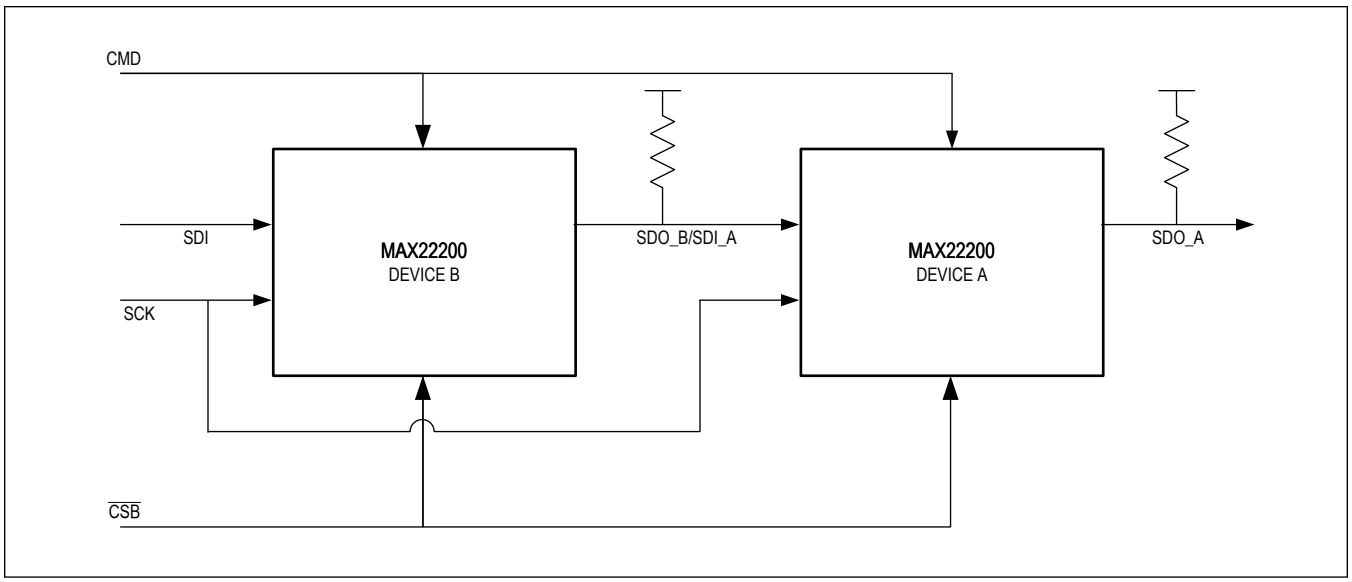

Figure 5. SPI Daisy-Chain Configuration

Programming Procedure

Figure 6 shows the recommended flow chart for the initialization and operation of the MAX22200.

Each step in the procedure requires two subsequent SPI transfers with the Command register written first (CMD = 1) to prepare for the following Write/Read operation on the other registers (see the *Command Register Description (COMMAND)* for further details).

1. The first step after power-up consists of reading the STATUS Register. This is necessary to clear the Undervoltage Fault Flag bit (UVM) and to deassert the nFAULT indicator pin.
2. The second step consists of writing the STATUS register Hardware configuration for each channel and declares which of them are used in parallel or Full-Bridge mode configuration. The ACTIVE bit is also set high to enable the device.
3. The third step consists of configuring the drive parameters for each individual channel. This is accomplished by writing to the 32-bit Configuration Register (CFG_CH) for each channel and setting the desired drive parameters such as HIT and HOLD currents, HIT Time, preferred drive mode (CDR/VDR), Slew Rate Control, etc.
4. Once all the channels are configured, the STATUS register must be read to ensure the UVM bit and all other Fault bits are cleared.

At each Write operation to the COMMAND register, the MAX22200 SPI outputs the Fault Flag Byte (STATUS[7:0]). The Controller should monitor whether Communication errors are reported. If a Communication Fault was reported (STATUS[7:0]=0x02), the procedure should be repeated as shown in Figure 6.

5. Once the procedure steps 1 to 4 are completed and no faults are reported, channels can be activated and "on-the-fly" actions can be performed. In particular:
    1. The ON/OFF status can be updated to individually activate/deactivate each channel. This action requires writing the most significant byte of the STATUS Register with a single byte transfer.
    2. The HOLD current value (IHOLD) and the Half Full-Scale Setting (HFS) can be updated in order to dynamically control the HOLD current delivered by each individual channel. This action requires writing the most significant byte of the Configuration Register of that specific channel. The IHOLD update can be done “on-the-fly” while the channel is delivering the HOLD current.
    3. Some of the configuration parameters for each individual channel can also be changed “on-the-fly” by writing the whole 32-bit Configuration Register for that specific channel. This includes the Slew Rate Control setting (SRC) and the chopping frequency settings (FREQ_CFG). Notice that the Control Mode setting (VDR/CDR bit) as well

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as the high-side/low-side setting (HSnLS bit) can only be modified if all the channels are OFF and both TRIGA and TRIGB inputs are logic low.

If a Fault occurs, the nFAULT indicator pin is asserted if not masked. This event can trigger a Fault procedure (not described in Figure 6). Moreover, at each Write operation to the COMMAND register, the MAX22200 SPI outputs the Fault Flag Byte (STATUS[7:0]) which can be used for diagnostic purposes as well.

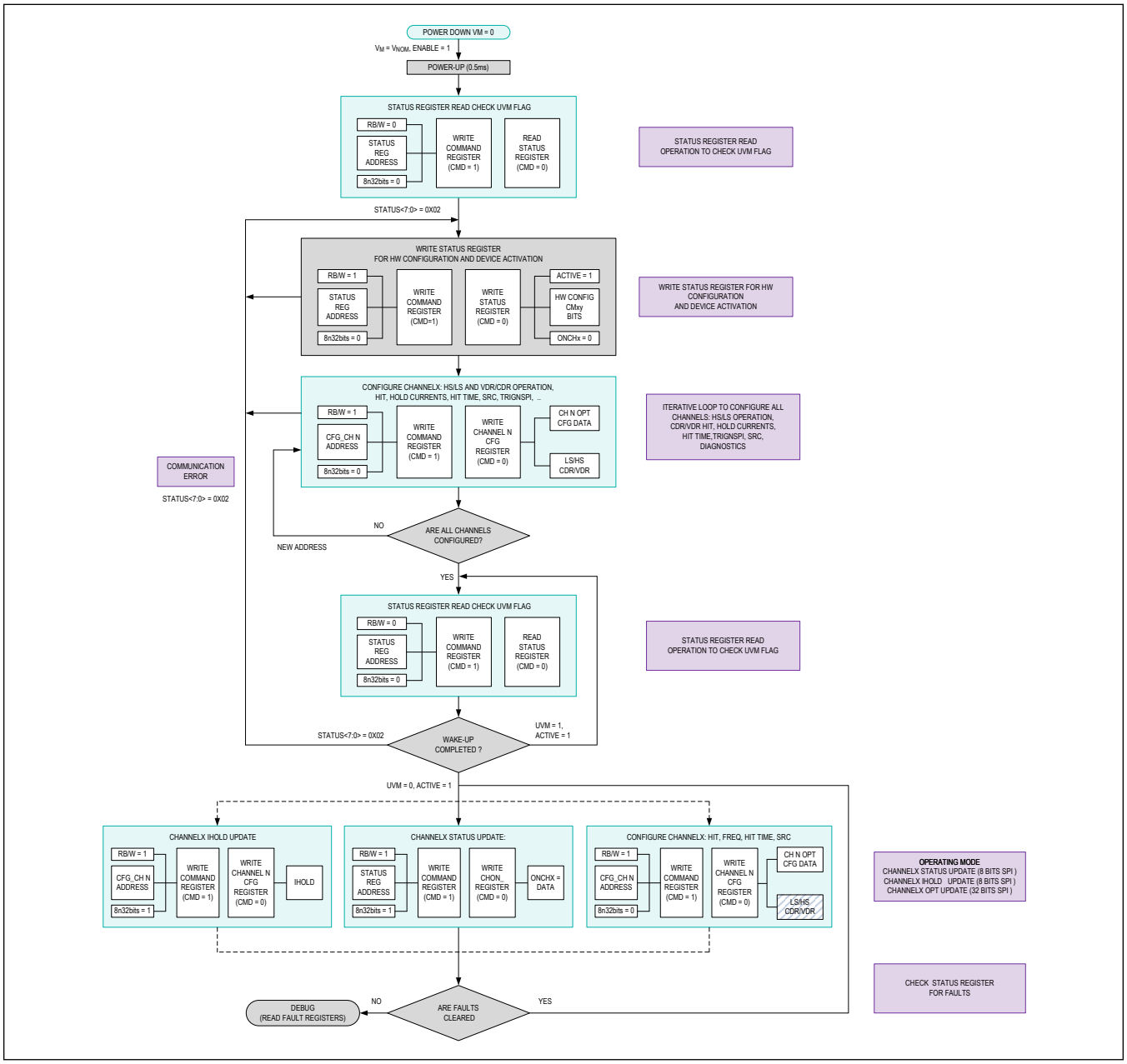

Figure 6. Programming Flow Chart

Command Register Description (COMMAND)

The Command Register is an 8-bit Register. Writing to the Command Register prepares the device for the follow-on SPI

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cycle. The user must write the Command register first since its content determines type and valid data format of the following SPI transfers. Once the user has written the Command Register, all the following SPI transfers remain of the same type until the Command Register is rewritten.

To write to the 8-bit Command Register, the logic input CMD must be logic-high and remain high during the entire SPI transfer. Operations on all the other registers (Status, Configuration and Fault Registers) require the CMD logic input to be logic low. Table 9 shows the Data Description of the Command Register bits. Figure 7 shows the Time Diagram for the Write operation of the Command Register for both the single-device and daisy-chain use cases. The logic-input CMD must be held high during the rising edge of $\overline{CSB}$. For diagnostic purposes, the SPI outputs the Fault Flag Byte (STATUS[7:0] when writing to the Command Register.

Table 9. Command Register

BIT	NAME	DESCRIPTION
7	RB/W	This bit determines whether the follow-on SPI transfer is a Write or Read operation. (Read = 0, Write = 1)
6:5	RFU	Reserved For Testing and Future Usage. Write these bits logic low.
4:1	A_BNK	This data field contains the address of the 32-bit register bank to be used for the follow-on SPI transfer (see the Register Map)
0	8bit/ n32bits	Set this bit logic High to have access to the 8 MSB of the 32-bit register bank. The follow-on SPI transfer is 8-bits long. Set this bit logic Low to have access to the whole 32 bits register bank. The follow-on SPI transfer is 32-bits long.

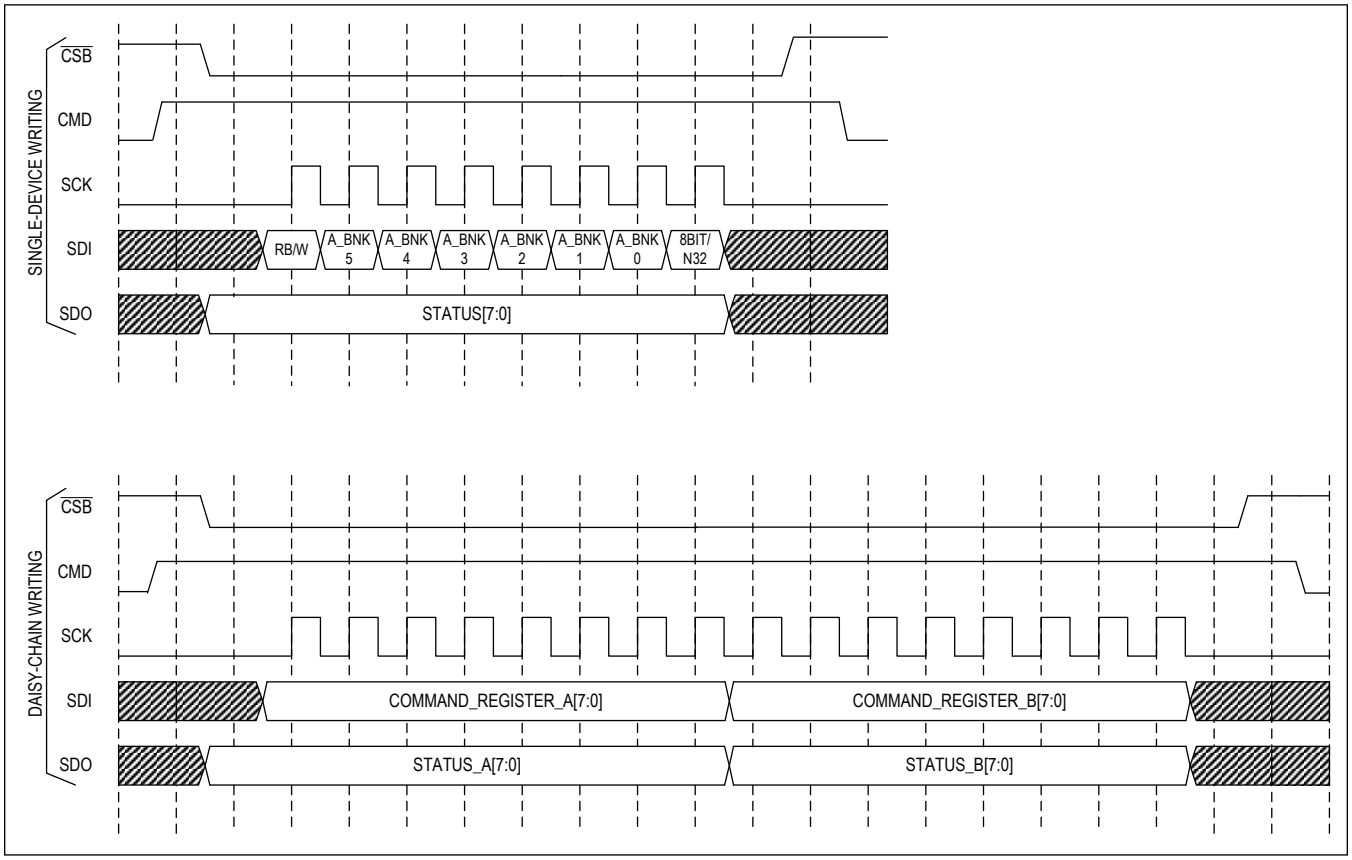

Figure 7. Writing Command Register

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Status Register Description (STATUS)

The Status Register is a 32-bit Register.

- The first Most Significant Byte (STATUS[31:24]) stores the activation bit for each individual channel. Set the ONCHx bit high to activate channel x. Set the ONCHx bit low to deactivate channel x.
- The second Most Significant Byte (STATUS[23:16]) stores the mask fault bits and the Master Frequency selection bit (FREQM)
- The third Most Significant Byte (STATUS[15:8]) stores the Hardware Configuration bits for pairs of contiguous channels. By programming this register, contiguous channels can be configured to operate in parallel mode or in full-bridge mode. Refer to the *Supported Driver Configurations* section for further information.
- The Least Significant Byte (STATUS[7:0]) stores seven Read-Only Flag Fault bits and the ACTIVE bit. The ACTIVE Bit is a global Enable bit set to "0" at power-up (default).
  - When ACTIVE is "0" the device enters in low-power mode and channels are three-stated.
  - For normal operation ACTIVE must be set to "1."

The Seven-Flag Fault bits are listed below:

- OVT = Overtemperature Fault Flag
- OCP = Overcurrent Fault Flag—at least one channel detected an overcurrent
- OLF = Open-Load Fault Flag—at least one channel detected an open-load
- HHF = HIT Current Not Reached Fault Flag—at least one channel detected a HIT current not-reached fault
- DPM = Detection of Plunger Movement Flag—at least one channel detected a plunger movement fault
- COMER = Communication Error Fault Flag
- UVM = Undervoltage Fault Flag—The UVM is set high at power-up and must be cleared by reading the STATUS register to enable operations.

Note: Further diagnostic information about OCP, OLF, HHF, and DPM are available at the FAULT register (see the Register Map).

Table 10. Status Register

BITS	DESCRIPTION
[32:24]	ONCHx bits. 1 = Channel is active. 0 = Channel is not active (default)
[23:16]	Fault Mask Bits: 1 = Fault is masked and does not assert the $\overline{\text{FAULT}}$, 0 = Fault is not masked (default) FREQM: set the master frequency of the internal oscillator
[15:8]	CMxy: Hardware Configuration bits for pairs of contiguous channels. Channels can be configured in Parallel or Full-Bridge mode (see the *Supported Driver Configurations* section)
[7:0]	Fault Flag Bits: OVT, OCP, OLF, HHF, DPM,COMER, UVM ACTIVE bit: 1 = The Device is Active ; 0 = The device is not Active and all channels are Hi-Z (default)

Configuration Register Description (CFG_CH_)

There are eight 32-bit (4 Byte) Configuration Registers for independent channel configuration.

- The Most Significant Byte CFG_CH_[31:24] stores the HOLD current information (7 bits) and the half full-scale selector bit (HFSx).
- The second Most Significant Byte CFG_CH_[23:16] stores the HIT current information (7 bits) and the external trigger selector bit (TRGnSPI)
- The third Most Significant Byte CFG_CH_[15:8] stores the excitation time information.
- The Least Significant Byte CFG_CH_[7:0] stores channel configuration settings:
  - VDR/CDR selector bit (VDRnCDR),
  - HS/LS selector bit (HSnLS),
  - Channel Chopping frequency bits (FREQ_CFG)
  - Slew Rate selector bit (SRC),
  - Open Load Detection Enable (OL_EN)
  - HIT current Detection Enable bit (HHF_EN).

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Refer to the *Detailed Description* and to the Register Map for more detail. The table below summarize the content of the Configuration Register.

Table 11. Configuration Register

BIT	DESCRIPTION
[31:24]	HFS selector bit. "1" for Half Full-Scale operation; "0" for Full-Scale operation (default) HOLD Current
[23:16]	TRGnSPI selector bit. "1" for external trigger; "0" for SPI trigger HIT Current
[15:8]	HIT Time
[7:0]	• VDRnCDR selector bit. "1" for Voltage Drive Regulation; "0" for Current Drive Regulation (default). The VDRnCDR selector bit can only be changed when STATUS = OFF. See the *Functional Description - Two Levels Drive Sequence for Solenoid Valves* • HSnLS selector bit. "1" for High-Side Drive; "0" for Low-Side Drive (default). The HSnLS selector bit can only be changed when STATUS = OFF. • FREQ_CFG bits. See the *Chopping Frequency (FREQM, FRQ_CFG_)* section • SRC. "1" for Slew-Rate Controlled mode; "0" for Fast Mode (default) • OL_EN Enable bit. "1" Enable Open-Load Detection; "0" Disable Open-Load Detection (default) • HHF_EN Enable bit. "1" Enable HIT Current Detection; "0" HIT Current Detection (default)

Fault Register Description (FAULT)

The Fault Register is a 32-bit Read-only register that contains the Fault flag bits for each individual channel.

- The Most Significant Byte FAULT[31:24] stores the Overcurrent Protection Flag bits (OCP). Channel 0 corresponds to the Less Significant bit.
- The Second Most Significant Byte FAULT[23:16] stores the "HIT Current not reached Flag" bits (HHF). Channel 0 corresponds to the Less Significant bit.
- The Third Most Significant Byte FAULT[15:8] stores the "Open-Load Detection" Flag bits (OLF). Channel 0 corresponds to the Less Significant bit.
- The Less Significant Byte FAULT[7:0] stores the "Detection of Plunger Movement" Flag bits (MCF). Channel 0 corresponds to the Less Significant bit.

For more information, refer to *Protection and Diagnostic Functions* section.

Table 12. Fault Register

BIT	DESCRIPTION
32:24	OCP - Overcurrent Protection Flag Bits. Channel 0 is the LSB
23:16	HHF - HIT Current Not Reached Flag Bits. Channel 0 is the LSB
15:8	OLF - Open-Load Detection Flag Bits. Channel 0 is the LSB
7:0	DPM - Detection of Plunger Movement Flag Bits. Channel 0 is the LSB

Detection of Plunger Movement Register Description (CFG_DPM)

The CFG_DPM Register is a 32-bit register that can be used to configure the detection of plunger movement algorithm (refer to the *Detection of Plunger Movement (DPM)* section). Only the 15 least significant bits (CFG_DPM[14:0]) are used for DPM configuration. The Most significant Bits CFG_DPM[31:15] must be set at zero.

CFG_DPM[14:8] stores the value of the current used by the DPM algorithm as a starting current (DPM_ISTART[6:0]) for the search of the dip. The ISTART current is given by

ISTART = $DPM\_ISTART[6:0]_{DEC}$ x (IFS / 127), where IFS is the full-scale current.

CFG_DPM[7:4] stores the value of the DPM debouncer (DPM_TDEB[3:0]). This parameter determines the minimum duration of a current dip that the algorithm recognizes as a valid one. DPM_TDEB is expressed in terms of chopping periods:

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$DPM\_TDEB = DPM\_TDEB[3:0]_{DEC} / f_{CHOP}$

CFG_DPM[3:0] stores the value of the DPM Threshold (DPM_ITPH[3:0]) with which the current dip is compared. The I_{TPH} threshold is given by

$I_{TPH} = DPM\_ITPH[3:0]_{DEC} \times (I_{FS} / 127)$

Figure 4 shows the above DPM parameters with reference to a typical profile of the excitation current. The DPM algorithm starts monitoring the current above the I_{START} level and looks for a valid "current dip" until either the current reaches the HIT level (I_{HIT}) or the HIT time (t_{HIT}) ends. If no valid dip is encountered, a DPM fault is signaled out (if not masked).

It is recommended to set I_{START} just below the minimum current value at which the current dip due to the plunger movement is expected. The current dip is recognized as valid if the dip amplitude is greater than the DPM_IPTH threshold AND the dip duration is longer than the DPM_TDEB debounce time.

Low DPM_IPTH and DPM_TDEB values result in greater sensitivity, but can result in false positive detection of plunger movement caused by spurious signals.

The accuracy of the detection algorithm becomes less reliable if the dip is not pronounced enough.

Also, to ensure a reliable detection it is required that the slope of the current above the I_{START} level is slower than 700mA/ms so that the internal ADC can track it.

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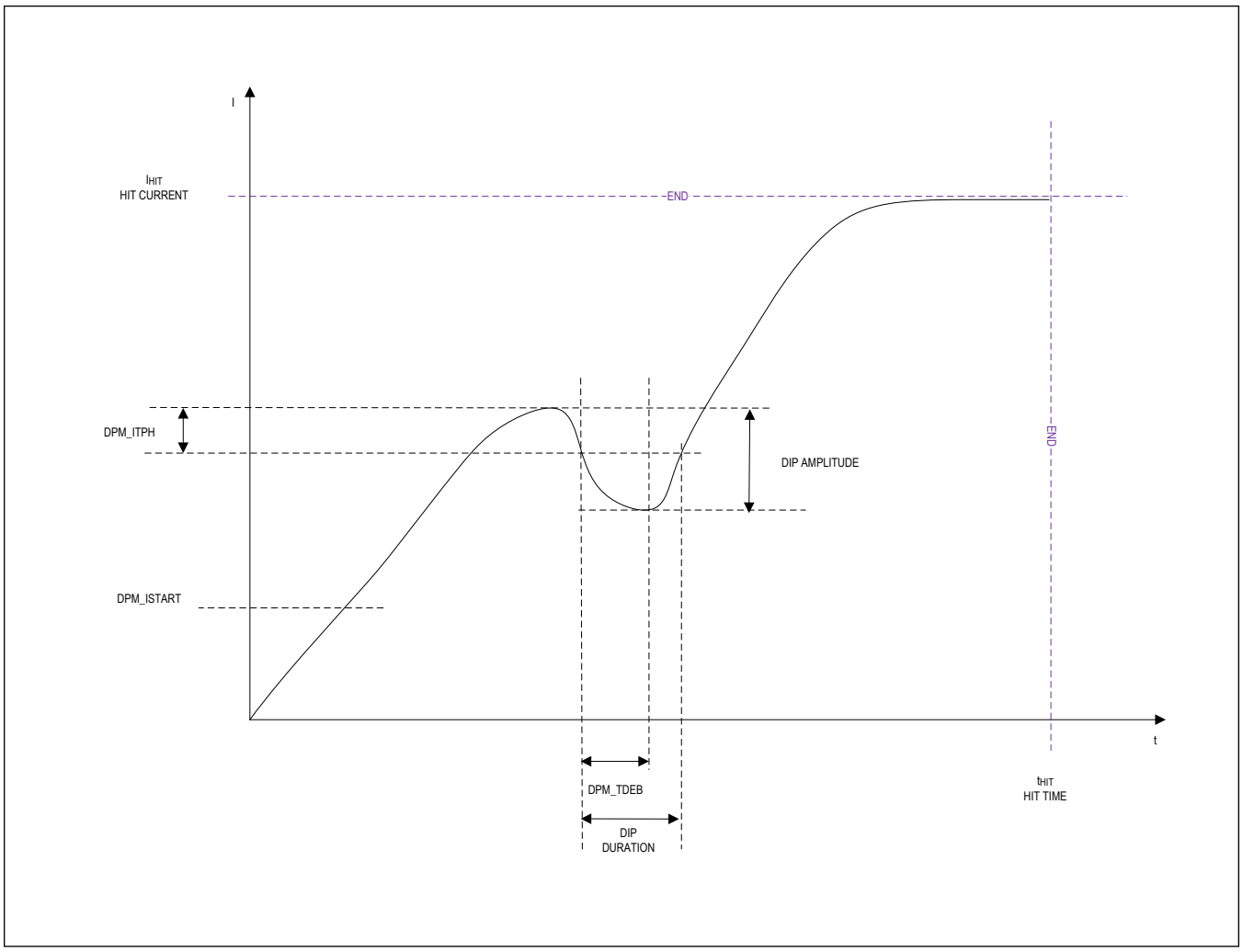

Figure 8. Detection of Plunger Movement

PRELIMINARY

Reading and Writing Operations of Registers

When the CMD pin is low, the SPI transfers are determined by the content of the preprogrammed Command Register. Two types of read/write data transfers are possible with 32 bits (see Figure 9 and Figure 10) or 8 bits (see Figure 11 and Figure 12). The 8/n32 bit into the Command Register, determines whether the data transfer of the follow on SPI is 8 or 32 bits long (see the *Command Register Description (COMMAND)* section).

Notice that when a Write/8-bit operation is executed (Figure 11) the MAX22200 outputs on SDO outputs the LSB of the STATUS register while when a Write/32-bit operation is executed (Figure 9), the MAX22200 outputs on SDO the STATUS plus the COMMAND register so that the user can check if the preprogrammed Command Register is set correctly.

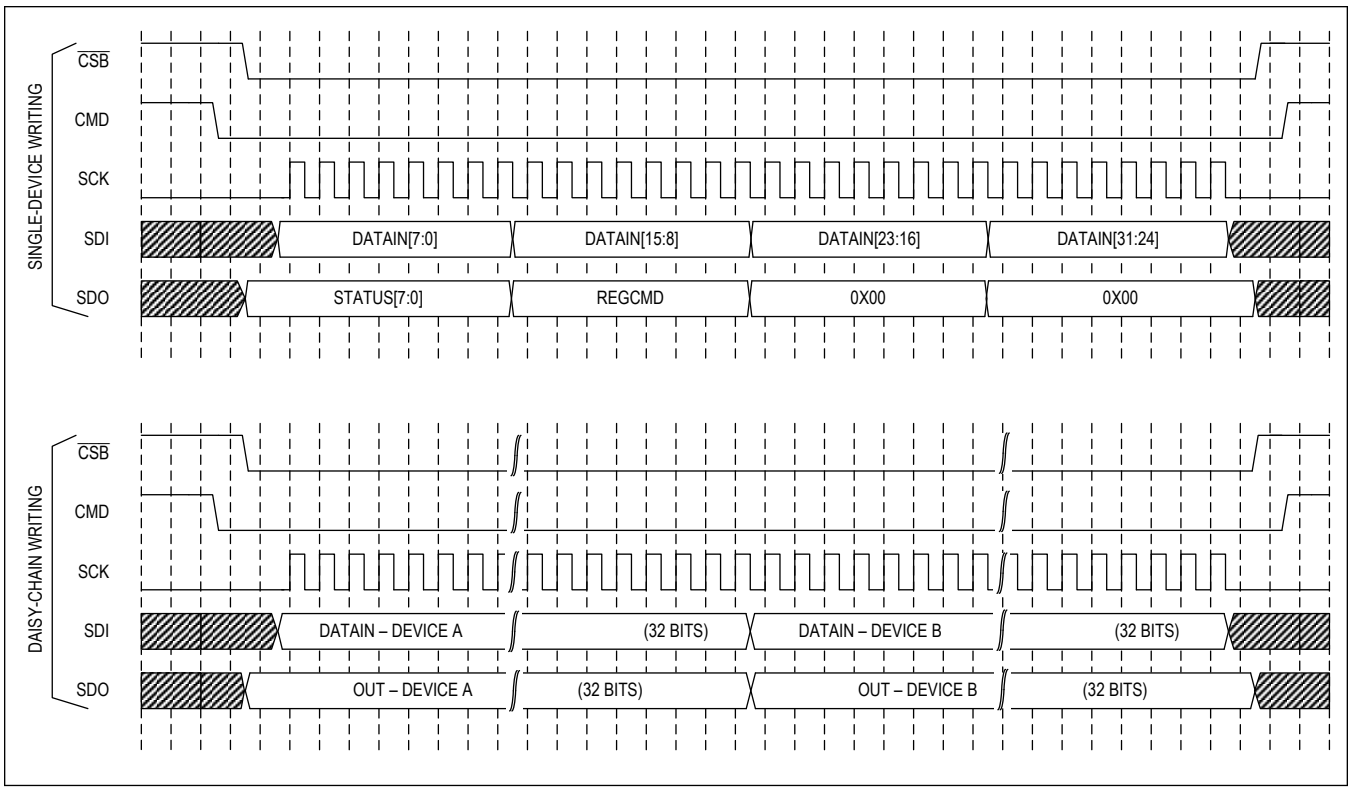

Figure 9. 32-Bit Register Writing—Timing Diagram

PRELIMINARY

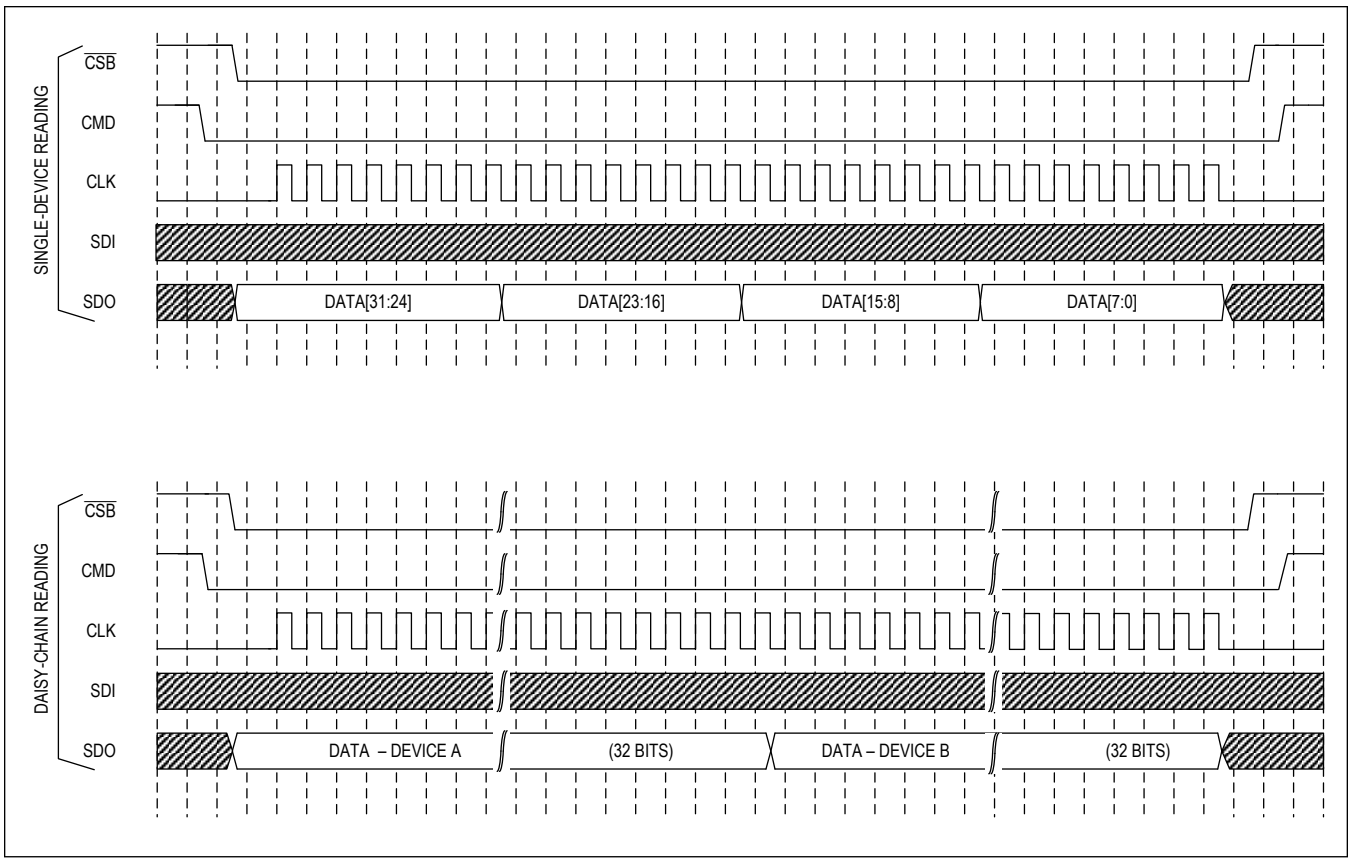

Figure 10. 32-Bit Register Reading—Timing Diagram

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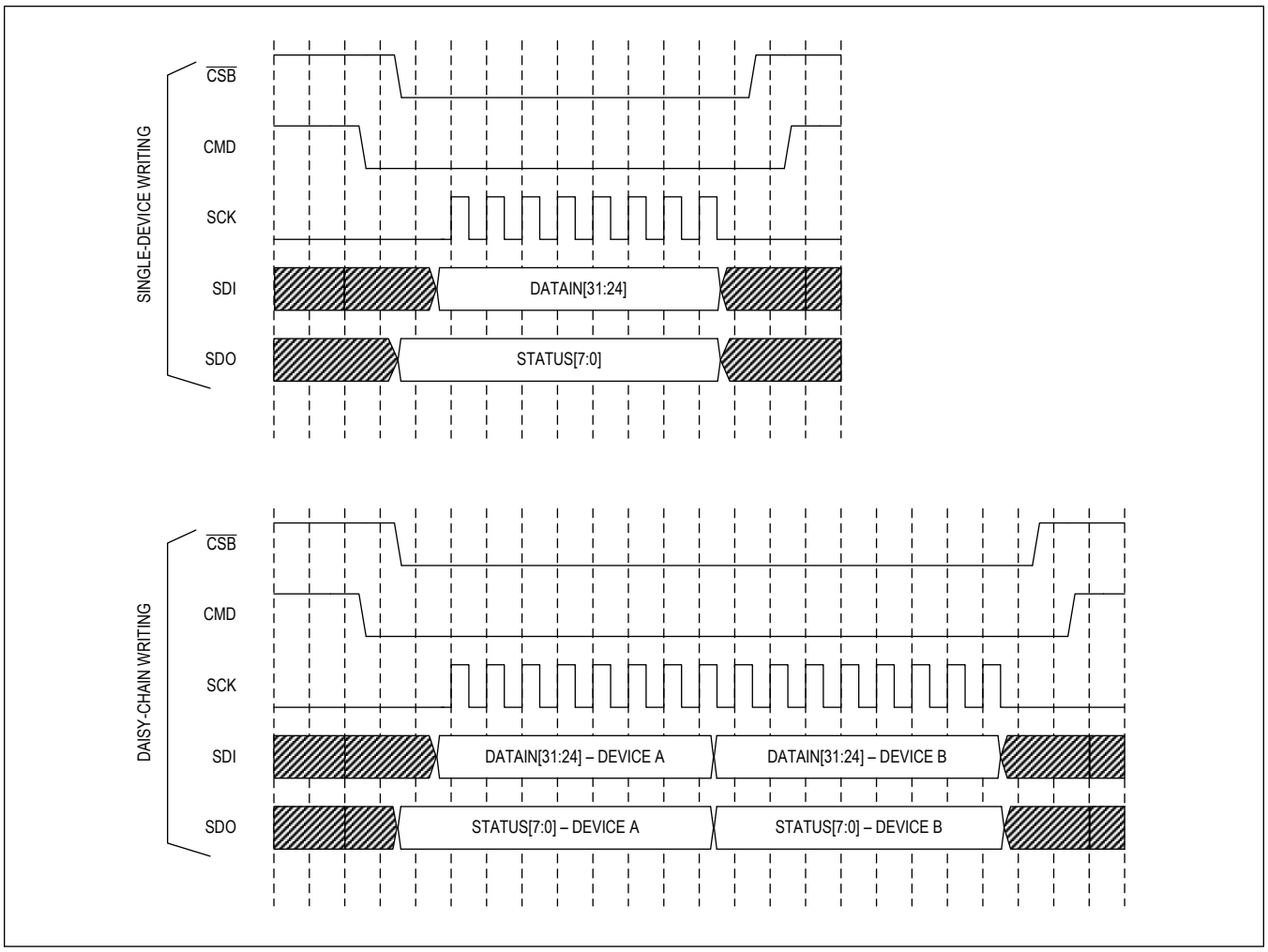

Figure 11. 8-Bit Register Writing—Timing Diagram

PRELIMINARY

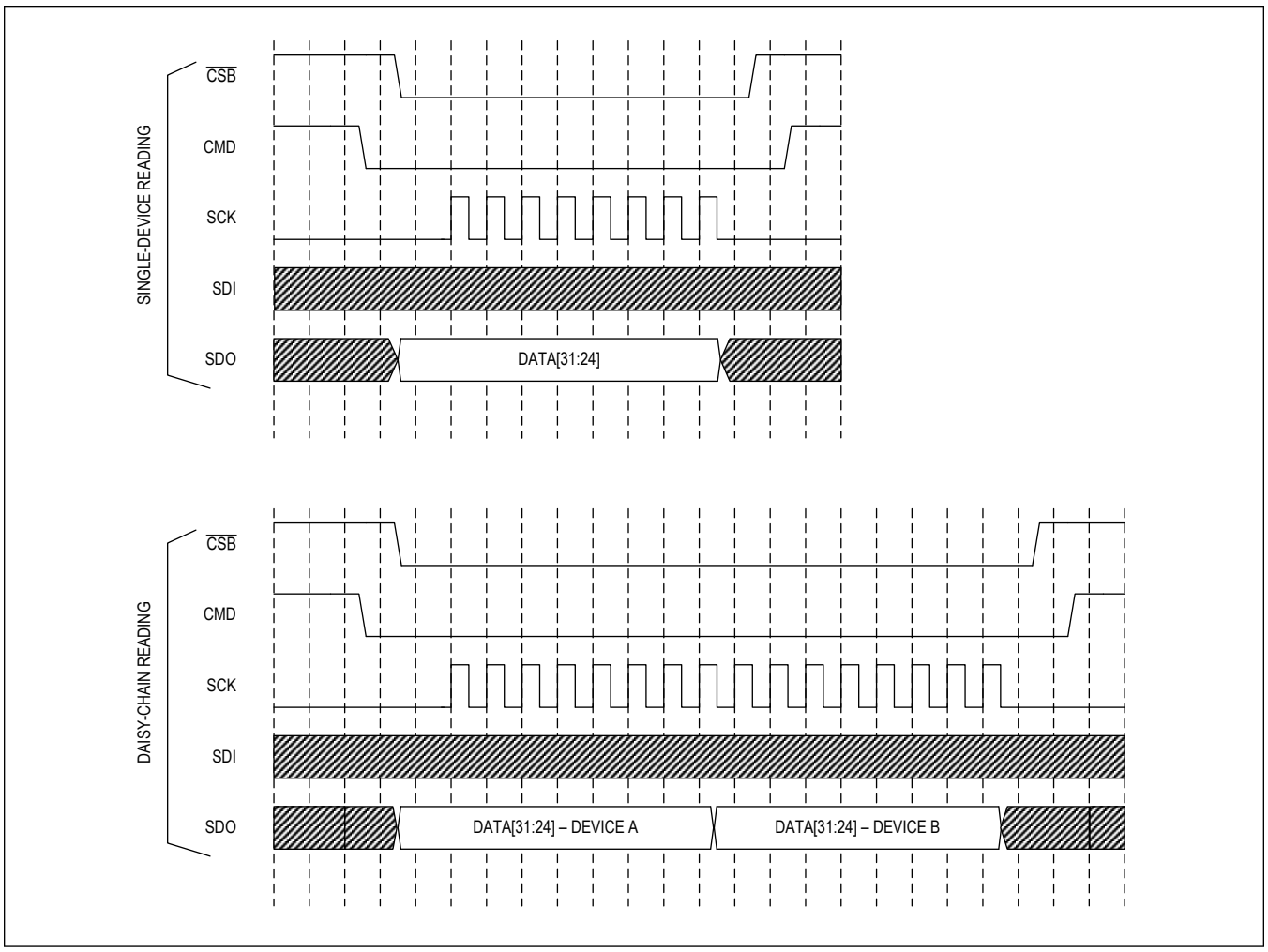

Figure 12. 8-Bit Register Reading—Timing Diagram

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Communication Error Detection (COMF)

For every write SPI transfer, the MAX22200 checks the number of clock cycles received. For a 32-bit write command, the control is performed on the first 32 clock cycles. After that, the control is on every 8 bits received (Figure 9). This is done in order to ensure the correct functionality of the device when it is connected in daisy chain. For an 8-bit write command, the control is performed every 8 clock cycles. If the number of clock cycles does not pass the check, a Communication Error is detected and the corresponding SPI transfer is ignored. Moreover the $\overline{\text{FAULT}}$ indication pin is asserted (if not masked).

Register Map

MAX22200 Register Map

ADDRESS	NAME	MSB							LSB
USER									
0x00	STATUS[31:24]	ONCH[7:0]							
	STATUS[23:16]	M_OVT	M_OCP	M_OLF	M_HHF	M_DPM	M_COMF	M_UVM	FREQM
	STATUS[15:8]	CM76[1:0]		CM54[1:0]		CM32[1:0]		CM10[1:0]	
	STATUS[7:0]	OVT	OCP	OLF	HHF	DPM	COMER	UVM	ACTIVE
0x01	CFG_CH 0[31:24]	HFS0	HOLD0[6:0]						
	CFG_CH 0[23:16]	TRGnSPI0	HIT0[6:0]						
	CFG_CH 0[15:8]	HIT_T0[7:0]							
	CFG_CH 0[7:0]	VDRnCDR0	HSnLS0	FREQ_CFG0[1:0]		SRC0	OL_EN0	DPM_EN0	HHF_EN0
0x02	CFG_CH 1[31:24]	HFS1	HOLD1[6:0]						
	CFG_CH 1[23:16]	TRGnSPI1	HIT1[6:0]						
	CFG_CH 1[15:8]	HIT_T1[7:0]							
	CFG_CH 1[7:0]	VDRnCDR1	HSnLS1	FREQ_CFG1[1:0]		SRC1	OL_EN1	DPM_EN1	HHF_EN1
0x03	CFG_CH 2[31:24]	HFS2	HOLD2[6:0]						
	CFG_CH 2[23:16]	TRGnSPI2	HIT2[6:0]						
	CFG_CH 2[15:8]	HIT_T2[7:0]							
	CFG_CH 2[7:0]	VDRnCDR2	HSnLS2	FREQ_CFG2[1:0]		SRC2	OL_EN2	DPM_EN2	HHF_EN2
0x04	CFG_CH 3[31:24]	HFS3	HOLD3[6:0]						
	CFG_CH 3[23:16]	TRGnSPI3	HIT3[6:0]						
	CFG_CH 3[15:8]	HIT_T3[7:0]							
	CFG_CH 3[7:0]	VDRnCDR3	HSnLS3	FREQ_CFG3[1:0]		SRC3	OL_EN3	DPM_EN3	HHF_EN3
0x05	CFG_CH 4[31:24]	HFS4	HOLD4[6:0]						
	CFG_CH 4[23:16]	TRGnSPI4	HIT4[6:0]						
	CFG_CH 4[15:8]	HIT_T4[7:0]							
	CFG_CH 4[7:0]	VDRnCDR4	HSnLS4	FREQ_CFG4[1:0]		SRC4	OL_EN4	DPM_EN4	HHF_EN4
0x06	CFG_CH 5[31:24]	HFS5	HOLD5[6:0]						
	CFG_CH 5[23:16]	TRGnSPI5	HIT5[6:0]						
	CFG_CH 5[15:8]	HIT_T5[7:0]							

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ADDRESS	NAME	MSB							LSB
	CFG_CH 5[7:0]	VDRnCDR5	HSnLS5	FREQ_CFG5[1:0]		SRC5	OL_EN5	DPM_EN5	HHF_EN5
0x07	CFG_CH 6[31:24]	HFS6	HOLD6[6:0]						
	CFG_CH 6[23:16]	TRGnSPI6	HIT6[6:0]						
	CFG_CH 6[15:8]	HIT_T6[7:0]							
	CFG_CH 6[7:0]	VDRnCDR6	HSnLS6	FREQ_CFG6[1:0]		SRC6	OL_EN6	DPM_EN6	HHF_EN6
0x08	CFG_CH 7[31:24]	HFS7	HOLD7[6:0]						
	CFG_CH 7[23:16]	TRGnSPI7	HIT7[6:0]						
	CFG_CH 7[15:8]	HIT_T7[7:0]							
	CFG_CH 7[7:0]	VDRnCDR7	HSnLS7	FREQ_CFG7[1:0]		SRC7	OL_EN7	DPM_EN7	HHF_EN7
0x09	FAULT[31:24]	OCP[7:0]							
	FAULT[23:16]	HHF[7:0]							
	FAULT[15:8]	OLF[7:0]							
	FAULT[7:0]	DPM[7:0]							
0x0A	CFG_DPM[31:24]	RSVD[10:3]							
	CFG_DPM[23:16]	RSVD[2:0]			RSVD	RSVD	RSVD	RSVD	RSVD
	CFG_DPM[15:8]	RSVD	DPM_ISTART[6:0]						
	CFG_DPM[7:0]	DPM_TDEB[3:0]				DPM_IPTH[3:0]			

Register Details

STATUS (0x00)

BIT	31	30	29	28	27	26	25	24
Field	ONCH[7:0]							
Reset	0x0							
Access Type	Write, Read							

BIT	23	22	21	20	19	18	17	16
Field	M_OVT	M_OCP	M_OLF	M_HHF	M_DPM	M_COMF	M_UVM	FREQM
Reset	0x0	0x0	0x0	0x0	0x0	0x1	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	15	14	13	12	11	10	9	8
Field	CM76[1:0]		CM54[1:0]		CM32[1:0]		CM10[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

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BIT	7	6	5	4	3	2	1	0
Field	OVT	OCP	OLF	HHF	DPM	COMER	UVM	ACTIVE
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x1	0x0
Access Type	Read Clears All	Read Only	Read Only	Read Only	Read Only	Read Only	Read Clears All	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ONCH	31:24	Channels Activation/Deactivation Bits	0: Half bridge is off 1: Half bridge is on
M_OVT	23	OVT fault mask bit	0x0: OVT signaled on the FAULT\ pin 0x1: OVT not signaled on the FAULT\ pin
M_OCP	22	OCP fault mask bit	0x0: OCP signaled on the FAULT\ pin 0x1: OCP not signaled on the FAULT\ pin
M_OLF	21	OLF fault mask bit	0x0: OLF signaled on the FAULT\ pin 0x1: OLF not signaled on the FAULT\ pin
M_HHF	20	HHF fault mask bit	0x0: HHC signaled on the FAULT\ pin 0x1: HHC not signaled on the FAULT\ pin
M_DPM	19	DPM Fault Mask Bit	0x0: DPM signaled on the FAULT\ pin 0x1: DPM not signaled on the FAULT\ pin
M_COMF	18	Comunication fault mask bit	0x0: MCOMER signaled on the FAULT\ pin 0x1: MCOMER not signaled on the FAULT\ pin
M_UVM	17	Undervoltage lockout fault mask bit	0x0: UV signaled on the FAULT\ pin 0x1: UV not signaled on the FAULT\ pin
FREQM	16	Internal oscillator frequency setting bit	0x0: 100kHz 0x1: 80kHz
CM76	15:14	CH6/CH7 operation mode configuration. CM76 bits can be written only when OCH6/ OCH7 are set to 0.	0x0: CH6/CH7 independently controlled by register CFG6/CFG7 0x1: CH6/CH7 in parallel mode both controlled by register CFG6 and ONCH6 0x2: CH6/CH7 H-Bridge mode - ONCH6 and ONCH7 control status and direction (00 = Hi-Z, 01 = Fwd, 10 = Rev, 11 = Brake). PWM regulation control on LS according to CFG6 0x3: Reserved
CM54	13:12	CH5/CH4 operation mode configuration. CM54 bits can be written only when OCH5/ OCH4 are set to 0.	0x0: CH4/CH5 independently controlled by register CFG4/CFG5 0x1: CH4/CH5 in parallel mode both controlled by register CFG4 and ONCH5 0x2: CH4/CH5 H-Bridge mode - ONCH4 and ONCH5 control status and direction (00 = Hi-Z, 01 = Fwd, 10 = Rev, 11 = Brake). PWM regulation control on LS according to CFG4 0x3: Reserved

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BITFIELD	BITS	DESCRIPTION	DECODE
CM32	11:10	CH3/CH2 operation mode configuration. CM32 bits can be written only when OCH3/ OCH2 are set to 0.	0x0: CH3/CH2 independently controlled by register CFG3/CFG2 0x1: CH3/CH2 in parallel mode both controlled by register CFG2 and ONCH2 0x2: CH3/CH2 H-Bridge mode - ONCH3 and ONCH2 control status and direction (00 = Hi-Z, 01 = Fwd, 10 = Rev, 11 = Brake). PWM regulation control on LS according to CFG2 0x3: Reserved
CM10	9:8	CH1/CH0 operation mode configuration. CM10 bits can be written only when OCH1/ OCH0 are set to 0.	0x0: CH0/CH1 independently controlled by register CFG0/CFG1 0x1: CH0/CH1 in parallel mode both controlled by register CFG0 and ONCH0 0x2: CH0/CH1 H-Bridge mode - ONCH0 and ONCH1 control status and direction (00 = Hi-Z, 01 = Fwd, 10 = Rev, 11 = Brake). PWM regulation control on LS according to CFG0 0x3: Reserved
OVT	7	Thermal protection flag bit	0x0: Normal operation 0x1: Chip is in thermal protection
OCP	6	Overcurrent protection flag bit	0x0: Normal operation 0x1: At least 1 channel has detected an overcurrent event
OLF	5	Open-load fault flag bit	0x0: Normal operation 0x1: At least 1 channel has detected an open load fault
HHF	4	HIT current not reached flag bit (CDR mode only)	0x0: Normal operation 0x1: At least 1 channel has detected a HIT current fault
DPM	3	DPM Fault Flag Bit	0x0: Normal operation 0x1: At least 1 channel has detected a Detection of Plunger Movement Fault
COMER	2	Communication error flag bit	0x0: No SPI error detected 0x1: SPI Write comunication error detected
UVM	1	Undervoltage lockout flag bit	0x0: Normal operation 0x1: VM UVLO event has been detected
ACTIVE	0	Active Bit	0x0: Low-power mode, chip off 0x1: Normal operation

CFG_CH (0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08)

BIT	31	30	29	28	27	26	25	24
Field	HFS	HOLD[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						

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BIT	23	22	21	20	19	18	17	16
Field	TRGnSPI	HIT[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						

BIT	15	14	13	12	11	10	9	8
Field	HIT_T[7:0]							
Reset	0x0							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	VDRnCDR	HSnLS	FREQ_CFG[1:0]		SRC	OL_EN	DPM_EN	HHF_EN
Reset	0x0	0x0	0x00		0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HFS	31	Full-Scale/Half-Full-Scale selection bit	0x0: 1 0x1: 0.5
HOLD	30:24	HOLD Current Configuration Bits	0: HS off, LS on (in HS mode) HS on, LS off (in LS mode) 1-126: VDR duty cycle setting (in HS mode) VDR duty cycle or CDR current setting (in LS mode) 127: HS on, LS off (in HS mode) HS off, LS on (in LS mode)
TRGnSPI	23	TRIG/SPI control selection bit	0x0: CH_ is controlled by ONCH_ SPI bit 0x1: CH_ is controlled by TRIG_ pin
HIT	22:16	HIT current configuration bits	0: HS off, LS on (in HS mode) HS on, LS off (in LS mode) 1-126: VDR duty cycle setting (in HS mode) VDR duty cycle or CDR current setting (in LS mode) 127: HS on, LS off (in HS mode) HS off, LS on (in SL mode)
HIT_T	15:8	HIT time configuration bIts	0: No HIT time 1-254: T_{HIT} = HIT_T_[7:0] x 40 / f_{CHOP} 255: Continous IHIT
VDRnCDR	7	Current-Drive/Voltage-Drive mode selection bit	0x0: CH_ is controlled in Current-Drive mode 0x1: CH_ is controlled Voltage-Drive mode
HSnLS	6	If VDRnCDR = 1 this bit allows the selection between high-side/low-side mode. If VDRnCDR = 0 the channel works always in low-side mode	0x0: CH_ works in low-side mode 0x1: CH_ works in high-side mode
FREQ_CFG	5:4	Chopping frequency configuration bits	0x0: FreqMain/4 0x1: FreqMain/3 0x2: FreqMain/2 0x3: FreqMain

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BITFIELD	BITS	DESCRIPTION	DECODE
SRC	3	Slew-rate control enable bit	0x0: Fast OUT transitions 0x1: OUT transition is slew-rate controlled in low-side mode
OL_EN	2	Open-load detection enable bit	0x0: Open-load diagnostic is disabled 0x1: Open-load diagnostic is enabled
DPM_EN	1	Detection of plunger movement enable bit	0x0: DPM fault diagnostic is disabled 0x1: DPM fault diagnostic is enabled
HHF_EN	0	HIT current check enable bit	0x0: HIT current reached diagnostic is disabled 0x1: HIT current reached diagnostic is enabled

FAULT (0x09)

BIT	31	30	29	28	27	26	25	24
Field	OCP[7:0]							
Reset								
Access Type	Read Clears All							
BIT	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	HHF[7:0]							
Reset								
Access Type	Read Clears All							
BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	OLF[7:0]							
Reset								
Access Type	Read Clears All							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	DPM[7:0]							
Reset								
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION
OCP	31:24	OCP protection flag
HHF	23:16	HIT current not reached flag
OLF	15:8	Open-load detection flag
DPM	7:0	Detection of plunger movement fault flag

CFG_DPM (0x0A)

BIT	31	30	29	28	27	26	25	24
Field	RSVD[10:3]							
Reset								
Access Type	Write, Read							

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BIT	23	22	21	20	19	18	17	16
Field	RSVD[2:0]			RSVD	RSVD	RSVD	RSVD	RSVD
Reset				0x0				0x0
Access Type	Write, Read			Read Only	Read Only	Write, Read	Read Only	Write 1 to Set, Read

BIT	15	14	13	12	11	10	9	8
Field	RSVD	DPM_ISTART[6:0]						
Reset								
Access Type	Write, Read	Write, Read						

BIT	7	6	5	4	3	2	1	0
Field	DPM_TDEB[3:0]				DPM_IPTH[3:0]			
Reset								
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	31:21	Reserved	Reserved
RSVD	20	Reserved	Reserved
RSVD	19	Reserved	Reserved
RSVD	18	Reserved	Reserved
RSVD	17	Reserved	Reserved
RSVD	16	Reserved	Reserved
RSVD	15	Reserved	Reserved
DPM_ISTART	14:8	Detection of plunger movement starting current	ISTART = $DPM\_ISTART[6:0]_{DEC}$ x (I_{FS} / 127)
DPM_TDEB	7:4	DPM BEMF debounce time	TDEB = $DPM\_TDEB[3:0]_{DEC}$ / f_{CHOP}
DPM_IPTH	3:0	DPM current dip threshold	IPTH = $DPM\_IPTH[3:0]_{DEC}$ x (I_{FS} / 127)

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Applications Information

Use Cases

The MAX22200 is designed for flexibility and covers different use cases:

1. Low-side CDR mode
2. Low-side VDR mode
3. High-side VDR mode
4. Bridge tied-load VDR mode (latched valves or brushed DC motors)
5. Bridge tied-load CDR mode (latched valves or brushed DC motors)

Each use case is supported with dedicated logic to ease the control. For instance, to support cases 4 and 5, the control provides simple SPI commands to drive brushed DC motors in forward, reverse, brake, and Hi-Z mode.

In addition to the aforementioned cases, pairs of half-bridges can be paralleled to double the driving current capability.

Current Rating

The maximum drive current is limited by two factors: overcurrent limitations and thermal limitation. The more restrictive of these two factors limits the current capability of the MAX22200.

When CDR is used, the current is internally limited by the regulation loop. When VDR is used, the current is limited by the overcurrent protection circuitry, which is set at 1.1A (min). In both the cases, for reliability reasons, we do not recommend to exceed $1A_{RMS}$ drive per channel.

The thermal limitation is due to the power losses inside the device, which cause the junction temperature to increase up to critical levels. The total power dissipation inside the device depends on several application parameters such as ambient temperature, PCB thermal characteristics, voltage supply, number of running channels, switching frequency, duty cycle, slew rate settings, etc. It must be understood that the thermal stress of the device, hence the maximum current allowed in a real application, strongly depends on the PCB thermal characteristics and environmental factors.

To ensure long term reliability and avoid device damages it is required that the junction temperature never exceeds $T_{J(MAX)}$ = 125°C. Figure 13, Figure 14, Figure 15, and Figure 16 show the Safe Operating Area ($I < I_{OCP}$ AND $T_J < T_{J(MAX)}$) assuming a standard JEDEC 2s2p Board.

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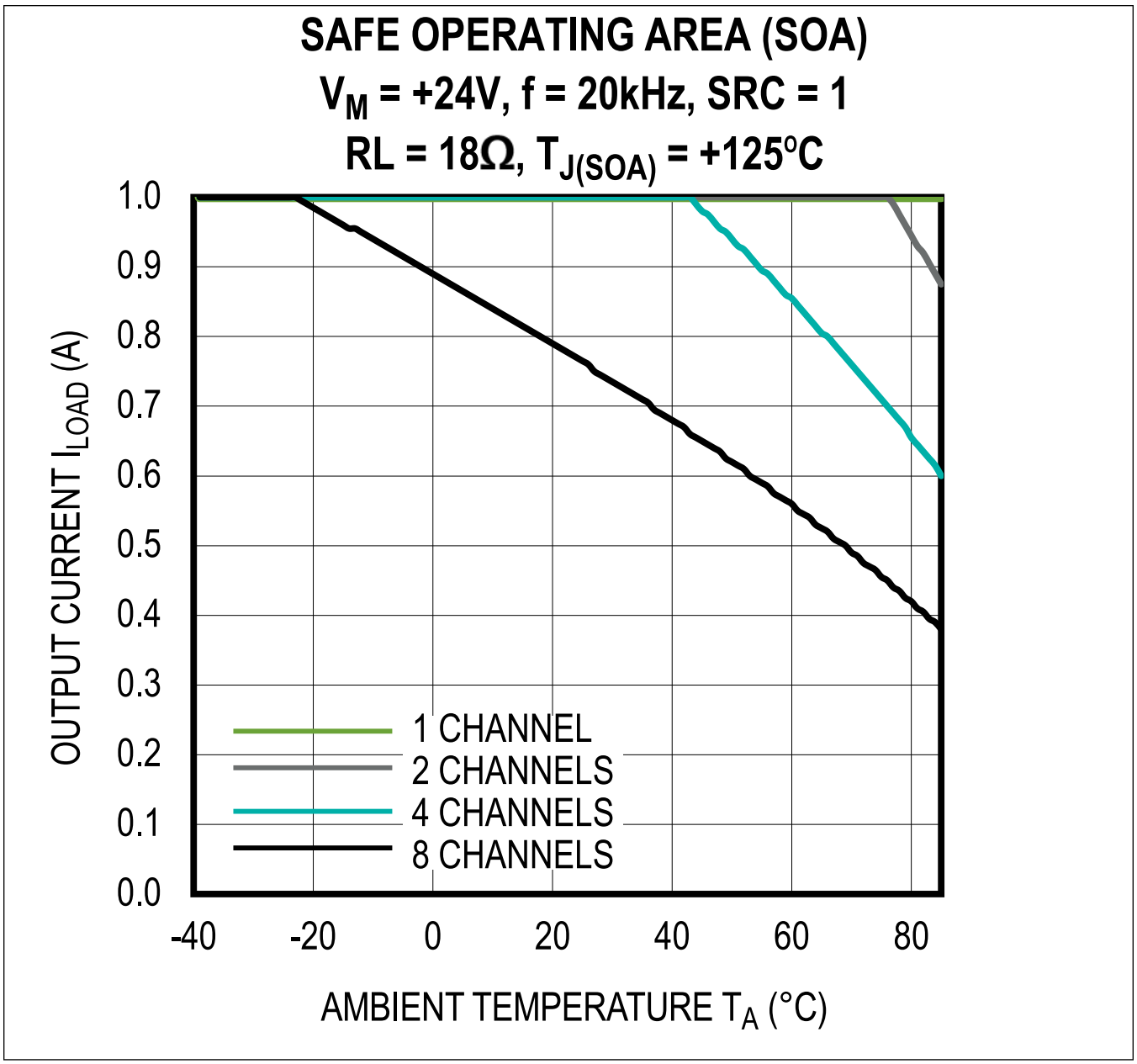


Figure 13. Safe Operating Area at +24V

PRELIMINARY

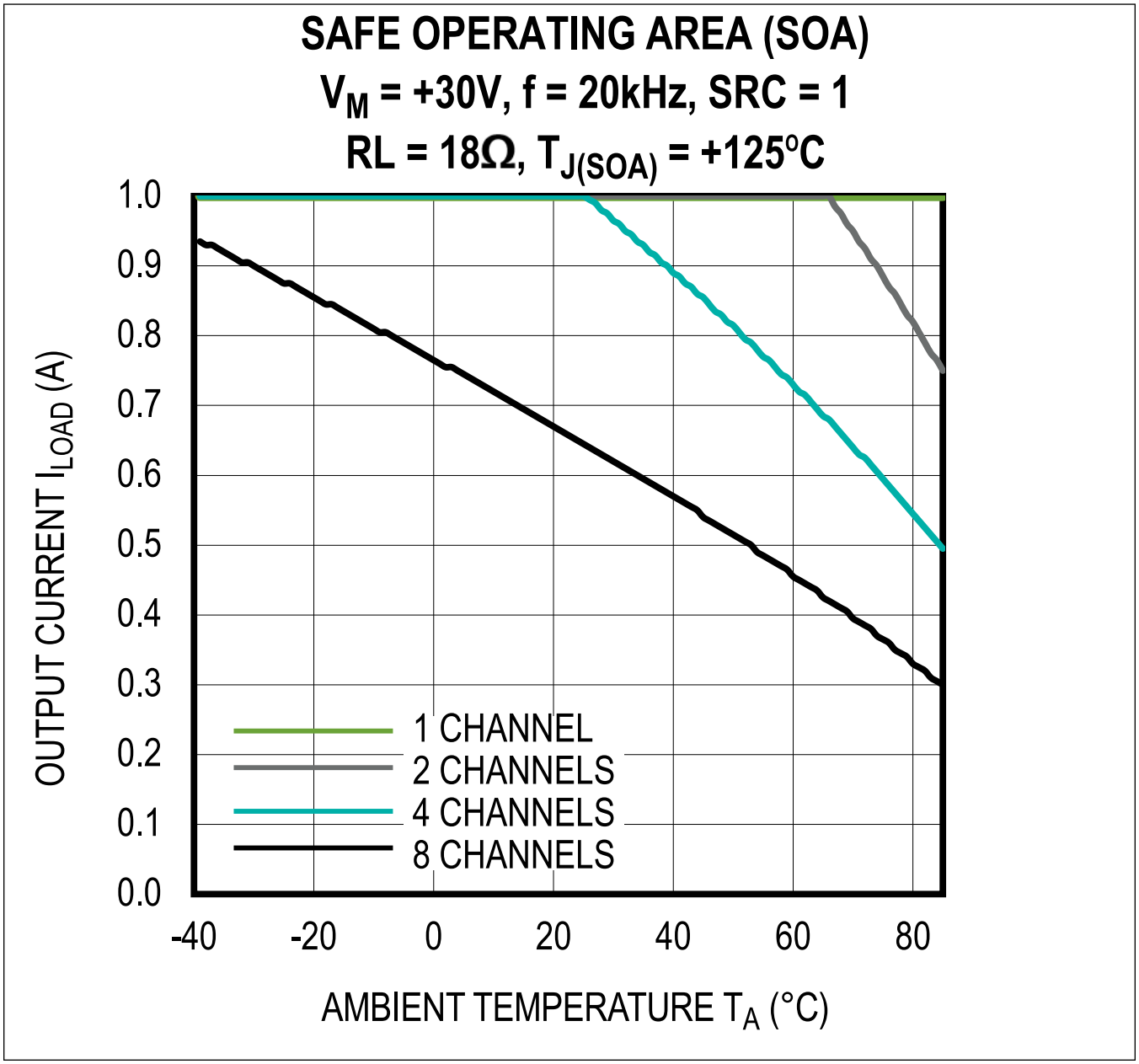


Figure 14. Safe Operating at Area +30V

PRELIMINARY

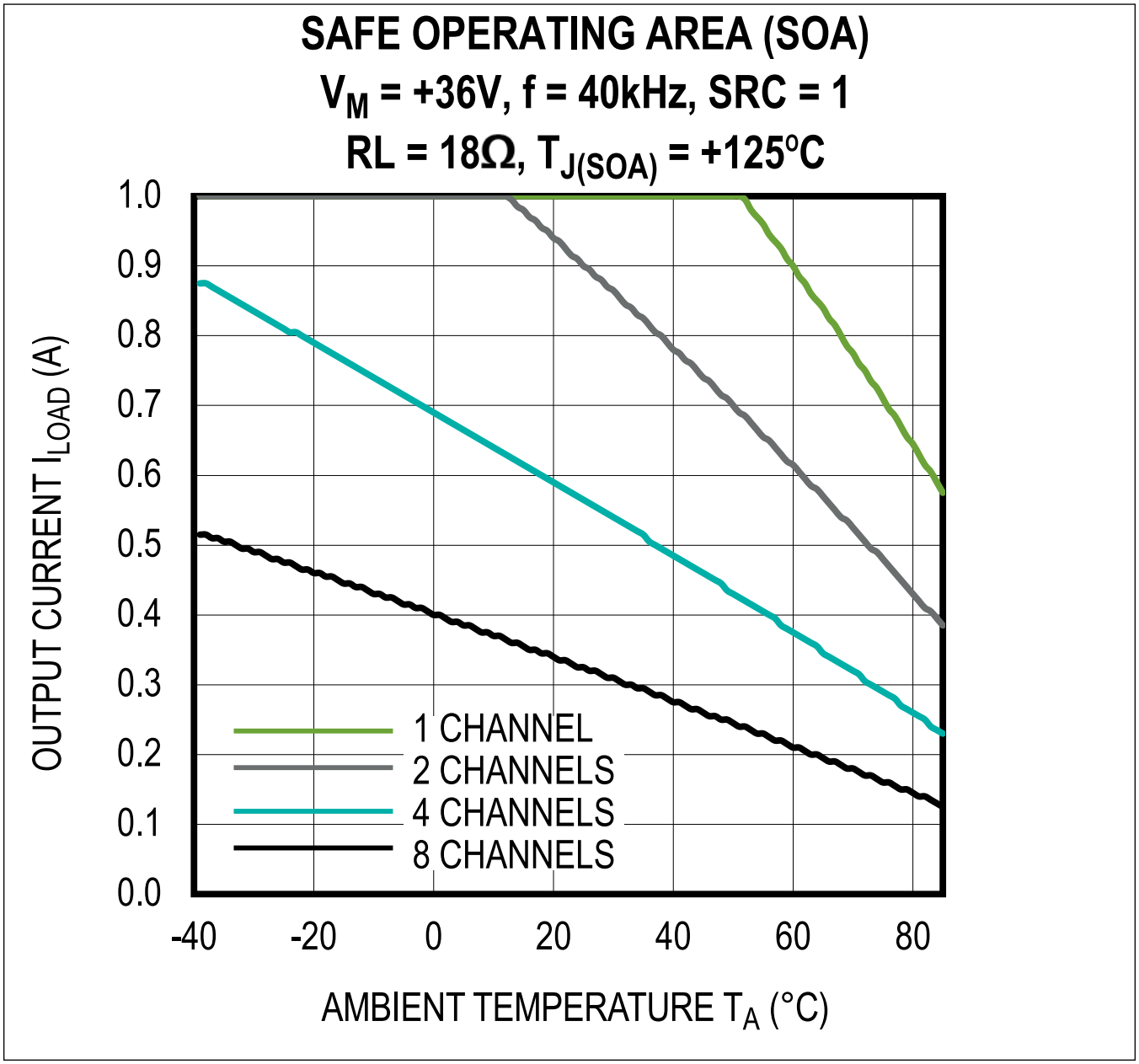


Figure 15. Safe Operating at Area +36V

PRELIMINARY

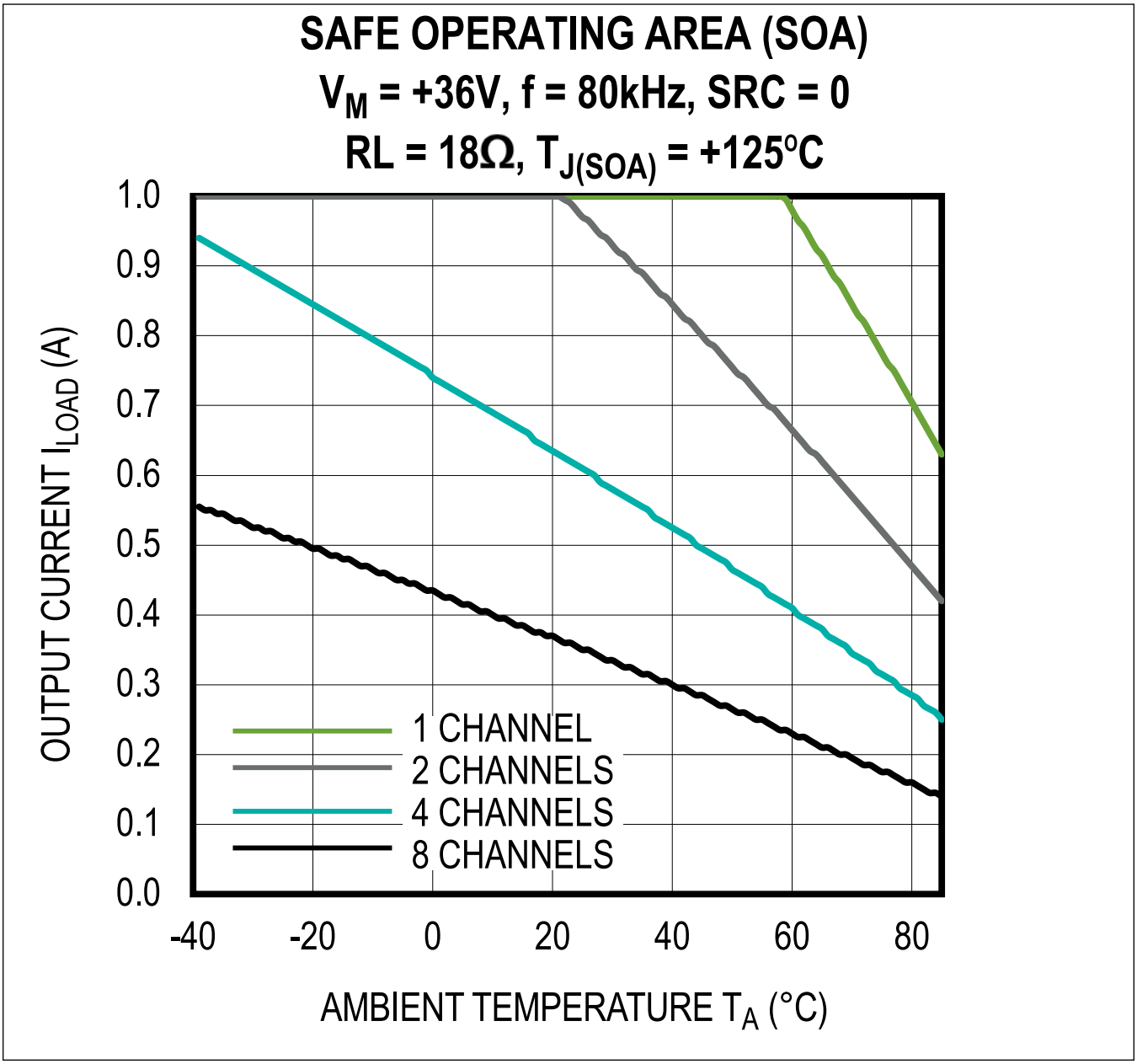


Figure 16. Safe Operating Area at +36V, SRC = 0

PRELIMINARY

Typical Application Circuits

Application Diagram

As a matter of example only, the *Application Diagram* shows an application of the MAX22200 in which:

- Channel 0 drives solenoid L0 tied to the GND (high-side driver configuration)

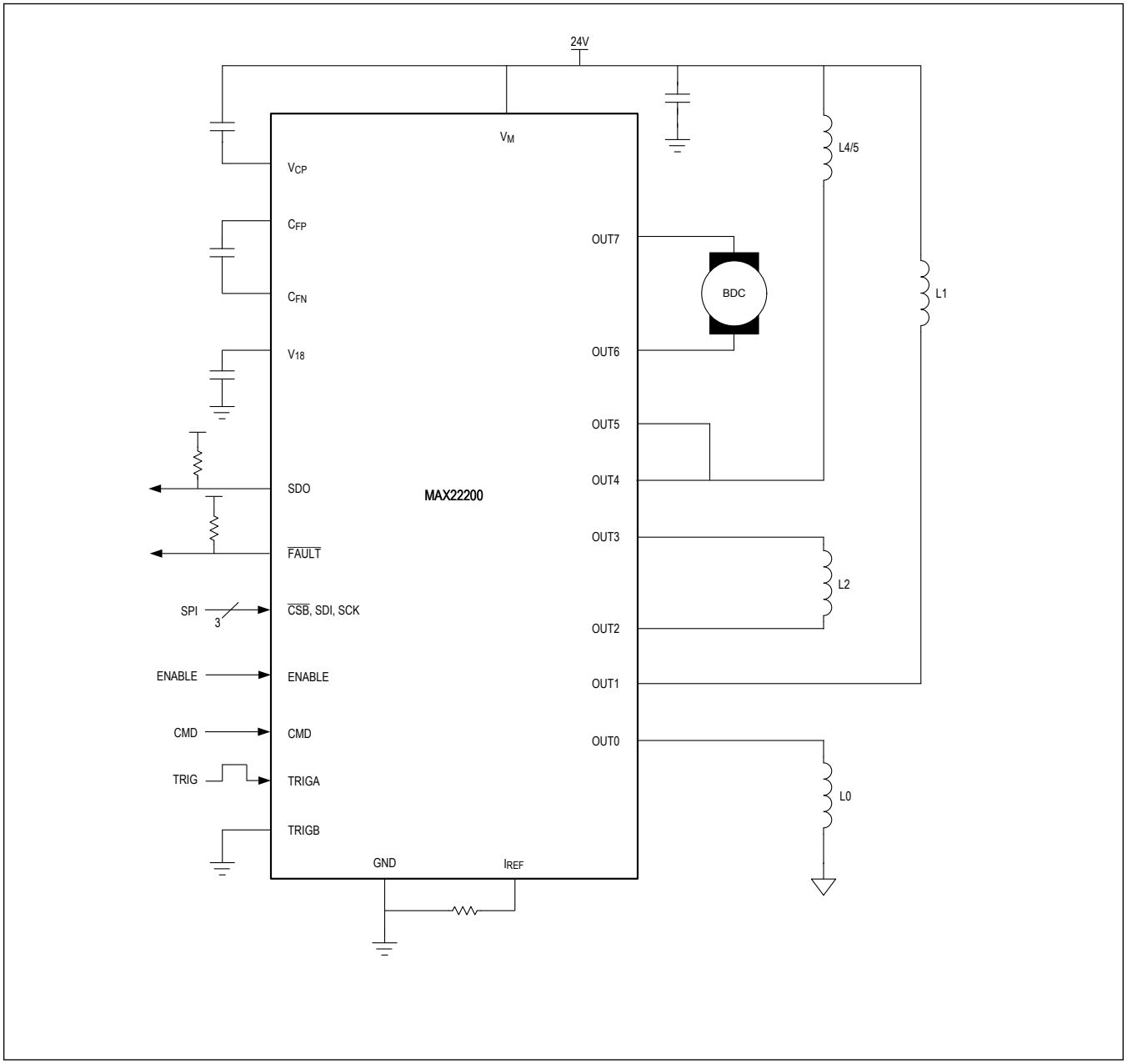
Typical Application Circuits (continued)

- Channel 1 drives solenoid L1 tied to the positive rail (low-side driver configuration)
- Channels 2 and 3 drive the Latched Valve L2 (full-bridge configuration).
- Channels 4 and 5 are connected in parallel and drive solenoid L4-5 tied to the positive rail (low-side driver configuration with parallelization).
- Channels 6 and 7 drive a Brushed DC Motor (full-bridge configuration)

Moreover, channels 4–7 are activated/deactivated through SPI (TRIGB is grounded) whereas one (or more) among channels 0–3 is activated using an external trigger signal (TRIGA).

PRELIMINARY

Typical Application Circuits (continued)



PRELIMINARY

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX22200ETJ+	-40°C to +85°C	32-TQFN 5x5mm

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

PRELIMINARY

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/20	Initial release	—

PRELIMINARY

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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