Data Sheet

AD9102

Low Power, 14 Bit, 180 MSPS, Digital-to-Analog Converter and Waveform Generator

FEATURES

- On-chip 4096 × 14-bit pattern memory
- On-chip DDS
- Power dissipation @ 3.3 V, 4 mA output
  - 96.54 mW @ 180 MSPS
- Sleep mode: <5 mW @ 3.3 V
- Supply voltage: 1.8 V to 3.3 V
- SFDR to Nyquist
  - 87 dBc @ 10 MHz output
- Phase noise @ 1 kHz offset, 180 MSPS, 8 mA: −150 dBc/Hz
- Differential current outputs: 8 mA max @ 3.3 V
- Small footprint, 32-lead, 5 mm × 5 mm LFCSP with 3.6 mm × 3.6 mm exposed paddle, and Pb-free package

APPLICATIONS

- Medical instrumentation
- Portable instrumentation
  - Signal generators, arbitrary waveform generators
- Automotive radar

GENERAL DESCRIPTION

The AD9102 TxDAC® and waveform generator is a high performance digital-to-analog converter (DAC) integrating on-chip pattern memory for complex waveform generation with a direct digital synthesizer (DDS).

The DDS is a 14-bit output, up to 180 MSPS main clock sine wave generator with a 24-bit tuning word, allowing 10.8 Hz/LSB frequency resolution.

SRAM data can include directly generated stored waveforms, amplitude modulation patterns applied to DDS outputs, or DDS frequency tuning words.

An internal pattern control state machine lets the user program the pattern period for the DAC as well the start delay within the pattern period for the signal output on the DAC.

A SPI interface is used to configure the digital waveform generator and load patterns into the SRAM.

A gain adjustment factor and an offset adjustment are applied to the digital signal on their way into the DAC.

The AD9102 offers exceptional ac and dc performance and supports DAC sampling rates of up to 180 MSPS.

The flexible power supply operating range of 1.8 V to 3.3 V and low power dissipation of the AD9102 make it well suited for portable and low power applications.

PRODUCT HIGHLIGHTS

1. High Integration: On-chip DDS and 4096 × 14 pattern memory
2. Low Power: Power-down mode provides for low power idle periods
3. Flexible Operation: 3- or 4-wire SPI interface; 1.8 V or 3.3 V supply

Rev. B

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REVISION HISTORY

7/2024—Rev. A to Rev. B

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FUNCTIONAL BLOCK DIAGRAM

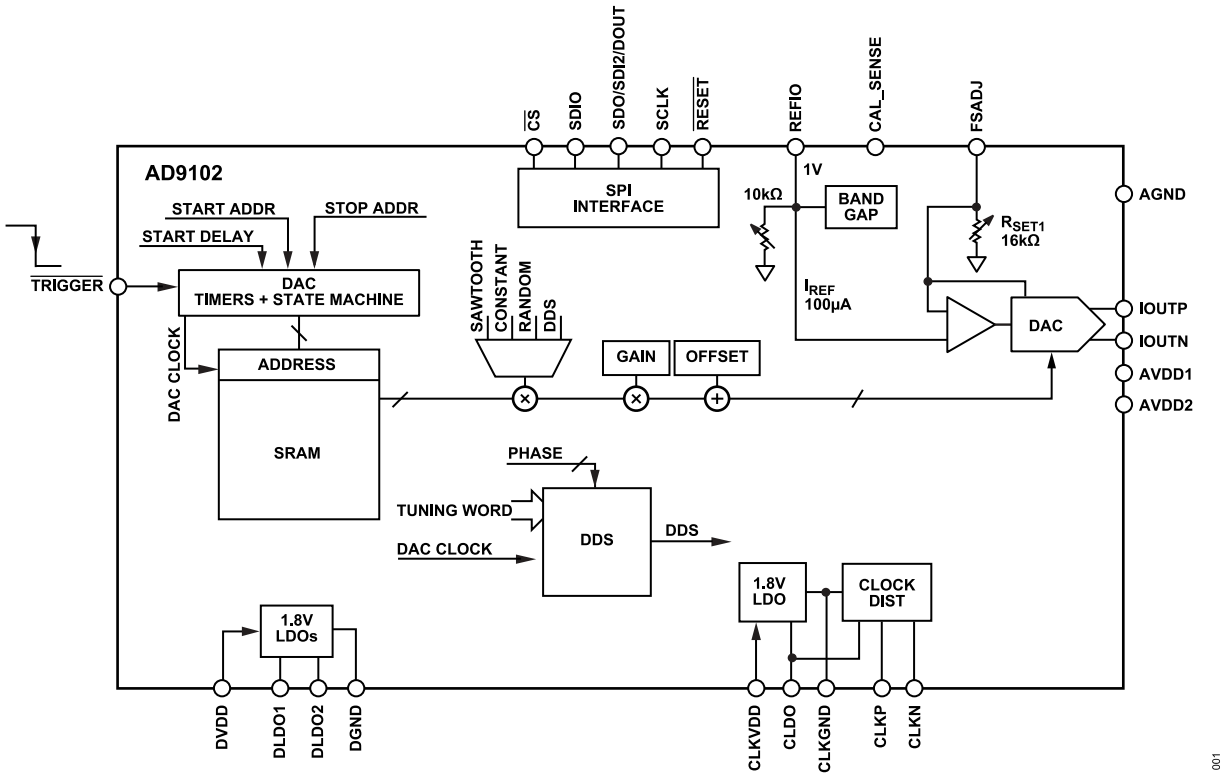

Figure 1.

SPECIFICATIONS

DC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}; AVDD = 3.3 V; DVDD = 3.3 V, CLKVDD = 3.3 V; internal CLDO, DLDO1 and DLDO2; I_{OUTFS} = 8 mA; maximum sample rate, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		14		Bits
ACCURACY @ 3.3 V				
Differential Nonlinearity (DNL)		±1.4		LSB
Integral Nonlinearity (INL)		±2.0		LSB
DAC OUTPUT				
Offset Error		±0.00025		% of FSR
Gain Error Internal Reference—No Automatic I_{OUTFS} Calibration	−1.0		+1.0	% of FSR
Full-Scale Output Current				
3.3 V	2	4	8	mA
Output Resistance		200		MΩ
Output Compliance Voltage	−0.5		+1.0	V
DAC TEMPERATURE DRIFT				
Gain with Internal Reference		±251		ppm/°C
Internal Reference Voltage		±119		ppm/°C
REFERENCE OUTPUT				
Internal Reference Voltage with AVDD = 3.3 V	0.8	1.0	1.2	V
Output Resistance		10		kΩ
REFERENCE INPUT				
Voltage Compliance	0.1		1.25	V
Input Resistance External Reference Mode		1		MΩ

DC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}; AVDD = 1.8 V; DVDD = DLDO1 = DLDO2 = 1.8 V; CLKVDD = CLDO = 1.8 V; I_{OUTFS} = 4 mA; maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
RESOLUTION		14		Bits
ACCURACY @ 1.8 V				
Differential Nonlinearity (DNL)		±1.5		LSB
Integral Nonlinearity (INL)		±1.4		LSB
DAC OUTPUTS				
Offset Error		±0.00025		% of FSR
Gain Error Internal Reference—No Automatic I_{OUTFS} Calibration	−1.0		+1.0	% of FSR
Full-Scale Output Current				
V_{CC} = 1.8 V	2	4	4	mA
Output Resistance		200		MΩ
Output Compliance Voltage	−0.5		+1.0	V
DAC TEMPERATURE DRIFT				
Gain		±228		ppm/°C
Reference Voltage		±131		ppm/°C
REFERENCE OUTPUT				
Internal Reference Voltage with AVDD = 1.8 V	0.8	1.0	1.2	V

SPECIFICATIONS

Table 2. (Continued)

Parameter	Min	Typ	Max	Unit
Output Resistance		10		kΩ
REFERENCE INPUT				
Voltage Compliance	0.1		1.25	V
Input Resistance External Reference Mode		1		MΩ

DIGITAL TIMING SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}; AVDD = 3.3 V; DVDD = 3.3 V, CLKVDD = 3.3 V, internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 8 mA; maximum sample rate, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKIN)				
Maximum Clock Rate	180			MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)	80			MHz
Minimum Pulse Width High		6.25		ns
Minimum Pulse Width Low		6.25		ns
Setup Time SDIO to SCLK	4.0			ns
Hold Time SDIO to SCLK	5.0			ns
Output Data Valid SCLK to SDO/SDI2/DOUT or SDIO		6.2		ns
Setup Time $\overline{CS}$ to SCLK	4.0			ns

DIGITAL TIMING SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}; AVDD = 1.8 V; DVDD = DLDO1 = DLDO2 = 1.8 V; CLKVDD = CLDO = 1.8 V; I_{OUTFS} = 4 mA; maximum sample rate, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKIN)				
Maximum Clock Rate	180			MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)	80			MHz
Minimum Pulse Width High		6.25		ns
Minimum Pulse Width Low		6.25		ns
Setup Time SDIO to SCLK	4.0			ns
Hold Time SDIO to SCLK	5.0			ns
Output Data Valid SCLK to SDO/SDI2/DOUT or SDIO		8.8		ns
Setup Time $\overline{CS}$ to SCLK	4.0			ns

INPUT/OUTPUT SIGNAL SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL (SCLK, $\overline{CS}$, SDIO, SDO/SDI2/DOUT, $\overline{RESET}$, $\overline{TRIGGER}$)					
Input V_{IN} Logic High	DVDD = 1.8 V	1.53			V
	DVDD = 3.3 V	2.475			V

SPECIFICATIONS

Table 5. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input V_{IN} Logic Low	DVDD = 1.8 V			0.27	V
	DVDD = 3.3 V			0.825	V
CMOS OUTPUT LOGIC LEVEL (SDIO, SDO/SDI2/DOUT)					
Output V_{OUT} Logic High	DVDD = 1.8 V	1.79			V
	DVDD = 3.3 V	3.28			V
Output V_{OUT} Logic Low	DVDD = 1.8 V			0.25	V
	DVDD = 3.3 V			0.625	V
DAC CLOCK INPUT (CLKP, CLKN)					
Minimum Peak-to-Peak Differential Input Voltage, V_{CLKP}/V_{CLKN}			150		mV
Maximum Voltage at V_{CLKP} or V_{CLKN}			V_{DVDD}		V
Minimum Voltage at V_{CLKP} or V_{CLKN}			V_{DGND}		V
Common-Mode Voltage	Generated on Chip		0.9		V

AC SPECIFICATIONS (3.3 V)

T_{MIN} to T_{MAX}; AVDD = 3.3 V; DVDD = 3.3 V, CLKVDD = 3.3 V, internal CLDO, DLDO1, and DLDO2; I_{OUTFS} = 8 mA; maximum sample rate, unless otherwise noted.

Table 6.

Parameter	Min	Typ	Max	Unit
SPURIOUS FREE DYNAMIC RANGE				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		87		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		67		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		88		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		68		dBc
NSD				
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		−163		dBm/Hz
PHASE NOISE @ 1 kHz FROM CARRIER				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		−150		dBc/Hz
DYNAMIC PERFORMANCE				
Output Settling Time, Full-Scale Output Step (to 0.1%)[1]		31.2		ns
Trigger to Output Delay, f_{DAC} = 180 MSPS[2]		96		ns
Rise Time, Full-Scale Swing[1]		3.25		ns
Fall Time, Full-Scale Swing[1]		3.26		ns

[1] Based on 85 Ω resistors from DAC output terminals to ground.

[2] Start delay = 0 f_{DAC} clock cycles.

AC SPECIFICATIONS (1.8 V)

T_{MIN} to T_{MAX}; AVDD = 1.8 V; DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V; I_{OUTFS} = 4 mA; maximum sample rate, unless otherwise noted.

Table 7.

Parameter	Min	Typ	Max	Unit
SPURIOUS FREE DYNAMIC RANGE (SFDR)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		84		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		73		dBc

SPECIFICATIONS

Table 7. (Continued)

Parameter	Min	Typ	Max	Unit
TWO-TONE INTERMODULATION DISTORTION (IMD)				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		91		dBc
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		86		dBc
NSD				
f_{DAC} = 180 MSPS, f_{OUT} = 50 MHz		−163		dBm/Hz
PHASE NOISE @ 1kHz FROM CARRIER				
f_{DAC} = 180 MSPS, f_{OUT} = 10 MHz		−150		dBc/Hz
DYNAMIC PERFORMANCE				
Output Settling Time (to 0.1%)[1]		31.2		ns
Trigger to Output Delay, f_{DAC} = 180 MSPS[2]		96		ns
Rise Time[1]		3.25		ns
Fall Time[1]		3.26		ns

[1] Based on 85 Ω resistors from DAC output terminals to ground.

[2] Start delay = 0 f_{DAC} clock cycles.

POWER SUPPLY VOLTAGE INPUTS AND POWER DISSIPATION

Table 8.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG SUPPLY VOLTAGES					
AVDD1, AVDD2		1.7		3.6	V
CLKVDD		1.7		3.6	V
CLDO	On-chip LDO not in use	1.7		1.9	V
DIGITAL SUPPLY VOLTAGES					
DVDD		1.7		3.6	V
DLDO1, DLDO2	On-chip LDO not in use	1.7		1.9	V
POWER CONSUMPTION	AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, internal CLDO, DLDO1, AND DLDO2				
f_{DAC} = 180 MSPS, Pure CW Sine Wave	12.5 MHz (DDS only)		96.54		mW
I_{AVDD}			7.67		mA
I_{DVDD}					
DDS Only	CW sine wave output		17.73		mA
RAM Only	50% duty cycle FS pulse output		11.31		mA
DDS and RAM Only	50% duty cycle sine wave output		14.6		mA
I_{CLKVDD}			3.85		mA
Power-Down Mode	REF on, DACs sleep, CLK power down, external CLK and supplies on		4.73		mW
POWER CONSUMPTION	AVDD = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V				
f_{DAC} = 180 MSPS, Pure CW Sine Wave	12.5 MHz (DDS only)		51.33		mW
I_{AVDD}			7.54		mA
I_{DVDD}			0.15		mA
I_{DLDO2}					
DDS Only	CW sine wave output		16.03		mA
RAM Only	50% duty cycle FS pulse output		10.07		mA
DDS and RAM Only	50% duty cycle sine wave output		13.26		mA
I_{DLDO1}			1.129		mA
I_{CLKVDD}			0.0096		mA

SPECIFICATIONS

Table 8. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
I_{CLDO}			3.65		mA
Power-Down Mode	REF on, DACs sleep, CLK power down, external CLK and supplies on		1.49		mW

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
AVDD1, AVDD2, DVDD to AGND, DGND, CLKGND	−0.3 V to +3.9 V
CLKVDD to AGND, DGND, CLKGND	−0.3 V to +3.9 V
CLDO, DLDO1, DLDO2 to AGND, DGND, CLKGND	−0.3 V to 2.2 V
AGND to DGND, CLKGND	−0.3 V to +0.3 V
DGND to AGND, CLKGND	−0.3 V to +0.3 V
CLKGND to AGND, DGND	−0.3 V to +0.3 V
$\overline{CS}$, SDIO, SCLK, SDO/SDI2/DOUT, $\overline{RESET}$, $\overline{TRIGGER}$ to DGND	−0.3 V to DVDD + 0.3 V
CLKP, CLKN to CLKGND	−0.3 V to CLKVDD + 0.3 V
REFIO to AGND	−1.0 V to AVDD + 0.3 V
IOUTP, IOUTN to AGND	−0.3 V to DVDD + 0.3 V
FSADJ, CAL_SENSE to AGND	−0.3 V to AVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a standard circuit board for surface-mount packages. θ_{JC} is measured from the solder side (bottom) of the package.

Table 10. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
32-Lead LFCSP with Exposed Paddle	30.18	6.59	3.84	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

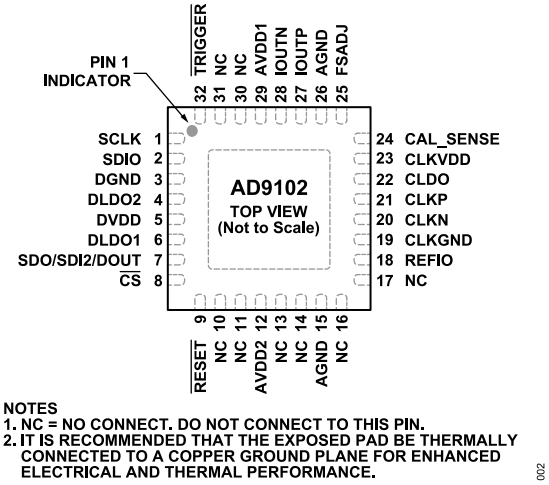

Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	SPI Clock Input.
2	SDIO	SPI Data Input/Output. Primary bidirectional data line for the SPI port.
3	DGND	Digital Ground.
4	DLDO2	1.8 V Internal Digital LDO2 Output. When the internal digital LDO2 is enabled, bypass this pin with a 0.1 µF capacitor.
5	DVDD	3.3 V External Digital Power Supply. DVDD defines the level of the digital interface of the AD9102 (SPI interface).
6	DLDO1	1.8 V Internal Digital LDO1 Output. When the internal digital LDO1 is enabled, bypass this pin with a 0.1 µF capacitor.
7	SDO/SDI2/DOUT	Serial Data Output (SDO). In 4-wire SPI mode, this pin outputs the data from the SPI. Digital I/O Pin. Second Data Input Line (SDI2). In double-SPI mode, this pin is a second data input line, SDI2, for the SPI port used to write to the SRAM. Pulse Output (DOUT). In data out mode, this terminal is a programmable pulse output.
8	$\overline{CS}$	SPI Port Chip Select, Active Low.
9	$\overline{RESET}$	Active Low Reset Pin. Resets registers to their default values.
10	NC	Not Connected. Do not connect to this pin.
11	NC	Not Connected. Do not connect to this pin.
12	AVDD2	1.8 V to 3.3 V Power Supply Input.
13	NC	Not Connected. Do not connect to this pin.
14	NC	Not Connected. Do not connect to this pin.
15	AGND	Analog Ground.
16	NC	Not Connected. Do not connect to this pin.
17	NC	Not Connected. Do not connect to this pin.
18	REFIO	DAC Voltage Reference Input/Output.
19	CLKGND	Clock Ground.
20	CLKN	Clock Input, Negative Side.
21	CLKP	Clock Input, Positive Side.
22	CLDO	Clock Power Supply Output (Internal Regulator in Use), Clock Power Supply Input (Internal Regulator Bypassed).
23	CLKVDD	Clock Power Supply Input.
24	CAL_SENSE	Sense Input for Automatic I_{OUTFS} Calibration.
25	FSADJ	External Full-Scale Current Output Adjust for DAC or Full-Scale Current Output Adjust Reference for Automatic I_{OUTFS} Calibration.
26	AGND	Analog Ground.
27	IOUTP	DAC Current Output, Positive Side.
28	IOUTN	DAC Current Output, Negative Side.
29	AVDD1	1.8 V to 3.3 V Power Supply Input for DAC.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 11. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
30	NC	Not Connected. Do not connect to this pin.
31	NC	Not Connected. Do not connect to this pin.
32	$\overline{\text{TRIGGER}}$	Pattern Trigger Input.
	EPAD	Exposed Pad. It is recommended that the exposed pad be thermally connected to a copper ground plane for enhanced electrical and thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, internal CLDO, DLDO1, and DLDO2.

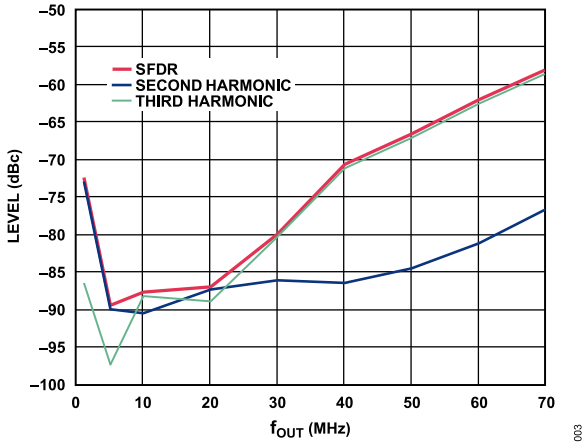

Figure 3. SFDR, 2nd and 3rd Harmonics vs. f_{OUT} at I_{OUTFS} = 8 mA

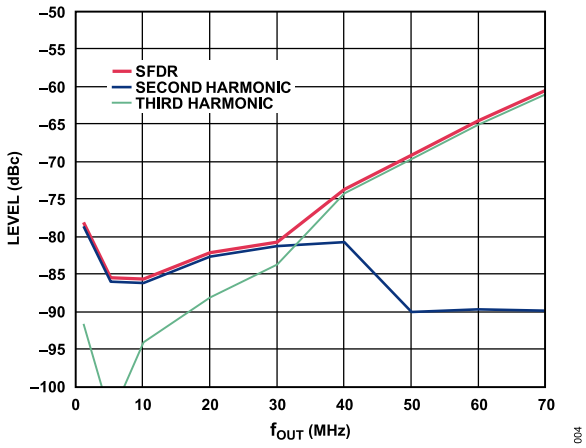

Figure 4. SFDR, 2nd and 3rd Harmonics vs. f_{OUT} at I_{OUTFS} = 4 mA

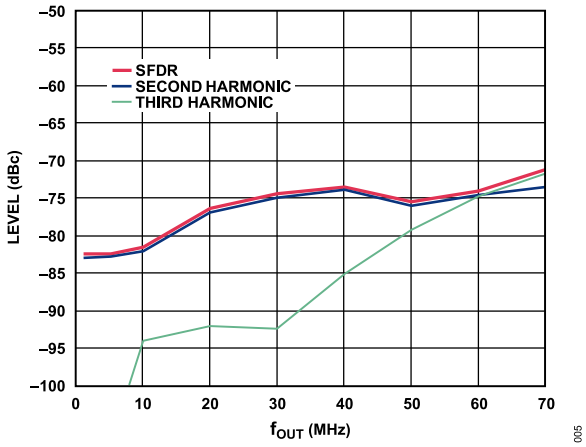

Figure 5. SFDR, 2nd and 3rd Harmonics vs. f_{OUT} at I_{OUTFS} = 2 mA

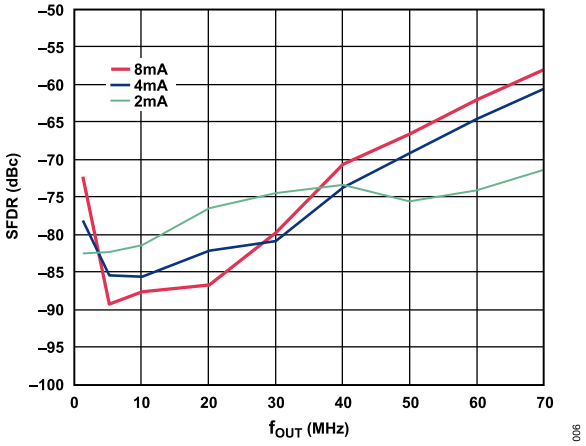

Figure 6. SFDR vs. f_{OUT} at Three I_{OUTFS} Values

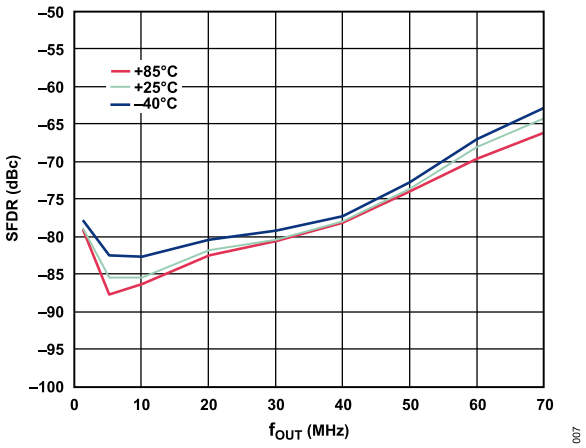

Figure 7. SFDR vs. f_{OUT} at Three Temperatures

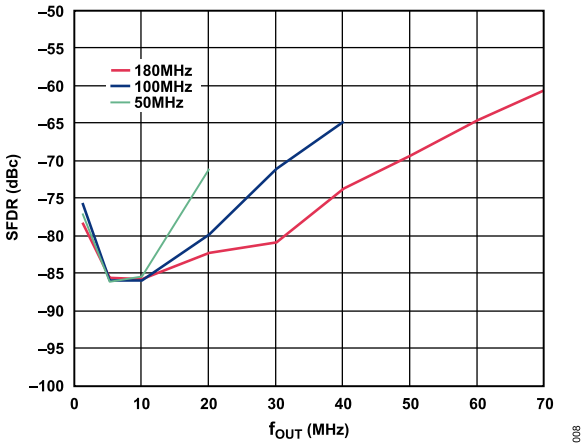

Figure 8. SFDR vs. f_{OUT} at Three f_{DAC} Values

TYPICAL PERFORMANCE CHARACTERISTICS

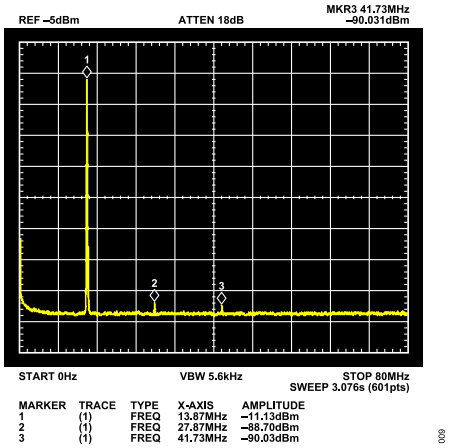

Figure 9. Output Spectrum, f_{OUT} = 13.87 MHz

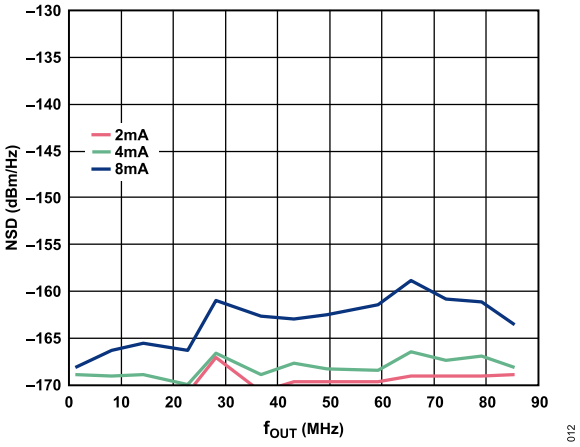

Figure 12. NSD vs. f_{OUT} at Three I_{OUTFS} Values

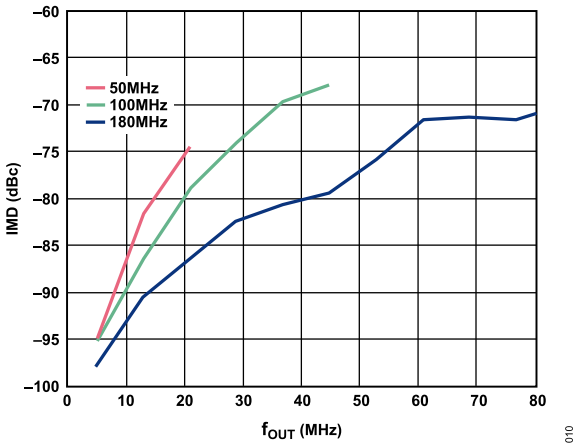

Figure 10. IMD vs. f_{OUT} at Three f_{DAC} Values

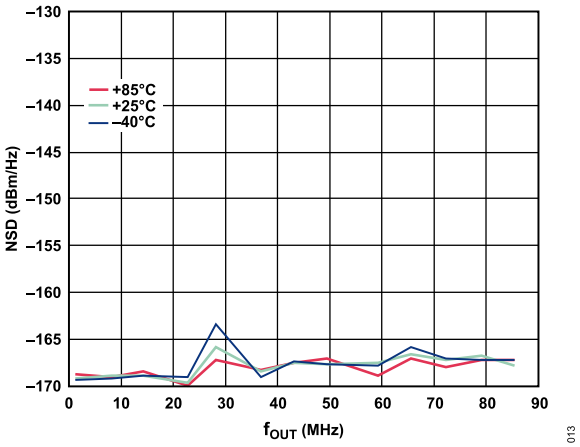

Figure 13. NSD vs. f_{OUT} at Three Temperatures

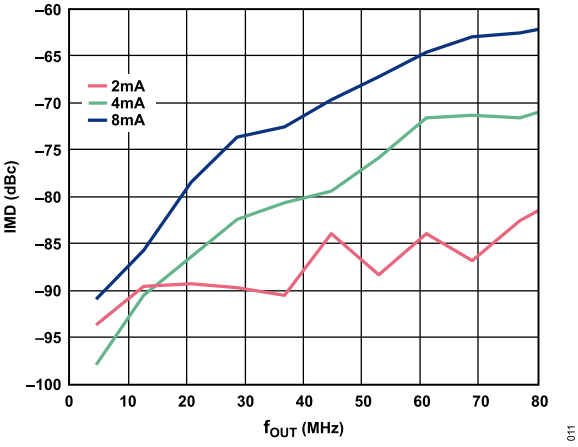

Figure 11. IMD vs. f_{OUT} at Three I_{OUTFS} Values

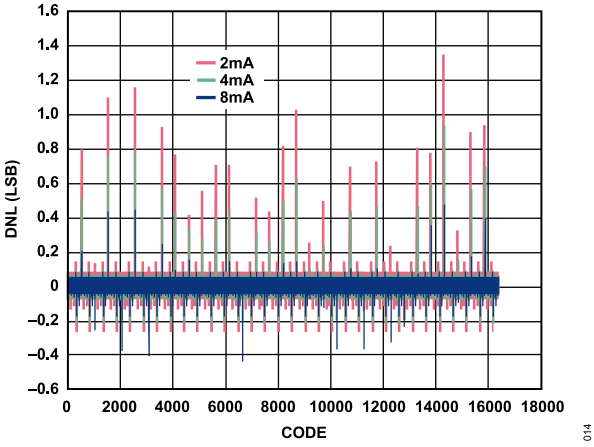

Figure 14. DNL, Three I_{OUTFS} Values

TYPICAL PERFORMANCE CHARACTERISTICS

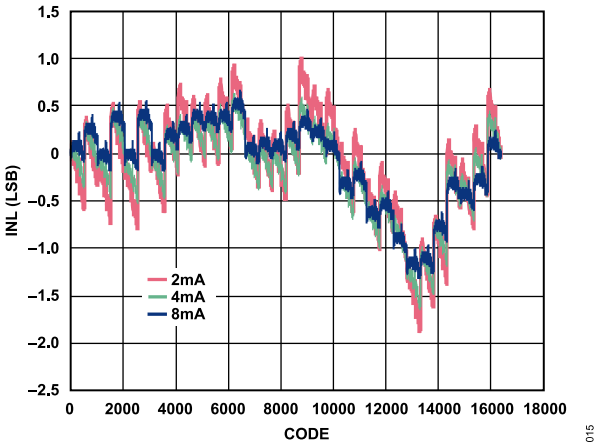

Figure 15. INL, Three I_{OUTFS} Values

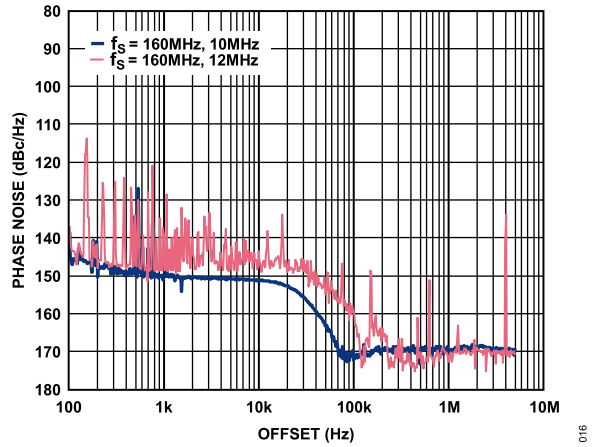

Figure 16. Phase Noise

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DVDD = DLDO1 = DLDO2 = 1.8 V, CLKVDD = CLDO = 1.8 V

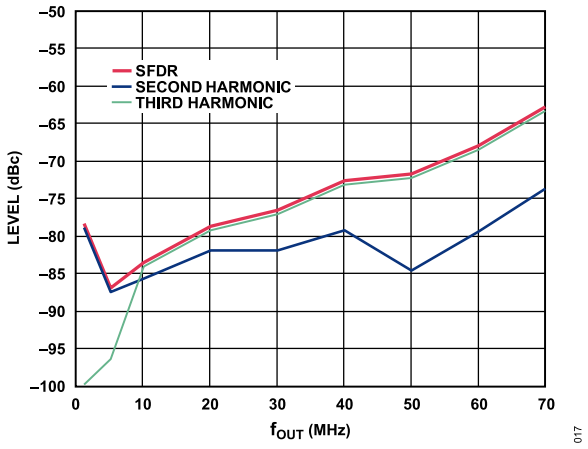

Figure 17. SFDR, 2nd and 3rd Harmonics vs. f_{OUT} at I_{OUTFS} = 4 mA

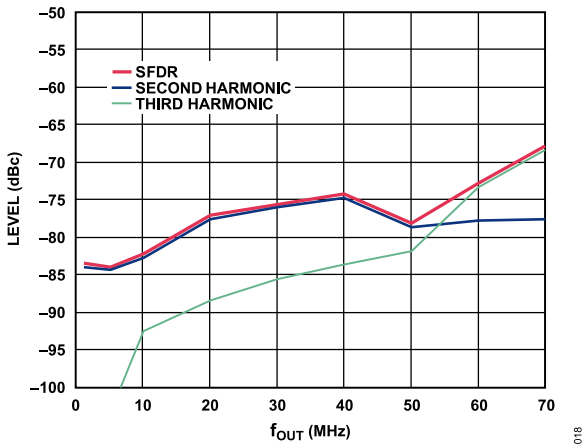

Figure 18. SFDR, 2nd and 3rd Harmonics vs. f_{OUT} at I_{OUTFS} = 2 mA

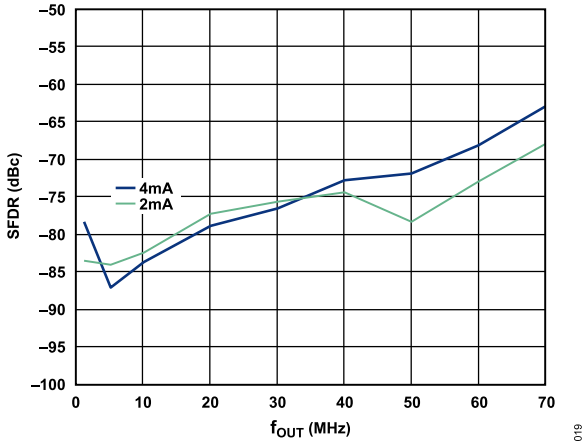

Figure 19. SFDR vs. f_{OUT} at Two I_{OUTFS} Values

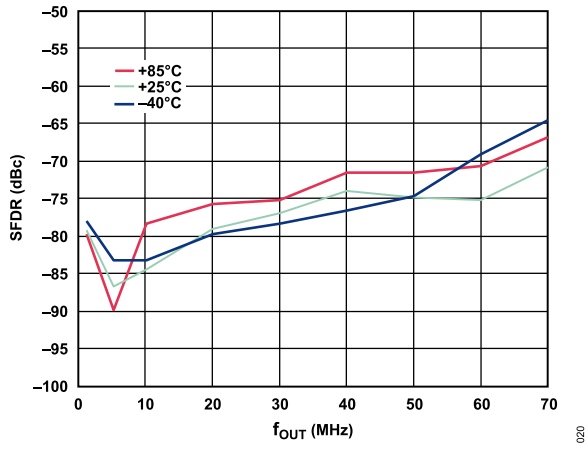

Figure 20. SFDR vs. f_{OUT} at Three Temperatures

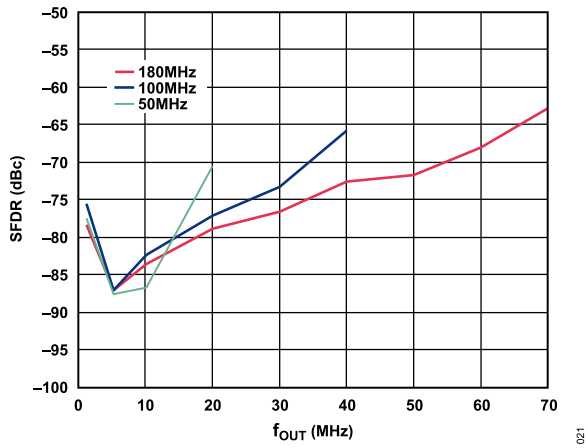

Figure 21. SFDR vs. f_{OUT} at Three f_{DAC} Values

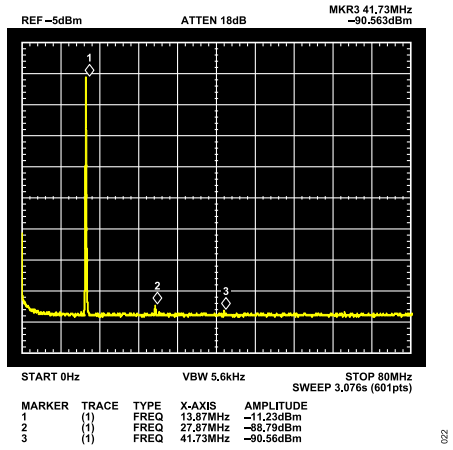

Figure 22. Output Spectrum, f_{OUT} = 13.87 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

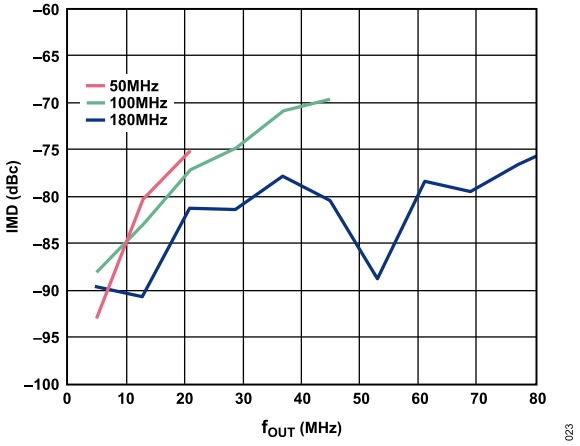

Figure 23. IMD vs. f_{OUT} at Three f_{OUT} Values

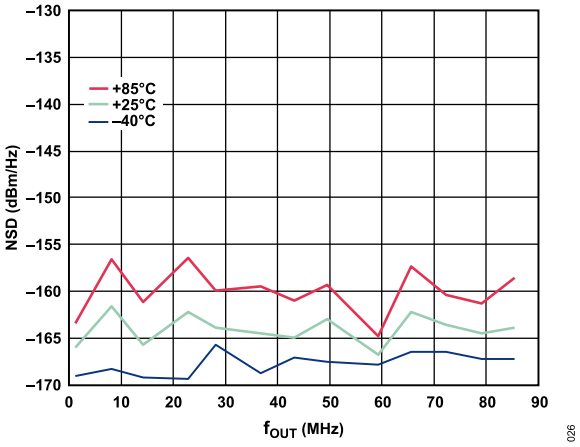

Figure 26. NSD vs. f_{OUT} at Three Temperatures

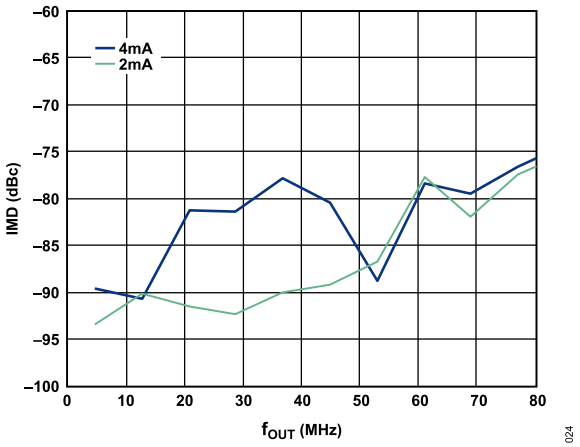

Figure 24. IMD vs. f_{OUT} at Two I_{OUTFS} Values

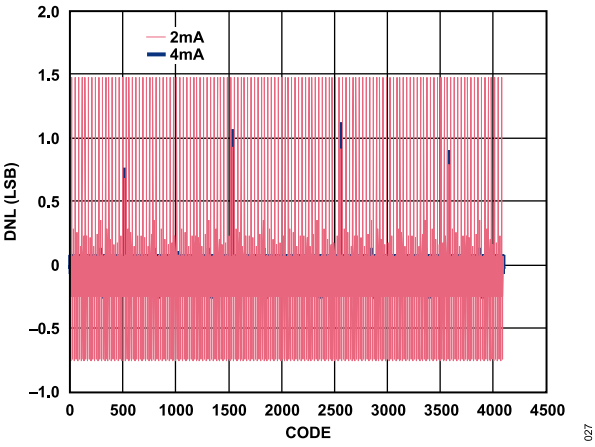

Figure 27. DNL, Two I_{OUTFS} Values

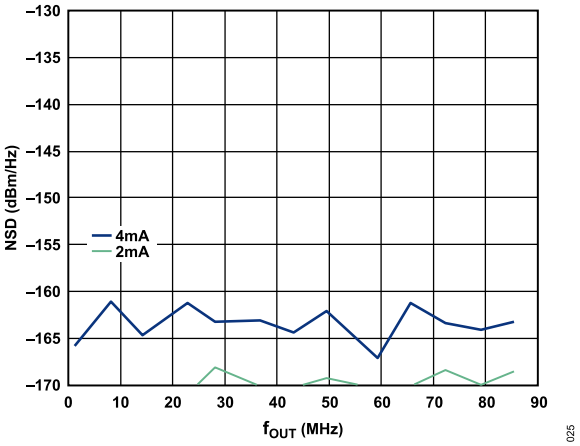

Figure 25. NSD vs. f_{OUT} at Two I_{OUTFS} Values

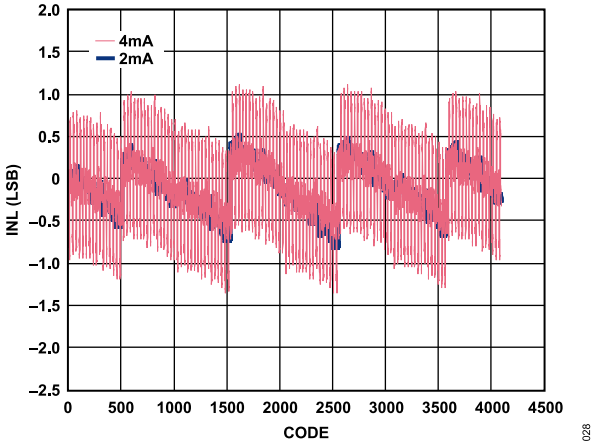

Figure 28. INL, Two I_{OUTFS} Values

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)

INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity DNL

DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity

A digital-to-analog converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error

Offset error is the deviation of the output current from the ideal of zero. For IOUTP, 0 mA output is expected when the inputs are all 0s. For IOUTN, 0 mA output is expected when all inputs are set to 1.

Gain Error

Gain error is the difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1, minus the output when all inputs are set to 0. The ideal gain is calculated using the measured V_{REF}. Therefore, the gain error does not include effects of the reference.

Output Compliance Voltage

Output compliance voltage is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift

Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection

Power supply rejection is the maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time

Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse

Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in picovolt-seconds (pV-s).

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Noise Spectral Density (NSD)

Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone.

THEORY OF OPERATION

Figure 1 is a block diagram of the AD9102. The AD9102 has a single 14-bit current output DAC.

An on-chip band gap reference is provided. Optionally, an off-chip voltage reference may be used. The full-scale DAC output current, also known as gain, is governed by the current, I_{REF}. I_{REF} is the current that flows through the I_{REF} resistor. The I_{REF} set resistor can be on or off chip at the discretion of the user. When the on-chip R_{SET} resistor is in use, DAC gain accuracy can be improved by employing the built in automatic gain calibration capability. Automatic calibration can be used with the on-chip reference or an external REFIO voltage. See the Automatic IOUTFS Calibration section for a procedure for automatic gain calibration.

The power supply rails for the AD9102 are AVDD for analog circuits, CLKVDD/CLDO for the clock input receiver, and DVDD/DLDO1/DLDO2 for the digital I/O and for the on-chip digital datapath. AVDD, DVDD, and CLKVDD can range from 1.8 V to 3.3 V nominal. DLDO1, DLDO2, and CLDO operate at 1.8 V. If DVDD = 1.8 V, DLDO1 and DLDO2 must be connected to DVDD, with the on-chip LDOs disabled. All three supplies are provided externally in this case. Also, if CLKVDD = 1.8 V, CLDO must be connected to CLKVDD, with the on-chip LDO disabled.

Digital signals input to the 14-bit DAC are generated by on-chip digital waveform generation resources. From a digital datapath, 14-bit samples are input to the DAC at the CLKP/CLKN sample rate. The data path includes gain and offset corrections and a digital waveform source selection multiplexer. Waveform sources are SRAM, direct digital synthesizer (DDS), DDS output amplitude modulated by SRAM data, a sawtooth generator, DC constant, and a pseudorandom sequence generator.

The waveforms output by the source selection multiplexer have programmable pattern characteristics. The waveforms can be set up to be continuous pulsed (fixed pattern period and start delay within each pattern period), or finite pulsed (a set number of pattern periods are output, then the pattern stops). Pulsed waveforms (finite or continuous) have a programmed pattern period and start delay. The waveform is present in each pulse period following the programmed pattern period start and the start delay.

A SPI port enables loading of data into SRAM and programming of all the control registers inside the device.

SPI PORT

The AD9102 provides a flexible, synchronous serial communications (SPI) port that allows easy interfacing to application specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and industry-standard microcontrollers. The interface allows read/write access to all registers that configure the AD9102 and to the on-chip SRAM. Its data rate can be up to the SCLK clock speed shown in Table 3 and Table 4.

The SPI interface operates as a standard synchronous serial communication port. Chip Select ($\overline{CS}$) is an active low chip select pin. When $\overline{CS}$ is active low, SPI address and data transfer begins on the SCLK rising edge. The first bit coming on SDIO is a read/write indicator (high for read, low for write). The next 15 bits are the initial register address.

For multiple consecutive register write/read operations in the 0x00 to 0x60 address space, the SPI port automatically decrements the register address if $\overline{CS}$ stays low beyond the first data-word, allowing writes to or reads from a set of contiguous addresses. Note that 0x60 must be used as the starting address for this to work. In this mode, there is no provision to choose the beginning and ending addresses to write. Refer to the SRAM section on how to access the SRAM.

Table 12. Command Word

MSB							LSB
DB15	**DB14**	**DB13**	**DB12**	**...**	**DB2**	**DB1**	**DB0**
R/$\overline{W}$	A14	A13	A12	...	A2	A1	A0

When the first bit of the command byte is a logic low (R/$\overline{W}$ bit = 0), the SPI command is a write operation. In this case, SDIO remains an input (see Figure 29 and Figure 31). When the first bit of the command byte is a logic high (R/$\overline{W}$ bit = 1), the SPI command is a read operation. In this case, data is driven out of the SDIO (see Figure 30).

The SPI interface has a provision for 4-wire (default) or 3-wire interface set in Bit 14 (SPI3WIRE) and Bit 1 (SPI3WIREM) in SPICONFIG (Register 0x00). In 4-wire SPI interface mode (see Figure 31), the AD9102 acts as the responder, whereas the FPGA (such as the SDP-K1) acts as the controller. Data is read from SDO (Pin 7), and the data is written by the controller through SDIO (Pin 2). The SPI communication finishes after the $\overline{CS}$ pin goes high.

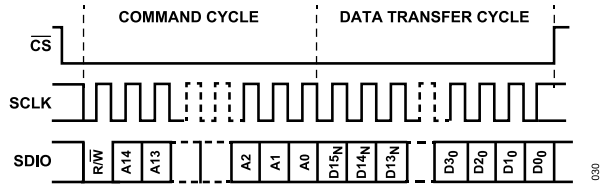

Figure 29. Serial Register Interface Timing, MSB First Write, 3-Wire SPI

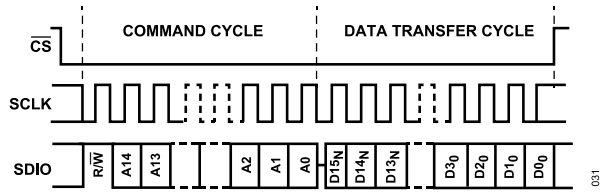

Figure 30. Serial Register Interface Timing, MSB First Read, 3-Wire SPI

THEORY OF OPERATION

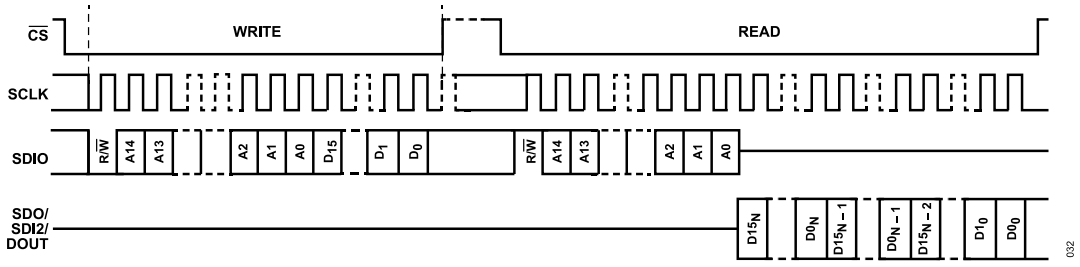

Figure 31. Serial Register Interface Timing, MSB First Write, 4-Wire SPI

Configuration Register Update Procedure

Most SPI accessible registers are double buffered. An active register set controls operation of the AD9102 during pattern generation, while a set of shadow registers stores updated register values. Register configuration updates can be written at any time on the shadow registers. After SPI configuration update is complete, Bit 0 in RAMUPDATE (Register 0x1D) must be set to 1 to arm the register set for transfer from shadow registers to active registers. This is required regardless of the state of the pattern generator in PAT_STATUS (Register 0x1E, Bit 1).

The RAMUPDATE applies to all SPI settings but does not apply to the 4096 × 14-bit SRAM registers. Refer to the SRAM section for the SRAM update procedure. Because of the double buffer configuration, performing an SPI read operation returns the values in the shadow registers, not the active registers.

DAC TRANSFER FUNCTION

The AD9102 DAC provides a differential current output: IOUTP/IOUTN. Digital waveforms, generated on-chip for input to the DAC, use a two's complement number system. The sign bit of each digital waveform word is inverted immediately prior to input to each DAC core. The DAC input code variable in Equation 1 and Equation 2 uses an offset binary number system (two's complement with the sign bit inverted).

The DAC output current equations are as follows:

$$IOUTP = I_{OUTFS} \times DAC\ INPUT\ CODE/2^{14} \quad (1)$$

$$IOUTN = I_{OUTFS} \times ((2^{14} - 1) - DAC\ INPUT\ CODE)/2^{14} \quad (2)$$

where:
DAC INPUT CODE = 0 to $2^{14} - 1$.

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

When using on-chip R_{SET} resistors, DAC gain accuracy can be improved by employing the built-in automatic gain calibration feature of the device (see the Automatic IOUTFS Calibration section).

Analog Current Outputs

Optimum linearity and noise performance of DAC outputs can be achieved when they are connected differentially to an amplifier or a transformer. In these configurations, common-mode signals at the DAC outputs are rejected.

The output compliance voltage specifications listed in Table 1 and Table 2 must be adhered to for the performance specifications in those tables to be met.

SETTING I_{OUTFS}, DAC GAIN

I_{OUTFS} is the full-scale current or DAC gain. I_{REF} is the current that flows through the I_{REF} resistor. The I_{REF} resistor can be on or off chip at the discretion of the user.

As expressed in Equation 3 and Equation 4, I_{OUTFS} is a function of the reference voltage at the REFIO terminal and R_{SET}.

Voltage Reference

The AD9102 contains an internal 1.0 V nominal band gap reference, V_{BG}. By default, the on-chip reference is powered up and ready to be used. When using the on-chip reference, the REFIO terminal needs to be decoupled to AGND using a 0.1 µF capacitor as shown in Figure 32.

Alternatively, on-chip reference can be replaced by a more accurate off-chip reference. To apply external reference, set REF_EXT in POWERCONFIG (Register 0x01, Bit 4) to 1 then apply the external reference to the REFIO pin. In this case, the 0.1 µF capacitor is not required. The internal reference can be directly overridden by the external reference.

When using an external reference, it is recommended to power down the internal reference to lessen power consumption. To do so, set REF_PDN field in POWERCONFIG (Register 0x01, Bit 5) to 1. An external reference can provide tighter reference voltage tolerances and/or lower temperature drift than the on-chip band gap. Table 13 summarizes reference connections and programming.

THEORY OF OPERATION

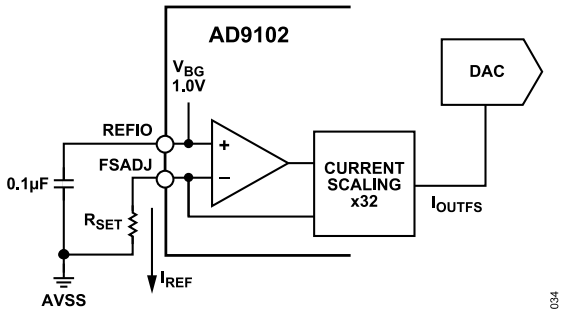

Figure 32. On-Chip Reference with External R_{SET} Resistor

Table 13. Reference Operation

Reference Mode	REFIO Pin	Register Setting
Internal	Connect 0.1 µF capacitor	Register 0x01, Bit 4 = 0 (default)
External	Connect off-chip reference	Register 0x01, Bit 4 = 1

Programming Internal V_{REFIO}

When the internal voltage reference is in use, the BGDR field in REFADJ (Register 0x03, Bits[5:0]) adjusts the V_{REFIO} level. This adjustment adds or subtracts up to 20% from the nominal band gap voltage on REFIO. The voltage across the FSADJ resistor tracks this change. As a result, I_{REF} varies by the same amount.

Figure 33 shows V_{REFIO} vs. BGDR code for an on-chip reference with a voltage (BGDR = 0x00) of 1.04 V. The V_{REFIO} voltage at BGDR = 0x00 can vary over the internal voltage range shown in Table 1 and Table 2 from chip to chip. The BGDR scaling is 6.25 mV per LSB, and the BGDR code is in two's complement format.

R_{SET} Resistors

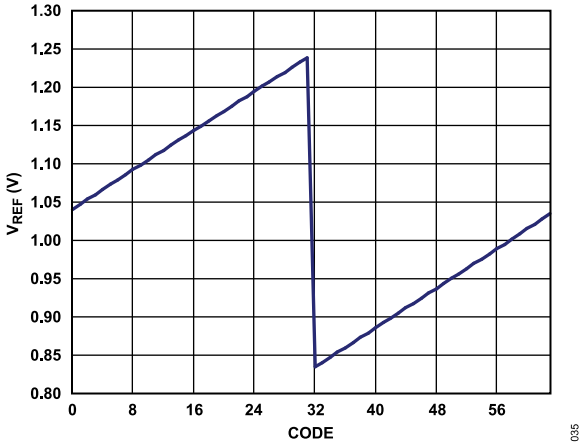

Figure 33. Typical V_{REFIO} Voltage vs. BGDR

R_{SET} in Equation 4 can be an internal resistor or a board level resistor of the user choosing connected to the FSADJ terminal.

To make use of the on-chip R_{SET} resistor, set DAC_RSET_EN (Register 0x0C, Bit 15) to 1. Set DAC_RSET (Register 0x0C, Bits[4:0]) to manually program values for the on-chip R_{SET}. Bitfield [4:0] is set to 0x0A by default which programs R_{SET} value to 8 kΩ. It can be adjusted from 4 kΩ to 16 kΩ with a resolution of 800 Ω.

Automatic I_{OUTFS} Calibration

Many applications require tight DAC gain control. The AD9102 provides an automatic I_{OUTFS} calibration procedure used with on-chip R_{SET} resistors only. The voltage reference, V_{REFIO}, can be an on-chip reference or an off-chip reference. The automatic calibration procedure performs a fine adjustment of the internal R_{SET} value and the current, I_{REF}.

When using automatic calibration, the following board level connections are required:

1. Connect FSADJ (Pin 25) and CAL_SENSE (Pin 24) together.
2. Install a resistor between CAL_SENSE (Pin 24) and AGND. The value of this resistor must be R_{CAL_SENSE} = 32 × V_{REFIO}/I_{OUTFS}, where I_{OUTFS} is the target full-scale current for the DAC.

Automatic calibration uses an internal clock. This calibration clock, described in Equation 5, is equal to the DAC clock divided by the division factor chosen in CAL_CLK_DIV (Register 0x0D, Bits[2:0]). Each calibration cycle is between 4 and 512 DAC clock cycles, depending on the value of CAL_CLK_DIV. The frequency of the calibration clock should be less than 500 kHz.

$$Calibration\ Clock = f_{CLKP/CLKN}/2^{(2\ +\ CAL\_CLK\_DIV)} \quad (5)$$

To perform an automatic calibration, follow these steps:

1. Set the calibration ranges in DACRANGE (Register 0x08, Bits[7:0]) and COMP_CAL_RNG (Register 0x0D, Bits[5:4]) to their minimum values to allow best calibration.
2. Enable the calibration clock bit, CAL_CLK_EN, (Register 0x0D, Bit 3).
3. Set the divider ratio for the calibration clock by setting CAL_CLK_DIV (Register 0x0D, Bits[2:0]). See Table 23 for the clock divider values. The default is 512.
4. Set CAL_MODE_EN (Register 0x0D, Bit 6) to Logic 1.
5. Set START_CAL (Register 0x0E, Bit 0) to Logic 1 to begin the calibration of the comparator, R_{SET}, and gain.
6. The CAL_MODE flag (Register 0x0D, Bit 7) goes to Logic 1 while the device is calibrating. The CAL_FIN flag (Register 0x0E, Bit 1) goes to Logic 1 when the calibration is complete.
7. Set START_CAL (Register 0x0E, Bit 0) to Logic 0.
8. After calibration, verify that the overflow and underflow flags (Register 0x0D, Bits[14:9]) are not set. If they are set, change the corresponding calibration range to the next larger range and begin again at Step 5.
9. If no flag is set, read the values of DAC_RSET_CAL (Register 0x0C, Bits[12:8]) and DAC_GAIN_CAL (Register 0x07, Bits[14:8]), then write them into the corresponding DAC_RSET (Register 0x0C, Bits[4:0]) and DAC_GAIN (Register 0x07, Bits[6:0]) register fields, respectively.

THEORY OF OPERATION

10. Reset CAL_MODE_EN (Register 0x0D, Bit 6) and the calibration clock bit, CAL_CLK_EN (Register 0x0D, Bit 3) to Logic 0 to disable the calibration clock.
11. Set CAL_MODE_EN (Register 0x0D, Bit 6) to Logic 0 to set the R_{SET} and gain control muxes to normal mode operation.
12. Disable the calibration clock bit, CAL_CLK_EN.

To reset the calibration, either pulse CAL_RESET (Register 0x0D, Bit 8) to Logic 1 then Logic 0, pulse $\overline{\text{RESET}}$ (Pin 9), or pulse the RESET bits in SPICONFIG (Register 0x00, Bit 13 and Bit 2).

CLOCK INPUT

For optimum DAC performance, the AD9102 clock input signal pair (CLKP/CLKN) must be a very low jitter, fast rise time differential signal. The clock receiver generates its own common-mode voltage, requiring these two inputs to be ac-coupled.

Figure 34 to Figure 37 are the preferred methods for clocking the AD9102. Figure 34 shows the recommended interface to a number of Analog Devices, Inc., low voltage differential signaling (LVDS) clock drivers that work well with the AD9102, where a 100 Ω termination resistor and two 0.1 µF coupling capacitors are used. Figure 35 shows an interface to an Analog Devices differential positive emitter coupled logic (PECL) driver, while Figure 36 shows a single-ended-to-differential converter using a balun driving CLKP/CLKN.

In applications where the analog output signals are at low frequencies, the AD9102 clock input can be driven with a single-ended complementary metal oxide semiconductor (CMOS) signal. Figure 37 shows such an interface. CLKP is driven directly from a CMOS gate, and CLKN is bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor. The optional resistor is a series termination.

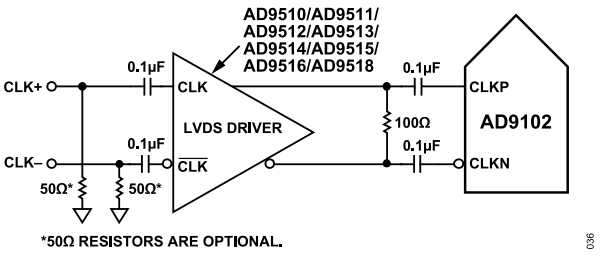

Figure 34. Differential LVDS Clock Input

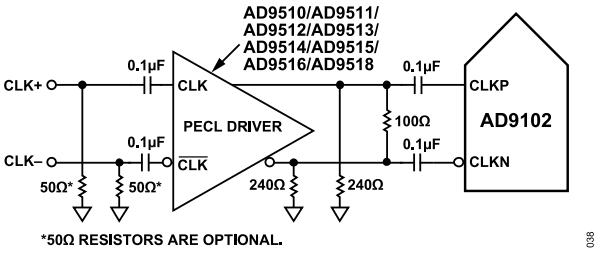

Figure 35. Differential PECL Sample Clock

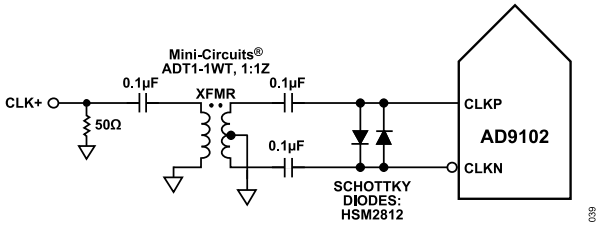

Figure 36. Transformer Coupled Clock

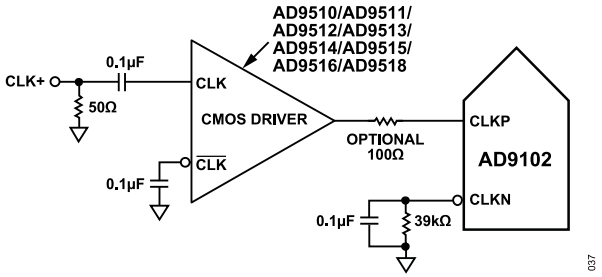

Figure 37. Single-Ended 1.8 V CMOS Sample Clock

DAC Output Clock Edge

The DAC can be configured to output samples on the rising or falling edge of the CLKP/CLKN clock input by configuring DAC_INV_CLK in CLOCKCONFIG (Register 0x02, Bit 3). This functionality sets the DAC output timing resolution at $1/(2 \times f_{CLKP/CLKN})$.

GENERATING SIGNAL PATTERNS

The AD9102 can generate two types of signal patterns under control of its programmable pattern generator.

- Periodic pulse train waveforms that repeat indefinitely, which are waveforms that are output once during each pattern period. Pattern periods occur one after the other so long as the pattern generator is in the pattern ON state.
- Periodic pulse train waveforms that repeat a finite number of times, which are similar to those that repeat indefinitely except that the waveforms are output during a finite number of consecutive pattern periods.

Pattern Generator Programming

Figure 38 shows periodic pulse train waveforms as seen at the output to the DAC. The DAC generates a digital signal stored in SRAM multiplied by the DAC digital gain factor (see the DAC Digital Gain Multiplier section). The SRAM data is read using the DAC address counter (see the SRAM section). The waveform is generated at every pattern period. See the Setting Pattern Period section on how to set the pattern period.

THEORY OF OPERATION

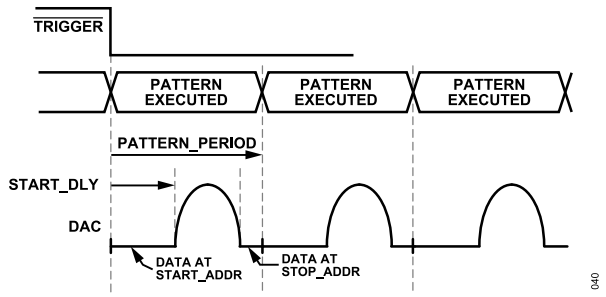

Figure 38. Periodic Pulse Trains Output on DAC

Setting Waveform Start Delay

The DAC has a start delay which is the delay between the start of the pattern period and the start of the waveform. This delay is set in START_DLY (Register 0x5C). To define the START_DLY register as a repetitive delay for each pattern, PATTERN_RPT (Register 0x1F, Bit 0) and TRIG_DELAY_EN (Register 0x44, Bit 1) must be set to 0.

The waveform start delay base is programmed in the START_DELAY_BASE field in PAT_TIMEBASE (Register 0x28, Bits[3:0]). START_DELAY_BASE determines how many CLKP/CLKN clock cycles there are per START_DELAY LSB.

Setting Pattern Period

Two register bit fields set the length of the pattern period. First is PAT_PERIOD (Register 0x29). The second is the PAT_PERIOD_BASE field in PAT_TIMEBASE (Register 0x28, Bits[7:4]) which sets the number of CLKP/CLKN clocks per PATTERN_PERIOD LSB. The longest pattern period available is 65,535 × 16/$f_{CLKP/CLKN}$. The pattern period length can be determined through Equation 6 and Equation 7.

$$Pattern\ period = PAT\_PERIOD \times PATTERN\_PERIOD\ LSB \quad (6)$$

where

$$PATTERN\_PERIOD\ LSB = PAT\_PERIOD\_BASE/f_{CLKP/CLKN} \quad (7)$$

Note that the pattern period must be at least equal to the sum of START_DELAY and the waveform length to generate the complete waveform. If the pattern period set is less than this, the generated waveform appears trimmed and the error flag PERIOD_SHORT_ERR (Register 0x60, Bit 2) toggles high.

RUN Bit, Trigger Terminal, and Pattern Bit (Read Only)

Both the RUN bit in PAT_STATUS (Register 0x1E, Bit 0) and the Trigger terminal (Pin 32) are required to generate a pattern out of the AD9102. The Run bit activates the pattern generator, whereas the falling edge on the Trigger terminal starts the generation of a pattern.

Setting the RUN bit activates the AD9102 for pattern generation, whereas clearing it shuts down the pattern generator (see Figure 41). If the RUN bit is set, the falling edge on the Trigger terminal starts pattern generation after a short delay. As shown in Figure 39, the pattern generator state turns ON after a number of CLKP/CLKN clock cycles following the falling edge of Trigger. This delay is programmed in PATTERN_DLY (Register 0x20). Consequently, a rising edge on the Trigger terminal terminates pattern generation after a short delay (see Figure 40).

So long as the RUN bit is enabled last after writing to all other SPI registers, then pattern generation is successful when a falling edge is provided to the Trigger terminal.

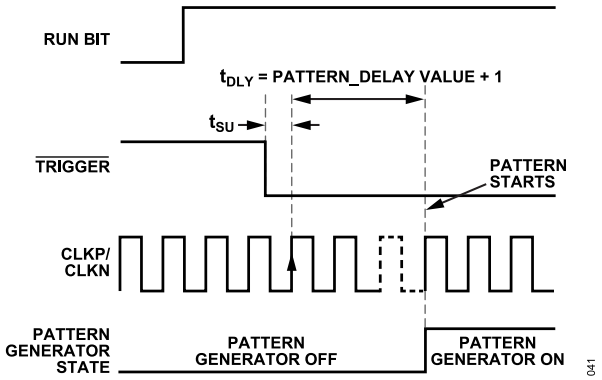

Figure 39. Trigger Initiated Pattern Start with Pattern Delay

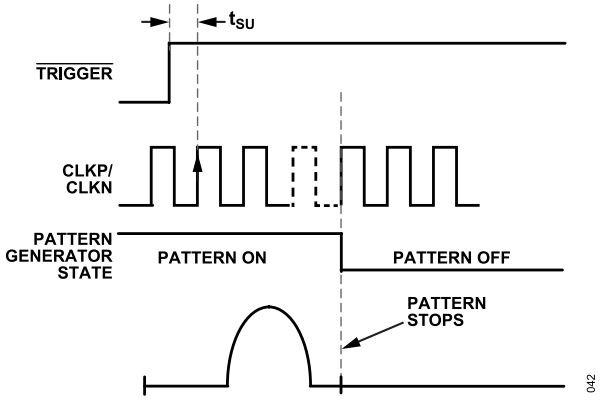

Figure 40. Trigger Rising Edge Initiated Pattern Stop

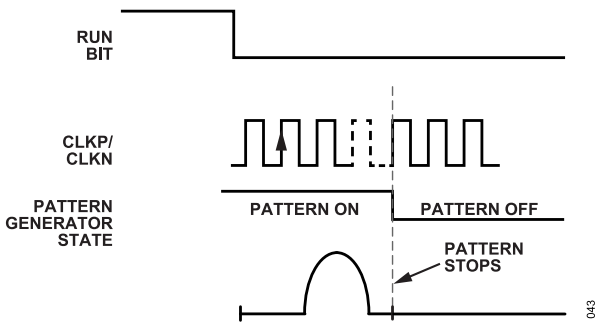

Figure 41. RUN Bit Driven Pattern Stop

The read-only Pattern bit (Register 0x1E, Bit 1) indicates whether the pattern generator is ON or OFF. A reading of 1 indicates that

THEORY OF OPERATION

the pattern generator is ON, whereas a reading of 0 indicates the pattern generator is OFF.

DAC INPUT DATAPATHS

Timing in the DAC datapath is governed by the pattern generator. The DAC datapath includes a waveform selector, a waveform repeat controller, RAM output and DDS output multiplier (RAM output can amplitude modulate DDS output), DDS cycle counter, DAC digital gain multiplier, and a DAC digital offset summer. DAC input datapath use a two's complement number system.

DAC Digital Gain Multiplier

On its way into the DAC, the digital waveform samples are multiplied by a 12-bit gain factor programmed in DAC_DGAIN (Register 0x35). The format of the register is in two's complement with a range of ±2.0 (unitless). The scaling of digital gain is $4/2^{12}$.

Although the digital data can be multiplied to a magnitude of 2, the DAC output current is limited to the range 0 to I_{OUTFS}. If the resulting DAC input code (DAC digital data times digital gain plus DAC offset) exceeds full-scale, the output is clipped at I_{OUTFS}. If the resulting DAC input code is lower than negative full-scale, the output is clipped at 0 A.

DAC Digital Offset Summer

DAC input samples are summed with a 12-bit DC offset value programmed in DACDOF (Register 0x25). The format of the register is in two's complement with a range of ±50% of the DAC output current. The scaling of digital offset is $1/2^{12}$.

Like in DAC digital gain, if the resulting DAC input code with the digital offset exceeds full-scale, the output is clipped at I_{OUTFS}. If the resulting DAC input code is lower than negative full-scale, the output is clipped at 0 A.

Pattern Period Repeat Controller

The PATTERN_RPT bit in PAT_TYPE (Register 0x1F, Bit 0) controls whether the pattern output repeats for infinite number of times (periodic pulse train repeats indefinitely) or repeats a number of consecutive times defined by DAC_REPEAT_CYCLE (Register 0x2B, Bits[7:0]). The latter are periodic pulse trains that repeat a finite number of times.

DAC Waveform Selectors

Waveform selector inputs are:

- Prestored waveform
  - Pulsed, phase shifted DDS sine wave output
  - Sawtooth generator output
  - Pseudorandom sequence generator output
  - DC constant generator output
- RAM loaded vectors (SRAM)
- Prestored waveform amplitude modulated by RAM output

Waveform selection for the DAC is made by programming WAV_CONFIG (Register 0x27).

DOUT FUNCTION

In applications where the AD9102 DAC drives a high voltage amplifier, such as in ultrasound transducer array element driver signal chains, it can be useful to turn on and off the amplifier at precise times relative to the waveform generated by the AD9102 DAC. The SDO/SDI2/DOUT terminal can be configured to provide this function.

The SPI interface needs to be configured in 3-wire mode (Figure 29 and Figure 30) by setting Bit 14 (SPI3WIRE) and Bit 3 (SPI3WIREM) in SPICONFIG (Register 0x00). When Bit 11 (SPI_DRV) and Bit 4 (SPI_DRVM) in SPICONFIG are set to Logic 1, the SDO/SDI2/DOUT terminal provides the DOUT function.

Manually Controlled DOUT

If the DOUT_MODE in DOUT_CONFIG (Register 0x2D, Bit 4) is set to Logic 0, DOUT can be turned on or off using DOUT_VAL (Register 0x2D, Bit 5).

Pattern Generator Controlled DOUT

Figure 42 depicts the rising edge of a pattern generator controlled DOUT pulse, whereas Figure 43 shows the falling edge. The pattern generator controlled DOUT is set up by setting DOUT_MODE bit in DOUT_CONFIG (Register 0x2D, Bit 4) to Logic 1. Then, the start delay is programmed in DOUT_START (Register 0x2C), and the stop delay is programmed in DOUT_STOP in DOUT_CONFIG (Register 0x2D, Bits[3:0]).

DOUT goes high after CLKP/CLKN cycles stated in DOUT_START after the falling edge of the signal input to the Trigger terminal (Pin 32). DOUT stays high as long as a pattern is being generated. DOUT goes low after CLKP/CLKN cycles stated in DOUT_STOP after the clock edge that causes pattern generation to stop.

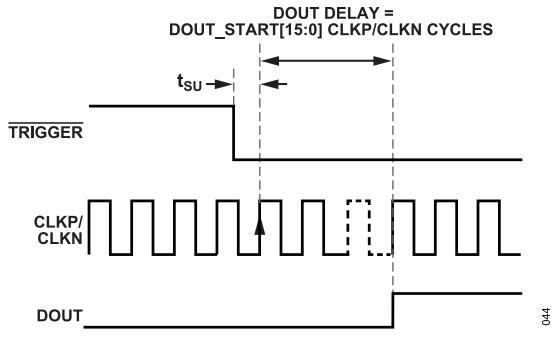

Figure 42. DOUT Start Sequence

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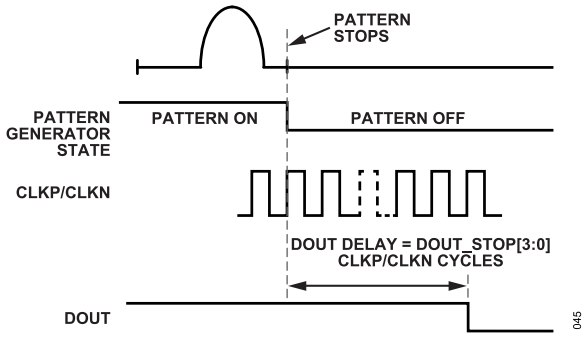

Figure 43. DOUT Stop Sequence

DIRECT DIGITAL SYNTHESIZER (DDS)

The DDS generates a sinusoid at a frequency determined by its tuning word input. The tuning word is 24 bits wide. The resolution of DDS tuning is $f_{CLKP/CLKN}/2^{24}$. Equation 8 describes the DDS output frequency as follows:

$$f_{OUT,DDS} = DDS\_TW \times f_{CLKP/CLKN}/2^{24} \quad (8)$$

The DDS tuning word can be programmed in one of two ways. First, for a fixed frequency, DDSTW_MSB (Register 0x3E, Bits[15:0]) and DDSTW_LSB (Register 0x3F, Bits[15:8]) are programmed with a constant and the output follows Equation 8.

Second, when the frequency of the DDS needs to change within each pattern period, a sequence of values stored in SRAM is combined with a selection of DDSTW_MSB bits to form the tuning word (see the Clock Selection for Incrementing Pattern Generation Mode—SRAM Address Counters section).

Number of DDS Cycles

The DAC input data path establishes the pulse width of the sine wave output from the DDS in a finite number of sine wave cycles. The cycle counts are programmed in DDS_CYC (Register 0x5F).

For the values in those registers to take effect, the programmable pattern generator must generate waveforms that repeat a finite number of times. This is done by setting the WAVE_SEL field in WAV_CONFIG (Register 0x27, Bits[1:0]) to 0x2.

DDS Phase Offset

The DDS includes a programmable phase shifter. The format of the register for the DDS phase offset is in two's complement with a range of 360°.

The phase shift is programmed in one of two ways. First is using DDS_PW (Register 0x43). The DDS_PW register can be used to adjust the phase offset of a DDS-generated waveform only. It does not affect other prestored waveforms and SRAM-generated waveforms. The scaling or resolution of DDS_PW is $360°/(2^{16} - 1)$. Equation 9 describes the phase offset from DDS_PW.

$$DDS_{Phase\ offset} = DDS\_PW \times 360°/(2^{16} - 1) \quad (9)$$

The second way to program the DDS phase offset is by using PHASE_MEM_EN (Register 0x45, Bit 1) which modifies the DDS phase offset based on the value stored in SRAM.

SRAM

The AD9102 contains an internal memory for storing data vectors which can be used for arbitrary waveform generation. The 4096 × 14-bit SRAM (SPI port address space located in 0x6000 to 0x6FFF) can contain any signal samples, such as amplitude modulation patterns, lists of DDS tuning words, or lists of DDS output phase offset words. The SRAM data follows a two's complement format, and SRAM data word is left justified. To output from SRAM, set the WAVE_SEL field in WAV_CONFIG (Register 0x27) to 0.

SRAM can be accessed using any of the SPI operating modes shown in Figure 29 through Figure 31. Using the SPI modes of operation in Figure 29 and Figure 30, the entire SRAM can be written in $(2 + 2 \times 4096) \times 8/f_{SLCK}$ seconds.

The DAC datapath has an SRAM address counter going from start address (START_ADDR, Register 0x5D) to stop address (STOP_ADDR, Register 0x5E). The SRAM start and stop addresses can be anywhere from 0x000 to 0xFFF. During each pattern period, data is read from SRAM after the START_DELAY period and while the address counter is incrementing. Refer to the Waveform Generation Setups and Sample Sequence section for sample register configurations of generating output from SRAM.

The SRAM length being written must be an even number if TRIG_DELAY_EN (Register 0x44, Bit 1) = 1. This requirement implies that the START_ADDR and STOP_ADDR cannot both be even or both be odd. Only one of the addresses can be even, while the other address must be odd.

Reading and Writing to On-Chip SRAM

Reading and writing is done directly in SRAM as opposed to SPI registers which implement a double buffer configuration (see the Configuration Register Update Procedure section). Data is written to and read from the memory via the SPI port as long as the SRAM is not actively engaged in pattern generation (the RUN bit in Register 0x1E = 0). Set up PAT_STATUS (Register 0x1E) to read and write from SRAM.

To write to any SRAM address, set PAT_STATUS to 0x04 as follows:

- BUF_READ (Bit 3) = 0
- MEM_ACCESS (Bit 2) = 1
- RUN (Bit 0) = 0

To read data from any SRAM address, set PAT_STATUS to 0x0C as follows:

- BUF_READ (Bit 3) = 1
- MEM_ACCESS (Bit 2) = 1
- RUN (Bit 0) = 0

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For multiple consecutive write operations in the SRAM address space, the SPI port automatically decrements the register address (0x6FFF down to 0x6000) if $\overline{CS}$ stays low beyond the first data word. The autodecrement feature does not apply to consecutive read operations from the SRAM.

Clock Selection for Incrementing Pattern Generation Mode—SRAM Address Counters

The SRAM address counter can be programmed to be incremented by either CLKP/CLKN (default) or by the rising edge of the DDS output MSB. The DDS_MSB_EN bit in DDS_CONFIG (Register 0x45, Bit 2) makes this selection.

For example, when generating SRAM waveform samples or DDS amplitude modulation samples, the SRAM address counter must be incremented by CLKP/CLKN (default). On the other hand, when generating a list of DDS tuning words (such as a chirp waveform), the SRAM address counters can be incremented by either CLKP/CLKN (default) or by the rising edge of the DDS output MSB. In this case, each frequency setting dwells for one DDS output sine wave cycle.

SAWTOOTH GENERATOR

When sawtooth is selected in the PRESTORE_SEL field in WAV_CONFIG (Register 0x27), the sawtooth generator is connected to the DAC digital datapath.

Sawtooth types, shown in Figure 44, are selected using the SAW_TYPE field in SAW_CONFIG (Register 0x37, Bits[1:0]). A positive sawtooth waveform ramps up from negative full-scale to positive full-scale in 1 LSB steps, while a negative sawtooth ramps down in the same manner.

The number of samples per sawtooth waveform step is programmed in the SAW_STEP field in SAW_CONFIG (Register 0x37, Bits[7:2]). Each sawtooth waveform step can have up to 63 samples, and the total of steps of the sawtooth waveform for the AD9102 is 2^{14} or 16384. For a triangular waveform, the total number of steps is twice as many.

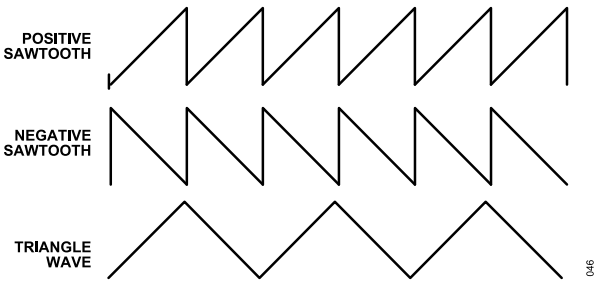

Figure 44. Sawtooth Patterns

The sawtooth frequency is determined based on two parameters: the DAC clock input ($f_{CLKP/CLKN}$) and the SAW_STEP field in SAW_CONFIG. Equation 10 to Equation 13 describe the sawtooth frequency equation.

$$Sawtooth\ frequency = 1/Sawtooth\ ramp\ time \quad (10)$$

$$Sawtooth\ ramp\ time = N \times 2^{14} \times Step\ time \quad (11)$$

where:
N = 1 for positive/negative sawtooth.
N = 2 for triangular sawtooth.

$$Step\ time = DAC\ clock\ period \times SAW\_STEP \quad (12)$$

$$DAC\ clock\ period = 1/f_{CLKP/CLKN} \quad (13)$$

Note that the sawtooth pattern period is not the same as the sawtooth ramp time. The sawtooth pattern period is calculated based on the sawtooth ramp time and the PAT_PERIOD_BASE field in PAT_TIMEBASE (Register 0x28, Bits[7:4]). Refer to the Setting Pattern Period section for the pattern period. Equation 14 describes the sawtooth pattern period.

$$Sawtooth\ \ Pattern\ \ Period\ \ = \frac{Sawtooth\ \ ramp\ \ time}{PAT\_PERIOD\_BASE} \quad (14)$$

Alternatively, sawtooth waveforms can be generated from SRAM. See the Reading and Writing to On-Chip SRAM section on how to access the SRAM. Table 14 provides sample sawtooth configurations for a DAC clock input of 180 MHz (DAC clock period = 5.56 ns), and the sawtooth waveforms are illustrated in Figure 45. The sawtooth frequency is calculated based on Equation 10 to Equation 13.

Table 14. Sample Sawtooth Waveforms Configurations

SAW_TYPE	PAT_PERIOD_BASE	SAW_STEP	Sawtooth Frequency
Ramp-Up	1	1	10.986 kHz
Triangular	2	2	2.746 kHz
Ramp-Down	2	3	3.662 kHz

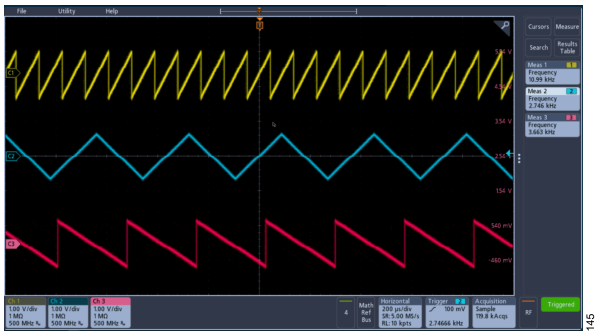

Figure 45. Sample Sawtooth Waveforms

PSEUDORANDOM SIGNAL GENERATOR

The pseudorandom noise generator generates a noise signal on the DAC output if pseudorandom sequence is selected in the PRESTORE_SEL field in WAV_CONFIG (Register 0x27). The pseudorandom noise signals are generated as continuous waveforms only.

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DC CONSTANT

A programmable DC current between 0.0 and I_{OUTFS} can be generated on the DAC if constant value is selected in the PRESTORE_SEL field in WAV_CONFIG (Register 0x27). DC constant current is generated as a continuous waveform only. The DC current level is programmed by writing to the 12-bit DAC_CONST field in DAC_CST (Register 0x31).

POWER SUPPLY NOTES

The AD9102 supply rails (AVDD1, AVDD2, DVDD, and CLKVDD) are specified in Table 9. The AD9102 includes three on-chip linear regulators (CLDO, DLDO1, and DLDO2). The supply rails driven by these regulators operate at 1.8 V. There are two usage rules for these regulators as follows:

- When CLKVDD ≥ 2.5 V, the 1.8 V on-chip CLDO regulator can be used. If CLKVDD = 1.8 V, CLDO must be disabled by setting PDN_LDO_CLK in POWERCONFIG (Register 0x01, Bit 8). CLKVDD and CLDO must be strapped together.
- When DVDD ≥ 2.5 V, the 1.8 V on-chip DLDO1 and DLDO2 regulators can be used. If DVDD = 1.8 V, DLDO1 and DLDO2 must be disabled by setting the PDN_LDO_DIG1 (Register 0x01, Bit 7) and PDN_LDO_DIG2 (Register 0x01, Bit 6) bits in the POWERCONFIG register. DVDD, DLDO1, and DLDO2 must be strapped together.

Power-Down Capabilities

By default, the DAC outputs (IOUTP and IOUTN) are at midrange or $I_{OUTFS}/2$ during power-up. This is also the case when the DAC is idle—before and after pattern generation. POWERCONFIG (Register 0x01) allows the user to place the AD9102 in a reduced power dissipation configuration while the CLKP/CLKN input is running and the power supplies are on. To save power, the DAC can be put to sleep by setting DAC_SLEEP in POWERCONFIG (Register 0x01, Bit 3).

Clocking of the waveform generator and the DAC can be turned on or off by setting CLK_PDN in CLOCKCONFIG (Register 0x02, Bit 5). Taking these actions places the AD9102 in the power-down mode, specified in Table 8.

APPLICATIONS INFORMATION

SIGNAL GENERATION EXAMPLES

Figure 46 shows a waveform stored in the 4096 × 14-bit SRAM in an address segment defined by the START_ADDR and STOP_ADDR being output by the DAC. The waveform is repeated once during each pattern period. In each pattern period, a start delay is executed, then the pattern is read from SRAM.

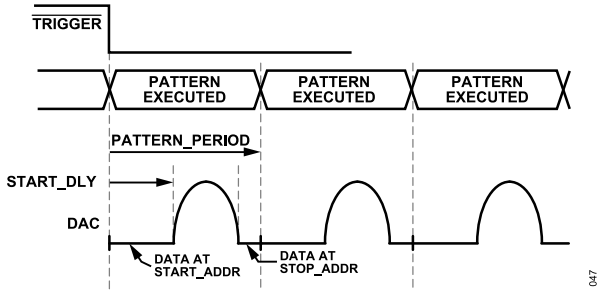

Figure 46. Pattern in SRAM

Figure 47 shows a pulsed sine wave generated by the DAC. The DDS generates a sine wave at a programmed frequency based on Equation 8. The DAC input datapath is programmed with a start delay and a number of sine wave cycles to output. Figure 48 shows a sawtooth wave shape generated by the DAC in successive pattern periods with a start delay.

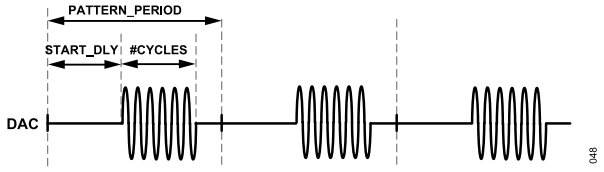

Figure 47. Pulsed Sine Wave in Pattern Periods

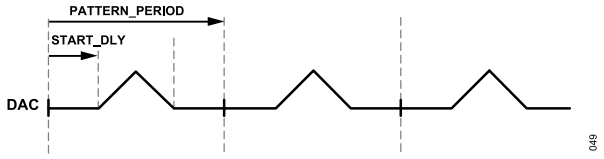

Figure 48. Pulsed Sawtooth Waveform in Pattern Periods

Figure 49 shows the DAC outputting a sine wave modulated by an amplitude envelope. The sine wave is generated by the DDS, and the amplitude envelope is stored in SRAM. A start delay and a digital gain factor are applied in the DAC input data path. Figure 50 and Figure 51 show the DAC generating continuous waveforms—one with start delays, one without. Figure 52 shows an FSK modulated signal generated using a list of DDS tuning word bit fields stored in SRAM. The SRAM address counter is incremented by the rising edge of the DDS output MSB.

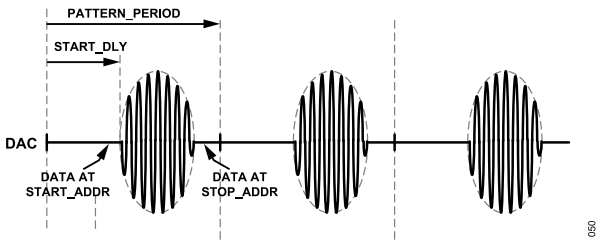

Figure 49. DDS Output Amplitude Modulated by SRAM Envelope

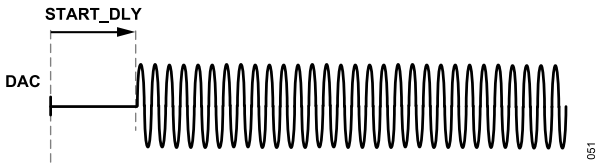

Figure 50. Waveform with Start Delays

Figure 51. Waveform Without Start Delays

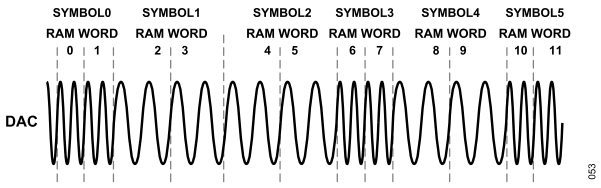

Figure 52. FSK Modulated Signal

APPLICATIONS INFORMATION

WAVEFORM GENERATION SETUPS AND SAMPLE SEQUENCE

A sample sequence for generating DDS waveforms is as follows:

1. Set initial values of I/O pins ($\overline{\text{RESET}}$, $\overline{\text{TRIGGER}}$, and $\overline{\text{CS}}$) to Logic 1 (high).
2. Set SPI frequency and mode as preferred.
3. Assert $\overline{\text{RESET}}$ (Pin 9) by pulsing from Logic 0 (low) then Logic 1 (high) to reset register values. Deassert $\overline{\text{RESET}}$ afterward.
4. Proceed with register read and write for DDS as follows:
   a. Set DDS output frequency in DDSTW_MSB (Register 0x3E, Bits[15:0]) and DDSTW_LSB (Register 0x3F, Bits[15:8]).
   b. (Optional) Set number of DDS cycles in DDS_CYC. For this, WAVE_SEL in WAV_CONFIG must be set to 0x2.
   c. (Optional) Set phase offset for DDS output in DDS_PW (Register 0x43).
5. Write to or read from SPI registers. Update the RUN bit and the RAMUPDATE bit and the end of the write sequence as follows:
   a. Set waveform select to DDS in WAV_CONFIG (Register 0x27).
   b. Set DAC digital gain in DAC_DGAIN (Register 0x35).
   c. (Optional) Set DAC digital offset in DACDOF (Register 0x25).
   d. Update the RUN bit (Register 0x1E).
   e. Update the RAMUPDATE bit (Register 0x1D).
6. Set Trigger terminal (Pin 32) to Logic 0 (low) to start pattern generation.

A sample sequence for generating SRAM waveforms is as follows:

1. Set initial values of I/O pins ($\overline{\text{RESET}}$, $\overline{\text{TRIGGER}}$, and $\overline{\text{CS}}$) to Logic 1 (high).
2. Set SPI frequency and mode as preferred.
3. Assert $\overline{\text{RESET}}$ (Pin 9) by pulsing from Logic 0 (low) then Logic 1 (high) to reset register values. Deassert $\overline{\text{RESET}}$ afterward.
4. Write data to SRAM. Set PAT_STATUS (Register 0x1E) = 0x04 as follows:
   a. BUF_READ (Bit 3) = 0
   b. MEM_ACCESS (Bit 2) = 1
   c. RUN (Bit 0) = 0
   d. Write left-justified data to SRAM registers (0x6000 to 0x6FFF address space). After writing, disable the MEM_ACCESS bit.
5. Read data from SRAM. Set PAT_STATUS (Register 0x1E) = 0x0C as follows:
   a. BUF_READ (Bit 3) = 1
   b. MEM_ACCESS (Bit 2) = 1
   c. RUN (Bit 0) = 0
   d. After reading data from SRAM registers, disable the BUF_READ and MEM_ACCESS bits.
6. Write to or read from SPI registers. Update the RUN bit and the RAMUPDATE bit and the end of the write sequence as follows:
   a. Set waveform select to SRAM in WAV_CONFIG (Register 0x27).
   b. Set SRAM start and stop addresses (can be anywhere from 0x000 to 0xFFF).
   c. Set DAC digital gain in DAC_DGAIN (Register 0x35).
   d. (Optional) Set DAC digital offset in DACDOF (Register 0x25).
   e. Update the RUN bit (Register 0x1E).
   f. Update the RAMUPDATE bit (Register 0x1D).
7. Set Trigger terminal (Pin 32) to Logic 0 (low) to start pattern generation.

APPLICATIONS INFORMATION

Programming Examples

For the programming examples (Figure 53 to Figure 58), the register value files and SRAM vectors can be obtained by downloading **EVAL-AD910x Program Files** under the **Code Examples** section from EVAL-AD9102 Software.

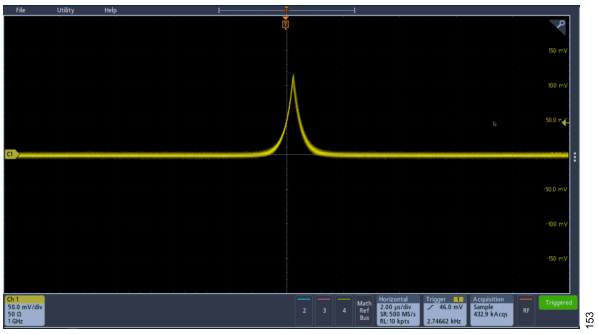

Figure 53. Programming Example 1: Gaussian Pulse from an SRAM Vector

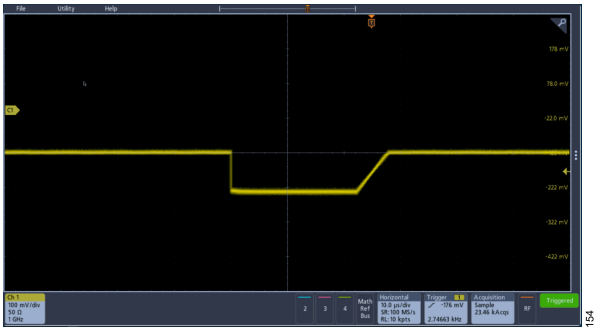

Figure 54. Programming Example 2: Pulse Generated from an SRAM Vector

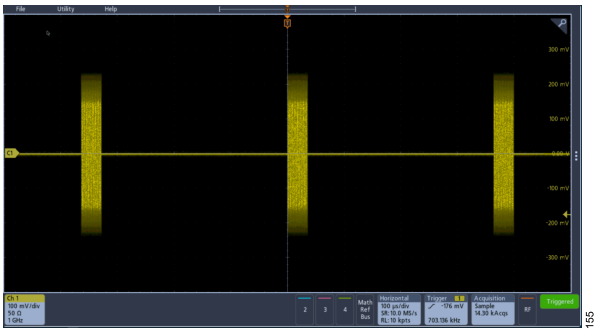

Figure 55. Programming Example 3: Pulsed-DDS Generated Sine Wave from a Prestored Waveform

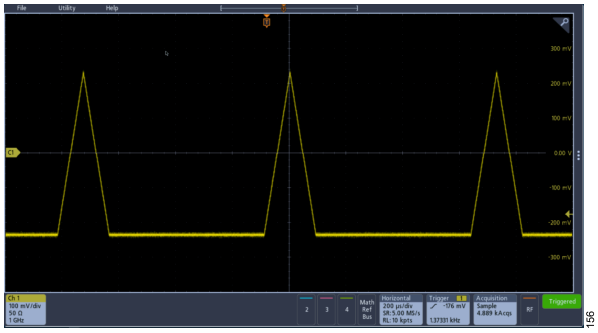

Figure 56. Programming Example 4: Sawtooth Waveform

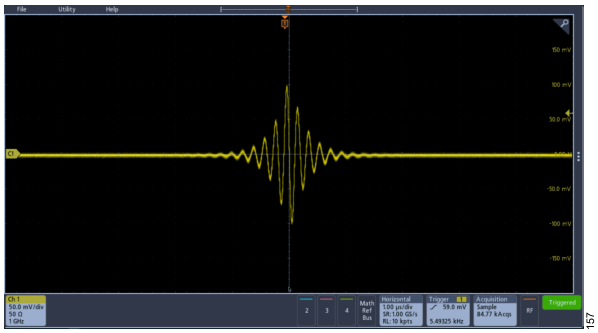

Figure 57. Programming Example 5: Pulsed-DDS Generated Sine Wave Amplitude Modulated by an SRAM Vector

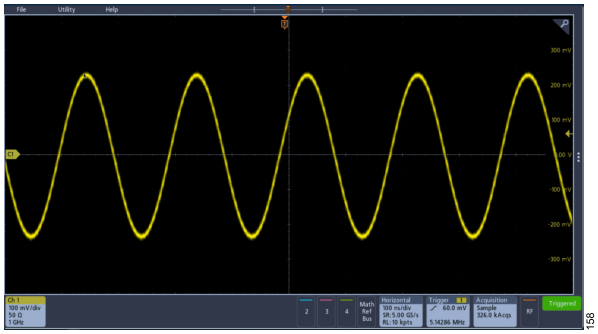

Figure 58. Programming Example 6: DDS-Generated Sine Wave

REGISTER MAP

Table 15. Register Summary

Addr	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	SPICONFIG	[15:8]	LSBFIRST	SPI3WIRE	RESET	DOUBLESPI	SPI_DRV	DOUT_EN	RESERVED		0x00	RW
		[7:0]	RESERVED		DOUT_ENM	SPI_DRVM	DOUBLESPIM	RESETM	SPI3WIREM	LSBFIRSTM		
0x01	POWERCONFIG	[15:8]	RESERVED				CLK_LDO_STAT	DIG1_LDO_STAT	DIG2_LDO_STAT	PDN_LDO_CLK	0x00	RW
		[7:0]	PDN_LDO_DIG1	PDN_LDO_DIG2	REF_PDN	REF_EXT	DAC_SLEEP	RESERVED				
0x02	CLOCKCONFIG	[15:8]	RESERVED				DIS_CLK	RESERVED			0x00	RW
		[7:0]	DIS_DCLK	CLK_SLEEP	CLK_PDN	EPS	DAC_INV_CLK	RESERVED				
0x03	REFADJ	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED		BGDR							
0x07	DACAGAIN	[15:8]	RESERVED	DAC_GAIN_CAL							0x00	RW
		[7:0]	RESERVED	DAC_GAIN								
0x08	DACRANGE	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED						DAC_GAIN_RNG			
0x0C	DACRSET	[15:8]	DAC_RSET_NE	RESERVED		DAC_RSET_CAL					0x0A	RW
		[7:0]	RESERVED			DAC_RSET						
0x0D	CALCONFIG	[15:8]	RESERVED	COMP_OFFSET_OF	COMP_OFFSET_UF	RSET_CAL_OF	RSET_CAL_UF	GAIN_CAL_OF	GAIN_CAL_UF	CAL_RESET	0x00	RW
		[7:0]	CAL_MODE	CAL_MODE_EN	COMP_CAL_RNG		CAL_CLK_EN	CAL_CLK_DIV				
0x0E	COMPOFFSET	[15:8]	RESERVED	COMP_OFFSET_CAL							0x00	RW
		[7:0]	RESERVED						CAL_FIN	START_CAL		
0x1D	RAMUPDATE	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED							RAMUPDATE		
0x1E	PAT_STATUS	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED				BUF_READ	MEM_ACCESS	PATTERN	RUN		
0x1F	PAT_TYPE	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED							PATTERN_RPT		
0x20	PATTERN_DLY	[15:8]	PATTERN_DELAY[15:8]								0x0E	RW
		[7:0]	PATTERN_DELAY[7:0]									
0x25	DACDOF	[15:8]	DAC_DIG_OFFSET[11:4]								0x00	RW
		[7:0]	DAC_DIG_OFFSET[3:0]				RESERVED					
0x27	WAV_CONFIG	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED		PRESTORE_SEL		RESERVED	CH_ADD	WAVE_SEL			
0x28	PAT_TIMEBASE	[15:8]	RESERVED				HOLD				0x0111	RW
		[7:0]	PAT_PERIOD_BASE				START_DELAY_BASE					
0x29	PAT_PERIOD	[15:8]	PATTERN_PERIOD[15:8]								0x8000	RW
		[7:0]	PATTERN_PERIOD[7:0]									
0x2B	DAC_PAT	[15:8]	RESERVED								0x0101	RW
		[7:0]	DAC_REPEAT_CYCLE									
0x2C	DOUT_START	[15:8]	DOUT_START[15:8]								0x03	RW
		[7:0]	DOUT_START[7:0]									

REGISTER MAP

Table 15. Register Summary (Continued)

Addr	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2D	DOUT_CONFIG	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED		DOUT_VAL	DOUT_MODE	DOUT_STOP					
0x31	DAC_CST	[15:8]	DAC_CONST[11:4]								0x00	RW
		[7:0]	DAC_CONST[3:0]				RESERVED					
0x35	DAC_DGAIN	[15:8]	DAC_DIG_GAIN[11:4]								0x00	RW
		[7:0]	DAC_DIG_GAIN[3:0]				RESERVED					
0x37	SAW_CONFIG	[15:8]	RESERVED								0x00	RW
		[7:0]	SAW_STEP						SAW_TYPE			
0x38 to 0x3D	RESERVED		RESERVED									
0x3E	DDS_TW32	[15:8]	DDSTW_MSB[15:8]								0x00	RW
		[7:0]	DDSTW_MSB[7:0]									
0x3F	DDS_TW1	[15:8]	DDSTW_LSB								0x00	RW
		[7:0]	RESERVED									
0x43	DDS_PW	[15:8]	DDS_PHASE[15:8]								0x00	RW
		[7:0]	DDS_PHASE[7:0]									
0x44	TRIG_TW_SEL	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED						TRIG_DELAY_EN	RESERVED		
0x45	DDS_CONFIG	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED				DDS_COS_EN	DDS_MSB_EN	PHASE_MEM_EN	TW_MEM_EN		
0x47	TW_RAM_CONFIG	[15:8]	RESERVED								0x00	RW
		[7:0]	RESERVED			TW_MEM_SHIFT						
0x5C	START_DELAY	[15:8]	START_DELAY[15:8]								0x00	RW
		[7:0]	START_DELAY[7:0]									
0x5D	START_ADDR	[15:8]	START_ADDR[11:4]								0x00	RW
		[7:0]	START_ADDR[3:0]				RESERVED					
0x5E	STOP_ADDR	[15:8]	STOP_ADDR[11:4]								0x00	RW
		[7:0]	STOP_ADDR[3:0]				RESERVED					
0x5F	DDS_CYC	[15:8]	DDS_CYC[15:8]								0x01	RW
		[7:0]	DDS_CYC[7:0]									
0x60	CFG_ERROR	[15:8]	ERROR_CLEAR	RESERVED							0x00	R
		[7:0]	RESERVED		DOUT_START_LG_ERR	PAT_DLY_SHORT_ERR	DOUT_START_SHORT_ERR	PERIOD_SHORT_ERR	ODD_ADDR_ERR	MEM_READ_ERR		
0x6000 to 0x6FFF	SRAM_DATA	[15:8]	SRAM_DATA[13:6]								0x00	RW
		[7:0]	SRAM_DATA[5:0]						RESERVED			

REGISTER DESCRIPTIONS

SPI CONTROL REGISTER (SPICONFIG, ADDRESS 0X00)

Table 16. Bit Descriptions for SPICONFIG

Bits	Bit Name	Settings	Description	Reset	Access
15	LSBFIRST		LSB first selection.	0	R/$\overline{W}$
		0	MSB first per SPI standard (default).		
		1	LSB first per SPI standard.		
14	SPI3WIRE		Selects if SPI is using 3-wire or 4-wire interface.	0	R/$\overline{W}$
		0	4-wire SPI (default).		
		1	3-wire SPI.		
13	RESET		Executes software reset of SPI and controllers, reloads default register values, except for Register 0x00.	0	R/$\overline{W}$
		0	Normal status.		
		1	Reset whole register map, except for Register 0x00.		
12	DOUBLESPI		Double SPI data line.	0	R/$\overline{W}$
		0	The SPI port has only 1 data line and can be used as a 3-wire or 4-wire interface.		
		1	The SPI port has two data lines both bidirectional defining a pseudo dual 3-wire interface where $\overline{CS}$ and SCLK are shared between the two ports. This mode is available only for SRAM data read or write.		
11	SPI_DRV		Double drive ability for SPI output.	0	R/$\overline{W}$
		0	Single SPI output drive ability.		
		1	Two time drive ability on SPI output.		
10	DOUT_EN		Enable DOUT signal on SDO/SDI2/DOUT pin.	0	R/$\overline{W}$
		0	SDO/SDI2 function input/output.		
		1	DOUT function output.		
[9:6]	RESERVED			0x0	R/$\overline{W}$
5	DOUT_ENM[1]		Enable DOUT signal on SDO/SDI2/DOUT pin.	0	R/$\overline{W}$
4	SPI_DRVM[1]		Double drive ability for SPI output.	0	R/$\overline{W}$
3	DOUBLESPIM[1]		Double SPI data line.	0	R/$\overline{W}$
2	RESETM[1]		Executes software reset of SPI and controllers, reloads default register values, except for Register 0x00.	0	R/$\overline{W}$
1	SPI3WIREM[1]		Selects if SPI is using 3-wire or 4-wire interface.	0	R/$\overline{W}$
0	LSBFIRSTM[1]		LSB first selection.	0	R/$\overline{W}$

[1] SPICONFIG[10:15] must always be set to the mirror of SPICONFIG[5:0] to allow easy recovery of the SPI operation when LSBFIRST bit is set incorrectly. (Bit 15 = Bit 0, Bit 14 = Bit 1, Bit 13 = Bit 2, Bit 12 = Bit 3, Bit 11 = Bit 4, and Bit 10 = Bit 5.)

POWER STATUS REGISTER (POWERCONFIG, ADDRESS 0X01)

Table 17. Bit Descriptions for POWERCONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED			0x0	R/$\overline{W}$
11	CLK_LDO_STAT		Read-only flag indicating the 1.8 V CLDO is on.	0	R
10	DIG1_LDO_STAT		Read-only flag indicating the 1.8 V DVDD1 LDO is on.	0	R
9	DIG2_LDO_STAT		Read-only flag indicating the 1.8 V DVDD2 LDO is on.	0	R
8	PDN_LDO_CLK		Disables the 1.8 V CLDO. An external supply is required.	0	R/$\overline{W}$
7	PDN_LDO_DIG1		Disables the DVDD1 LDO. An external supply is required.	0	R/$\overline{W}$
6	PDN_LDO_DIG2		Disables the DVDD2 LDO. An external supply is required.	0	R/$\overline{W}$
5	REF_PDN		Disables 10 kΩ resistor that creates REFIO voltage. User can drive with external voltage or provide external bandgap (BG) resistor.	0	R/$\overline{W}$
4	REF_EXT		Power down main BG reference including DAC bias.	0	R/$\overline{W}$
3	DAC_SLEEP		Disables DAC output current.	0	R/$\overline{W}$

REGISTER DESCRIPTIONS

Table 17. Bit Descriptions for POWERCONFIG (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
[2:0]	RESERVED			0x0	RW

CLOCK CONTROL REGISTER (CLOCKCONFIG, ADDRESS 0X02)

Table 18. Bit Descriptions for CLOCKCONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED			0x0	RW
11	DIS_CLK		Disable the analog clock to the DAC out of the clock distribution block.	0	RW
[10:8]	RESERVED			0x0	RW
7	DIS_DCLK		Disable the clock to core digital block.	0	RW
6	CLK_SLEEP		Enables a very low power clock mode.	0	RW
5	CLK_PDN		Disables and powers down the main clock receiver. No clocks are active in the part.	0	RW
4	EPS		Enables Power Save (EPS). This enables a low power option for clock receiver, but maintains low jitter performance on the DAC clock rising edge. The DAC clock falling edge is substantially degraded.	0	RW
3	DAC_INV_CLK		Cannot use EPS while using this bit. Inverts the clock inside DAC Core allowing a 180° phase shift in DAC update timing.	0	RW
[2:0]	RESERVED			0x0	RW

REFERENCE RESISTOR REGISTER (REFADJ, ADDRESS 0X03)

Table 19. Bit Descriptions for REFADJ

Bits	Bit Name	Settings	Description	Reset	Access
[15:6]	RESERVED			0x000	RW
[5:0]	BGDR		Adjusts the BG 10 kΩ resistor (nominal) to 8 kΩ to 12 kΩ, which changes the BG voltage from 840 mV to 1.24 V, respectively (see Figure 33). Scaling is 6.25 mV per LSB.	0x00	RW
		0x20	On-chip reference voltage of 1.24 V		
		0x00	On-chip reference voltage of 1.04 V (default)		
		0x1F	On-chip reference voltage of 840 mV		

DAC ANALOG GAIN REGISTER (DACAGAIN, ADDRESS 0X07)

Table 20. Bit Descriptions for DACAGAIN

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED			0	RW
[14:8]	DAC_GAIN_CAL		DAC analog gain calibration output—read only	0x00	R
7	RESERVED			0	RW
[6:0]	DAC_GAIN		DAC analog gain control while not in calibration mode—two's complement format. This allows to have fine gain control/adjustments in the DAC output current. The range of the fine gain adjustments and resolution of DACAGAIN depend on DAC_GAIN_RNG (Register 0x08, Bits[1:0]). For wider range and better accuracy, use digital gain registers.	0x00	RW

DAC ANALOG GAIN RANGE REGISTER (DACRANGE, ADDRESS 0X08)

Table 21. Bit Descriptions for DACRANGE

Bits	Bit Name	Settings	Description	Reset	Access
[15:2]	RESERVED			0x00	RW
[1:0]	DAC_GAIN_RNG		DAC gain range control, two's complement format.	0x0	RW
		0x0	±33% * 0.25		
		0x1	±33% * 0.50		
		0x2	±33% * 0.75		

REGISTER DESCRIPTIONS

Table 21. Bit Descriptions for DACRANGE (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		0x3	±33% * 1.00		

FSADJ REGISTER (DACRSET, ADDRESS 0X0C)

Table 22. Bit Descriptions for DACRSET

Bits	Bit Name	Settings	Description	Reset	Access
15	DAC_RSET_EN		For write, enable the internal R_{SET} resistor for the DAC; for read, R_{SET} for the DAC is enabled during calibration mode.	0	R/$\overline{W}$
[14:13]	RESERVED			0x0	R/$\overline{W}$
[12:8]	DAC_RSET_CAL		Digital control of the R_{SET} resistor for the DAC after calibration—read only.	0x00	R
[7:5]	RESERVED			0x0	R/$\overline{W}$
[4:0]	DAC_RSET		Digital control to set the value of the R_{SET} resistor in the DAC. The scaling/resolution of DAC_RSET is 800 Ω per LSB.	0x0A	R/$\overline{W}$
		0x05	R_{SET} is set to 4 kΩ (minimum).		
		0x0A	R_{SET} is set to 8 kΩ (default).		
		0x14	R_{SET} is set to 16 kΩ (maximum).		

CALIBRATION REGISTER (CALCONFIG, ADDRESS 0X0D)

Table 23. Bit Descriptions for CALCONFIG

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED			0	R/$\overline{W}$
14	COMP_OFFSET_OF		Compensation offset calibration value overflow.	0	R
13	COMP_OFFSET_UF		Compensation offset calibration value underflow.	0	R
12	RSET_CAL_OF		R_{SET} calibration value overflow.	0	R
11	RSET_CAL_UF		R_{SET} calibration value underflow.	0	R
10	GAIN_CAL_OF		Gain calibration value overflow.	0	R
9	GAIN_CAL_UF		Gain calibration value underflow.	0	R
8	CAL_RESET		Pulse this bit high and low to reset the calibration results.	0	R/$\overline{W}$
7	CAL_MODE		Read-only flag indicating calibration is being used.	0	R
6	CAL_MODE_EN		Enables the gain calibration circuitry.	0	R/$\overline{W}$
[5:4]	COMP_CAL_RNG		Offset calibration range.	0x0	R/$\overline{W}$
3	CAL_CLK_EN		Enables the calibration clock to calibration circuitry.	0	R/$\overline{W}$
[2:0]	CAL_CLK_DIV		Sets divider from DAC clock to calibration clock. Clock dividers are powers of 2 (that is 2^{2+N}). Note that the calibration clock must be less than 500 kHz.	0x0	R/$\overline{W}$
		0x0	CLK Divider = 4		
		0x1	CLK Divider = 8		
		0x2	CLK Divider = 16		
		0x3	CLK Divider = 32		
		0x4	CLK Divider = 64		
		0x5	CLK Divider = 128		
		0x6	CLK Divider = 256		
		0x7	CLK Divider = 512 (default)		

COMP OFFSET REGISTER (COMPOFFSET, ADDRESS 0X0E)

Table 24. Bit Descriptions for COMPOFFSET

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED			0	R/$\overline{W}$

REGISTER DESCRIPTIONS

Table 24. Bit Descriptions for COMPOFFSET (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
[14:8]	COMP_OFFSET_CAL		The result of the offset calibration for the comparator.	0x00	R
[7:2]	RESERVED			0x00	R/W
1	CAL_FIN		Read only flag indicating calibration is completed.	0	R
0	START_CAL		Start a calibration cycle.	0	R/W

UPDATE PATTERN REGISTER (RAMUPDATE, ADDRESS 0X1D)

Table 25. Bit Descriptions for RAMUPDATE

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x000	R/W
0	RAMUPDATE		Update all SPI settings with a new configuration (self-clearing).	0	R/W

COMMAND/STATUS REGISTER (PAT_STATUS, ADDRESS 0X1E)

Table 26. Bit Descriptions for PAT_STATUS

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	RESERVED			0x000	R/W
3	BUF_READ		Read back from updated buffer.	0	R/W
2	MEM_ACCESS		Memory (SRAM) SPI access enable.	0	R/W
1	PATTERN		Status of pattern being played (Read only).	0	R
0	RUN		Allows the pattern generation and stop pattern after trigger.	0	R/W

COMMAND/STATUS REGISTER (PAT_TYPE, ADDRESS 0X1F)

Table 27. Bit Descriptions for PAT_TYPE

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	RESERVED			0x0000	R/W
0	PATTERN_RPT		Setting this bit allows the pattern to repeat a number of times defined in DAC_PAT (Register 0x2B).	0	R/W
		0	Pattern continuously runs.		
		1	Pattern repeats the number of times defined in DAC_PAT (Register 0x2B).		

TRIGGER START TO REAL PATTERN DELAY REGISTER (PATTERN_DLY, ADDRESS 0X20)

Table 28. Bit Descriptions for PATTERN_DLY

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	PATTERN_DELAY		Number of DAC clock cycles + 1 that it takes between Trigger low and pattern start. Increment = 1.	0x000E	R/W
		0x000E	Sets Pattern Delay to minimum—14 (default).		
		0xFFFF	Sets Pattern Delay to maximum—65535.		

DAC DIGITAL OFFSET REGISTER (DACDOF, ADDRESS 0X25)

Table 29. Bit Descriptions for DACDOF

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	DAC_DIG_OFFSET		DAC digital offset.	0x000	R/W
		0x800	Digital offset = −0.500		
		0xC00	Digital offset = −0.250		
		0x000	Digital offset = 0		
		0x400	Digital offset = 0.250		

REGISTER DESCRIPTIONS

Table 29. Bit Descriptions for DACDOF (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		0x7FF	Digital offset = $0.500 \cong {}^{2047}/_{4096}$		
[3:0]	RESERVED			0x0	R$\overline{W}$

WAVE SELECT REGISTER (WAV_CONFIG, ADDRESS 0X27)

Table 30. Bit Descriptions for WAV_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[15:10]	RESERVED			0x0	R$\overline{W}$
[9:8]	RESERVED			0x1	R$\overline{W}$
[7:6]	RESERVED			0x0	R$\overline{W}$
[5:4]	PRESTORE_SEL		DAC Prestored waveform selection.	0x0	R$\overline{W}$
		0	Constant value held into DAC constant value MSB/LSB register.		
		1	Sawtooth defined in the DAC sawtooth configuration register (SAW_CONFIG).		
		2	Pseudorandom sequence.		
		3	DDS output.		
3	RESERVED			0	R$\overline{W}$
2	CH_ADD	0	Normal operation for the DAC.	0	R$\overline{W}$
[1:0]	WAVE_SEL		Selects source of waveform output for DAC.	0x1	R$\overline{W}$
		0	Waveform read from RAM between START_ADDR and STOP_ADDR.		
		1	Prestored waveform.		
		2	Prestored waveform using START_DELAY and PATTERN_PERIOD.		
		3	Prestored waveform modulated by waveform from RAM.		

DAC TIME CONTROL REGISTER (PAT_TIMEBASE, ADDRESS 0X28)

Table 31. Bit Descriptions for PAT_TIMEBASE

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED			0x0	R$\overline{W}$
[11:8]	HOLD		Specifies how long the DAC holds the SRAM sample in terms of DAC clock periods. This can be used for coarse adjustment of the SRAM increment clock.	0x1	R$\overline{W}$
		0x0	DAC holds each sample for 16 DAC clock periods.		
		0x1	DAC holds each sample for 1 DAC clock period (default).		
		0xF	DAC holds each sample for 15 DAC clock periods.		
[7:4]	PAT_PERIOD_BASE		The number of DAC clock periods per PATTERN_PERIOD LSB	0x1	R$\overline{W}$
		0x0	PATTERN_PERIOD LSB = 16 DAC clock periods.		
		0x1	PATTERN_PERIOD LSB = 1 DAC clock period (default).		
		0xF	PATTERN_PERIOD LSB = 15 DAC clock periods.		
[3:0]	START_DELAY_BASE		Number of DAC clock periods per START_DELAY × LSB (0 = START_DELAY × LSB = 1 DAC clock period).	0x1	R$\overline{W}$
		0x0	START_DELAY LSB = 16 DAC clock periods.		
		0x1	START_DELAY LSB = 1 DAC clock period (default).		
		0xF	START_DELAY LSB = 15 DAC clock periods.		

PATTERN PERIOD REGISTER (PAT_PERIOD, ADDRESS 0X29)

Table 32. Bit Descriptions for PAT_PERIOD

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	PATTERN_PERIOD		Pattern period register.	0x8000	R$\overline{W}$

REGISTER DESCRIPTIONS

DAC PATTERN REPEAT CYCLES REGISTER (DAC_PAT, ADDRESS 0X2B)

Table 33. Bit Descriptions for DAC_PAT

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x01	R/W
[7:0]	DAC_REPEAT_CYCLE		The number of DAC pattern repeat cycles + 1, (0 → repeat 1 pattern).	0x01	R/W

$\overline{\text{TRIGGER}}$ START TO DOUT SIGNAL REGISTER (DOUT_START, ADDRESS 0X2C)

Table 34. Bit Descriptions for DOUT_START

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	DOUT_START		Time between Trigger low and DOUT signal high in number of DAC clock cycles. Increment = 1.	0x0003	R/W
		0x0003	3 DAC clock cycles (minimum).		
		0xFFFF	65535 DAC clock cycles (maximum).		

DOUT CONFIGURATION REGISTER (DOUT_CONFIG, ADDRESS 0X2D)

Table 35. Bit Descriptions for DOUT_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[15:6]	RESERVED			0x000	R/W
5	DOUT_VAL		Manually sets DOUT signal value; only valid when DOUT_MODE = 0 (manual mode).	0	R/W
4	DOUT_MODE		Set different enable signal mode.	0	R/W
		0	DOUT pin is output from SDO/SDI2/DOUT pin and is manually controlled by Bit 5 (DOUT_ENM) and Bit 10 (DOUT_EN) in Register 0x00, which must be set to use this feature.		
		1	DOUT pin is output from SDO/SDI2/DOUT. The pin is controlled by DOUT_START and DOUT_STOP fields. Bit 5 (DOUT_ENM) and Bit 10 (DOUT_EN) in Register 0x00 must be set to use this feature.		
[3:0]	DOUT_STOP		Time between pattern end and DOUT signal low in number of DAC clock cycles. Increment = 1.	0x0	R/W
		0x0	0 DAC clock cycles (minimum)		
		0xF	15 DAC clock cycles (maximum)		

DAC CONSTANT VALUE REGISTER (DAC_CST, ADDRESS 0X31)

Table 36. Bit Descriptions for DAC_CST

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	DAC_CONST		Most significant byte of DAC constant value	0x000	R/W
		0x7FF	Digital constant = IOUTFS − 1 LSB		
		0x000	Digital constant = 0		
		0x800	Digital constant = −IOUTFS + 1 LSB		
[3:0]	RESERVED			0x0	R/W

DAC DIGITAL GAIN REGISTER (DAC_DGAIN, ADDRESS 0X35)

Table 37. Bit Descriptions for DAC_DGAIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	DAC_DIG_GAIN		DAC digital gain. Range +2 to −2.	0x000	R/W
		0x400	Multiplies digital data at DAC channel path by +1		
		0x7FF	Multiplies digital data at DAC channel path by +2		
		0x800	Multiplies digital data at DAC channel path by −2		
		0xC00	Multiplies digital data at DAC channel path by −1		

REGISTER DESCRIPTIONS

Table 37. Bit Descriptions for DAC_DGAIN (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	RESERVED			0x0	RW

DAC SAWTOOTH CONFIGURATION REGISTER (SAW_CONFIG, ADDRESS 0X37)

Table 38. Bit Descriptions for SAW_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED			0x01	RW
[7:2]	SAW_STEP		Number of samples per step for the DAC. Up to 64 samples per step.	0x01	RW
[1:0]	SAW_TYPE		The type of sawtooth (positive, negative or triangle) for the DAC.	0x0	RW
		0x0	Ramp up saw wave.		
		0x1	Ramp down saw wave.		
		0x2	Triangle saw wave.		
		0x3	No wave, zero.		

DDS TUNING WORD MSB REGISTER (DDS_TW32, ADDRESS 0X3E)

Table 39. Bit Descriptions for DDS_TW32

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	DDSTW_MSB		DDS tuning word MSB.	0x0000	RW

DDS TUNING WORD LSB REGISTER (DDS_TW1, ADDRESS 0X3F)

Table 40. Bit Descriptions for DDS_TW1

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	DDSTW_LSB		DDS tuning word LSB.	0x00	RW
[7:0]	RESERVED			0x00	RW

DDS PHASE OFFSET REGISTER (DDS_PW, ADDRESS 0X43)

Table 41. Bit Descriptions for DDS1_PW

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	DDS_PHASE		DDS phase offset.	0x0000	RW
		0x0000	DDS phase offset = 0°		
		0x4000	DDS phase offset = 90°		
		0x8000	DDS phase offset = 180°		
		0xC000	DDS phase offset = 270°		

PATTERN CONTROL 1 REGISTER (TRIG_TW_SEL, ADDRESS 0X44)

Table 42. Bit Descriptions for TRIG_TW_SEL

Bits	Bit Name	Settings	Description	Reset	Access
[15:2]	RESERVED			0x0000	RW
1	TRIG_DELAY_EN		Enable start delay as trigger delay for DAC channel.	0	RW
		0	Delay repeats for all patterns.		
		1	Delay is only at the start of first pattern.		
0	RESERVED			0	RW

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PATTERN CONTROL 2 REGISTER (DDS_CONFIG, ADDRESS 0X45)

Table 43. Bit Descriptions for DDS_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	RESERVED			0x000	RW
3	DDS_COS_EN		Enables DDS cosine output of DDS instead of sine wave.	0	RW
2	DDS_MSB_EN		Enables the clock for the SRAM address counter. Increment is coming from the DDS MSB.	0	RW
		0	DAC Clock CLKP/CLKN (default)		
		1	Rising edge of the DDS output MSB. This can be used when the SRAM contains a list of DDS tuning words.		
1	PHASE_MEM_EN		Enables DDS phase offset input coming from SRAM reading START_ADDR. Because phase word is 8 bits and SRAM data is 14 bits, only 8 MSB of SRAM are taken into account.	0	RW
		0	Selects the DDS_PW as the source of DDS offset.		
		1	Selects the SRAM as source of DDS phase offset input.		
0	TW_MEM_EN		Enables DDS tuning word input coming from SRAM reading using START_ADDR. Because tuning word is 24 bits and SRAM data is 14 bits, 14 bits are set to 0s depending on the value of the TW_MEM_SHIFT (Register 0x47, Bits[4:0]).	0	RW
		0	Selects the DDS_TW registers as the source for DDS tuning words (default)		
		1	Selects the SRAM and DDS_TW registers as configured in the TW_RAM_CONFIG register as the source of DDS tuning word input.		

TW_RAM_CONFIG REGISTER (TW_RAM_CONFIG, ADDRESS 0X47)

Table 44. Bit Descriptions for TW_RAM_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[15:5]	RESERVED			0x000	RW
[4:0]	TW_MEM_SHIFT		TW_MEM_EN must be set to 1 to use this bit field.	0x00	RW
		0x00	DDSTW = {RAM[13:0],10'b0}		
		0x01	DDSTW = {DDSTW[23],RAM[13:0],9'b0}		
		0x02	DDSTW = {DDSTW[23:22],RAM[13:0],8'b0}		
		0x03	DDSTW = {DDSTW[23:21],RAM[13:0],7'b0}		
		0x04	DDSTW = {DDSTW[23:20],RAM[13:0],6'b0}		
		0x05	DDSTW = {DDSTW[23:19],RAM[13:0],5'b0}		
		0x06	DDSTW = {DDSTW[23:18],RAM[13:0],4'b0}		
		0x07	DDSTW = {DDSTW[23:17],RAM[13:0],3'b0}		
		0x08	DDSTW = {DDSTW[23:16],RAM[13:0],2'b0}		
		0x09	DDSTW = {DDSTW[23:15],RAM[13:0],1'b0}		
		0x0A	DDSTW = {DDSTW[23:14],RAM[13:0]}		
		0x0B	DDSTW = {DDSTW[23:13],RAM[13:1]}		
		0x0C	DDSTW = {DDSTW[23:12],RAM[13:2]}		
		0x0D	DDSTW = {DDSTW[23:11],RAM[13:3]}		
		0x0E	DDSTW = {DDSTW[23:10],RAM[13:4]}		
		0x0F	DDSTW = {DDSTW[23:9],RAM[13:5]}		
		0x10	DDSTW = {DDSTW[23:8],RAM[13:6]}		
		0x11 to 0x1F	Reserved		

START DELAY REGISTER (START_DLY, ADDRESS 0X5C)

Table 45. Bit Descriptions for START_DLY

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	START_DELAY		Start delay of DAC.	0x0000	RW

REGISTER DESCRIPTIONS

START ADDRESS REGISTER (START_ADDR, ADDRESS 0X5D)

Table 46. Bit Descriptions for START_ADDR

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	START_ADDR		RAM address where DAC starts to read waveform.	0x000	R/W
[3:0]	RESERVED			0x0	R/W

STOP ADDRESS REGISTER (STOP_ADDR, ADDRESS 0X5E)

Table 47. Bit Descriptions for STOP_ADDR

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	STOP_ADDR		RAM address where DAC stops to read waveform.	0x000	R/W
[3:0]	RESERVED			0x0	R/W

DDS CYCLES REGISTER (DDS_ CYC, ADDRESS 0X5F)

Table 48. Bit Descriptions for DDS_CYC

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	DDS_CYC		Number of sine wave cycles when DDS prestored waveform using START_DELAY and PATTERN_PERIOD is selected for DAC output.	0x0001	R/W

CONFIGURATION ERROR REGISTER (CFG_ERROR, ADDRESS 0X60)

Table 49. Bit Descriptions for CFG_ERROR

Bits	Bit Name	Settings	Description	Reset	Access
15	ERROR_CLEAR		Writing this bit clears all errors.	0	R/W
[14:6]	RESERVED			0x000	R
5	DOUT_START_LG_ERR		When the DOUT_START value is larger than the pattern delay, this error is toggled.	0	R
4	PAT_DLY_SHORT_ERR		When the pattern delay value is smaller than the default value, this error is toggled. The actual PATTERN_DELAY_SHORT is 65536 – (14 – PATTERN_DELAY_SHORT).	0	R
2	DOUT_START_SHORT_ERR		When the DOUT_START value is smaller than the default value, this error is toggled. The actual DOUT_START is 65536 – (3 – DOUT_START).	0	R
2	PERIOD_SHORT_ERR		When the period register setting value is smaller than the pattern play cycle, this error is toggled.	0	R
1	ODD_ADDR_ERR		When the memory pattern play is not of even length in trigger delay mode, this error flag is toggled.	0	R
0	MEM_READ_ERR		When there is a memory read conflict, this error flag is toggled.	0	R

SRAM DATA REGISTER (SRAM_DATA, ADDRESS 0X6000 TO ADDRESS 0X6FFF)

Table 50. Bit Descriptions for SRAM_DATA

Bits	Bit Field Name	Settings	Description	Reset	Access
[15:8]	SRAM_DATA		SRAM_DATA[13:6]. The 8 MSBs of the programmable 14-bit SRAM_DATA.	0x00	R/W
[7:2]	SRAM_DATA		SRAM_DATA[5:0]. The 6 LSBs of the programmable 14-bit SRAM_DATA.	0x0	R/W
[1:0]	RESERVED			0x0	R/W

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CP-32-12	LFCSP	32-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD9102BCPZ	−40°C to +85°C	32-Lead LFCSP	TRAY, 490	CP-32-12
AD9102BCPZRL7	−40°C to +85°C	32-Lead LFCSP	REEL, 1500	CP-32-12

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
AD9102-ARDZ-EBZ	Evaluation Board

[1] Z = RoHS Compliant Part.