Click here for production status of specific part numbers.

MAX28200

16-Bit Microcontroller with ADC and I²C

General Description

The MAX28200 is a low-power, 16-bit MAXQ® microcontroller (µC) designed for low-power applications including smart phones, and consumer electronics. The device combines a powerful 16-bit RISC microcontroller with a 10-bit, 93.75ksps ADC along with an I²C communications port. The device includes four GPIO pins. The device includes 16KB of flash memory and 2KB of data SRAM. Additional utility ROM space includes macros such as an I²C bootloader to enable flash memory firmware updates in the field. The device provides NIST SP 800-185 compliant secure hash algorithm (SHA-3) KMAC challenge and response authentication and can be paired with other SHA-3 devices.

For the ultimate in low-power battery-operated performance, the device includes an ultra-low-power stop mode. In this mode, the minimum amount of circuitry is powered. The device wakes up on a matching I²C address. Wake-up sources also include external interrupts, the power-fail warning, and a wake-up timer interrupts. The microcontroller runs from a wide 1.71V to 3.63V operating voltage.

Applications

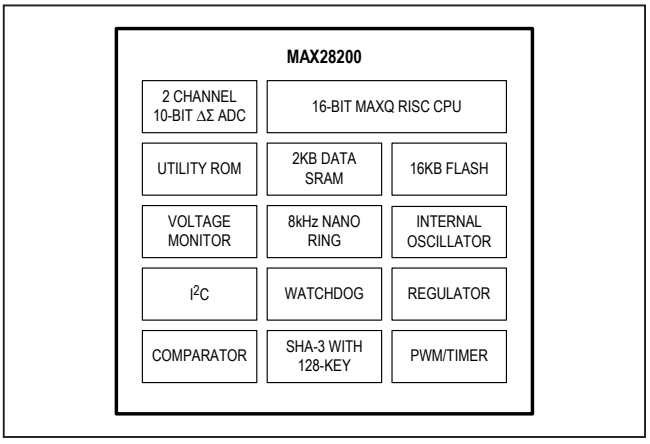
- Smartphones
- Consumer Electronics

Ordering Information appears at end of data sheet.

Benefits and Features

- High-Performance, Low-Power, 16-Bit RISC Core
- Internal 12MHz Oscillator Requires No External Components
- Two-Channel, 10-Bit 93.75ksps ADC
- I²C Slave Peripheral
  - 400kHz Operating Frequency
  - Flash Bootloader Function
  - Wakeup from Ultra-Low Power Stop Mode on I²C Address Match
- 16-Bit PWM Timer Output
- Wake-Up Timer
- SHA-3 KMAC Secure Authentication with RNG
- 1.71V to 3.63V Operating Voltage
- 16-Bit Instruction Word, 16-Bit Data Bus
- Memory Features
  - 16KB Flash Memory
  - 2KB Data SRAM
- -40°C to +85°C Operating Temperature
- Low Power Consumption
  - 0.2µA (typ), 2.0µA (max) in Stop Mode, T_A = +25°C, Power-Fail Monitor Disabled
  - 2.7mA (typ) at 12MHz in Active Mode
- 1.7mm x 1.8mm x 0.5mm 12-Bump WLP Package

Applications



19-100388; Rev 0; 8/18

maxim integrated™

Absolute Maximum Ratings

V_{DD}.....-0.3V to +3.63V
Any Ball .....-0.3V to +3.63V
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 WLP

Package Code	N121C1+1
Outline Number	**21-100300**
Land Pattern Number	Refer to **Application Note 1891**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	72.82°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}			V_{RST}		3.63	V
1.8V Internal Regulator	V_{REG18}			1.62	1.8	1.98	V
Power-Fail Warning Voltage	V_{PFW}	Rising V_{DD}	CMPCN[4:3] = 00		2.214		V
			CMPCN[4:3] = 01		2.503		
		Rising V_{DD}	CMPCN[4:3] = 10		2.805		
		Rising V_{DD}	CMPCN[4:3] = 11		3.005		
		Hysteresis	CMPCN[4:3] = 00		17		mV
			CMPCN[4:3] = 01		18		
			CMPCN[4:3] = 10		22		
			CMPCN[4:3] = 11		25		
Power-Fail Reset Voltage	V_{RST}				1.71		V
Power-On Reset Voltage	V_{POR}	Monitors V_{DD}			1.2		V
Active Current	I_{DD_1}	f_{SYSCLK} = 12MHz, executing code from flash memory, all inputs connected to GND/V_{DD}, outputs do not source or sink current			2.7	4.7	mA
Stop Mode Current	I_{S1}	T_A = +25°C (power-fail off)			0.4	2	µA
	I_{S2}	T_A = +25°C (power-fail on)			33	50	
Power Consumption During Power-On Reset	I_{POR}	During POR while $V_{DD} < V_{POR}$			450		nA
Stop Mode Resume Time	t_{ON}				375 + (16t_{CK})		µs
Input Low Voltage for All GPIO Pins	V_{IL}			V_{GND}		0.3 x V_{DD}	V
Input Low Voltage for SDA and SCL	V_{IL_I2C}			V_{GND}		0.54	V
Input High Voltage for All GPIO Pins	V_{IH}			0.7 x V_{DD}		V_{DD}	V
Input High Voltage for SDA and SCL	V_{IH_I2C}			1.35		V_{DD}	V
Input Hysteresis (Schmitt) for All GPIO Pins	V_{IHYS}	V_{DD} = 3.3V, T_A = +25°C			300		mV
Input Hysteresis (Schmitt) for SDA, SDL	V_{IHYS_I2C}	V_{DD} = 3.3V, T_A = +25°C			250		mV

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage for All GPIO, SDA, SCL	V_{OL}	V_{DD} = 3.6V, I_{OL} = 5.5mA		0.4	0.5	V
		V_{DD} = 2.35V, I_{OL} = 4mA		0.4	0.5	
		V_{DD} = 1.8V, I_{OL} = 2mA		0.4	0.5	
Output High Voltage All GPIO Pins	V_{OH}	I_{OH} = -2mA	V_{DD} - 0.5		V_{DD}	V
Input/Output Pin Capacitance	C_{IO}			15		pF
Input Leakage Current for All Pins	I_L	V_{IN} at 0V or V_{DD}, internal pullup disabled	-100		+100	nA
Input Pullup Resistor for P0.1, P0.2, P0.3	R_{PU}	V_{DD} = 3.0V, V_{OL} = 0.4V	16	28	39	kΩ
		V_{DD} = 1.8V, V_{OL} = 0.4V	18	31	43	
Internal Oscillator	f_{OSC}		10.8	12	13.2	MHz
System Clock Period	t_{CK}			$1/f_{OSC}$		ns
System Clock Frequency	f_{CK}			$1/t_{CK}$		MHz
Nanopower Ring Frequency	f_{NANO}	T_A = +25°C	3.0	8.0	20.0	kHz
Wakeup Timer Interval	t_{WAKEUP}		$1/f_{NANO}$		65,535/ f_{NANO}	s
FLASH MEMORY						
System Clock During Flash Programming/Erase	$f_{FPSYSCLK}$	$f_{FPSYSCLK}$/(FCKDIV[3:0]+1) must equal 1MHz, verify PFI = 0 before calling utility ROM		f_{OSC}		MHz
Flash Erase Time	t_{ME}	Mass erase		40		ms
	t_{ERASE}	Page erase		40		
Flash Programming Time Per Word	t_{PROG}	Excluding utility ROM overhead		40		µs
Flash Endurance			20			kcycles
Data Retention	t_{RET}	T_A = +25°C	100			years

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC (DELTA-SIGMA)						
Resolution				10		bits
ADC Clock Rate	f_{ACLK}	$f_{ACLK} = f_{OSC}$		12		MHz
ADC Clock Period	t_{ACLK}			$1/f_{ACLK}$		µs
Input Voltage Range	V_{AIN}		V_{GND}		V_{DD}	V
Analog Input Capacitance	C_{AIN}			1		pF
Integral Nonlinearity	INL	V_{IN} = -0.5dB full scale		±3		LSb
Differential Nonlinearity	DNL	V_{IN} = -0.5dB full scale		±3		LSb
Offset Error	V_{OS}			±3		LSb
ADC Active Current	I_{ADC}	ADEN = 1		280		µA
ADC Setup Time	t_{ADC_SU}	Settling time due to channel, reference or scale change (not production tested)		35		µs
ADC Oversampling Ratio	OSR			128		
ADC Output Latency	t_{ADC}			2 x OSR + 1		t_{ACLK}
ADC Throughtput	f_{ADC}	$f_{ADC} = f_{ACLK}/OSR$		93.75		ksps

Electrical Characteristics—I2C

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			µs
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs

Electrical Characteristics—I2C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs
FAST MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs

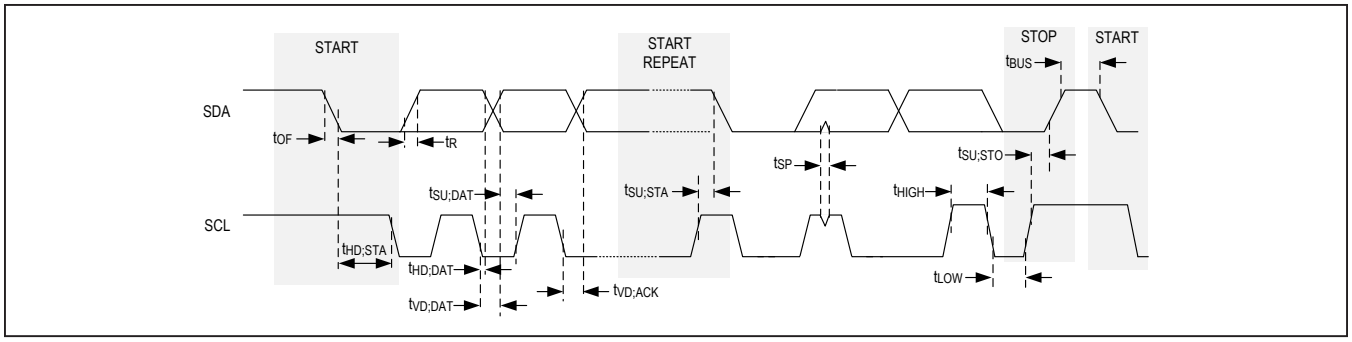
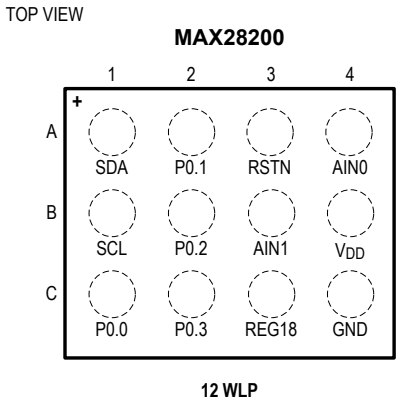


Figure 1. I2C Timing Diagram

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
A1	SDA	I2C Slave Data
A2	P0.1	Digital GPIO. Alternately, this pin can be configured as a PWM output.
A3	RSTN	Digital, Active-Low Reset Input. The device remains in reset as long as this pin is low and begins executing from the utility ROM at address 8000h when this pin returns to a high state. The pin includes pullup current source; if this pin is driven by an external device, it should be driven by an open-drain source capable of sinking in excess of 4mA. This pin can be left unconnected if there is no need to place the device in a reset state using an external signal.
A4	AIN0	Analog-to-Digital Input 0
B1	SCL	I2C Slave Clock
B2	P0.2	Digital GPIO. Alternately, this pin can be configured as CMP comparator negative input.
B3	AIN1	Analog-to-Digital Input 1
B4	V_{DD}	Supply Voltage. This pin must be connected to ground through a 0.47µF external ceramic chip capacitor. The capacitor must be placed as close as possible to this pin.
C1	P0.0	Digital GPIO
C2	P0.3	Digital GPIO. Alternately, this pin can be configured as CMP comparator positive input.
C3	REG18	1.8V Regulator Output. This pin must be connected to ground through a 0.47µF external ceramic chip capacitor. The capacitor must be placed as close as possible to this pin. No devices other than the capacitor should be connected to this pin.
C4	GND	Ground. Connect directly to the ground plane.

Detailed Description

The MAX28200 is a low-power, 16-bit MAXQ microcontroller (µC) designed for low-power applications including smartphones and consumer electronics. The device combines a powerful 16-bit RISC µC with a SP 800-185 compliant secure hash algorithm (SHA-3) challenge and response authentication system, 10-bit, 93.75ksps ADC, along with an I2C communications port. A general-purpose comparator can be configured for differential measurement or single-ended using the bandgap 1.23V as a reference. The device includes 4 GPIO pins.

The device includes 16KB of flash memory and 2KB of data SRAM. Additional utility ROM space includes macros such as an I2C bootloader to enable flash memory firmware updates in the field.

For the ultimate in low-power, battery-operated performance, the device includes an ultra-low-power stop mode (0.2µA typ). In this mode, the minimum amount of circuitry is powered. The device wakes up on a matching I2C address. Wake-up sources also include external interrupts, the power-fail warning, and a wake-up timer interrupts. The µC runs from a wide 1.71V to 3.63V operating voltage.

Microprocessor

The device is based on Maxim's low-power, 16-bit MAXQ20. The core supports the Harvard memory architecture with separate 16-bit program and data address buses. A fixed 16-bit instruction word is standard, but data can be arranged in 8 or 16 bits. The MAXQ core in the device is implemented as a pipe-lined processor with performance approaching 1MIPS per MHz. The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). A configurable soft stack supports program flow.

Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides maximum flexibility and reusability that are important for a microprocessor used in embedded applications.

The MAXQ instruction set is highly orthogonal. All arithmetical and logical operations can use any register in conjunction with the accumulator. Data movement is supported from any register to any other register. Memory is accessed through specific data-pointer registers with autoincrement/decrement support.

Memory

This device includes several memory types:

- 16KB flash memory
- 2KB SRAM data memory
- Dedicated utility ROM, including I2C bootloader
- Soft stack

Operating Modes

The lowest power mode of operation is stop mode. In this mode, CPU state and memories are preserved, but the CPU is not actively running. Wake-up sources include I2C address match, external I/O interrupts, the power-fail warning interrupt, wake-up timer, or a power-fail reset. Any time the microcontroller is in a state where code does not need to be executed, the user software can put the device into stop mode. The nanopower ring oscillator is an internal ultra low-power (400nA) 8kHz ring oscillator that can be used to drive a wake-up timer that exits stop mode. The wakeup timer is programmable by software in steps of 125µs up to approximately 8s.

SHA-3 Authentication

The MAX28200 contains an SP 800-185 compliant hardware SHA-3 KMAC engine with preprogrammed 128-bit secret key for challenge and response secure authentication.

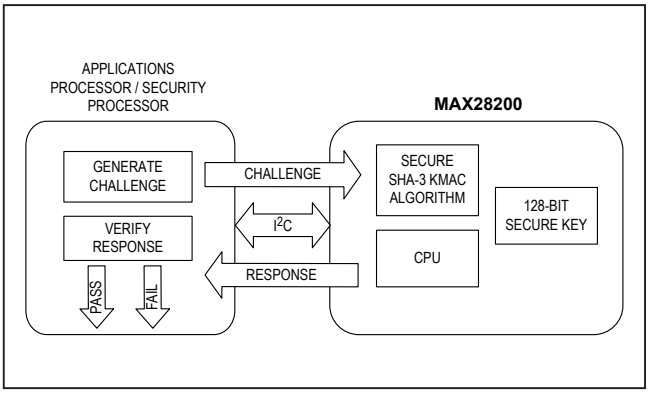


Figure 2. SHA-3 Authentication

ADC

The two-channel, 10-bit delta-sigma analog-to-digital converter (ADC) provides an integrated reference generator (bandgap).

I2C

The device supports the I2C slave protocol. The I2C bus is a 2-wire, bidirectional bus using a serial data line (SDA) and a serial clock line (SCL). Signals SDA and SCL are open-drain, allowing multiple devices to reside on the same bus. The microprocessor core can be awakened from its stop mode when an I2C address match (factory-programmed address) is received. External pullup resistors are required to pull the lines to a logic-high state.

An I2C master has ownership of the I2C bus, drives the clock, and generates the required protocol signals. This allows it to send data to a slave or receive data from a slave as required. One exception is when the MAX28200 performs clock-stretching. Slave devices that need some time to process a received byte or are not ready yet to send the next byte can pull the SCL low to signal to the master that it should wait. Once the clock is released the master can proceed with the next byte.

Alternatively, the device supports a technique where the master can effectively poll the device for the ACK bit to determine when the device is ready to send or receive more data bytes. To use this technique, clock-stretching must first be disabled and then the slave must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse. When a slave does not acknowledge (NACK) a received data byte, the data line must be left high by the slave. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. Should the master choose to generate a repeated START condition and transmit the device address, it can then wait for the device to respond with ACK pulling down the SDA line during the ACK clock pulse.

The device also supports a direct memory access (DMA) mode of operation. When active, I2C slave read and write accesses will allow 256 bytes of system SRAM to be accessed directly by the I2C interface. The contiguous 256 byte block can be positioned anywhere within the 2Kbyte memory space on 256 byte boundaries. SRAM data is accessed one byte at a time. The I2C master controls the SRAM address written and read through a locally maintained pointer. The pointer must be initialized by the first data byte write following an initial START, with a DMA address, and the R/W bit indicating a write operation. The initial START is defined as the first access after reset, or the first START issued after a STOP. The DMA state machine detects this sequence and directs the first byte of write data to the address pointer. All subsequent write or read data is directed to or from the SRAM. The pointer is incremented after any SRAM read or write operation, but can be reloaded at any time by issuing the STOP→START sequence.

The device supports two read modes. The default mode begins reading data during the I2C address acknowledge bit time. Data is read until the Tx FIFO is full. The DMA continues reading a new byte of data as soon as a byte is read from the FIFO. In this read ahead mode, unread data remains in the FIFO after the I2C master terminates the transaction. It is up to the host microcontroller to manage the residual data in the FIFO, by either letting it remain for the next read transaction or flushing the data from the FIFO. The second mode is an I2C EEPROM compatibility mode. In this mode, the DMA reads a single byte of SRAM data following an address ACK, and reads one additional byte after receipt of each master sourced TX_DATA (read) acknowledge. If a NACK is received following a TX_DATA operation, the read for the next byte of data is not initiated.

SRAM DMA writes are initiated once the entire byte is received through an I2C write. Writes are initiated one byte at a time, during the ACK bit time, once the data has been received. Writes are absolute and there is no bounds checking performed by the DMA if a address rollover condition occurs.

PWM/Timer

The device provides a PWM/Timer as an alternate function on one of the GPIO pins. The PWM/Timer is an enhanced timer with modifications to support different input clock prescaling and set/reset/compare output functionality:

- 16-bit timer/counter
- 16-bit up/down autoreload
- Counter function of external pulse
- 16-bit timer with capture
- 16-bit timer with compare
- Input/output enhancements for pulse-width modulation
- Set/reset/toggle output state on comparator match
- Prescaler with 2n divider (for n = 0, 2, 4, 6, 8, 10)

Comparator

The comparator provided can be configured for differential measurement or single-ended comparison to the bandgap 1.23V reference. The comparator is also used to provide the power-fail warning voltage indicator. Interrupts can be generated when a comparator event is detected with the transition direction of the monitored signal being programmable.

GPIO

The microcontroller provides four port pins for general-purpose I/O that have the following features:

- CMOS output drivers
- Schmitt trigger inputs
- Optional weak pullup to V_{DD} when operating in input mode

While the microcontroller is in a reset state, P0.1, P0.2, and P0.3 have weak pullups and their input buffers are disabled. P0.0 has a weak pulldown and its input buffer is disabled.

System Clock

The device provides an internal 12MHz oscillator that requires no external components, thereby reducing system cost, PCB area, and radiated EMI.

Watchdog Timer

The internal watchdog timer greatly increases system reliability. The watchdog timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the software periodically resets the counter so it never reaches its maximum count. However, if software operation is interrupted and the counter is not reset, a system reset is triggered and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer functions as the source of both the watchdog timer timeout and the watchdog timer reset. The timeout period can be programmed in a range of 2^{15} to 2^{24} system clock cycles. An interrupt is generated when the timeout period expires if the interrupt is enabled. All watchdog timer resets follow the programmed interrupt timeouts by 512 system clock cycles. If the watchdog timer is not restarted for another full interval in this time period, a system reset occurs when the reset timeout expires. See Table 1

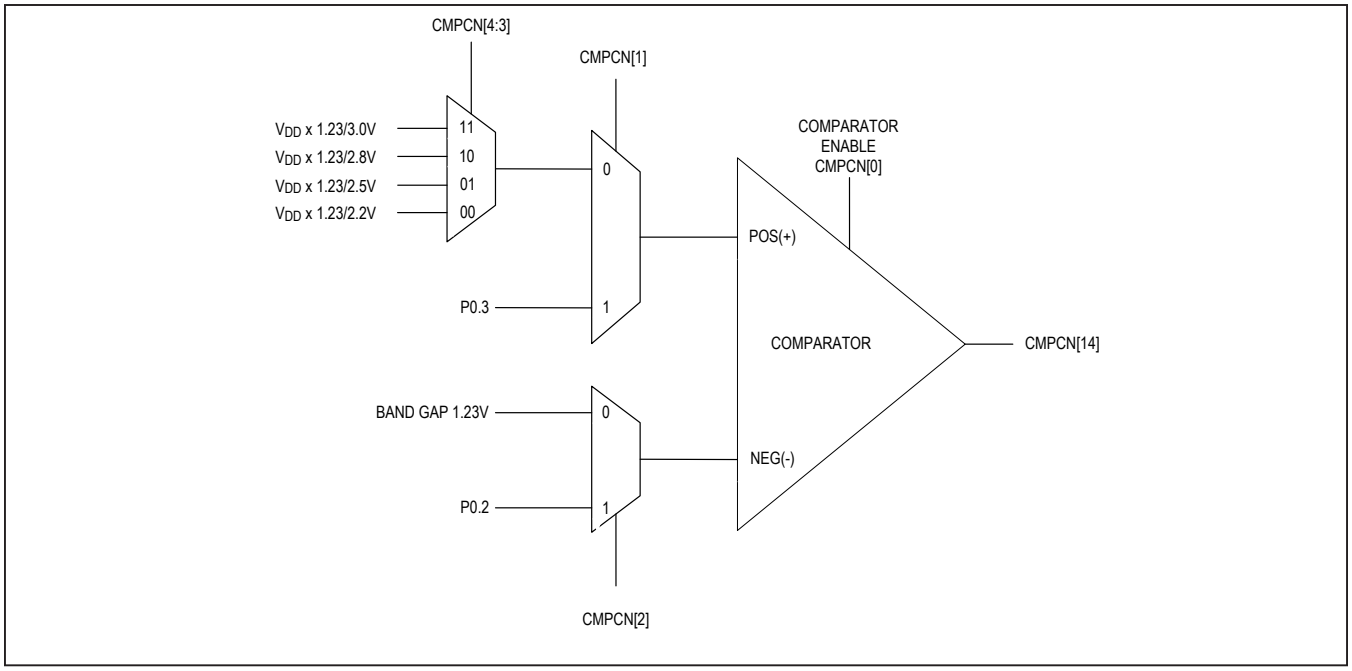


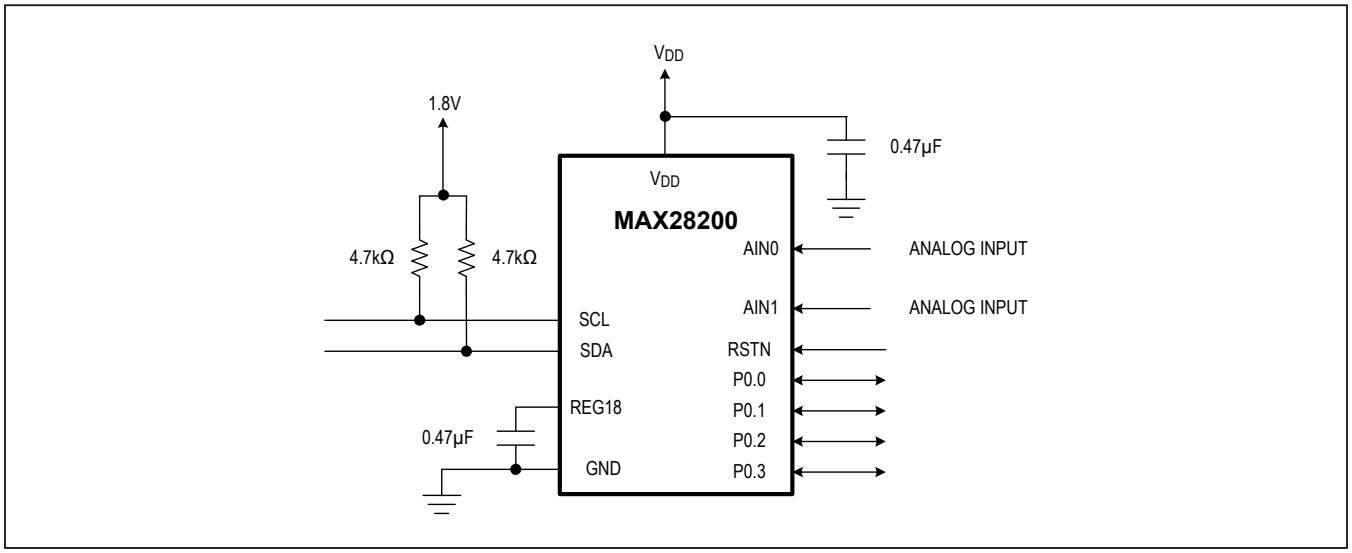
Figure 3. Comparator Configuration

Table 1. Watchdog Timer Settings

WD (CD = 00)	PERIOD	INTERRUPT (F_{CK} = 12MHZ)	RESET (F_{CK} = 12MHZ)
00	$2^{15}/f_{CK}$	2.7ms	2.7ms + 42.7µs
01	$2^{18}/f_{CK}$	21.9ms	21.9ms + 42.7µs
10	$2^{21}/f_{CK}$	174.7ms	174.7ms + 42.7µs
11	$2^{24}/f_{CK}$	1.4s	1.4s + 42.7µs

Typical Application Circuits

Basic Application



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX28200EWC+T	-40°C to +85°C	12 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/18	Initial release	—

