MAX22190 Octal Industrial Digital Input with Diagnostics

General Description

The MAX22190 is an IEC 61131-2 compliant Industrial Digital Input device. MAX22190 translates eight, 24V current-sinking, industrial inputs to a serialized SPI-compatible output that interfaces with 3V to 5.5V logic. A current setting resistor allows the MAX22190 to be configured for Type 1, Type 2, or Type 3 inputs. Field wiring is verified for proximity switches, by a second threshold detector on each input. When wire-break is enabled, the $\overline{\text{FAULT}}$ output is asserted and a register flag set if the input current drops below the wire-break threshold for more than 20ms. Additional diagnostics that assert $\overline{\text{FAULT}}$ include: over temperature, low 24V field supply, 24V field supply missing, and CRC communication error.

For robust operation in industrial environments, each input includes a programmable glitch filter. The filter delay on each channel can be independently programmed to one of eight values between 50µs and 20ms, including and filter bypass. MAX22190 has a 4-pin SPI interface and in addition uses $\overline{\text{LATCH}}$ input for synchronizing input data across multiple device in parallel.

MAX22190 field-side accepts a single 7V to 65V supply to VDD24 pin. When powered by the field supply, MAX22190 generates a 3.3V output from an integrated LDO regulator, which can provide up to 25mA of current for external loads in addition to powering the MAX22190. Alternatively, MAX22190 can be powered from a 3.0V to 5.5V logic side supply connected to VDD pin. For flexibility, the SPI interface operates at 3.3V or 5V logic levels as controlled by the VL pin.

Applications

- Programmable Logic Controllers
- Industrial Automation
- Process Automation
- Building Automation

Benefits and Features

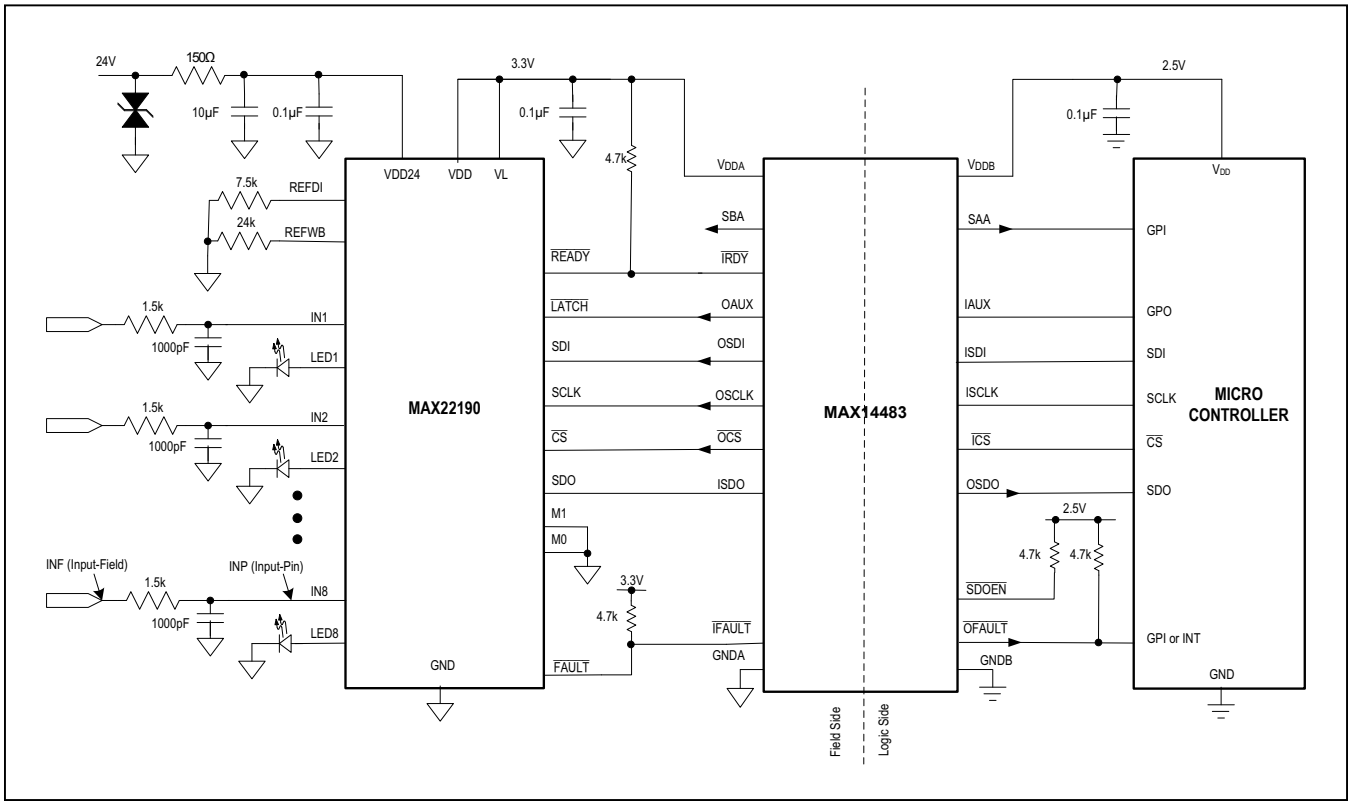
- High Integration Reduces BOM Count and Board Space
  - Eight Input Channels with Serializer
  - Operates Directly From Field Supply (7V to 65V)
  - Compatible with 3.3V or 5V Logic
  - 5mm x 5mm TQFN Package
- Reduced Power and Heat Dissipation
  - Accurate Input-Current Limiters
  - Energyless Field-Side LED Drivers
- Fault Tolerant with Built-In Diagnostics
  - Input Protection to ±40V with Low-Input Leakage Current
  - Wire Break Detection
  - Integrated Field-Supply Voltage Monitors
  - Integrated Overtemperature Monitor
  - 5-Bit CRC Code Generation and Transmission for Error Detection
- Configurability Enables Wide Range of Applications
  - Configurable IEC 61131-2 Type 1, 2, 3 Inputs
  - Configurable Input Current-Limiting from 0.5mA to 3.4mA
  - Selectable Input Debounce Filtering
- Robust Design
  - ±8kV Contact ESD and ±15kV Air Gap ESD Using Minimum 1kΩ Resistor
  - ±1kV Surge Tolerant Using Minimum 1kΩ Resistor
  - -40°C to +125°C Ambient Operating Temperature

Ordering Information ***appears at end of data sheet.***

19-100224; Rev 0; 12/17

maxim integrated™

Isolated Octal Digital Input



Absolute Maximum Ratings

VL, VDD to GND .....-0.3V to +6V
VDD24 to GND.....-0.3V to +70V
SCLK, $\overline{CS}$, SDI, M0, M1 to GND.....-0.3V to +6V
$\overline{LATCH}$, $\overline{FAULT}$, $\overline{READY}$ to GND .....-0.3V to +6V
REFWB, REFDI to GND .....-0.3V to (VDD + 0.3V)
SDO to GND.....-0.3V to (VL + 0.3V)
IN1–IN8 to GND .....-40V to +40V
LED1 – LED8 to GND .....-0.3V to +6V

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate at 27.8mW/°C above +70°C) 2222mW
Operating Temperature Range
Ambient Temperature .....+125°C
Junction Temperature .....+150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θJ_A)
Multilayer Board.....36°C/W

Junction-to-Case Thermal Resistance (θJ_C)
Multilayer Board .....3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

V_L - V_{GND} = +3.0V to +5.5V, V_{DD} - V_{GND} = +3.0V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. C_L = 15pF. Typical values are at V_L - V_{GND} = +3.3V, V_{DD} - V_{GND} = +3.3V, V_{DD24} - V_{GND} = +24V, INx = +24V, and T_A = +25°C. (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Logic Supply Voltage	V_L			3.0		5.5	V
Logic Supply Current	I_{VL}	$\overline{CS}$ = V_L, All logic pins static	V_{VL} – V_{GND} = +5.5V		13	30	µA
Supply Voltage	V_{DD24}	Normal operation		7		65	V
	V_{DD}	Powered from a external supply		3.0		5.5	V
Supply Current of V_{DD24}	I_{DD24}	V_{DD24} = 24V	IN1–IN8 = 0V, LED1–LED8 = GND, SPI static, REFDI = 7.5kΩ, REFWB = 24kΩ.		0.6	1.2	mA
Supply Current Powered From V_{DD}	I_{DD}	V_{DD} = 3.3V	IN1–IN8 = 0V, LED1–LED8 = GND, SPI static, REFDI = 7.5kΩ, REFWB = 24kΩ.		0.6	1.2	mA
V_{DD} Undervoltage-Lockout Threshold	V_{UVLO}	V_{DD} rising		2.4		2.9	V
V_{DD} Undervoltage-Lockout-Threshold Hysteresis	V_{UVHYST}				0.07		V

DC Electrical Characteristics (continued)

V_L - V_{GND} = +3.0V to +5.5V, V_{DD} - V_{GND} = +3.0V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. C_L = 15pF. Typical values are at V_L - V_{GND} = +3.3V, V_{DD} - V_{GND} = +3.3V, V_{DD24} - V_{GND} = +24V, INx = +24V, and T_A = +25°C. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD24} Undervoltage-Lockout Threshold	V_{UVLO24}	V_{DD24} rising	6		6.8	V
V_{DD24} Undervoltage-Lockout-Threshold Hysteresis	$V_{UVHYST24}$			0.5		V
V_L Undervoltage-Lockout Threshold	V_{UVLOVL}	V_L rising	0.9		1.6	V
V_L Undervoltage-Lockout-Threshold Hysteresis	$V_{UVHYSTVL}$			0.07		V
Regulator Output Voltage	V_{DD}	I_{LOAD} = 1mA, V_{DD24} ≥ 7V	3.0	3.3	3.6	V
Line Regulation	$dVDD_{LINE}$	I_{LOAD} = 1mA, V_{DD24} = 12V to 24V		0		mV
Load Regulation	$dVDD_{LOAD}$	I_{LOAD} = 1mA to 10mA, V_{DD24} = 24V		4		mV
Regulator Current Capability	I_{DD_CC}				25	mA
Short-Circuit Current	I_{DD24_SC}	V_{DD24} current when V_{DD} shorted to GND	28		50	mA
$\overline{READY}$ Threshold	V_{READY}	V_{DD} rising, V_{DD24} = 0V	2.4		2.9	V
$\overline{READY}$ Threshold Hysteresis	V_{READY_HYST}			0.07		V
$\overline{READY}$ Delay	$\overline{READY}_{DELAY}$	V_{DD} valid to $\overline{READY}$ low		1		ms
SUPPLY ALARMS						
V_{DD24} UV Alarm On/Off	$V_{ALRMOFFUV}$	Rising V_{DD24}, under voltage			17	V
V_{DD24} UV Alarm Off/On	$V_{ALRMONUV}$	Falling V_{DD24}, under voltage	15			V
Glitch Filter for V_{DD24} UV				3		µs
V_{DD24} VM Alarm On/Off	$V_{ALRMOFFVM}$	Rising V_{DD24}, missing voltage			13.9	V
V_{DD24} VM Alarm Off/On	$V_{ALRMONVM}$	Falling V_{DD24}, missing voltage	12.1			V
Glitch Filter for V_{DD24} VM				3		µs
TEMPERATURE ALARMS						
Overtemperature Alarm 1	T_{ALRM1}	ALRMT1 bit set in FAULT register		115		°C
Overtemperature Alarm 2	T_{ALRM2}	ALRMT2 bit set in FAULT register		140		°C
Overtemperature Alarm Hysteresis	T_{ALRM_HYS}			10		°C
Thermal-Shutdown Threshold	T_{SHDN}	OTSHDN bit set in FAULT2 register		165		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			10		°C
WIRE BREAK ALARMS						
REF Wire Break Voltage	V_{REFWB}	R_{REFWB} = 5.2kΩ to 50kΩ		0.61		V

DC Electrical Characteristics (continued)

V_L - V_{GND} = +3.0V to +5.5V, V_{DD} - V_{GND} = +3.0V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. C_L = 15pF. Typical values are at V_L - V_{GND} = +3.3V, V_{DD} - V_{GND} = +3.3V, V_{DD24} - V_{GND} = +24V, INx = +24V, and T_A = +25°C. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Wire Break Current Range	I_{WB}	R_{REFWB} = 5.2kΩ		470		µA
		R_{REFWB} = 50kΩ		48.8		µA
PCB FAULT ALARMS						
REFWB Pin Short	RWBS	RFWBS bit set in FAULT2 Register		550		µA
REFWB Pin Open	RWBO	RFWBO bit set in FAULT2 Register		6.6		µA
REFDI Pin Short Alarm	REFDIS	RFDIS bit set in FAULT2 Register		550		µA
REFDI Pin Open	REFDIO	RFDIO bit set in FAULT2 Register		6.6		µA
IC INPUTS (TYPES 1, 2, 3)						
Input Threshold Low-to-High	V_{THP+}	IN1 – IN8			6	V
Input Threshold High-to-Low	V_{THP-}	IN1 – IN8	4.4			V
Input Threshold Hysteresis	$V_{INPHYST}$	IN1 – IN8		0.8		V
LED On-State Current	I_{LEDON}	R_{REFDI} = 7.5kΩ, V_{LED} = 3V	1.5			mA
DI Leakage, Current Sources Disabled	I_{DI_LEAK}	IN1 – IN8 = 36V		73		µA
		IN1 – IN8 = 24V		42		µA
FIELD INPUTS						
Current-Limit Setting	I_{CLIM}	R_{REFDI} = 5.2kΩ		3.39		mA
		R_{REFDI} = 36kΩ		0.48		
REFDI Pin Voltage	V_{REFDI}	R_{REFDI} = from 5.2kΩ to 36kΩ		0.61		V
TYPE 1,3: External Series Resistor R = 1.5K, R_{REFDI} = 7.5K, WB detect off, unless otherwise noted						
Input Current Limit	I_{INLIM}	28V > VINx at the pin > 5V, R_{REFDI} = 7.5kΩ (Note 3)	2.10	2.35	2.60	mA
Field Input Threshold Low-to-High	V_{INF+}	R_{REFDI} = 7.5kΩ, 1.5kΩ external series resistor			9.9	V
Field Input Threshold High-to-Low	V_{INF-}	R_{REFDI} = 7.5kΩ, 1.5kΩ external series resistor	7.4			V
Field Input Threshold Hysteresis	$V_{INFHYST}$	R_{REFDI} = 7.5kΩ, 1.5kΩ external series resistor		0.9		V
TYPE 2: External Series Resistor R = 1K, R_{REFDI} = 5.2K, WB detect Off, unless otherwise noted						
Input Current Limit	I_{INLIM}	28V > VINx at the pin > 5V, R_{REFDI} = 5.2kΩ (Note 3)	3.05	3.39	3.71	mA
Field Input Threshold Low-to-High	V_{INF+}	R_{REFDI} = 5.2kΩ, 1kΩ external series resistor			9.9	V
Field Input Threshold High-to-Low	V_{INF-}	R_{REFDI} = 5.2kΩ, 1kΩ external series resistor	7.4			V
Field Input Threshold Hysteresis	$V_{INFHYST}$	R_{REFDI} = 5.2kΩ, 1kΩ external series resistor		0.9		V

DC Electrical Characteristics (continued)

V_L - V_{GND} = +3.0V to +5.5V, V_{DD} - V_{GND} = +3.0V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. C_L = 15pF. Typical values are at V_L - V_{GND} = +3.3V, V_{DD} - V_{GND} = +3.3V, V_{DD24} - V_{GND} = +24V, INx = +24V, and T_A = +25°C. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Filter Delay (See bits DELAY[2:0] in FLTx Register)	t_{BOUNCE}	FBP = 1: bypass filtering		2		µs
		FBP = 0, DELAY = 0		0.05		ms
		FBP = 0, DELAY = 1		0.1		
		FBP = 0, DELAY = 2		0.4		
		FBP = 0, DELAY = 3		0.8		
		FBP = 0, DELAY = 4		1.6		
		FBP = 0, DELAY = 5		3.2		
		FBP = 0, DELAY = 6		12.8		
		FBP = 0, DELAY = 7		20		
Wire Break Filter Delay	t_{WBD}			20		ms
DYNAMIC CHARACTERISTICS						
Field-Input Sampling Rate	f_{IN}	Input Filter Bypass mode		1000		kHz
		Input Filter Not Bypass mode		200		
Minimum Detectable Field Input Pulse Width	t_{PW}	No external capacitors on pins IN1-IN8 (Note 3)		3		µs
$\overline{LATCH}$ Delay		Assertion of $\overline{LATCH}$ or $\overline{CS}$ until input data is frozen		50		ns
$\overline{FAULT}$ Minimum Pulse Width	$t_{\overline{FAULT}\_PW}$	$\overline{FAULT}$ low, pullup 4mA	0.8			µs
INTERFACE LOGIC						
Input Logic-High Voltage	V_{IH}	SCLK, $\overline{CS}$, SDI, $\overline{LATCH}$, M0, M1 relative to GND	0.7 x VL			V
Input Logic-Low Voltage	V_{IL}	SCLK, $\overline{CS}$, SDI, $\overline{LATCH}$, M0, M1 relative to GND			0.3 x VL	V
Output Logic-High Voltage	V_{OH}	SDO, sourcing 4mA	VL - 0.4			V
Output Logic-Low Voltage	V_{OL}	SDO, $\overline{FAULT}$ sinking 4mA			0.4	V
Input Pullup Resistance $\overline{CS}$, $\overline{LATCH}$	R_{PU}			195		KΩ
Input Pulldown Resistance SCLK, SDI, M1, M0	R_{PD}			195		

AC Electrical Characteristics

V_L - V_{GND} = +3.0V to +5.5V, V_{DD} - V_{GND} = +3.0V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. C_L = 15pF. Typical values are at V_L - V_{GND} = +3.3V, V_{DD} - V_{GND} = +3.3V, V_{DD24} - V_{GND} = +24V, INx = +24V, and T_A = +25°C. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI CHARACTERISTICS						
SCLK Pulse Width-High	t_{SCLKH}	See Figure 1	20			ns
SCLK Pulse Width-Low	t_{SCLKL}	See Figure 1	20			ns
SCLK Clock Period	t_{SCLK}	See Figure 1	100			ns
SCLK Clock Frequency	f_{SCLK}				10	MHz
$\overline{CS}$ Pulse Width	t_{CSBPW}	See Figure 1	20			ns
SDI-to-SCLK Setup Time	t_{DINSU}	See Figure 1	5			ns
SDI-to-SCLK Hold Time	t_{DINH}	See Figure 1	15			ns
$\overline{CS}$-Fall-to-SCLK Rise Time	t_{CLK_SU}	See Figure 1	80			ns
SCLK-Rise-to-$\overline{CS}$ Rise Time	t_{CSBH}	Rising edge of SCLK to rising edge of $\overline{CS}$ (Figure 1)	40			ns
SDO Enable Time	$t_{CSB\_SDOVALID}$	$\overline{CS}$ Falling to SDO Valid (Figure 1)			50	ns
SDO Disable Time	t_{CSB_SDOTRI}	$\overline{CS}$ Rising to SDO Tristate (Figure 1)			50	ns
Output Data Propagation Delay	t_{DO}	SCLK Falling Edge-to-SDO Valid (Figure 1)			50	ns
Rise/Fall Time SDO	$t_{R/F}$	SDO 10% to 90% rising, 90% to 10% falling		4		ns

Note 2: All units are production tested at T_A = 25°C. Specifications over temperature are guaranteed by design.
Note 3: External resistor R_{REFDI} is selected to set any desired current limit between 0.5mA and 3.4mA.

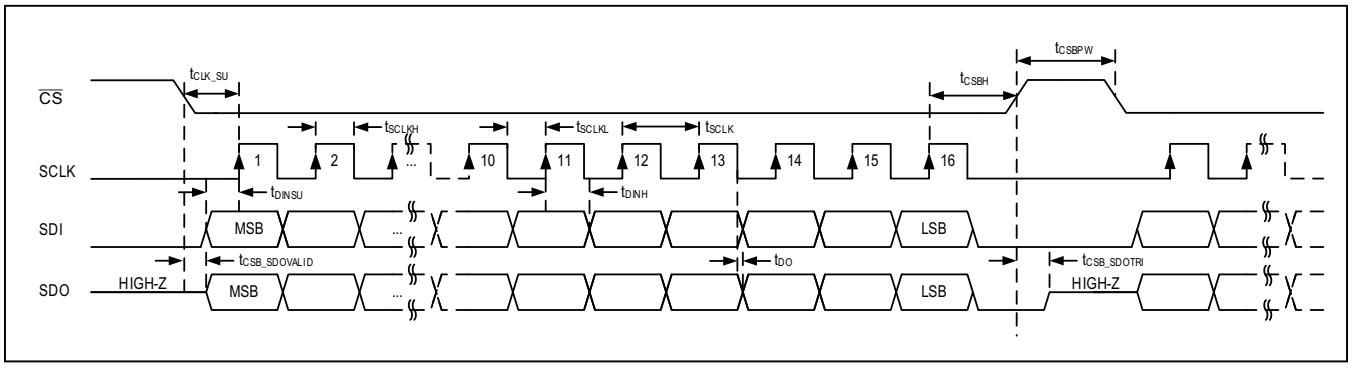


Figure 1. SPI Timing Diagram

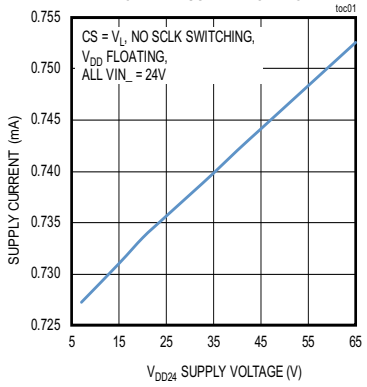
ESD and EMC Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Surge	Line-to-Line	IEC 61000-4-5, 1.2/50µs pulse, 1kΩ resistor in series with IN_ pin	±2	kV
	Line-to-Ground	IEC 61000-4-5, 1.2/50µs pulse, 1kΩ resistor in series with IN_ pin	±1	
ESD	Human Body Model	All pins	±2	
	Contact	Minimum 1kΩ resistor in series with IN1- IN8, with respect to GND	±8	
	Air Gap	Minimum 1kΩ resistor in series with IN1 - IN8, with respect to GND	±15	

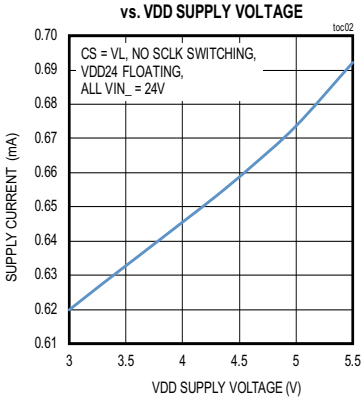
Typical Operating Characteristics

V_{DD24} = 24V, V_{DD} = V_L = 3.3V, T_A = +25°C, R_{REFDI} = 7.5kΩ, R_{REFWB} = 24kΩ, R_{IN} = 1kΩ, unless otherwise noted.

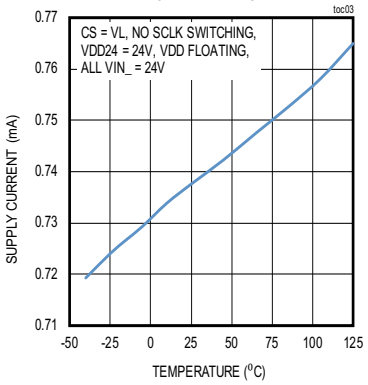
VDD24 SUPPLY CURRENT vs. VDD24 SUPPLY VOLTAGE



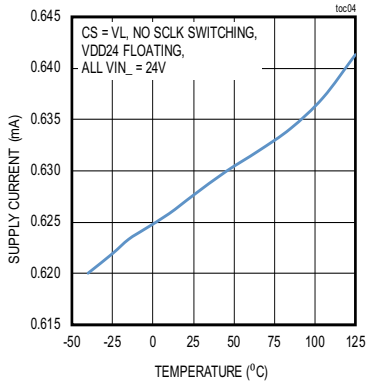
VDD SUPPLY CURRENT vs. VDD SUPPLY VOLTAGE



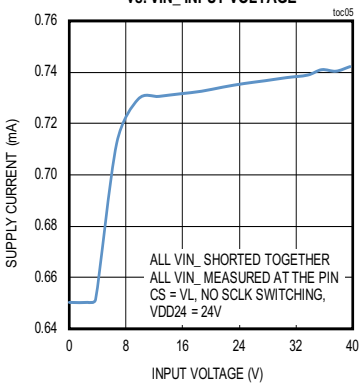
VDD24 SUPPLY CURRENT vs. TEMPERATURE



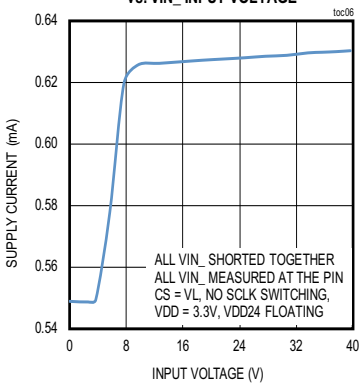
VDD SUPPLY CURRENT vs. TEMPERATURE



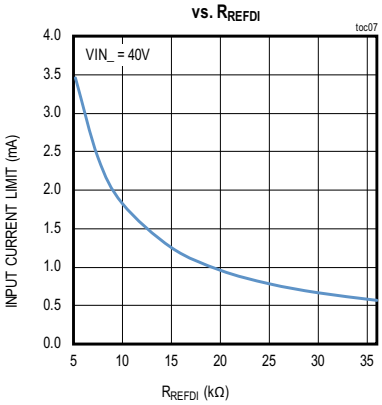
VDD24 SUPPLY CURRENT vs. VIN_ INPUT VOLTAGE



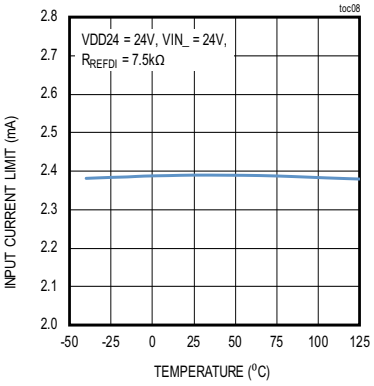
VDD SUPPLY CURRENT vs. VIN_ INPUT VOLTAGE



INPUT CURRENT LIMIT I_{INLIM} vs. R_{REFDI}



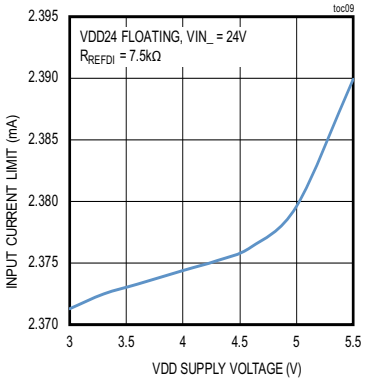
INPUT CURRENT LIMIT I_{INLIM} vs. TEMPERATURE



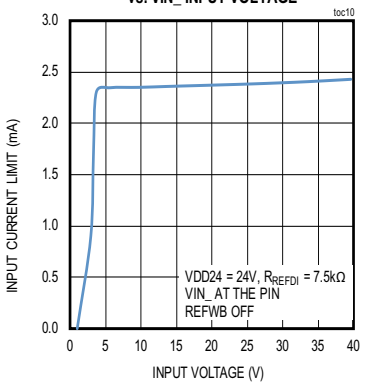
Typical Operating Characteristics (continued)

V_{DD24} = 24V, V_{DD} = V_L = 3.3V, T_A = +25°C, R_{REFDI} = 7.5kΩ, R_{REFWB} = 24kΩ, R_{IN} = 1kΩ, unless otherwise noted.

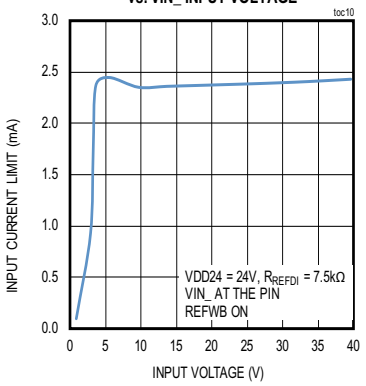
INPUT CURRENT LIMIT I_{INLIM} vs. VDD SUPPLY VOLTAGE



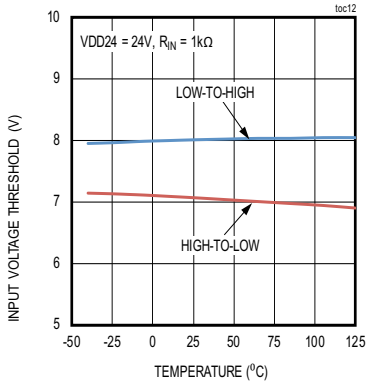
INPUT CURRENT LIMIT I_{INLIM} vs. VIN_ INPUT VOLTAGE



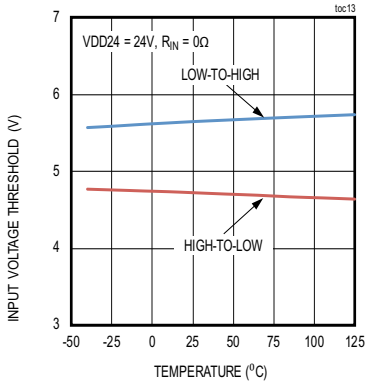
INPUT CURRENT LIMIT I_{INLIM} vs. VIN_ INPUT VOLTAGE



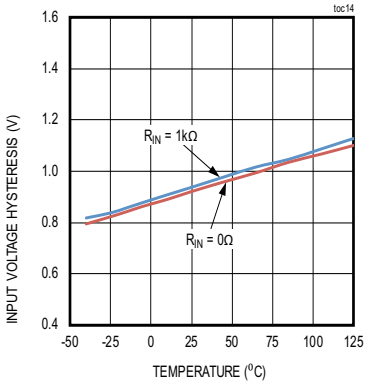
INPUT VOLTAGE THRESHOLD vs. TEMPERATURE



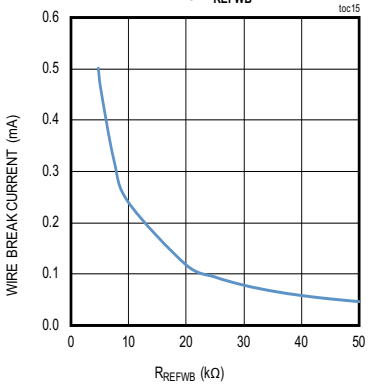
INPUT VOLTAGE THRESHOLD vs. TEMPERATURE



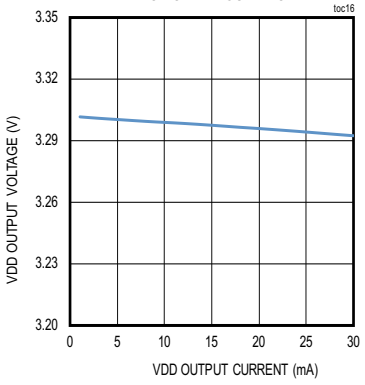
INPUT VOLTAGE HYSTERESIS vs. TEMPERATURE



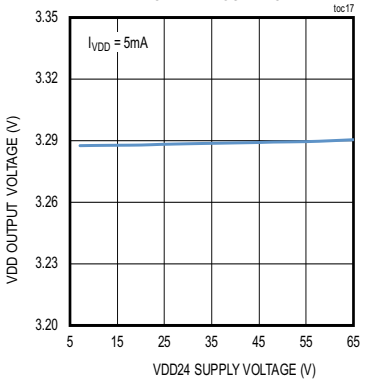
WIRE BREAK CURRENT THRESHOLD vs. R_{REFWB}



LDO LOAD REGULATION



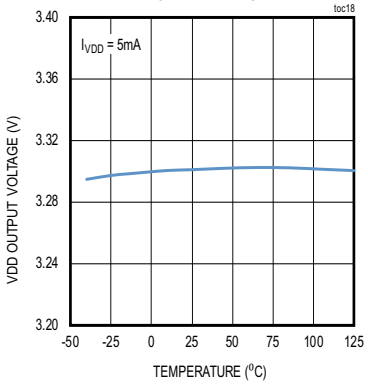
LDO LINE REGULATION



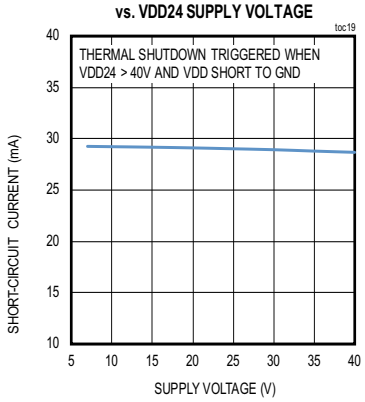
Typical Operating Characteristics (continued)

V_{DD24} = 24V, V_{DD} = V_L = 3.3V, T_A = +25°C, R_{REFDI} = 7.5kΩ, R_{REFWB} = 24kΩ, R_{IN} = 1kΩ, unless otherwise noted.

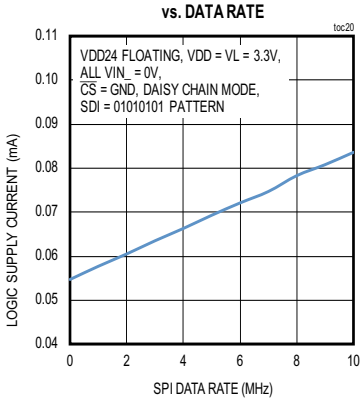
LDO OUTPUT VOLTAGE vs. TEMPERATURE



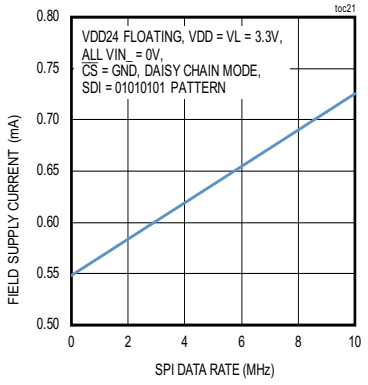
LDO SHORT-CIRCUIT CURRENT vs. VDD24 SUPPLY VOLTAGE



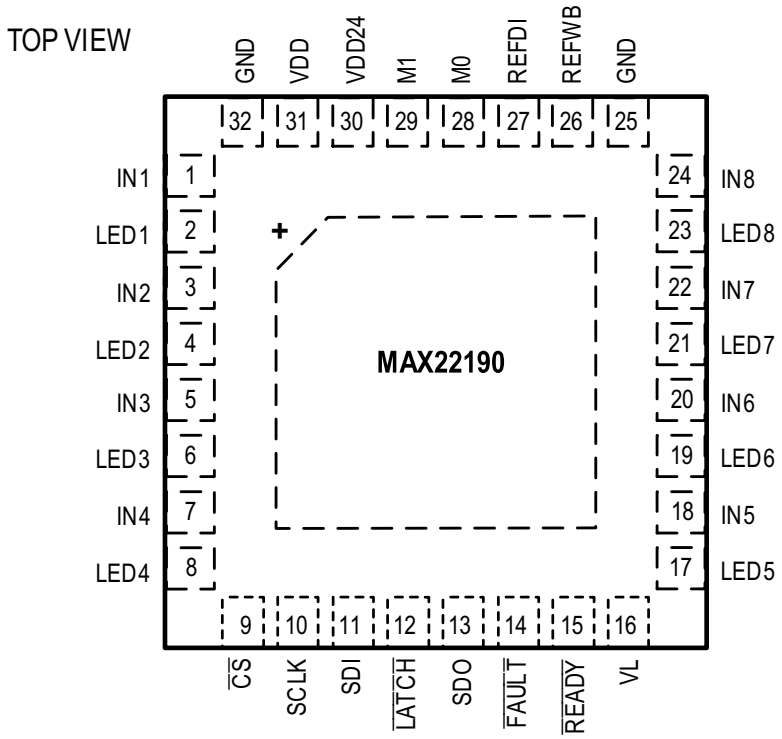
LOGIC SUPPLY CURRENT vs. DATA RATE



VDD SUPPLY CURRENT vs. DATA RATE



Pin Configurations

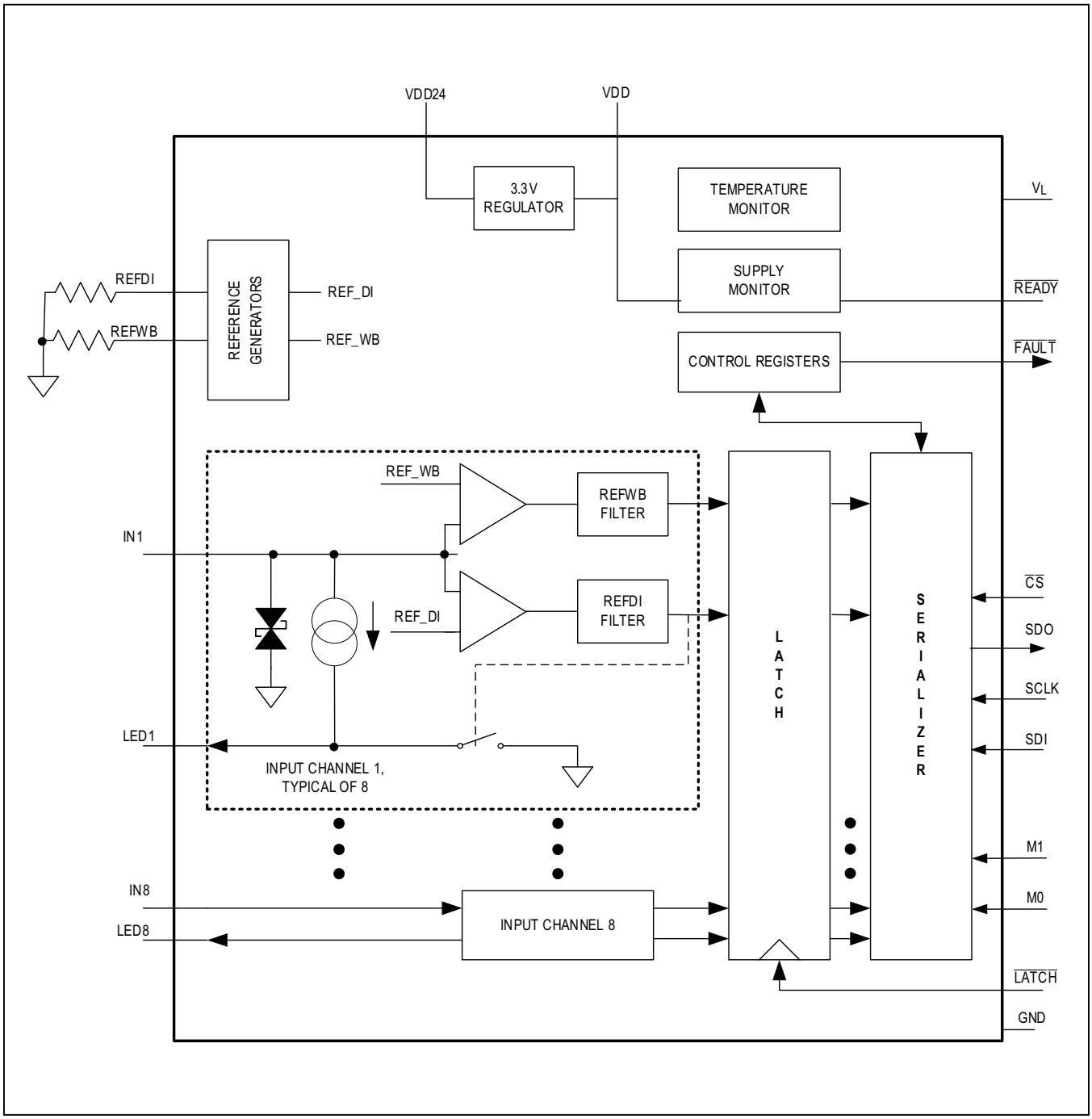


TQFN
5mm x 5mm

Pin Description

PIN	NAME	FUNCTION
SPI INTERFACE		
16	VL	Logic Interface Supply, 3.0V to 5.5V.
10	SCLK	Serial Clock Input.
9	$\overline{CS}$	Chip-Select Input. Assert low to latch input states and enable the SPI interface.
13	SDO	Serial Data Output. Data is updated on the falling edge of SCLK. When $\overline{CS}$ is high SDO is high-Z.
11	SDI	Serial Data Input. Data is clocked into SDI on the rising edge of SCLK.
14	$\overline{FAULT}$	Active-Low Fault Indicator. Open drain output, $\overline{FAULT}$ goes low to indicate that one or more of the flags in the FAULT register have been set. The faults are: Supply Monitor, Temperature Monitor, CRC error, wire-break error, short or open at REFDI or REFWB pins.
12	$\overline{LATCH}$	$\overline{LATCH}$ and $\overline{CS}$ control the data latch at the input of the serializer (after the inputs). The latch is transparent when both $\overline{CS}$ and $\overline{LATCH}$ are high. The data at the input of the serializer is frozen on the falling edge of either $\overline{LATCH}$ or $\overline{CS}$. $\overline{LATCH}$ is typically used to synchronize input timing across multiple MAX22190s.
28	M0	SPI Control Mode. See Table 1 for details.
29	M1	
15	$\overline{READY}$	Open-drain output, $\overline{READY}$ goes low indicating that MAX22190 is powered and ready for operation.
FIELD INPUT PINS		
25,32	GND	Ground return for all data inputs and the field power supply
30	VDD24	24V field supply. Bypass to GND with 0.1µF capacitor in parallel with 1µF capacitor
31	VDD	3.3V Output from integrated LDO when powered from VDD24, or 3.0 - 5.5V Supply Input when VDD24 not driven. Bypass to GND with 0.1µF capacitor in parallel with 1µF capacitor. If powering MAX22190 from an external supply, leave VDD24 floating.
1, 3, 5, 7, 18, 20, 22, 24	IN1 – IN8, respectively	Field inputs. For type 1 and type 3 inputs, place a 1.5kΩ MELF resistor between the field input and INx.
2, 4, 6, 8, 17, 19, 21, 23	LED1 – LED8, respectively	Energyless LED Driver Outputs. Connect to GND if LEDs are not used.
26	REFWB	Wire Break Current-Limit Reference Resistor. Connect a resistor from REFWB to GND to set Wire Break threshold.
27	REFDI	Digital Input Current-Limit Reference Resistor. For 24V Type 1 and Type 3 inputs, place a 7.5kΩ resistor from REFDI to GND.
EP	—	Exposed Pad. Connect to GND. Solder entire exposed pad area (EP = exposed pad on back of package) to ground plane for best thermal performance.

Functional/Block Diagram

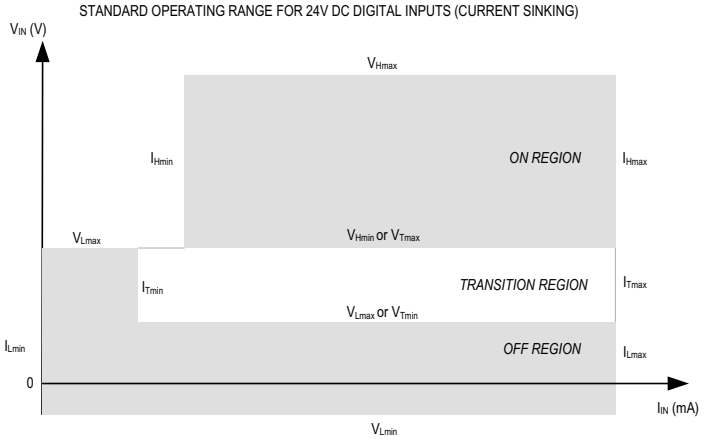


Detailed Description

The MAX22190 senses the state (on, high or off, low) of eight digital inputs. The voltages at the IN1–IN8 input pins are compared against internal references to determine whether the sensor is ON (logic 1) or OFF (logic 0). All eight inputs are simultaneously latched by the assertion of either $\overline{LATCH}$ or $\overline{CS}$, and the data made available in a serialized format via the SPI interface. Placing a 7.5k current-setting resistor between REFDI and GND, and a 1.5k resistor between each field input and the corresponding INx input pin ensures that the current at the ON and OFF trip points as well as the voltage at the trip points satisfy the requirements of IEC 61131-2 for Type 1 and Type 3 inputs. The current sunk by each input pin rises linearly with input voltage until the level set by the current limiter is reached; any voltage increase beyond this point does not increase the input current. Limiting the input current ensures compliance with IEC 61131-2 while significantly reducing power dissipation compared to traditional resistive inputs.

The current-setting resistor R_{REFDI} can be calculated using this equation:

$$R_{REFDI} = 17.63V / I_{INLIM}$$



Type of Limit	Type 1 Limits						Type 2 Limits						Type 3 Limits					
	Off Region		Transition		On Region		Off Region		Transition		On Region		Off Region		Transition		On Region	
	VL (V)	IL (mA)	VT (V)	IT (mA)	VH (V)	IH (mA)	VL (V)	IL (mA)	VT (V)	IT (mA)	VH (V)	IH (mA)	VL (V)	IL (mA)	VT (V)	IT (mA)	VH (V)	IH (mA)
Max	15/5	15	15	15	30	15	11/5	30	11	30	30	30	11/5	15	11	15	30	15
Min	-3	ND	5	0.5	15	2	-3	ND	5	2	11	6	-3	ND	5	1.5	11	2

ND = NOT DEFINED

Figure 2. Switching Characteristics for IEC61131-2 Type 1, 2, and 3 24VDC Digital Inputs

Input Filters

Each input (IN1 - IN8) has a programmable filter and input data may be filtered to reduce noise, or it may be read directly for more rapid response. Bit FBP in the corresponding FLTx register is used to bypass the filter or to enable the filter. One of eight filter delays (50µs, 100µs, 400µs, 800µs, 1.6ms, 3.2ms, 12.8ms, 20ms) may be independently selected for each channel. Noise rejection is accomplished through a no-rollover up-down counter where the state of the field input controls the counting direction (up or down), The filter uses an up-down counter fed by a 200kHz clock. If the input is high, it counts up; if the input is low, it counts down. The filter output is updated when the counter hits the upper or lower limit, with the upper limit depending on the selected filter delay and the lower limit being zero regardless of the filter delay. The low-to-high transition of the filter occurs when the counter reaches the upper limit. The high-to-low transition occurs when the counter reaches the lower limit. There is no rollover; counting simply stops when the upper or lower limit is hit. The filter delay is the time it takes to reach the upper/lower limit in response to a step input when the counter starts from the lower/upper limit. If the input is not a step function, but is bouncing, as shown in Figure 3, the output changes state after a total delay of:

(Total Delay) = (Filter Delay) + 2* (Total Time at the Old State)

In the example in Figure 3, the filter has a nominal delay of 1.6ms, and the input returns high for two 0.2ms periods

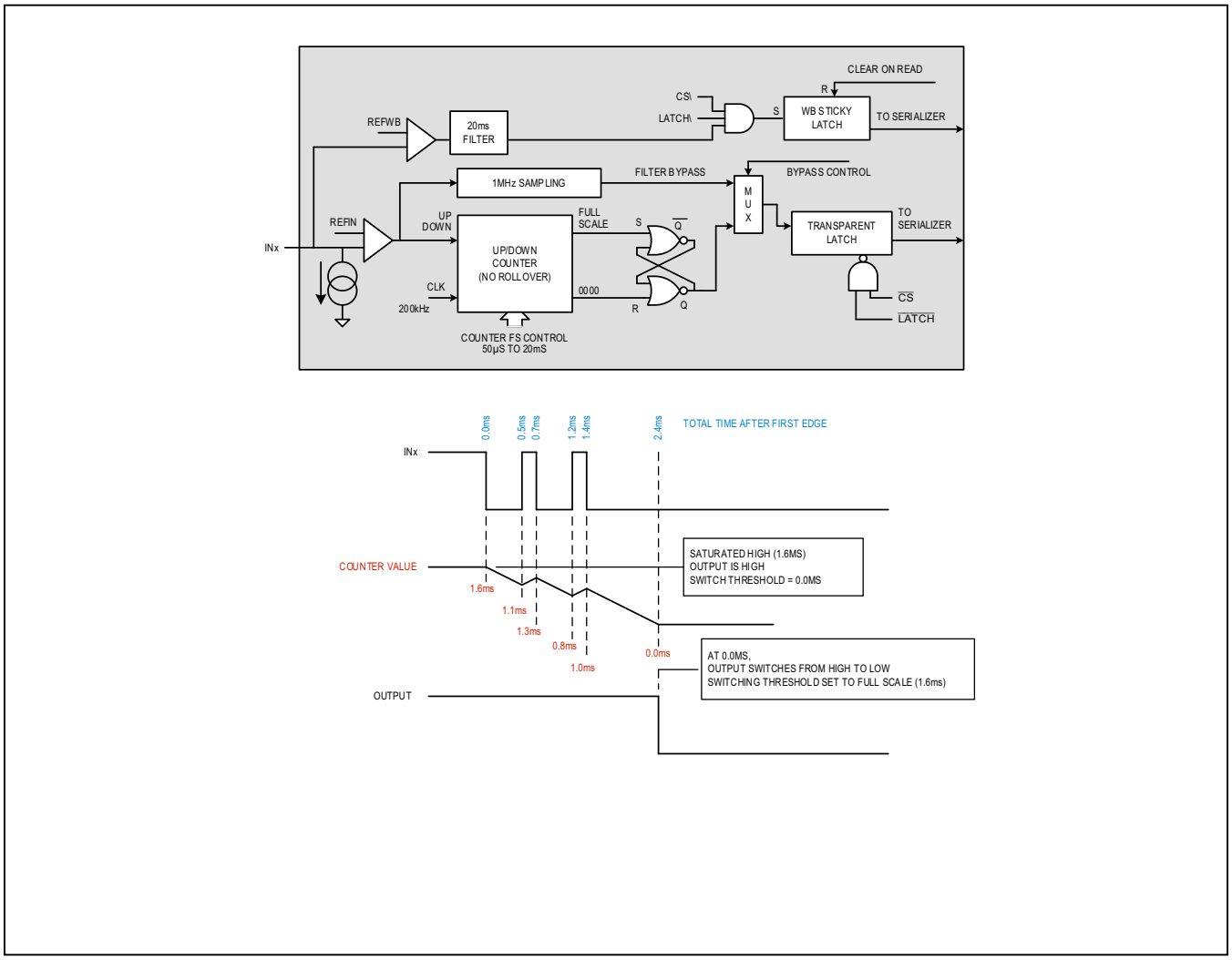


Figure 3. MAX22190 Digital Filter

after the first transition from high to low. These transitions back to the high state extend the time before the output of the filter switches. Total Delay = 1.6ms + 2* (0.2ms + 0.2ms) = 2.4ms.

Wire Break Detection

Each input (IN1 – IN8) includes a second threshold comparator that can be individually enabled to verify the integrity of field wiring. The comparator senses the presence of the small input current produced by a two wire proximity sensor in its open state, or the current from an open switch with a diagnostic resistor placed across it. The wire-break current threshold is set by placing a resistor between REFWB and GND, and is adjustable from 50µA to 470µA. If this current is missing, due to an open wire or a wire shorted to GND, the comparator trips, and after filtering, sets a corresponding sticky bit in the WB register. Bits in this register remain set until the register is read, which automatically clears all bits in the register. All wire-break detectors include a fixed 20ms filter, and like the input data, the input to the WB latch is frozen when either $\overline{CS}$ or $\overline{LATCH}$ is held low. The eight wire break flags are ORed together to produce the WBG flag in the FAULT register. This flag remains set until all flags in the WB register have been cleared.

The wire-break threshold resistor R_{REFWB} can be calculated using this equation:

$$R_{REFWB} = 2.44V / I_{WB}$$

Energyless LED Drivers

When INx is determined to be on, its input current is diverted to the LEDx pin and flows from that pin to GND. Placing an LED between LEDx and GND provides an indication of the input state without increasing overall power dissipation. If the indicator LEDs are not used, connect LEDx to GND.

Fault Detection and Monitoring

$\overline{FAULT}$ is an open-drain output that can be wire ORed with the other open-drain outputs and used to notify the host processor of a fault. When enabled, $\overline{FAULT}$ goes low to indicate that one or more of the flags in the FAULT1 register have been set. These faults are: VDD24 low voltage alarm (24VL), VDD24 voltage missing alarm (24VM), over temperature alarm 1 (ALRMT1), over temperature alarm 2 (ALRMT2), CRC error detected on the previous SPI frame (CRC), Power On Reset event (POR), wire-break group error detected (WBG), and source from FAULT2 register. Enable bits in the FAULT1 and FAULT2 registers select which flags in the FAULT1 and FAULT2 registers will assert the $\overline{FAULT}$ pin. The enable bits do not affect the flags in the FAULT1 register, they only affect the $\overline{FAULT}$ pin. Flags ALRMT1, ALRMT2, 24VL, and 24VM in the FAULT register are latched; they remain set until read even if the fault goes away. WBG is equivalent to the ORed output of the individual wire-break flags WB[7:0] which are latched until cleared by reading the WB register. CRC is not latched, but remains set until an uncorrupted SPI frame is received. The STK bit in the GPO register configures the $\overline{FAULT}$ pin to be sticky or to clear when the fault is removed. For example: if a low voltage condition on VDD24 is detected, the 24VL bit in the FAULT1 register will be set and $\overline{FAULT}$ will assert low provided bit 24VLE in the FAULT1EN register is set. If VDD24 then returns to normal levels, the 24VL bit in the FAULT1 register will remain set until read; however the state of $\overline{FAULT}$ pin depends on configuration bit STK. If STK = 0, the $\overline{FAULT}$ pin is not sticky and will clear when the fault goes away even though the 24VL bit remains set. If STK = 1, then $\overline{FAULT}$ pin reflects the state of the bit in the FAULT1 register and remains set until the bits are cleared by reading the FAULT1 register. The minimum pulse width for $\overline{FAULT}$ pin asserting low is 1µs typical. This ensures adequate time for the assertion of $\overline{FAULT}$

to be recognized by the host even if the fault was present for a shorter time.

The power-on default for the FAULT1EN register is to enable CRC and POR. FAULT pin is in the non-sticky mode.

Clearing Bits in FAULT1 Register

24VL and 24VM sticky (or latched) bits in the FAULT1 register may be read and cleared either through a direct read of the FAULT1 register, or through a SPI mode 0 or mode 2 read or write command if bit 24VF in the CFG register is equal to 0. SPI modes 0 and 2 transactions read and clear bits 24VL, and 24VM (Table 3). This valid SPI transaction will also clear the CRC bit. Note that the CRC bit is only active in modes 0 and 2 since this is the only time a CRC test is performed. The WBG bit in the FAULT1 register is the real-time ORed value of bits WB[7:0] in the WB register and the WBG bit is not cleared by reading the FAULT1 register. Reading the bits in the WB register clears the WB register and for convenience will also clear the WBG bit in the FAULT1 register.

CRC generation

In SPI interface modes 0 and 2, five CRC bits can be used to check data integrity during transfer between the device and an external microcontroller. In applications where the integrity of data transferred is not of concern, the CRC bits can be ignored. The CRC uses the following polynomial:

$$P(x) = x^5 + x^4 + x^2 + x^0$$

The CRC value is calculated using the first 19 data bits and the 5-bit CRC is then appended to the data bits to create the 24bit SPI data frame. When the MAX22190 receives a data frame with a CRC error, the CRC error flag (CRC) in the FAULT1 register is set and, if CRCE is set FAULT pin is asserted. The CRC bit is not sticky, but does remain set until an error-free frame is received. SPI commands within a corrupt frame are ignored.

SPI Interface

MAX22190 has an SPI compatible interface used to read input data, read diagnostic data, and configure all of the registers. Each configuration register can be read back to ensure proper configuration. The interface can be operated in one of four modes as controlled by the strapping inputs M0 and M1. Asserting CS low latches the state of all inputs and enables the SPI interface. For all modes, data at the SDI input is sampled on the rising edge of SCLK and data at SDO is updated on the falling edge of SCLK.

Table 1. SPI Interface Modes

MODE	M1: M0	FRAME LENGTH	CRC	DAISY CHAIN
0	0 0	24-bit	Yes	No
1	0 1	16-bit	No	No
2	1 0	24-bit	Yes	Yes
3	1 1	16-bit	No	Yes

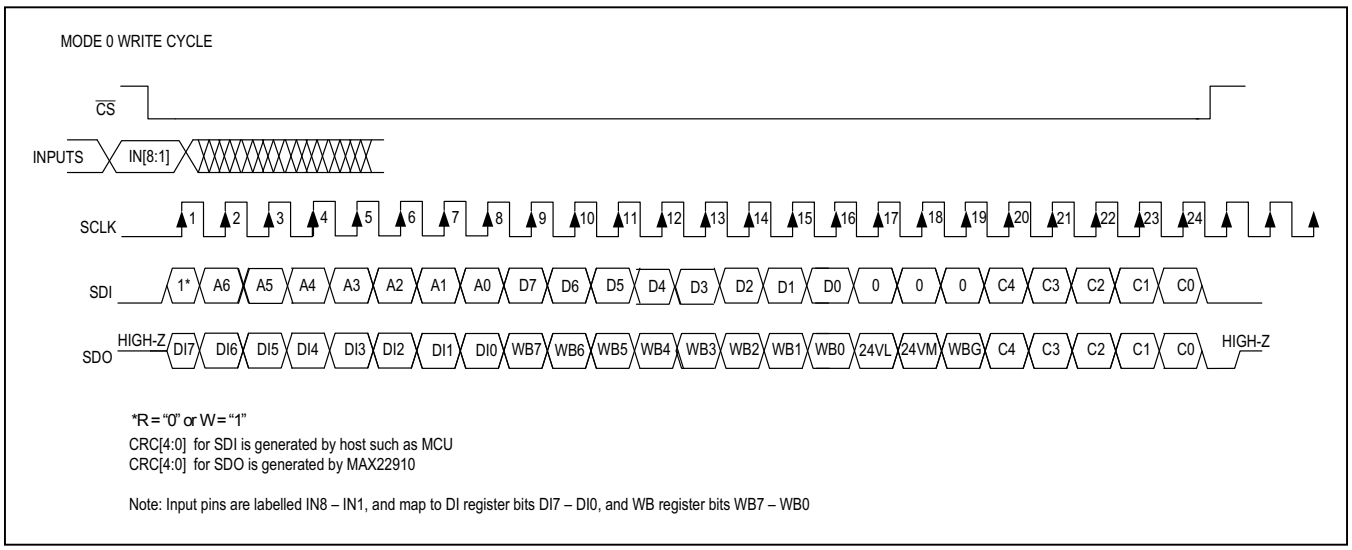


Figure 4. SPI Communication Example

The MSB ($\overline{\text{READ}}$/write bit) is always the first bit of the SPI frame. Transitions of SCLK while $\overline{\text{CS}}$ is deasserted (high) are ignored. SCLK must idle low when $\overline{\text{CS}}$ is asserted.

SPI Protocol

The serial output of the device adheres to the SPI protocol, running with CPHA = 0 and CPOL = 0. In all modes, the first 8-bits clocked out of SDO after $\overline{\text{CS}}$ is asserted are data bits showing the status of inputs IN8 – IN1; this allows for rapid and convenient retrieval of the primary data. For write operations in Modes 0 and 1, the next 8-bits clocked out of SDO are the status bits of the WB (wire-break) register. This is true even if wire-break detection is not enabled, in which case all bits will be 0. For reads in Modes 0 and 1, the second 8 bits will be the data from the specified register.

Modes 2 and 3 are more complex, since the content of the second byte is determined by the previous instruction. For non-daisy-chain compatible modes (Modes 0 and 1), the read instruction is decoded on-the-fly as the SPI frame is clocked in. The instruction is immediately executed and data from the specified register is clocked out in the same SPI frame. This is convenient and quick, but not compatible with daisy-chaining. When daisy-chaining, each unit does not know which portion of the bit stream it should decode until $\overline{\text{CS}}$ is deasserted (the frame is finished). To accommodate this, all daisy-chainable read instruction require two SPI frames. The first frame contains the read instruction and register address, the second frame returns the register data as the second byte of the frame. This is true regardless of the instruction being clocked in during the second frame.

$\overline{\text{LATCH}}$ is used to simultaneously capture the input states of different MAX22190s that are not controlled by the same $\overline{\text{CS}}$. This could be multiple MAX22190s in the same module, or MAX22190s in different modules.

Clock Count for Multiples of 8

For each SPI cycle (between $\overline{\text{CS}}$ going low and going high), the device counts the number of SCLK pulses. If it is not a multiple of 8 the SPI input data is discarded and bit FAULT8CK is set in the FAULT2 register.

SPI Power Status

Only the SPI port buffers are powered from the VL supply; internal SPI circuits are powered from the VDD supply. Both VDD and VL must be valid for SPI communication to take place. In addition to powering the SPI circuits, VDD also sustains the SPI memory (configuration and status registers). If power is being supplied through VDD24, then an auxiliary supply for the memory is also available. The auxiliary supply only sustains memory, it does not allow SPI communication. The auxiliary supply takes over if VDD is lost due to external loading or due to a thermal shutdown event. When the event is over, the device configuration is maintained and fault information is available in the FAULT registers.

Table 2. SPI Port Power Status

VDD24	VDD	VL	SPI REGISTER MAP CONFIGURATION	SPI PORT COMMUNICATION
Valid	Valid	Valid	Configuration and fault data maintained	Normal Operation
Not Valid	Valid	Valid	Configuration and fault data maintained	Normal Operation
Valid	Not Valid	X	Configuration and fault data maintained	$\overline{\text{CS}}$ ignored, SDO is High-Z
X	Valid	Not Valid	Configuration and fault data maintained	$\overline{\text{CS}}$ ignored, SDO is High-Z
Not Valid	Not Valid	X	Configuration and fault data lost	$\overline{\text{CS}}$ ignored, SDO is High-Z

Daisy-Chaining

For systems with more than eight sensor inputs, multiple devices can be daisy-chained to allow access to all data inputs through a single serial port. When using a daisy-chain configuration, connect MOSI to SDI of the first device in the chain. Connect MISO to SDO of the last device in the chain. For all middle links, connect SDI to SDO of the previous device and SDO to SDI of the next device. $\overline{CS}$ and SCLK of all devices in the chain should be connected together in parallel, see Figure 5 which illustrates a 16-input application for daisy chaining and Figure 6 whch shows SPI timing. In a daisy-chain configuration, external components used to enhance EMC robustness do not need to be duplicated for each device of a circuit board.

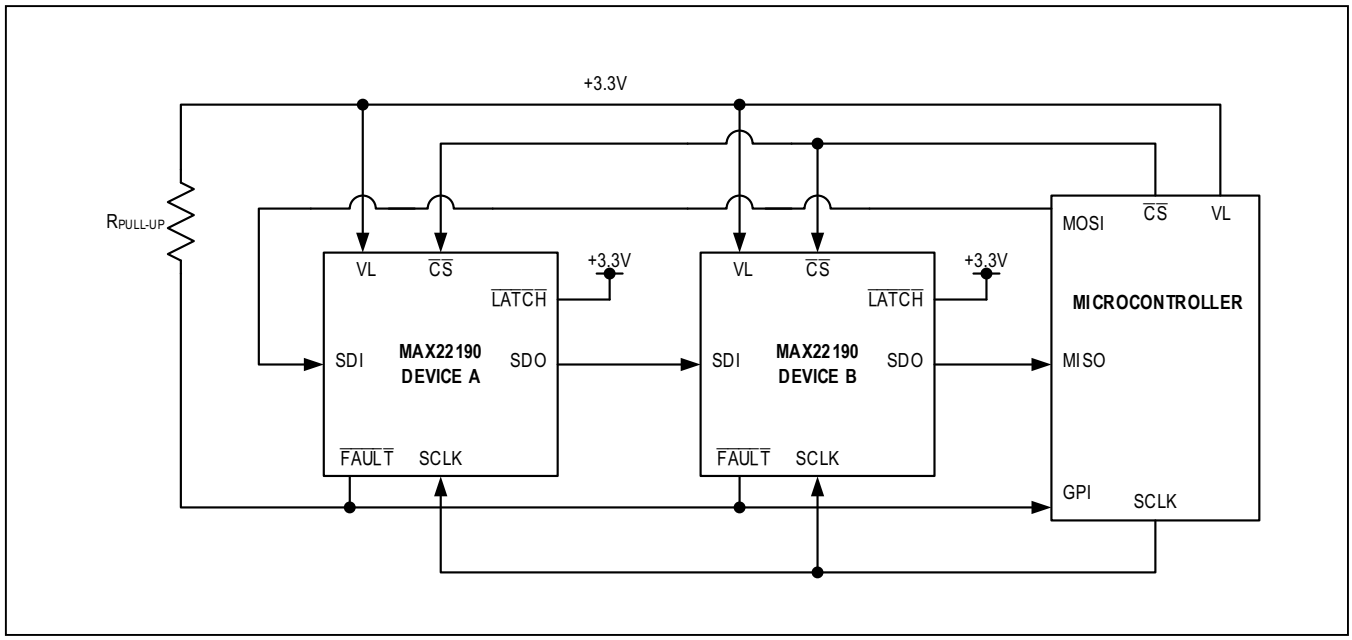


Figure 5. SPI Daisy-Chain Operation

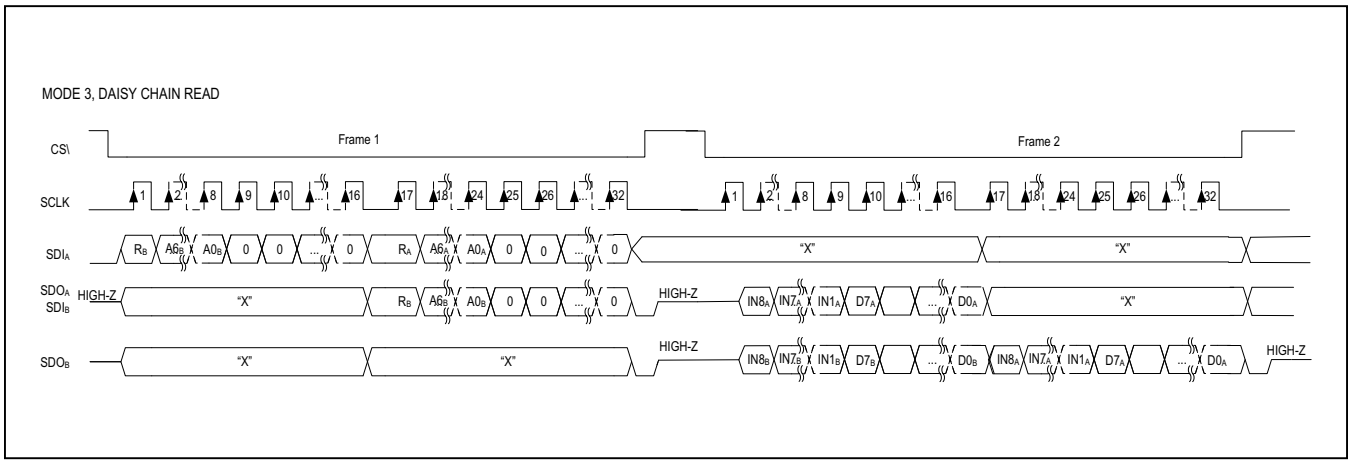


Figure 6. SPI Timing Diagram Daisy-Chain

Configuration Flowchart

The MAX22190 powers on with default register settings and can be used in default mode to read the data inputs, or it can be configured to match the individual application requirements. Before any register access for configuration or reading data, the MCU needs to wait until $\overline{\text{READY}}$ goes low indicating that the MAX22190 is powered up and 'ready' for use. Next, the MCU will need to clear the $\overline{\text{FAULT}}$ pin that asserts low after every power-up event due to the default state (high) of the POR flag.

Default Mode: (Power-up mode) In this mode, the Wire Break (WB) function is disabled, all input channel filters (FLTx) are set to BYPASS, all input channels are enabled, and all fault sources are disabled *except* the CRC and POR flags. Upon power-up, the POR flag will be set to 1. If the $\overline{\text{FAULT}}$ pin is being used, then a write operation must be performed to the FAULT1 register to reset POR to 0 for normal operating conditions. Now the MAX22190 can be polled to read data from DI register to show the logic state of the 8 input channels.

Configurable Mode: MAX22190 can be configured for different parameters based upon the application requirements. The MCU can write to the various registers to set the options for Wire Break, Input Channel Filters, enabling different Fault Sources, or disabling specific Input Channels. In addition, the user can enable features such as detecting a short on pin REFDI and making $\overline{\text{FAULT}}$ pin sticky or not. Once the configuration is complete, the MAX22190 can be polled to read from DI register to show the logic state of the 8 input channels.

FAULT Asserted: MAX22190 uses the open-drain $\overline{\text{FAULT}}$ pin to indicate to the MCU that a Fault has occurred, often by using this pin to trigger an interrupt function within the MCU. The MCU can determine the source of the fault by reading regsiter FAULT1. If bit 5 of FAULT1 is set, then register FAULT2 is indicating a fault and FAULT2 must also be read. Reading the FAULT_ register clears the fault flag, unless the fault condition persists, which would immediately reset the flag.

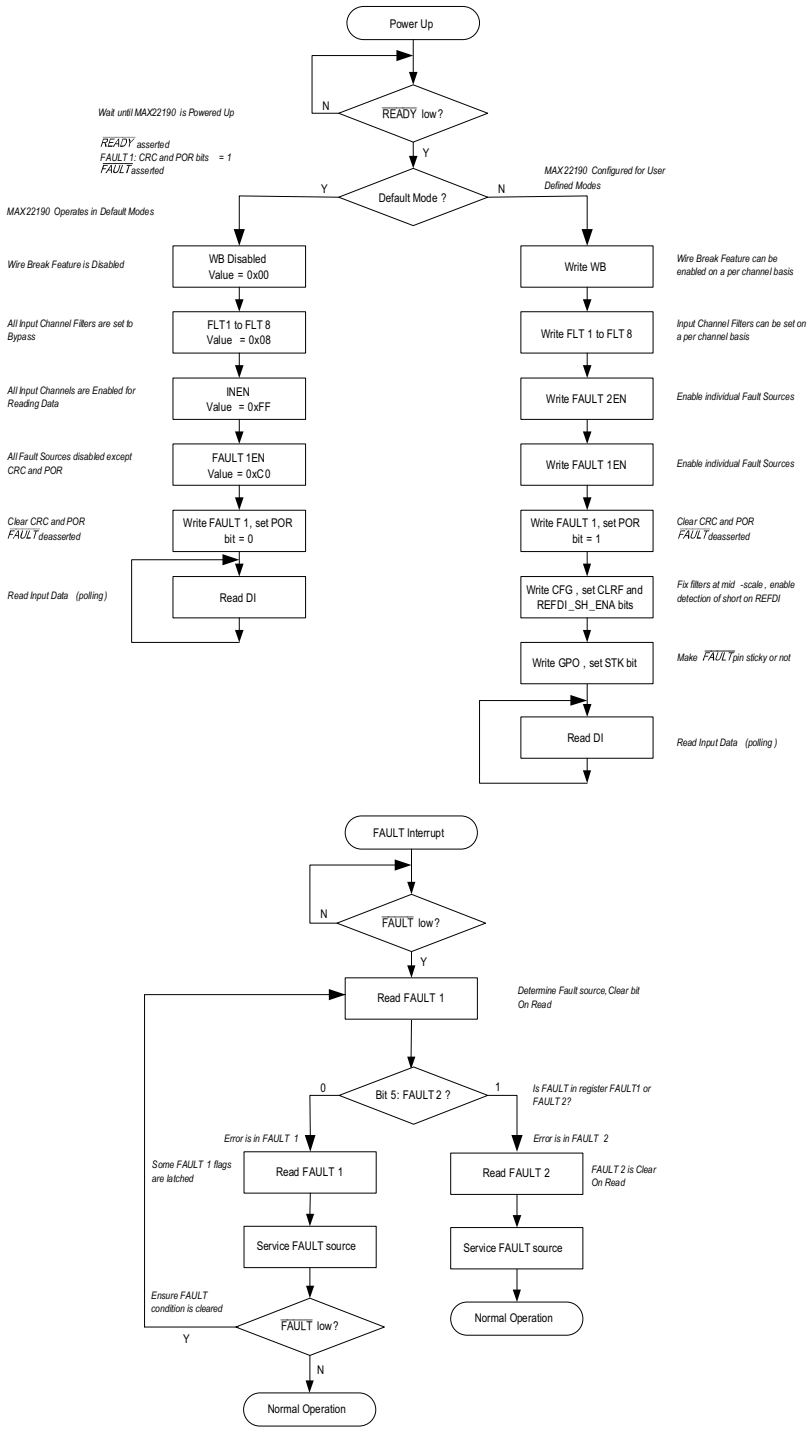


Figure 7. MAX22190 Configuration Flowchart

Table 3. SPI Frames for SPI Modes

Mode 0: M1 = 0, M0 = 0

Write

SDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits	000 Fill Data 3-bits			CRC from Host LSB 5-bits
SDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits	24VL	24VM	WBG	CRC from MAX22190 5-bits

Read

SDI	MSB = 0 1-bit	Register Address 7-bits	00000000 Fill Data 8-bits	000 Fill Data 3-bits			CRC from Host LSB 5-bits
SDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits	24VL	24VM	WBG	CRC from MAX22190 5-bits

Mode 1: M1 = 0, M0 = 1

Write

SDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits
SDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits

Read

SDI	MSB = 0 1-bit	Register Address 7-bits	00000000 Fill Data 8-bits
SDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits

Mode 2: M1 = 1, M0 = 0

Write – Preceding frame was a write or no-op

SDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits	000 Fill Data 3-bits			CRC from Host LSB 5-bits
SDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits	24VL	24VM	WBG	CRC from MAX22190 5-bits

Write – Preceding frame was a read

SDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits	000 Fill Data 3-bits			CRC from Host LSB 5-bits
SDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits	24VL	24VM	WBG	CRC from MAX22190 5-bits

Read – Preceding frame was a write or no-op

SDI	MSB = 0 1-bit	Register Address 7-bits	0000,000 Fill Data 8-bits	000 Fill Data 3-bits			CRC from Host LSB 5-bits
SDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits	24VL	24VM	WBG	CRC from MAX22190 5-bits

Table 3: SPI Frames for SPI Modes (continued)

Read – Preceding frame was a read

SDI	MSB = 0 1-bit	Register Address 7-bits	0000,000 Fill Data 8-bits	000 Fill Data 3-bits			CRC from Host LSB 5-bits
SDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits	24VL	24VM	WBG	CRC from MAX22190 5-bits

Mode 3: M1 = 1, M0 = 1

Write – Preceding frame was a write or no-op

SDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits
SDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits

Write – Preceding frame was a read

SDI	MSB = 1 1-bit	Register Address 7-bits	Write Data 8-bits
SDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits

Read – Preceding frame was a write or no-op

SDI	MSB = 0 1-bit	Register Address 7-bits	0000,000 Fill Data 8-bits
SDO	Input data: IN8 – IN1 8-bits		WB data: WB7 – WB0 8-bits

Read – Preceding frame was a read

SDI	MSB = 0 1-bit	Register Address 7-bits	0000,000 Fill Data 8-bits
SDO	Input data: IN8 – IN1 8-bits		Register Data: D7 – D0 8-bits

Notes:

SDI – CRC generated by external device such as MCU, Data D7 - D0 clocked in from MCU

SDO – CRC generated by MAX22190, Data D7 - D0 clocked out from MAX22190 Register

NO-OP – No Operation, i.e. write cycle with no valid data to specified address

Write Cycle – DI[7:0] and WB[7:0] are from internal latches whose outputs are frozen when $\overline{CS}$ or $\overline{LATCH}$ goes low. Bits 24VL, 24VM and WBG are frozen by $\overline{CS}$ going low but not by $\overline{LATCH}$.

Read Cycle – D7 - D0 are the register data addressed through SDI. Bits 24VL, 24VM, and WBG reflect the corresponding bits in the FAULT register.

Input Channel pins are numbered IN1 – IN8, so input IN1 maps to bit DI0, input IN2 to bit DI1 …. and input IN8 to bit DI7

Table 4. Register Map

REGISTER	ADDRESS	SYMBOL	TYPE	POR (DEFAULT)	7	6	5	4	3	2	1	0
Wire Break	00h	WB	COR	00h	WB7	WB6	WB5	WB4	WB3	WB2	WB1	WB0
Digital Input	02h	DI	R	00h	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Fault 1	04h	FAULT1	MIXED	46h	CRC	POR	FAULT2	ALRMT2	ALRMT1	24VL	24VM	WBG
Filter IN1	06h	FLT1	RW	08h	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN2	08h	FLT2	RW	08h	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN3	0Ah	FLT3	RW	08h	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN4	0Ch	FLT4	RW	08h	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN5	0Eh	FLT5	RW	08h	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN6	10h	FLT6	RW	08h	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN7	12h	FLT7	RW	08h	0	0	0	WBE	FBP	DELAY[2:0]		
Filter IN8	14h	FLT8	RW	08h	0	0	0	WBE	FBP	DELAY[2:0]		
Configuration	18h	CFG	RW	00h	0	0	0	24VF	CLRF	0	0	REFDI_SH_ENA
Input Enable	1Ah	INEN	RW	FFh	CH[7]	CH[6]	CH[5]	CH[4]	CH[3]	CH[2]	CH[1]	CH[0]
Fault 2	1Ch	FAULT2	COR	00h	0	0	FAULT8CK	OTSHDN	RFDIO	RFDIS	RFWBO	RFWBS
Fault 2 Enables	1Eh	FAULT2EN	RW	00h	0	0	FAULT8CKE	OTSHDNE	RFDIOE	RFDISE	RFWBOE	RFWBSE
GPO	22h	GPO	RW	00h	STK	0	0	0	0	0	0	0
Fault 1 Enables	24h	FAULT1EN	RW	C0h	CRCE	PORE	FAULT2E	ALRMT2E	ALRMT1E	24VLE	24VME	WBGE
No-Op	26h	NOP	NA	-	Dummy register. Contents of registers DI and WB are clocked out normally during attempted SPI writes to this register. Useful for Daisy Chain mode.							

Register Type Legend:

R: Read only
RW: Read and Write
COR: Latched Read only, Clear-On-Read
MIXED: Some bits are Clear-On-Read type, others are cleared differently. See bit descriptions for details.

Register Detailed Description

WB (Clear On Read)

Address = 0x00
Default = 0x00
Wire break status for each channel. Not cleared if the wire break condition is still present upon reading the register.

BIT	NAME	DESCRIPTION
7:0	WB[7:0]	0: No Wire Break condition detected for channel x 1: Wire Break condition detected for channel x The bit remains high even if the wire break condition disappears and is only cleared upon reading the register.

DI (Read)

Address = 0x02
Default = 0x00
Digital input state, DIx is the state of the corresponding input pin after the multiplexer that selects between the filter output and the comparator output.

BIT	NAME	DESCRIPTION
7:0	DI[7:0]	0: Channel x is driven low 1: Channel x is driven high Note: Input Channels are numbered IN1 – IN8, so IN1 maps to DI0, IN2 to DI1 …. and IN8 to DI7.

FAULT1 (Mixed)

Address = 0x04

Default = 0x46

BIT	NAME	DESCRIPTION
7	CRC	0: The last received SPI frame was not corrupted 1: The last received SPI frame was corrupted It is not cleared upon read, but when an uncorrupted SPI frame is received. CRC is only active in SPI Interface Modes 0 and 2
6	POR	0: Normal operating conditions 1: POR event has reset the register map to its power-on reset state This bit is cleared only if the user writes “0” to it. The other bits in this register are unaffected by the write access.
5	FAULT2	0: An enabled bit in the FAULT2 register is not set 1: An enabled bit in the FAULT2 register is set This bit is cleared on read only if the FAULT2 register is cleared or the bit is disabled.
4	ALRMT2*	0: Temperature Alarm 1 threshold has not been exceeded 1: Temperature Alarm 1 threshold has been exceeded Cleared upon reading this register.
3	ALRMT1*	0: Temperature Alarm 2 threshold has not been exceeded 1: Temperature Alarm 2 threshold has been exceeded Cleared upon reading this register.
2	24VL*	0: 24V supply is normal (above the 24VL threshold) 1: 24V supply is low (below the 24VL threshold) Cleared upon reading this register. If bit 4 in CFG Register (24VF) is 0, 24VL is can also be cleared after any SPI transaction while operation in modes 0 or 2.

BIT	NAME	DESCRIPTION
1	24VM*	0: 24V supply is normal (above the 24VM threshold) 1: 24V supply is missing (below the 24VM threshold) Cleared upon reading this register. If bit 4 in CFG Register (24VF) is 0, 24VM is can also be cleared after any SPI transaction while operation in modes 0 or 2.
0	WBG	0: No bit in the WB register is set 1: One or more bits in the WB register are set Cleared upon reading the WB register.

*These flags are “latched” and they remain set until read even if the fault goes away, and are not cleared if the fault condition is still present when the register is read.

FLT1 to FLT8 (Read/Write)

Address = 0x06 – 0x14 (increments of 2)
Default = 0x08

BIT	NAME	DESCRIPTION
7	0	Reserved
6	0	Reserved
5	0	Reserved
4	WBE	0: Wire Break detection is disabled for channel x 1: Wire Break detection is enabled for channel x If WBE = 0 the corresponding WBx bit is always low and the WB detection circuits for channel x are off. The REFWB resistor on pin REFWB can be removed if the WBE bits of all the channels are low.
3	FBP	0: Programmable filter on INx is used 1: Programmable filter on INx is bypassed
2:0	DELAY[2:0]	Programmable filter values for INx (the WBx filter value is 20ms and is not programmable). 000 -> 50µs 001 -> 100µs 010 -> 400µs 011 -> 800µs 100 -> 1.6ms 101 -> 3.2ms 110 -> 12.8ms 111 -> 20ms

CFG (Read/Write)

Address = 0x18
Default = 0x00

BIT	NAME	DESCRIPTION
7:5	0	Reserved
4	24VF	0: Flags 24VL and 24VM are cleared after any full frame SPI transaction or by reading the FAULT1 register 1: 24VL and 24VM are cleared only by reading the FAULT1 register Only affects SPI modes 0 and 2.
3	CLRF	0: Filters (INx and WBx) operate normally 1: All the filters (INx and WBx) are fixed at the mid-scale value for the chosen delay The filters resume normal operation when CLRF is cleared.
2:1	0	Reserved
0	REFDI_ SH_ENA	0: Disables the detection of a short circuit condition on the REFDI pin 1: Enables the detection of a short circuit condition on the REFDI pin

INEN (Read/Write)

Address = 0x1A
Default = 0xFF

BIT	NAME	DESCRIPTION
7:0	CH[7:0]	0: CH[x] = 0, INx is disabled and the current source is set to 0mA and the DIx bit in the DI register is set to 0. 1: CH[x] = 1, INx is enabled Note: Input Channels are numbered IN1 – IN8, so IN1 maps to DI0, IN2 to DI1 …. and IN8 to DI7

FAULT2 (Clear On Read)

Address = 0x1C
Default = 0x00

BIT	NAME	DESCRIPTION
7:6	0	Reserved
5	FAULT8CK	0: SPI receives a number of clock pulses equal to a multiple of eight, valid transaction 1: SPI receives a number of clock pulses not equal to a multiple of eight, the SPI command is rejected
4	OTSHDN	0: Normal operating conditions 1: Over temperature shutdown (the safe operating temperature has been exceeded). Over Temperature Shutdown: all inputs and LED drivers are turned off to reduce power dissipation and protect the die. The SPI interface and Internal Regulator remain active and if the temperature continues to rise, the regulator will be turned off.
3	RFDIO	0: Normal operating conditions 1: Open condition is detected on the REFDI pin This bit remains 1 even if the fault condition disappears and is cleared upon reading this register. This bit is 1 when thermal shutdown happens, because REFDI function turns off in thermal shutdown No action on the IN[8:1] channels when this condition occurs.
2	RFDIS	0: Normal operating conditions 1: Short condition is detected on the REFDI pin The bit remains 1 even if the fault condition disappears and is cleared upon reading this register. All the IN[8:1] channels are disabled as long as the short condition on REFDI is present.

BIT	NAME	DESCRIPTION
1	RFWBO	0: Normal operating conditions 1: Open condition is detected on the REFWB pin This bit remains 1 even if the fault condition disappears and is cleared upon reading this register. This bit is 1 when thermal shutdown happens, because REFWB function turns off in thermal shutdown. No action on the IN[8:1] channels when this condition occurs.
0	RFWBS	0: Normal operating conditions 1: Short condition is detected on the REFWB pin This bit remains 1 even if the fault condition disappears and is cleared upon reading this register. No action on the IN[8:1] channels when this condition occurs.

FAULT2EN (Read/Write)

Address = 0x1E
Default = 0x00

BIT	NAME	DESCRIPTION
7:6	0	Reserved
5	FAULT8CKE	0: Disable bit FAULT2 in FAULT1 Register 1: Enable bit FAULT2 in FAULT1 register to be set when FAULT8CK is high
4	OTSHDNE	0: Disable bit FAULT2 in FAULT1 Register 1: Enable bit FAULT2 in FAULT1 register to be set when OTSHDN is high
3	RFDIOE	0: Disable bit FAULT2 in FAULT1 Register 1: Enable bit FAULT2 in FAULT1 register to be set when RFDIO is high
2	RFDISE	0: Disable bit FAULT2 in FAULT1 Register 1: Enable bit FAULT2 in FAULT1 register to be set when RFDIS is high
1	RFWBOE	0: Disable bit FAULT2 in FAULT1 Register 1: Enable bit FAULT2 in FAULT1 register to be set when RFWBO is high
0	RFWBSE	0: Disable bit FAULT2 in FAULT1 Register 1: Enable bit FAULT2 in FAULT1 register to be set when RFWBS is high

GPO (Read/Write)

Address = 0x22
Default = 0x00

BIT	NAME	DESCRIPTION
7	STK	0: $\overline{\text{FAULT}}$ pin is not sticky. $\overline{\text{FAULT}}$ condition is determined by the logical OR of the unmasked real-time FAULT1 register sources, and not the FAULT1 Register bits. 1: $\overline{\text{FAULT}}$ pin is sticky. If at least one bit in the FAULT1 register is set and unmasked, $\overline{\text{FAULT}}$ remains low until FAULT1 register is read (Figure 8).
6:0	0	Reserved

FAULT1EN (Read/Write)

Address = 0x24
Default = 0xC0

BIT	NAME	DESCRIPTION
7	CRCE	0: $\overline{\text{FAULT}}$ pin is not asserted when CRC is 1 1: $\overline{\text{FAULT}}$ pin is asserted when CRC is 1
6	PORE	0: $\overline{\text{FAULT}}$ pin is not asserted when POR is 1 1: $\overline{\text{FAULT}}$ pin is asserted when POR is 1
5	ALRMT2E	0: $\overline{\text{FAULT}}$ pin is not asserted when ALRMT1 is 1 1: $\overline{\text{FAULT}}$ pin is asserted when ALRMT2 is 1
4	ALRMT1E	0: $\overline{\text{FAULT}}$ pin is not asserted when ALRMT1 is 1 1: $\overline{\text{FAULT}}$ pin is asserted when ALRMT1 is 1:
3	FAULT2	0: $\overline{\text{FAULT}}$ pin is not asserted when FAULT2 is 1 1: $\overline{\text{FAULT}}$ pin is asserted when FAULT2 is 1:
2	24VLE	0: $\overline{\text{FAULT}}$ pin is not asserted when 24VL is 1 1: $\overline{\text{FAULT}}$ pin is asserted when 24VL is 1 .
1	24VME	0: $\overline{\text{FAULT}}$ pin is not asserted when 24VM is 1 1: $\overline{\text{FAULT}}$ pin is asserted when 24VM is 1
0	WBGE	0: $\overline{\text{FAULT}}$ pin is not asserted when WBG is 1 1: $\overline{\text{FAULT}}$ pin is asserted when WBG is 1

NOP (N/A)

Address = 0x26
Default = N/A

BIT	NAME	DESCRIPTION
7:0	NOP[7:0]	Dummy register. DI and WB are clocked out normally during attempted writes to this register. Useful for Daisy Chain mode.

Applications Information

Power Supply Sequencing

The MAX22190 does not require special power supply sequencing. The SPI interface logic level (VL) is set independently from the field (VDD24) or LDO output (VDD) levels.

Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass VDD24, VL, and VDD with 0.1µF ceramic capacitors to GND. Place the bypass capacitors as close as possible to the power supply input pins.

Powering the MAX22190 With the VDD Pin

The MAX22190 can alternatively be powered using a 3.0 - 5.5V supply connected to the VDD pin. In this case a 24V supply is no longer needed and the VDD24 pin must be left floating (not connected). This configuration has lower power consumption and heat dissipation since the on-chip LDO voltage regulator is disabled (the VDD24 Undervoltage Lockout is below threshold and automatically disables the LDO).

In this configuration, the device will always indicate a “24V FAULT” due to bits 24VL and 24VM in FAULT1 register and the $\overline{FAULT}$ pin will always be active (pulled low). To overcome this, these two bits should be disabled if 24VLE and 24VME bits are enabled in FAULT1EN register by setting bits 24VLE and 24VME in the FAULT1EN register to 0.

PCB Layout Recommendations

The PCB designer should follow some critical recommendations in order to get the best prformance from the design.

- Keep the input/output traces as short as possible. Avoid using vias to make low-inductance paths for the signals.
- Have a solid ground plane underneath the entire EP area with multiple thermal vias for best thermal performance.

Isolating the SPI Interface

A companion product, MAX14483 is available which is optimized to support the MAX22190. MAX14483 is an 6-channel, 3.75kV$_{RMS}$, low power Digital Isolator ideal for interfacing to low-voltage products such as microcontrollers or FPGAs. Figure 9 demonstrates daisy chain operation, showing SPI signals, control signals, and power monitoring signals isolated between the “field” and “logic” sides of the design. A single MAX14483 can be used for multiple MAX22190s.

Figure 10 demonstrates two MAX22190’s connected as Independent Slaves, meaning they have separate Chip Select ($\overline{CS}$) signals from the master (MCU). In order to support the extra isolated $\overline{CS}$ channel a second isolator, MAX12930 is used. Care must be taken to ensure both MAX22190’s are not enabled simultaneously to avoid SPI-bus contention.

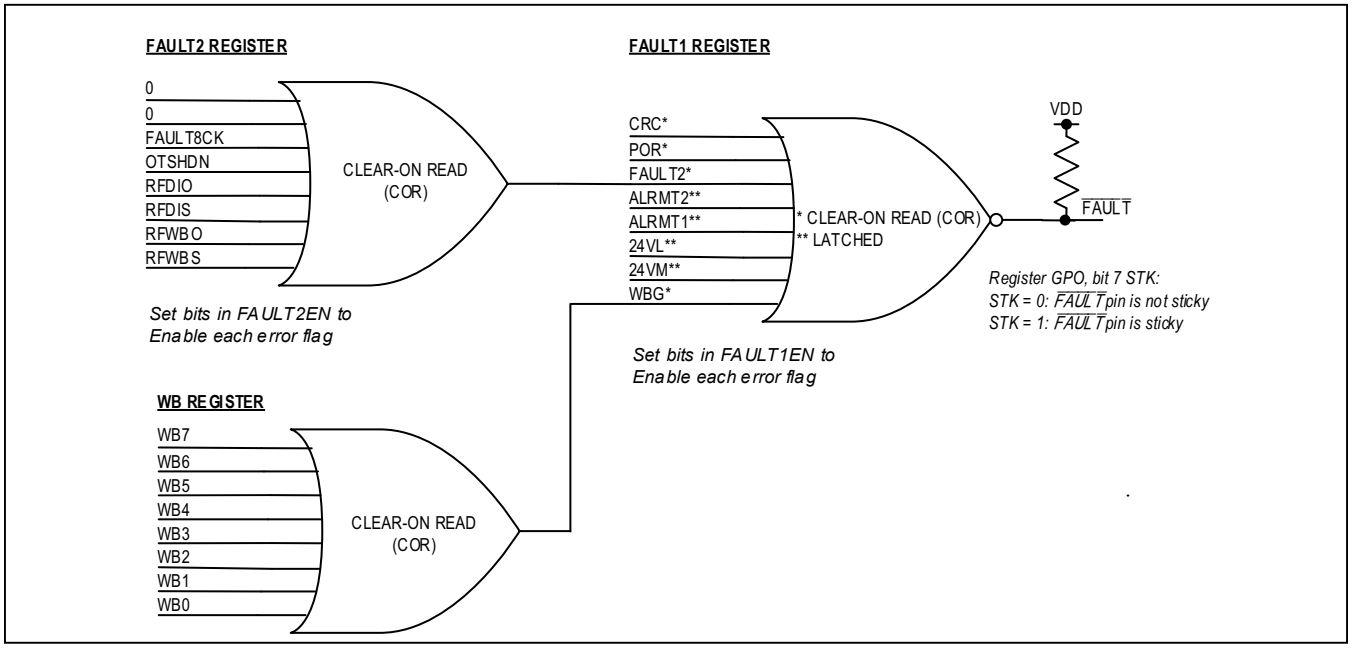


Figure 8. $\overline{FAULT}$ Output Sources

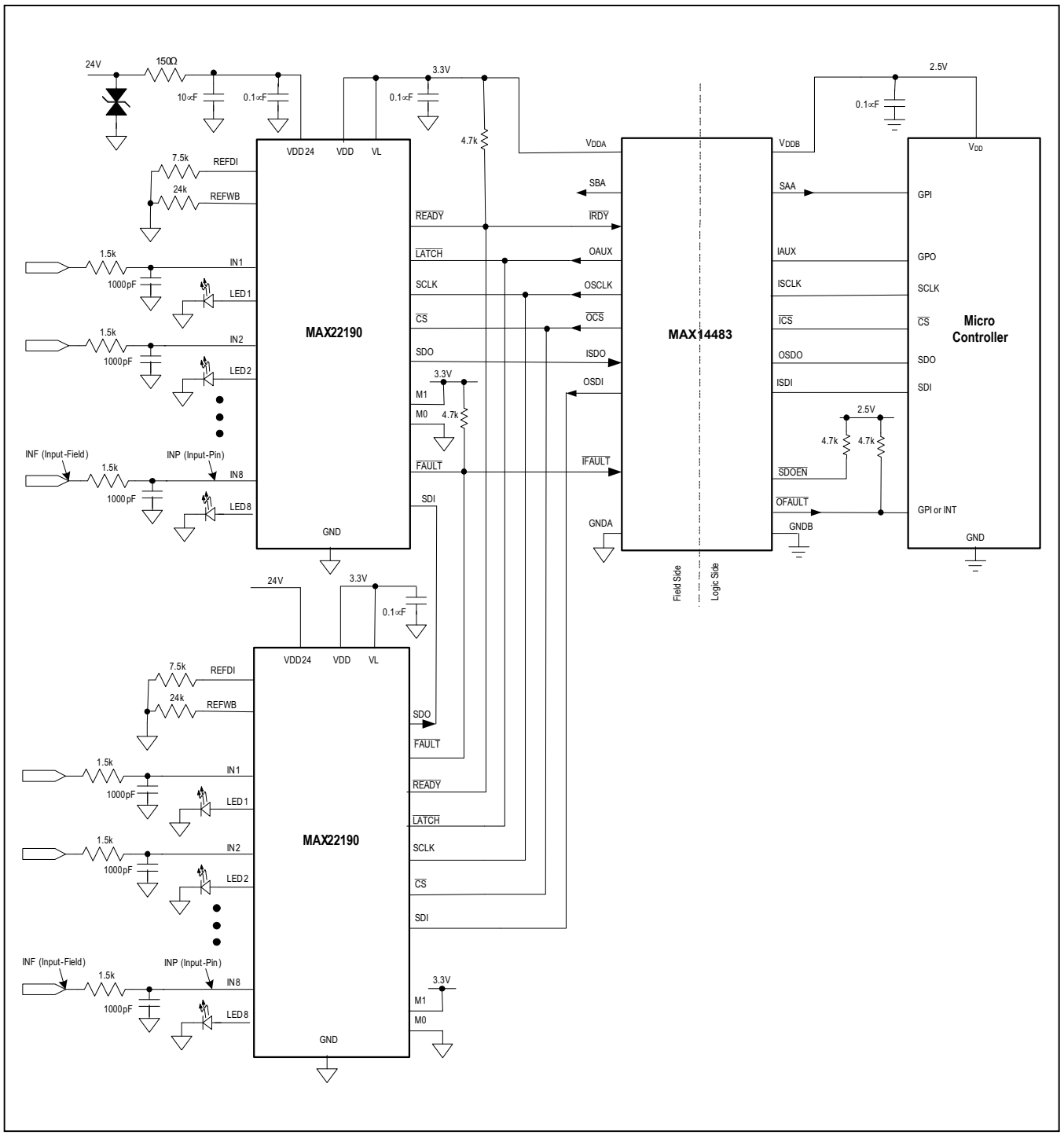


Figure 9. 16 Input, SPI Daisy Chain

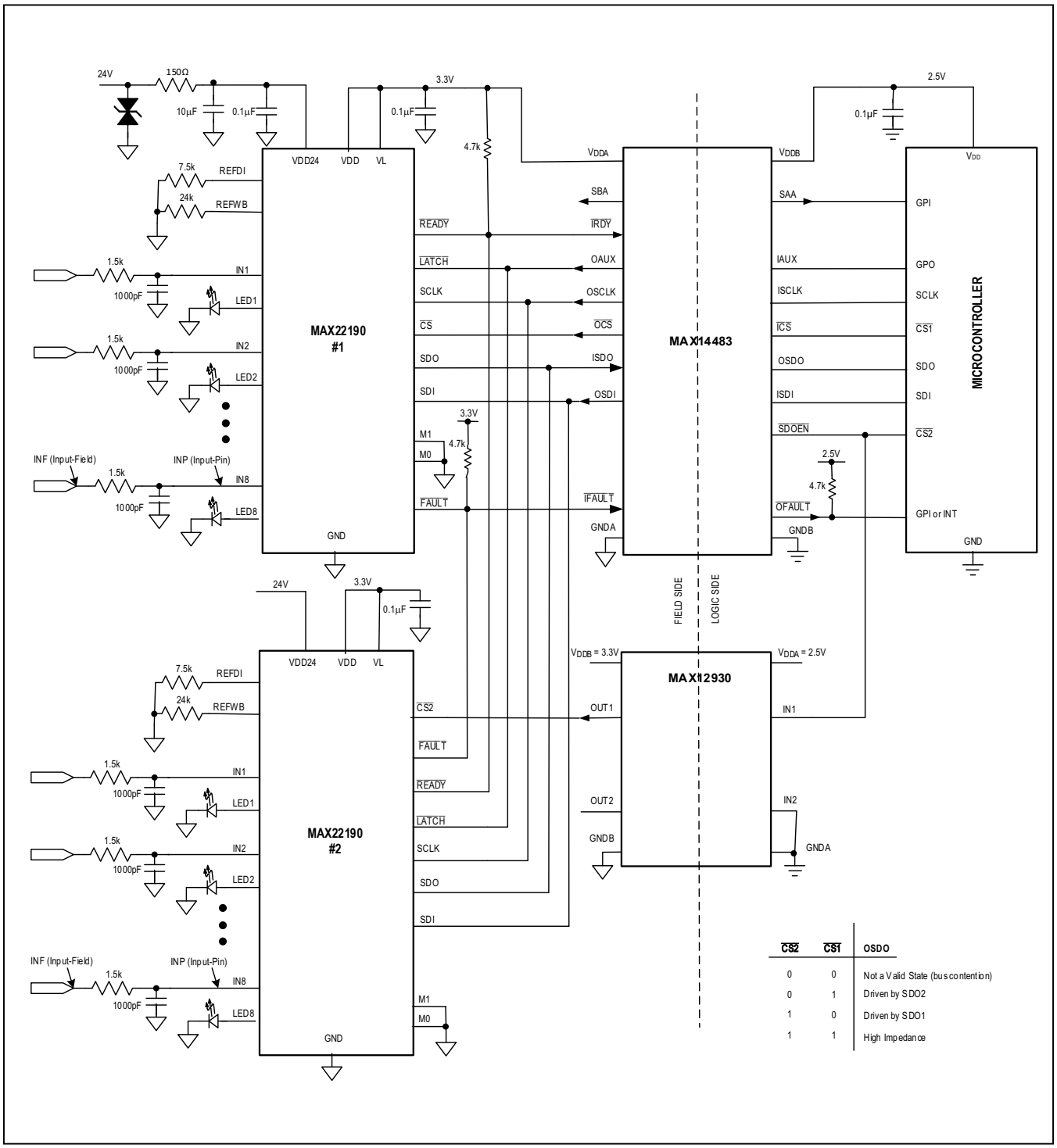


Figure 10. 16 Input, Independent Slave SPI (Seperate $\overline{CS}$ for Each SPI Slave)

Type 2 Sensor Inputs

The additional input current (6mA min) and associated power dissipation of Type 2 input requires the use of two MAX22190 inputs in parallel. The current of each channel is set to a nominal 3.39mA (6.78mA total) by placing a 5.2kΩ resistor from REFDI to GND. The proper voltage drop across the input resistor is maintained by reducing the resistance from 1.5kΩ to 1kΩ for each MAX22190 channel. For proper surge protection, it is important that each MAX22190 input has its own resistor. Any two MAX22190 channels may be used; they need not be contiguous, or even on the same IC (Figure 11). Either channel may be read to determine the input state. The additional power dissipation from this Type 2 configuration reduces the maximum ambient operating temperature to 120°C, when all inputs are at 30V, and the MAX22190s are powered from a 30V supply and there is no additional load on VDD.

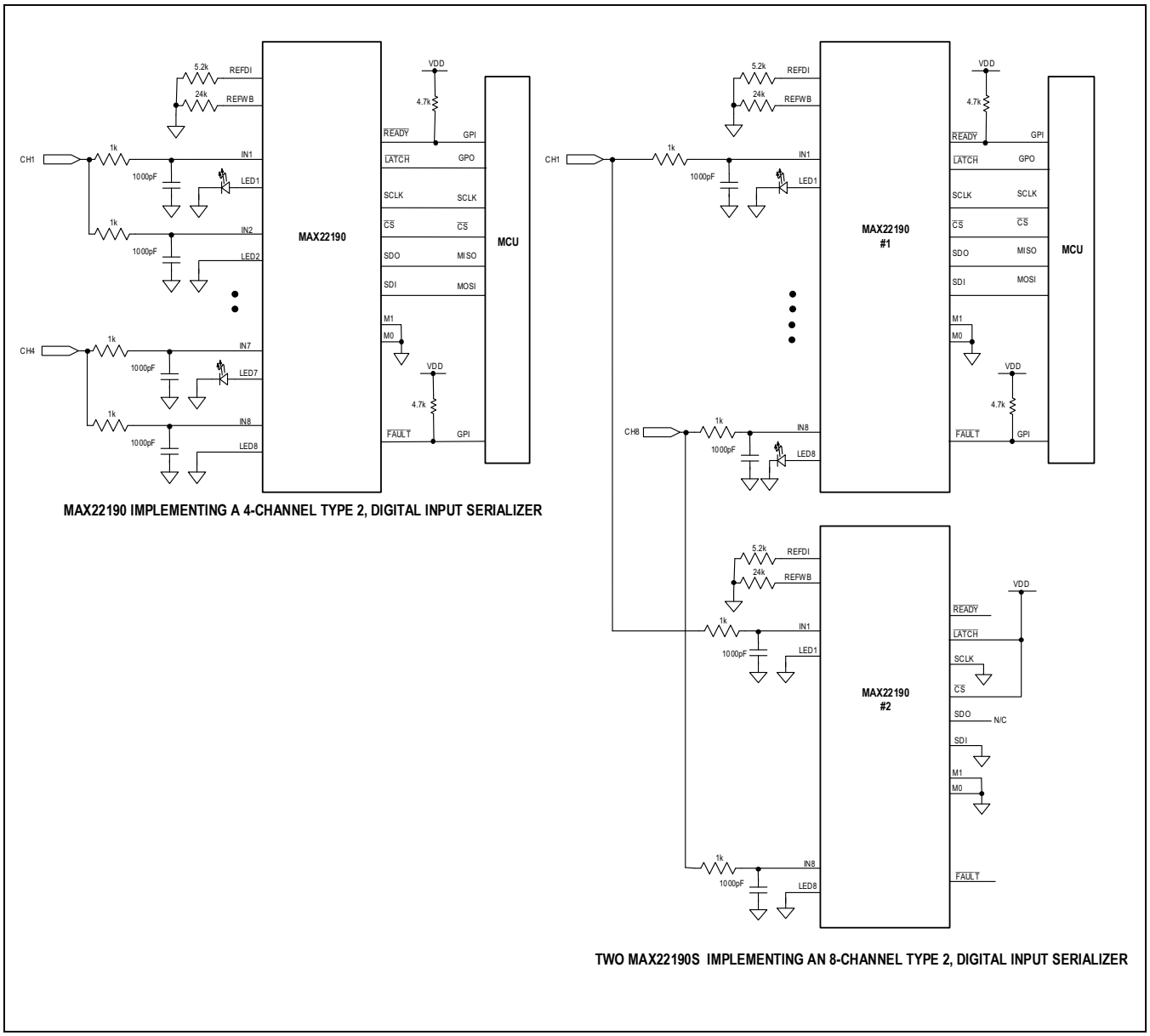


Figure 11. Implementing a Type 2 Sensor with MAX22190

EMC Standard Compliance

The MAX22910 is required to operate reliably in harsh industrial envicomments. Maxim does board-level immunity testing for products such as the MAX22190 to address IEC61000-4-x Transient Immunity Standards:

- IEC 61000-4-2 Electrostatic Discharge (ESD)
- IEC 61000-4-4 Electrical Fast Transient /Burst (EFT)
- IEC 61000-4-5 Surge Immunity

Maxim's proprietary process technology provides high ESD support with internal ESD structures, but external components are also required to absorb energy from burst and surge transients. The circuit with external components shown in Figure 12 allows the device to operate in harsh industrial environments. Components were chosen to assist in suppression of voltage burst and surge transients, allowing the system to meet or exceed international EMC requirements. The system shown in Figure 12, using the components shown in Table 5, is designed to be robust against IEC ESD, EFT, and Surge specifications.

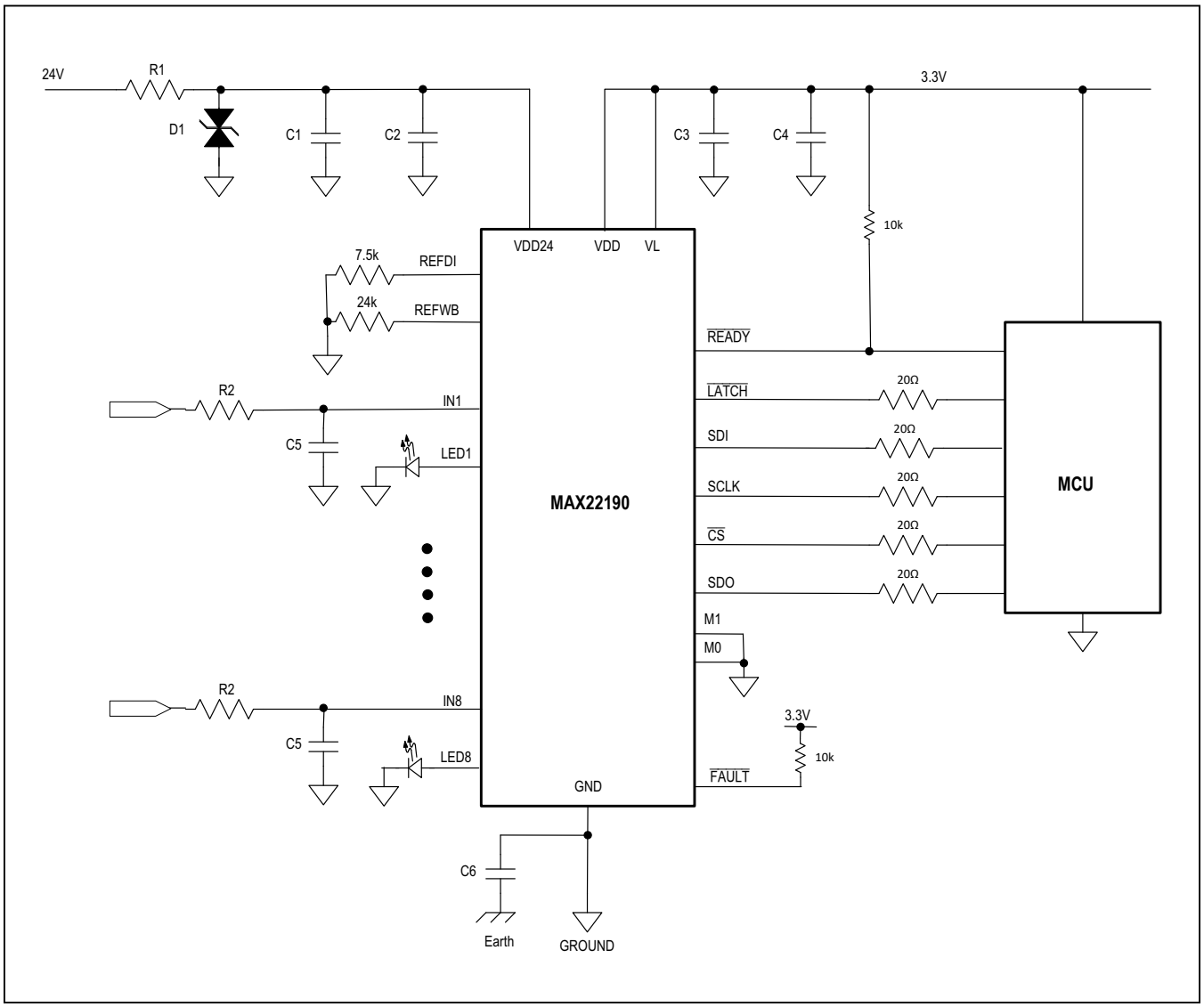


Figure 12. Typical EMC Protection Circuitry for the MAX22190

Table 5. Recommended Components

COMPONENT	DESCRIPTION	REQUIRED/RECOMMENDED/OPTIONAL
C1	10µF, 100V ceramic capacitor	Required
C2	0.1µF, 100V ceramic capacitor	Required
C3	1µF, 10V low ESR ceramic capacitor	Required
C4	0.1µF, 10V ceramic capacitor	Required
C5	1000pF, 100V ceramic capacitor	Recommended
C6	0.33µF, 3kV polypropylene capacitor (2220)	Recommended
D1	Bidirectional TVS diode (SMAJ33CA or SM30T39AY)	Recommended
R1	150Ω, 1W MELF resistor (CMB0207 series)	Recommended
R2	1.5kΩ or 1kΩ, 1W MELF resistor (CMB0207 series)	Required
All other Resistors	1/8W resistor	Required
D1 - D8	LEDs for visual input status indication	Recommended

Test Levels and Methodology

MAX22190 is tested for Transient Immunity Standards as specified in IEC 61000-4-x. These tests are for industrial equipment which are subjected to various transients. The three main tests are:

- IEC 61000-4-2: This ESD standard covering surges of tens of ns duration, is more stressful than other standards such as Human Body Model (HBM) or Machine Model (MM), both of which are tested as standard for all Maxim products.
- IEC 61000-4-4: This standard indicates the capability of the device or equipment to able to survive repetitive electrical fast transients and bursts which often occur from arcing contacts in switches and relays.
- IEC 61000-4-5: This standard indicates the capability of the device or equipment to survive surges caused by events such as lightning strikes or industrial power surges caused by switching heavy loads or short circuit fault conditions.

In all these tests the part or DUT is soldered onto an application board with bypass capacitors on power supply pins. In the case of MAX22190 the standard Evaluation Kit (MAX22190EVKIT#) is used for these tests.

IEC 61000-4-2 Electrostatic Discharge (ESD):

This is an international standard which gives immunity requirements and test procedures related to “electrostatic discharge”.

Contact Discharge method: the electrode of the test generator is held in contact with the EUT, and the discharge actuated by the discharge switch within the generator.

Air Gap Discharge method: the charged electrode of the generator is brought close to the EUT, and the discharge actuated by a spark to the EUT.

An ESD Test Generator is used with a “sharp point’ to make direct connection to the EUT (pin) under test for Contact ESD testing, and a ‘round tip’ is added to the generator for Air-Gap ESD testing.

Output Voltage	Up to 8kV (nominal) for contact discharge up to 15kV (nominal) for air gap discharge
Polarity of the output voltage	Positive and negative
Holding time	At least 5 seconds
Number of applications	10 consecutive ESD discharges for each polarity

Transient Voltage Suppression (TVS) diodes are used to meet the ESD transient immunity requirements of IEC 61000-4-2. These diodes have extremely fast response times in order to respond to the 1ns rise time of the ESD pulse, Figure 13a shows the IEC 61000-4-2 model and-Figure 13b shows the current waveform for IEC 61000-4-2 ESD Contact Discharge Test. The TVS diode clamps the incoming transients at a safe level to avoid damage to the semiconductor device.

IEC 61000-4-4 Electrical Fast Transient / Burst (EFT)

An EFT/Surge Generator with an output voltage range with 50Ω load of up to 2kV is used to generate the voltage waveforms defined by the IEC specification. The Capacitive Coupling Clamp provides the ability to couple the fast transients (burst) from the EFT Generator to the pins of the MAX22190 without any galvanic connection to the MAX22190's pins. The waveform is shown in Figure 14.

Polarity	Positive and negative
Test Voltage	Up to ±2 kV
Repetition Frequency	5kHz
Burst Duration	15ms (at 5 kHz)
Burst Period	300ms
Signal Applied To	Input ports and Voltage Supplies (VDD24 and VDD)
Test Duration	60 seconds

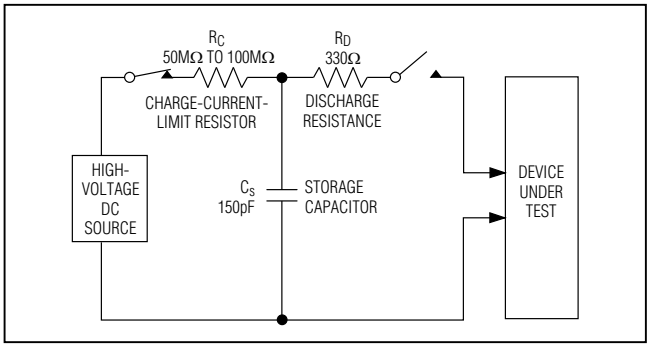


Figure 13a. Test Circuit

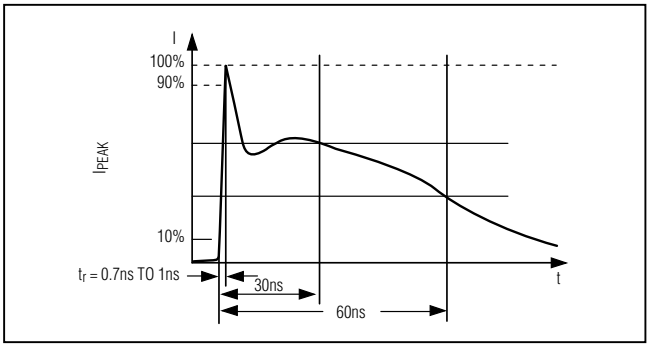


Figure 13b. Test Waveform

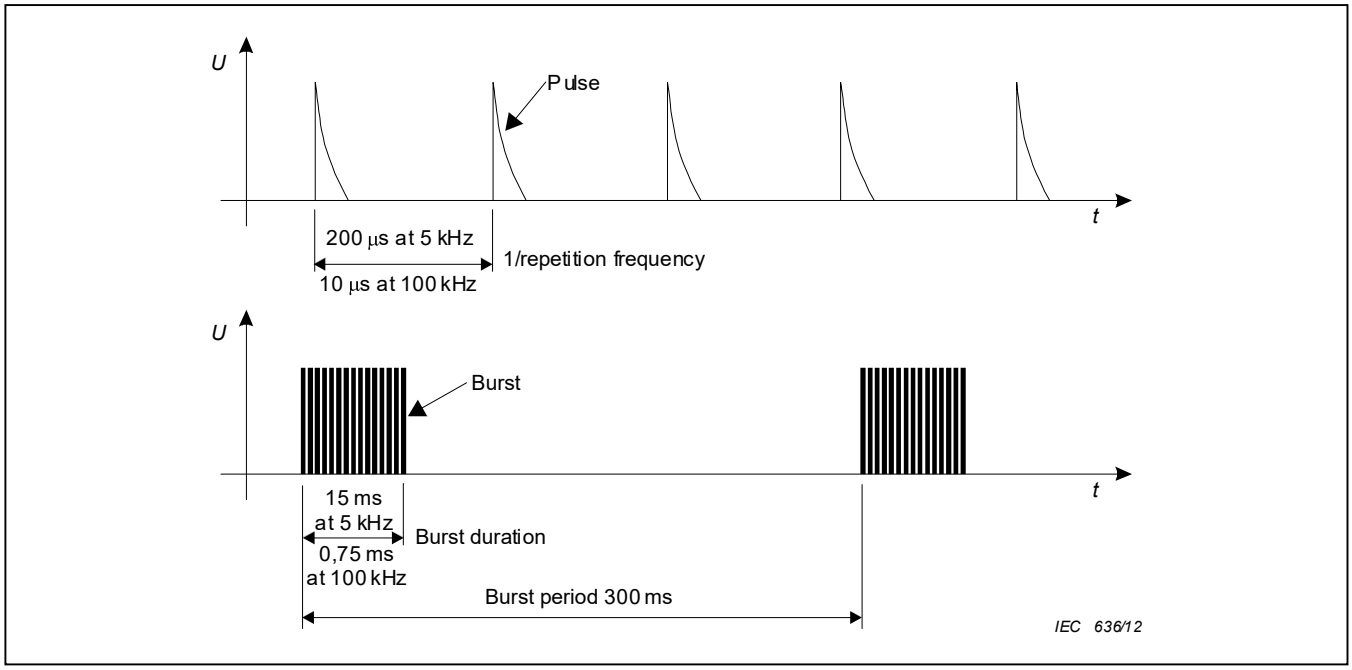


Figure 14. Electrical Fast Transient/Burst Waveform

IEC 61000-4-5 Surge Immunity

This standard specifies different wave generator specifications. The 1.2/50µs combination wave generator is used for testing ports intended for power lines and short-distance signal connections. This is the test Maxim uses and the waveform is shown in Figure 15.

Polarity	Positive and negative
Test Voltage	Up to ±2kV
Waveform parameters	Front time 1.2µs Time to half Value 50µs
Signal applied to	Input port-to-Input port, Input port-to-Ground
Repetition Rate	1 per minute

The standard defines 6 classes of test levels which depend on the installation conditions (see Annex A, table A.1 in IEC 61000-4-5 standard). The class determines the protection with corresponding voltage levels from 25V to 4kV. In addition this defines the coupling mode (Line-Line or Line-to-Ground) and the source impedance (Zs) required. The Class which most closely fits the applications using products such as MAX22190 are Class 3 for Unsymetrical operated circuits/lines with suggested test levels of 1 kV for Line-to-Line and 2 kV for Line-to-Ground.

The selection of source impedance is discussed in Annex B of IEC 61000-4-5 with recommended Zs of 42Ω. Since the generator has an internal impedance or 2Ω an external 40Ω resistor is used in series with the generator, as shown in simplified version in Figure 16.

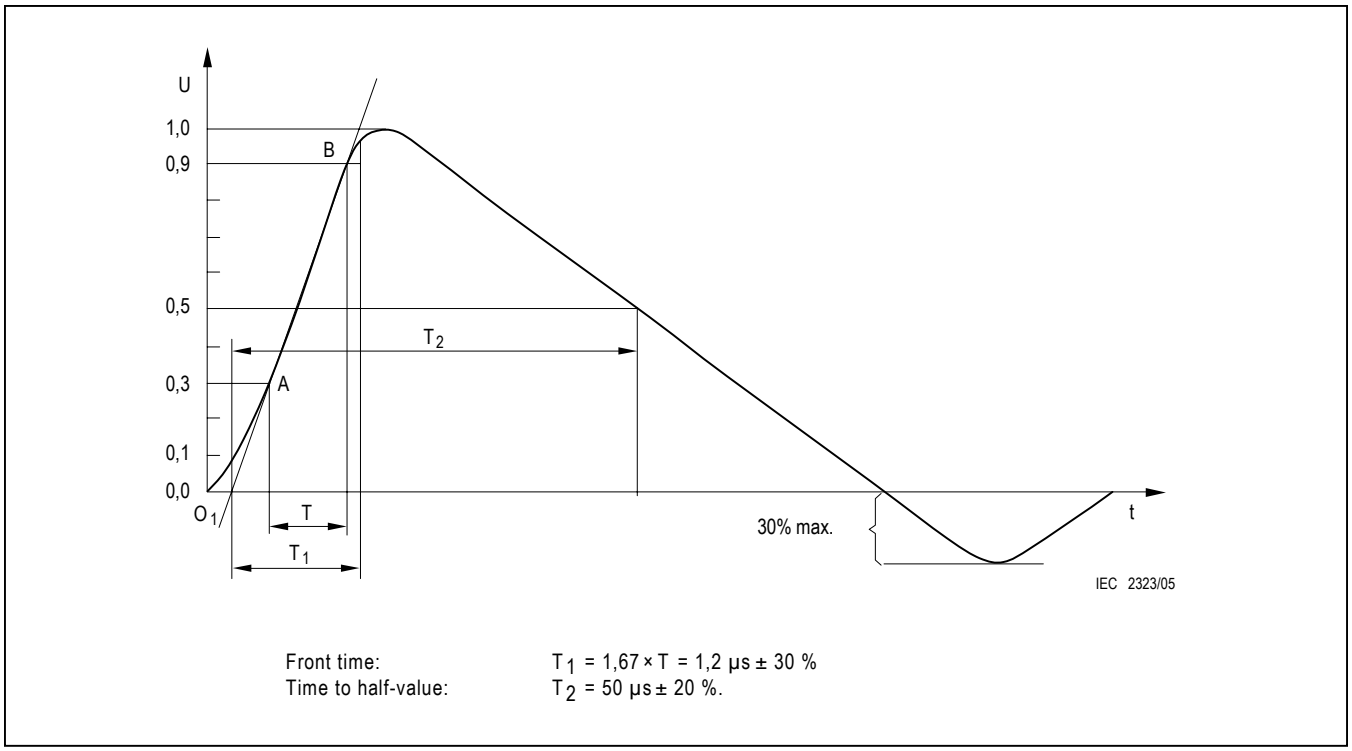


Figure 15. 1.2/50 µs Surge Voltage Waveform

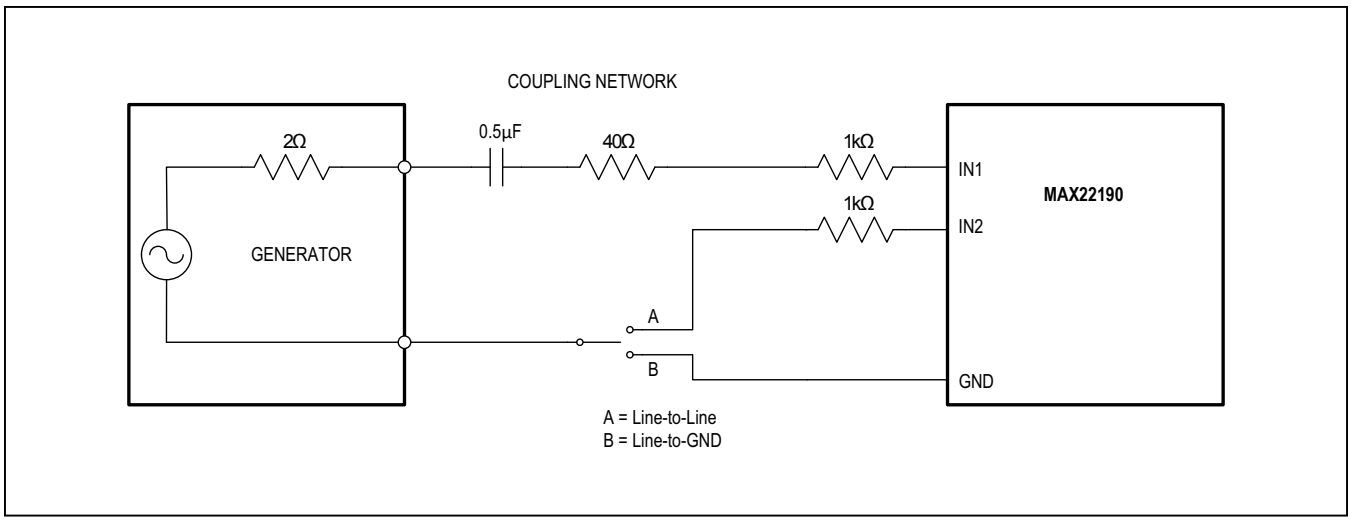


Figure 16. Surge Testing Methods

Table 6. Equipment Used for EMC Tests

EQUIPMENT	DESCRIPTION	TEST(S)
MAX22190EVKIT#	Evaluation board with MAX22190 and recommend operating circuit	All
ESD Test Generator	Teseq NSG438 with Air Gap Discharge Tip 403-826	Contact ESD and Air-Gap ESD
EFT/Surge Generator	Haefely Technology ECOMPACT4	EFT and Surge
Signal & Data Line Coupling Network	Teseq CDN 117	Surge
Coupler with 0.5µF Capacitor	INA 174A	Surge
Burst/EFT Dateline Coupling Clamp	Teseq CDN 3425	EFT

Table 7. Transient Immunity Test Results

TEST		RESULT
IEC 61000-4-2 Electrostatic Discharge (ESD)	Contact ESD	±8kV
	Air Gap ESD	±15kV
IEC 61000-4-4 Electrical Fast Transient/Burst (EFT)	Input Line	±1kV
	Power Supply	±1kV
IEC 61000-4-5 Surge Immunity	Line-to-Line	±2kV
	Line-to-Ground	±1kV

Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX22190ATJ+	-40°C to +125°C	32-TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32-TQFN	T3255+6	**21-0140**	**90-0603**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/17	Initial release	—