# 8-Channel, 24-Bit, Simultaneous Sampling ADC with Power Scaling, 110.8 kHz BW

# AD7768

## FEATURES

- Precision ac and dc performance
- 8-channel simultaneous sampling
  - 256 kSPS ADC output data rate per channel
  - 108 dB dynamic range
  - 110.8 kHz input bandwidth (−3 dB bandwidth (BW))
  - −120 dB THD typical
  - ±2 ppm INL, ±50 µV offset error, ±30 ppm gain error
- Optimized power dissipation vs. noise vs. input bandwidth
  - Selectable power, speed, and input bandwidth
    - Fast: highest speed; 110.8 kHz BW, 51.5 mW per channel
    - Median: half speed, 55.4 kHz BW, 27.5 mW per channel
    - Eco: lowest power, 13.8 kHz BW, 9.375 mW per channel
  - Input BW range: dc to 110.8 kHz
  - Programmable input bandwidth/sampling rates
- Cyclic redundancy check (CRC) error checking on data interface
- Daisy-chaining
- Linear phase digital filter
  - Low latency sinc5 filter
  - Wideband brick wall filter: ±0.005 dB ripple to 102.4 kHz
- Analog input precharge buffers
- Power supply
  - AVDD1 = 5 V, AVDD2 = 2.25 V to 5 V
  - IOVDD = 2.5 V to 3.3 V or IOVDD = 1.8 V
- 64-lead LQFP package, no pad
- Temperature range: −40°C to +105°C

## APPLICATIONS

- Data acquisition systems: USB/PXI/Ethernet
- Instrumentation and industrial control loops
- Audio test and measurement
- Vibration and asset condition monitoring
- 3-phase power quality analysis
- Sonar
- High precision medical EEG/EMG/ECG

## FUNCTIONAL BLOCK DIAGRAM

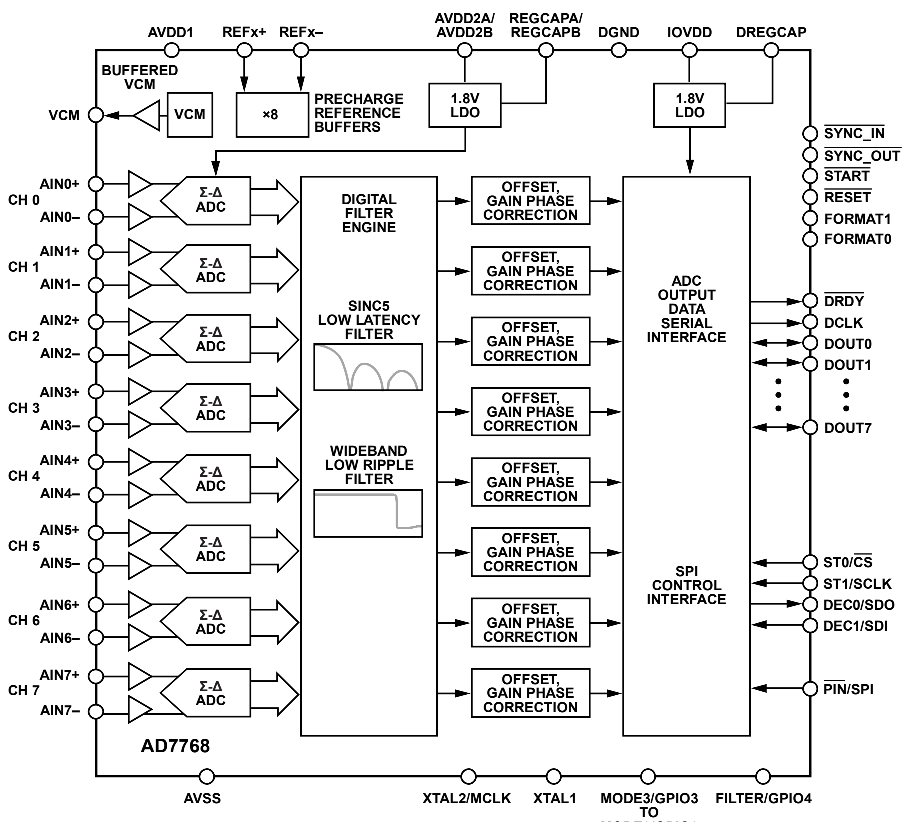


*Figure 1.*



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## REVISION HISTORY

**1/16—Revision 0: Initial Version**

# GENERAL DESCRIPTION

The AD7768 is an 8-channel, simultaneous sampling Σ-Δ analog-to-digital converter (ADC) with a Σ-Δ modulator and digital filter per channel, enabling synchronized sampling of ac and dc signals.

The AD7768 achieves 108 dB dynamic range at a maximum input bandwidth of 110.8 kHz, combined with typical performance of ±2 ppm integral nonlinearity (INL), ±50 µV offset error, and ±30 ppm gain error.

The AD7768 user can trade off input bandwidth, output data rate, and power dissipation. Select one of three power modes to optimize for noise targets and power consumption. The flexibility of the AD7768 allows it to become a reusable platform for low power dc and high performance ac measurement modules.

The AD7768 has three modes: fast mode (256 kSPS maximum, 110.8 kHz input bandwidth, 51.5 mW per channel), median mode (128 kSPS maximum, 55.4 kHz input bandwidth, 27.5 mW per channel) and eco mode (32 kSPS maximum, 13.8 kHz input bandwidth, 9.375 mW per channel).

The AD7768 offers extensive digital filtering capabilities, such as a wideband, low ±0.005 dB pass-band ripple, antialiasing low-pass filter with sharp roll off, and 105 dB attenuation at the Nyquist frequency.

Frequency domain measurements can use the wideband linear phase filter. This filter has a flat pass band (±0.005 dB ripple) from dc to 102.4 kHz at 256 kSPS, from dc to 51.2 kHz at 128 kSPS, or from dc to 12.8 kHz at 32 kSPS.

The AD7768 also offers sinc response via a sinc5 filter, a low latency path for low bandwidth, and low noise measurements. The wideband and sinc5 filters can be selected and run on a per channel basis.

Within these filter options, the user can improve the dynamic range by selecting from decimation rates of ×32, ×64, ×128, ×256, ×512, and ×1024. The ability to vary the decimation filtering optimizes noise performance to the required input bandwidth.

Embedded analog functionality on each ADC channel makes design easier, such as a precharge buffer on each analog input that reduces analog input current and a precharge reference buffer per channel reduces input current and glitches on the reference input terminals.

The device operates with a 5 V AVDD1A and AVDD1B supply, a 2.25 V to 5.0 V AVDD2A and AVDD2B supply, and a 2.5 V to 3.3 V or 1.8 V IOVDD supply (see the 1.8 V IOVDD Operation section for specific requirements for operating at 1.8 V IOVDD).

For the purposes of clarity within this document, the AVDD1A and AVDD1B supplies are referred to as AVDD1 and the AVDD2A and AVDD2B supplies are referred to as AVDD2. For the negative supplies, AVSS is used to refer to AVSS1A, AVSS1B, AVSS2A, AVSS2B, and all other AVSS pins.

The specified operating temperature range is −40°C to +105°C. The device is housed in a 12 mm × 12 mm, 64-lead LQFP package.

Throughout this data sheet, multifunction pins, such as XTAL2/MCLK, are referred to either by the entire pin name or by a single function of the pin, for example MCLK, when only that function is relevant.

# SPECIFICATIONS

AVDD1A = AVDD1B = 4.5 V to 5.5 V, AVDD2A = AVDD2B = 2.0 V to 5.5 V, IOVDD = 2.25 V to 3.6 V, AVSS = DGND = 0 V, REFx+ = 4.096 V and REFx− = 0 V, MCLK = 32.768 MHz, analog input precharge buffers on, reference precharge buffers off, wideband filter, $f_{CHOP}$ = $f_{MOD}$/32, $T_A$ = −40°C to +105°C, unless otherwise noted. See Table 2 for specifications at 1.8 V IOVDD.

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ADC SPEED AND PERFORMANCE | | | | | |
| Output Data Rate (ODR), per Channel[1] | Fast | 8 | | 256 | kSPS |
| | Median | 4 | | 128 | kSPS |
| | Eco | 1 | | 32 | kSPS |
| Bandwidth | Fast, wideband filter | | | 110.8 | kHz |
| | Median, wideband filter | | | 55.4 | kHz |
| | Eco, wideband filter | | | 13.8 | kHz |
| Data Output Coding | | | Twos complement, MSB first | | |
| No Missing Codes[2] | | 24 | | | Bits |
| DYNAMIC PERFORMANCE | For 1.8 V operation, see Table 2; for dynamic range and SNR across all decimation rates, see Table 11 and Table 12 | | | | |
| Fast | Decimation by 32, 256 kSPS ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| Signal-to-Noise Ratio (SNR) | 1 kHz, −0.5 dBFS, sine wave input | | | | |
| | Sinc5 filter | 109 | 111 | | dB |
| | Wideband filter | 106 | 107.8 | | dB |
| Signal-to-Noise-and-Distortion Ratio (SINAD) | | 104.3 | 106.9 | | dB |
| Total Harmonic Distortion (THD) | | | −120 | −107 | dB |
| Spurious-Free Dynamic Range (SFDR) | | | 128 | | dBc |
| Median | Decimation by 32, 128 kHz ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| SNR | 1 kHz, −0.5 dBFS, sine wave input | | | | |
| | Sinc5 filter | 109 | 111 | | dB |
| | Wideband filter | 106 | 107.8 | | dB |
| SINAD | | 105.3 | 106.9 | | dB |
| THD | | | −120 | −113 | dB |
| SFDR | | | 128 | | dBc |
| Eco | Decimation by 32, 32 kHz ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| SNR | 1 kHz, −0.5 dBFS, sine wave input | | | | |
| | Sinc5 filter | 109 | 111 | | dB |
| | Wideband filter | 106 | 107.8 | | dB |
| SINAD | | 105.3 | 106.9 | | dB |
| THD | | | −120 | −113 | dB |
| SFDR | | | 128 | | dBc |
| INTERMODULATON DISTORTION (IMD) | $f_{INA}$ = 9.7 kHz, $f_{INB}$ = 10.3 kHz | | | | |
| | Second order | | −125 | | dB |
| | Third order | | −125 | | dB |
| ACCURACY | See Table 2 for 1.8 V operation | | | | |
| INL | Endpoint method | | ±2 | ±7 | ppm of FSR |
| Offset Error[3] | DCLK frequency ≤ 24 MHz | | ±50 | ±115 | µV |
| | 24 MHz to 32.768 MHz DCLK frequency[2] | | ±75 | ±150 | µV |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Offset Error Drift | DCLK frequency ≤ 24 MHz | | ±250 | | nV/°C |
| | 24 MHz to 32.768 MHz DCLK frequency | | ±750 | | nV/°C |
| Gain Error[3] | $T_A$ = 25°C | | ±30 | ±70 | ppm of FSR |
| Gain Drift vs. Temperature[2] | | | ±0.5 | ±1 | ppm/°C |
| VCM PIN | | | | | |
| Output | With respect to AVSS | | (AVDD1 − AVSS)/2 | | V |
| Load Regulation | $\Delta V_{OUT}/\Delta I_L$ | | 400 | | µV/mA |
| Voltage Regulation | Applies to the following VCM output options only: $V_{CM} = \Delta V_{OUT}/\Delta$(AVDD1 − AVSS)/2; $V_{CM}$ = 1.65 V; and $V_{CM}$ = 2.5 V | | 5 | | µV/V |
| Short-Circuit Current | | | 30 | | mA |
| ANALOG INPUTS | See the Analog Inputs section | | | | |
| Differential Input Voltage Range | $V_{REF}$ = (REFx+) − (REFx−) | $-V_{REF}$ | | $+V_{REF}$ | V |
| Input Common-Mode Range[2] | | AVSS | | AVDD1 | V |
| Absolute Analog Input Voltage Limits[2] | | AVSS | | AVDD1 | V |
| Analog Input Current | | | | | |
| Unbuffered | Differential component | | ±48 | | µA/V |
| | Common-mode component | | ±17 | | µA/V |
| Precharge Buffer On[4] | | | −20 | | µA |
| Input Current Drift | See Figure 48 | | | | |
| Unbuffered | | | ±5 | | nA/V/°C |
| Precharge Buffer On | | | ±31 | | nA/°C |
| EXTERNAL REFERENCE | | | | | |
| Reference Voltage | $V_{REF}$ = (REFx+) − (REFx−) | 1 | | AVDD1 − AVSS | V |
| Absolute Reference Voltage Limits[2] | Precharge reference buffers off | AVSS − 0.05 | | AVDD1 + 0.05 | V |
| | Precharge reference buffer on | AVSS | | AVDD1 | V |
| Average Reference Current | See Figure 47 | | | | |
| | Precharge reference buffers off | | ±72 | | µA/V/channel |
| | Precharge reference buffers on | | ±16 | | µA/V/channel |
| Average Reference Current Drift | See Figure 47 | | | | |
| | Precharge reference buffers off | | ±1.7 | | nA/V/°C |
| | Precharge reference buffers on | | ±49 | | nA/V/°C |
| Common-Mode Rejection | | | 95 | | dB |
| DIGITAL FILTER RESPONSE | | | | | |
| Low Ripple Wideband Filter | FILTER = 0 | | | | |
| Decimation Rate | Up to six selectable decimation rates; see the Decimation Rate Control section | 32 | | 1024 | |
| Group Delay | Latency | | 34/ODR | | sec |
| Settling Time | Complete settling, see Table 31 | | 68/ODR | | sec |
| Pass-Band Ripple[2] | | | | ±0.005 | dB |
| Pass Band | ±0.005 dB bandwidth | | 0.4 × ODR | | Hz |
| | −0.1 dB bandwidth | | 0.409 × ODR | | Hz |
| | −3 dB bandwidth | | 0.433 × ODR | | Hz |
| Stop Band Frequency | Attenuation > 105 dB | | 0.499 × ODR | | Hz |
| Stop Band Attenuation | See the Wideband Low Ripple Filter section | | 105 | | dB |
| Sinc5 Filter | FILTER = 1 | | | | |
| Decimation Rate | Up to six selectable decimation rates; see the Decimation Rate Control section | 32 | | 1024 | |
| Group Delay | Latency | | 3/ODR | | sec |
| Settling Time | Complete settling, see Table 32 | | 7/ODR | | sec |
| Pass Band | −3 dB bandwidth | | 0.204 × ODR | | Hz |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| REJECTION | | | | | |
| AC Power Supply Rejection Ratio (PSRR) | $V_{IN}$ = 0.1 V, AVDD1 = 5 V, AVDD2 = 5 V, IOVDD = 2.5 V | | | | |
| AVDD1 | | | 90 | | dB |
| AVDD2 | | | 100 | | dB |
| IOVDD | | | 75 | | dB |
| DC PSRR | $V_{IN}$ = 1 V | | | | |
| AVDD1 | | | 100 | | dB |
| AVDD2 | | | 118 | | dB |
| IOVDD | | | 90 | | dB |
| Analog Input Common-Mode Rejection Ratio (CMRR) | | | | | |
| DC | $V_{IN}$ = 0.1 V | 95 | | | dB |
| AC | Up to 10 kHz | | 95 | | dB |
| Crosstalk | −0.5 dBFS input on adjacent channels | | −115 | | dB |
| CLOCK | | | | | |
| Crystal Frequency | | 8 | 32.768 | 34 | MHz |
| External Clock (MCLK) | See the Timing Specifications section | | 32.768 | | MHz |
| Duty Cycle | For data sheet performance | | 50:50 | | % |
| MCLK Pulse Width[2] | Functionality | | | | |
| Logic Low | | 12.2 | | | ns |
| Logic High | | 12.2 | | | ns |
| CMOS Clock Input Voltage | See the logic inputs parameter | | | | |
| High, $V_{INH}$ | | | | | |
| Low, $V_{INL}$ | | | | | |
| LVDS Clock[2] | $R_L$ = 100 Ω | | | | |
| Differential Input Voltage | | 100 | | 650 | mV |
| Common-Mode Input Voltage | | 800 | | 1575 | mV |
| ADC RESET[2] | | | | | |
| ADC Start-Up Time After Reset[5] | Time to first $\overline{\text{DRDY}}$, fast mode, decimation by 32 | | 1.58 | 1.66 | ms |
| Minimum $\overline{\text{RESET}}$ Low Pulse Width | $t_{MCLK}$ = 1/MCLK | 2 × $t_{MCLK}$ | | | |
| LOGIC INPUTS | See Table 2 for 1.8 V operation | | | | |
| Input Voltage[2] | | | | | |
| High, $V_{INH}$ | | 0.65 × IOVDD | | | V |
| Low, $V_{INL}$ | | | | 0.7 | V |
| Hysteresis[2] | | 0.04 | | 0.09 | V |
| Leakage Current | | −10 | +0.03 | +10 | µA |
| | $\overline{\text{RESET}}$ pin[6] | −10 | | +10 | µA |
| LOGIC OUTPUTS | See Table 2 for 1.8 V operation | | | | |
| Output Voltage[2] | | | | | |
| High, $V_{OH}$ | $I_{SOURCE}$ = 200 µA | 0.8 × IOVDD | | | V |
| Low, $V_{OL}$ | $I_{SINK}$ = 400 µA | | | 0.4 | V |
| Leakage Current | Floating state | −10 | | +10 | µA |
| Output Capacitance | Floating state | | 10 | | pF |
| SYSTEM CALIBRATION[2] | | | | | |
| Full-Scale Calibration Limit | | | | 1.05 × $V_{REF}$ | V |
| Zero-Scale Calibration Limit | | −1.05 × $V_{REF}$ | | | V |
| Input Span | | 0.4 × $V_{REF}$ | | 2.1 × $V_{REF}$ | V |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER REQUIREMENTS | | | | | |
| Power Supply Voltage | | | | | |
| AVDD1 − AVSS | | 4.5 | 5.0 | 5.5 | V |
| AVDD2 − AVSS | | 2.0 | 2.25 to 5.0 | 5.5 | V |
| AVSS − DGND | | −2.75 | | 0 | V |
| IOVDD − DGND | See Table 2 for 1.8 V operation | 2.25 | 2.5 to 3.3 | 3.6 | V |
| POWER SUPPLY CURRENTS | Maximum output data rate, CMOS MCLK, eight DOUTx signals, all supplies at maximum voltages | | | | |
| Eight Channels Active | | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 36\|\|57.5 | 40\|\|64 | mA |
| AVDD2 Current | | | 37.5 | 40 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 27\|\|63 | 28\|\|67 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 18.5\|\|29 | 20.5\|\|32.5 | mA |
| AVDD2 Current | | | 21.3 | 23 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 16\|\|34 | 18\|\|37 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 5.1\|\|8 | 5.8\|\|9 | mA |
| AVDD2 Current | | | 9.3 | 10.1 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 8\|\|12.5 | 9\|\|13.7 | mA |
| Four Channels Active[2] | | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 18.2\|\|28.8 | 20.3\|\|32.5 | mA |
| AVDD2 Current | | | 18.8 | 20.3 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 17\|\|37 | 18.6\|\|40 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 9.3\|\|14.7 | 10.5\|\|16.6 | mA |
| AVDD2 Current | | | 10.7 | 11.7 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 11\|\|21 | 12.3\|\|23 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 2.7\|\|4.1 | 3.1\|\|4.7 | mA |
| AVDD2 Current | | | 4.7 | 5.3 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 6.5\|\|9 | 7.6\|\|10 | mA |
| Two Channels Active[2] | | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 9.3\|\|14.7 | 10.5\|\|16.6 | mA |
| AVDD2 Current | | | 9.5 | 10.5 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 11.9\|\|23.4 | 13.3\|\|25.5 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 4.8\|\|7.5 | 5.5\|\|8.6 | mA |
| AVDD2 Current | | | 5.5 | 6.2 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 8.5\|\|14.1 | 9.6\|\|15.5 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 1.52\|\|2.2 | 1.77\|\|2.6 | mA |
| AVDD2 Current | | | 2.4 | 3 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 5.8\|\|7.2 | 6.7\|\|8 | mA |
| Standby Mode | All channels disabled (sinc5 filter enabled) | | 6.5 | 8 | mA |
| Sleep Mode | Full power-down (SPI mode only) | | 0.73 | | mA |
| Crystal Excitation Current | Extra current in IOVDD when using an external crystal compared to using the CMOS MCLK | | 540 | | μA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER DISSIPATION | External CMOS MCLK, all channels active, MCLK = 32.768 MHz | | | | |
| Full Operating Mode | Analog precharge buffers on | | | | |
| Wideband Filter | | | | | |
| Fast | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2] | | 412 | 446 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2] | | 600 | 645 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V | | 631 | 681 | mW |
| Median | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2] | | 220 | 240 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2] | | 320 | 345 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V | | 341 | 372 | mW |
| Eco | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2] | | 75 | 85 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2] | | 107 | 118 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V | | 124 | 137 | mW |
| Sinc5 Filter | | | | | |
| Fast | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2] | | 325 | 355 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2] | | 475 | 525 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V | | 501 | 541 | mW |
| Median | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2] | | 175 | 195 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2] | | 260 | 285 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V | | 277 | 304 | mW |
| Eco | AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2] | | 65 | 72 | mW |
| | AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2] | | 95 | 105 | mW |
| | AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V | | 108 | 120 | mW |
| Standby Mode | All channels disabled (sinc5 filter enabled), AVDD1 = 5.5 V, AVDD2 = IOVDD = 2.5 V[2] | | | 18 | mW |
| | AVDD1 = 5.5 V, AVDD2 = IOVDD = 3.3 V[2] | | | 26 | mW |
| | AVDD1 = AVDD2 = 5.5 V, IOVDD = 3.6 V | | | 29 | mW |
| Sleep Mode | Full power-down (SPI mode only), AVDD1 = 5.5 V, AVDD2 = IOVDD = 2.5 V[2] | | 1.9 | | mW |
| | AVDD1 = 5.5 V,.AVDD2 = IOVDD = 3.3 V[2] | | 2.5 | | mW |
| | AVDD1 = AVDD2 = 5.5 V, IOVDD = 3.6 V | | 2.7 | | mW |

[1] The output data rate ranges refer to the programmable decimation rates available on the AD7768 for a fixed MCLK rate of 32.768 MHz. Varying MCLK rates allow users a wider variation of ODR.
[2] These specifications are not production tested but are supported by characterization data at initial product release.
[3] Following a system zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.
[4] −25 µA is measured when the analog input is close to either the AVDD1 or AVSS rail. The input current reduces as the common-mode voltage approaches (AVDD1 − AVSS)/2. The analog input current scales with the MCLK frequency and device power mode. See Figure 87 for more details.
[5] For lower MCLK rates or higher decimation rates, use Table 31 and Table 32 to calculate any additional delay before the first $\overline{\text{DRDY}}$ pulse.
[6] The $\overline{\text{RESET}}$ pin has an internal pull-up device to IOVDD.

## 1.8 V IOVDD SPECIFICATIONS

AVDD1A = AVDD1B = 4.5 V to 5.5 V, AVDD2A = AVDD2B = 2.0 V to 5.5 V, IOVDD = 1.72 V to 1.88 V, AVSS = DGND = 0 V, REFx+ = 4.096 V and REFx− = 0 V, MCLK = 32.76 8 MHz, analog precharge buffers on, reference precharge buffers off, wideband filter, $f_{CHOP}$ = $f_{MOD}$/32, $T_A$ = −40°C to +105°C, unless otherwise noted.

**Table 2.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | For dynamic range and SNR across all decimation rates, see Table 11 and Table 12 | | | | |
| Fast | Decimation by 32, 256 kSPS ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| SNR | 1 kHz, −0.5 dBFS, sine wave input | | | | |
| | Sinc5 filter | 109 | 111 | | dB |
| | Wideband filter | 106 | 107.8 | | dB |
| SINAD[1] | | 103.4 | 106.9 | | dB |
| THD | | | −120 | −107 | dB |
| SFDR | | | 128 | | dBc |
| Median | Decimation by 32, 128 kHz ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| SNR | 1 kHz, −0.5 dBFS, sine wave input | | | | |
| | Sinc5 filter | 109 | 111 | | dB |
| | Wideband filter | 106 | 107.8 | | dB |
| SINAD | | 105.3 | 106.9 | | dB |
| THD | | | −120 | −113 | dB |
| SFDR | | | 128 | | dBc |
| Eco | Decimation by 32, 32 kHz ODR | | | | |
| Dynamic Range | Shorted input, wideband filter | 106.2 | 108 | | dB |
| SNR | 1 kHz, −0.5 dBFS, sine wave input | | | | |
| | Sinc5 filter | 109 | 111 | | dB |
| | Wideband filter | 106 | 107.8 | | dB |
| SINAD | | 105.3 | 106.9 | | dB |
| THD | | | −120 | −113 | dB |
| SFDR | | | 128 | | dBc |
| ACCURACY[1] | | | | | |
| INL | Endpoint method | | ±2 | ±7 | ppm of FSR |
| Offset Error[2] | DCLK frequency ≤ 24 MHz | | ±50 | ±115 | µV |
| | 24 MHz to 32.768 MHz DCLK frequency | | ±75 | ±170 | µV |
| Offset Error Drift | DCLK frequency ≤ 24 MHz | | ±250 | | nV/°C |
| | 24 MHz to 32.768 MHz DCLK frequency | | ±750 | | nV/°C |
| Gain Error | $T_A$ = 25°C | | ±60 | ±120 | ppm/FSR |
| Gain Drift vs. Temperature | | | ±0.5 | ±2 | ppm/°C |
| LOGIC INPUTS | | | | | |
| Input Voltage[1] | | | | | |
| High, $V_{INH}$ | | 0.65 × IOVDD | | | V |
| Low, $V_{INL}$ | | | | 0.4 | V |
| Hysteresis[1] | | 0.04 | | 0.2 | V |
| Leakage Current | | −10 | +0.03 | +10 | µA |
| | $\overline{RESET}$ pin | −10 | | +10 | µA |
| LOGIC OUTPUTS | | | | | |
| Output Voltage[1] | | | | | |
| High, $V_{OH}$ | $I_{SOURCE}$ = 200 µA | 0.8 × IOVDD | | | V |
| Low, $V_{OL}$ | $I_{SINK}$ = 400 µA | | | 0.4 | V |
| Leakage Current | Floating state | −10 | | +10 | µA |
| Output Capacitance | Floating state | | 10 | | pF |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER REQUIREMENTS | | | | | |
| Power Supply Voltage | | | | | |
| AVDD1 − AVSS | | 4.5 | 5.0 | 5.5 | V |
| AVDD2 − AVSS | | 2.0 | 2.25 to 5.0 | 5.5 | V |
| AVSS − DGND | | −2.75 | | 0 | V |
| IOVDD − DGND | DREGCAP shorted to IOVDD | 1.72 | 1.8 | 1.88 | V |
| POWER SUPPLY CURRENTS | Maximum output data rate, CMOS MCLK, eight DOUTx signals, all supplies at maximum voltages | | | | |
| Eight Channels Active | | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 36\|\|57.5 | 40\|\|64 | mA |
| AVDD2 Current | | | 37.5 | 40 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 26\|\|63 | 28.4\|\|69 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 18.5\|\|29 | 20.5\|\|32.5 | mA |
| AVDD2 Current | | | 21.3 | 23 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 15\|\|34 | 16.8\|\|36.8 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 5.1\|\|8 | 5.8\|\|9 | mA |
| AVDD2 Current | | | 9.3 | 10.1 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 7\|\|11.6 | 8.1\|\|12.9 | mA |
| Four Channels Active | | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 18.2\|\|28.8 | 20.3\|\|32.5 | mA |
| AVDD2 Current | | | 18.8 | 20.3 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 16\|\|44 | 17.7\|\|48 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 9.3\|\|14.7 | 10.5\|\|16.6 | mA |
| AVDD2 Current | | | 10.7 | 11.7 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 10\|\|24 | 11.3\|\|26.1 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 2.7\|\|4.1 | 3.1\|\|4.7 | mA |
| AVDD2 Current | | | 4.7 | 5.3 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 5.5\|\|9 | 6.5\|\|10.2 | mA |
| Two Channels Active | | | | | |
| Fast Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 9.3\|\|14.7 | 10.5\|\|16.6 | mA |
| AVDD2 Current | | | 9.5 | 10.5 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 11\|\|34 | 12.3\|\|37 | mA |
| Median Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 4.8\|\|7.5 | 5.5\|\|8.6 | mA |
| AVDD2 Current | | | 5.5 | 6.2 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 7.4\|\|19 | 8.6\|\|21 | mA |
| Eco Mode | | | | | |
| AVDD1 Current | Precharge reference buffers off\|\|on | | 1.52\|\|2.2 | 1.77\|\|2.6 | mA |
| AVDD2 Current | | | 2.4 | 3 | mA |
| IOVDD Current | Sinc5 filter\|\|wideband filter | | 4.8\|\|7.6 | 5.8\|\|8.8 | mA |
| Standby Mode | All channels disabled (sinc5 filter enabled) | | 6.5 | 8 | mA |
| Sleep Mode | Full power-down (SPI mode only) | | 0.73 | | mA |
| Crystal Excitation Current | Extra current in IOVDD when using an external crystal compared to using the CMOS MCLK | | 540 | | µA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER DISSIPATION[1] | External CMOS MCLK, all channels active, AVDD1 = AVDD2 = 5.5 V, IOVDD = 1.88 V, MCLK = 32.768 MHz | | | | |
| Full Operating Mode | Analog precharge buffers on | | | | |
| Wideband Filter | | | | | |
| Fast | Precharge reference buffers off | | 524 | 571 | mW |
| | Precharge reference buffers on | | 638 | 700 | mW |
| Median | Precharge reference buffers off | | 284 | 309 | mW |
| | Precharge reference buffers on | | 342 | 375 | mW |
| Eco | Precharge reference buffers off | | 98.5 | 109 | mW |
| | Precharge reference buffers on | | 118 | 130 | mW |
| Sinc5 Filter | | | | | |
| Fast | Precharge reference buffers off | | 455 | 495 | mW |
| Median | Precharge reference buffers off | | 248 | 271 | mW |
| Eco | Precharge reference buffers off | | 94 | 105 | mW |
| Standby Mode | All channels disabled (sinc5 filter enabled) | | | 29 | mW |
| Sleep Mode | Full power-down (SPI mode only) | | 1.5 | | mW |

[1] These specifications are not production tested but are supported by characterization data at initial product release.
[2] Following a system zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.

## TIMING SPECIFICATIONS

AVDD1A = AVDD1B = 5 V, AVDD2A = AVDD2B = 5 V, IOVDD = 2.25 V to 3.6 V, Input Logic 0 = DGND, Input Logic 1 = IOVDD; $C_{LOAD}$ = 10 pF on the DCLK pin, $C_{LOAD}$ = 20 pF on the other digital outputs; REFx+ = 4.096 V, $T_A$ = −40°C to +105°C. See Table 5 and Table 6 for timing specifications at 1.8 V IOVDD.

**Table 3. Data Interface Timing[1]**

| Parameter | Description | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MCLK | Master clock[2] | | 1.15 | | 34 | MHz |
| $f_{MOD}$ | Modulator frequency | Fast mode | | MCLK/4 | | Hz |
| | | Median mode | | MCLK/8 | | Hz |
| | | Eco mode | | MCLK/32 | | Hz |
| $t_1$ | $\overline{\text{DRDY}}$ high time | $t_{DCLK} = t_8 + t_9$ | $t_{DCLK}$ − 10% | 28 | | ns |
| $t_2$ | DCLK rising edge to $\overline{\text{DRDY}}$ rising edge | | | | 2 | ns |
| $t_3$ | DCLK rising to $\overline{\text{DRDY}}$ falling | | −3.5 | | 0 | ns |
| $t_4$ | DCLK rise to DOUTx valid | | | | 1.5 | ns |
| $t_5$ | DCLK rise to DOUTx invalid | | −3 | | | ns |
| $t_6$ | DOUTx valid to DCLK falling | | 9.5 | $t_{DCLK}/2$ | | ns |
| $t_7$ | DCLK falling edge to DOUTx invalid | | 9.5 | $t_{DCLK}/2$ | | ns |
| $t_8$ | DCLK high time, DCLK = MCLK/1 | 50:50 MCLK | $t_{DCLK}/2$ | $t_{DCLK}/2$ | $(t_{DCLK}/2) + 5$ | ns |
| | $t_{8a}$ = DCLK = MCLK/2 | $t_{MCLK}$ = 1/MCLK | | $t_{MCLK}$ | | ns |
| | $t_{8b}$ = DCLK = MCLK/4 | | | $2 \times t_{MCLK}$ | | ns |
| | $t_{8c}$ = DCLK = MCLK/8 | | | $4 \times t_{MCLK}$ | | ns |
| $t_9$ | DCLK low time DCLK=MCLK/1 | | $(t_{DCLK}/2) - 5$ | $t_{MCLK}/2$ | $t_{DCLK}/2$ | ns |
| | $t_{9a}$ = DCLK = MCLK/2 | | | $t_{MCLK}$ | | ns |
| | $t_{9b}$ = DCLK = MCLK/4 | | | $2 \times t_{MCLK}$ | | ns |
| | $t_{9c}$ = DCLK = MCLK/8 | | | $4 \times t_{MCLK}$ | | ns |
| $t_{10}$ | MCLK rising to DCLK rising | | | | 30 | ns |
| $t_{11}$ | Setup time DOUT6 and DOUT7 | | 14 | | | ns |
| $t_{12}$ | Hold time DOUT6 and DOUT7 | | 0 | | | ns |
| $t_{13}$ | $\overline{\text{START}}$ low time | | $1 \times t_{MCLK}$ | | | ns |
| $t_{14}$ | Falling edge of MCLK to $\overline{\text{SYNC\_OUT}}$ valid | Modulator delay disabled | 4.5 | | 22 | ns |
| | | Modulator delay enabled | 9.5 | | 27.5 | ns |
| $t_{15}$ | $\overline{\text{SYNC\_IN}}$ setup time | | 0 | | | ns |
| $t_{16}$ | $\overline{\text{SYNC\_IN}}$ hold time | | 10 | | | ns |

[1] These specifications are not production tested but are supported by characterization data at initial product release.
[2] Lower MCLK frequencies than specified can be used by disabling the clock qualifier check. See Table 39 for details.

**Table 4. SPI Control Interface Timing[1]**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{17}$ | SCLK period | 100 | | | ns |
| $t_{18}$ | $\overline{\text{CS}}$ falling edge to SCLK rising edge | 26.5 | | | ns |
| $t_{19}$ | SCLK falling edge to $\overline{\text{CS}}$ rising edge | 27 | | | ns |
| $t_{20}$ | $\overline{\text{CS}}$ falling edge to data output enable | 22.5 | | 40.5 | ns |
| $t_{21}$ | SCLK high time | 20 | 50 | | ns |
| $t_{22}$ | SCLK low time | 20 | 50 | | ns |
| $t_{23}$ | SCLK falling edge to SDO valid | | | 15 | ns |
| $t_{24}$ | SDO hold time after SCLK falling | 7 | | | ns |
| $t_{25}$ | SDI setup time | 0 | | | ns |
| $t_{26}$ | SDI hold time | 6 | | | ns |
| $t_{27}$ | SCLK enable time | 0 | | | ns |
| $t_{28}$ | SCLK disable time | 0 | | | ns |
| $t_{29}$ | $\overline{\text{CS}}$ high time | 10 | | | ns |

[1] These specifications are not production tested but are supported by characterization data at initial product release.

## 1.8 V IOVDD TIMING SPECIFICATIONS

AVDD1A = AVDD1B = 5 V, AVDD2A = AVDD2B = 5 V, IOVDD = 1.72 V to 1.88 V (DREGCAP tied to IOVDD), Input Logic 0 = DGND, Input Logic 1 = IOVDD, $C_{LOAD}$ = 10 pF on DCLK pin, $C_{LOAD}$ = 20 pF on other digital outputs, $T_A$ = −40°C to +105°C.

**Table 5. Data Interface Timing[1]**

| Parameter | Description | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MCLK | Master clock[2] | | 1.15 | | 34 | MHz |
| $f_{MOD}$ | Modulator frequency | Fast mode | | MCLK/4 | | Hz |
| | | Median mode | | MCLK/8 | | Hz |
| | | Eco mode | | MCLK/32 | | Hz |
| $t_1$ | DRDY high time | | $t_{DCLK}$ − 10% | 28 | | ns |
| $t_2$ | DCLK rising edge to DRDY rising edge | | | | 2 | ns |
| $t_3$ | DCLK rising to DRDY falling | | −4.5 | | 0 | ns |
| $t_4$ | DCLK rise to DOUTx valid | | | | 2.0 | ns |
| $t_5$ | DCLK rise to DOUTx invalid | | −4 | | | ns |
| $t_6$ | DOUTx valid to DCLK falling | | 8.5 | $t_{DCLK}$/2 | | ns |
| $t_7$ | DCLK falling edge to DOUTx invalid | | 8.5 | $t_{DCLK}$/2 | | ns |
| $t_8$ | DCLK high time, DCLK = MCLK/1 | 50:50 MCLK | $t_{DCLK}$/2 | $t_{DCLK}$/2 | ($t_{DCLK}$/2) + 5 | ns |
| | $t_{8a}$ = DCLK = MCLK/2 | | | $t_{MCLK}$ | | ns |
| | $t_{8b}$ = DCLK = MCLK/4 | | | 2 × $t_{MCLK}$ | | ns |
| | $t_{8c}$ = DCLK = MCLK/8 | | | 4 × $t_{MCLK}$ | | ns |
| $t_9$ | DCLK low time DCLK=MCLK/1 | | ($t_{DCLK}$/2) − 5 | $t_{MCLK}$/2 | ($t_{DCLK}$/2 | ns |
| | $t_{9a}$ = DCLK = MCLK/2 | | | $t_{MCLK}$ | | ns |
| | $t_{9b}$ = DCLK = MCLK/4 | | | 2 × $t_{MCLK}$ | | ns |
| | $t_{9c}$ = DCLK = MCLK/8 | | | 4 × $t_{MCLK}$ | | ns |
| $t_{10}$ | MCLK rising to DCLK rising | | | | 37 | ns |
| $t_{11}$ | Setup time DOUT6 and DOUT7 | | 14 | | | ns |
| $t_{12}$ | Hold time DOUT6 and DOUT7 | | 0 | | | ns |
| $t_{13}$ | START low time | | 1 × $t_{MCLK}$ | | | ns |
| $t_{14}$ | Falling edge of MCLK to SYNC_OUT valid | Modulator delay disabled | 10 | | 31 | ns |
| | | Modulator delay enabled | 15 | | 37 | |
| $t_{15}$ | SYNC_IN setup time | | 0 | | | ns |
| $t_{16}$ | SYNC_IN hold time | | 11 | | | ns |

[1] These specifications are not production tested but are supported by characterization data at initial product release.
[2] Lower MCLK frequencies than specified can be used by disabling the clock qualifier check. See Table 39 for details.

**Table 6. SPI Control Interface Timing[1]**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{17}$ | SCLK period | 100 | | | ns |
| $t_{18}$ | CS falling edge to SCLK rising edge | 31.5 | | | ns |
| $t_{19}$ | SCLK falling edge to CS rising edge | 30 | | | ns |
| $t_{20}$ | CS falling edge to data output enable | 29 | | 54 | ns |
| $t_{21}$ | SCLK high time | 20 | 50 | | ns |
| $t_{22}$ | SCLK low time | 20 | 50 | | ns |
| $t_{23}$ | SCLK falling edge to SDO valid | | | 16 | ns |
| $t_{24}$ | SDO hold time after SCLK falling | 7 | | | ns |
| $t_{25}$ | SDI setup time | 0 | | | ns |
| $t_{26}$ | SDI hold time | 10 | | | ns |
| $t_{27}$ | SCLK enable time | 0 | | | ns |
| $t_{28}$ | SCLK disable time | 0 | | | ns |
| $t_{29}$ | CS high time | 10 | | | ns |

[1] These specifications are not production tested but are supported by characterization data at initial product release.

### *Timing Diagrams*

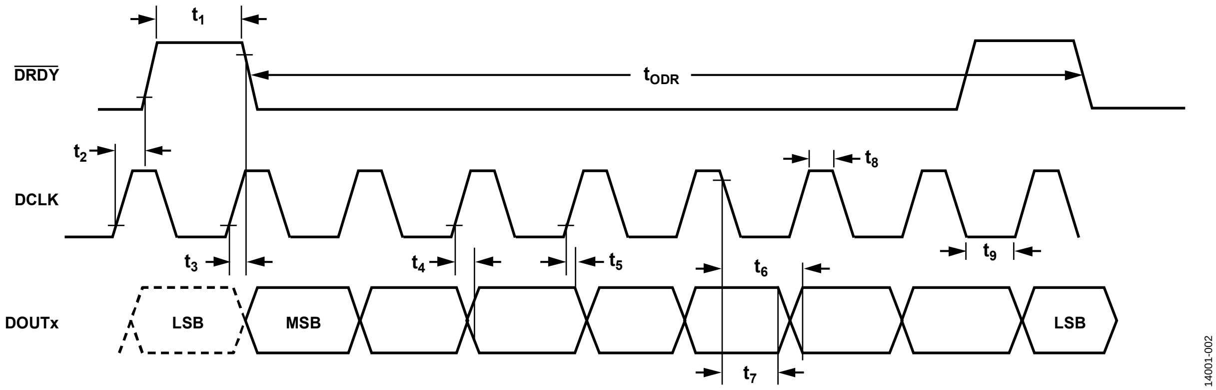



*Figure 2. Data Interface Timing Diagram*

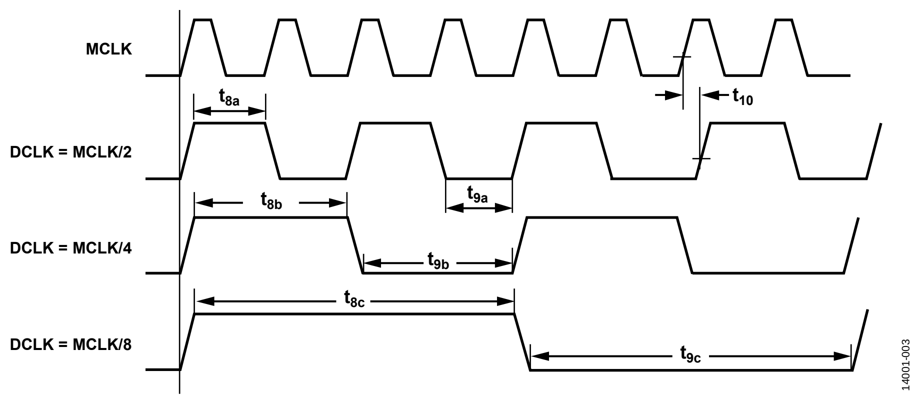



*Figure 3. MCLK to DCLK Divider Timing Diagram*

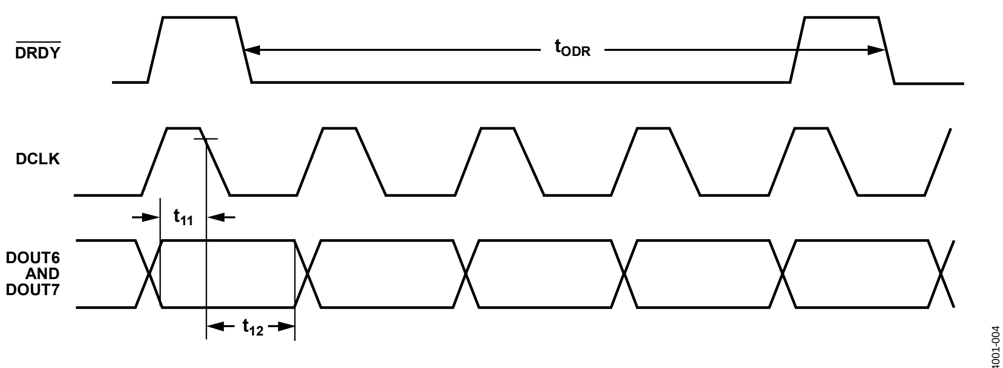



*Figure 4. Daisy-Chain Setup and Hold Timing Diagram*

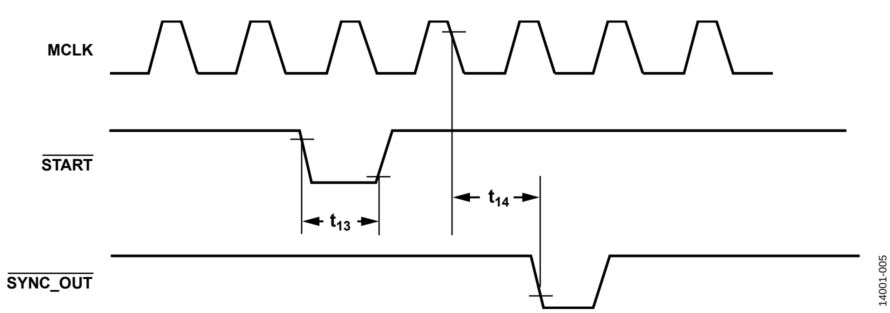



*Figure 5. Asynchronous $\overline{\text{START}}$ and $\overline{\text{SYNC\_OUT}}$ Timing Diagram*

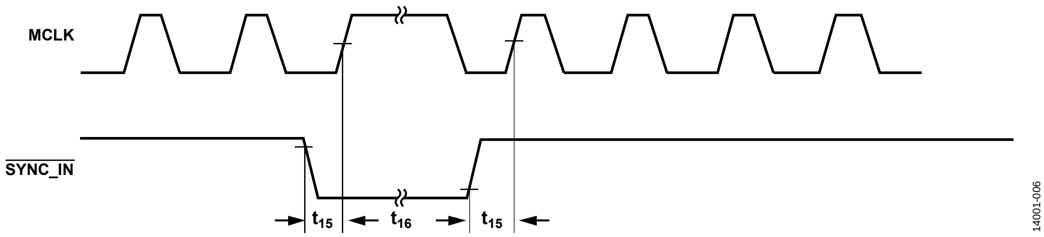



Figure 6. Synchronous SYNC_IN Pulse Timing Diagram

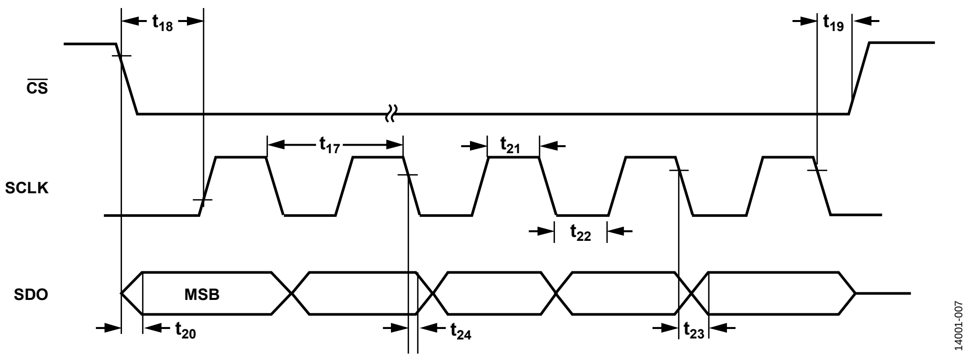



Figure 7. SPI Serial Read Timing Diagram

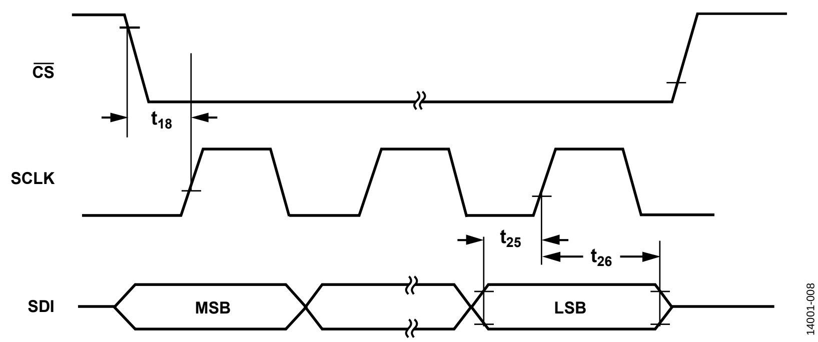



Figure 8. SPI Serial Write Timing Diagram

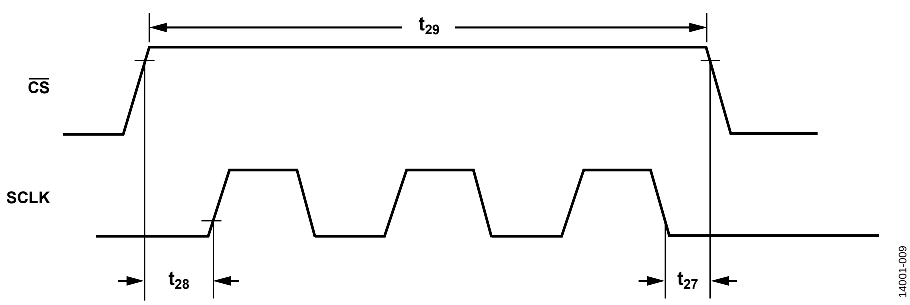



Figure 9. SCLK Enable and Disable Timing Diagram

# ABSOLUTE MAXIMUM RATINGS

**Table 7.**

| Parameter | Rating |
|---|---|
| AVDD1, AVDD2 to AVSS[1] | −0.3 V to +6.5 V |
| AVDD1 to DGND | −0.3 V to +6.5 V |
| IOVDD to DGND | −0.3 V to +6.5 V |
| IOVDD, DREGCAP to DGND (IOVDD Tied to DREGCAP for 1.8 V Operation) | −0.3 V to +2.25 V |
| IOVDD to AVSS | −0.3 V to +7.5 V |
| AVSS to DGND | −3.25 V to +0.3 V |
| Analog Input Voltage to AVSS | −0.3 V to AVDD1 + 0.3 V |
| Reference Input Voltage to AVSS | −0.3 V to AVDD1 + 0.3 V |
| Digital Input Voltage to DGND | −0.3 V to IOVDD + 0.3 V |
| Digital Output Voltage to DGND | −0.3 V to IOVDD + 0.3 V |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Pb-Free Temperature, Soldering Reflow (10 sec to 30 sec) | 260°C |
| Maximum Junction Temperature | 150°C |
| Maximum Package Classification Temperature | 260°C |

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

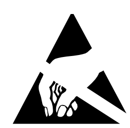
## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 8. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit | JEDEC Board Layers |
|---|---|---|---|---|
| 64-Lead LQFP | 38 | 9.2 | °C/W | 2P2S |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

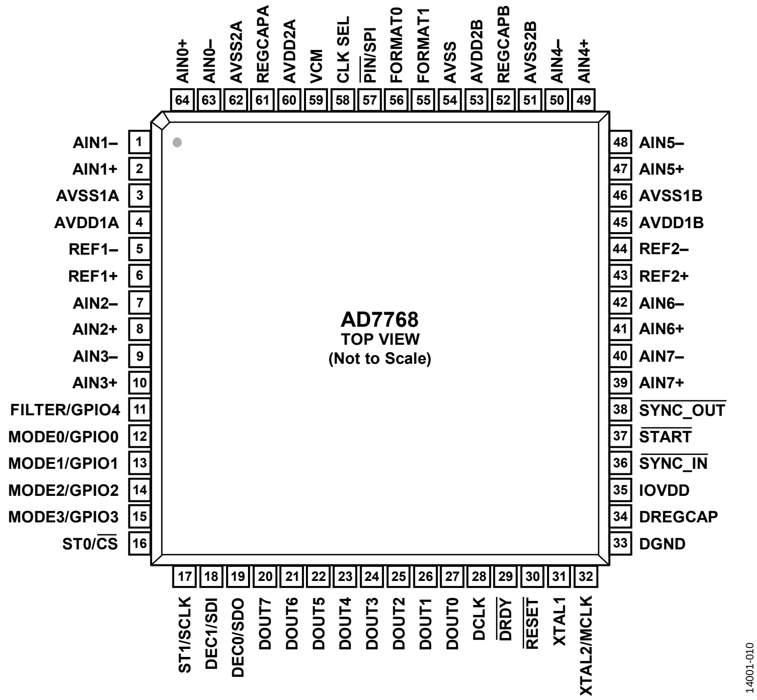



*Figure 10. Pin Configuration*

**Table 9. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 1 | AIN1− | AI | Negative Analog Input to ADC Channel 1. |
| 2 | AIN1+ | AI | Positive Analog Input to ADC Channel 1. |
| 3 | AVSS1A | P | Negative Analog Supply. This pin is nominally 0 V. |
| 4 | AVDD1A | P | Analog Supply Voltage, 5 V ± 10% with Respect to AVSS. |
| 5 | REF1− | AI | Reference Input Negative. REF1− is the negative reference terminal for Channel 0 to Channel 3. The REF1− voltage range is from AVSS to (AVDD1 − 1 V). Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3. |
| 6 | REF1+ | AI | Reference Input Positive. REF1+ is the positive reference terminal for Channel 0 to Channel 3. The REF1+ voltage range is from (AVSS + 1 V) to AVDD1. Apply an external reference differential between REF1+ and REF1− in the range from 1 V to \|AVDD1 − AVSS\|. Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3. |
| 7 | AIN2− | AI | Negative Analog Input to ADC Channel 2. |
| 8 | AIN2+ | AI | Positive Analog Input to ADC Channel 2. |
| 9 | AIN3− | AI | Negative Analog Input to ADC Channel 3. |
| 10 | AIN3+ | AI | Positive Analog Input to ADC Channel 3. |
| 11 | FILTER/GPIO4 | DI/O | Filter Select/General-Purpose Input/Output 4. In pin control mode, this pin selects the filter type.<br>Set this pin to Logic 1 for the sinc5 filter. This sinc5 filter is a low latency filter, and is best for dc applications or where a user has specialized post filtering implemented off-chip.<br>Set this pin to Logic 0 for the wideband low ripple filter response. This filter has a steep transition band and 105 dB stop band attenuation. Full attenuation at Nyquist (ODR/2) means that no aliasing occurs at ODR/2 out to the first chopping zone.<br>When in SPI control mode, this pin can be used as a general-purpose input/output (GPIO4). See Table 45 for more details. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 12, 13, 14, 15 | MODE0/GPIO0, MODE1/GPIO1, MODE2/GPIO2, MODE3/GPIO3 | DI/DI/O | Mode Selection/General-Purpose Input/Output Pin 0 to Pin 3. In pin control mode, the MODEx pins set the mode of operation for all ADC channels, controlling power consumption, DCLK frequency, and the ADC conversion type, allowing one-shot conversion operation. In SPI control mode, the GPIOx pins, in addition to the FILTER/GPIO4 pin, form five general-purpose input/output pins (GPIO4 to GPIO0). See Table 45 for more details. |
| 16 | ST0/$\overline{\text{CS}}$ | DI | Standby 0/Chip Select Input. In pin control mode, a Logic 1 places Channel 0 to Channel 3 into standby mode. In SPI control mode, this pin is the active low chip select input to the SPI control interface. |
| 17 | ST1/SCLK | DI | Standby 1/Serial Clock Input. In pin control mode, a Logic 1 places Channel 4 to Channel 7 into standby mode. In SPI control mode, this pin is the serial clock input pin for the SPI control interface. |
| 18 | DEC1/SDI | DI | Decimation Rate Control Input 1/Serial Data Input. In pin control mode, the DEC0 and DEC1 pins configure the decimation rate for all ADC channels. See Table 16 in the Setting the Decimation Rate section for more information. In SPI control mode, this pin is the serial data input pin used to write data to the AD7768 register bank. |
| 19 | DEC0/SDO | DI/O | Decimation Rate Control Input 0/Serial Data Output. In pin control mode, the DEC0 and DEC1 pins configure the decimation rate for all ADC channels. See Table 16 in the Setting the Decimation Rate section for more information. In SPI control mode, this pin is the serial data output pin, allowing readback from the AD7768 registers. |
| 20 | DOUT7 | DI/O | Conversion Data Output 7. This pin is synchronous to DCLK and framed by $\overline{\text{DRDY}}$. This pin acts as a digital input from a separate AD7768 device if configured in a synchronized multidevice daisy chain when the FORMATx pins are configured as 01. To use the AD7768 in a daisy chain, hardwire the FORMATx pins as either 01, 10, or 11, depending on the best interfacing format for the application. When FORMATx is set to 10 or 11, connect this pin to ground through a pull-down resistor. |
| 21 | DOUT6 | DI/O | Conversion Data Output 6. This pin is synchronous to DCLK and framed by $\overline{\text{DRDY}}$. This pin acts as a digital input from a separate AD7768 device if configured in a synchronized multidevice daisy chain. To use this pin in a daisy chain, hardwire the FORMATx pins as either 01, 10, or 11, depending on the best interfacing format for the application. |
| 22 | DOUT5 | DO | Conversion Data Output 5. This pin is synchronous to DCLK and framed by $\overline{\text{DRDY}}$. |
| 23 | DOUT4 | DO | Conversion Data Output 4. This pin is synchronous to DCLK and framed by $\overline{\text{DRDY}}$. |
| 24 | DOUT3 | DO | Conversion Data Output 3. This pin is synchronous to DCLK and framed by $\overline{\text{DRDY}}$. |
| 25 | DOUT2 | DO | Conversion Data Output 2. This pin is synchronous to DCLK and framed by $\overline{\text{DRDY}}$. |
| 26 | DOUT1 | DO | Conversion Data Output 1. This pin is synchronous to DCLK and framed by $\overline{\text{DRDY}}$. |
| 27 | DOUT0 | DO | Conversion Data Output 0. This pin is synchronous to DCLK and framed by $\overline{\text{DRDY}}$ |
| 28 | DCLK | DO | ADC Conversion Data Clock. This pin clocks conversion data out to the digital host (DSP/FPGA). This pin is synchronous with $\overline{\text{DRDY}}$ and any conversion data output on DOUT0 to DOUT7 and is derived from the MCLK signal. This pin is unrelated to the control SPI interface. |
| 29 | $\overline{\text{DRDY}}$ | DO | Data Ready. Periodic signal output framing the conversion results from the eight ADCs. This pin is synchronous to DCLK and DOUT0 to DOUT7. |
| 30 | $\overline{\text{RESET}}$ | DI | Hardware Asynchronous Reset Input. After the device is fully powered up, it is recommended to perform a hard or soft reset. |
| 31 | XTAL1 | DI | Input 1 for Crystal or Connection to an LVDS Clock. When CLK_SEL is 0, connect XTAL1 to DGND. |
| 32 | XTAL2/MCLK | DI | Input 2 for CMOS/Crystal/LVDS Sampling Clock. See the CLK_SEL pin for the details of this configuration. External crystal: XTAL2 is connected to the external crystal. LVDS: a second LVDS input is connected to this pin. CMOS clock: this pin operates as an MCLK input. CMOS input with logic level of IOVDD/DGND. |
| 33 | DGND | P | Digital Ground. This pin is nominally 0 V. |
| 34 | DREGCAP | AO | Digital LDO Regulator Output. Decouple this pin to DGND with a high quality, low ESR, 10 µF capacitor. For optimum performance, use a decoupling capacitor with an ESR specification between 50 mΩ and 400 mΩ. This pin is not for use in circuits external to the AD7768. For 1.8 V IOVDD operation, connect this pin to IOVDD via an external trace to provide power to the digital processing core. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 35 | IOVDD | P | Digital Supply. This pin sets the logic levels for all interface pins. IOVDD also powers the digital processing core via the digital LDO when IOVDD is at least 2.25 V. For 1.8 V IOVDD operation, connect this pin to DREGCAP via an external trace to provide power to the digital processing core. |
| 36 | $\overline{\text{SYNC\_IN}}$ | DI | Synchronization Input. $\overline{\text{SYNC\_IN}}$ receives the synchronous signal from $\overline{\text{SYNC\_OUT}}$. It is used in the synchronization of any AD7768 that requires simultaneous sampling or is in a daisy chain. Ignore the $\overline{\text{START}}$ and $\overline{\text{SYNC\_OUT}}$ functions if the $\overline{\text{SYNC\_IN}}$ pin is connected to the system synchronization pulse. This signal pulse must be synchronous to the MCLK clock domain. |
| 37 | $\overline{\text{START}}$ | DI | Start Signal. The $\overline{\text{START}}$ pulse synchronizes the AD7768 to other devices. The signal can be asynchronous. The AD7768 samples the input and then outputs a $\overline{\text{SYNC\_OUT}}$ pulse. This $\overline{\text{SYNC\_OUT}}$ pulse must be routed to the $\overline{\text{SYNC\_IN}}$ pin of this device, and any other AD7768 devices that must be synchronized together. This means that the user does not need to run the ADCs and their digital host from the same clock domain, which is useful when there are long traces or back planes between the ADC and the controller. If this pin is not used, it must be tied to a Logic 1 through a pull-up resistor. |
| 38 | $\overline{\text{SYNC\_OUT}}$ | DO | Synchronization Output. This pin operates only when the $\overline{\text{START}}$ input is used. When using the $\overline{\text{START}}$ input feature, the $\overline{\text{SYNC\_OUT}}$ pin must be connected to $\overline{\text{SYNC\_IN}}$ via an external trace. $\overline{\text{SYNC\_OUT}}$ is a digital output that is synchronous to the MCLK signal; the synchronization signal driven in on $\overline{\text{START}}$ is internally synchronized to the MCLK signal and is driven out on $\overline{\text{SYNC\_OUT}}$. $\overline{\text{SYNC\_OUT}}$ may also be routed to other AD7768 devices requiring simultaneous sampling and/or daisy-chaining, ensuring synchronization of devices related to the MCLK clock domain. It must then be wired to drive the $\overline{\text{SYNC\_IN}}$ pin on the same AD7768 and on the other AD7768 devices. |
| 39 | AIN7+ | AI | Positive Analog Input to ADC Channel 7. |
| 40 | AIN7− | AI | Negative Analog Input to ADC Channel 7. |
| 41 | AIN6+ | AI | Positive Analog Input to ADC Channel 6. |
| 42 | AIN6− | AI | Negative Analog Input to ADC Channel 6. |
| 43 | REF2+ | AI | Reference Input Positive. REF2+ is the positive reference terminal for Channel 4 to Channel 7. The REF2+ voltage range is from (AVSS + 1 V) to AVDD1. Apply an external reference differential between REF2+ and REF2− in the range from 1 V to \|AVDD1 − AVSS\|. Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 46. |
| 44 | REF2− | AI | Reference Input Negative. REF2− is the negative reference terminal for Channel 4 to Channel 7. The REF2− voltage range is from AVSS to (AVDD1 − 1 V). Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 46. |
| 45 | AVDD1B | P | Analog Supply Voltage. This pin is 5 V ± 10% with respect to AVSS. |
| 46 | AVSS1B | P | Negative Analog Supply. This pin is nominally 0 V. |
| 47 | AIN5+ | AI | Positive Analog Input to ADC Channel 5. |
| 48 | AIN5− | AI | Negative Analog Input to ADC Channel 5. |
| 49 | AIN4+ | AI | Positive Analog Input to ADC Channel 4. |
| 50 | AIN4− | AI | Negative Analog Input to ADC Channel 4. |
| 51 | AVSS2B | P | Negative Analog Supply. This pin is nominally 0 V. |
| 52 | REGCAPB | AO | Analog LDO Regulator Output. Decouple this pin to AVSS with a 1 μF capacitor. |
| 53 | AVDD2B | P | Analog Supply Voltage. This pin is 2 V to 5.5 V with respect to AVSS. |
| 54 | AVSS | P | Negative Analog Supply. This pin is nominally 0 V. |
| 55, 56 | FORMAT1, FORMAT0 | DI | Format Selection Pins. Hardwire the FORMATx pins to the required values in pin and SPI mode. These pins set the number of DOUTx pins used to output ADC conversion data. The FORMATx pins are checked by the AD7768 on power up; the AD7768 then remains in this data output configuration (see Table 28). |
| 57 | $\overline{\text{PIN}}$/SPI | DI | Pin Control/SPI Control. This pin sets the control method.<br>Logic 0 = pin control mode for the AD7768. Pin control mode allows pin strapped configuration of the AD7768 by tying logic input pins to required logic levels. Tie the logic pins (MODE0 to MODE4, DEC0 and DEC1, and FILTER) as required for the configuration. See the Pin Control section for more details.<br>Logic 1 = SPI control mode for the AD7768. Use the SPI control interface signals ($\overline{\text{CS}}$, SCLK, SDI, and SDO) for reading and writing to the AD7768 memory map. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 58 | CLK_SEL | DI | Clock Select.<br>0 = pull this pin low for the CMOS clock option. The clock is applied to Pin 32 (Connect Pin 31 to DGND).<br>1 = pull this pin high for the crystal or LVDS clock option. The crystal or LVDS clock is applied to Pin 31 and Pin 32. The LVDS option is available only in SPI control mode. A write is required to enable the LVDS clock option. |
| 59 | VCM | AO | Common-Mode Voltage Output. This pin outputs (AVDD1 − AVSS)/2, which is 2.5 V by default in pin control mode. Configure this pin to (AVDD1 − AVSS)/2, 2.5 V, 2.14 V, or 1.65 V in SPI mode. When driving capacitive loads larger than 0.1 µF, it is recommended to place a 50 Ω series resistor between the pin and the capacitive load for stability. |
| 60 | AVDD2A | P | Analog Supply Voltage. This pin is 2 V to 5.5 V with respect to AVSS. |
| 61 | REGCAPA | AO | Analog LDO Regulator Output. Decouple this pin to AVSS with a 1 µF capacitor. |
| 62 | AVSS2A | P | Negative Analog Supply. This pin is nominally 0 V. |
| 63 | AIN0− | AI | Negative Analog Input to ADC Channel 0. |
| 64 | AIN0+ | AI | Positive Analog Input to ADC Channel 0. |

[1] AI is analog input, P is power, DI/O is digital input/output, DI is digital input, DO is digital output, and AO is analog output.

# TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 5 V, AVDD2 = 2.5 V, AVSS = 0 V, IOVDD = 2.5 V, $V_{REF}$ = 4.096 V, $T_A$ = 25°C, wideband filter, decimation = ×32, MCLK = 32.768 MHz, analog input precharge buffers on, precharge reference buffers off, unless otherwise noted.

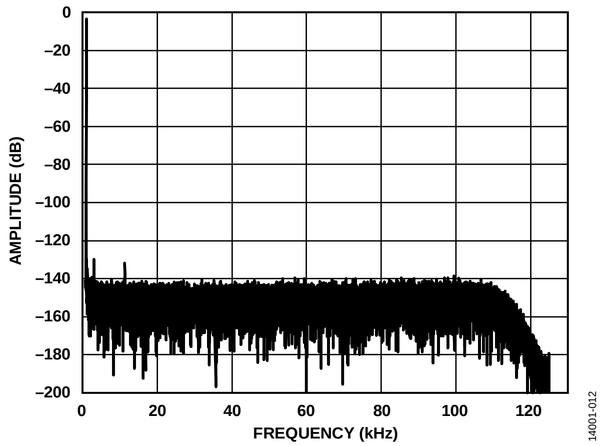



*Figure 11. FFT, Fast Mode, Wideband Filter, −0.5 dBFS*

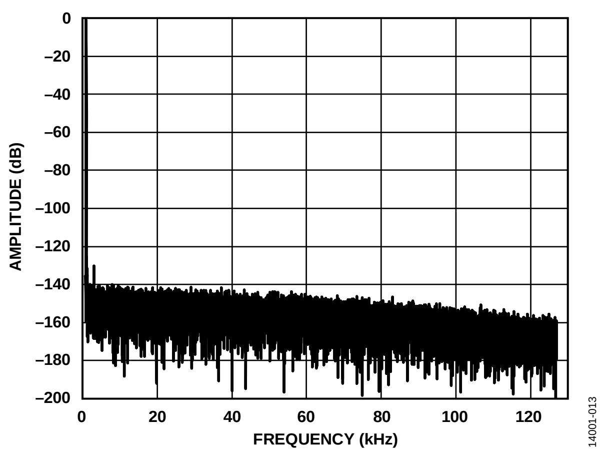



*Figure 12. FFT, Fast Mode, Sinc5 Filter, −0.5 dBFS*

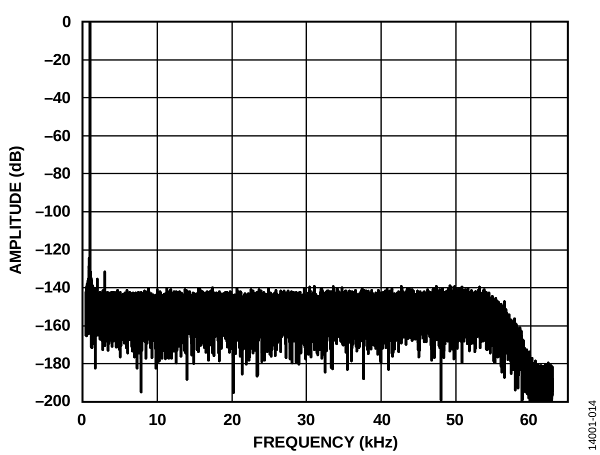



*Figure 13. FFT, Median Mode, Wideband Filter, −0.5 dBFS*

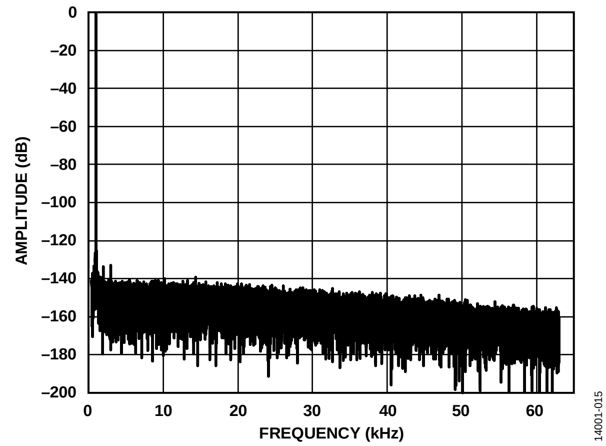



*Figure 14. FFT, Median Mode, Sinc5 Filter, −0.5 dBFS*

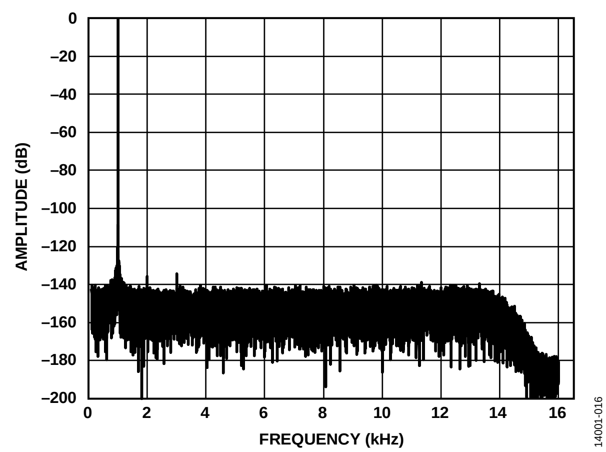



*Figure 15. FFT, Eco Mode, Wideband Filter, −0.5 dBFS*

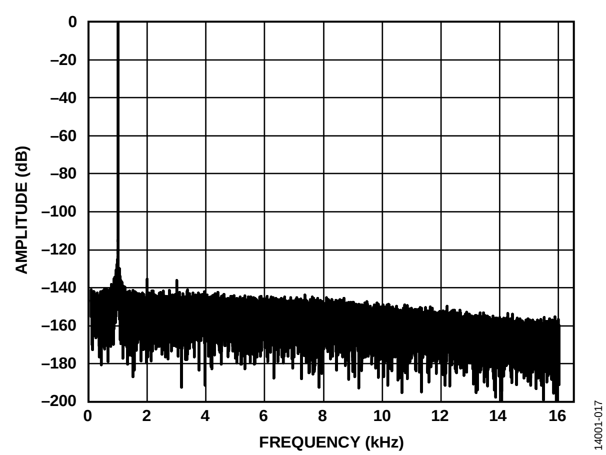



*Figure 16. FFT, Eco Mode, Sinc5 Filter, −0.5 dBFS*

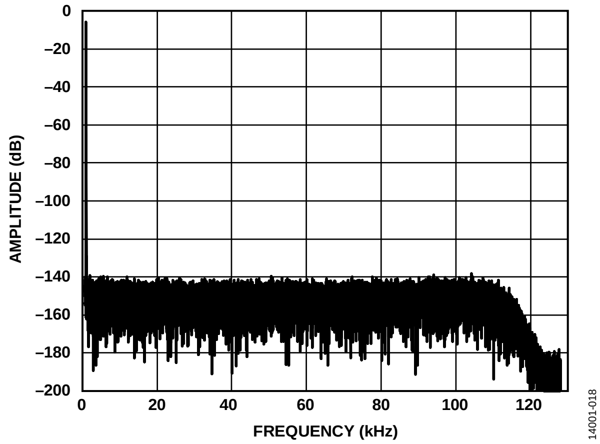



*Figure 17. FFT, Fast Mode, Wideband Filter, –6 dBFS*

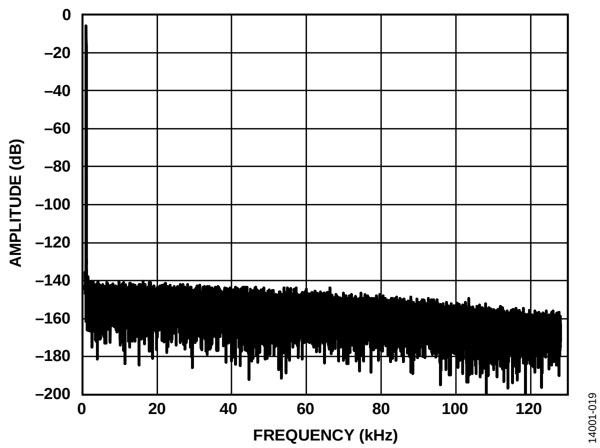



*Figure 18. FFT, Fast Mode, Sinc5 Filter, –6 dBFS*

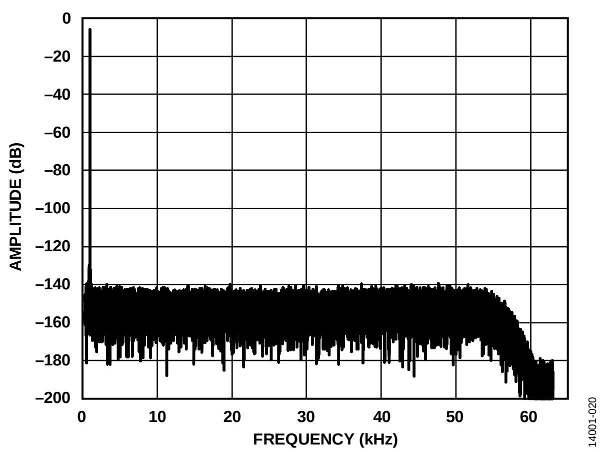



*Figure 19. FFT, Median Mode, Wideband Filter, –6 dBFS*

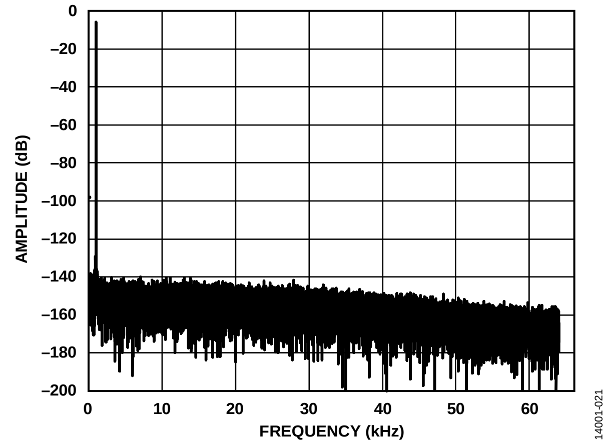



*Figure 20. FFT, Median Mode, Sinc5 Filter, –6 dBFS*

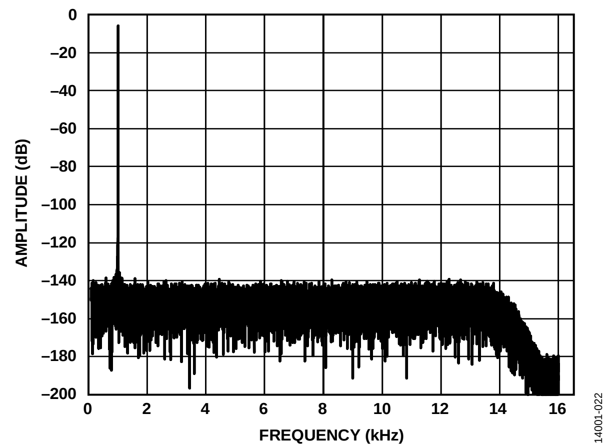



*Figure 21. FFT, Eco Mode, Wideband Filter, –6 dBFS*

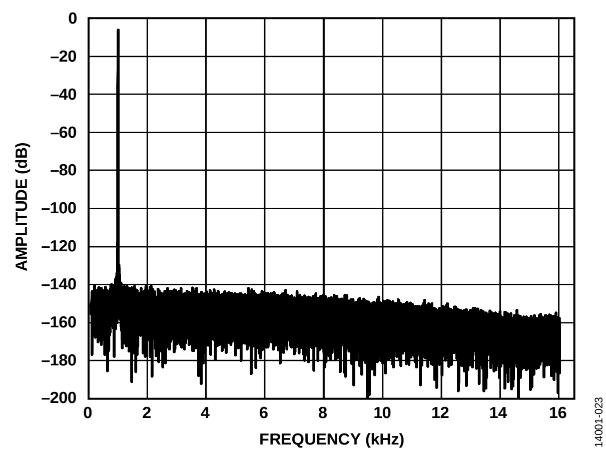



*Figure 22. FFT, Eco Mode, Sinc5 Filter, –6 dBFS*

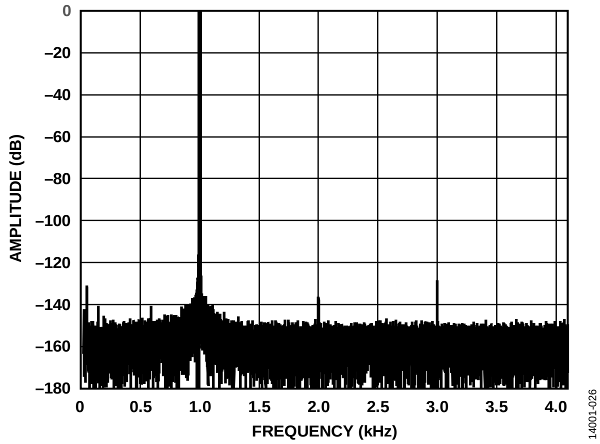



*Figure 23. FFT One-Shot-Mode, Sinc5 Filter, Median Mode, Decimation = ×64, −0.5 dBFS*

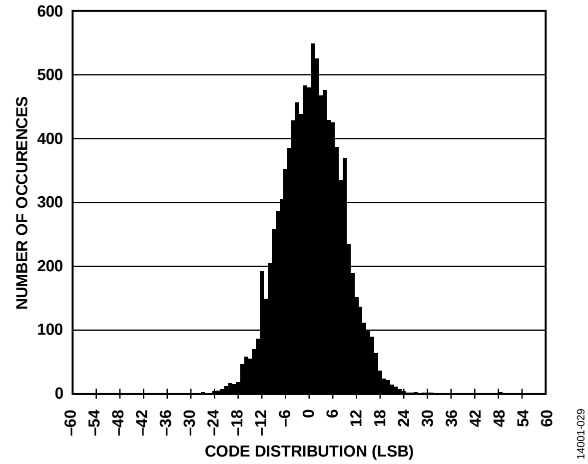



*Figure 26. Shorted Noise, Fast Mode, Sinc5 Filter*

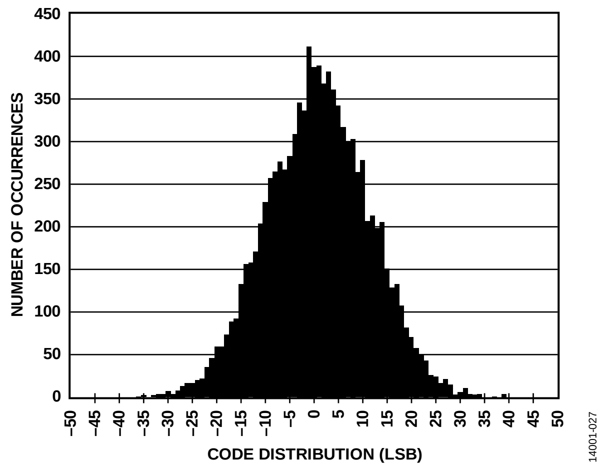



*Figure 24. Shorted Noise, One-Shot Mode, Sinc5 Filter, Median Mode, Decimation = ×32*

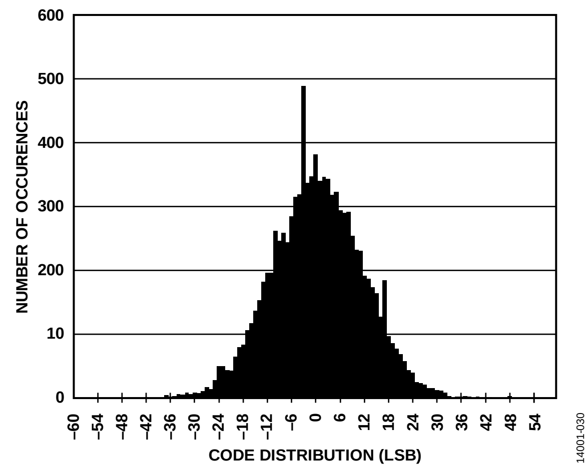



*Figure 27. Shorted Noise, Median Mode, Wideband Filter*

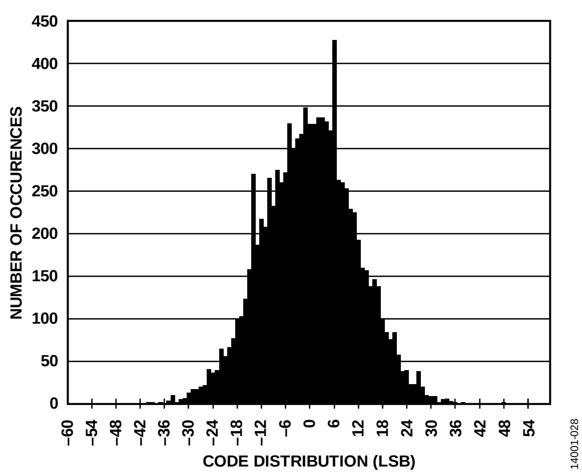



*Figure 25. Shorted Noise, Fast Mode, Wideband Filter*

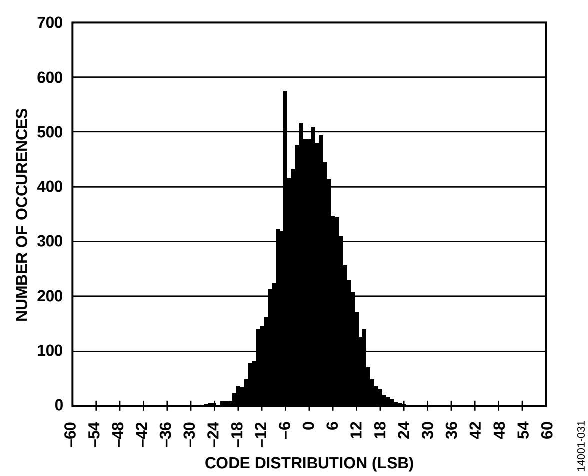



*Figure 28. Shorted Noise, Median Mode, Sinc5 Filter*

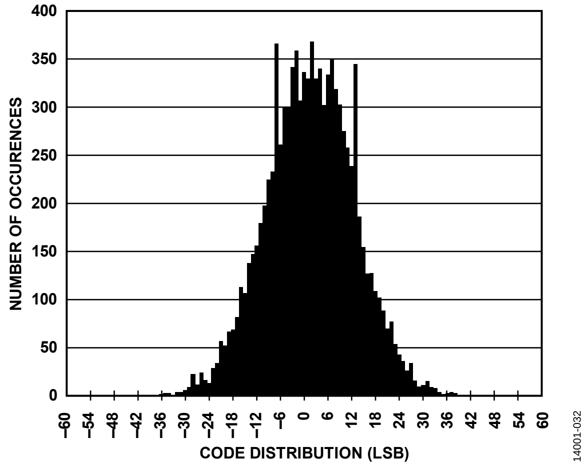


Figure 29. Shorted Noise, Eco Mode, Wideband Filter

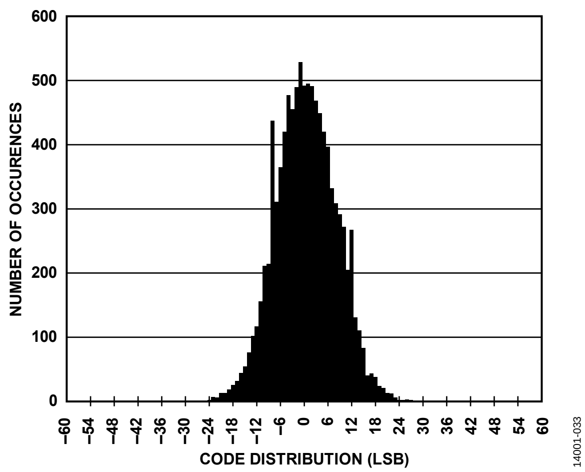


Figure 30. Shorted Noise, Eco Mode, Sinc5 Filter

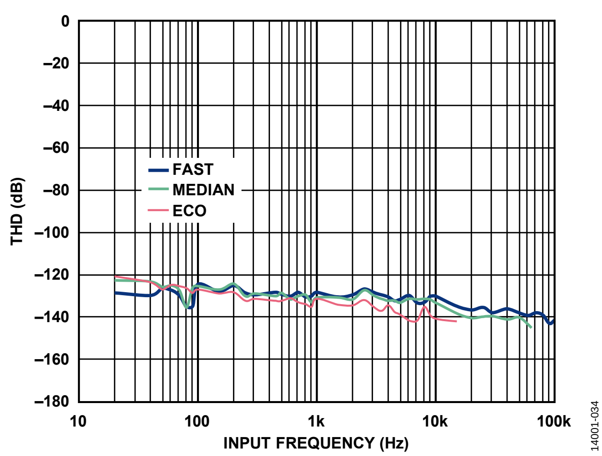


Figure 31. THD vs. Input Frequency, Three Power Modes, Wideband Filter

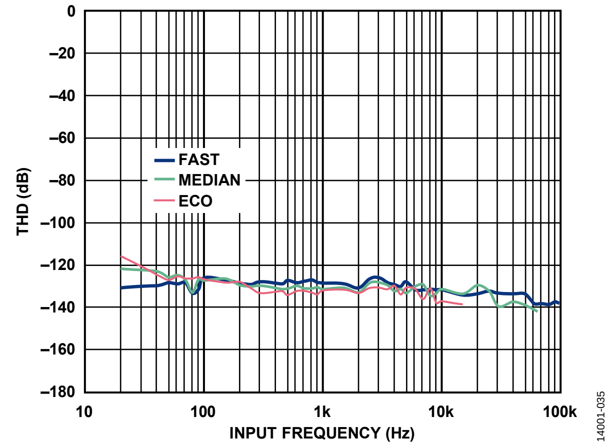


Figure 32. THD vs. Input Frequency, Three Power Modes, Sinc5 Filter

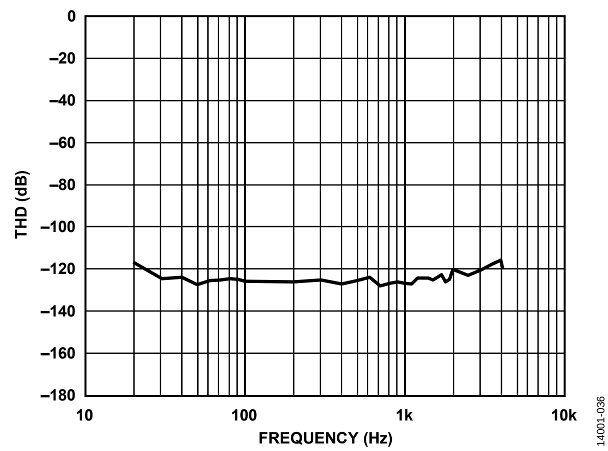


Figure 33. THD vs. Frequency, One-Shot Mode, Sinc5 Filter

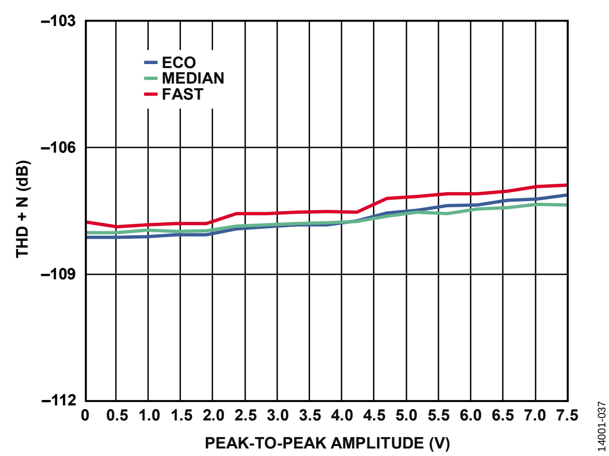


Figure 34. THD + N vs. Peak-to-Peak Amplitude, Three Power Modes, Wideband Filter

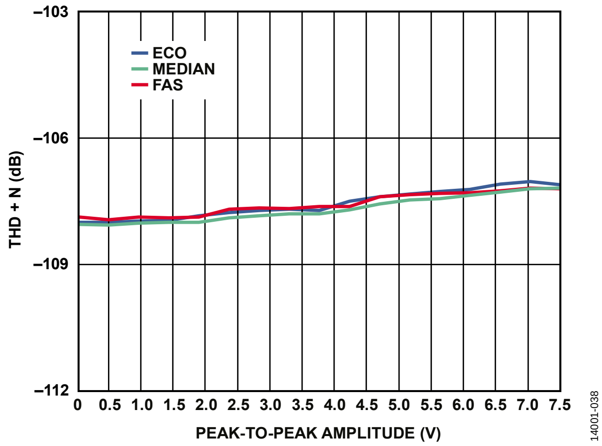



*Figure 35. THD + N vs. Peak-to-Peak Amplitude, Three Power Modes, Sinc5 Filter*

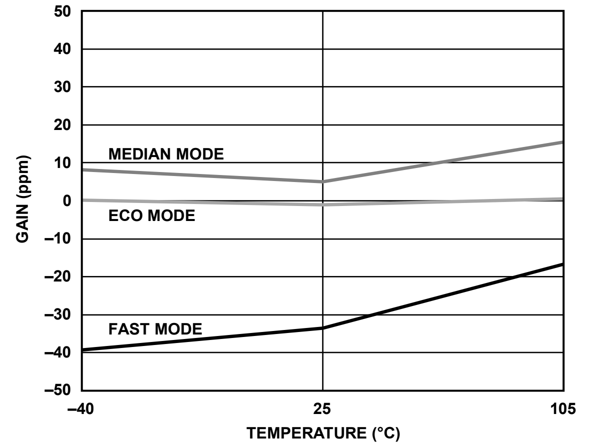



*Figure 38. Gain vs. Temperature for Various Power Modes*

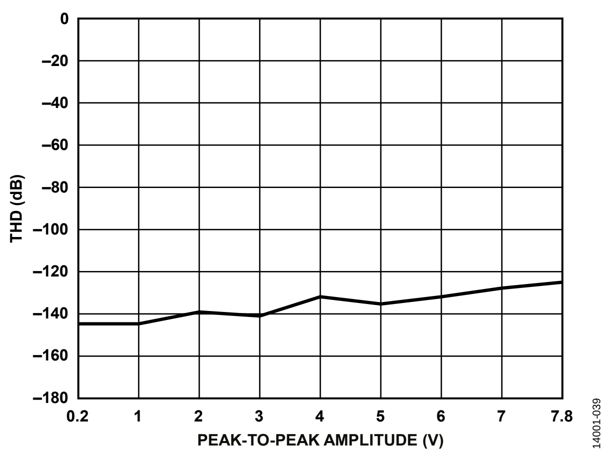



*Figure 36. THD vs. Peak-to-Peak Amplitude, One-Shot Mode, Sinc5 Filter*

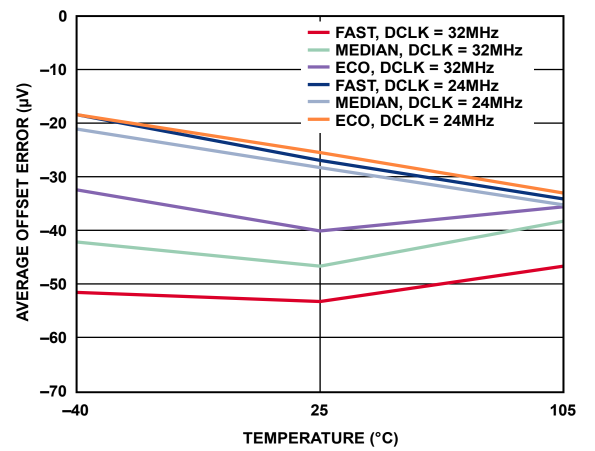



*Figure 39. Average Offset Error vs. Temperature for Various Power Modes and DCLK Frequencies*

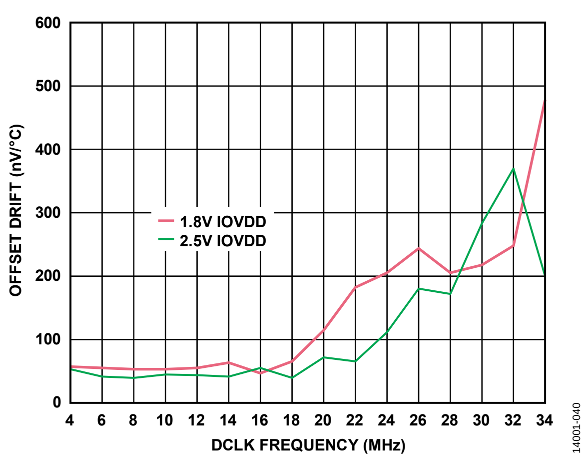



*Figure 37. Offset Drift vs. DCLK Frequency*

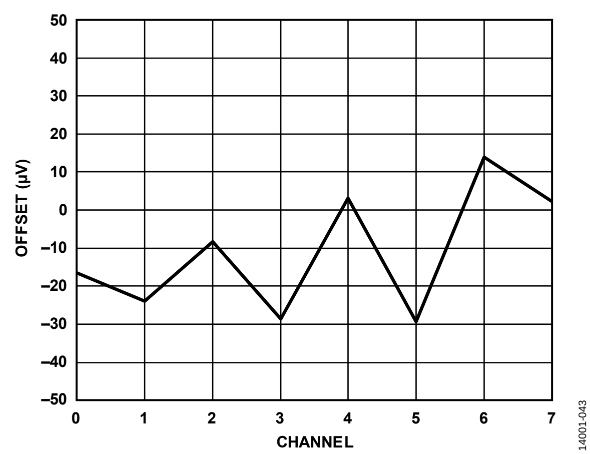



*Figure 40. Offset, One-Shot Mode*

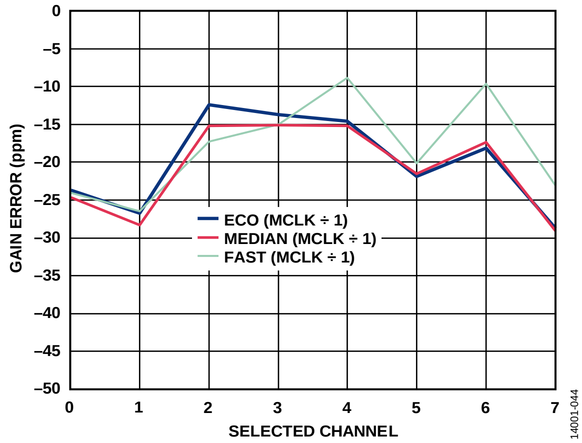



*Figure 41. Gain Error vs. Power Modes per Selected Channel*

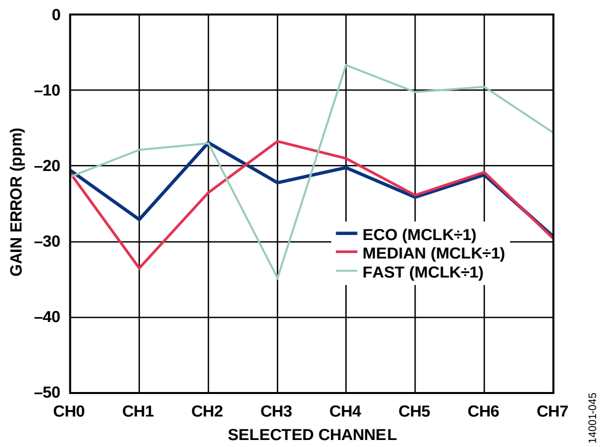



*Figure 42. Gain Error vs. Power Mode per Selected Channel, One-Shot Mode*

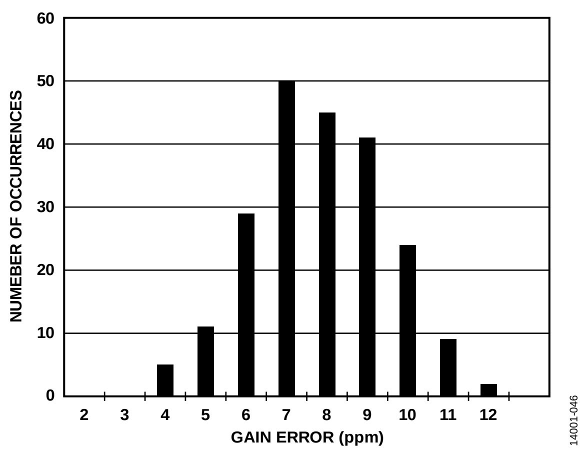



*Figure 43. Channel to Channel Gain Error Matching*

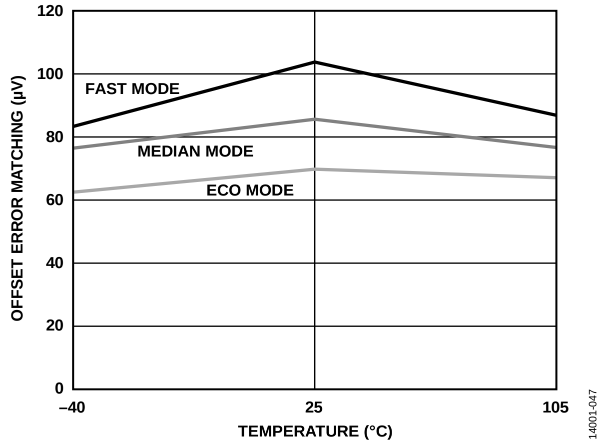



*Figure 44. Channel Offset Matching*

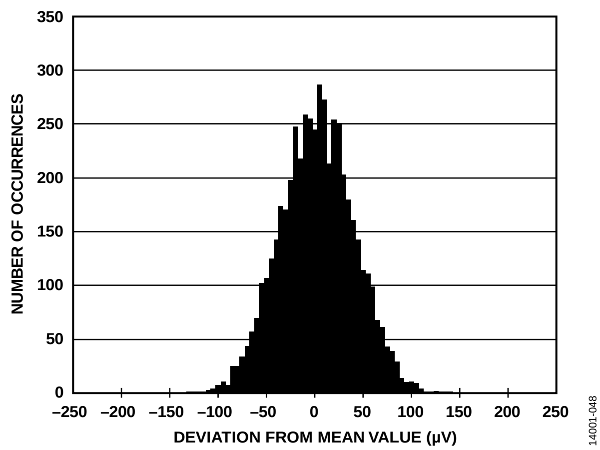



*Figure 45. VCM Output Histogram*

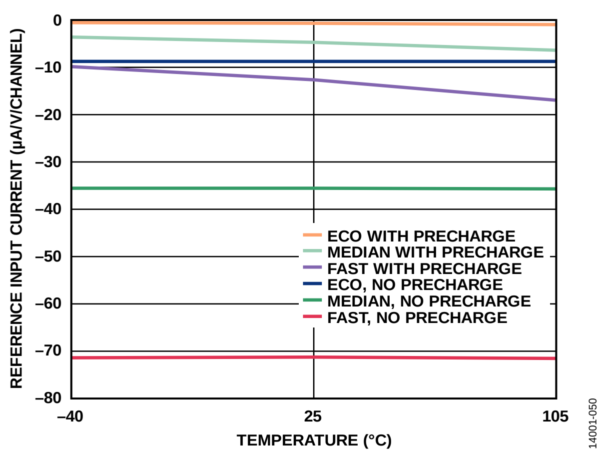



*Figure 46. Reference Input Current vs. Temperature, Reference Precharge Buffers On/Off*

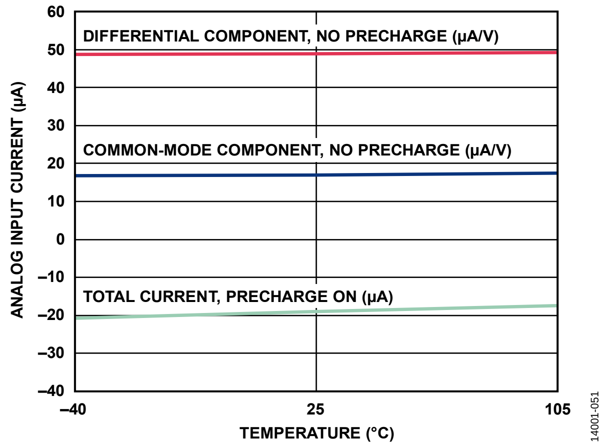



Figure 47. Analog Input Current vs. Temperature, Analog Input Precharge Buffers On/Off

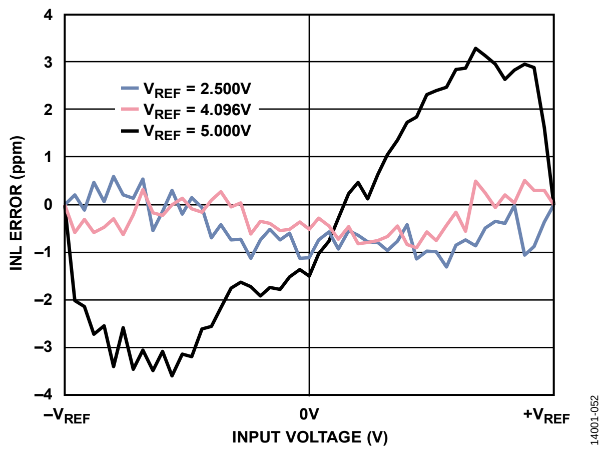



Figure 48. INL Error vs. Input Voltage for Various Voltage Reference Levels, Fast Mode

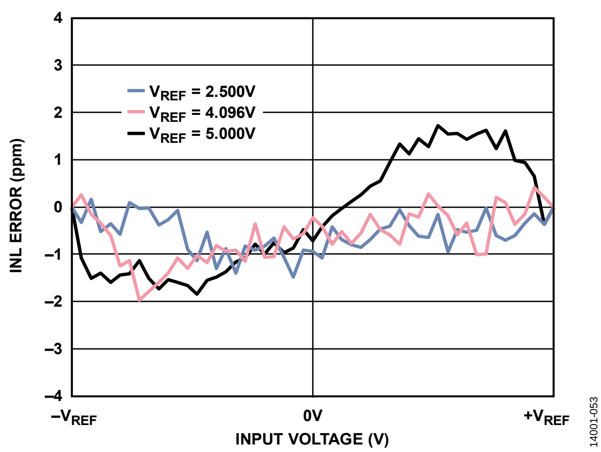



Figure 49. INL Error vs. Input Voltage for Various Voltage Reference Levels, Median Mode

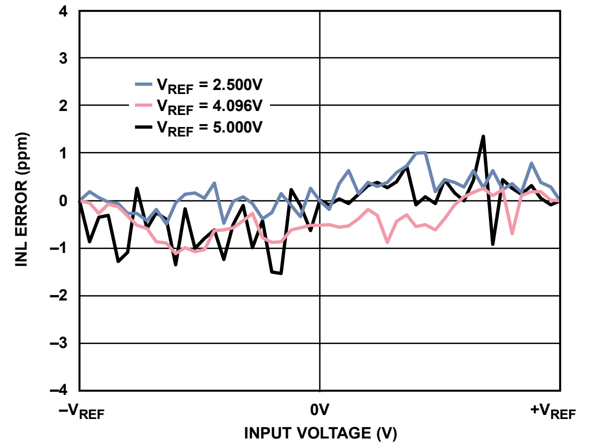



Figure 50. INL Error vs. Input Voltage for Various Voltage Reference Levels, Eco Mode

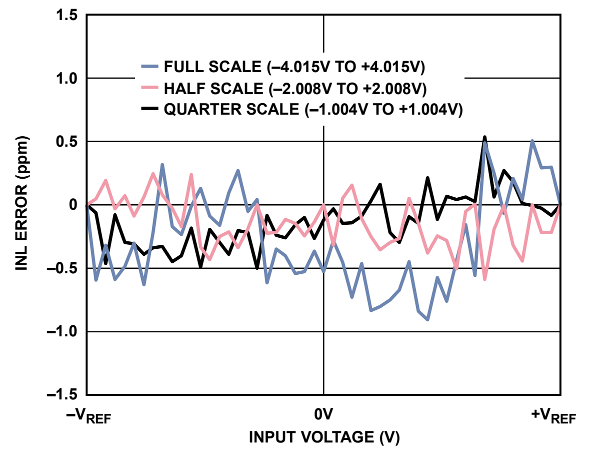



Figure 51. INL Error vs. Input Voltage, Full-Scale, Half-Scale, and Quarter-Scale Inputs

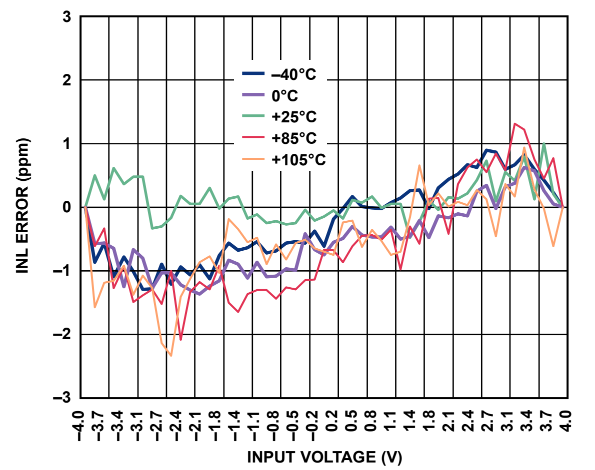



Figure 52. Maximum INL Error vs. Input Voltage for Various Temperatures, Fast Mode

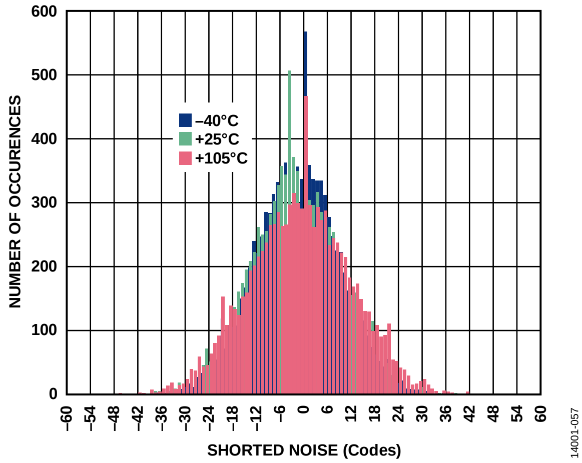



Figure 53. Shorted Noise vs. Temperature Drift

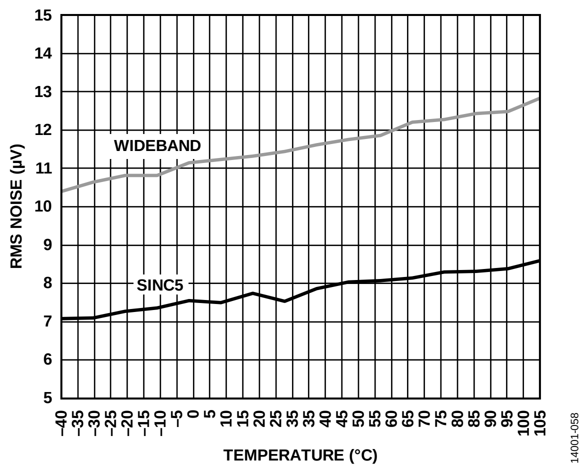



Figure 54. RMS Noise vs. Temperature, Fast Mode

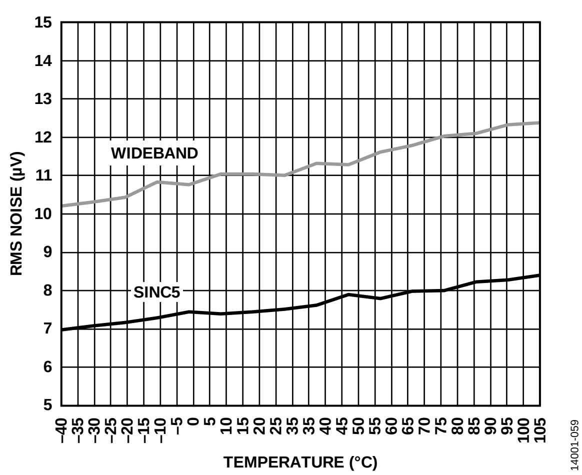



Figure 55. RMS Noise vs. Temperature, Median Mode

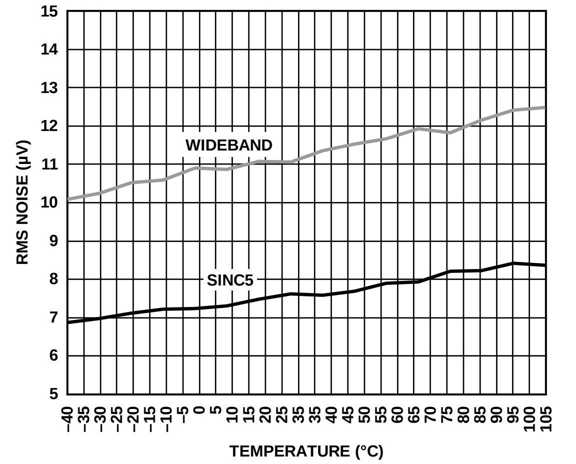



Figure 56. RMS Noise vs. Temperature, Eco Mode

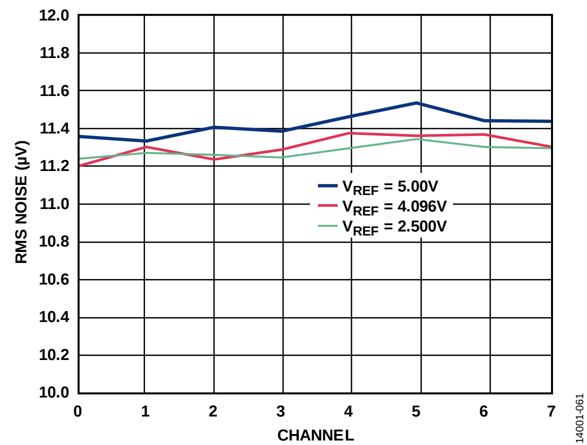



Figure 57. RMS Noise per Channel for Various $V_{REF}$ Values

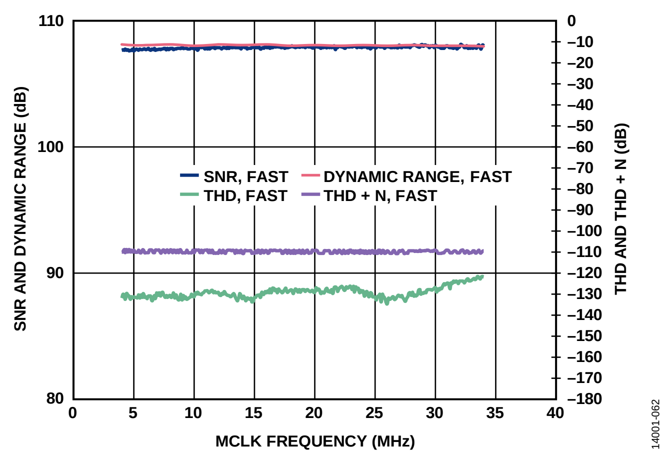



Figure 58. SNR, THD, THD +N, and Dynamic Range vs. MCLK Frequency

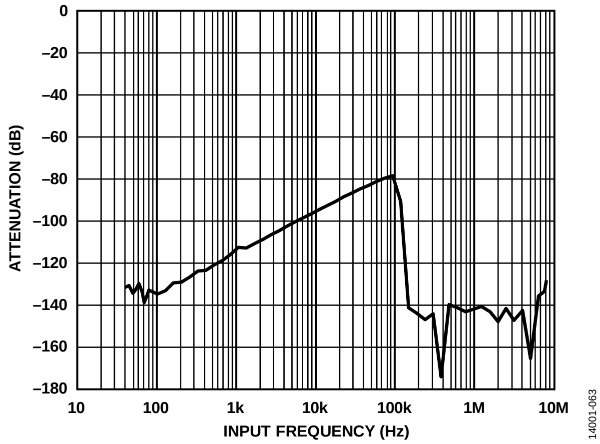



Figure 59. AC CMRR vs. Input Frequency

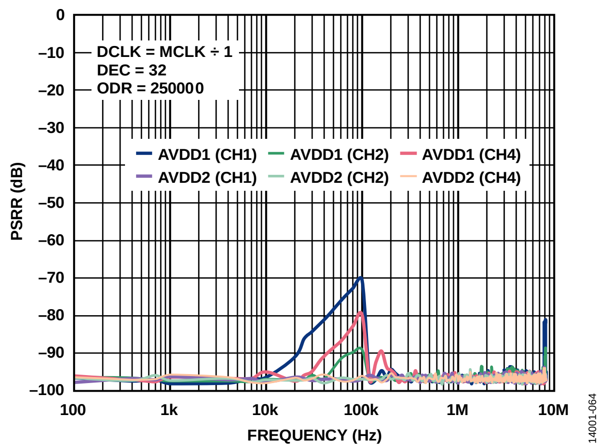



Figure 60. AC PSRR vs. Frequency, AVDD1/AVDD2

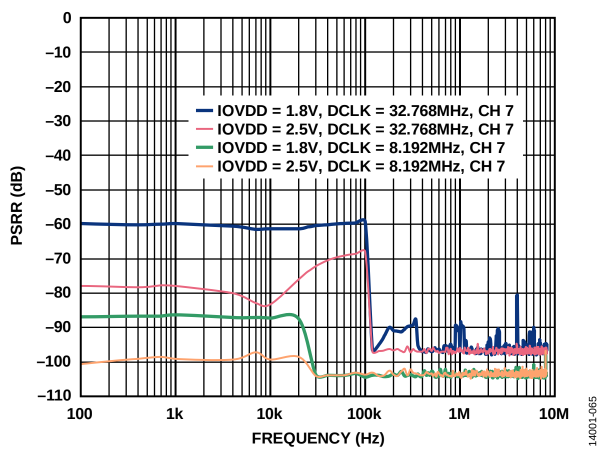



Figure 61. AC PSRR vs. Frequency, IOVDD

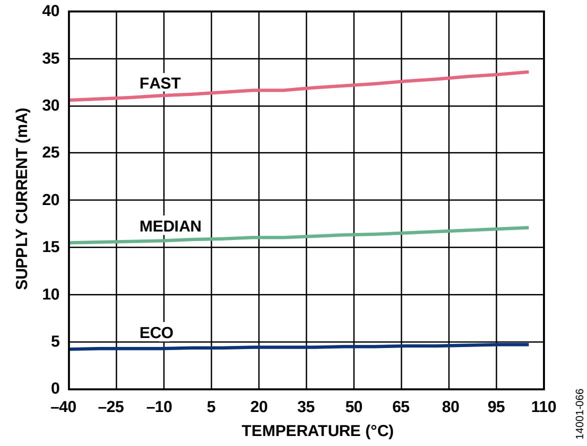



Figure 62. Supply Current vs. Temperature, AVDD1

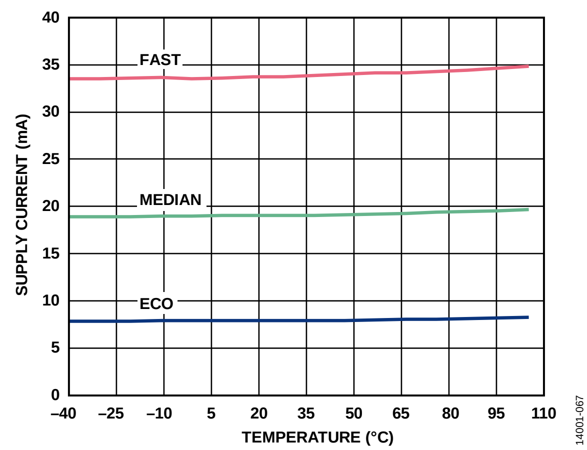



Figure 63. Supply Current vs. Temperature, AVDD2

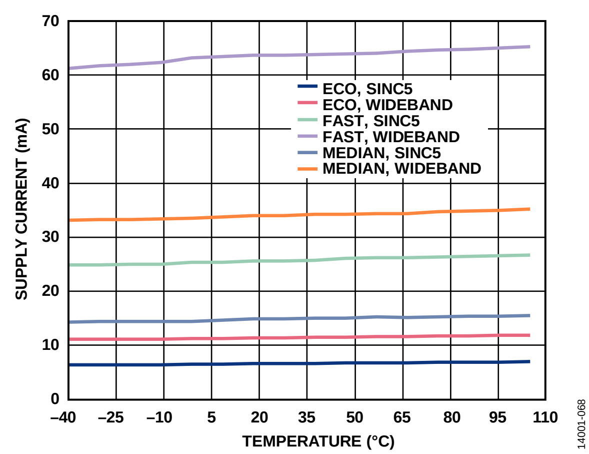



Figure 64. Supply Current vs. Temperature, IOVDD

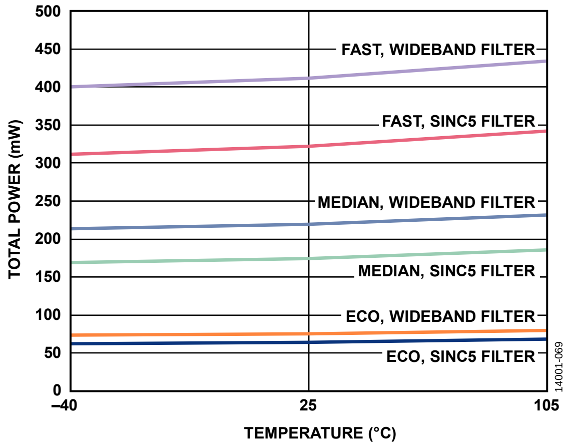



Figure 65. Total Power vs. Temperature

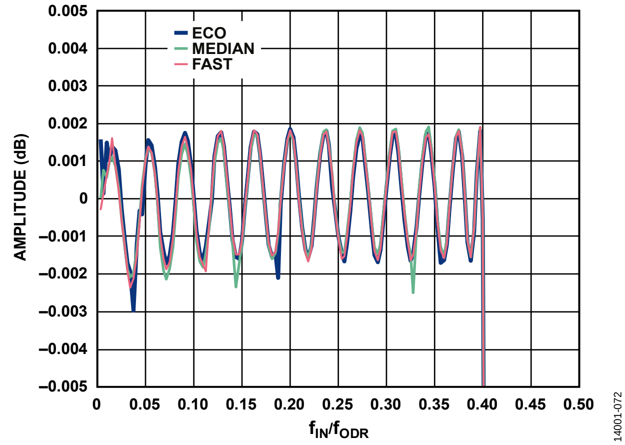



Figure 68. Wideband Filter Ripple

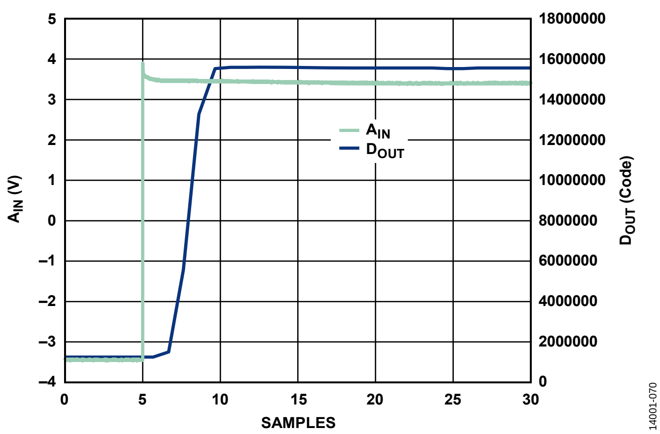



Figure 66. Step Response, Sinc5 Filter

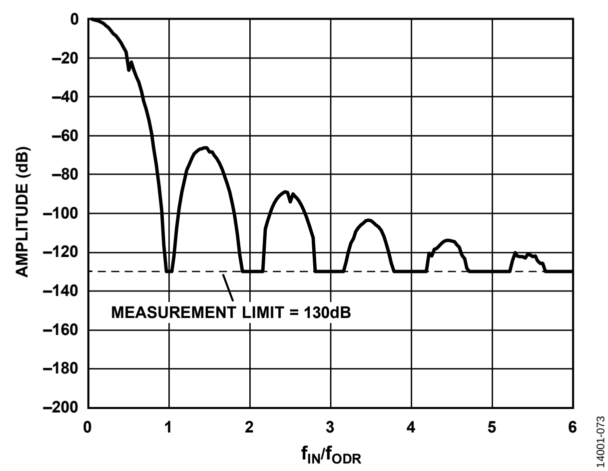



Figure 69. Sinc5 Filter Profile vs. ODR

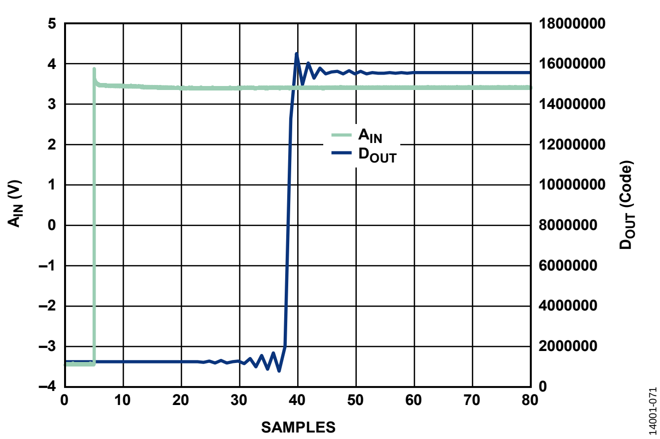



Figure 67. Step Response, Wideband Filter

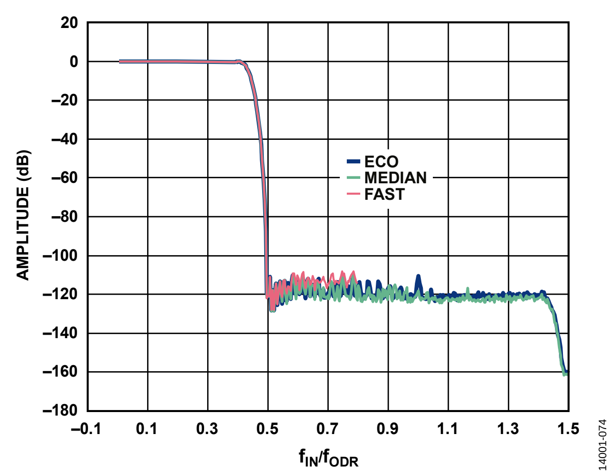



Figure 70. Wideband Filter Profile vs. ODR

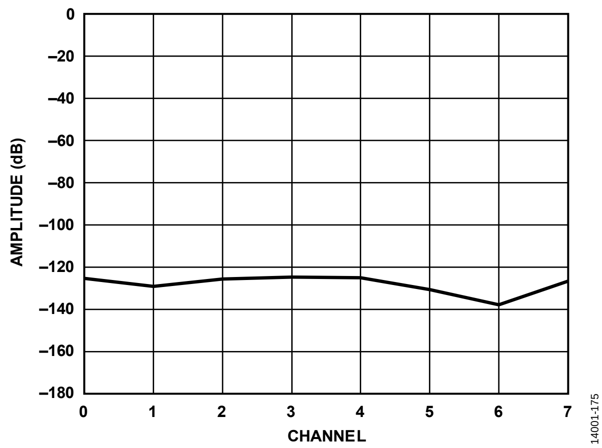



Figure 71. Crosstalk

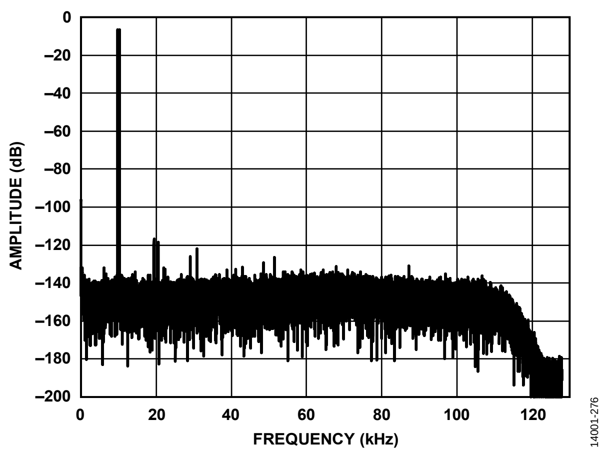



Figure 72. IMD with Input Signals at 9.7 kHz and 10.3 kHz

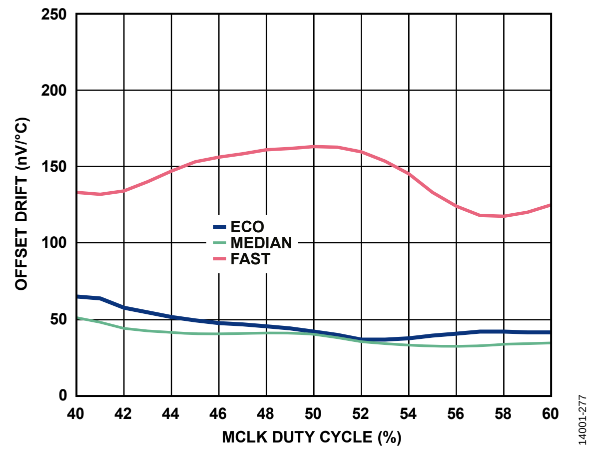



Figure 73. Offset Drift vs. MCLK Duty Cycle

# TERMINOLOGY

**AC Common-Mode Rejection Ratio (AC CMRR)**

AC CMRR is defined as the ratio of the power in the ADC output at frequency, f, to the power of a sine wave applied to the common-mode voltage of AINx+ and AINx− at frequency, $f_S$.

$$AC\ CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:

*Pf* is the power at frequency, *f*, in the ADC output.

$Pf_S$ is the power at frequency, $f_S$, in the ADC output.

**Gain Error**

The first transition (from 100 … 000 to 100 … 001) occurs at a level ½ LSB above nominal negative full scale (−4.0959375 V for the ±4.096 V range). The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale (+4.0959375 V for the ±4.096 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

**Gain Error Drift**

Gain error drift is defined as the gain error change due to a temperature change of 1°C. It is expressed in parts per million per degree Celsius.

**Integral Nonlinearity (INL) Error**

INL error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

**Intermodulation Distortion (IMD)**

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa and nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m or n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7768 is tested using the CCIF standard, where two input frequencies near to each other are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second-order and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in decibels.

**Least Significant Bit (LSB)**

The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is:

$$LSB\ (\text{V}) = (2 \times V_{REF})/2^N$$

For the AD7768, $V_{REF}$ is the difference voltage between the REFx+ and REFx− pins, and N = 24.

**Offset Error**

Offset error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

**Power Supply Rejection Ratio (PSRR)**

Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in the power supply voltage from the nominal value.

**Signal-to-Noise Ratio (SNR)**

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

**Signal-to-Noise-and-Distortion Ratio (SINAD)**

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

**Spurious-Free Dynamic Range (SFDR)**

SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal (excluding the first five harmonics).

**Total Harmonic Distortion (THD)**

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

# THEORY OF OPERATION

The AD7768 is an 8-channel, simultaneously sampled, low noise, 24-bit Σ-Δ ADC.

Each ADC within the AD7768 employs a Σ-Δ modulator, sampling at 2 × $f_{MOD}$, to convert the analog input into an equivalent digital representation. The modulator samples represent a quantized version of the analog input signal.

The Σ-Δ conversion technique is an oversampled architecture. This oversampled approach spreads the quantization noise over a wide frequency band (see Figure 74). To reduce the quantization noise in the signal band, the high order modulator shapes the noise spectrum so that most of the noise energy is shifted out of the band of interest (see Figure 75). The digital filter that follows the modulator removes the large out of band quantization noise (see Figure 76).

For further information on the basics as well as more advanced concepts of Σ-Δ ADCs, see the MT-022 Tutorial and the MT-023 Tutorial.

Digital filtering has certain advantages over analog filtering. First, because digital filtering occurs after the analog-to-digital conversion, it can remove noise injected during the conversion process; analog filtering cannot remove noise injected during conversion. Second, the digital filter combines low pass-band ripple with a steep roll-off, while also maintaining a linear phase response.

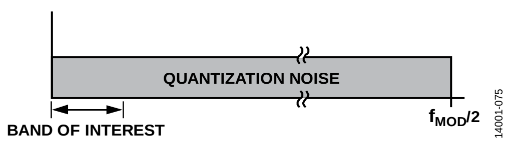



*Figure 74. Σ-Δ ADC Quantization Noise (Linear Scale X-Axis)*

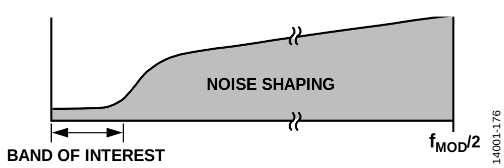



*Figure 75. Σ-Δ ADC Noise Shaping (Linear Scale X-Axis)*

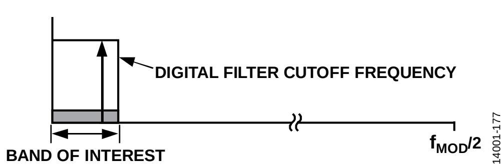



*Figure 76. Σ-Δ ADC Digital Filter Cutoff Frequency (Linear Scale X-Axis)*

## CLOCKING AND SAMPLING TREE

The AD7768 includes multiple ADC cores. Each of these ADCs receives the same master clock signal, MCLK. The MCLK signal is an external CMOS, crystal oscillator or LVDS clock source. This MCLK signal generates the sampling frequency of the modulator, $f_{MOD}$, and the digital output clock, DCLK. The $f_{MOD}$ and DCLK are synchronous with MCLK.

The user has three options for the $f_{MOD}$ frequency: MCLK/4, MCLK/8, or MCLK/32. The user has four options for the DCLK rate: MCLK/1, MCLK/2, MCLK/4, and MCLK/8.

Three power modes are available for the modulator: fast, median, and eco. Lower power modes reduce the bias current to the ADC; however, the AD7768 meets the specified performance only when the modulator frequency, $f_{MOD}$, does not exceed the upper limit of the operating power mode selected by the user. Table 10 shows the recommended $f_{MOD}$ ranges to achieve the best performance while minimizing the power consumption.

To achieve the maximum throughput rate of 256 kSPS/channel, $f_{MOD}$ must be 8.192 MHz. This requires a 32.768 MHz MCLK, MCLK_DIV of MCLK/4, and fast power mode.

By varying the power modes, MCLK_DIV and decimation ratios, users can achieve performance increases or power savings while maintaining the same bandwidth.

For example, if MCLK is 16 MHz and the target bandwidth is approximately 25 kHz, the median power mode is acceptable for all MCLK_DIV ratios, because the maximum $f_{MOD}$ frequency available is MCLK/4, which is 4.0 MHz. The user has the option of using one of the following configurations:

- Median power, $f_{MOD}$ = MCLK/4, decimation = ×64, and ODR = 62.5 kHz, which achieves the maximum performance for the given bandwidth requirements and MCLK rate.
- Median power, $f_{MOD}$ = MCLK/8 and decimation = ×32, and ODR = 62.5 kHz, which saves 48 mW of power for a 3 dB reduction in the dynamic range, compared to the previous case.

**Table 10. Recommended $f_{MOD}$ Range for Each Power Mode**

| Power Mode | Recommended $f_{MOD}$ (MHz), MCLK = 32.768 MHz |
|---|---|
| Eco | 0.036 to 1.024 |
| Median | 1.025 to 4.096 |
| Fast | 4.1 to 8.192 |

In pin control mode, the MODEx pins determine the power mode, modulator frequency, and DCLK frequency. The modulator frequency tracks the power mode. This means that $f_{MOD}$ is fixed at MCLK/32 for eco mode, MCLK/8 for median mode, and MCLK/4 for fast mode (see Table 19).

In SPI mode, the user can program the power mode, modulator frequency, and DCLK frequency using Register 0x04 and Register 0x07 (see Table 38 for register information). Independent selection of the power mode and MCLK_DIV allows freedom in the MCLK speed selection to achieve a target modulator frequency.

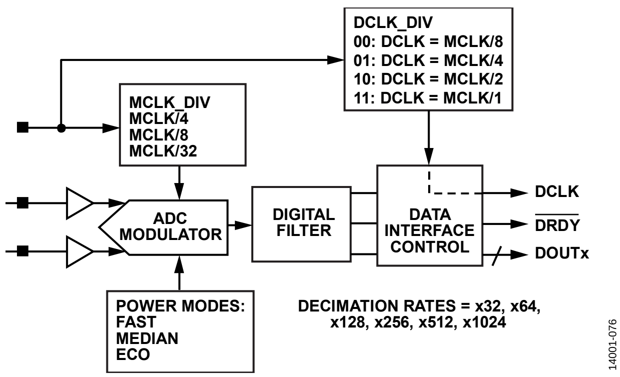



*Figure 77. Sampling Structure, Defined by MCLK, DCLK_DIV, and MCLK_DIV Settings*

## NOISE PERFORMANCE AND RESOLUTION

Table 11 and Table 12 show the noise performance for the wideband and sinc5 digital filters of the AD7768 for various output data rates and power modes. The noise values and dynamic ranges specified are typical for the bipolar input range with an external 4.096 V reference ($V_{REF}$). The rms noise is measured with shorted analog inputs, which are driven to (AVDD1 − AVSS)/2 using the on-board VCM buffer output.

The dynamic range is calculated as the ratio of the rms shorted input noise to the rms full-scale input signal range.

$$Dynamic\ Range\ (dB) = 20\log_{10}((2 \times V_{REF}/2\sqrt{2})/(RMS\ Noise))$$

The LSB size with 4.096 V reference is 488 nV, and is calculated as follows:

$$LSB\ (V) = (2 \times V_{REF})/2^{24}$$

Table 11. Wideband Filter Noise: Performance vs. Output Data Rate ($V_{REF}$ = 4.096 V)

| Output Data Rate (kSPS) | −3 dB Bandwidth (kHz) | Shorted Input Dynamic Range (dB) | RMS Noise (µV) |
|---|---|---|---|
| Fast Mode | | | |
| 256 | 110.8 | 107.96 | 11.58 |
| 128 | 55.4 | 111.43 | 7.77 |
| 64 | 27.7 | 114.55 | 5.42 |
| 32 | 13.9 | 117.58 | 3.82 |
| 16 | 6.9 | 120.56 | 2.72 |
| 8 | 3.5 | 123.5 | 1.94 |
| Median Mode | | | |
| 128 | 55.4 | 108.13 | 11.36 |
| 64 | 27.7 | 111.62 | 7.6 |
| 32 | 13.9 | 114.75 | 5.3 |
| 16 | 6.9 | 117.79 | 3.74 |
| 8 | 3.5 | 120.8 | 2.64 |
| 4 | 1.7 | 123.81 | 1.87 |
| Eco Mode | | | |
| 32 | 13.9 | 108.19 | 11.28 |
| 16 | 6.9 | 111.69 | 7.54 |
| 8 | 3.5 | 114.83 | 5.25 |
| 4 | 1.7 | 117.26 | 3.71 |
| 2 | 0.87 | 120.88 | 2.62 |
| 1 | 0.43 | 123.88 | 1.85 |

Table 12. Sinc5 Filter Noise: Performance vs. Output Data Rate ($V_{REF}$ = 4.096 V)

| Output Data Rate (kSPS) | −3 dB Bandwidth (kHz) | Shorted Input Dynamic Range (dB) | RMS Noise (µV) |
|---|---|---|---|
| Fast Mode | | | |
| 256 | 52.224 | 111.36 | 7.83 |
| 128 | 26.112 | 114.55 | 5.43 |
| 64 | 13.056 | 117.61 | 3.82 |
| 32 | 6.528 | 120.61 | 2.71 |
| 16 | 3.264 | 123.52 | 1.93 |
| 8 | 1.632 | 126.39 | 1.39 |
| Median Mode | | | |
| 128 | 26.112 | 111.53 | 7.68 |
| 64 | 13.056 | 114.75 | 5.3 |
| 32 | 6.528 | 117.81 | 3.72 |
| 16 | 3.264 | 120.82 | 2.64 |
| 8 | 1.632 | 123.82 | 1.87 |
| 4 | 0.816 | 126.79 | 1.33 |
| Eco Mode | | | |
| 32 | 6.528 | 111.57 | 7.65 |
| 16 | 3.264 | 114.82 | 5.26 |
| 8 | 1.632 | 117.88 | 3.7 |
| 4 | 0.816 | 120.9 | 2.61 |
| 2 | 0.408 | 123.91 | 1.85 |
| 1 | 0.204 | 126.89 | 1.31 |

# APPLICATIONS INFORMATION

The AD7768 offers users a multichannel platform measurement solution for ac and dc signal processing.

Flexible filtering allows the AD7768 to be configured to simultaneously sample ac and dc signals on a per channel basis. Power scaling allows users to trade off the input bandwidth of the measurement versus the current consumption. This ability, coupled with the flexibility of the digital filtering, allows the user to optimize the energy efficiency of the measurement, while still meeting power, bandwidth, and performance targets.

Key capabilities that allow users to choose the AD7768 as their platform high resolution ADC are highlighted as follows:

- Eight fully differential or pseudo differential analog inputs.
- Fast throughput simultaneous sampling ADCs catering for input signals up to 110.8 kHz.
- Three selectable power modes (fast, median, and eco) for scaling the current consumption and input bandwidth of the ADC for optimal measurement efficiency.
- Precharge analog input and precharge reference buffers reduce the drive requirements of external amplifiers.
- Control of reference and analog precharge buffers on a per channel basis.
- Wideband, low ripple, digital filter for ac measurement.
- Fast sinc5 filter for precision low frequency measurement.
- Two channel modes, defined by the user selected filter choice, and decimation ratios, can be defined for use on different ADC channels. This enables optimization of the input bandwidth versus the signal of interest.
- Option of SPI or pin strapped control and configuration.
- Offset, gain, and phase calibration registers per channel.
- Common-mode voltage output buffer for use by driver amplifier.
- On-board AVDD2 and IOVDD LDOs for the low power, 1.8 V, internal circuitry.

Refer to Figure 78 and Table 13 for the typical connections and minimum requirements to get started using the AD7768.

Table 14 shows the typical power and performance of the AD7768 for the available power modes, for each filter type.

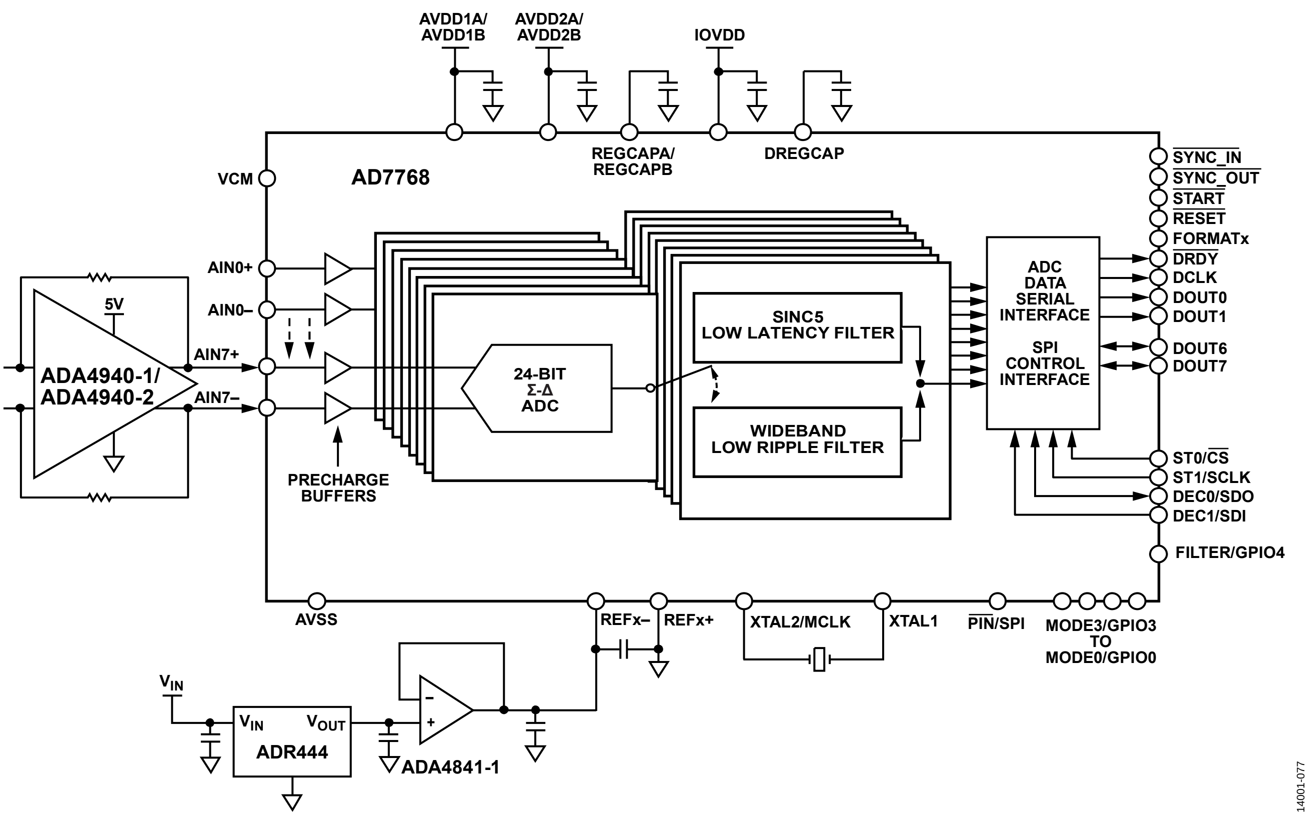



*Figure 78. Typical Connection Diagram*

**Table 13. Requirements to Operate the AD7768**

| Requirement | Description |
|---|---|
| Power Supplies | 5 V AVDD1 supply, 2.25 V to 5 V AVDD2 supply, 1.8 V or 2.5 V to 3.6 V IOVDD supply (ADP7104/ADP7118) |
| External Reference | 2.5 V, 4.096 V, or 5 V (ADR441, ADR444, or ADR445) |
| External Driver Amplifiers | The ADA4896-2, the ADA4940-2, the ADA4805-2, and the ADA4807-2 |
| External Clock | Crystal or a CMOS/LVDS clock for the ADC modulator sampling |
| FPGA or DSP | Input/output voltage of 2.5 V to 3.6 V, or 1.8 V (see the 1.8 V IOVDD Operation section) |

**Table 14. Speed, Dynamic Range, THD, and Power Overview; Eight Channels Active, Decimate by 32[1]**

| Power Mode | Output Data Rate (kSPS) | THD (dB) | Sinc5 Filter Dynamic Range (dB) | Sinc5 Filter Bandwidth (kHz) | Sinc5 Filter Power Dissipation (mW per channel) | Wideband Filter Dynamic Range (dB) | Wideband Filter Bandwidth (kHz) | Wideband Filter Power Dissipation (mW per channel) |
|---|---|---|---|---|---|---|---|---|
| Fast | 256 | −115 | 111 | 52.224 | 41 | 108 | 110.8 | 52 |
| Median | 128 | −120 | 111 | 26.112 | 22 | 108 | 55.4 | 28 |
| Eco | 32 | −120 | 111 | 6.528 | 8.5 | 108 | 13.9 | 9.5 |

[1] Analog precharge buffers on, precharge reference buffers and VCM disabled, typical values, AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, $V_{REF}$ = 4.096 V MCLK = 32.768 MHz, DCLK = MCLK/4, $T_A$ = 25°C.

## POWER SUPPLIES

The AD7768 has three independent power supplies: AVDD1 (AVDD1A and AVDD2A), AVDD2 (AVDD2A and AVDD2B), and IOVDD.

The reference potentials for these supplies are AVSS and DGND. Tie all the AVSS supply pins (AVSS1A, AVSS1B, AVSS2A, AVSS2B, and AVSS) to the same potential with respect to DGND. AVDD1A, AVDD1B, AVDD2A, and AVDD2B are referenced to this AVSS rail. IOVDD is referenced to DGND.

The supplies can be powered within the following ranges:

- AVDD1 = 5 V ± 10%, relative to AVSS
- AVDD2 = 2 V to 5.5 V, relative to AVSS
- IOVDD (with internal regulator) = 2.25 V to 3.6 V, relative to DGND
- IOVDD (bypassing regulator) = 1.72 V to 1.88 V, relative to DGND
- AVSS = 0 V to −2.75 V, relative to DGND

The AVDD1A and AVDD1B (AVDD1) supplies power the analog front end, reference input, and common-mode output circuitry. AVDD1 is referenced to AVSS, and all AVDD1 supplies must be tied to the same potential with respect to AVSS. If AVDD1 supplies are used in a ±2.5 V split supply configuration, the ADC inputs are truly bipolar. When using split supplies, reference the absolute maximum ratings, which deal with the voltage allowed between AVSS and IOVDD supplies.

The AVDD2A and AVDD2B (AVDD2) supplies connect to internal 1.8 V analog LDO regulators. The regulators power the ADC core. AVDD2 is referenced to AVSS, and all AVDD2 supplies must be tied to the same potential with respect to AVSS. The voltage on AVDD2 can range from 5.5 V (maximum) to 2 V (minimum), with respect to AVSS.

IOVDD powers the internal 1.8 V digital LDO regulator. This regulator powers the digital logic of the ADC. IOVDD also sets the voltage levels for the SPI interface of the ADC. IOVDD is referenced to DGND, and the voltage on IOVDD can vary from 3.6 V (maximum) to 2.25 V (minimum), with respect to DGND. IOVDD can also be configured to run at 1.8 V. In this case, IOVDD and DREGCAP must be tied together and must be within the range of 1.88 V (maximum) to 1.72 V (minimum), with respect to DGND. See the 1.8 V IOVDD Operation section for more information on operating the AD7768 at 1.8 V IOVDD.

### *Recommended Power Supply Configuration*

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a power solution that uses the ADP7118 is shown in Figure 79. The ADP7118 provides positive supply rails for optimal converter performance, creating either a single 5 V, 3.3 V, or dual AVDD1/IOVDD, depending on the required supply configuration. The ADP7118 can operate from input voltages of up to 20 V.

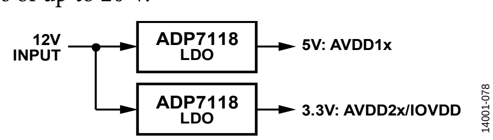



*Figure 79. Power Supply Configuration*

Alternatively, the ADP7112 or ADP7104 can be selected for powering the AD7768. Refer to the AN-1120 Application Note for more information regarding low noise LDO performance and power supply filtering.

## DEVICE CONFIGURATION

The AD7768 has independent paths for reading data from the ADC conversions and for controlling the device functionality.

For control, the device can be configured in either of two modes. The two modes of configuration are

- Pin control mode: pin strapped digital logic inputs (which allows a subset of the configurability options)
- SPI mode: over a 3-wire or 4-wire SPI interface (complete configurability)

On power-up, the state of the $\overline{\text{PIN}}$/SPI pin determines the mode used. Immediately after power-up, the user must apply a soft or hard reset to the device when using either control mode.

### *Interface Data Format*

When operating the device, the data format of the serial interface is determined by the FORMATx pins. Table 28 shows that each ADC can be assigned a DOUTx pin, or, alternatively, the data can be arranged to share the DOUTx pins in a time division multiplexed manner. For more details, see the Data Interface section.

## PIN CONTROL

Pin control mode eliminates the need for an SPI communication interface. Where a single known configuration is required by the user, or where only limited reconfiguration is required, the number of signals that require routing to the digital host can be reduced using this mode. Pin control mode is useful in digitally isolated applications where minimal adjustment of the configuration is needed. Pin control offers a subset of the core functionality and ensures a known state of operation after power-up, reset, or a fault condition on the power supply. In pin control mode, the analog input precharge buffers are enabled by default for best performance. The reference input precharge buffers are disabled in pin control mode.

### *Setting the Filter*

The filter function chooses between the two filter settings. In pin control mode all ADC channels use the same filter type, which is selected by the FILTER pin, as shown in Table 15.

**Table 15. FILTER Control Pin**

| Logic Level | Function |
|---|---|
| 1 | Sinc5 filter selected |
| 0 | Wideband filter selected |

### *Setting the Decimation Rate*

Pin control mode allows selection from four possible decimation rates. The decimation rate is selected via the DEC1 and DEC0 pins. The chosen decimation rate is used on all ADC channels. Table 16 shows the truth table for the DECx pins.

**Table 16. Decimation Rate Control Pins Truth Table**

| DEC1 | DEC0 | Decimation Rate |
|---|---|---|
| 0 | 0 | ×32 |
| 0 | 1 | ×64 |
| 1 | 0 | ×128 |
| 1 | 1 | ×1024 |

### *Operating Mode*

The MODE3 to MODE0 pins determine the configuration of all channels when using pin control mode. The variables controlled by the MODEx pins are shown in Table 17. The user selects how much current the device consumes, the sampling speed of the ADC (power mode), how fast the ADC result is received by the digital host (DCLK_DIV), and how the ADC conversion is initiated (conversion operation). Figure 80 illustrates the inputs used to configure the device in pin control mode.

**Table 17. Mode Pins: Variables for Control**

| Control Variable | Possible Settings |
|---|---|
| Sampling Speed/Power Consumption Power Mode | Fast |
| | Median |
| | Eco |
| Data Clock Output Frequency (DCLK_DIV) | DCLK = MCLK/1 |
| | DCLK = MCLK/2 |
| | DCLK = MCLK/4 |
| | DCLK = MCLK/8 |
| Conversion Operation | Standard conversion |
| | One-shot conversion |

The MODEx pins map to 16 distinct settings. The settings are selected to optimize the use cases of the AD7768, allowing the user to reduce the DCLK frequency for lower, less demanding power modes and selecting either the one-shot or standard conversion modes.

See Table 19 for the complete selection of operating modes that are available via the MODEx pins in pin control mode.

The power mode setting automatically scales the bias currents of the ADC and divides the applied MCLK to the correct setting for that mode. Note that this is not the same as using SPI control, where separate bit fields exist to control the bias currents of the ADC and MCLK division.

In pin control mode, the modulator rate is fixed for each power mode to achieve the best performance. Table 18 shows the modulator division for each power mode.

**Table 18. Modulator Rate, Pin Control Mode**

| Power Mode | Modulator Rate, $f_{MOD}$ |
|---|---|
| Fast | MCLK/4 |
| Median | MCLK/8 |
| Eco | MCLK/32 |

### *Diagnostics*

Pin control mode offers a subset of diagnostics features. Internal errors are reported in the status header output with the data conversion results for each channel.

Internal CRC errors, memory map flipped bits, and external clocks not detected are reported by Bit 7 of the status header and indicate that a reset is required. The status header also reports filter not settled, filter type, and filter saturated signals. Users can determine when to ignore data by monitoring these error flags. For more information on the status header, see the ADC Conversion Output: Header and Data section.

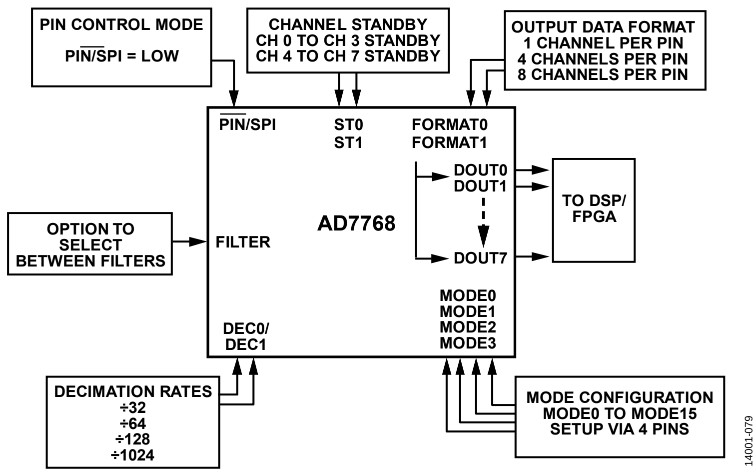



*Figure 80. Pin Configurable Functions*

**Table 19. MODEx Selection Details: Pin Control Mode**

| Mode Hex. | MODE3 | MODE2 | MODE1 | MODE0 | Power Mode | DCLK Frequency | Data Conversion |
|---|---|---|---|---|---|---|---|
| 0x0 | 0 | 0 | 0 | 0 | Eco | MCLK/1 | Standard |
| 0x1 | 0 | 0 | 0 | 1 | Eco | MCLK/2 | Standard |
| 0x2 | 0 | 0 | 1 | 0 | Eco | MCLK/4 | Standard |
| 0x3 | 0 | 0 | 1 | 1 | Eco | MCLK/8 | Standard |
| 0x4 | 0 | 1 | 0 | 0 | Median | MCLK/1 | Standard |
| 0x5 | 0 | 1 | 0 | 1 | Median | MCLK/2 | Standard |
| 0x6 | 0 | 1 | 1 | 0 | Median | MCLK/4 | Standard |
| 0x7 | 0 | 1 | 1 | 1 | Median | MCLK/8 | Standard |
| 0x8 | 1 | 0 | 0 | 0 | Fast | MCLK/1 | Standard |
| 0x9 | 1 | 0 | 0 | 1 | Fast | MCLK/2 | Standard |
| 0xA | 1 | 0 | 1 | 0 | Fast | MCLK/4 | Standard |
| 0xB | 1 | 0 | 1 | 1 | Fast | MCLK/8 | Standard |
| 0xC | 1 | 1 | 0 | 0 | Eco | MCLK/1 | One-shot |
| 0xD | 1 | 1 | 0 | 1 | Median | MCLK/1 | One-shot |
| 0xE | 1 | 1 | 1 | 0 | Fast | MCLK/2 | One-shot |
| 0xF | 1 | 1 | 1 | 1 | Fast | MCLK/1 | One-shot |

### Configuration Example

In the example in Table 21, the lowest current consumption is used, and the AD7768 is connected to an FPGA. The FORMATx pins are set such that all eight data outputs, DOUT0 to DOUT7, connect to the field-programmable gate array (FPGA). For the lowest power, the lowest DCLK frequency is used. The input bandwidth is set through the combination of selecting decimation by 64 and selecting the wideband filter.

$$ODR = f_{MOD} \div Decimation\ Ratio$$

where:
*MCLK* = 32.768 MHz.
$f_{MOD}$ is MCLK/32 for eco mode (see Table 18).
*Decimation Ratio* = 64.

Thus, for this example, where MCLK = 32.768 MHz,

$$ODR = (32.768\ \text{MHz}/32) \div 64 = 16\ \text{kHz}$$

Minimizing the DCLK frequency means selecting DCLK = MCLK/8. In this example, this results in a 4 MHz DCLK signal. The period of DCLK in this case is 1/4 MHz = 250 ns. The data conversion on each DOUTx pin is 32 bits long. The conversion data takes 32 × 250 ns = 8 µs to be output. All 32 bits must be output within the ODR period of 1/16 kHz, which is approximately 64 µs. In this case, the 8 µs required to read out the conversion data is well within the 64 µs between conversion outputs. Therefore, this combination, which is summarized in Table 21, is viable for use.

### Channel Standby

Table 20 shows how the user can put channels into standby mode. Set either ST0 or ST1 to Logic 1 to place banks of four channels into standby mode. When in standby mode, the disabled channels hold their position in the output data stream. The 8-bit header and 24-bit conversion result are set to all zeros when the ADC channels are set to standby.

**Table 20. Truth Table for the ST0 and ST1 Pins**

| ST1 | ST0 | Function |
|---|---|---|
| 0 | 0 | All channels operational. |
| 0 | 1 | Channel 0 to Channel 3 in standby. Channel 4 to Channel 7 operational. |
| 1 | 0 | Channel 4 to Channel 7 in standby. Channel 0 to Channel 3 operational. |
| 1 | 1 | All channels in standby. |

## SPI CONTROL

The AD7768 has a 4-wire SPI interface that is compatible with QSPI™, MICROWIRE®, and DSPs. The interface operates in SPI Mode 0. In SPI Mode 0, SCLK idles low, the falling edge of $\overline{CS}$ clocks out the MSB, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

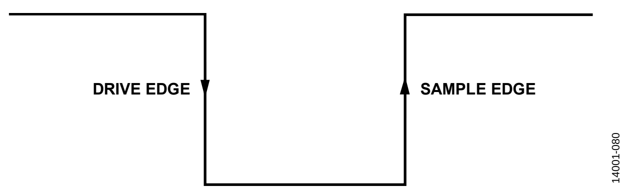



*Figure 81. SPI Mode SCLK Edges*

### Accessing the ADC Register Map

To use SPI control mode, set the $\overline{PIN}$/SPI pin to logic high. The SPI control operates as a 16-bit, 4-wire interface, allowing read and write access. Figure 82 shows the interface format between the AD7768 and the digital host.

The SPI serial control interface of the AD7768 is an independent path for controlling and monitoring the AD7768. There is no direct link to the data interface. Both the MCLK and DCLK signals can be configured by the SPI control interface. However, the MCLK and DCLK timing is not related in any way to the timing of the SPI control interface.

**Table 21. MODEx Example Selection**

| Mode Hex. | MODE3 | MODE2 | MODE1 | MODE0 | Power Mode | DCLK Frequency | Data Conversion |
|---|---|---|---|---|---|---|---|
| 0×3 | 0 | 0 | 1 | 1 | Eco | MCLK/8 | Standard |

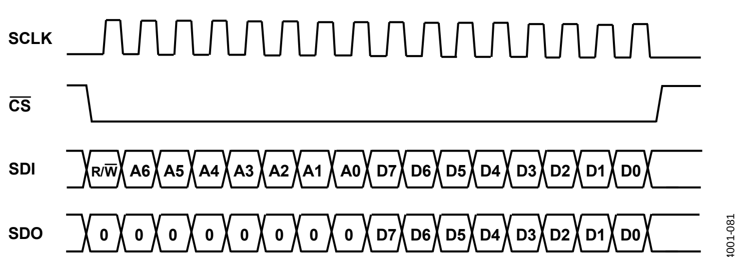



*Figure 82. Write/Read Command*

### SPI Interface Details

Each SPI access frame is 16 bits long. The MSB (Bit 15) of the SDI command is the R/W bit; 1= read and 0 = write. Bits[14:8] of the SDI command are the address bits.

The SPI control interface uses an off frame protocol. This means that the master (FPGA/DSP) communicates with the AD7768 in two frames. The first frame sends a 16-bit instruction R/W, address, and data) and the second frame is the response where the AD7768 sends 16 bits back to the master.

During the master write command, the SDO output contains eight leading zeros, followed by eight bits of data, as shown in Figure 82.

Figure 83 illustrates the off frame protocol. Register access responses are always offset by one CS frame. In Figure 83, the response (READ RESP 1) to the first command (CMD 1) is output by the AD7768 during the following CS frame at the same time as the second command (CMD 2) is being sent.

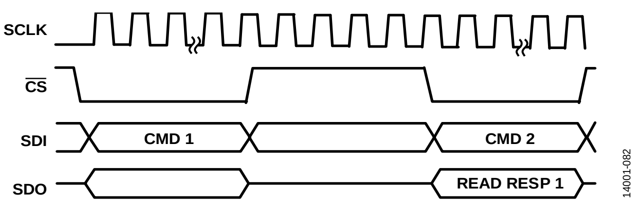



Figure 83. Off Frame Protocol

### SPI Control Interface Error Handling

The AD7768 SPI control interface detects if it has received an illegal command. An illegal command is a write to a read only register, a write to a register address that does not exist, or a read from a register address that does not exist. If any of these illegal commands are received by the AD7768, it responds with an error output of 0x0E00.

### SPI Reset Configuration

After power-on or reset, the AD7768 default configuration is set to the following low current consumption settings:

- Eco power mode with MCLK/32.
- Interface configuration of DCLK = MCLK/8, header output enabled, and CRC disabled.
- Filter configuration of Channel Mode A and Channel Mode B is set to sinc5 and decimation = ×1024. Channel mode select is set to 0x00, and all channels are assigned to Channel Mode A.
- Channel configuration of Channel 0 to Channel 7 is enabled, with the analog input buffers enabled. The reference precharge buffers are disabled. The offset, gain, and phase calibration are set to the zero position.
- Continuous conversion mode is enabled.

## SPI CONTROL FUNCTIONALITY

SPI control offers the superset of flexibility and diagnostics to the user. The following sections highlight the functionality and diagnostics offered when SPI control is used.

After any change to these configuration register settings, the user must provide a sync signal to the AD7768 through either the SPI_SYNC command, or by applying the appropriate pulse to the START pin or SYNC_IN pin to ensure that the configuration changes are applied correctly to the ADC and digital filters.

### Channel Configuration

The AD7768 has eight fully differential analog input channels. The channel configuration registers allow the AD7768 channel to be individually configured to adapt to the measurement required on that channel. Channels can be enabled or disabled using the channel standby register, Register 0x00. Analog input and reference precharge buffers can be assigned per input terminal. Gain, offset, and phase calibration can be controlled on a per channel basis using the calibration register. See the Per Channel Calibration Gain and Offset and Sync Phase section for more information.

### Filter Configuration Registers

In SPI control mode, the user can set up two channel modes, Channel Mode A (Register 0x01), and Channel Mode B (Register 0x02). Each channel mode register can have a specific filter type and decimation ratio. Using the channel mode selection register (Register 0x03), the user can assign either Channel Mode A or Channel Mode B to each channel.

**Table 22. Channel Mode A/Channel Mode B, Register 0x01 and Register 0x02**

| Bits | Bit Name | Setting | Description | Reset | Access |
|---|---|---|---|---|---|
| 3 | FILTER_TYPE_x | | Filter output | 0x1 | RW |
| | | 0 | Wideband filter | | |
| | | 1 | Sinc5 filter | | |
| [2:0] | DEC_RATE_x | | Decimation rate | 0x5 | RW |
| | | 000 to 101 | ×32 to ×1024 | | |

**Table 23. Channel Mode Selection, Register 0x03**

| Bits | Bit Name | Setting | Description | Reset | Access |
|---|---|---|---|---|---|
| [7:0] | CH_x_MODE | | Channel x | 0x0 | RW |
| | | 0 | Mode A | | |
| | | 1 | Mode B | | |

### Reset over SPI Control Interface

Two successive commands must be written to the AD7768 data control register to initiate a full reset of the device over the SPI interface. This action fully resets all registers to the default conditions. Details of the commands and their sequence are shown in Table 40.

After a reset over the SPI control interface, the first command sent to the AD7768 is responded to with 0x0E00 by the device. This response, in addition the fact that all registers have assumed their default values, indicates that the software reset succeeded.

### Sleep Mode

Sleep mode puts the AD7768 into its lowest power mode. In sleep mode, all clocks are internally gated and all ADCs are disabled. A large portion of the digital core is inactive.

The AD7768 SPI remains active and is available to the user when in sleep mode. Write to Register 0x04, Bit 7 to exit sleep mode. For the lowest power consumption, select the sinc5 filter before entering sleep mode.

### Channel Standby Mode

For efficient power usage, users can place selected channels into standby mode when not in use. Setting the bits in Register 0x00 disables the corresponding channel (see Table 34). For maximum power savings, switch disabled channels to the sinc5 filter using the channel mode configurations. This disables the wideband filter in the digital core and gives additional power savings.

### Clocking Selections

The internal modulator frequency ($f_{MOD}$) that is used by each of the ADCs in the AD7768 is derived from the externally applied MCLK signal. The MCLK division bits allow the user to control the ratio between the MCLK frequency and the internal modulator clock frequency. This allows the user to select the division ratio which is best for their configuration.

This depends on the power mode, the decimation rate, and the base MCLK available in the system. See the Clocking and Sampling Tree section for further information on setting MCLK_DIV correctly.

### MCLK Source Selection

The following clocking options are available as the MCLK input source in SPI mode:

- LVDS
- External crystal
- CMOS input MCLK

Setting CLK_SEL to logic low configures the AD7768 for correct operation using a CMOS clock. Setting CLK_SEL to logic high enables the use of an external crystal.

If CLK_SEL is set to logic high and Bit 3 of Register 0x04 is also set, the application of an LVDS clock signal to the MCLK pin is enabled. LVDS clocking is exclusive to SPI mode and requires the register selection for operation (see Table 38).

The DCLK rate is derived from MCLK. DCLK division (the ratio between MCLK and DCLK) is controlled in the interface configuration selection register, Register 0x07 (see Table 41).

### Interface Configuration

The data interface is a master output interface, where ADC conversion results are output by the AD7768 at a rate based on the mode selected. The interface consists of a data clock (DCLK), the data ready ($\overline{\text{DRDY}}$) framing output, and the data output pins (DOUT0 to DOUT7). The interface can be configured to output conversion data on one, two, or eight of the DOUTx pins. The DOUTx configuration is selected using the FORMATx pins (see Table 28).

The DCLK rate is a direct division of the MCLK input and can be controlled using Bits[1:0] of Register 0x07. The minimum DCLK rate can be calculated as

$$DCLK\ (minimum) = Output\ Data\ Rate \times Channels\ per\ DOUTx \times 32\ \text{bits}$$

where MCLK ≥ *DCLK*.

With eight ADCs enabled, an MCLK rate of 32.768 MHz, an ODR of 256 kSPS, and two DOUTx channels, DCLK (minimum) is

$$256\ \text{kSPS} \times 4\ \text{channels per DOUTx} \times 32\ \text{bits} = 32.768\ \text{MHz}$$

where DCLK = MCLK/1.

For more information on the status header, CRC, and interface configuration, see the Data Interface section.

### CRC Protection

The AD7768 can be configured to output a CRC message per channel every 4 or 16 samples. This function is available only with SPI control. CRC is enabled in the interface control register, Register 0x07 (see the CRC Check on Data Interface section).

### ADC Synchronization over SPI

The ADC synchronization over SPI allows the user to request a synchronization pulse to the ADCs over the SPI interface. To initiate the synchronization in this manner, write to Bit 7 in Register 0x06 twice.

First, the user must write a 0, which sets $\overline{\text{SYNC\_OUT}}$ low, and then write a 1 to set the $\overline{\text{SYNC\_OUT}}$ logic high again.

The SPI_SYNC command is recognized after the last rising edge of SCLK in the SPI instruction, where the SPI_SYNC bit is changed from low to high. The SPI_SYNC command is then output synchronously to the AD7768 MCLK signal on the $\overline{\text{SYNC\_OUT}}$ pin. The user must connect the $\overline{\text{SYNC\_OUT}}$ signal to the $\overline{\text{SYNC\_IN}}$ pin on the printed circuit board (PCB).

The $\overline{\text{SYNC\_OUT}}$ pin may also be routed to the $\overline{\text{SYNC\_IN}}$ pins of other AD7768 devices, allowing simultaneous sampling to occur across larger channel count systems. Any daisy-chained system of AD7768 devices requires that all ADCs be synchronized.

As per any synchronization pulse present on the $\overline{\text{SYNC\_IN}}$ pin, the digital filters of the AD7768 are reset by the SPI_SYNC command. The full settling time of the filters must then elapse before valid data is output on the data interface.

### *Analog Input Precharge Buffers*

The AD7768 contains precharge buffers on each analog input to ease the drive requirements on the external amplifier. Each analog input precharge buffer can be enabled or disabled using the analog input precharge buffer registers (see Table 48 and Table 49).

### *Reference Precharge Buffers*

The AD7768 contains reference precharge buffers on each reference input to ease the drive requirements on the external reference and help to settle any nonlinearity on the reference inputs. Each precharge reference buffer can be enabled or disabled using the precharge reference buffer registers (see Table 50 and Table 51).

### *Per Channel Calibration Gain and Offset and Sync Phase*

The user can adjust the gain, offset, and sync phase of the AD7768. These options are available only in SPI mode. Further register information and calibration instructions are available in the Offset Registers section, the Gain Registers section, and the Sync Phase Offset Registers section. See the Calibration section for information on calibration equations.

### *GPIOs*

The AD7768 has five general-purpose input/output (GPIO) pins available when operating in SPI mode. For further information on GPIO configuration, see the GPIO Functionality section.

## SPI MODE EXTRA DIAGNOSTIC FEATURES

### *RAM Built In Self Test*

The RAM built in self test (BIST) is a coefficient check for the digital filters. The AD7768 DSP path uses some internal memories for storing data associated with filtering and calibration. A user may, if desired, initiate a built in self test (BIST) of these memories. Normal conversions are not possible while BIST is running. The test is started by writing to the BIST control register, Register 0x08. The results and status of the test are available in the status register, Register 0x09 (see Table 34).

### *Revision Identification Number*

The AD7768 contains an identification register that can be accessed in SPI mode, the revision identification register. This register is an excellent way to verify the correct operation of the serial control interface. Register information is available in the Revision Identification Register section.

### *Diagnostic Meter Mode*

The diagnostic metering mode can be used to verify the functionality of each ADC by internally passing a positive full-scale, midscale, or negative full-scale voltage to the ADC. The user can then read the resulting ADC conversion result to determine that the ADC is operating correctly. To configure ADC conversion diagnostics, see the ADC Diagnostic Receive Select Register section and the ADC Diagnostic Control Register section.

# CIRCUIT INFORMATION

## CORE SIGNAL CHAIN

Each ADC channel on the AD7768 has an identical signal path from the analog input pins to the data interface. Figure 84 shows a top level implementation of the core signal chain. Each ADC channel has its own Σ-Δ modulator that oversamples the analog input and passes the digital representation to the digital filter block. The modulator sampling frequency ($f_{MOD}$) ranges are explained in the Clocking and Sampling Tree section. The data is filtered, scaled for gain and offset (depending on user settings), and then output on the data interface. Control of the flexible settings for the signal chain is provided by either using the pin control or the SPI control set at power-up by the state of the PIN/SPI input pin.

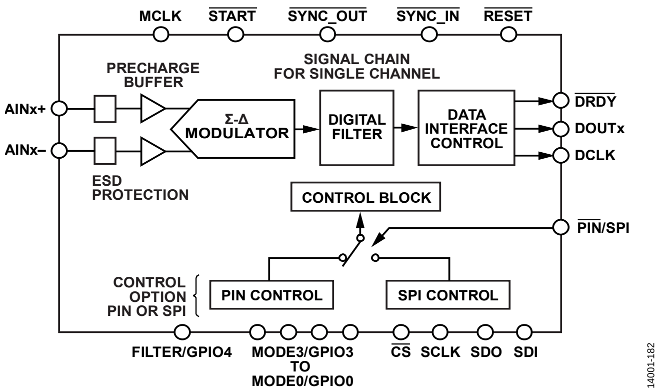



Figure 84. Top Level Core Signal Chain and Control

The AD7768 can use up to a 5 V reference and converts the differential voltage between the analog inputs (AINx+ and AINx−) into a digital output. The analog inputs can be configured as either differential or pseudo differential inputs. As a pseudo differential input, either AINx+ or AINx− can be connected to a constant input voltage (such as 0 V, GND, AVSS, or some other reference voltage). The ADC converts the voltage difference between the analog input pins into a digital code on the output. Using a common-mode voltage of AVDD1/2 for the analog inputs, AINx+ and AINx−, maximizes the ADC input range. The 24-bit conversion result is in twos complement, MSB first, format. Figure 85 shows the ideal transfer functions for the AD7768.

### *ADC Power Modes*

The AD7768 has three selectable power modes. In pin control mode, the modulator rate and power mode are tied together for best performance. In SPI control mode, the user can select the power mode and modulator MCLK divider settings. This gives more flexibility to control the bandwidth and power dissipation for the AD7768. Table 10 shows the $f_{MOD}$ frequencies allowed for each power mode and Table 38 shows the register information.

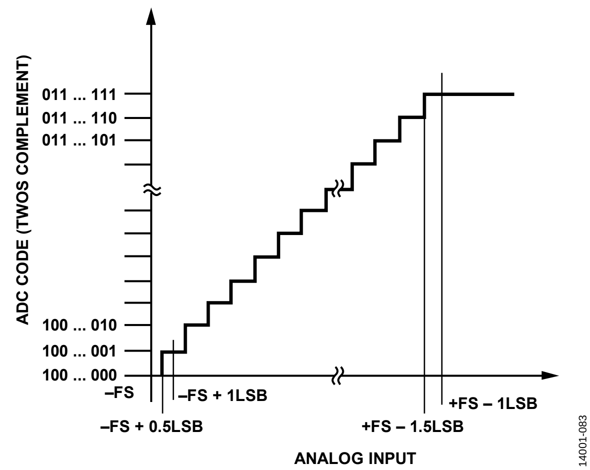



*Figure 85. ADC Ideal Transfer Functions (FS is Full-Scale)*

## ANALOG INPUTS

Figure 86 shows the AD7768 analog front end. Shown on the signal path are the ESD protection diodes that are designed to protect the ADC from some short duration overvoltage and ESD events. The analog input is sampled at twice the modulator sampling frequency, $f_{MOD}$, which is derived from MCLK. By default, the ADC internal sampling capacitors, CS1 and CS2, are driven by a per channel analog input precharge buffer, to ease the driving requirement of the external network.

The analog input precharge buffers provide the initial rough charging of the switched capacitor network for 25% of the sampling phase. For the final remaining 75% of sampling phase, the fine accuracy settling charge is provided by the external source.

The analog input precharge buffers reduce the switching kickback from the sampling stage to the external circuitry. It reduces the average input current by a factor of eight, and makes the input current more signal independent, to reduce the effects of sampling distortion. This reduction in drive requirements allows pairing of the AD7768 with lower power, lower bandwidth front end driver amplifiers such as the ADA4940-2.

**Table 24. Output Codes and Ideal Input Voltages**

| Description | Analog Input (AINx+ – (AINx–)) $V_{REF}$ = 4.096 V | Digital Output Code, Twos Complement (Hex.) |
|---|---|---|
| FS – 1 LSB | +4.095999512 V | 0x7FFFFF |
| Midscale + 1 LSB | +488 nV | 0x000001 |
| Midscale | 0 V | 0x000000 |
| Midscale – 1 LSB | −488 nV | 0xFFFFFF |
| −FS + 1 LSB | −4.095999512 V | 0x800001 |
| −FS | −4.096 V | 0x800000 |

The analog input precharge buffers can be turned on/off by means of a register write to Register 0x11 and Register 0x12 (Precharge Buffer Register 1 and Precharge Buffer Register 2). Each analog input precharge buffer is selectable per channel. In pin control mode, the analog input precharge buffers are always enabled for optimum performance.

When the precharge analog input buffers are disabled, the analog input current is sourced completely from the analog input source. The unbuffered analog input current is calculated from two components: the differential input voltage on the analog input pair, and the analog input voltage with respect to AVSS. With the precharge buffers disabled, for 32.768 MHz MCLK in fast mode with $f_{MOD}$ = MCLK/4, the differential input current is approximately 48 µA/V and the current with respect to ground is approximately 16 µA/V.

For example, if the precharge buffers are off, with AIN1+= 5 V, and AIN1− = 0 V, estimate the current in each input pin as follows:

AIN1+ = 5 V × 48 µA/V + 5 V × 16 µA/V = 320 µA

AIN1− = −5 V × 48 µA/V + 0 V × 16 µA/V = −240 µA

When the precharge buffers are enabled, the absolute voltage with respect to AVSS determines the majority of the current. The maximum input current of approximately −25 µA is measured when the analog input is close to either the AVDD1 or AVSS rails.

With either precharge buffers enabled or disabled, the analog input current scales linearly with the modulator clock rate. The analog input current versus input voltage is shown in Figure 87.

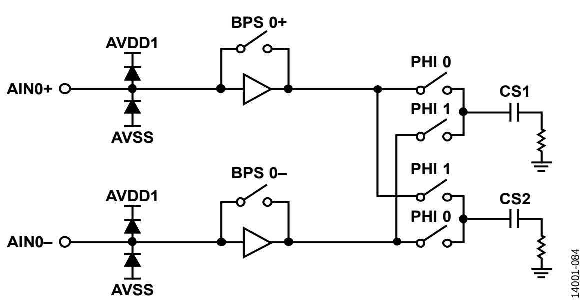



*Figure 86. Analog Front End*

Full settling of the analog inputs to the ADC requires the use of an external amplifier. Pair amplifiers such as the ADA4805-2 for eco mode, the ADA4807-2 or ADA4940-2 for median mode, and the ADA4807-2 or ADA4896-2 for fast mode with the AD7768. Use the ADA4940-2 with a 4.096 V reference to give the amplifier sufficient headroom and foot room to achieve the best distortion performance from the amplifier. Running the AD7768 in median and eco modes or reducing the MCLK rate reduces the load and speed requirements of the amplifier; therefore, lower power amplifiers may be paired with the analog inputs to achieve the optimum signal chain efficiency.

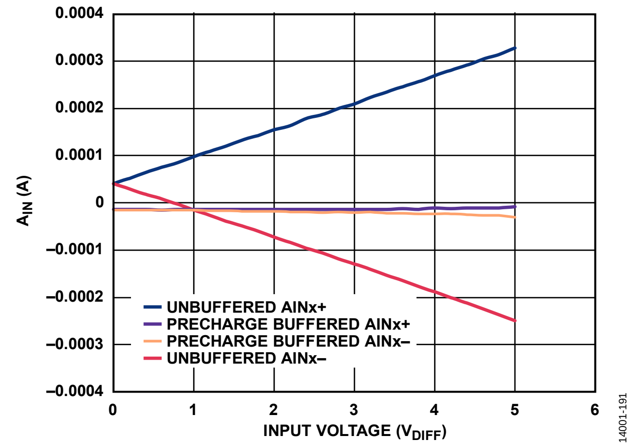



*Figure 87. Analog Input Current ($A_{IN}$) vs. Input Voltage Precharge Buffer On/Off, $V_{CM}$ = 2.5 V*

## VCM

The AD7768 provides a buffered common-mode voltage output on Pin 59. This output can bias up analog input signals. By incorporating the VCM buffer into the ADC, the AD7768 reduces component count and board space. In pin control mode, the VCM potential is fixed to (AVDD1 − AVSS)/2, and is enabled by default.

In SPI mode, configure the VCM potential using the general configuration register (Register 0x05). The output can be enabled or disabled, and set to (AVDD1 − AVSS)/2, 1.65 V, 2.14 V, or 2.5 V, with respect to AVSS.

## REFERENCE INPUT

The AD7768 has two differential reference input pairs: REF1+ and REF1− for Channel 0 to Channel 3, and REF2+ and REF2− for Channel 4 to Channel 7. The absolute input reference voltage range is 1 V to AVDD1 − AVSS.

Like the analog inputs, the reference inputs have a precharge buffer option. Each ADC has an individual buffer for each REFx+ and REFx−. The precharge buffers help reduce the burden on the external reference circuitry.

In pin control mode, the precharge reference buffers are off by default. In SPI mode, the user can enable or disable the reference precharge buffers. In the case of unipolar analog supplies, in SPI mode, the user can achieve the best performance and power efficiency by enabling only the REFx+ buffers. The reference input current scales linearly with the modulator clock rate.

For 32 MHz MCLK and MCLK/4 fast mode, the differential input current is ~72 µA/V unbuffered, and ~16 µA/V with the precharge buffers enabled.

With the precharge buffers off, REFx+ = 5 V, and REFx− = 0 V,

REFx± = 5 V × 72 µA/V = 360 µA

With the precharge buffers on, REFx+ = 5 V, and REFx− = 0 V,

REFx± = 5 V × 16 µA/V = 80 µA

For the best performance and headroom, it is recommended to use a 4.096 V reference such as the ADR444 or the ADR4540.

For the best performance at high sampling rates, it is recommended to use an external reference drive amplifier such as the ADA4841-1 or the AD8031.

## CLOCK SELECTION

The AD7768 has an internal oscillator that is used for initial power-up of the device. After the AD7768 has completed its start-up routine, a clock handover to the externally applied MCLK normally occurs. The AD7768 counts the falling edges of the external MCLK over a given number of internal clock cycles to determine if the clock is valid and at least a frequency of 1.15 MHz. If there is a fault with the external MCLK, the handover does not occur and the AD7768 outputs an error in the status header and the clock error bit is set in the device status register. No conversion data is output and a reset is required to exit this error state.

Three clock source input options are available to the AD7768: external CMOS, crystal oscillator, or LVDS. The clock is selected on power-up and is determined by the state of the CLK_SEL pin.

If CLK_SEL = 0, the CMOS clock option is selected and the clock is applied to Pin 32 (Pin 31 is tied to DGND).

If CLK_SEL = 1, the crystal or LVDS option is selected and the crystal or LVDS is applied to Pin 31 and Pin 32. The LVDS option is available only in SPI control mode. An SPI write to Bit 3 of Register 0x04 enables the LVDS clock option.

## DIGITAL FILTERING

The AD7768 offers two types of digital filters. In SPI control mode, these filters can be chosen on a per channel basis. In pin control mode, only one filter can be selected for all channels. The digital filters available on the AD7768 are

- Sinc5 low latency filter, −3 dB at 0.2 × ODR
- Wideband low ripple filter, −3 dB at 0.433 in specs × ODR

Both filters can be operated in one of six different decimation rates, allowing the user to choose the optimal input bandwidth and speed of the conversion versus the desired power mode or resolution.

### *Sinc5 Filter*

Most precision Σ-Δ ADCs use a sinc filter. The sinc5 filter offered in the AD7768 enables a low latency signal path useful for dc inputs, for control loops, or where other specific postprocessing is required. The sinc5 filter path offers the lowest noise and power consumption. The sinc5 filter has a −3 dB BW of 0.2 × ODR. Table 12 contains the noise performance for the sinc5 filter across power modes and decimation ratios.

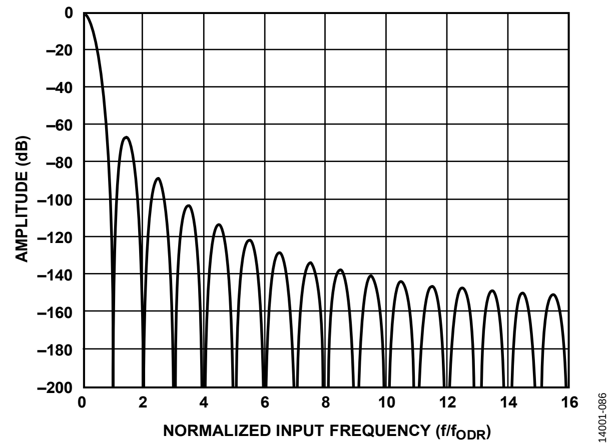



*Figure 88. Sinc5 Filter Frequency Response (Decimation = ×32)*

The settling times for the AD7768 when using the sinc5 filter are shown in Table 32.

### *Wideband Low Ripple Filter*

The wideband filter has a low ripple pass band, within ±0.005 dB of ripple, of 0.4 × ODR. The wideband filter has full attenuation at 0.499 × ODR (Nyquist), maximizing antialias protection. The wideband filter has a pass-band ripple of ±0.005 dB and a stop band attenuation of 105 dB from Nyquist out to $f_{CHOP}$. For more information on antialiasing and $f_{CHOP}$ aliasing, see the Antialiasing section.

The wideband filter is a very high order digital filter with a group delay of approximately 34/ODR. After a synchronization pulse, there is an additional delay from the $\overline{SYNC\_IN}$ rising edge to fully settled data. The settling times for the AD7768 when using the wideband filter are shown in Table 31. See Table 11 for the noise performance of the wideband filter across power modes and decimation rates.

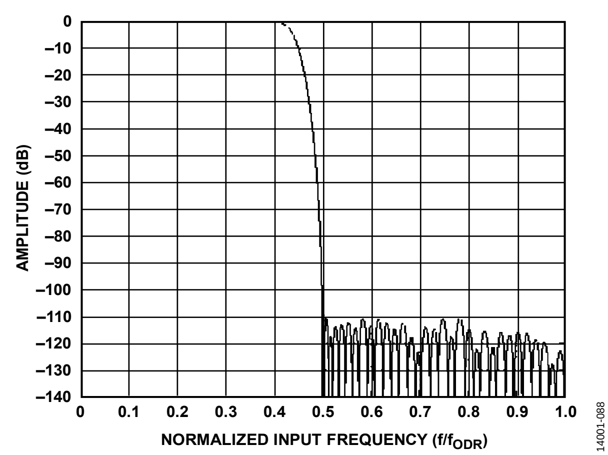



*Figure 89. Wideband Filter Frequency Response*

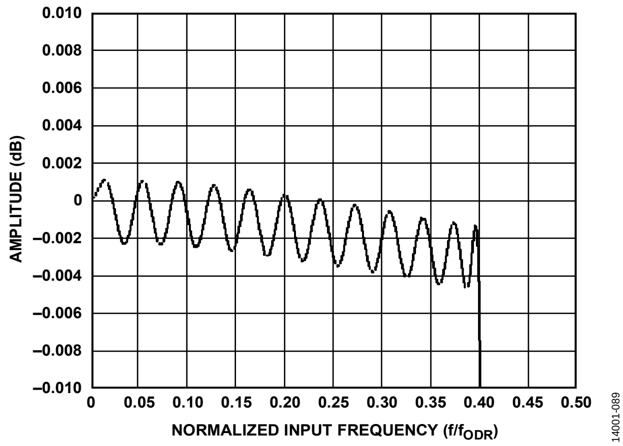



*Figure 90. Wideband Filter Pass-Band Ripple*

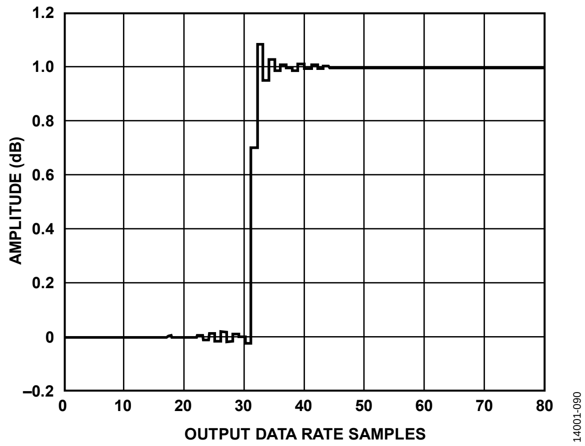



*Figure 91. Wideband Filter Step Response*

## DECIMATION RATE CONTROL

The AD7768 has programmable decimation rates for the digital filters. The decimation rates allow the user to reduce the measurement bandwidth, reducing the speed but increasing the resolution. When using the SPI control, control the decimation rate on the AD7768 through the channel mode registers. These registers set two separate channel modes with a given decimation rate and filter type. Each ADC is mapped to one of these modes via the channel mode select register. Table 25 details both the decimation rates available, and the filter types for selection, within Mode A and Mode B.

In pin control mode, the decimation ratio is controlled by the DEC0 and DEC1 pins; see Table 16 for decimation configuration in pin control mode.

**Table 25. Channel x Mode Registers, Register 0x01 and Register 0x02**

| Bits | Name | Logic Value | Decimation Rate |
|---|---|---|---|
| 3 | FILTER_TYPE_x | 0 | Wideband filter |
| | | 1 | Sinc5 filter |
| [2:0] | DEC_RATE_x | 000 | 32 |
| | | 001 | 64 |
| | | 010 | 128 |
| | | 011 | 256 |
| | | 100 | 512 |
| | | 101 | 1024 |
| | | 110 | 1024 |
| | | 111 | 1024 |

## ANTIALIASING

When designing an antialiasing filter for the AD7768, three main aliasing regions must be taken into account. After the alias requirements of each zone are understood, the user can design an antialiasing filter to meet the needs of the specific application. The three zones for consideration are related to the modulator sampling frequency, the modulator chopping frequency, and the modulator saturation point.

### *Modulator Sampling Frequency*

The AD7768 modulator signal transfer contains a zero, or notch, at odd multiples of $f_{MOD}$.

The modulator does not reject signals around its sampling frequency of 2 × $f_{MOD}$ or around even multiples of $f_{MOD}$. Figure 92 shows the modulator frequency response when using the wideband filter. The input frequency is swept from dc to 10 MHz. The rejection at the modulator rate is −35 dB. Table 26 shows the aliasing achieved by the filter options at the critical aliasing points mentioned in this section.

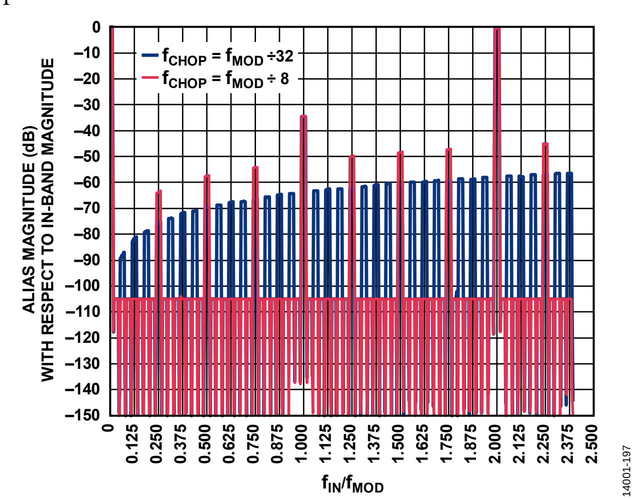



*Figure 92. Wideband Filter Stop Band Rejection, $f_{MOD}$ = 8.192 MHz*

### Modulator Chopping Frequency

The AD7768 uses a chopping technique in the modulator similar to that of a chopped amplifier to remove offset, offset drift, and 1/f noise. The AD7768 has a predetermined chopping rate of $f_{MOD}/32$ for pin control mode, and user selectable rates in SPI mode of $f_{MOD}/32$ or $f_{MOD}/8$.

The rate of chopping, $f_{CHOP}$, generates a tone that can appear at $(2 \times N \times f_{CHOP}) \pm f_{IN}$. Chopping at $f_{MOD}/32$ offers the best ac and dc performance for the AD7768. Chopping at $f_{MOD}/8$ offers better stop band attenuation by moving the first chopping tone further out of band, reducing the requirements of the analog filter. However, chopping at $f_{MOD}/8$ may lead to slightly degraded noise and offset performance compared to the default chop rate of $f_{MOD}/32$. Figure 92 displays the frequency response of the AD7768 when using the wideband filter for chopping frequencies of $f_{MOD}/32$ and $f_{MOD}/8$. Table 26 shows the aliasing achieved by the filter options at the critical aliasing points mentioned in this section.

**Table 26. External Antialiasing Filter Attenuation**

| RC Filter | $f_{MOD}/32$ (dB) | $f_{MOD}/16$ (dB) | $f_{MOD}/8$ (dB) | $2 \times f_{MOD}$ (dB) |
|---|---|---|---|---|
| First Order | −10 | −16 | −24 | −42 |
| Second Order | −20 | −32 | −48 | −84 |
| Third Order | −30 | −48 | −72 | −126 |

### Modulator Saturation Point

A Σ-Δ modulator can be thought of as a standard control loop, employing negative feedback. The control loop works to ensure that the average processed error signal is very small over time. It uses an integrator to remember preceding errors and force the mean error to be zero. As the input signal rate of change increases with respect to the modulator clock, $f_{MOD}$, a larger voltage feedback error is processed. Above a certain frequency, the error begins to saturate the modulator.

For the AD7768, the modulator may saturate for inputs greater than $f_{MOD}/16$, depending on the rate of change of input signal, input signal amplitude, and reference input level. A half power input tone at $f_{MOD}/8$ also causes the modulator to saturate. To protect against modulator saturation, a first-order antialiasing filter is required with a bandwidth of $f_{MOD}/16$.

## CALIBRATION

In SPI control mode, the AD7768 offers users the ability to adjust offset, gain, and phase delay on a per channel basis.

### Offset Adjustment

The CHx_OFFSET_MSB, CHx_OFFSET_MID, and CHx_OFFSET_LSB registers provide 24-bit, signed twos complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. As offset calibration occurs before gain calibration, the ratio above changes linearly with gain adjustment via the CHx gain registers (see Table 53). After a reset or power cycle, the offset register values revert to the default factory setting.

### Gain Adjustment

Each ADC channel has an associated gain coefficient. The coefficient is stored in three single-byte registers split up as MSB, MID, and LSB. Each of the gain registers are factory programmed. Nominally, this gain is around the value 0x555555 (for an ADC channel). The user may overwrite the gain register setting. However, after a reset or power cycle, the gain register values revert to the hard coded programmed factory setting.

Calculate the approximate result that is output using the following formula:

$$Data = \left( \frac{3 \times V_{IN}}{V_{REF}} \times 2^{21} - (Offset) \right) \times \frac{Gain}{4} \times \frac{4{,}194{,}300}{2^{42}}$$

where:
*Offset* is the offset register setting.
*Gain* is the gain register setting.

### Sync Phase Offset Adjustment

The AD7768 has one synchronization signal for all channels. The sync phase offset register allows the user to vary the phase delay on each of the channels relative to the synchronization edge received on the $\overline{\text{SYNC\_IN}}$ pin.

By default, all ADC channels react simultaneously to the $\overline{\text{SYNC\_IN}}$ pulse. The sync phase registers can be programmed to equalize known external phase differences on ADC input channels, relative to one another. The range of phase compensation is limited to a maximum of one conversion cycle, and the resolution of the correction depends on the decimation rate in use.

Table 27 displays the resolution and register bits used for phase offset for each decimation ratio.

**Table 27. Phase Delay Resolution**

| Decimation Ratio | Resolution | Steps | Phase Register Bits |
|---|---|---|---|
| ×32 | $1/f_{MOD}$ | 32 | [7:3] |
| ×64 | $1/f_{MOD}$ | 64 | [7:2] |
| ×128 | $1/f_{MOD}$ | 128 | [7:1] |
| ×256 | $1/f_{MOD}$ | 256 | [7:0] |
| ×512 | $2/f_{MOD}$ | 256 | [7:0] |
| ×1024 | $4/f_{MOD}$ | 256 | [7:0] |

# DATA INTERFACE

## SETTING THE FORMAT OF DATA OUTPUT

The data interface format is determined by setting the FORMATx pins. The logic state of the FORMATx pins are read on power-up and determine how many data lines (DOUTx) the ADC conversions are output on.

As the FORMATx pins are read on power-up of the AD7768 and the device remains in this output configuration, this function must always be hardwired and cannot be altered dynamically. Table 28, Figure 93, Figure 94, and Figure 95 show the formatting configuration for the digital output pins.

Calculate the minimum required DCLK rate for a given data interface configuration as follows:

*DCLK (minimum)* = *Output Data Rate* × *Channels per DOUTx* × 32

where MCLK ≥ DCLK.

For example, if MCLK = 32.768 MHz, with 2 DOUTx lines,

*DCLK (minimum)* = 256 kSPS × 4 channels per DOUTx × 32 = 32.768 Mbps

Therefore, DCLK = MCLK/1.

Or, if MCLK = 32.768 MHz, with 8 DOUTx lines,

*DCLK (minimum)* = 256 kSPS × 1 channel per DOUTx × 32 = 8.192 Mbps

Therefore, DCLK = MCLK/4.

**Table 28. FORMATx Truth Table**

| FORMAT1 | FORMAT0 | Description |
|---|---|---|
| 0 | 0 | Each ADC channel outputs on its own dedicated pin. DOUT0 to DOUT7 are in use. |
| 0 | 1 | The ADCs share the DOUT0 and DOUT1 pins: Channel 0 to Channel 3 output on DOUT0. Channel 4 to Channel 7 output on DOUT1. The ADC channels share data pins in time division multiplexed (TDM) output. DOUT0 and DOUT1 are in use. |
| 1 | X | All channels output on the DOUT0 pin, in TDM output. Only DOUT0 is in use. |

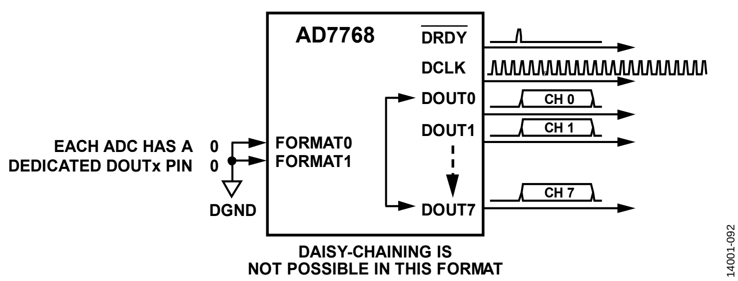



*Figure 93. FORMATx = 00, Eight Data Output Pins*

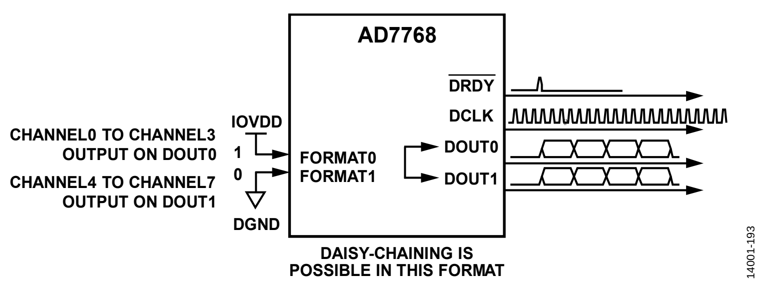



*Figure 94. FORMATx = 01, Two Data Output Pins*

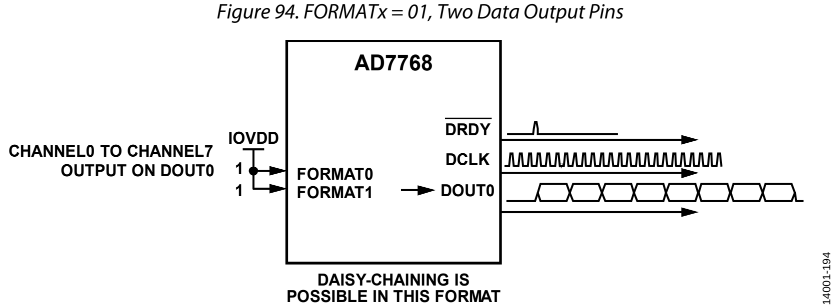



*Figure 95. FORMATx = 10 or 11, One Data Output Pin*

## ADC CONVERSION OUTPUT: HEADER AND DATA

The AD7768 data is output on the DOUT0 to DOUT7 pins, depending on the FORMATx pins. The actual structure of the data output for each ADC result is shown in Figure 96. Each ADC result comprises 32 bits. The first 8 bits are the header status bits, which contain status information and the channel number. The names of each of the header status bits are shown in Table 29, and their functions are explained in the subsequent sections. These header bits are followed by a 24-bit ADC output in twos complement coding, MSB first.

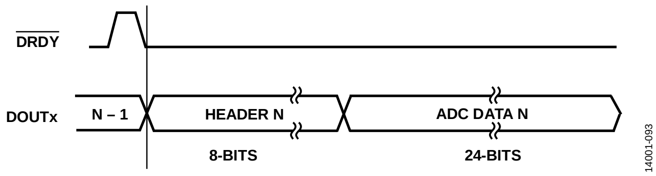



*Figure 96. ADC Output: 8-Bit Header, 24-Bit ADC Conversion Data*

**Table 29. Header Status Bits**

| Bit | Bit Name |
|---|---|
| 7 | CHIP_ERROR |
| 6 | Filter not settled |
| 5 | Repeated data |
| 4 | Filter type |
| 3 | Filter saturated |
| [2:0] | Channel ID[2:0] |

### Chip Error

The chip error bit indicates that a serious error has occurred. If this bit is set, a reset is required to clear this bit. This bit indicates that the external clock is not detected, a memory map bit flip, or an internal CRC error.

### Filter Not Settled

After power-up, reset, or synchronization, the AD7768 clears the digital filters and begins conversion. Due to the weighting of the digital filters, there is a delay from the first conversion to fully settled data. The settling times for the AD7768 when using the wideband and sinc5 filters are shown in Table 31 and Table 32, respectively. This bit is set if this settling delay has not yet elapsed.

### Repeated Data

If different channels use different decimation rates, data outputs are repeated for the slower speed channels. In these cases, the header is output as normal with the repeated data bit set to 1, and the following repeated ADC result is output as all zeros. This bit indicates that the conversion result of all zeros is not real; it indicates that there is a repeated data condition because two different decimation rates are selected. This condition can only occur during SPI control of the AD7768.

### Filter Type

In pin control mode, all channels operate using one filter selection. The filter selected in pin control mode is determined by the logic level of the FILTER pin. In SPI control mode, the digital filters can be selected on a per channel basis, using the mode registers. This header bit is 0 for channels using the wideband filter, and 1 for channels using the sinc5 filter.

### Filter Saturated

The filter saturated bit indicates that the filter output is clipping at either positive or negative full scale. The digital filter clips if the signal goes beyond the specification of the filter; it does not wrap. The clipping may be caused by the analog input exceeding the analog input range, or by a step change in the input which may cause overshoot in the digital filter. Clipping may also occur where the combination of the analog input signal and the channel gain register setting cause the signal seen by the filter to be higher than the analog input range.

### Channel ID

The channel ID bits indicate the ADC channel from which the succeeding conversion data originates (see Table 30).

**Table 30. Channel ID vs. Channel Number**

| Channel | Channel ID2 | Channel ID1 | Channel ID0 |
|---|---|---|---|
| Channel 0 | 0 | 0 | 0 |
| Channel 1 | 0 | 0 | 1 |
| Channel 2 | 0 | 1 | 0 |
| Channel 3 | 0 | 1 | 1 |
| Channel 4 | 1 | 0 | 0 |
| Channel 5 | 1 | 0 | 1 |
| Channel 6 | 1 | 1 | 0 |
| Channel 7 | 1 | 1 | 1 |

### Data Interface: Standard Conversion Operation

In standard mode operation, the AD7768 operates as the master and streams data to the DSP or FPGA. The AD7768 supplies the data, the data clock (DCLK), and a falling edge framing signal ($\overline{\text{DRDY}}$) to the slave device. All of these signals are synchronous. The data interface connections to DSP/FPGA are shown in Figure 100. The FORMATx pins determine how the data is output from the AD7768.

Figure 97 through Figure 99 show the data interface operating in standard mode at the maximum data rate. In all instances, $\overline{\text{DRDY}}$ is asserted one clock cycle before the MSB of the data conversion is made available on the data pin.

Each $\overline{\text{DRDY}}$ falling edge starts the output of the new ADC conversion data. The first 8 bits output after the $\overline{\text{DRDY}}$ falling edge are the header bits; the last 24 bits are the ADC conversion result.

Figure 97, Figure 98, and Figure 99 are distinct examples of the impact of the FORMATx pins on the AD7768 output operating in standard conversion operation. These figures represent running the AD7768 at maximum data rate for the three format options.

Figure 97 shows FORMATx = 00 each ADC has its own data out pin running at the MCLK/4 bit rate. In pin control mode, this is achieved by selecting Mode 0xA (fast mode, DCLK = MCLK/4, standard conversion, see Table 19) with the decimation rate set as ×32.

Figure 98 shows FORMATx = 01, where Channel 0 to Channel 3 share DOUT0 and Channel 4 to Channel 7 share DOUT1 at the maximum bit rate. In pin control mode, this is achieved by selecting Mode 0x8 (fast mode, DCLK = MCLK/1, standard conversion) with a decimation rate of ×32.

If running in pin control mode, the example shown in Figure 99 represents Mode 0x4 (median mode, DCLK = MCLK/1, standard conversion) with a decimation rate of ×32, giving the maximum output data capacity possible on one DOUTx pin.

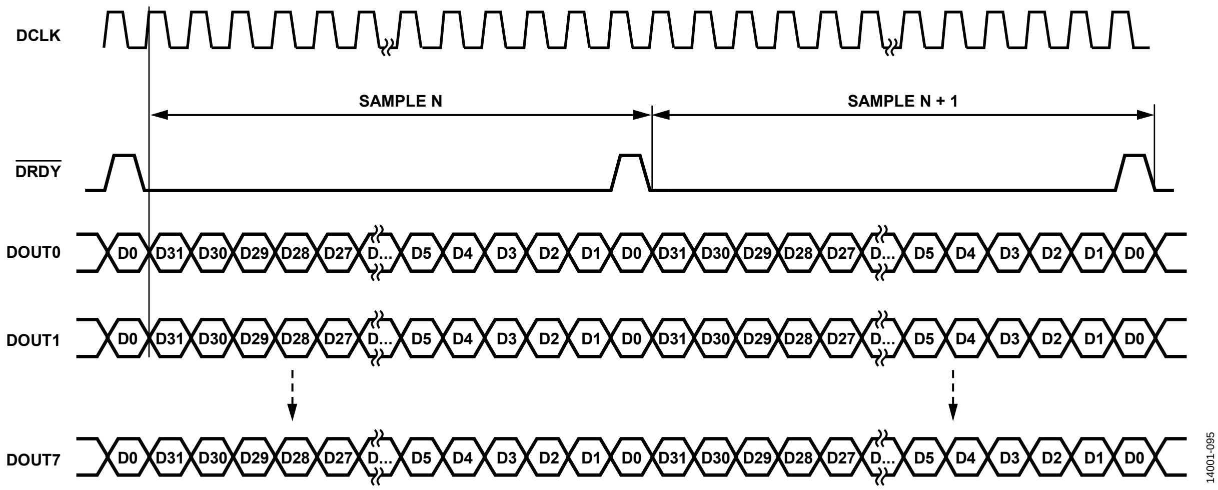



Figure 97. FORMATx = 00: Each ADC Has a Dedicated Data Out Pin, Maximum Data Rate

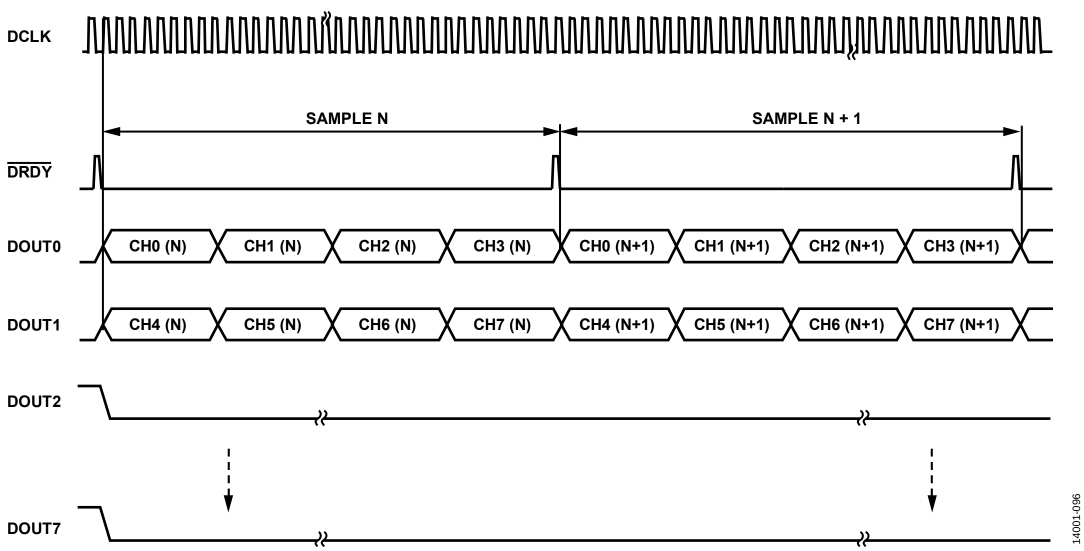



Figure 98. FORMATx = 01: Channel 0 to Channel 3 Share DOUT0, and Channel 4 to Channel 7 Share DOUT1, Maximum Data Rate

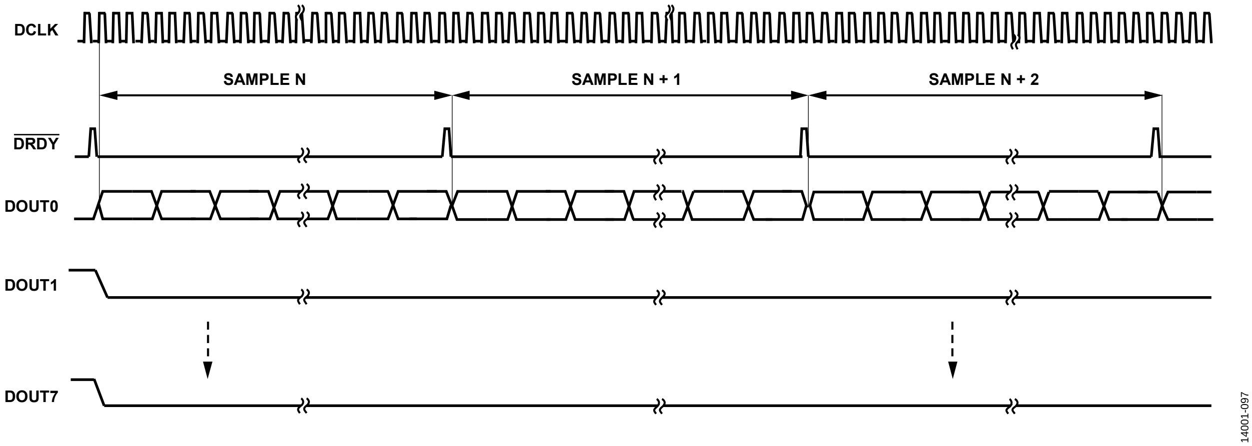



*Figure 99. FORMATx = 11 or 10: Channel 0 to Channel 7 Output on DOUT0 Only, Maximum Data Rate*

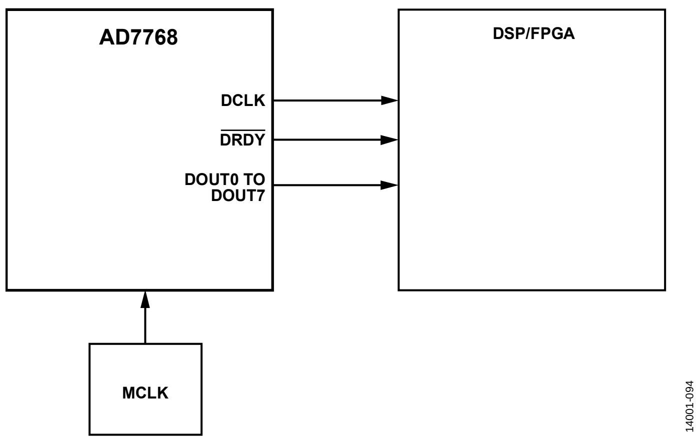



*Figure 100. Data Interface: Standard Conversion Operation, AD7768 = Master, DSP/FPGA = Slave*

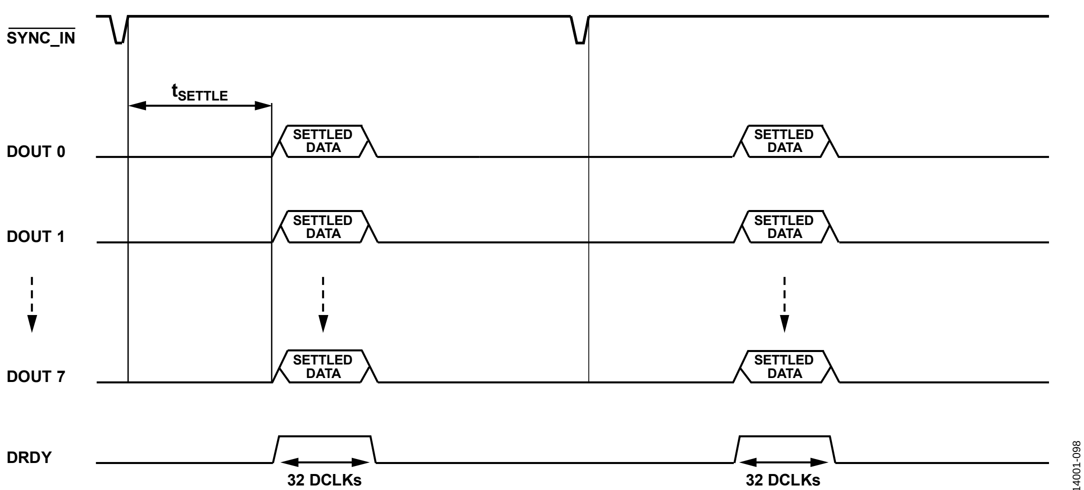



*Figure 101. One-Shot Mode*

### Data Interface: One-Shot Conversion Operation

One-shot mode is available in both SPI and pin control modes. This conversion mode is available by selecting one of Mode 0xC to Mode 0xF when in pin control mode. In SPI control mode, set Bit 4 (single-shot) of Register 0x06, the data control register. Figure 101 shows the device operating in one-shot mode.

In one-shot mode, the AD7768 is a pseudo slave. Conversions occur on request by the master device, for example, the DSP or FPGA. The SYNC_IN pin initiates the conversion request. In one-shot mode, all ADCs run continuously; however, the rising edge of the SYNC_IN pin controls the point in time from which data is output.

To receive data, the master must pulse the SYNC_IN pin to reset the filter and force DRDY low. DRDY subsequently goes high to indicate to the master device that the device has valid settled data available. Unlike standard mode, DRDY remains high for the number of clock periods of valid data before it goes low again; thus, in this conversion mode, it is an active high frame of the data.

When the master pulses SYNC_IN and the AD7768 receives the rising edge of this signal, the digital filter is reset and the full settling time of the filter elapses before the data is available. The duration of the settling time depends on the filter path and decimation rate. Running one-shot mode with the sinc5 filter allows the fastest throughput, because this filter has a lower settling time than the wideband filter.

As soon as settled data is available on any channel, the device outputs data from all channels. The contents of Bit 6 of the channel header status bits indicates if the data is fully settled.

The period before the data is settled on all channels ($t_{SETTLE}$) is shown in Figure 101. After the data has settled on all channels, DRDY is asserted high and the device outputs the required settled data on all channels before DRDY is asserted low. By adhering to the constraint of using the same filter and decimation rate on each ADC, the data is settled for all channels on the first DRDY output frame. This avoids a period of unsettled data prior to the settled data and ensures that all data is output at the same time on all ADCs. The device then waits for another SYNC_IN signal before outputting more data.

Because all the ADCs are sampling continuously, one-shot mode affects the sampling theory of the AD7768. Particularly, a user periodically sending a SYNC_IN pulse to the device is a form of subsampling of the ADC output. The SYNC_IN pulse must be synchronous with the master clock to ensure coherent sampling and reduce the effects of jitter on the frequency response.

### Daisy-Chaining

Daisy-chaining devices allows numerous devices to use the same data interface lines by cascading the outputs of multiple ADCs from separate AD7768 devices. Only one ADC device has its data interface in direct connection with the digital host. For the AD7768, this can be implemented by cascading DOUT0 and DOUT1 through a number of devices, or just using DOUT0; whether two data output pins or only one data output pin is enabled depends on the FORMATx pins. The ability to daisy-chain devices and the limit on the number of devices that can be handled by the chain is dependent on the power mode, DCLK, and decimation rate employed.

The maximum usable DCLK frequency allowed when daisy-chaining devices is limited by the combination of timing specifications in Table 3 or Table 5, as well as by the propagation delay of the data between devices and any skew between the MCLK signals at each AD7768 device. The propagation delay and MCLK skew are dependent on the PCB layout and trace lengths.

This feature is especially useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity.

When daisy-chaining, DOUT6 and DOUT7 become serial data inputs and DOUT0 and DOUT1 remain as serial data outputs under the control of the FORMATx pins.

Figure 102 shows an example of daisy-chaining when FORMATx = 01. In this case, the DOUT1 and DOUT0 pins of the AD7768 devices are cascaded to the DOUT6 and DOUT7 pins of the next device in the chain. Data readback is analogous to clocking a shift register where data is clocked on the rising edge of DCLK.

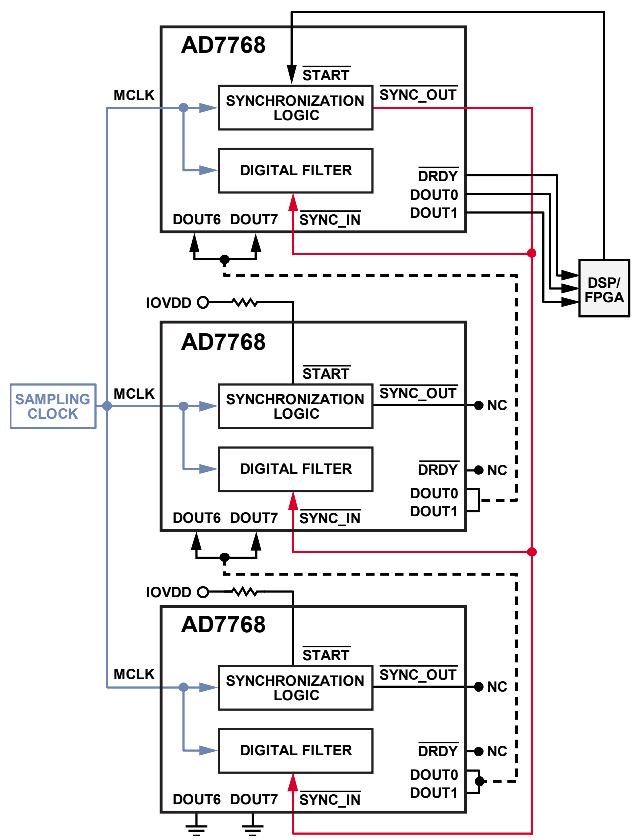



Figure 102. Daisy-Chaining Multiple AD7768 Devices

The scheme operates by passing the output data of the DOUT0 and DOUT1 pins of an AD7768 upstream device to the DOUT6 and DOUT7 inputs of the next AD7768 device downstream in the chain. The data then continues through the chain until it is clocked onto the DOUT0 and DOUT1 pins of the final downstream device in the chain. After power-up, two SYNC_IN pulses are required to initialize daisy-chain mode.

### Synchronization

An important consideration for daisy-chaining more than two AD7768 devices is synchronization. The basic provision for synchronizing multiple devices is that each device is clocked with the same base MCLK signal.

The AD7768 offers three options to allow ease of system synchronization. Choosing between the options depends on the system, but comes down to whether the user can supply a synchronization pulse that is truly synchronous with the base MCLK signal.

If the user cannot provide a signal that is synchronous to the base MCLK signal, one of the following two methods can be employed:

- Apply a START pulse to the first AD7768 device. The first AD7768 samples the asynchronous START pulse and generates a pulse on SYNC_OUT of the first device related to the base MCLK signal for distribution locally.
- Use synchronization over SPI (only available in SPI control mode) to write a synchronization command to the first AD7768 device. Similarly to the START pin method, the SPI sync generates a pulse on SYNC_OUT of the first device related to the base MCLK signal for distribution locally.

In both cases, route the SYNC_OUT pin of the first device to the SYNC_IN pin of that same device and to the SYNC_IN pins of all other devices that are to be synchronized. The SYNC_OUT pins of the other devices must remain open circuit. Tie all unused START pins to a Logic 1 through pull-up resistors.

If the user can provide a signal that is synchronous to the base MCLK, this signal can be applied directly to the SYNC_IN pin. Route the signal from a star point and connect it directly to the SYNC_IN pin of each AD7768 device. The signal is sampled on the rising MCLK edge; setup and hold times are associated with the SYNC_IN input are relative to the AD7768 MCLK rising edge.

In this case, tie the START pin Logic 1 through a pull-up resistor; SYNC_OUT is not used and can remain open circuit.

### CRC Check on Data Interface

The AD7768 delivers 32 bits per channel as standard, which by default consists of 8 status header bits and 24 bits of data.

The header bits default per the description in Table 29. However, there is also the option to employ a CRC check on the ADC conversion data. This functionality is available only when operating in SPI control mode. The function is controlled by CRC_SELECT in the interface configuration register (Register 0x07). When employed, the CRC message is calculated internally by the AD7768 on a per channel basis. The CRC then replaces the 8-bit header every four samples or every 16 samples.

When configured to output a CRC every four conversions, the AD7768 combines four 24-bit data outputs into a 96-bit word, Data N to Data N + 3 (see Figure 103).

The AD7768 uses a CRC polynomial to calculate the CRC message. The 8-bit CRC polynomial used is $x^8 + x^2 + x + 1$.

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight 1s.

The polynomial is aligned such that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned such that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

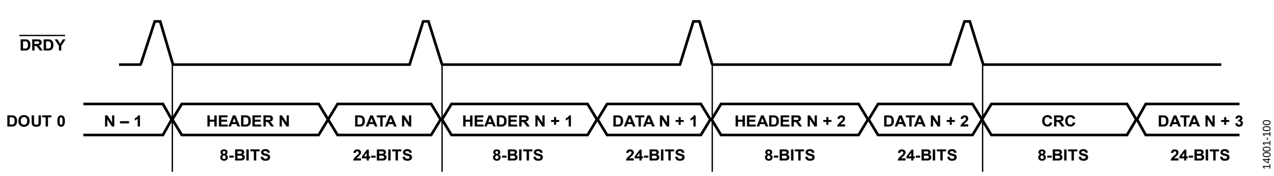



*Figure 103. CRC 4-Bit Stream*

**Table 31. Wideband Filter SYNC_IN to Settled Data[1]**

| Power Mode | Filter Type[2] | | Decimation Factor | | Delay from First MCLK Rise After SYNC_IN Rise to First DRDY Rise | | Delay from First MCLK Rise After SYNC_IN Rise to Earliest Settled Data DRDY Rise | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Group A | | Group B | |
| | Group A | Group B | Group A | Group B | MCLK Periods | Time (µs) (MCLK = 32.768 MHz) | MCLK Periods | Time (µs) (MCLK = 32.768 MHz) | MCLK Periods | Time (µs) (MCLK = 32.768 MHz) |
| Fast | WB | WB | 32 | N/A | 336 | 10.25391 | 8400 | 256.34766 | N/A | N/A |
| | WB | WB | 64 | N/A | 620 | 18.92090 | 16,748 | 511.10840 | N/A | N/A |
| | WB | WB | 128 | N/A | 1187 | 36.22437 | 33,443 | 1020.59937 | N/A | N/A |
| | WB | WB | 256 | N/A | 2325 | 70.95337 | 66,837 | 2039.70337 | N/A | N/A |
| | WB | WB | 512 | N/A | 4601 | 140.41138 | 133,625 | 4077.91138 | N/A | N/A |
| | WB | WB | 1024 | N/A | 9153 | 279.32739 | 267,201 | 8154.32739 | N/A | N/A |
| | WB | WB | 32 | 32 | 758 | 23.13232 | 8822 | 269.22607 | 8822 | 269.22607 |
| | WB | WB | 32 | 64 | 758 | 23.13232 | 8822 | 269.22607 | 17,014 | 519.22607 |
| | WB | WB | 32 | 128 | 758 | 23.13233 | 8822 | 269.22608 | 33,526 | 1023.13233 |
| | WB | WB | 32 | 256 | 758 | 23.13232 | 8822 | 269.22607 | 66,934 | 2042.66357 |
| | WB | WB | 32 | 512 | 758 | 23.13232 | 8822 | 269.22607 | 133,622 | 4077.81982 |
| | WB | WB | 32 | 1024 | 758 | 23.13232 | 8822 | 269.22607 | 267,253 | 8155.94482 |
| | WB | WB | 64 | 32 | 759 | 23.16284 | 17,015 | 519.25659 | 8823 | 269.25659 |
| | WB | WB | 128 | 32 | 760 | 23.19336 | 33,528 | 1023.19336 | 8824 | 269.28711 |
| | WB | WB | 256 | 32 | 762 | 23.25439 | 66,938 | 2042.78564 | 8826 | 269.34814 |
| | WB | WB | 512 | 32 | 782 | 23.86475 | 133,646 | 4078.55225 | 8846 | 269.95850 |
| | WB | WB | 1024 | 32 | 806 | 24.59717 | 267,302 | 8157.40967 | 8870 | 270.69099 |
| Median | WB | WB | 32 | N/A | 656 | 20.01953 | 16,784 | 512.20703 | N/A | N/A |
| | WB | WB | 64 | N/A | 1225 | 37.38403 | 33,481 | 1021.75903 | N/A | N/A |
| | WB | WB | 128 | N/A | 2359 | 71.99097 | 66,871 | 2040.74097 | N/A | N/A |
| | WB | WB | 256 | N/A | 4635 | 141.44898 | 133,659 | 4078.94898 | N/A | N/A |
| | WB | WB | 512 | N/A | 9187 | 280.36499 | 267,235 | 8155.36499 | N/A | N/A |
| | WB | WB | 1024 | N/A | 18,291 | 558.19702 | 534,387 | 16,308.19702 | N/A | N/A |
| | WB | WB | 32 | 32 | 820 | 25.02441 | 16,948 | 517.21191 | 16,948 | 517.21191 |
| | WB | WB | 32 | 64 | 820 | 25.02442 | 16,948 | 517.21192 | 33,588 | 1025.02467 |
| | WB | WB | 32 | 128 | 820 | 25.02441 | 16,948 | 517.21191 | 66,868 | 2040.64941 |
| | WB | WB | 32 | 256 | 820 | 25.02441 | 16,948 | 517.21191 | 133,684 | 4079.71191 |
| | WB | WB | 32 | 512 | 820 | 25.02441 | 16,948 | 517.21191 | 267,316 | 8157.83691 |
| | WB | WB | 32 | 1024 | 820 | 25.02441 | 16,948 | 517.21191 | 534,580 | 16,314.08691 |
| | WB | WB | 64 | 32 | 822 | 25.08545 | 33,590 | 1025.08545 | 16,950 | 517.27295 |
| | WB | WB | 128 | 32 | 824 | 25.14648 | 66,872 | 2040.77148 | 16,952 | 517.33398 |
| | WB | WB | 256 | 32 | 844 | 25.75684 | 133,708 | 4080.44434 | 16,972 | 517.94434 |
| | WB | WB | 512 | 32 | 836 | 25.51270 | 267,332 | 8158.32520 | 16,964 | 517.70020 |
| | WB | WB | 1024 | 32 | 852 | 26.00098 | 534,612 | 16,315.06348 | 16,980 | 518.18848 |
| Eco | WB | WB | 32 | N/A | 2587 | 78.94897 | 67,099 | 2047.69897 | N/A | N/A |
| | WB | WB | 64 | N/A | 4855 | 148.16286 | 133,879 | 4085.66284 | N/A | N/A |
| | WB | WB | 128 | N/A | 9391 | 286.59058 | 267,439 | 8161.59058 | N/A | N/A |
| | WB | WB | 256 | N/A | 18,495 | 564.42261 | 534,591 | 16,314.42261 | N/A | N/A |
| | WB | WB | 512 | N/A | 36,703 | 1120.08667 | 1,068,895 | 32,620.08667 | N/A | N/A |
| | WB | WB | 1024 | N/A | 73,119 | 2231.41480 | 2,137,503 | 65,231.41480 | N/A | N/A |
| | WB | WB | 32 | 32 | 2587 | 78.94898 | 67,099 | 2047.69898 | 67,099 | 2047.69898 |
| | WB | WB | 32 | 64 | 2587 | 78.94898 | 67,099 | 2047.69898 | 134,683 | 4110.19898 |
| | WB | WB | 32 | 128 | 2587 | 78.94898 | 67,099 | 2047.69898 | 267,803 | 8172.69898 |
| | WB | WB | 32 | 256 | 2587 | 78.94897 | 67,099 | 2047.69897 | 535,067 | 16,328.94897 |
| | WB | WB | 32 | 512 | 2587 | 78.94897 | 67,099 | 2047.69897 | 1,069,595 | 32,641.44897 |
| | WB | WB | 32 | 1024 | 2587 | 78.94898 | 67,099 | 2047.69898 | 2,137,627 | 65,235.19898 |
| | WB | WB | 64 | 32 | 2587 | 78.94898 | 134,683 | 4110.19898 | 67,099 | 2047.69898 |
| | WB | WB | 128 | 32 | 2587 | 78.94898 | 267,803 | 8172.69898 | 67,099 | 2047.69898 |
| | WB | WB | 256 | 32 | 2587 | 78.94898 | 535,067 | 16,328.94898 | 67,099 | 2047.69898 |
| | WB | WB | 512 | 32 | 2587 | 78.94898 | 1,069,595 | 32,641.44898 | 67,099 | 2047.69898 |
| | WB | WB | 1024 | 32 | 2587 | 78.94898 | 2,137,627 | 65,235.19898 | 67,099 | 2047.69898 |

[1] N/A means not applicable.
[2] WB means wideband.

**Table 32. Sinc5 Filter SYNC_IN to Settled Data[1, 2]**

| | Filter Type | | Decimation Factor | | Delay from First MCLK Rise After SYNC_IN Rise to First DRDY Rise | | Delay from First MCLK Rise After SYNC_IN Rise to Earliest Settled Data DRDY Rise | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Group A | | Group B | |
| Power Mode | Group A | Group B | Group A | Group B | MCLK Periods | Time (µs) (MCLK = 32.768 MHz) | MCLK Periods | Time (µs) (MCLK = 32.768 MHz) | MCLK Periods | Time (µs) (MCLK = 32.768 MHz) |
| Fast | Sinc | Sinc5 | 32 | N/A | 199 | 6.07300 | 839 | 25.60425 | N/A | N/A |
| | Sinc5 | Sinc5 | 64 | N/A | 327 | 9.97925 | 1607 | 49.04175 | N/A | N/A |
| | Sinc5 | Sinc5 | 128 | N/A | 583 | 17.79175 | 3143 | 95.91675 | N/A | N/A |
| | Sinc5 | Sinc5 | 256 | N/A | 1095 | 33.41675 | 6215 | 189.66675 | N/A | N/A |
| | Sinc5 | Sinc5 | 512 | N/A | 2119 | 64.66675 | 12359 | 377.16675 | N/A | N/A |
| | Sinc5 | Sinc5 | 1024 | N/A | 4167 | 127.16675 | 24,647 | 752.16675 | N/A | N/A |
| | Sinc5 | Sinc5 | 32 | 32 | 199 | 6.07300 | 839 | 25.60425 | 839 | 25.60425 |
| | Sinc5 | Sinc5 | 32 | 64 | 199 | 6.07300 | 839 | 25.60425 | 1607 | 49.04175 |
| | Sinc5 | Sinc5 | 32 | 128 | 199 | 6.07300 | 839 | 25.60425 | 3143 | 95.91675 |
| | Sinc5 | Sinc5 | 32 | 256 | 199 | 6.07300 | 839 | 25.60425 | 6215 | 189.66675 |
| | Sinc5 | Sinc5 | 32 | 512 | 199 | 6.07300 | 839 | 25.60425 | 12,359 | 377.16675 |
| | Sinc5 | Sinc5 | 32 | 1024 | 199 | 6.07300 | 839 | 25.60425 | 24,647 | 752.16675 |
| | Sinc5 | Sinc5 | 64 | 32 | 199 | 6.07300 | 1607 | 49.04175 | 839 | 25.60425 |
| | Sinc5 | Sinc5 | 1024 | 32 | 199 | 6.07300 | 24,647 | 752.16675 | 839 | 25.60425 |
| Median | Sinc5 | Sinc5 | 32 | N/A | 383 | 11.68823 | 1663 | 50.75073 | N/A | N/A |
| | Sinc5 | Sinc5 | 64 | N/A | 639 | 19.50073 | 3199 | 97.62573 | N/A | N/A |
| | Sinc5 | Sinc5 | 128 | N/A | 1151 | 35.12573 | 6271 | 191.37573 | N/A | N/A |
| | Sinc5 | Sinc5 | 256 | N/A | 2175 | 66.37573 | 12,415 | 378.87573 | N/A | N/A |
| | Sinc5 | Sinc5 | 512 | N/A | 4223 | 128.87573 | 24,703 | 753.87573 | N/A | N/A |
| | Sinc5 | Sinc5 | 1024 | N/A | 8319 | 253.87573 | 49,279 | 1503.87573 | N/A | N/A |
| | Sinc5 | Sinc5 | 32 | 32 | 383 | 11.68823 | 1663 | 50.75073 | 1663 | 50.75073 |
| | Sinc5 | Sinc5 | 32 | 64 | 383 | 11.68823 | 1663 | 50.75073 | 3199 | 97.62573 |
| | Sinc5 | Sinc5 | 32 | 128 | 383 | 11.68823 | 1663 | 50.75073 | 6271 | 191.37573 |
| | Sinc5 | Sinc5 | 32 | 256 | 398 | 11.68823 | 1663 | 50.75073 | 12,415 | 378.87573 |
| | Sinc5 | Sinc5 | 32 | 512 | 398 | 11.68823 | 1663 | 50.75073 | 24,703 | 753.87573 |
| | Sinc5 | Sinc5 | 32 | 1024 | 398 | 11.68823 | 1663 | 50.75073 | 49,279 | 1503.87573 |
| | Sinc5 | Sinc5 | 64 | 32 | 383 | 11.68823 | 3199 | 97.62573 | 1663 | 50.75073 |
| | Sinc5 | Sinc5 | 1024 | 32 | 398 | 11.68823 | 49,279 | 1503.87573 | 1663 | 50.75073 |
| Eco | Sinc5 | Sinc5 | 32 | N/A | 1487 | 45.37964 | 6607 | 201.62964 | N/A | N/A |
| | Sinc5 | Sinc5 | 64 | N/A | 2511 | 76.62964 | 12,751 | 389.12964 | N/A | N/A |
| | Sinc5 | Sinc5 | 128 | N/A | 4559 | 139.12964 | 25,039 | 764.12964 | N/A | N/A |
| | Sinc5 | Sinc5 | 256 | N/A | 8655 | 264.12964 | 49,615 | 1514.12964 | N/A | N/A |
| | Sinc5 | Sinc5 | 512 | N/A | 16,847 | 514.12964 | 98,767 | 3014.12964 | N/A | N/A |
| | Sinc5 | Sinc5 | 1024 | N/A | 33,231 | 1014.12964 | 197,071 | 6014.12964 | N/A | N/A |
| | Sinc5 | Sinc5 | 32 | 32 | 1487 | 45.37964 | 6607 | 201.62964 | 6607 | 201.62964 |
| | Sinc5 | Sinc5 | 32 | 64 | 1487 | 45.37964 | 6607 | 201.62964 | 12,751 | 389.12964 |
| | Sinc5 | Sinc5 | 32 | 128 | 1487 | 45.37964 | 6607 | 201.62964 | 25,039 | 764.12964 |
| | Sinc5 | Sinc5 | 32 | 256 | 1487 | 45.37964 | 6607 | 201.62964 | 49,615 | 1514.12964 |
| | Sinc5 | Sinc5 | 32 | 512 | 1487 | 45.37964 | 6607 | 201.62964 | 98,767 | 3014.12964 |
| | Sinc5 | Sinc5 | 32 | 1024 | 1487 | 45.37964 | 6607 | 201.62964 | 197,071 | 6014.12964 |
| | Sinc5 | Sinc5 | 64 | 32 | 1487 | 45.37964 | 12,751 | 389.12964 | 6607 | 201.62964 |
| | Sinc5 | Sinc5 | 1024 | 32 | 1487 | 45.37964 | 197,071 | 6014.12964 | 6607 | 201.62964 |

[1] This table is based on default internal clock divide settings of MCLK/4 in fast mode, MCLK/8 in median mode, and MCLK/32 in eco mode.
[2] N/A means not applicable.

# FUNCTIONALITY

## GPIO FUNCTIONALITY

The AD7768 has additional GPIO functionality when operated in SPI mode. This fully configurable mode allows the device to operate five GPIOs. These pins can be configured as read or write in any order.

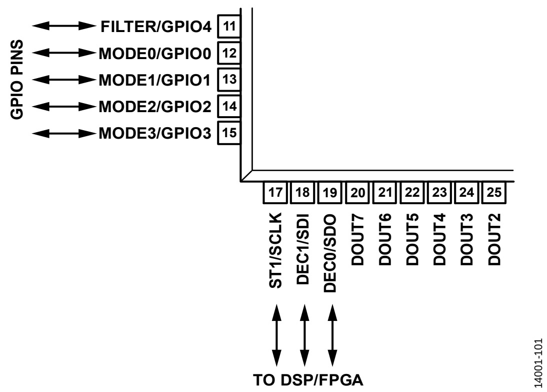



*Figure 104. GPIO Functionality*

The details for configuration control and read back of the GPIOx pins are dealt with by Register 0x0E, Register 0x0F, and Register 0x10 and documented in Table 45, Table 46, and Table 47.

GPIO read is a useful feature, because it allows a peripheral device to send information to the input GPIO and then this information can be read from the SPI interface of the AD7768.

The GPIOx pins can be set as inputs or outputs on a per pin basis.

## 1.8 V IOVDD OPERATION

The AD7768 contains an internal 1.8 V LDO on the IOVDD supply to regulate the IOVDD down to the operating voltage of the digital core. This allows the internal logic to operate efficiently at 1.8 V and the input/output logic to operate at the level set by IOVDD. The IOVDD supply is rated from 2.25 V to 3.6 V for normal operation, and 1.8 V for LDO bypass setup.

Users can bypass the LDO by shorting the DREGCAP pin to IOVDD, which pulls the internal LDO out of regulation and sets the internal core voltage and input/output logic levels to the IOVDD level. When bypassing the internal LDO, the maximum operating voltage of the IOVDD supply is equal to the maximum operating voltage of the internal digital core, which is 1.72 V to 1.88 V.

There are a number of performance differences to consider when operating at 1.8 V IOVDD. See the 1.8 V IOVDD Specifications section for detailed specifications while operating at 1.8 V IOVDD.

## ANALOG SUPPLY INTERNAL CONNECTIVITY

The AD7768 has two analog supply rails, AVDD1 and AVDD2, which are both referred to AVSS. These supplies are completely separate from the digital pins IOVDD, DREGCAP, and DGND. To achieve optimal performance and isolation of the ADCs, more than one device pin supplies these analog rails to the internal ADCs.

- AVSS1A (Pin 3) and AVSS2A (Pin 62) are internally connected.
- AVSS (Pin 54) is connected to the substrate, and is connected internally to AVSS1B (Pin 46) and AVSS2B (Pin 51).
- The following supply and reference input pins are separate on chip: AVDD1A, AVDD1B, AVDD2A, AVDD2B, REF1+, REF1−, REF2+, and REF2−.

The details of which individual supplies are shorted internally are given in this section for information purposes. In general, connect the supplies as described in the Power Supplies section.

# REGISTER MAP DETAILS (SPI CONTROL)

## REGISTER MAP

**Table 33. Detailed Register Map**

| Reg. | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | Channel Standby | CH_7 | CH_6 | CH_5 | CH_4 | CH_3 | CH_2 | CH_1 | CH_0 | 0x00 | RW |
| 0x01 | Channel Mode A | Unused | | | | FILTER_TYPE_A | DEC_RATE_A | | | 0x0D | RW |
| 0x02 | Channel Mode B | Unused | | | | FILTER_TYPE_B | DEC_RATE_B | | | 0x0D | RW |
| 0x03 | Channel Mode Select | CH_7_MODE | CH_6_MODE | CH_5_MODE | CH_4_MODE | CH_3_MODE | CH_2_MODE | CH_1_MODE | CH_0_MODE | 0x00 | RW |
| 0x04 | POWER_MODE | SLEEP_MODE | Unused | POWER_MODE | | LVDS_ENABLE | Unused | MCLK_DIV | | 0x00 | RW |
| 0x05 | General Configuration | Unused | CLK_QUAL_DIS | Reserved | VCM_PD | Reserved | Unused | VCM_VSEL | | 0x08 | RW |
| 0x06 | Data Control | SPI_SYNC | Unused | | SINGLE_SHOT_EN | Unused | | SPI_RESET | | 0x80 | RW |
| 0x07 | Interface Configuration | Unused | | | | CRC_SELECT | | DCLK_DIV | | 0x0 | RW |
| 0x08 | BIST Control | Unused | | | | | | | RAM_BIST_START | 0x0 | RW |
| 0x09 | Device Status | Unused | | | | CHIP_ERROR | NO_CLOCK_ERROR | RAM_BIST_PASS | RAM_BIST_RUNNING | 0x0 | R |
| 0x0A | Revision ID | REVISION_ID | | | | | | | | 0x06 | R |
| 0x0B | Reserved | Reserved | | | | | | | | 0x00 | R |
| 0x0C | Reserved | Reserved | | | | | | | | 0x00 | R |
| 0x0D | Reserved | Reserved | | | | | | | | 0x00 | R |
| 0x0E | GPIO Control | UGPIO_ENABLE | Unused | | GPIOE4_FILTER | GPIOE3_MODE3 | GPIOE2_MODE2 | GPIOE1_MODE1 | GPIO0_MODE0 | 0x00 | RW |
| 0x0F | GPIO Write Data | Unused | | | GPIO4_WRITE | GPIO3_WRITE | GPIO2_WRITE | GPIO1_WRITE | GPIO0_WRITE | 0x00 | RW |
| 0x10 | GPIO Read Data | Unused | | | GPIO4_READ | GPIO3_READ | GPIO2_READ | GPIO1_READ | GPIO0_READ | 0x00 | R |
| 0x11 | Precharge Buffer 1 | CH3_PREBUF_NEG_EN | CH3_PREBUF_POS_EN | CH2_PREBUF_NEG_EN | CH2_PREBUF_POS_EN | CH1_PREBUF_NEG_EN | CH1_PREBUF_POS_EN | CH0_PREBUF_NEG_EN | CH0_PREBUF_POS_EN | 0xFF | RW |
| 0x12 | Precharge Buffer 2 | CH7_PREBUF_NEG_EN | CH7_PREBUF_POS_EN | CH6_PREBUF_NEG_EN | CH6_PREBUF_POS_EN | CH5_PREBUF_NEG_EN | CH5_PREBUF_POS_EN | CH4_PREBUF_NEG_EN | CH4_PREBUF_POS_EN | 0xFF | RW |
| 0x13 | Positive Precharge Reference Buffer | CH7_REFP_BUF | CH6_REFP_BUF | CH5_REFP_BUF | CH4_REFP_BUF | CH3_REFP_BUF | CH2_REFP_BUF | CH1_REFP_BUF | CH0_REFP_BUF | 0x00 | RW |
| 0x14 | Negative Precharge Reference Buffer | CH7_REFN_BUF | CH6_REFN_BUF | CH5_REFN_BUF | CH4_REFN_BUF | CH3_REFN_BUF | CH3_REFN_BUF | CH1_REFN_BUF | CH0_REFN_BUF | 0x00 | RW |
| 0x1E | Channel 0 Offset | CH0_OFFSET_MSB | | | | | | | | 0x00 | RW |
| 0x1F | | CH0_OFFSET_MID | | | | | | | | | |
| 0x20 | | CH0_OFFSET_LSB | | | | | | | | | |
| 0x21 | Channel 1 Offset | CH1_OFFSET_MSB | | | | | | | | 0x00 | RW |
| 0x22 | | CH1_OFFSET_MID | | | | | | | | | |
| 0x23 | | CH1_OFFSET_LSB | | | | | | | | | |
| 0x24 | Channel 2 Offset | CH2_OFFSET_MSB | | | | | | | | 0x00 | RW |
| 0x25 | | CH2_OFFSET_MID | | | | | | | | | |
| 0x26 | | CH2_OFFSET_LSB | | | | | | | | | |
| 0x27 | Channel 3 Offset | CH3_OFFSET_MSB | | | | | | | | 0x00 | RW |
| 0x28 | | CH3_OFFSET_MID | | | | | | | | | |
| 0x29 | | CH3_OFFSET_LSB | | | | | | | | | |
| 0x2A | Channel 4 Offset | CH4_OFFSET_MSB | | | | | | | | 0x00 | RW |
| 0x2B | | CH4_OFFSET_MID | | | | | | | | | |
| 0x2C | | CH4_OFFSET_LSB | | | | | | | | | |
| 0x2D | Channel 5 Offset | CH5_OFFSET_MSB | | | | | | | | 0x00 | RW |
| 0x2E | | CH5_OFFSET_MID | | | | | | | | | |
| 0x2F | | CH5_OFFSET_LSB | | | | | | | | | |
| 0x30 | Channel 6 Offset | CH6_OFFSET_MSB | | | | | | | | 0x00 | RW |
| 0x31 | | CH6_OFFSET_MID | | | | | | | | | |
| 0x32 | | CH6_OFFSET_LSB | | | | | | | | | |
| 0x33 | Channel 7 Offset | CH7_OFFSET_MSB | | | | | | | | 0x00 | RW |
| 0x34 | | CH7_OFFSET_MID | | | | | | | | | |
| 0x35 | | CH7_OFFSET_LSB | | | | | | | | | |
| 0x36 | Channel 0 Gain | CH0_GAIN_MSB | | | | | | | | 0xXX | RW |
| 0x37 | | CH0_GAIN_MID | | | | | | | | | |
| 0x38 | | CH0_GAIN_LSB | | | | | | | | | |

| Reg. | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x39 | Channel 1 Gain | CH1_GAIN_MSB | | | | | | | | 0xXX | RW |
| 0x3A | | CH1_GAIN_MID | | | | | | | | | |
| 0x3B | | CH1_GAIN_LSB | | | | | | | | | |
| 0x3C | Channel 2 Gain | CH2_GAIN_MSB | | | | | | | | 0xXX | RW |
| 0x3D | | CH2_GAIN_MID | | | | | | | | | |
| 0x3E | | CH2_GAIN_LSB | | | | | | | | | |
| 0x3F | Channel 3 Gain | CH3_GAIN_MSB | | | | | | | | 0xXX | RW |
| 0x40 | | CH3_GAIN_MID | | | | | | | | | |
| 0x41 | | CH3_GAIN_LSB | | | | | | | | | |
| 0x42 | Channel 4 Gain | CH4_GAIN_MSB | | | | | | | | 0xXX | RW |
| 0x43 | | CH4_GAIN_MID | | | | | | | | | |
| 0x44 | | CH4_GAIN_LSB | | | | | | | | | |
| 0x45 | Channel 5 Gain | CH5_GAIN_MSB | | | | | | | | 0xXX | RW |
| 0x46 | | CH5_GAIN_MID | | | | | | | | | |
| 0x47 | | CH5_GAIN_LSB | | | | | | | | | |
| 0x48 | Channel 6 Gain | CH6_GAIN_MSB | | | | | | | | 0xXX | RW |
| 0x49 | | CH6_GAIN_MID | | | | | | | | | |
| 0x4A | | CH6_GAIN_LSB | | | | | | | | | |
| 0x4B | Channel 7 Gain | CH7_GAIN_MSB | | | | | | | | 0xXX | RW |
| 0x4C | | CH7_GAIN_MID | | | | | | | | | |
| 0x4D | | CH7_GAIN_LSB | | | | | | | | | |
| 0x4E | Channel 0 Sync Offset | CH0_SYNC_OFFSET | | | | | | | | 0x00 | RW |
| 0x4F | Channel 1 Sync Offset | CH1_SYNC_OFFSET | | | | | | | | 0x00 | RW |
| 0x50 | Channel 2 Sync Offset | CH2_SYNC_OFFSET | | | | | | | | 0x00 | RW |
| 0x51 | Channel 3 Sync Offset | CH3_SYNC_OFFSET | | | | | | | | 0x00 | RW |
| 0x52 | Channel 4 Sync Offset | CH4_SYNC_OFFSET | | | | | | | | 0x00 | RW |
| 0x53 | Channel 5 Sync Offset | CH5_SYNC_OFFSET | | | | | | | | 0x00 | RW |
| 0x54 | Channel 6 Sync Offset | CH6_SYNC_OFFSET | | | | | | | | 0x00 | RW |
| 0x55 | Channel 7 Sync Offset | CH7_SYNC_OFFSET | | | | | | | | 0x00 | RW |
| 0x56 | Diagnostic Rx | CH7_RX | CH6_RX | CH5_RX | CH4_RX | CH3_RX | CH2_RX | CH1_RX | CH0_RX | 0x00 | RW |
| 0x57 | Diagnostic Mux Control | Unused | GRPB_SEL | | | Unused | GRPA_SEL | | | 0x00 | RW |
| 0x58 | Modulator Delay Control | Unused | | | | CLK_MOD_DEL_EN | | Reserved | Reserved | 0x02 | RW |
| 0x59 | Chop Control | Unused | | | | GRPA_CHOP | | GRPB_CHOP | | 0x0A | RW |

## CHANNEL STANDBY REGISTER

**Address: 0x00, Reset: 0x00, Name: Channel Standby**

Each of the ADC channels can be put into standby mode independently by setting the appropriate bit in the channel standby register. When a channel is in standby mode, its position in the data output stream is held. The 8-bit header is all zeros, as is the conversion result output of 24 zeros.

**Table 34. Bit Descriptions for Channel Standby**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | CH_7 | | Channel 7 | 0x0 | RW |
| | | 0 | Enabled | | |
| | | 1 | Standby | | |
| 6 | CH_6 | | Channel 6 | 0x0 | RW |
| | | 0 | Enabled | | |
| | | 1 | Standby | | |
| 5 | CH_5 | | Channel 5 | 0x0 | RW |
| | | 0 | Enabled | | |
| | | 1 | Standby | | |
| 4 | CH_4 | | Channel 4 | 0x0 | RW |
| | | 0 | Enabled | | |
| | | 1 | Standby | | |
| 3 | CH_3 | | Channel 3 | 0x0 | RW |
| | | 0 | Enabled | | |
| | | 1 | Standby | | |
| 2 | CH_2 | | Channel 2 | 0x0 | RW |
| | | 0 | Enabled | | |
| | | 1 | Standby | | |
| 1 | CH_1 | | Channel 1 | 0x0 | RW |
| | | 0 | Enabled | | |
| | | 1 | Standby | | |
| 0 | CH_0 | | Channel 0 | 0x0 | RW |
| | | 0 | Enabled | | |
| | | 1 | Standby | | |

## CHANNEL MODE A REGISTER

**Address: 0x01, Reset: 0x0D, Name: Channel Mode A**

Two mode options are available on the AD7768 ADCs. The channel modes are defined by the contents of the Channel Mode A and Channel Mode B registers. Each mode is then mapped as desired to the required ADC channel. Mode A and Mode B allow different filter types and decimation rates to be selected and mapped to any of the ADC channels.

When different decimation rates are selected, the AD7768 outputs a data ready signal at the fastest selected decimation rate. Any channel that runs at a lower output data rate is updated only at that slower rate. In between valid result data, the data for that channel is set to zero and the repeated data bit is set in the header status bits to distinguish it from a real conversion result (see the ADC Conversion Output: Header and Data section).

**Table 35. Bit Descriptions for Channel Mode A**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 3 | FILTER_TYPE_A | | Filter selection | 0x1 | RW |
| | | 0 | Wideband filter | | |
| | | 1 | Sinc5 filter | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [2:0] | DEC_RATE_A | | Decimation rate selection | 0x5 | RW |
| | | 000 | ×32 | | |
| | | 001 | ×64 | | |
| | | 010 | ×128 | | |
| | | 011 | ×256 | | |
| | | 100 | ×512 | | |
| | | 101 | ×1024 | | |
| | | 110 | ×1024 | | |
| | | 111 | ×1024 | | |

## CHANNEL MODE B REGISTER

**Address: 0x02, Reset: 0x0D, Name: Channel Mode B**

**Table 36. Bit Descriptions for Channel Mode B**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 3 | FILTER_TYPE_B | | Filter selection | 0x1 | RW |
| | | 0 | Wideband filter | | |
| | | 1 | Sinc5 filter | | |
| [2:0] | DEC_RATE_B | | Decimation rate selection | 0x5 | RW |
| | | 000 | ×32 | | |
| | | 001 | ×64 | | |
| | | 010 | ×128 | | |
| | | 011 | ×256 | | |
| | | 100 | ×512 | | |
| | | 101 | ×1024 | | |
| | | 110 | ×1024 | | |
| | | 111 | ×1024 | | |

## CHANNEL MODE SELECT REGISTER

**Address: 0x03, Reset: 0x00, Name: Channel Mode Select**

This register selects the mapping of each ADC channel to either Mode A or Mode B.

**Table 37. Bit Descriptions for Channel Mode Select**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | CH_7_MODE | | Channel 7 | 0x0 | RW |
| | | 0 | Mode A | | |
| | | 1 | Mode B | | |
| 6 | CH_6_MODE | | Channel 6 | 0x0 | RW |
| | | 0 | Mode A | | |
| | | 1 | Mode B | | |
| 5 | CH_5_MODE | | Channel 5 | 0x0 | RW |
| | | 0 | Mode A | | |
| | | 1 | Mode B | | |
| 4 | CH_4_MODE | | Channel 4 | 0x0 | RW |
| | | 0 | Mode A | | |
| | | 1 | Mode B | | |
| 3 | CH_3_MODE | | Channel 3 | 0x0 | RW |
| | | 0 | Mode A | | |
| | | 1 | Mode B | | |
| 2 | CH_2_MODE | | Channel 2 | 0x0 | RW |
| | | 0 | Mode A | | |
| | | 1 | Mode B | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 1 | CH_1_MODE | | Channel 1 | 0x0 | RW |
| | | 0 | Mode A | | |
| | | 1 | Mode B | | |
| 0 | CH_0_MODE | | Channel 0 | 0x0 | RW |
| | | 0 | Mode A | | |
| | | 1 | Mode B | | |

## POWER MODE SELECT REGISTER

**Address: 0x04, Reset: 0x00, Name: POWER_MODE**

**Table 38. Bit Descriptions for POWER_MODE**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | SLEEP_MODE | | In sleep mode, all clocks are internally gated and all of the ADCs are disabled. The analog LDOs are not disabled.<br>The AD7768 SPI is live and is available to the user. Writing to this bit brings the AD7768 out of sleep mode again. Any decoupling capacitors on the DREGCAP pin must recharge after exiting sleep mode. | 0x0 | RW |
| | | 0 | Normal operation. | | |
| | | 1 | Sleep mode. | | |
| [5:4] | POWER_MODE | | Power mode. The power mode bits control the power mode setting for the bias currents used on all ADCs on the AD7768. The user can select the current consumption target to meet the application. The power modes of fast, median, and eco give optimum performance when mapped to the correct MCLK division setting. These power mode bits do not control the MCLK division of the ADCs. See the MCLK_DIV bits for control of the division of the MCLK input. | 0x0 | RW |
| | | 00 | Eco. | | |
| | | 10 | Median. | | |
| | | 11 | Fast. | | |
| 3 | LVDS_ENABLE | | LVDS clock. | 0x0 | RW |
| | | 0 | LVDS input clock disabled. | | |
| | | 1 | LVDS input clock enabled. | | |
| [1:0] | MCLK_DIV | | MCLK division. The MCLK division bits control the divided ratio between the MCLK applied at the input to the AD7768 and the clock used by each of the ADC modulators. The appropriate division ratio depends on the following factors: power mode, decimation rate, and the base MCLK available in the system. See the Clocking and Sampling Tree section for more information on setting MCLK_DIV correctly. | 0x0 | RW |
| | | 00 | MCLK/32: with a base MCLK of 32.768 MHz, set to MCLK/32 for eco mode. | | |
| | | 10 | MCLK/8: with a base MCLK of 32.768 MHz, set to MCLK/8 for median mode. | | |
| | | 11 | MCLK/4: with a base MCLK of 32.768 MHz, set to MCLK/4 for fast mode. | | |

## GENERAL DEVICE CONFIGURATION REGISTER

**Address: 0x05, Reset: 0x08, Name: General Configuration**

**Table 39. Bit Descriptions for General Configuration**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 6 | CLK_QUAL_DIS | | Clock check. This bit enables or disables the clock qualification check when switching from the internal clock to the external clock at start up. When enabled, the external MCLK frequency is checked to be at least approximately 1.15 MHz before being accepted as valid. If the qualification check fails, the NO_CLOCK_ERROR bit is set. Users can disable this qualification check to allow lower MCLK frequencies to be used without causing an error. | 0x0 | RW |
| | | 0 | Enabled. Clock qualification check is performed. | | |
| | | 1 | Disabled. Clock qualification check is not performed. | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 4 | VCM_PD | | VCM buffer power-down. | 0x0 | RW |
| | | 0 | Enabled: VCM buffer normal mode. | | |
| | | 1 | Powered down: VCM buffer powered down. | | |
| 3 | Reserved | 1 | Not a user option. This bit must be set to 1. | 0x1 | RW |
| [1:0] | VCM_VSEL | | VCM voltage. These bits select the output voltage of the VCM pin. This voltage is derived from the AVDD1 supply and can be output as half of that AVDD1 voltage, or other fixed voltages, with respect to AVSS. | 0x0 | RW |
| | | 00 | (AVDD1 − AVSS)/2. | | |
| | | 01 | 1.65 V. | | |
| | | 10 | 2.5 V. | | |
| | | 11 | 2.14 V. | | |

## DATA CONTROL: SOFT RESET, SYNC, AND SINGLE-SHOT CONTROL REGISTER

**Address: 0x06, Reset: 0x80, Name: Data Control**

**Table 40. Bit Descriptions for Data Control**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | SPI_SYNC | | Software synchronization of the AD7768. This command has the same effect as sending a signal pulse to the START pin. To operate the SPI_SYNC, the user must write to this bit on two separate times. First, write a zero, putting SPI_SYNC low, and then write a 1 to set SPI_SYNC logic high again. The SPI_SYNC command is recognized after the last rising edge of SCLK in the SPI instruction where the SPI_SYNC bit is changed from low to high. The SPI_SYNC command is then output synchronous to the AD7768 MCLK on the SYNC_OUT pin. The user must connect the SYNC_OUT signal to the SYNC_IN pin on the PCB. The SYNC_OUT pin may also be routed to the SYNC_IN pins of other AD7768 devices, allowing larger channel count simultaneous sampling systems. Any daisy-chained system of AD7768 devices requires that all ADCs be synchronized. As per any synchronization pulse seen by the SYNC_IN pin, the digital filters of the AD7768 are reset. The fully settling time of the filters must elapse before data is output on the data interface. | 0x1 | RW |
| | | 0 | Change to SPI_SYNC low. | | |
| | | 1 | Change to SPI_SYNC high. | | |
| 4 | SINGLE_SHOT_EN | | One-shot mode. Enables one-shot mode. In one-shot mode, the AD7768 outputs a conversion result in response to a SYNC_IN rising edge. | 0x0 | RW |
| | | 0 | Disabled. | | |
| | | 1 | Enabled. | | |
| [1:0] | SPI_RESET | | Soft reset. These bits allow\ a full device reset over the SPI port. Two successive commands must be received in the correct order to generate a reset: first, write 0x03 to the soft reset register, and then write 0x02 to the soft reset register. This causes the digital core to reset and all registers return to their default values. Following a soft reset, if the SPI master sends a command to the AD7768, it responds on the next frame to that command with an output of 0x0E00. | 0x0 | RW |
| | | 00 | No effect. | | |
| | | 01 | No effect. | | |
| | | 10 | Second reset command. | | |
| | | 11 | First reset command. | | |

## INTERFACE CONFIGURATION REGISTER

**Address: 0x07, Reset: 0x0, Name: Interface Configuration**

**Table 41. Bit Descriptions for Interface Configuration**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [3:2] | CRC_SELECT | | CRC select. These bits allow the user to implement a CRC on the data interface. When selected, the CRC replaces the header every fourth or 16th output sample depending on the CRC option chosen. There are two options for the CRC; both use the same polynomial: $x^8 + x^2 + x + 1$. The options offer the user the ability to reduce the duty cycle of the CRC calculation by performing it less often: in the case of having it every 16th sample or more often in the case of every fourth conversion. The CRC is calculated on a per channel basis and it includes conversion data only. | 0x0 | RW |
| | | 00 | No CRC. Status bits with every conversion. | | |
| | | 01 | Replace the header with CRC message every 4 samples. | | |
| | | 10 | Replace the header with CRC message every 16 samples. | | |
| | | 11 | Replace the header with CRC message every 16 samples. | | |
| [1:0] | DCLK_DIV | | DCLK divider. These bits control division of the DCLK clock used to clock out conversion data on DOUT0 to DOUT7. The DCLK signal is derived from the MCLK applied to the AD7768. The DCLK divide mode allows the user to optimize the DCLK output to fit the application. Optimizing the DCLK per application depends on the requirements of the user. When the AD7768 is using the highest capacity output on the fewest DOUTx pins, for example, running in decimate by 32 using the DOUT0 and DOUT1 pins, the DCLK must equal the MCLK; thus, in this case, choosing the no division setting is the only way the user can output all the data within the conversion period.<br>There are other cases, however, when the ADC may be running in fast mode with high decimation rates, or in median or eco mode where the DCLK does not need to run at the same speed as MCLK. In these cases, the DCLK divide allows the user to reduce the clock speed and makes routing and isolating such signals easier. | 0x0 | RW |
| | | 00 | Divide by 8. | | |
| | | 01 | Divide by 4. | | |
| | | 10 | Divide by 2. | | |
| | | 11 | No division. | | |

## DIGITAL FILTER RAM BUILT IN SELF TEST (BIST) REGISTER

**Address: 0x08, Reset: 0x0, Name: BIST Control**

**Table 42. Bit Descriptions for BIST Control**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 0 | RAM_BIST_START | | RAM BIST. Filter RAM BIST is a built in self test of the RAM storage of the coefficients used by the digital filter.<br>This test cannot be run concurrent with ADC sampling. The test may be run at intervals depending on user preference. The status and result of the RAM BIST is available in the device status register; see the RAM_BIST_PASS and RAM_BIST_RUNNING bits in Table 43. | 0x0 | RW |
| | | 0 | Off. | | |
| | | 1 | Begin RAM BIST. | | |

## STATUS REGISTER

**Address: 0x09, Reset: 0x0, Name: Device Status**

**Table 43. Bit Descriptions for Device Status**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 3 | CHIP_ERROR | | Chip error. Chip error is a global error flag that is output within the status byte of each ADC conversion output. The following bits lead to the chip error bit being set to logic high: CRC check on internally hard coded settings after power-up does not pass; XOR check on the memory map does not pass (this check runs continuously in the background); and clock error is detected on power-up. | 0x0 | R |
| | | 0 | No error present. | | |
| | | 1 | Error has occurred. | | |
| 2 | NO_CLOCK_ERROR | | External CLK check. This bit indicates if the externally applied MCLK is detected correctly. If the MCLK is not applied correctly, to the ADC at power up this bit is set and the DCLK frequency is approximately 16 MHz. If this bit is set, the chip error bit is set to logic high in the status bits of the data output headers. | 0x0 | R |
| | | 0 | MCLK detected. | | |
| | | 1 | No MCLK detected. | | |
| 1 | RAM_BIST_PASS | | BIST pass/fail. RAM BIST result status. This bit indicates the result of the most recent RAM BIST. The result is latched to this register and is only cleared by a device reset. | 0x0 | R |
| | | 0 | BIST failed or not run. | | |
| | | 1 | BIST passed. | | |
| 0 | RAM_BIST_RUNNING | | BIST Status. Reading back the value of this bit allows the user to poll when the BIST test has finished. | 0x0 | R |
| | | 0 | BIST not running. | | |
| | | 1 | BIST running. | | |

## REVISION IDENTIFICATION REGISTER

**Address: 0x0A, Reset: 0x06, Name: Revision ID**

**Table 44. Bit Descriptions for Revision ID**

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [7:0] | REVISION_ID | ASIC revision. 8-bit ID for revision details. | 0x06 | R |

## GPIO CONTROL REGISTER

**Address: 0x0E, Reset: 0x00, Name: GPIO Control**

**Table 45. Bit Descriptions for GPIO Control**

| Bits | Bit Name | Setting | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | UGPIO_ENABLE | | User GPIO enable. The GPIOx pins are dual-purpose and can be operated only when the device is in SPI control mode. By default, when the AD7768 is powered up in SPI control mode, the GPIOx pins are disabled. This bit is a universal enable/disable for all GPIOx input/outputs. The direction of each general-purpose pin is determined by Bits[4:0] of this register. | 0x0 | RW |
| | | 0 | GPIO Disabled. | | |
| | | 1 | GPIO Enabled. | | |
| 4 | GPIOE4_FILTER | | GPIO4 Direction. This bit assigns the direction of GPIO4 as either an input or an output. For SPI control, GPIO4 maps to Pin 11, which is the GPIO4/FILTER pin. | 0x0 | RW |
| | | 0 | Input. | | |
| | | 1 | Output. | | |
| 3 | GPIOE3_MODE3 | | GPIO3 Direction. This bit assigns the direction of GPIO3 as either an input or an output. For SPI control, GPIO3 maps to Pin 15, which is the GPIO3/MODE3 pin. | 0x0 | RW |
| | | 0 | Input. | | |
| | | 1 | Output. | | |

| Bits | Bit Name | Setting | Description | Reset | Access |
|---|---|---|---|---|---|
| 2 | GPIOE2_MODE2 | | GPIO2 Direction. This bit assigns the direction of GPIO2 as either an input or an output. For SPI control, GPIO2 maps to Pin 14, which is the GPIO2/MODE2 pin. | 0x0 | RW |
| | | 0 | Input. | | |
| | | 1 | Output. | | |
| 1 | GPIOE1_MODE1 | | GPIO1 Direction. This bit assigns the direction of GPIO1 as either an input or an output. For SPI control, GPIO1 maps to Pin 13, which is the GPIO1/MODE1 pin. | 0x0 | RW |
| | | 0 | Input. | | |
| | | 1 | Output. | | |
| 0 | GPIO0_MODE0 | | GPIO0 Direction. This bit assigns the direction of GPIO0 as either an input or an output. For SPI control, GPIO0 maps to Pin 12, which is the GPIO0/MODE0 pin. | 0x0 | RW |
| | | 0 | Input. | | |
| | | 1 | Output. | | |

## GPIO WRITE DATA REGISTER

**Address: 0x0F, Reset: 0x00, Name: GPIO Write Data**

This register writes the values to be set on each of the general-purpose pins when selected as general-purpose outputs. Each bit, from Bits[4:0], maps directly to the GPIOx pins.

**Table 46. Bit Descriptions for GPIO Write Data**

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| 4 | GPIO4_WRITE | GPIO4/FILTER | 0x0 | RW |
| 3 | GPIO3_WRITE | GPIO3/MODE3 | 0x0 | RW |
| 2 | GPIO2_WRITE | GPIO2/MODE2 | 0x0 | RW |
| 1 | GPIO1_WRITE | GPIO1/MODE1 | 0x0 | RW |
| 0 | GPIO0_WRITE | GPIO0/MODE0 | 0x0 | RW |

## GPIO READ DATA REGISTER

**Address: 0x10, Reset: 0x00, Name: GPIO Read Data**

This register reads back the value of the logic input level at the general-purpose pins when selected to operate as general-purpose inputs. Each bit, from Bits[4:0], maps directly to the GPIO0 to GPIO4 pins.

**Table 47. Bit Descriptions for GPIO Read Data**

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| 4 | GPIO4_READ | GPIO4/FILTER | 0x0 | R |
| 3 | GPIO3_READ | GPIO3/MODE3 | 0x0 | R |
| 2 | GPIO2_READ | GPIO2/MODE2 | 0x0 | R |
| 1 | GPIO1_READ | GPIO1/MODE1 | 0x0 | R |
| 0 | GPIO0_READ | GPIO0/MODE0 | 0x00 | R |

## PRECHARGE ANALOG INPUT BUFFER ENABLE REGISTER CHANNEL 0 TO CHANNEL 3

**Address: 0x11, Reset: 0xFF, Name: Precharge Buffer 1**

This register turns on or off the precharge buffers on the analog inputs. When writing to these registers, the user must write the inverse of the required bit settings. For example, to clear Bit 7 of this register, the user must write 0x01 to the register. This clears Bit 7 and sets all other bits. If the user reads the register again after writing 0x01, the data read is 0xFE, as required.

**Table 48. Bit Descriptions for Precharge Buffer 1**

| Bits | Bit Name | Settings | Description | Reset |
|---|---|---|---|---|
| 7 | CH3_PREBUF_NEG_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 6 | CH3_PREBUF_POS_EN | 0 | Off | 0x1 |
| | | 1 | On | |

| Bits | Bit Name | Settings | Description | Reset |
|---|---|---|---|---|
| 5 | CH2_PREBUF_NEG_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 4 | CH2_PREBUF_POS_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 3 | CH1_PREBUF_NEG_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 2 | CH1_PREBUF_POS_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 1 | CH0_PREBUF_NEG_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 0 | CH0_PREBUF_POS_EN | 0 | Off | 0x1 |
| | | 1 | On | |

## PRECHARGE ANALOG INPUT BUFFER ENABLE REGISTER CHANNEL 4 TO CHANNEL 7

**Address: 0x12, Reset: 0xFF, Name: Precharge Buffer 2**

This register turns on or off the precharge buffers on the analog inputs. When writing to these registers, the user must write the inverse of the required bit settings. For example, to clear Bit 7 of this register, the user must write 0x01 to the register. This clears Bit 7 and sets all other bits. If the user reads the register again after writing 0x01, the data read is 0xFE, as required.

**Table 49. Bit Descriptions for Precharge Buffer 2**

| Bits | Bit Name | Settings | Description | Reset |
|---|---|---|---|---|
| 7 | CH7_PREBUF_NEG_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 6 | CH7_PREBUF_POS_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 5 | CH6_PREBUF_NEG_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 4 | CH6_PREBUF_POS_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 3 | CH5_PREBUF_NEG_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 2 | CH5_PREBUF_POS_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 1 | CH4_PREBUF_NEG_EN | 0 | Off | 0x1 |
| | | 1 | On | |
| 0 | CH4_PREBUF_POS_EN | 0 | Off | 0x1 |
| | | 1 | On | |

## POSITIVE PRECHARGE REFERENCE BUFFER ENABLE REGISTER

**Address: 0x13, Reset: 0x00, Name: Positive Precharge Reference Buffer**

This register turns on or off the precharge buffers on the reference positive input to each of the ADCs from Channel 0 to Channel 7.

**Table 50. Bit Descriptions for Positive Precharge Reference Buffer**

| Bits | Bit Name | Settings | Description | Reset |
|---|---|---|---|---|
| 7 | CH7_REFP_BUF | 0 | Off | 0x0 |
| | | 1 | On | |
| 6 | CH6_REFP_BUF | 0 | Off | 0x0 |
| | | 1 | On | |
| 5 | CH5_REFP_BUF | 0 | Off | 0x0 |
| | | 1 | On | |
| 4 | CH4_REFP_BUF | 0 | Off | 0x0 |
| | | 1 | On | |

| Bits | Bit Name | Settings | Description | Reset |
|---|---|---|---|---|
| 3 | CH3_REFP_BUF | 0<br>1 | Off<br>On | 0x0 |
| 2 | CH2_REFP_BUF | 0<br>1 | Off<br>On | 0x0 |
| 1 | CH1_REFP_BUF | 0<br>1 | Off<br>On | 0x0 |
| 0 | CH0_REFP_BUF | 0<br>1 | Off<br>On | 0x0 |

## NEGATIVE PRECHARGE REFERENCE BUFFER ENABLE REGISTER

**Address: 0x14, Reset: 0x00, Name: Negative Precharge Reference Buffer**

This register turns on or off the precharge buffers on the reference negative input to each of the ADCs from Channel 0 to Channel 7.

**Table 51. Bit Descriptions for Negative Precharge Reference Buffer**

| Bits | Bit Name | Settings | Description | Reset |
|---|---|---|---|---|
| 7 | CH7_REFN_BUF | 0<br>1 | Off<br>On | 0x0 |
| 6 | CH6_REFN_BUF | 0<br>1 | Off<br>On | 0x0 |
| 5 | CH5_REFN_BUF | 0<br>1 | Off<br>On | 0x0 |
| 4 | CH4_REFN_BUF | 0<br>1 | Off<br>On | 0x0 |
| 3 | CH3_REFN_BUF | 0<br>1 | Off<br>On | 0x0 |
| 2 | CH2_REFN_BUF | 0<br>1 | Off<br>On | 0x0 |
| 1 | CH1_REFN_BUF | 0<br>1 | Off<br>On | 0x0 |
| 0 | CH0_REFN_BUF | 0<br>1 | Off<br>On | 0x0 |

## OFFSET REGISTERS

The CHx_OFFSET_MSB, CHx_OFFSET_MID, and CHx_OFFSET_LSB registers provide 24-bit, signed twos complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. As offset adjustment occurs before gain adjustment, the ratio above changes linearly with gain adjustment via the CHx_GAIN registers. After a reset or power cycle, the register values revert to the default factory setting.

**Table 52. Per Channel 24-Bit Offset Registers, Three 8-Bit Registers for Each Channel, Split with MSB, MID, and LSB**

| Address | | | Name | Description | Reset | | | Access |
|---|---|---|---|---|---|---|---|---|
| MSB | MID | LSB | | | MSB | MID | LSB | |
| 0x1E | 0x1F | 0x20 | Channel 0 Offset | Channel 0 offset registers, upper, middle and lower bytes (24 bits in total) | 0x00 | 0x00 | 0x00 | RW |
| 0x21 | 0x22 | 0x23 | Channel 1 Offset | Channel 1 offset registers, upper, middle and lower bytes (24 bits in total) | 0x00 | 0x00 | 0x00 | RW |
| 0x24 | 0x25 | 0x26 | Channel 2 Offset | Channel 2 offset registers, upper, middle and lower bytes (24 bits in total) | 0x00 | 0x00 | 0x00 | RW |
| 0x27 | 0x28 | 0x29 | Channel 3 Offset | Channel 3 offset registers, upper, middle and lower bytes (24 bits in total) | 0x00 | 0x00 | 0x00 | RW |
| 0x2A | 0x2B | 0x2C | Channel 4 Offset | Channel 4 offset registers, upper, middle and lower bytes (24 bits in total) | 0x00 | 0x00 | 0x00 | RW |
| 0x2D | 0x2E | 0x2F | Channel 5 Offset | Channel 5 offset registers, upper, middle and lower bytes (24 bits in total) | 0x00 | 0x00 | 0x00 | RW |
| 0x30 | 0x31 | 0x32 | Channel 6 Offset | Channel 6 offset registers, upper, middle and lower bytes (24 bits in total) | 0x00 | 0x00 | 0x00 | RW |
| 0x33 | 0x34 | 0x35 | Channel 7 Offset | Channel 7 offset registers, upper, middle and lower bytes (24 bits in total) | 0x00 | 0x00 | 0x00 | RW |

## GAIN REGISTERS

Each ADC channel has an associated gain coefficient. The coefficient is stored in three single-byte registers split up as MSB, MID, and LSB. Each of the gain registers are factory programmed. Nominally, this gain is around the value 0x555555 (for an ADC channel). The user may overwrite the gain register setting however, after a reset or power cycle, the gain register values revert to the hard coded programmed factory setting.

**Table 53 Per Channel 24-Bit Gain Registers, 3 8-Bit Registers for Each Channel, Split with MSB, MID, and LSB**

| Address | | | | | Reset | | | |
|---|---|---|---|---|---|---|---|---|
| MSB | MID | LSB | Name | Description | MSB | MID | LSB | Access |
| 0x36 | 0x37 | 0x38 | Channel 0 Gain | Channel 0 gain registers, upper, middle and lower bytes (24 bits in total) | 0xXX | 0xXX | 0xXX | RW |
| 0x39 | 0x3A | 0x3B | Channel 1 Gain | Channel 1 gain registers, upper, middle and lower bytes (24 bits in total) | 0xXX | 0xXX | 0xXX | RW |
| 0x3C | 0x3D | 0x3E | Channel 2 Gain | Channel 2 gain registers, upper, middle and lower bytes (24 bits in total) | 0xXX | 0xXX | 0xXX | RW |
| 0x3F | 0x40 | 0x41 | Channel 3 Gain | Channel 3 gain registers, upper, middle and lower bytes (24 bits in total) | 0xXX | 0xXX | 0xXX | RW |
| 0x42 | 0x43 | 0x44 | Channel 4 Gain | Channel 4 gain registers, upper, middle and lower bytes (24 bits in total) | 0xXX | 0xXX | 0xXX | RW |
| 0x45 | 0x46 | 0x47 | Channel 5 Gain | Channel 5 gain registers, upper, middle and lower bytes (24 bits in total) | 0xXX | 0xXX | 0xXX | RW |
| 0x48 | 0x49 | 0x4A | Channel 6 Gain | Channel 6 gain registers, upper, middle and lower bytes (24 bits in total) | 0xXX | 0xXX | 0xXX | RW |
| 0x4B | 0x4C | 0x4D | Channel 7 Gain | Channel 7 gain registers, upper, middle and lower bytes (24 bits in total) | 0xXX | 0xXX | 0xXX | RW |

## SYNC PHASE OFFSET REGISTERS

The AD7768 has one synchronization signal for all channels. The sync phase offset register allows the user to vary the phase delay on each of the channels relative to the synchronization edge received on the $\overline{\text{SYNC\_IN}}$ pin. See the Sync Phase Offset Adjustment section for details on the use of this function.

**Table 54. Per Channel 8-Bit Sync Phase Offset Registers**

| Address | Name | Description | Reset | Access |
|---|---|---|---|---|
| 0x4E | Channel 0 Sync Offset | Channel 0 sync phase offset register | 0x00 | RW |
| 0x4F | Channel 1 Sync Offset | Channel 1 sync phase offset register | 0x00 | RW |
| 0x50 | Channel 2 Sync Offset | Channel 2 sync phase offset register | 0x00 | RW |
| 0x51 | Channel 3 Sync Offset | Channel 3 sync phase offset register | 0x00 | RW |
| 0x52 | Channel 4 Sync Offset | Channel 4 sync phase offset register | 0x00 | RW |
| 0x53 | Channel 5 Sync Offset | Channel 5 sync phase offset register | 0x00 | RW |
| 0x54 | Channel 6 Sync Offset | Channel 6 sync phase offset register | 0x00 | RW |
| 0x55 | Channel 7 Sync Offset | Channel 7 sync phase offset register | 0x00 | RW |

## ADC DIAGNOSTIC RECEIVE SELECT REGISTER

**Address: 0x56, Reset: 0x00, Name: Diagnostic Rx**

The AD7768 ADC diagnostic allows the user to select a zero-scale, positive full-scale, or negative full-scale input to the ADC, which can be converted to verify the correct operation of the ADC channel. This register enables the diagnostic. Enable the receive (Rx) for each channel and set each bit in this register to 1.

The ADC diagnostic feature depends on some features of the analog input precharge buffers. The user must ensure that the analog input precharge buffers are enabled on the channels that are selected to receive the diagnostic voltages internally.

**Table 55. Bit Descriptions for Diagnostic Rx**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 7 | CH7_RX | | Channel 7 | 0x0 | RW |
| | | 0 | Not in use | | |
| | | 1 | Receive | | |
| 6 | CH6_RX | | Channel 6 | 0x0 | RW |
| | | 0 | Not in use | | |
| | | 1 | Receive | | |
| 5 | CH5_RX | | Channel 5 | 0x0 | RW |
| | | 0 | Not in use | | |
| | | 1 | Receive | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| 4 | CH4_RX | | Channel 4 | 0x0 | RW |
| | | 0 | Not in use | | |
| | | 1 | Receive | | |
| 3 | CH3_RX | | Channel 3 | 0x0 | RW |
| | | 0 | Not in use | | |
| | | 1 | Receive | | |
| 2 | CH2_RX | | Channel 2 | 0x0 | RW |
| | | 0 | Not in use | | |
| | | 1 | Receive | | |
| 1 | CH1_RX | | Channel 1 | 0x0 | RW |
| | | 0 | Not in use | | |
| | | 1 | Receive | | |
| 0 | CH0_RX | | Channel 0 | 0x0 | RW |
| | | 0 | Not in use | | |
| | | 1 | Receive | | |

## ADC DIAGNOSTIC CONTROL REGISTER

**Address: 0x57, Reset: 0x00, Name: Diagnostic Mux Control**

The AD7768 ADC diagnostic allows the user to select a zero-scale, positive full-scale, or negative full-scale input to the ADC, which can be converted to verify the correct operation of the ADC channel. This register controls the voltage that is applied to each of the ADC channels for the diagnostic. There are three input voltage options that the user can select. The voltage selected is mapped the channels based on which mode (Mode A or Mode B) they belong to. This is set according to the channel mode select register (Register 0x03).

Set Bits[7:0] to 1 in the ADC diagnostic receive select register, then select the voltage check desired for the channels on Mode A and the channels on Mode B through Bits[2:0] and Bits[6:4], respectively.

**Table 56. Bit Descriptions for Diagnostic Mux Control**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [6:4] | GRPB_SEL | | Mux B. | 0x0 | RW |
| | | 000 | Off. | | |
| | | 011 | Positive full-scale ADC check. A voltage close to positive full-scale is applied internally to the ADC channel. | | |
| | | 100 | Negative full-scale ADC check. A voltage close to negative (or minus) full-scale is applied internally to the ADC channel. | | |
| | | 101 | Zero-scale ADC check. A voltage close to 0 V is applied internally to the ADC channel. | | |
| [2:0] | GRPA_SEL | | Mux A. | 0x0 | RW |
| | | 000 | Off. | | |
| | | 011 | Positive full-scale ADC check. A voltage close to positive full-scale is applied internally to the ADC channel. | | |
| | | 100 | Negative full-scale ADC check. A voltage close to negative (or minus) full-scale is applied internally to the ADC channel. | | |
| | | 101 | Zero-scale ADC check. A voltage close to 0 V is applied internally to the ADC channel. | | |

## MODULATOR DELAY CONTROL REGISTER

**Address: 0x58, Reset: 0x02, Name: Modulator Delay Control**

**Table 57. Bit Descriptions for Modulator Delay Control**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [3:2] | CLK_MOD_DEL_EN | | Enable delayed modulator clock. | 0x0 | RW |
| | | 00 | Disabled delayed clock for all channels. | | |
| | | 01 | Enable delayed clock for Channel 0 to Channel 3 only. | | |
| | | 10 | Enable delayed clock for Channel 4 to Channel 7 only. | | |
| | | 11 | Enable delayed clock for all channels. | | |
| [1:0] | Reserved | 10 | Not a user option. Must be set to 0x2. | 0x2 | RW |

## CHOPPING CONTROL REGISTER

**Address: 0x59, Reset: 0x0A, Name: Chop Control**

**Table 58. Bit Descriptions for Chop Control**

| Bits | Bit Name | Settings | Description | Reset | Access |
|---|---|---|---|---|---|
| [3:2] | GRPA_CHOP | | Group A chopping | 0x2 | RW |
| | | 01 | Chop at $f_{MOD}/8$ | | |
| | | 10 | Chop at $f_{MOD}/32$ | | |
| [1:0] | GRPB_CHOP | | Group B chopping | 0x2 | RW |
| | | 01 | Chop at $f_{MOD}/8$ | | |
| | | 10 | Chop at $f_{MOD}/32$ | | |

# OUTLINE DIMENSIONS

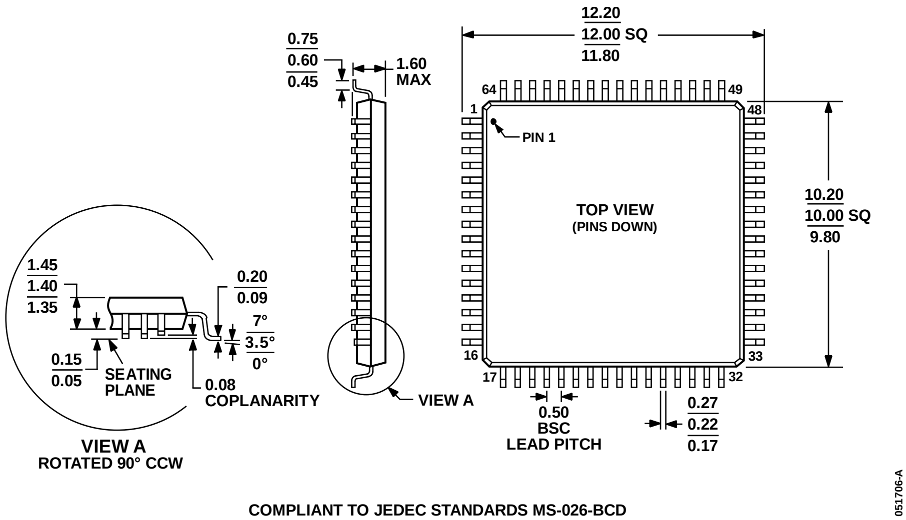



*Figure 105. 64-Lead Low Profile Quad Flat Package [LQFP]*
*(ST-64-2)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD7768BSTZ | −40°C to +105°C | 64-Lead Low Profile Quad Flat Package [LQFP] | ST-64-2 |
| AD7768BSTZ-RL7 | −40°C to +105°C | 64-Lead Low Profile Quad Flat Package [LQFP] | ST-64-2 |
| AD7768BSTZ-RL | −40°C to +105°C | 64-Lead Low Profile Quad Flat Package [LQFP] | ST-64-2 |
| EVAL-AD7768FMCZ | | Evaluation Board | |
| EVAL-SDP-CH1Z | | Controller Board | |

[1] Z = RoHS Compliant Part.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