Click here for production status of specific part numbers.

MAX25201/MAX25202

36V HV Synchronous Boost Controller for Automotive Infotainment Applications

General Description

The MAX2501/MAX25202 are high-performance, current-mode PWM controllers with 1.5µA (typ) shutdown current for wide input voltage range boost converters. The 4.5V to 36V input operating voltage range makes these devices ideal in automotive applications, such as front-end preboost or general-purpose boost power supply, for the first boost stage in high-power LED lighting applications or to generate audio amplifier voltages. An internal low-dropout regulator with a 5V output voltage enables the MAX25201/MAX25202 to operate directly from an automotive battery input. The input operating range can be extended to as low as 1.8V after startup.

The MAX25201/MAX25202's switching frequency operation (up to 2.2MHz) reduces output ripple, avoids AM band interference, and allows for the use of smaller external components. The switching frequency is resistor adjustable from 220kHz to 2.2MHz. Alternatively, the frequency can be synchronized to an external clock. A spread-spectrum option is available to improve system EMI performance. For high-current applications the dual-phase MAX25202 is available. The MAX25202 operates at a fixed 400kHz switching frequency and can be synchronized to an external clock.

The controllers feature a power-OK monitor and undervoltage lockout. Protection features include cycle-by-cycle current limit and thermal shutdown. The MAX25201/MAX25202 operate over the -40°C to +125°C automotive temperature range.

Applications

Infotainment Systems

Cluster Systems

E-Call

Benefits and Features

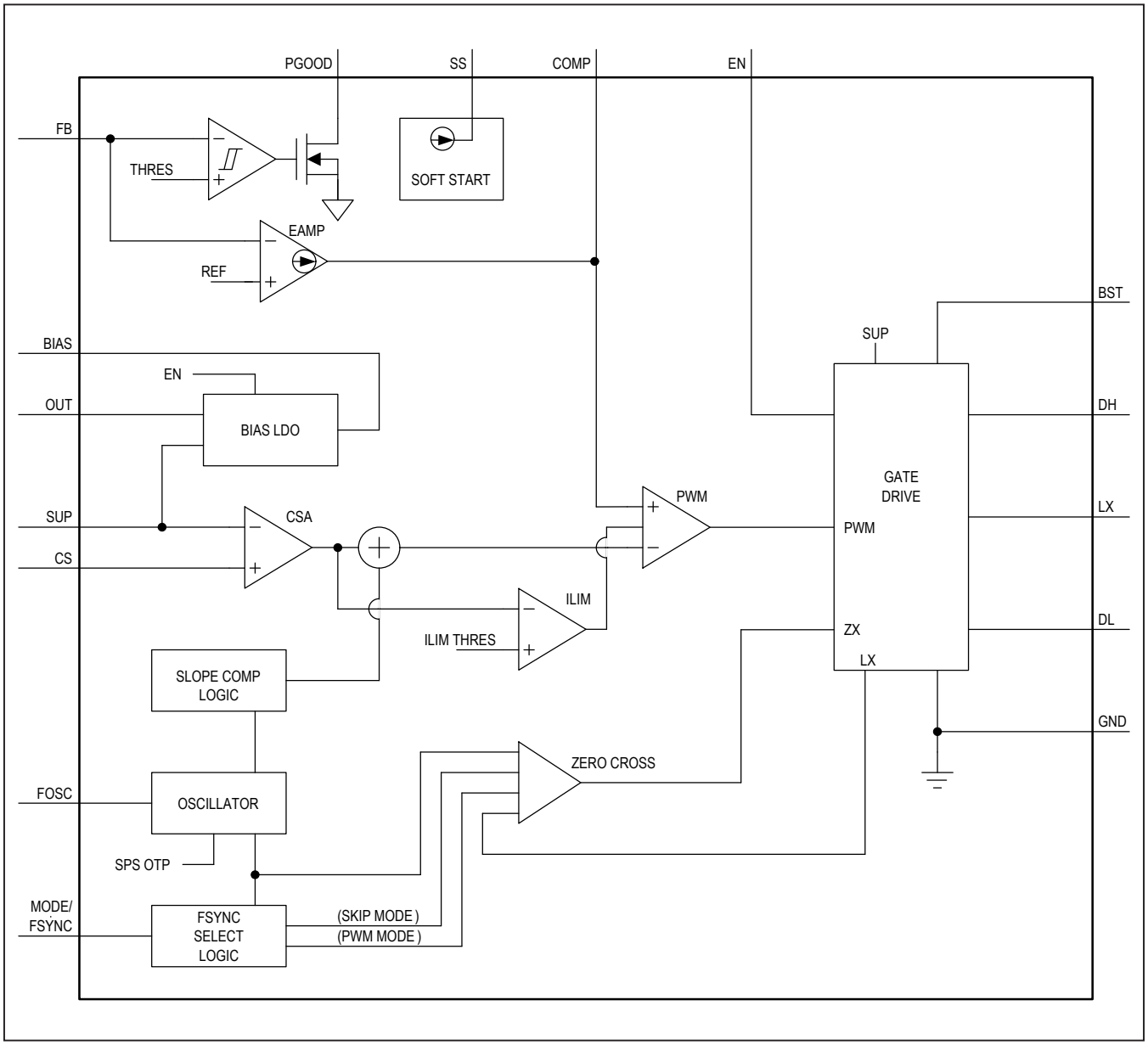
- Meets Stringent OEM Module Power Consumption and Performance Specifications
  - 20µA Quiescent Current in Skip Mode
  - ±1.5% FB Voltage Accuracy
  - Output Voltage Range: Fixed or Adjustable Between 3.5V and 60V
- Enables Crank-Ready Designs
  - Operates Down to 1.8V After Startup
  - Wide Input Supply Range from 4.5V to 36V
- EMI Reduction Features Reduce Interference with Sensitive Radio Bands Without Sacrificing Wide Input Voltage Range
  - Spread-Spectrum Option
  - Frequency-Synchronization Input
  - Resistor-Programmable Frequency Between 200kHz and 2.2MHz
- Integration and Thermally Enhanced Packages Save Board Space and Cost
  - Current-Mode Controllers with Forced-Continuous and Skip Modes
  - Thermally Enhanced 16-Pin TQFN-EP Package
- Protection Features Improve System Reliability
  - Supply Undervoltage Lockout
  - Overtemperature and Short-Circuit Protection

***Ordering Information* appears at end of data sheet.**

19-100588; Rev 3; 2/20

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

SUP, EN to GND .....-0.3V to 42V
OUT, FB, LX to GND .....-0.3V to 65V
SUP to CS .....-0.3V to 0.3V
BIAS, MODE/FSYNC, PGOOD, SS to GND.....-0.3V to 6V
DL, FOSC, COMP to GND..... -0.3V to BIAS + 0.3V
BST to LX .....-0.3V to 6V
DH to LX.....-0.3V to BST+0.3V
Continuous Power Dissipation
TQFN (derate 28.8mW/°C* above +70°C).....1666mW

Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to 125	°C

Note: These limits are not guaranteed.

Package Information

TQFN

Package Code	T1633Y+5C
Outline Number	**21-100150**
Land Pattern Number	**90-100064**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	44.5°C/W
Junction to Case (θ_{JC})	5°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP} = 14V, V_{EN} = 14V, C_{BIAS} = 1µF, C_{BST} = 0.1µF, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STEP UP CONTROLLER						
Supply Voltage Range		Initial startup, V_{OUT} = V_{BATT}	4.5		36	V
	V_{SUP}	Operation after initial startup condition is satisfied	1.8		36	
Output Over-Voltage Threshold		Detected with respect to V_{FB} rising	102.0	105	107.5	%
Supply Current	I_{IN}	V_{EN} = V_{SUP}, V_{FB} = V_{BIAS} (fixed output voltage), V_{SUP} > V_{OUT}, no load (MAX25201)		25		µA
		V_{EN} = V_{SUP}, V_{SUP} > V_{OUT}, adjustable output, no load. Excludes current through external FB divider (MAX25201)		20		
		Shutdown, V_{EN} = 0V, fixed output voltage		1.5	3	
		Shutdown, V_{EN} = 0V, adjustable output, excludes current through external FB divider		1.5	3	
Fixed Output Voltage	V_{OUT}	V_{FB} = V_{BIAS}, PWM mode, MAX25201ATEA/VY+ and MAX25201ATEB/VY+ only	9.85	10.04	10.25	V
		V_{FB} = V_{BIAS}, skip mode, MAX25201ATEA/VY+ and MAX25201ATEB/VY+ only	9.70	10.04	10.30	
Output Voltage Adjustable Range		MAX25201ATEA/VY+ and MAX25201ATEB/VY+	3.5		36	V
		MAX25201ATEC/VY+, MAX25201ATED/VY+, MAX25202MATEA/VY+, MAX25202SATEA/VY+	20		60	
Regulated Feedback Voltage	V_{FB}		0.99	1.005	1.02	V
Feedback Leakage Current	I_{FB}	T_A = 25°C		0.01	1	µA
Feedback Line Regulation Error		V_{IN} = 3.5V to 36V, V_{FB} = 1V		0.01		%/V
Transconductance (from FB to COMP)	gm_boost	V_{FB} = 1V, V_{BIAS} = 5V (Note 1)	165	250	345	µS
Dead Time		DL low to DH rising		20		ns
		DH low to DL rising		20		
DH Pullup Resistance		V_{BIAS} = 5V, I_{DH} = -100mA		1.5	2.6	Ω
DH Pulldown Resistance		V_{BIAS} = 5V, I_{DH} = 100mA		1	2	Ω
DL Pullup Resistance		V_{BIAS} = 5V, I_{DL} = -100mA		1.5	2.8	Ω
DL Pulldown Resistance		V_{BIAS} = 5V, I_{DL} = 100mA		1	2	Ω
Minimum Off Time	t_{OFFBST}			80		ns
PWM Switching Frequency Range	f_{SW}	MAX25201, programmable with R_{FOSC}	0.22		2.2	MHz
Switching Frequency Accuracy		R_{FOSC} = 70kΩ, V_{BIAS} = 5V, 3.3V (MAX25201)	380	400	420	kHz
		MAX25202M/MAX25202S	375	400	425	

Electrical Characteristics (continued)

(V_{SUP} = 14V, V_{EN} = 14V, C_{BIAS} = 1µF, C_{BST} = 0.1µF, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CS Current-Limit Voltage Threshold	V_{LIMIT}	V_{SUP} - V_{CS}; V_{BIAS} = 5V, V_{SUP} > 2.5V	MAX25201	40	50	60	mV
			MAX25202M/S	36	48	60	
Soft-Start Current Source	I_{SS}	V_{BIAS} = 5V		8	10	12	µA
LX Leakage Current		V_{LX} = V_{PGND} or V_{SUP}, T_A = 25°C			0.001	5	µA
PGOOD Threshold	PGOOD_H	% of V_{FB}, rising		92.5	94.5	96.5	%
	PGOOD_F	% of V_{FB}, falling		90.5	92.5	94.5	
PGOOD Leakage Current		V_{PGOOD} = 5V, T_A = 25°C				1	µA
PGOOD Output Low Voltage		I_{PGOOD} = 1mA				0.2	V
PGOOD Debounce Time		Fault detection, rising and falling			150		µs
PGOOD Timeout		Output in regulation to PGOOD high			1.5		ms
FSYNC INPUT							
FSYNC Frequency Range		Minimum sync pulse of 100ns, f_{OSC} = 2.2MHz		1.8		2.6	MHz
		Minimum sync pulse of 100ns, f_{OSC} = 400kHz		250		550	kHz
FSYNC Switching Thresholds		High threshold		1.4			V
		Low threshold				0.4	
INTERNAL LDO BIAS							
Internal BIAS Voltage		V_{IN} > 6V			5		V
BIAS UVLO Threshold		V_{BIAS} rising			3.1	3.25	V
		V_{BIAS} falling		2.4	2.6		
Minimum Current Capability		V_{BIAS} = 5V			150		mA
THERMAL OVERLOAD							
Thermal Shutdown Temperature		(Note 1)			170		°C
Thermal Shutdown Hysteresis		(Note 1)			20		°C
EN LOGIC INPUT							
High Threshold				1.8			V
Low Threshold						0.8	V
EN Input Bias Current		EN logic inputs only, T_A = 25°C			0.01	1	µA
SPREAD SPECTRUM							
Spread Spectrum					f_{OSC} ± 6%		

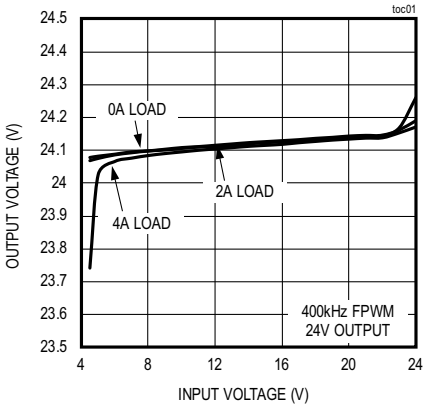
Note 1: Limits are 100% tested at +25°C. Limits over operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at +25°C.

Note 2: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

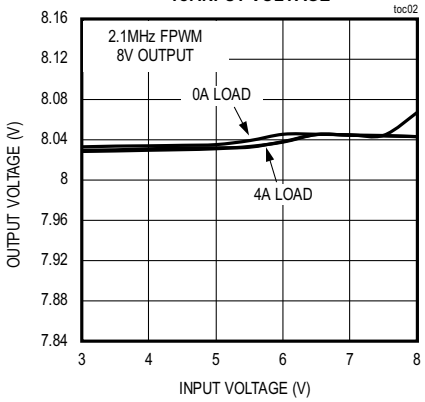
Typical Operating Characteristics

(V_{SUP} = 14V, T_A = 25°C, unless otherwise noted.)

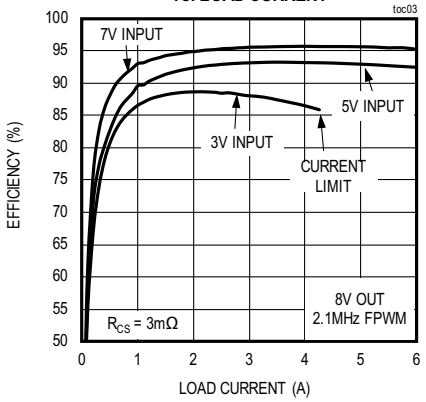
OUTPUT VOLTAGE vs. INPUT VOLTAGE



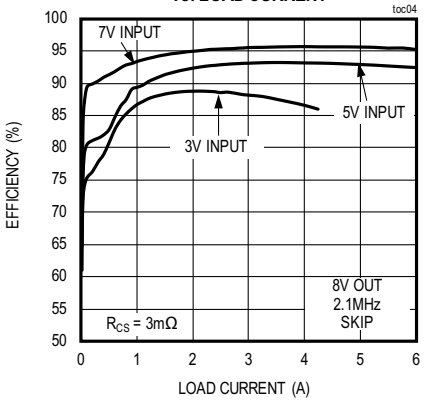
OUTPUT VOLTAGE vs. INPUT VOLTAGE



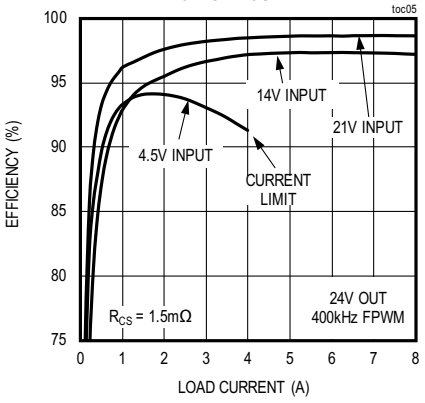
MAX25201 EFFICIENCY vs. LOAD CURRENT



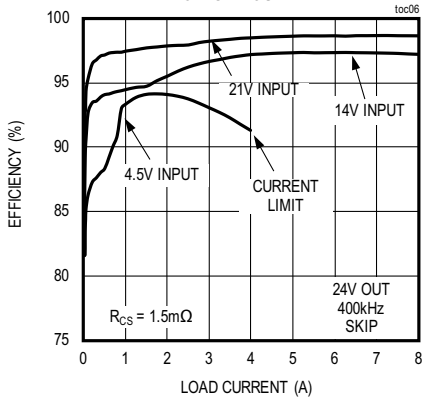
MAX25201 EFFICIENCY vs. LOAD CURRENT



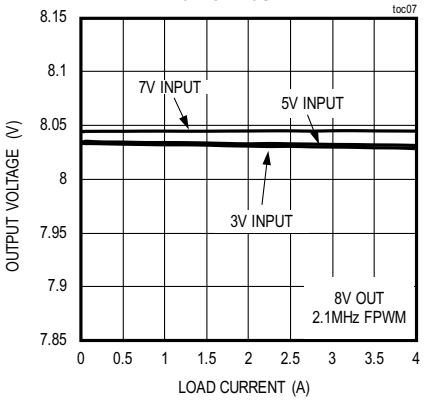
MAX25201 EFFICIENCY vs. LOAD CURRENT



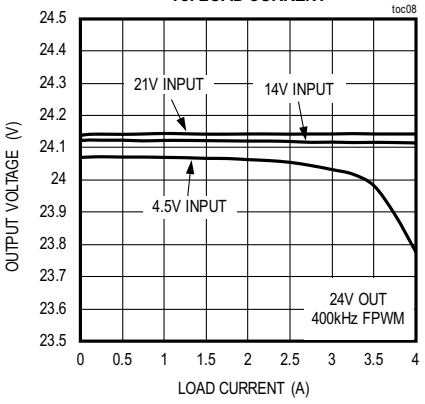
MAX25201 EFFICIENCY vs. LOAD CURRENT



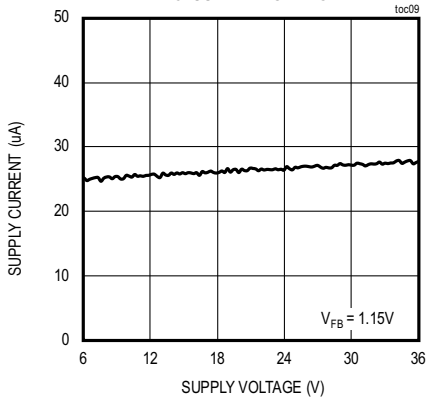
OUTPUT VOLTAGE vs. LOAD CURRENT



OUTPUT VOLTAGE vs. LOAD CURRENT



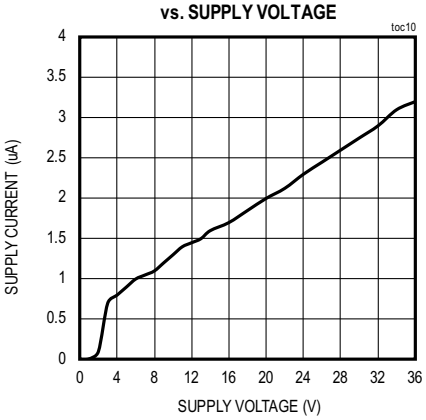
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



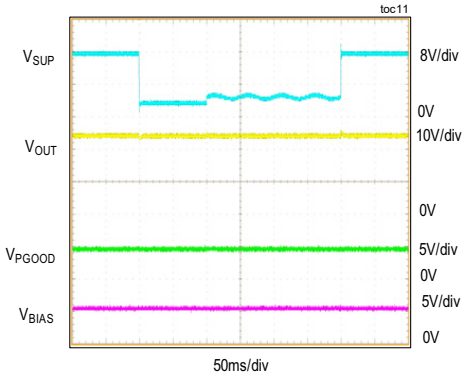
Typical Operating Characteristics (continued)

(V_{SUP} = 14V, T_A = 25°C, unless otherwise noted.)

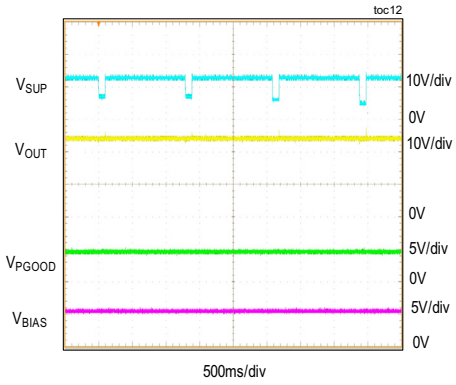
SHUTDOWN SUPPLY CURRENT
vs. SUPPLY VOLTAGE



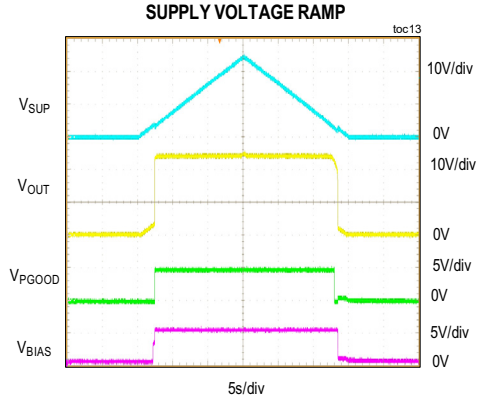
COLD-CRANK INPUT
VOLTAGE TRANSIENT



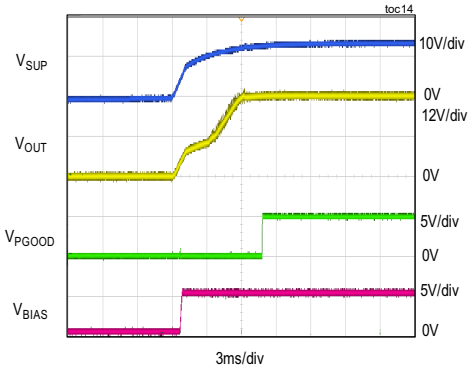
INPUT UNDERVOLTAGE PULSE



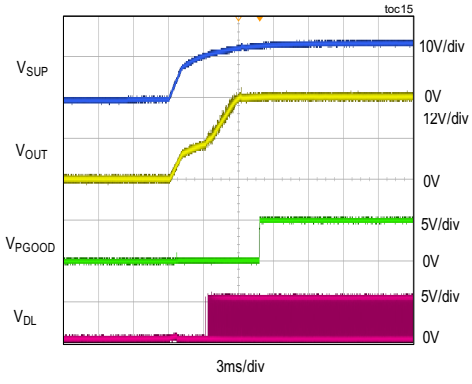
SUPPLY VOLTAGE RAMP



POWER-UP RESPONSE



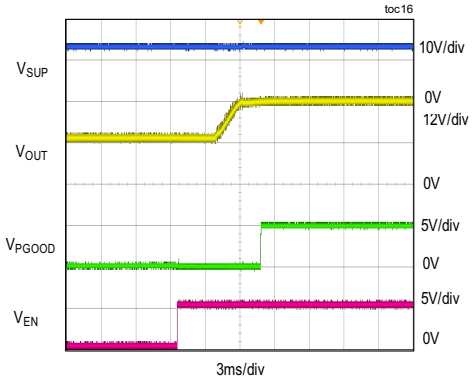
POWER-UP RESPONSE



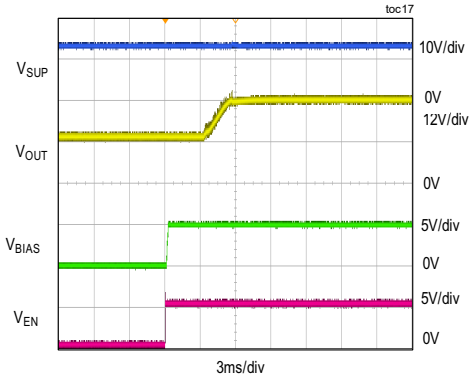
Typical Operating Characteristics (continued)

(V_{SUP} = 14V, T_A = 25°C, unless otherwise noted.)

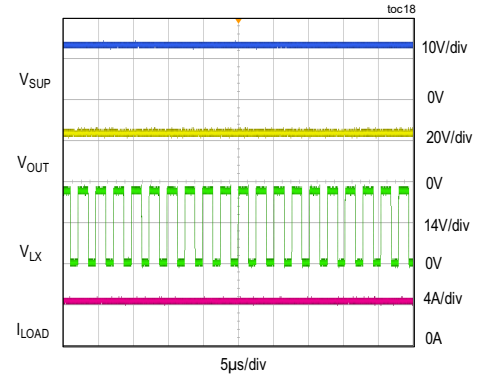
STARTUP RESPONSE



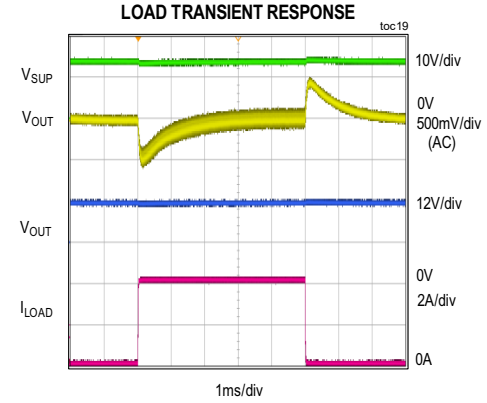
STARTUP RESPONSE



SWITCHING WAVEFORM

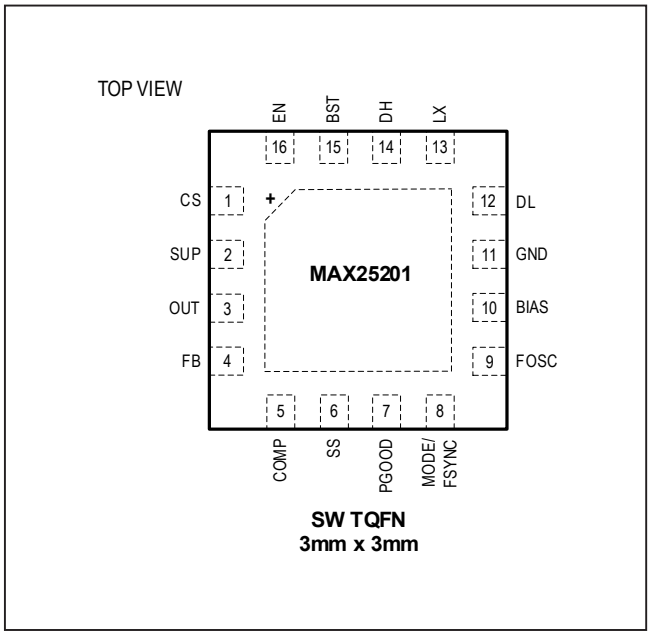


LOAD TRANSIENT RESPONSE

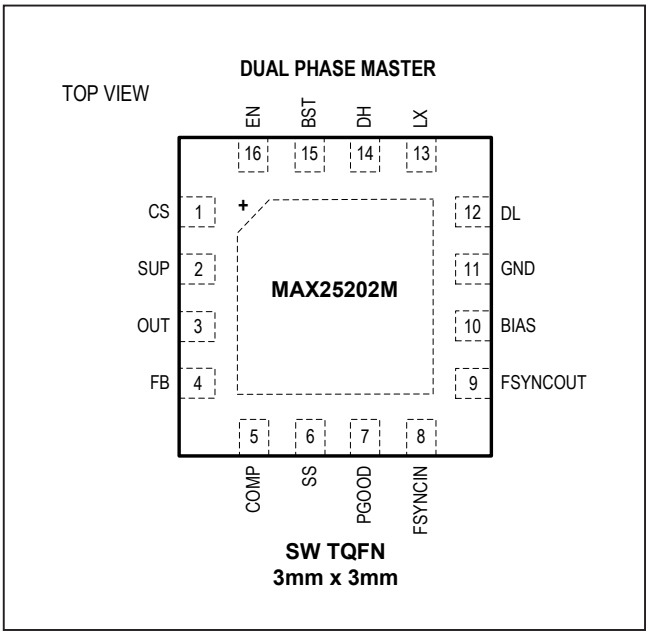


Pin Configurations

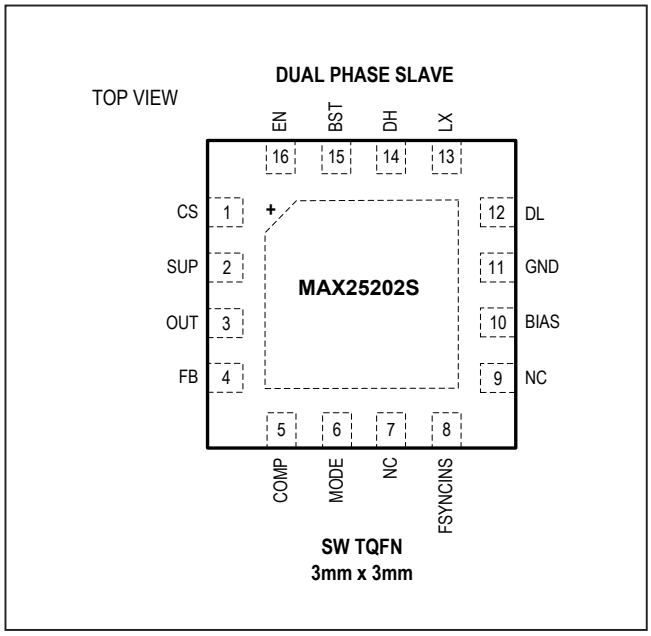
MAX25201



MAX25202M



MAX25202S



Pin Description

PIN			NAME	FUNCTION
MAX25201	MAX25202M	MAX25202S		
1	1	1	CS	Negative Current-Sense Input for Boost Controller. Connect CS to the negative side of the current-sense element. See the *Current Limiting and Current-Sense Inputs (SUP and CS)* and *Current-Sense Resistor Selection* sections.
2	2	2	SUP	Supply Input and Positive Current-Sense Input for Boost Controller. Connect SUP to the positive terminal of the current-sense element. See the *Current Limiting and Current-Sense Inputs (SUP and CS)* and Current Sense Measurement sections.
3	3	3	OUT	Input for the BIAS LDO. Connect OUT to the boost output when the output voltage is set at 24V or below. For V_{OUT} greater than 24V, connect OUT to the input supply.
4	4	4	FB	Boost Converter Feedback Input. To set the output voltage between 3.5V and 60V, connect FB to the center tap of a resistive divider between the boost regulator output. FB regulates to 1V (typ). To use the factory set fixed output voltage on applicable parts (see the *Ordering Information* section, connect FB to BIAS and connect OUT to the output. For more information, see the *Setting the Output Voltage* section.
5	5	5	COMP	Boost Controller Error Amplifier Output. Connect a RC network to COMP to compensate boost converter.
6	6	—	SS	Programmable Soft-Start. Connect a capacitor from SS to GND to set the soft-start time. To select the value, see the *Typical Operating Characteristics* section.
—	—	6	MODE	Connect to FSYNCIN of the MAX25202M.
7	7	—	PGOOD	Open-Drain Power-Good Output for Buck Controller One. PGOOD goes low if OUT drops below 92.5% (typ falling) of the normal regulation point. PGOOD asserts low during soft-start and in shutdown. PGOOD becomes high impedance when OUT is in regulation. To obtain a logic signal, pull up PGOOD with an external resistor connected to a positive voltage lower than 5.5V.
—	—	7, 9	NC	Do Not Connect
8	—	—	MODE/ FSYNC	External Clock Synchronization Input. To use the internal oscillator connect MODE/FSYNC high for forced-PWM or low for skip-mode operation. To synchronize with an external clock, connect the clock to MODE/ FSYNC. See the *Light-Load Efficiency Skip Mode* and *Forced-PWM Mode* sections.
—	8	—	FSYNCIN	Synchronization Input. Connect to an external clock for synchronization. Connect to ground for internal frequency setting. When an external signal is connected, the spread spectrum is disabled.
—	—	8	FSYNCINS	Slave Input Synchronization. For dual-phase operation, connect FSYNCINS of the MAX25202S to FSYNCOUT of the MAX25202M.
9	—	—	FOSC	Frequency Setting Input. Connect a resistor to FOSC to set the switching frequency of the DC-DC converters.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX25201	MAX25202M	MAX25202S		
—	9	—	FSYNCOUT	Clock Synchronization Output. Connect FSYNCOUT to FSYNCINS of the MAX25202S.
10	10	10	BIAS	5V Internal Linear Regulator Output. Bypass BIAS to GND with a low-ESR ceramic capacitor of 1µF minimum value. BIAS provides the power to the internal circuitry and external loads. See the *Fixed 5V Linear Regulator (BIAS)* section.
11	11	11	GND	Ground
12	12	12	DL	Low-Side N-Channel MOSFET Gate Driver Output
13	13	13	LX	Inductor Connection for Boost Controller. Connect LX to the switched side of the inductor. LX serves as the lower supply rail for the DH high-side gate driver.
14	14	14	DH	High-Side MOSFET Gate Driver Output for Boost Controller. DH output voltage swings from V_{LX} to V_{BST}.
15	15	15	BST	Boost Flying Capacitor Connection for High-Side Gate Voltage of Boost Controller. Connect a high-voltage diode between BIAS and BST. Connect a ceramic capacitor between BST and LX. See the *High-Side Gate-Driver Supply (BST)* section.
16	16	16	EN	High-Voltage Tolerant, Active-High Digital Enable Input for Controller
—	—	—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to GND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Detailed Description

The MAX25201/MAX25202 automotive controller maintains regulation during cold crank or start-stop operations down to a battery input of 1.8V, and operates with only 20µA I_Q. The devices generate backlight voltages, audio amplifier voltages, stand-alone preboost, as well as a standby voltage in telematics applications. The devices can start up with an input voltage supply from 3.5V to 42V and can operate down to 1.8V after startup.

The MAX25201/MAX25202's 2.2MHz switching frequency reduces output ripple, avoids AM band interference, and allows for the use of smaller external components. The switching frequency is resistor adjustable from 220kHz to 2.2MHz. Alternatively, the frequency can be synchronized to an external clock. A spread-spectrum option is available to improve system EMI performance.

These controllers feature a power-OK monitor as well as overvoltage and undervoltage lockout. Protection features include cycle-by-cycle current limit and thermal shutdown. The MAX25201/MAX25202 are specified for operation over the -40°C to +125°C automotive temperature range.

Current-Mode Control Loop

Peak current-mode control operation provides excellent load step performance and simple compensation. The inherent feed-forward characteristic is useful especially in automotive applications where the input voltage changes quickly during cold-crank and load dump conditions. To avoid premature turn-off at the beginning of the on cycle the current-limit and PWM comparator inputs have leading-edge blanking.

Fixed 5V Linear Regulator (BIAS)

An internal 5V linear regulator (BIAS) is used to power the controller's internal circuitry. Connect a 1µF or greater ceramic capacitor from BIAS to GND as close as possible to the IC pins to guarantee stability under the full-load condition. The internal linear regulator can provide up to 150mA (typ) total. The internal bias current requirements can be estimated as follows:

$$I_{BIAS} = I_{CC} + f_{SW} (QG\_DL + QG\_DH)$$

where:

I_{CC} = the internal supply current

f_{SW} = the switching frequency

QG_ = the low- and high-side MOSFET total gate charge (specification limits at V_{GS} = 5V).

To reduce the internal power dissipation, BIAS can optionally be connected to an external 5V rail, bypassing the internal linear regulator.

The OUT pin is the input to the linear regulator. OUT is typically connected to the boost output for applications with the output voltage set to 24V or less and applications that require operation with a supply voltage below 5.2V. To reduce power dissipation in applications with higher output voltages, OUT should be connected to SUP. Bypass OUT with a 1µF or greater ceramic capacitor to GND.

Startup Operation/UVLO/EN

The BIAS undervoltage lockout (UVLO) circuitry inhibits switching if the 5V bias supply (BIAS) is below its 2.6V (typ) UVLO falling threshold. Once BIAS rises above its UVLO rising threshold and EN is high, the boost controller starts switching and the output voltage begins to ramp up using soft-start. Driving EN low disables the device and reduces the standby current to less than 10µA.

Soft-Start

Soft-start ramps up the internal reference during startup to reduce input surge current. Connect a capacitor from SS to GND to set the soft-start time. Select the capacitor value as follows:

$$C_{SS}\ [nF] = 10 \times t_{ss}\ [ms]$$

Soft-start begins when EN is logic-high and V_{BIAS} is above the undervoltage lockout threshold.

Oscillator Frequency/External Synchronization

The MAX25201's internal oscillator is set by a resistor connected from FOSC to GND with an adjustment range of 220kHz to 2.2MHz. High-frequency operation optimizes the application for the smallest component size, trading off efficiency to higher switching losses. Low-frequency operation offers the best overall efficiency at the expense of component size and board space.

$$F_{SW} = \frac{24500 + \sqrt{\frac{R_{FOSC}}{0.006}}}{R_{FOSC}}$$

The MAX25202's internal oscillator is fixed at 400kHz.

The devices can also be synchronized to an external clock by connecting the external clock signal to MODE/FSYNC (MAX25201) or FSYNCIN (MAX25202M). The internal oscillator is synchronized on the rising edge of the external clock. See the *Electrical Characteristics* table for the FSYNC frequency range and voltage levels.

Light-Load Efficiency Skip Mode

The skip mode feature of the MAX25201/MAX25202 is used to improve light-load efficiency. Drive MODE/FSYNC low to enable skip mode.

In skip mode, once the output reaches regulation, the MAX25201/MAX25202 stop switching until the FB voltage drops below the reference voltage. Once the FB voltage has dropped below the reference voltage, the devices resume switching until the inductor current reaches 30% (skip threshold) of the maximum current set by the inductor DCR or current-sense resistor.

Forced-PWM Mode

Drive MODE/FSYNC of the MAX25201/MAX25202 high (connect to BIAS) for forced-PWM operation. This prevents the devices from entering skip mode by disabling the zero-crossing detection of the inductor current, and forces the low-side gate-drive waveform to the complement of the high-side gate-drive waveform. Under light-load the inductor current reverses, discharging the output capacitor. The benefit of forced-PWM mode is that it keeps the switching frequency constant under all load conditions. This reduces ripple and makes it predictable and easier to filter. Forced-PWM mode is useful for improving load-transient response and eliminating unknown frequency harmonics that can interfere with AM radio bands. The disadvantage with forced-PWM operation is that it reduces light-load efficiency.

Forced-PWM is always used when synchronizing to an external clock and in multiphase applications.

Spread Spectrum

Spread spectrum reduces peak emission noise at the clock frequency and its harmonics, making it easier to meet stringent EMI limits. This is done by dithering the switching frequency ±6%. Using an external clock source (i.e. driving the MODE/FSYNC input with an external clock) disables spread spectrum.

Spread spectrum is a factory set option. See the *Ordering Information* section to determine which part numbers have spread spectrum enabled.

MOSFET Drivers (DH and DL)

The DH high-side n-channel MOSFET driver is powered from BST. The low-side driver (DL) is powered from BIAS. To prevent a MOSFET from turning on before a complementary switch is fully off, each driver has shoot-through protection that monitors the gate-to-source voltage of the external MOSFETs. A low-resistance, low-inductance path from DL and DH to the MOSFET gates is required in order for the protection circuits to work properly.

High-Side Gate-Driver Supply (BST)

The high-side MOSFET is turned on by closing an internal switch between BST and DH and transferring the bootstrap capacitor's (at BST) charge to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX voltage drops down to ground potential, taking the negative terminal of the capacitor to the same potential. The bootstrap diode then recharges the positive terminal of the bootstrap capacitor.

The selected n-channel high-side MOSFET determines the appropriate boost capacitance values according to the following equation:

$$C_{BST} = Q_G/\Delta V_{BST}$$

where:

Q_G = the total gate charge of the high-side MOSFET

ΔV_{BST} = the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST} such that the available gate-drive voltage is not significantly degraded (e.g., ΔV_{BST} = 100mV to 300mV) when determining C_{BST}. The boost capacitor should be a low-ESR ceramic capacitor. A minimum value of 0.1µF works well in most cases.

Current Limiting and Current-Sense Inputs (SUP and CS)

The current-limit circuit uses differential current-sense inputs (SUP and CS) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold (V_{LIMIT} > 50mV (typ)), the PWM controller turns off the high-side MOSFET.

For the most accurate current sensing, use a current-sense resistor between the inductor and the input capacitor. Connect CS to the inductor side of R_{CS} and SUP to the capacitor side. See the *Current-Sense Resistor Selection* section to determine the resistor value.

To improve efficiency, the current can also be measured directly across the inductor, eliminating the power loss from the sense resistor. However, this method is significantly less accurate and requires a filter network in the current-sense circuit. See the *Inductor DCR Current Sense* section for more information.

Voltage Monitoring (PGOOD)

PGOOD is the open-drain output of the output voltage monitor. PGOOD is high impedance when the output voltage is in regulation. PGOOD pulls low when the output voltage drops below the PGOOD threshold. See the *Electrical Characteristics* table. Typically, a pullup resistor is connected from PGOOD to the relevant logic rail to provide a logic-level output. PGOOD asserts low during soft-start and when disabled (EN is low).

Protection Features

Overcurrent Protection

If the inductor current exceeds the maximum current limit set by R_{CS} or inductor DCR sensing, the respective MOSFET driver turns off. Increasing the output current further results in shorter and shorter high-side pulses. A hard short results in a minimum on-time pulse every clock cycle. When required, choose components that can withstand the short-circuit current.

Thermal Overload Protection

Thermal-overload protection limits total power dissipation in the MAX25201/MAX25202. When the junction temperature exceeds +170°C (typ), an internal thermal sensor shuts the devices off, allowing them to cool down. The thermal sensor turns the devices on again after the junction temperature cools by 20°C (typ).

Overvoltage Protection

The devices limit the output voltage by turning off the high-side gate driver if the output voltage exceeds 105% (typ) of the nominal output voltage. The output voltage must come back into regulation before the devices resume switching.

Slope Compensation

The devices use an internal current-ramp generator for slope compensation. The slope compensation for the MAX25201A and MAX25201B is optimized for operation with output voltage set to 36V or lower. The MAX25201C, MAX25201D, and MAX25202 are optimized for output voltages between 20V and 60V.

Applications Information

Setting the Output Voltage

All versions of the MAX25201/MAX25202 support an adjustable output voltage. See the *Ordering Information* section for the adjustable output voltage range. To set the output voltage, connect FB to the center a resistor divider from the output to ground. Calculate the resistor values as follows:

$$R1 = R2 \left[\frac{V_{OUT}}{V_{FB}} - 1\right]$$

where R1 is the resistor connected from FB to the output, R2 is the resistor connected from FB to ground, V_{OUT} is the desired output voltage, and V_{FB} is the regulated feedback voltage (1.005V typ).

Parts with a fixed output voltage option (see the *Ordering Information* section) can also be used without the external FB divider. To use the preset output voltage, connect FB to BIAS, and connect OUT to the regulator output.

Inductor Selection

Duty cycle and frequency are important when calculating the inductor size because the inductor current ramps up during the on-time of the switch and ramps down during its off-time. A higher switching frequency generally improves transient response and reduces component size; however, if the boost components are used as the input filter components during non-boost operation, a low frequency is advantageous.

The duty-cycle range of the boost converter depends on the effective input-to-output voltage ratio. In the following calculations, the duty cycle refers to the on-time of the boost MOSFET:

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{SUP(MIN)}}{V_{OUT(MAX)}}$$

or including losses in the inductor and high-side MOSFET (VON,FET):

$$D_{MAX} = \frac{V_{OUT(MAX)} - V_{SUP(MIN)} + \left(I_{OUT} \times (R_{DC} + R_{HSRDSON})\right)}{V_{OUT(MAX)}}$$

The ratio of the inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good initial value is a 30% peak-to-peak ripple current to average current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR determine the inductor value as follows:

$$L[\mu H] = \frac{V_{SUP} \times D}{f_{SW}[MHz] \times LIR}$$

where:

$D = (V_{OUT}-V_{SUP})/V_{OUT}$

V_{SUP} = Typical input voltage

V_{OUT} = Typical output voltage

$LIR = 0.3 \times I_{OUT}/(1-D)$

Select the inductor with a saturation current rating higher than the peak switch current limit of the converter:

$$I_{L\_PEAK} > I_{L\_MAX} + \frac{\Delta I_{L\_RIP\_MAX}}{2}$$

Running a boost converter in continuous-conduction mode introduces a right-half plane zero into the transfer function. To avoid the effect of this right-half plane zero, the crossover frequency for the control loop should be ≤ 1/3 x f_{RHP_ZERO}. If faster bandwith is required, a smaller inductor and higher switching frequency is recommended.

Input Capacitor Selection

The input current for the boost converter is continuous and the RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value and the maximum ESR using the following equations:

$$C_{SUP} = \frac{\Delta I_L \times D}{4 \times f_{SW} \times \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

where:

$$\Delta I_L = \frac{\left(V_{SUP} - V_{DS}\right) \times D}{L \times f_{SW}}$$

V_{DS} is the total voltage drop across the external MOSFET plus the voltage drop across the inductor ESR. ΔI_L is the peak-to-peak inductor ripple current as calculated above. ΔV_Q is the portion of input ripple due to the capacitor discharge and ΔV_{ESR} is the contribution due to ESR of the capacitor. Assume the input capacitor ripple contribution due to ESR (ΔV_{ESR}) and capacitor discharge (ΔV_Q) are equal when using a combination of ceramic and aluminum capacitors. During the converter turn-on, a large current is drawn from the input source, especially at high output-to-input differential.

Output Capacitor Selection

In a boost converter, the output capacitor supplies the load current when the boost MOSFET is on. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop while supporting the load current. Use the following equations to calculate the output capacitor for a specified output ripple. All ripple values are peak-to-peak:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT}}$$

$$C = \frac{I_{OUT} \times D_{MAX}}{\Delta V_Q \times f_{SW}}$$

I_{OUT} is the load current in A, f_{SW} is in MHz, C_{OUT} is in µF, ΔV_Q is the portion of the ripple due to the capacitor discharge, and ΔV_{ESR} is the contribution due to the ESR of the capacitor. D_{MAX} is the maximum duty cycle at the minimum input voltage. Use a combination of low-ESR ceramic and high-value, low-cost aluminum capacitors for lower output ripple and noise.

Current-Sense Resistor Selection

The current-sense resistor (R_{CS}), connected between the battery and the inductor, sets the current limit. The CS input has a voltage trip level (V_{CS}) of 50mV (typ).

Set the current-limit threshold high enough to accommodate the component variations. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{V_{CS}}{I_{SUP(MAX)}}$$

where $I_{IN(MAX)}$ is the peak current that flows through the MOSFET at full load and minimum V_{IN}.

$$I_{SUP(MAX)} = \frac{I_{LOAD(MAX)}}{1 - D_{MAX}}$$

When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (DL) quickly terminates the on-cycle.

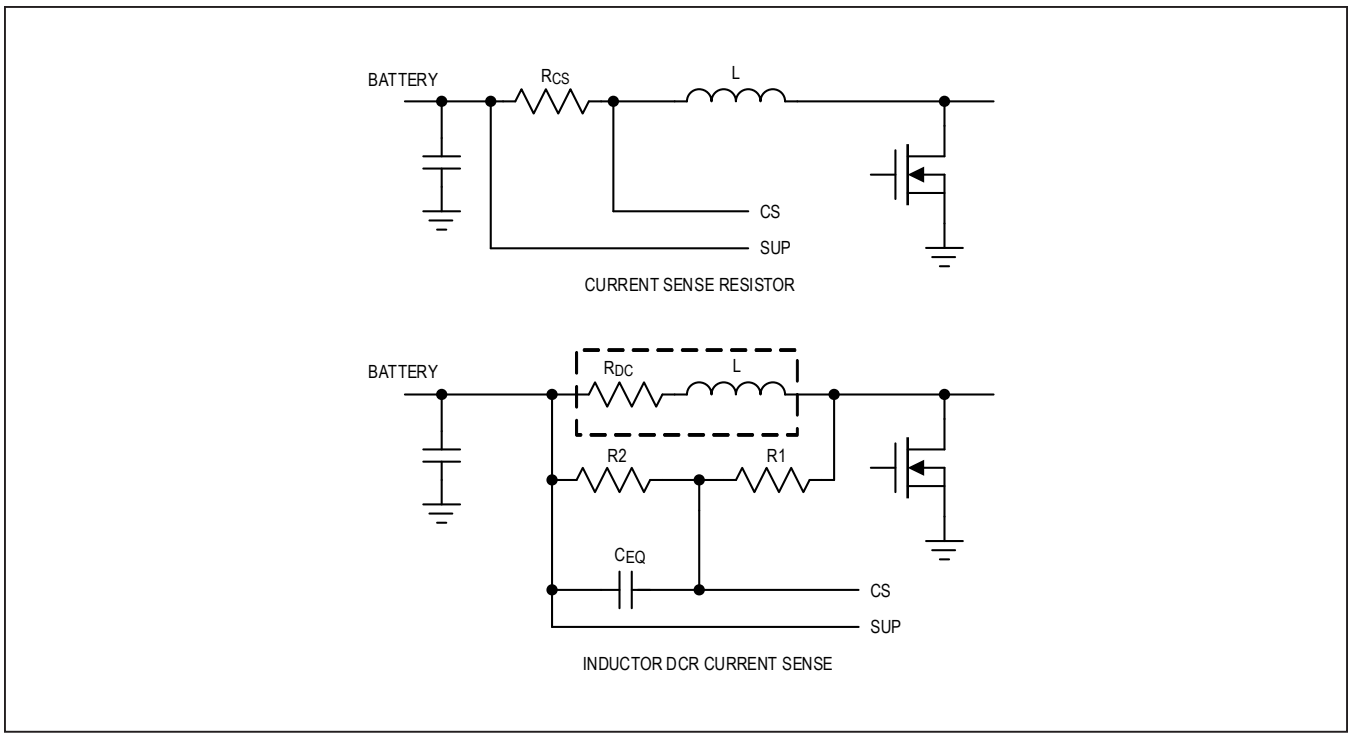


Figure 1. Current-Sense Configurations

Inductor DCR Current Sense

High-power applications that do not require accurate current sense can use the inductor's DC resistance as the current sense element instead of the current-sense resistor. This is done by connecting an RC network across the inductor. The equivalent sense resistance of the network is:

$$R_{CS\_EQ} = \left(\frac{R2}{R1 + R2}\right) \times R_{DC}$$

where R_{DC} is the DC resistance of the inductor, R1 is connected from the switch side of the inductor to CS, and R2 is connected from the battery side of the inductor to CS. The capacitor C_{EQ} (connected parallel to R2) is calculated as follows:

$$C_{EQ} = \frac{L}{R_{DC}}\left(\frac{1}{R1} + \frac{1}{R2}\right)$$

Boost Converter Compensation

The basic regulator loop is modeled as a power modulator, output feedback-divider, and an error amplifier, as shown in the *Synchronous Boost Application Circuit*. The power modulator has a DC gain set by gmc x R_{LOAD}, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The loop response is set by the following equations:

$$G_{MOD} = g_{MC} \times R_{LOAD} \times \left(\frac{1 - D}{2}\right) \times \left(\frac{1 + j\frac{f}{f_{zMOD}}}{1 + j\frac{f}{f_{pMOD}}}\right)$$

$$\times \left(1 - j\frac{f}{f_{Rph\_zMOD}}\right)$$

where $R_{LOAD} = V_{OUT}/I_{LOUT(MAX)}$ in Ω and g_{mc} =1/(A_{V_CS} x R_{DC}) in S. A_{V_CS} is the voltage gain of the current-sense amplifier and is typically 12V/V. R_{DC} is the DC resistance of the inductor or the current-sense resistor in Ω.

In a current-mode step-down converter, the output capacitor and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{\pi \times R_{LOAD} \times C_{OUT}}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

The right-half plane zero is at:

$$f_{Rph\_zMOD} = \frac{R_{LOAD}}{2\pi \times L} \times (1 - D) \times (1 - D)$$

When C_{OUT} is composed of "n" identical capacitors in parallel, the resulting C_{OUT} = n x $C_{OUT(EACH)}$, and ESR = ESR(EACH)/n. Note that the capacitor zero for a parallel combination of similar capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB}$ = V_{FB}/V_{OUT}, where V_{FB} is 1.0V (typ).

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)}$ = $gm_{,EA}$ x $R_{OUT,EA}$, where $gm_{,EA}$ is the error-amplifier transconductance, which is 345µS (max), and $R_{OUT,EA}$ is the output resistance of the error amplifier, which is 10MΩ (typ). See the *Electrical Characteristics* table.

A dominant pole (f_{dpEA}) is set by the compensation capacitor (CC) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{ZEA}) is set by the compensation resistor (RC) and the compensation capacitor (CC). There is an optional pole (f_{PEA}) set by CF and RC to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C), where the loop gain equals 1 (0dB). Thus:

$$f_{pEA} = \frac{1}{2\pi \times \left(R_{OUTEA} + R_C\right) \times C_C}$$

$$f_{zEA} = \frac{1}{2\pi \times R_C \times C_C}$$

$$f_{p2EA} = \frac{1}{2\pi \times R_C \times C_F}$$

The loop gain crossover frequency (f_C) should be ≤ 1/3 of right-half plane zero frequency.

$$f_C \le \frac{f_{Rph\_zMOD}}{3}$$

At the crossover frequency, the total loop gain must be equal to 1. So:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(f_C)} = 1$$

$$GAIN_{EA(f_C)} = g_{m,\,EA} \times R_C$$

$$GAIN_{MOD(f_C)} = GAIN_{MOD(dc)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(f_C)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,\,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,\,EA} \times V_{FB} \times GAIN_{MOD(f_C)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor (C_F) from COMP to GND. The value of C_F is:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

MOSFET Selection

The key selection parameters to choose the n-channel MOSFET used in the boost converter are as follows.

Threshold Voltage

The boost n-channel MOSFETs must be a logic-level type with guaranteed on-resistance specifications at V_{GS} = 4.5V.

Maximum Drain-to-Source Voltage (VDS(MAX))

The MOSFET must be chosen with an appropriate VDS rating to handle all VIN voltage conditions.

Current Capability

The n-channel MOSFET must deliver the input current ($I_{IN(MAX)}$):

$$I_{IN(MAX)} = I_{LOAD(MAX)} \times \frac{D_{MAX}}{1 - D_{MAX}}$$

Choose MOSFETs with the appropriate average current at V_{GS} = 4.5V.

Low Voltage Operation

The devices start with a supply voltage as low as 4.5V, and can operate after initial start up with a supply voltage as low as 1.8V. At very low input voltages it is important to remember that input current will be high and the power components (inductor, MOSFET, and diode) must be specified for this higher input current.

In addition, the current-limit must be set high enough so that the limit is not reached during the MOSFET's on time, which would limit output power and eventually force the MAX25201/MAX25202 into hiccup mode. Estimate the maximum input current using the following equation:

$$I_{SUPMAX} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{SUPMIN}} + 0.5 \times \frac{V_{OUT} - V_{SUPMIN}}{V_{OUT}} \times \frac{V_{SUPMIN}}{f_{SW} \times L}$$

where I_{SUPMAX} is the maximum input current; V_{OUT} and I_{OUT} are the output voltage and current, respectively; η is the estimated efficiency (which is lower at low input voltages due to higher resistive losses); V_{SUPMIN} is the minimum value of the input voltage; f_{SW} is the switching frequency; and L is the minimum value of the chosen inductor.

Multiphase Operation

Dual-Phase (MAX25202)

Dual-phase operation uses a MAX25202M as the master controller and MAX25202S as the slave. Connect these devices as shown in the *Dual-Phase Application Circuit*. In this configuration, the master outputs a clock from SYNCOUT that is 180° out-of-phase for driving the slave FSYNCINS input. When synchronizing to an external clock, connect the clock to FSYNCIN of the master and MODE of the slave. The external clock must have 50% duty-cycle to ensure the 180° phase shift. To use the internal oscillator from the master, drive FSYNCIN of the master and MODE of the slave high (connect to BIAS). Dual-phase solutions allow spread spectrum operation on both the master and slave.

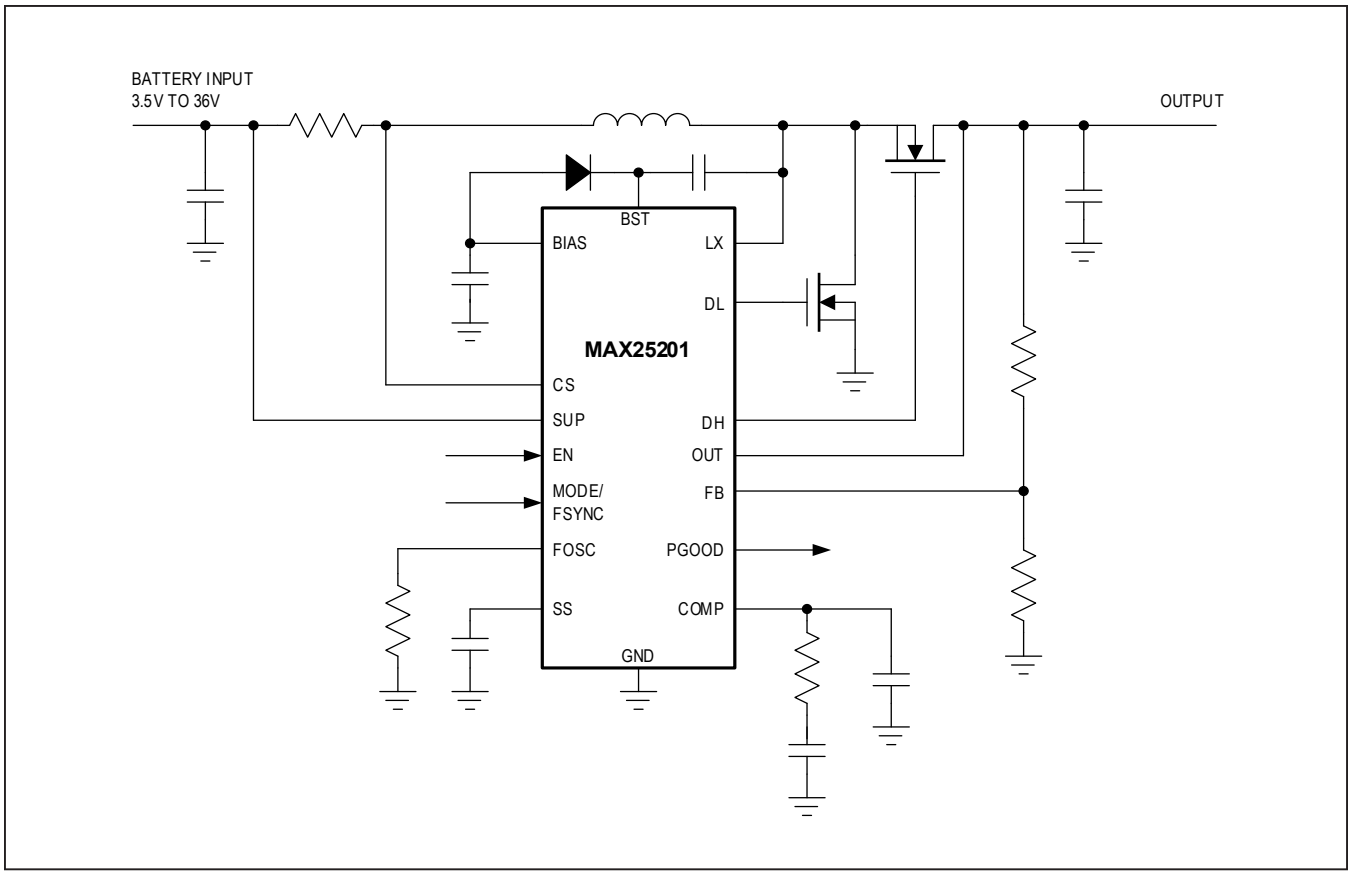
Layout Recommendations

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Layout of the switching power components requires particular attention. Follow these guidelines for good PCB layout:

- Keep high-current paths short, especially at the ground terminals.
- Minimize resistance in high-current paths by keeping the traces short and wide. Using thick (2oz vs. 1oz copper) improves full load efficiency.
- Connect the CS and SUP connections used for current sensing directly across the sense resistor using a Kelvin sense connection.
- Route noisy switching and clock traces away from sensitive analog areas (FB, CS).

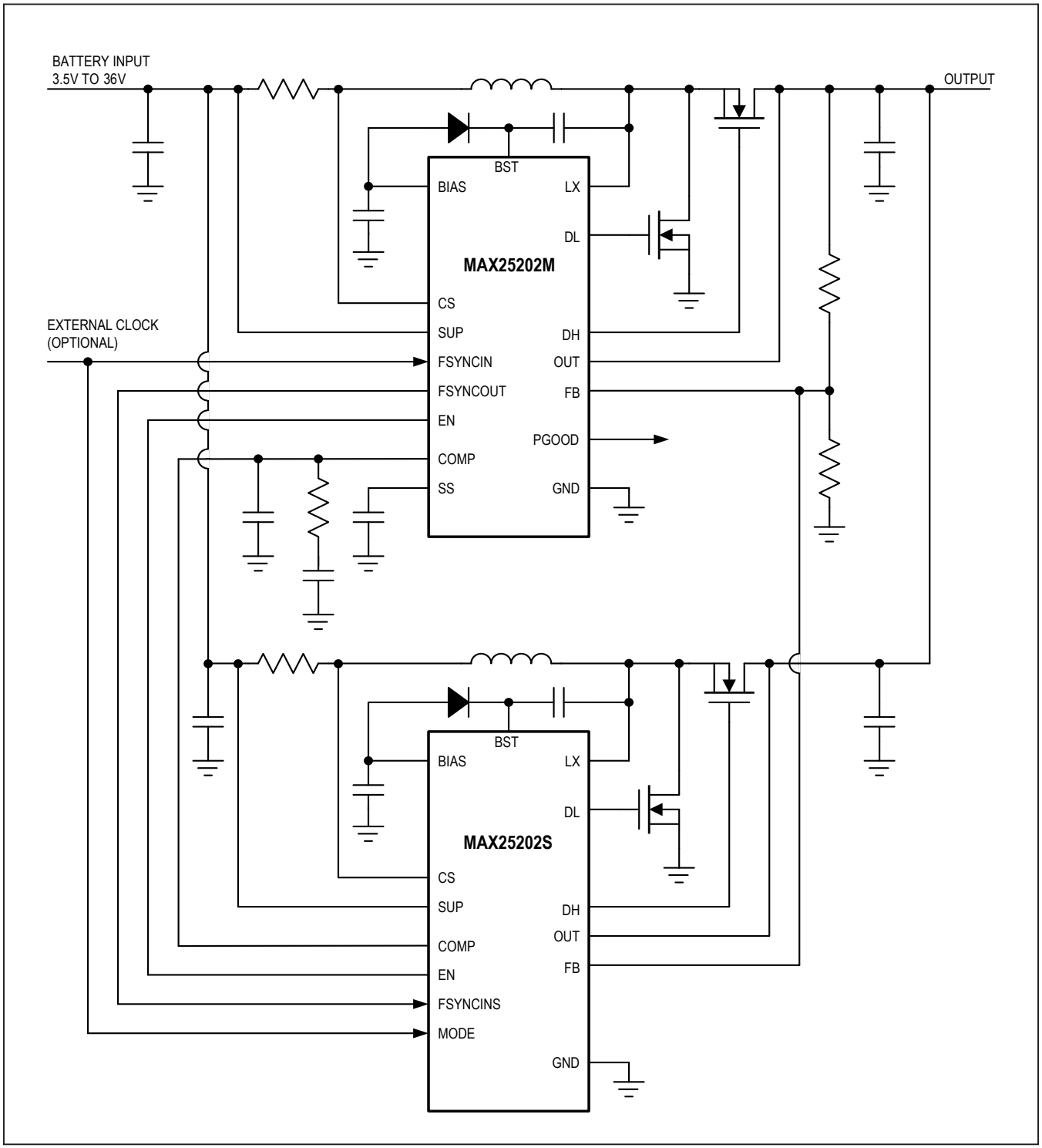
Typical Application Circuits

Synchronous Boost Application Circuit



Typical Application Circuits (continued)

Dual-Phase Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	V_{OUT} RANGE	FIXED V_{OUT}	INTERNAL SWITCHING FREQUENCY	SPREAD SPECTRUM	TOPOLOGY
MAX25201ATEA/VY+	-40°C to +125°C	16 SW TQFN-EP*	3.5V to 36V	10	Adjustable	OFF	SINGLE PHASE
MAX25201ATEB/VY+	-40°C to +125°C	16 SW TQFN-EP*	3.5V to 36V	10	Adjustable	ON	SINGLE PHASE
MAX25201ATEC/VY+	-40°C to +125°C	16 SW TQFN-EP*	20V to 60V	N/A	Adjustable	OFF	SINGLE PHASE
MAX25201ATED/VY+	-40°C to +125°C	16 SW TQFN-EP*	20V to 60V	N/A	Adjustable	ON	SINGLE PHASE
MAX25202MATEA/VY+	-40°C to +125°C	16 SW TQFN-EP*	20V to 60V	N/A	400kHz	ON	2-PHASE MASTER
MAX25202SATEA/VY+	-40°C to +125°C	16 SW TQFN-EP*	20V to 60V	N/A	400kHz	ON	2-PHASE SLAVE

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/19	Initial release	—
1	7/19	Updated *Ordering Information* section	21
2	12/19	Updated *Electrical Chracteristics* table and *Ordering Information*	4. 5, 21
3	2/20	Removed remaining future-product notation in *Ordering Information*	21

