Evaluating the ADAQ7768-1 24-Bit, Single-Channel Precision µModule Data Acquisition System

FEATURES

- Evaluation kit for ADAQ7768-1 24-bit single-channel precision µModule® data acquisition system
- Switch or GPIO controlled gain mode
- Complete power management solution
- FMC connector to FPGA for digital interface
- Optional Arduino and PMOD connector

EVALUATION KIT CONTENTS

- EV-ADAQ7768-1FMC1Z evaluation board

EQUIPMENT NEEDED

- SDP-H1 (EVAL-SDP-CH1Z) system demonstration platform
- DC/AC signal source (audio precision or similar high performance signal source)
- PC running Microsoft Windows 7, 8, or 10 with USB 2.0 port

SOFTWARE NEEDED

- Analysis, control, evaluation (ACE) software
- ADAQ7768-1 ACE plugin

GENERAL DESCRIPTION

The EV-ADAQ7768-1FMC1Z evaluation kit features the ADAQ7768-1, a 24-bit, single-channel precision µModule® data acquisition (DAQ) system. The evaluation board demonstrates the performance of the ADAQ7768-1 µModule and is a versatile tool for a variety of applications.

The EV-ADAQ7768-1FMC1Z board connects to the USB port of the PC through the system demonstration platform (SDP-H1). By default, all the necessary supply rails on the EV-ADAQ7768-1FMC1Z are powered by a 3.3 V rail coming from the SDP-H1. The 3.3 V rail is regulated by the on-board power solution to ±15 V and 5.3 V to power the ADAQ7768-1 and its support components.

The EV-ADAQ7768-1FMC1Z is used alongside a downloadable evaluation software (ACE) that fully configures the ADAQ7768-1 device register functionality, and also provides DC and AC time and frequency domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation. The ACE software controls the EV-ADAQ7768-1FMC1Z over the USB through the system demonstration platform (SDP-H1).

The ADAQ7768-1 data sheet provides a full description and complete specifications of the ADAQ7768-1. Consult it in conjunction with this user guide when using the evaluation board. Full details on the SDP-H1 are available on the SDP-H1 product page.

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REVISION HISTORY

3/2023—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

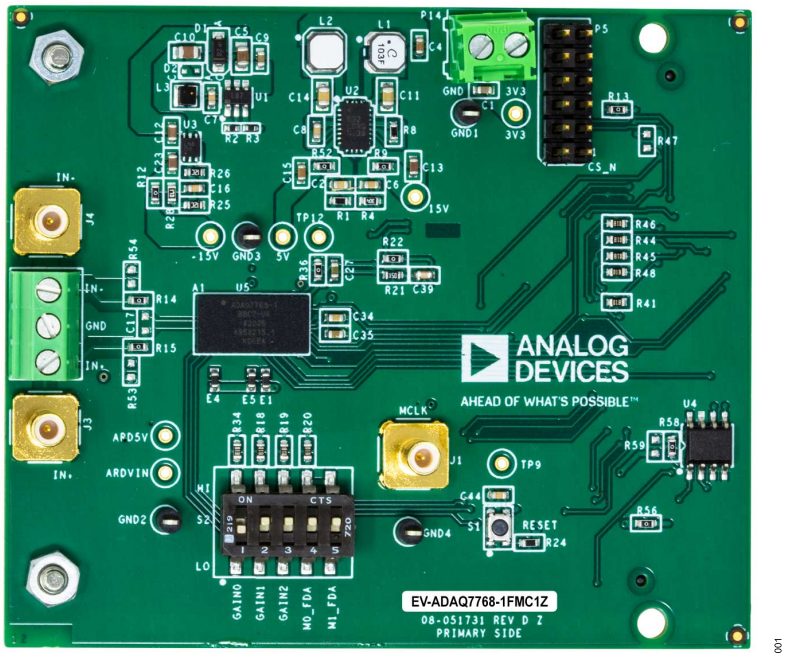

Figure 1. Evaluation Board Photograph

GETTING STARTED

SOFTWARE INSTALLATION PROCEDURES

Before using the EV-ADAQ7768-1FMC1Z, download and install the analysis, control, evaluation (ACE) software from the ACE software page. Download also the ADAQ7768-1 ACE plugin from the plugin manager, or from the EV-ADAQ7768-1FMC1Z product page.

ACE is a desktop software application that evaluates and controls multiple evaluation systems across the Analog Devices product portfolio. The installation process consists of the ACE software installation and SDP-H1 driver installation.

Warning

To ensure the evaluation system is correctly recognized when it is connected to the PC, install the ACE software and SDP-H1 driver first before connecting the EV-ADAQ7768-1FMC1Z and SDP-H1 board to the USB port of the PC.

Installing the ACE Software

Follow these steps to install the ACE software:

1. Download the ACE software to a Windows-based PC.
2. Double-click the **ACEInstall.exe** file to begin the installation. By default, the software is saved at **C:\Program Files (x86)\Analog Devices\ACE**.
3. A dialog box appears seeking permission to allow the program to make changes to the PC. Click **Yes** to begin the installation process.
4. Click **Next >** to continue the installation, as shown in Figure 2.

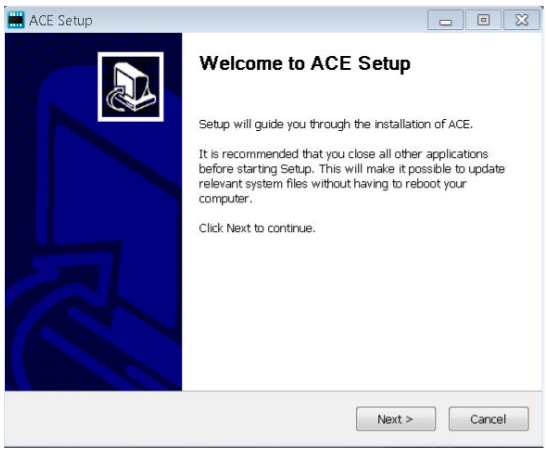

Figure 2. Evaluation Software Install Confirmation

5. Read the software license agreement and click **I Agree** (see Figure 3).

Figure 3. License Agreement

6. Choose an installation location and click **Next** (see Figure 4).

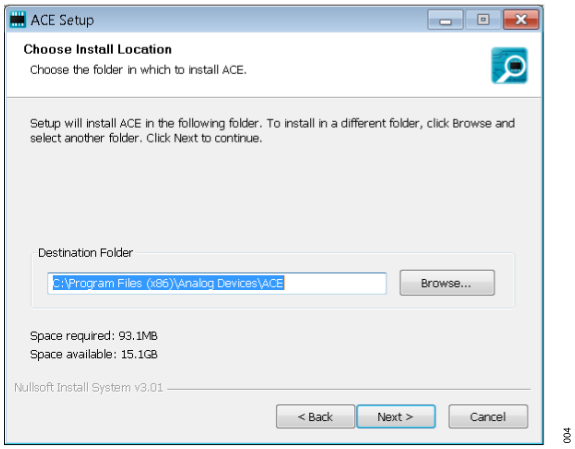

Figure 4. Choose Install Location

7. Select the **Pre-Requisites** checkbox to include the installation of the SDP-H1 driver. Click **Install** (see Figure 5).

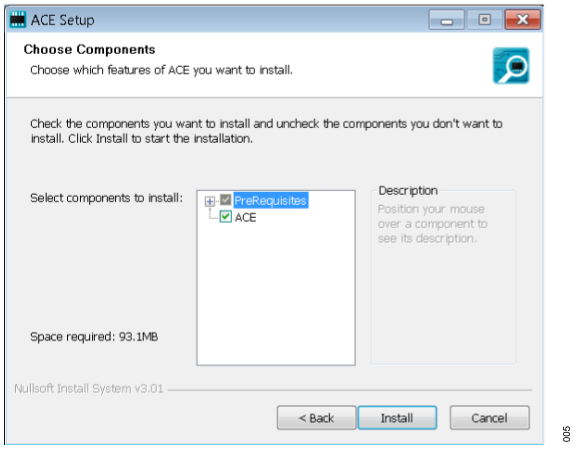

Figure 5. Choose Components

8. The **Windows Security** window appears. Click **Install** (see Figure 6). The installation is in progress. No action is required (see Figure 7).

GETTING STARTED

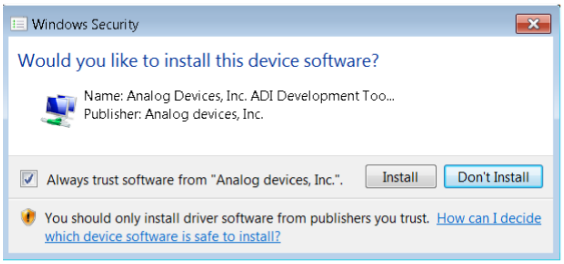

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Figure 6. Windows Security Window

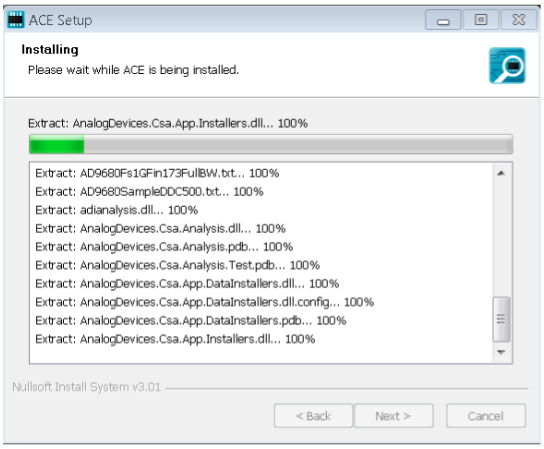

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Figure 7. Installation in Progress

9. The installation is complete (see Figure 8). Click **Next >** and then **Finish** to complete.

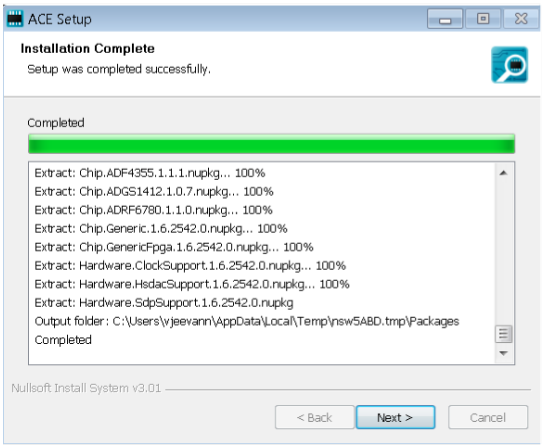

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Figure 8. Installation Complete

EVALUATION BOARD SETUP

The EV-ADAQ7768-1FMC1Z connects to the SDP-H1. The SDP-H1 board serves as the communication link between the PC and EV-ADAQ7768-1FMC1Z. Figure 11 shows the connections between the EV-ADAQ7768-1FMC1Z and SDP-H1 board.

Connecting the EV-ADAQ7768-1FMC1Z and SDP-H1 to a PC

After installing the ACE software, follow these steps to set up the EV-ADAQ7768-1FMC1Z and SDP-H1, as shown in Figure 9.

1. Ensure all configuration links are in the appropriate positions, as detailed in Table 2.
2. Connect the EV-ADAQ7768-1FMC1Z securely to the 160-way connector on the SDP-H1. The EV-ADAQ7768-1FMC1Z does not require an external power supply adapter.
3. Connect the SDP-H1 to the PC through the USB cable and power it up with the 12 V wall adapter included in the SDP-H1 kit.

GETTING STARTED

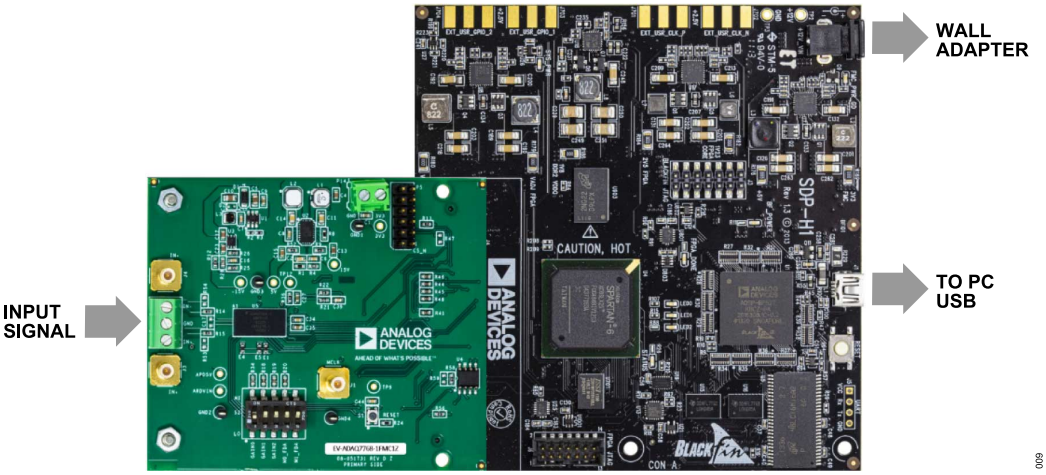

Figure 9. Evaluation Board Connection

Verifying the Board Connection

After completing Software Installation Procedures and Evaluation Board Setup, follow these steps to verify the board connection:

1. Run the **Found New Hardware Wizard** after the SDP-H1 system demonstration platform board is plugged into the PC. If using Windows XP, search for the SDP-H1 drivers. Automatically search for the drivers of the SDP-H1 system demonstration platform board, if prompted by the operating system.
2. Check the evaluation board is connecting to the PC correctly using the **Device Manager** of the PC. Access the **Device Manager** as follows:
   a. Right click **My Computer** and then click **Manage**.
   b. A dialog box appears seeking permission to allow the program to make changes to the computer. Click **Yes**.
   c. The **Computer Management** window appears. Click **Device Manager** from the list of **System Tools** (see Figure 10.
   d. If the SDP-H1 system demonstration platform board appears under **ADI Development Tools**, the driver software is installed and the evaluation board is connecting to the PC correctly.

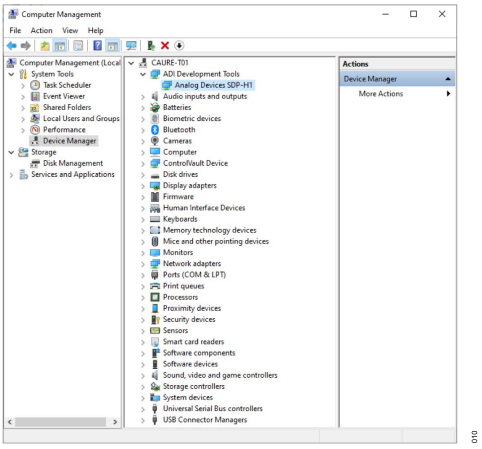

Figure 10. Checking the Evaluation Board is Connected to the PC Correctly

Disconnecting the EV-ADAQ7768-1FMC1Z

Disconnect the EV-ADAQ7768-1FMC1Z from the SDP-H1 by either:

1. Turning off the power from the SDP-H1 by unplugging the 12 V wall adapter.
2. Pressing the reset tact switch located alongside the mini-USB port on the SDP-H1.

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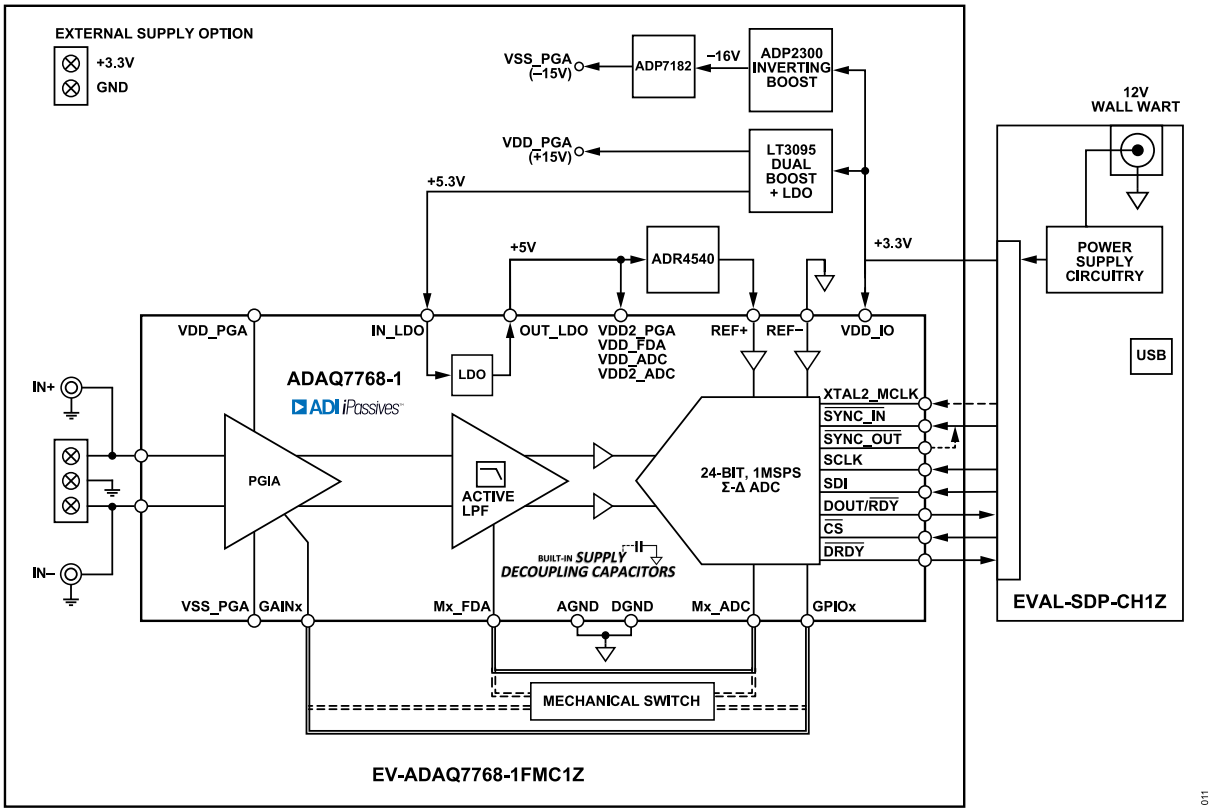

Figure 11. Simplified Evaluation Board Block Diagram

HARDWARE OVERVIEW

Figure 11 shows the simplified evaluation board block diagram of EVAL-ADAQ7768-1FMC1Z connected to the SDP-H1 controller board. The board features ADAQ7768-1 (U5), ADR4540 4.096 V reference (U6), and on-board power solution consisting of the ADP2300 (U1), ADP7182 (U3), and LT3095 (U2). See the Evaluation Board Schematic section for more details.

SDP-H1 CONTROLLER BOARD

The EV-ADAQ7768-1FMC1Z evaluation board uses the serial peripheral interface (SPI) and is connected to the high speed controller board for the system demonstration platform (SDP-H1) controller board. The SDP-H1 board requires power from a 12 V wall adapter. The SDP-H1 has the Xilinx® Spartan 6 and ADSP-BF527 processor with connectivity to the PC through a USB 2.0 high speed port. The controller boards configure and capture data on the daughter boards from the PC through a USB.

The SDP-H1 has an FMC low pin count (LPC) connector with full differential LVDS and singled-ended LVCMOS support. It also features the 160-pin connector, found on the SDP-B, which exposes the Blackfin® processor peripherals. This connector provides a configurable serial, parallel I^2C and SPI, and general-purpose input/output (GPIO) communication lines to the attached daughter board for the functional description of the on-board power supplies.

POWER SUPPLIES

By default, the EV-ADAQ7768-1FMC1Z obtains its power from the 3.3 V rail of the SDP-H1 board. The 3.3 V rail directly supplies VDD_IO power pin of the ADAQ7768-1. At the same time, this rail is boosted and regulated to provide the supply rails required by the ADAQ7768-1, as well as the voltage reference and additional signal conditioning. The terminal block (P14) can also be used as an option to externally supply the evaluation board with 3.3 V in case the user prefers a third-party capture board for evaluation.

The EV-ADAQ7768-1FMC1Z uses LT3095 (U2), a dual-channel integrated boost and a low dropout (LDO) regulator in a single package, for its positive supply rails. The LT3095 generates the +15 V needed by the VDD_PGA power pin and the 5.3 V to supply the built-in LDO of the ADAQ7768-1. This built-in LDO regulator then generates 5 V to the power pins VDD2_PGA, VDD_FDA, VDD_ADC, VDD2_ADC, and ADR4540 voltage reference.

Similarly, the ADP2300 (U1), a step-down regulator, scales down the 3.3 V from the SDP-H1 to -16 V. This -16 V is used by the ADP7182 (U3), a low noise LDO, to regulate the voltage to -15 V, which powers the negative supply rail, VSS_PGA, of the device.

Each supply is decoupled at the point it enters the board and again at the point it connects to each device. The ADAQ7768-1 has built-

EVALUATION BOARD HARDWARE

in 0.1 µF supply decoupling capacitors on VDD_PGA, VSS_PGA, VDD2_PGA, VDD_FDA, VDD_ADC, and VDD2_ADC supply pins. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

Table 1. On-Board Power Supplies

Power Supply (V)	Function
+3.3 V	VDD_IO and EV-ADAQ7768-1FMC1Z main supply rail from the SDP-H1 board.
+5 V	VDD2_PGA, VDD_FDA, VDD_ADC, VDD2_ADC, and ADR4540 supply rails using internal LDO.
+15 V	VDD_PGA supply rail using the LT3095.
–15 V	VSS_PGA supply rail using the ADP7182.

ANALOG INPUTS

Input signals through IN+ and IN− are fed directly to the ADAQ7768-1 either through the subminiature version B (SMB) connectors, J3 and J4, or the screw terminal block P7.

In the default configuration of the board, the inputs float with high impedance. Thus, ensure the signal source is properly biased to a common-mode voltage. See the Input Range Control section for detailed information on input configuration and control.

Measure the true dynamic range of the board by connecting the two inputs to the board's ground reference through the screw terminal by a short piece of wire, as displayed in Figure 12.

It is also recommended to use a low distortion AC source, such as the Audio Precision APx555 series, when evaluating the dynamic performance of the ADAQ7768-1.

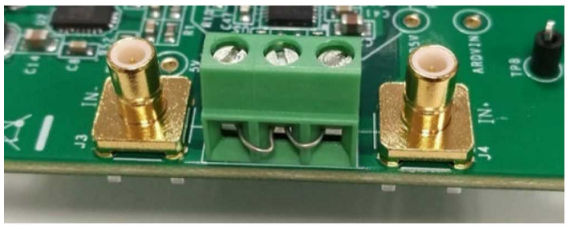

Figure 12. Short the Inputs to Ground with Wire to Measure the Signal Chain Dynamic Range

HARDWARE LINK OPTIONS

Set the multiple link options correctly for the appropriate operating setup before applying the power and signal to the EV-ADAQ7768-1FMC1Z. Table 2 shows the default link positions for the EV-ADAQ7768-1FMC1Z.

Table 2. Default Link and Solder Link Options

Name	Link No.	Default Link Option	Description
Differential/Single Ended Input		DNI	
	R53		R53 set IN+ to ground for single-ended input.
	R54		R54 set IN- to ground for single-ended input.
ADR4540 V_{IN} Select		R23	Set the source for the voltage input for ADR4540.
	R23		R23 set ADR4540 voltage input to the output of the LDO.
	R60		R60 set ADR4540 voltage input to 5.3V.
FDA Power Mode Input		DNI	Set the power mode selection to auto or manual selection.
	R10		R10 set the M1_FDA power mode input to manual selection.
	R11		R11 set the M0_FDA power mode input to manual selection.
S2			Set the GPIO mode and FDA power mode.
	1A-1B		1A-1B set the GPIO0 to high or low.
	2A-2B		2A-2B set the GPIO1 to high or low.
	3A-3B		3A-3B set the GPIO2 to high or low.
	4A-4B		4A-4B set the M1_FDA power mode to low-power/high-power mode
	5A-5B		5A-5B set the M0_FDA power mode to low-power/high-power mode

On-Board Connectors

Table 3 provides information about the EV-ADAQ7768-1FMC1Z external on-board connectors.

Table 3. On-Board Connectors

Connector	Function
P1	FMC connector to interface all digital signals to the SDP-H1 board.
P2/P3	Arduino header pads, not installed by default.
P5	PMOD connector allows interface with the board.

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Table 3. On-Board Connectors (Continued)

Connector	Function
P14	Terminal block connector for external 3.3 V supply.
J3/J4/P7	SMB and terminal block connector for analog inputs, IN+ and IN–.
S1	ADC reset switch
S2	Mechanical switch for PGIA Gain and FDA power mode control.
J1	SMB connector for the external MCLK.

EVALUATION BOARD SOFTWARE

LAUNCHING THE SOFTWARE

Follow these steps to launch the ACE software:

1. From the **Start** menu, select **All Programs** > **Analog Devices > ACE > ACE.exe** to open the main window shown in Figure 13.
2. The EV-ADAQ7768-1FMC1Z icon appears in the **Attached Hardware** section.
3. If the EV-ADAQ7768-1FMC1Z is not connected to the USB port through the SDP-H1 board when the software is launched, the EV-ADAQ7768-1FMC1Z board icon does not appear in the **Attached Hardware** section. Connect the EV-ADAQ7768-1FMC1Z and SDP-H1 board to the USB port of the PC and wait a few seconds. Then continue following these instructions.
4. Double-click the EV-ADAQ7768-1FMC1Z board icon to open the window shown in Figure 14.
5. Click **Software Defaults** and then **Apply Changes**.
6. Click **Proceed to Analysis** to open the EV-ADAQ7768-1FMC1Z analysis shown in Figure 16

START-UP SEQUENCE

After running the software, the following events occur:

1. The software accesses the EEPROM on the main evaluation board, which contains the board ID.
2. Once the EEPROM value is verified, the PC loads the corresponding firmware to the FPGA on the SDP-H1.
3. After the loading of the firmware, the SDP-H1 supplies the 3.3 V to the main evaluation board and establishes communication with the ADAQ7768-1.
4. The software then loads a preset of register values to the user register map of the ADAQ7768-1 to configure it to the tool's default operating mode.

DESCRIPTION OF THE ANALYSIS WINDOW

Click **Proceed to Analysis** in the chip view window to open the window shown in Figure 15. The **Analysis** view window showcases the performance of the EV-ADAQ7768-1FMC1Z. Before performing any measurements, set the Capture Settings and Analysis.

The **Analysis** view window contains the **Waveform** (Figure 17), **Histogram** (Figure 18), and **FFT** tabs (Figure 19).

Capture Settings

The **General Capture Settings** configures the sample count and the output data rate (ODR). These settings reflect in the registers automatically before data capture.

The **Sample Count** selects the number of samples per capture. The default value is set at 8192 samples, which can also be changed to the selection of the dropdown list, ranging from 512 to 131072 samples.

The **ODR (Output Data Rate)** is automatically calculated by the software based on the selected ADC filter settings. By default, this is set to 256 kSPS.

Click **Run Once** in the **Capture Settings** section to start a data capture of the samples at the sample rate specified in the **Sample Count** dropdown list. These samples are stored on the FPGA device and are only transferred to the PC when the sample frame is complete.

Click **Run Continuously** in the **Capture Settings** section to start a data capture that gathers samples continuously with one batch of data at a time. This runs the **Run Once** operation continuously.

Analysis

The **General Settings** section sets up the preferred configuration of the fast fourier transform (FFT) analysis. This configuration sets the number of tones to analyze and the fundamental strategy to use.

The **Windowing** section sets up the preferred windowing type to use in the FFT analysis. It also configures the other parameters to include in the analysis (i.e., number of harmonics, fundamental bins, harmonic bins, DC bins, and worst other bins).

The **Single Tone Analysis** and **Two-Tone Analysis** sections set up the fundamental frequencies included in the FFT analysis. When one frequency is analyzed, use the **Single Tone Analysis** section. When two frequencies are analyzed, use the **Two-Tone Analysis** section.

Results

Click **Export** to export the captured data. The waveform, histogram, and FFT data are stored in .xml files along with the values of the parameters at capture.

Waveform Tab

The **Waveform** tab displays data as time vs. discrete values with the results, as shown in Figure 17.

The data waveform graph shows each successive sample of the µModule output. Zoom in on and pan over the waveform graph using the embedded waveform tools above the graph.

Click the display unit's dropdown (shown with the **Codes** option selected in Figure 17) to select if the data graph displays in units of hexadecimal, volts, or codes. The axis controls are dynamic.

When selecting either the y-scale or x-scale dynamic, the corresponding axis width automatically adjusts to show the entire range of the µModule results after each batch of samples.

Histogram Tab

The **Histogram** tab contains the histogram graph, together with the capture results related to the DC performance (Figure 18).

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The histogram graph displays the number of hits per code within the sampled data. This graph is useful for DC analysis and indicates the noise performance of the device.

FFT Tab

The **FFT** results display fast fourier transform (FFT) information of the last batch of samples gathered, as shown in Figure 19.

The **Signal** section displays the fundamental frequency and fundamental power. The **Noise** section displays the signal-to-noise ratio (SNR) and other noise performance results.

The **Distortion** section displays the harmonic content of the sampled signal, and the **DC** section displays the DC Power when viewing the FFT analysis.

EXITING THE SOFTWARE

To exit the software, click the file icon on the upper right tab, and then click **Exit**.

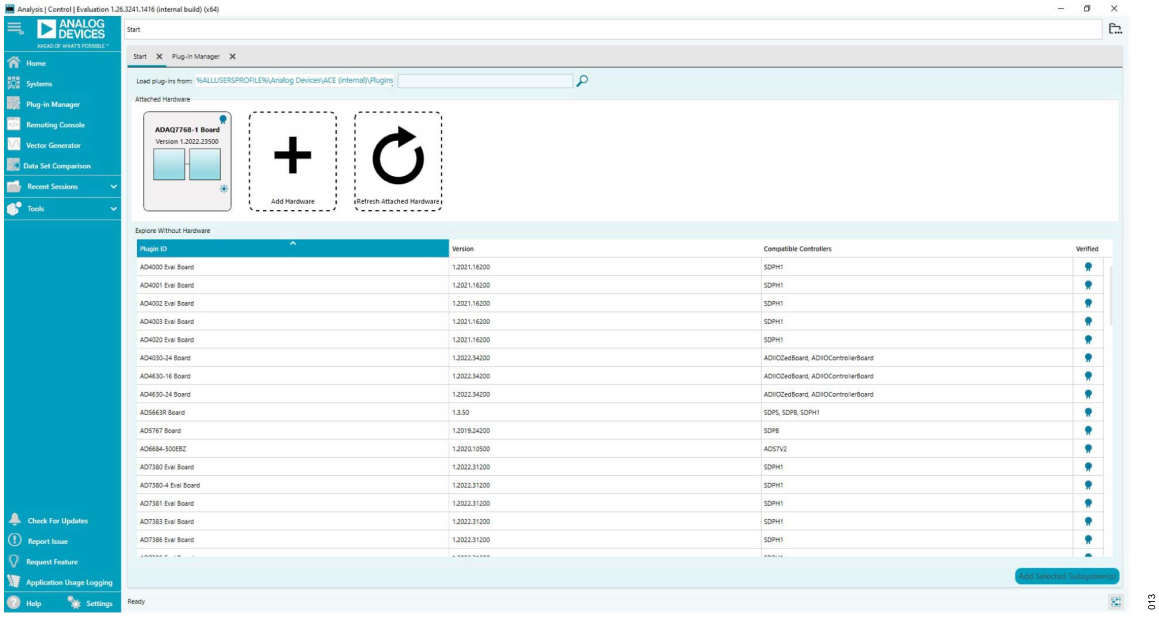

Figure 13. EV-ADAQ7768-1FMC1Z ACE Software Main Window

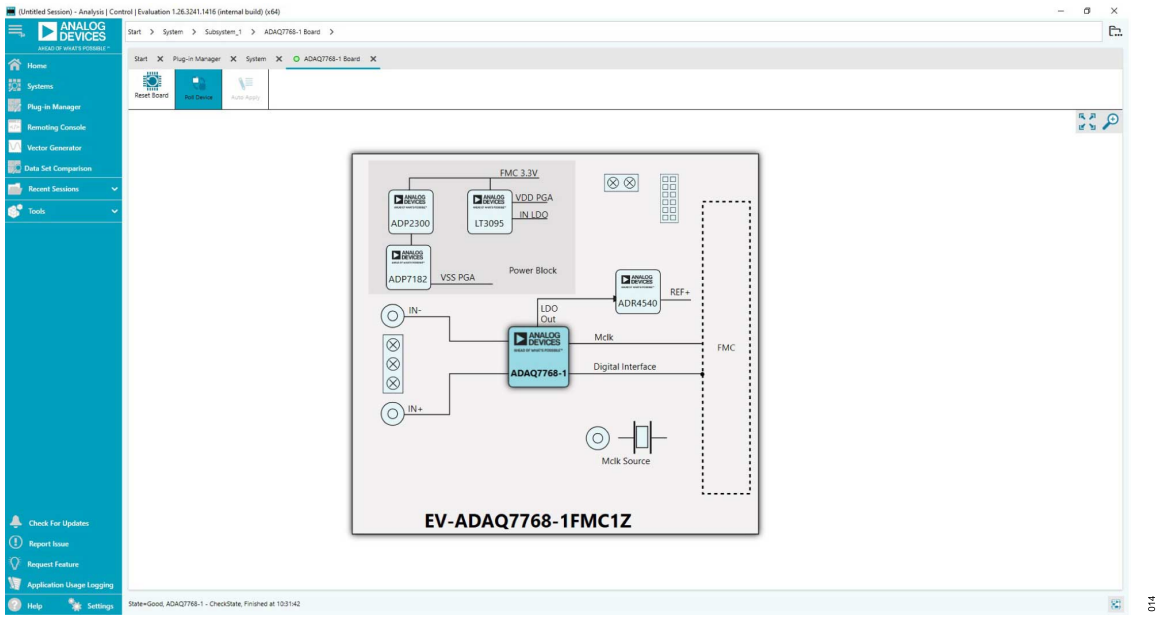

Figure 14. EV-ADAQ7768-1FMC1Z Board View

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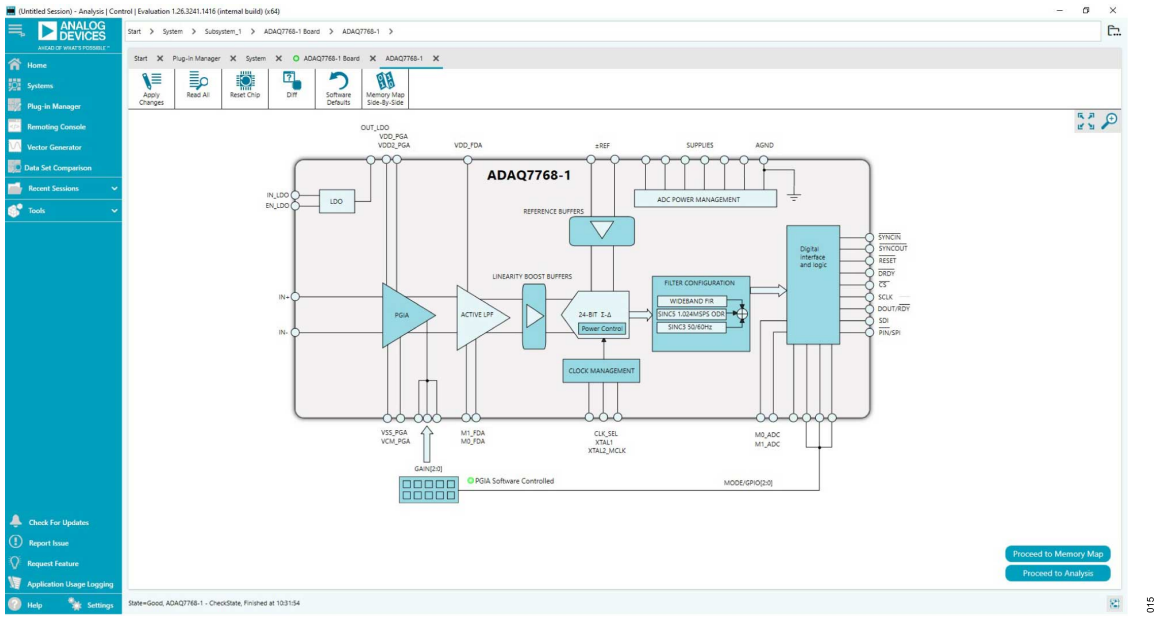

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Figure 15. EV-ADAQ7768-1FMC1Z Chip View

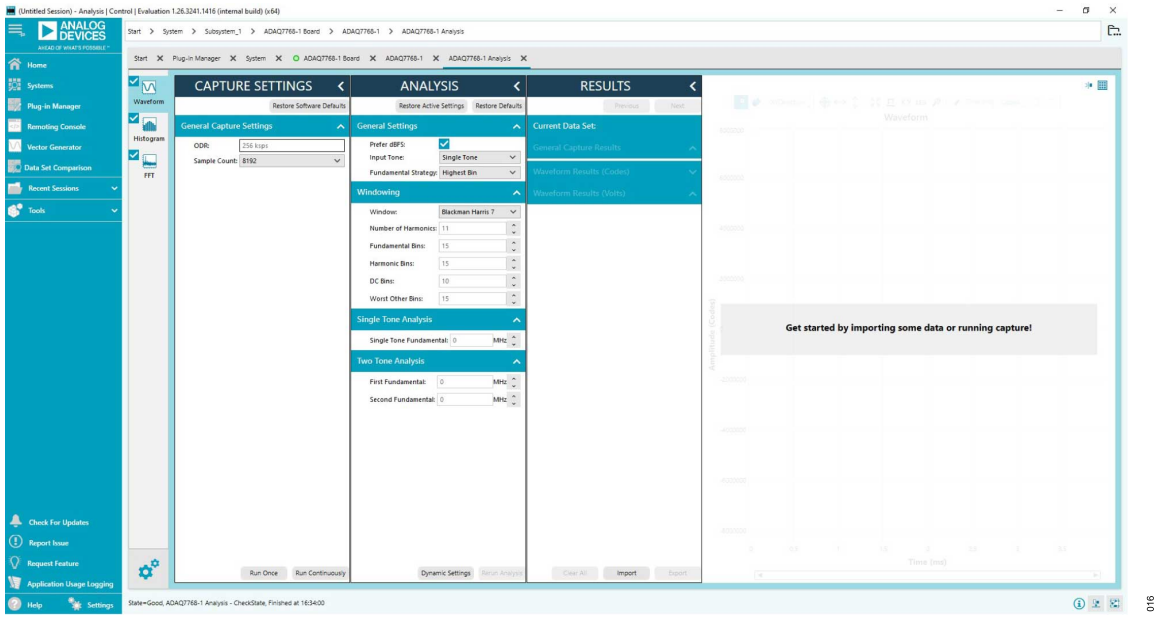

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Figure 16. EV-ADAQ7768-1FMC1Z Analysis View

EVALUATION BOARD SOFTWARE

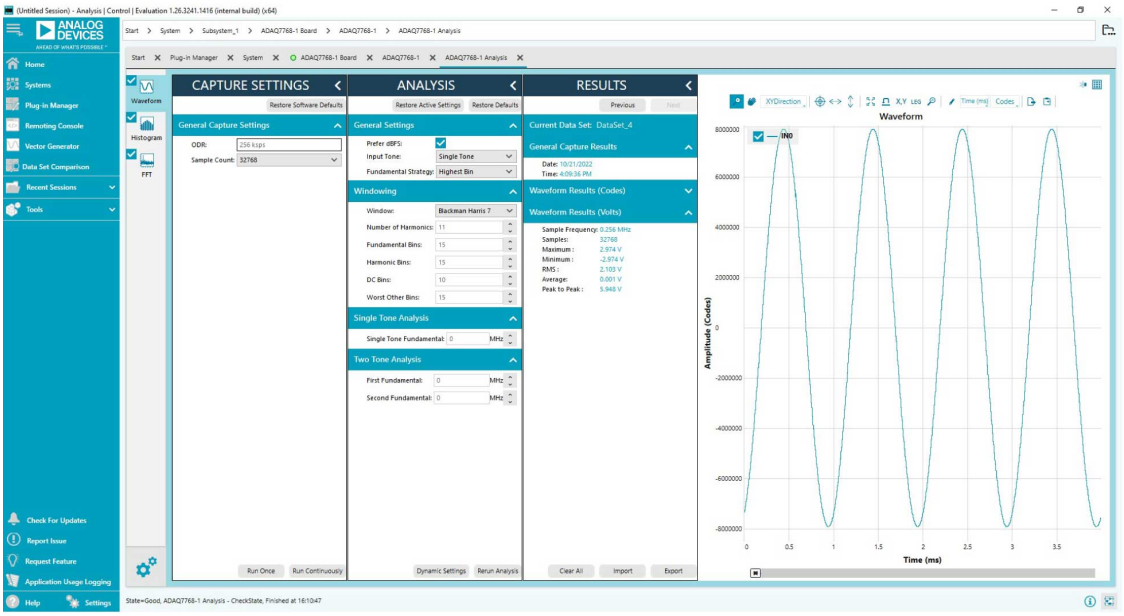

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Figure 17. EV-ADAQ7768-1FMC1Z Waveform

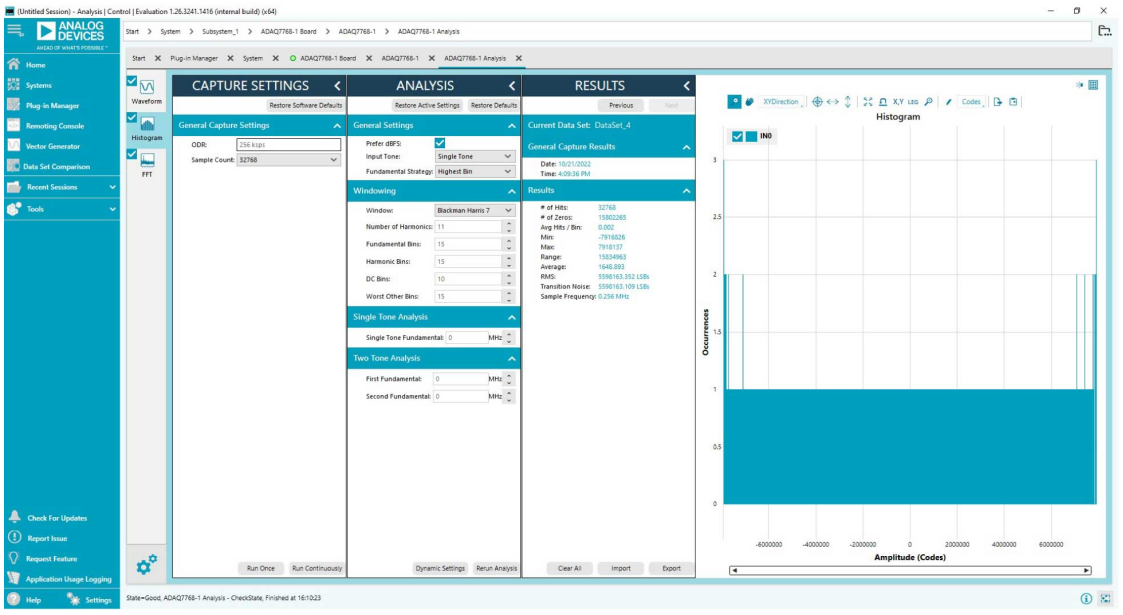

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Figure 18. EV-ADAQ7768-1FMC1Z Histogram

EVALUATION BOARD SOFTWARE

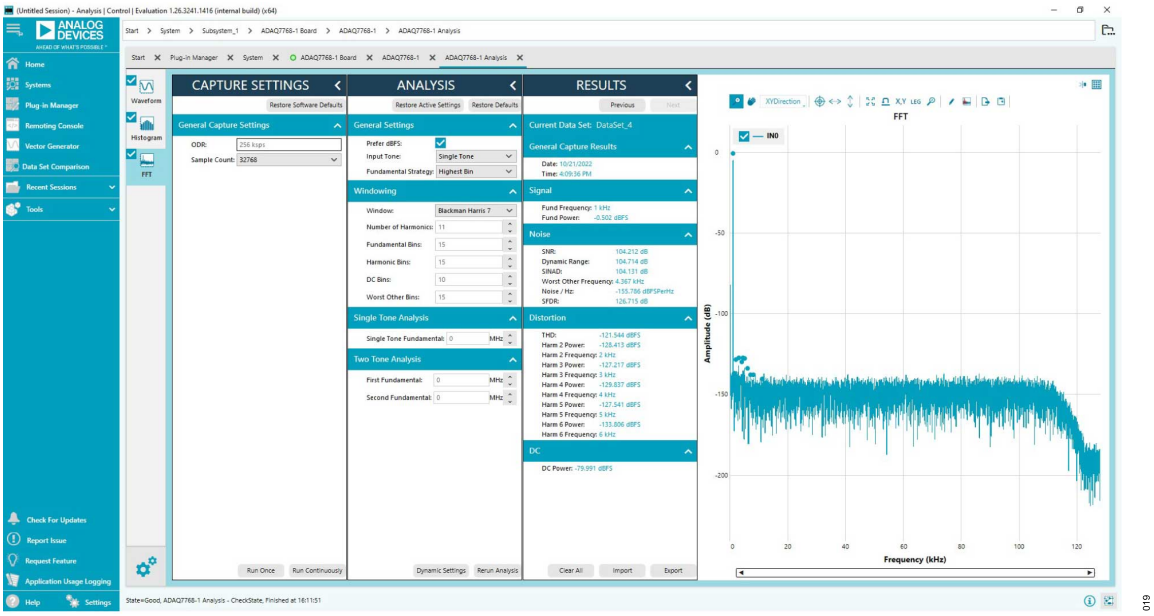


Figure 19. EV-ADAQ7768-1FMC1Z FFT

CONFIGURING THE BOARD AND THE ADAQ7768-1

INPUT RANGE CONTROL

There are two ways to control the ADAQ7768-1 input range.

1. Through the GPIO of ADAQ7768-1, controlled over the SPI.
   - By default, the ACE software uses the GPIO to control the input range. Configure the programmable-gain instrumentation amplifier (PGIA) gain by clicking the PGIA icon in the **Chip View** of the ACE software to select the input ranges. Once done, click **Apply Changes** in the upper left corner for the PGIA gain to take effect (Figure 20).
   - Set S2 switches to low to properly control the device input range using the GPIO.
2. Through the on-board mechanical switch, S2.
   - For this to work, check the **Control PGIA with switch** in the PGIA gain section. Then, click the **Apply Changes** for this to take effect, as shown in Figure 21 (with **PGIA Software Controlled** indicator turned off).
   - See Table 5 for the proper switch settings. Note that when choosing the manual input range control option, adjust the **PGIA Gain Value** in the ACE software accordingly (Figure 20) for it to display the correct measurement result.

Table 4. Configuration Switch (S2) Functions

Name	Description
GAIN0, GAIN1, GAIN2 (labeled A0, A1, A2 on the Revision A board)	Gain mode/input range control for the ADAQ7768-1. See Table 5 for more details. Set to low for GPIO input control mode.
M0_FDA	Reserved. Default low.
M1_FDA	Reserved. Default low.

Table 5. PGIA Mode Settings

Gain Mode Setting	Differential Input Ranges (V)	GAIN2 Pin Logic	GAIN1 Pin Logic	GAIN0 Pin Logic
	Shutdown	High	High	High
Gain 0	±12.603	High	High	Low
Gain 1	±6.302	High	Low	High
Gain 2	±3.151	High	Low	Low
Gain 3	±1.575	Low	High	High
Gain 4	±0.788	Low	High	Low
Gain 5	±0.394	Low	Low	High
Gain 6	±0.197	Low	Low	Low

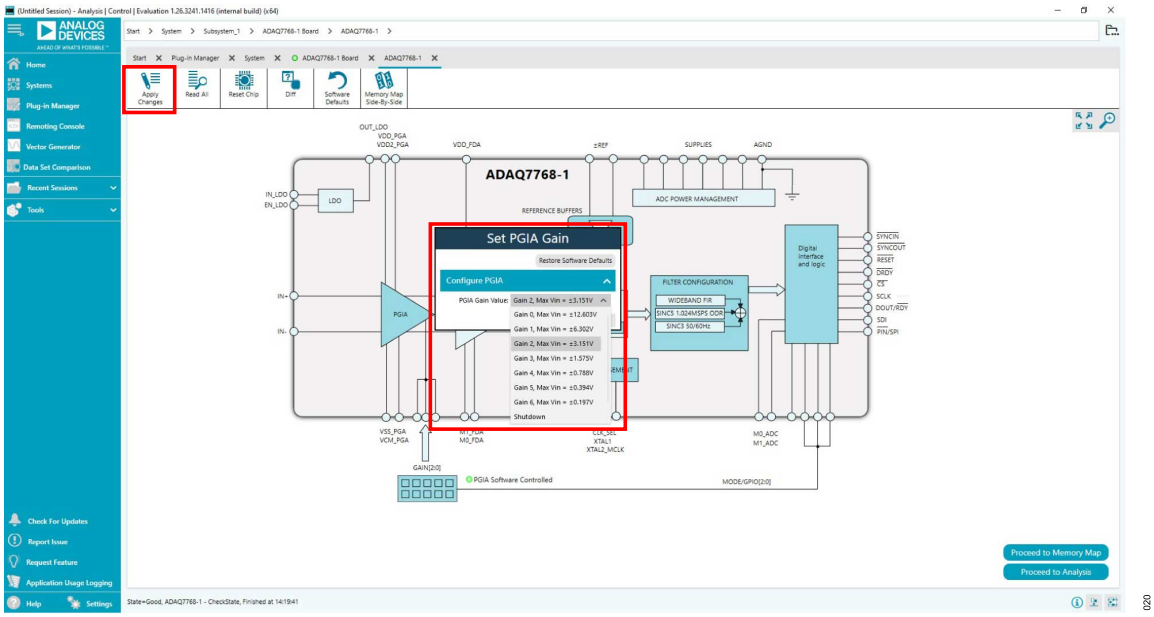


Figure 20. Input Range Selection Menu

CONFIGURING THE BOARD AND THE ADAQ7768-1

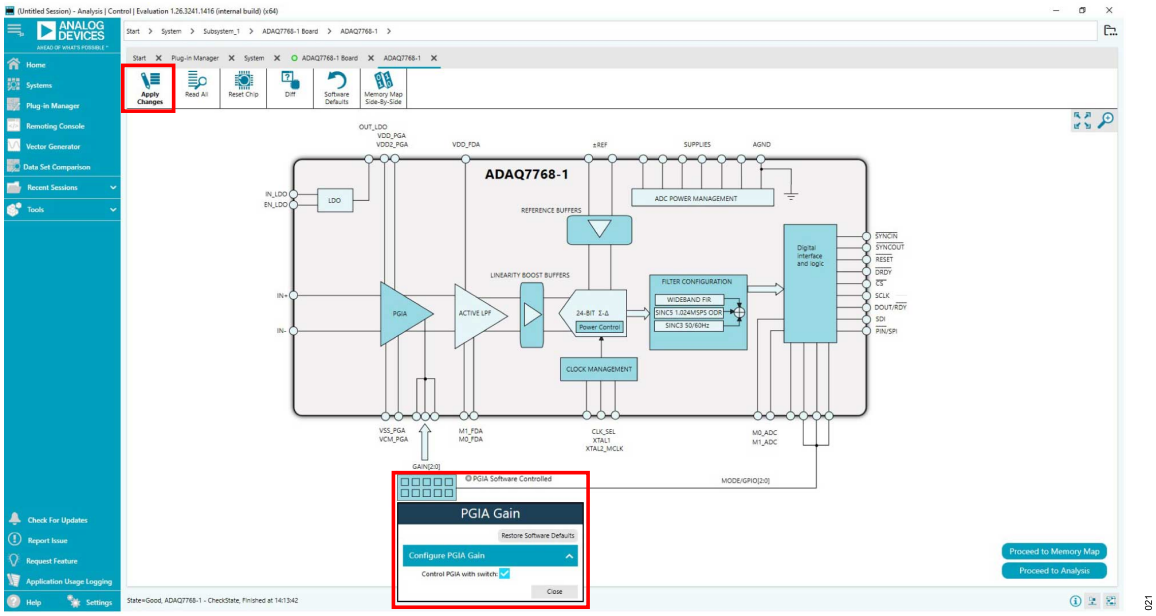


Figure 21. Input Range Through Mechanical Switch (S2)

DATA CAPTURE

The ADAQ7768-1 has excellent performance in both AC and DC measurement. The digital filter inside the ADAQ7768-1 can be programmed with a wide range of decimation ratios to achieve input bandwidth from a few Hertz to a maximum of 204 kHz. The succeeding subsections demonstrate examples of data captures using AC and DC signals.

AC Measurement

By default, the software configures the ADAQ7768-1 to perform wide bandwidth measurement with the wideband low ripple digital filter (brick wall) of 110 kHz of -3 dB bandwidth, with ODR = 256 kSPS. In this mode, the wide band dynamic range (noise), as well as other AC parameters such as signal-to-noise ratio (SNR), total harmonic distortion (THD), spurious free dynamic range (SFDR), etc. are evaluated. Perform the following steps for AC measurement:

1. Modify the PGIA gain according to the desired analog input signal range. Click **Apply Changes** for this to take effect.
2. Apply the analog signal to the input (IN+ and IN–) connectors of the evaluation board.
3. Click **Proceed to Analysis > Run Once** in the **Chip View** of the software. ACE captures 8192 samples by default. Vary the sample count by choosing from the dropdown.
4. The sampled data is now present in the data capture tabs (waveform, histogram, and FFT tabs). Change among each of these tabs to view the results. Figure 22 shows an FFT plot for a typical AC measurement.

Also test the device's anti-aliasing performance by sweeping an out-of-band signal to the input across frequency.

CONFIGURING THE BOARD AND THE ADAQ7768-1

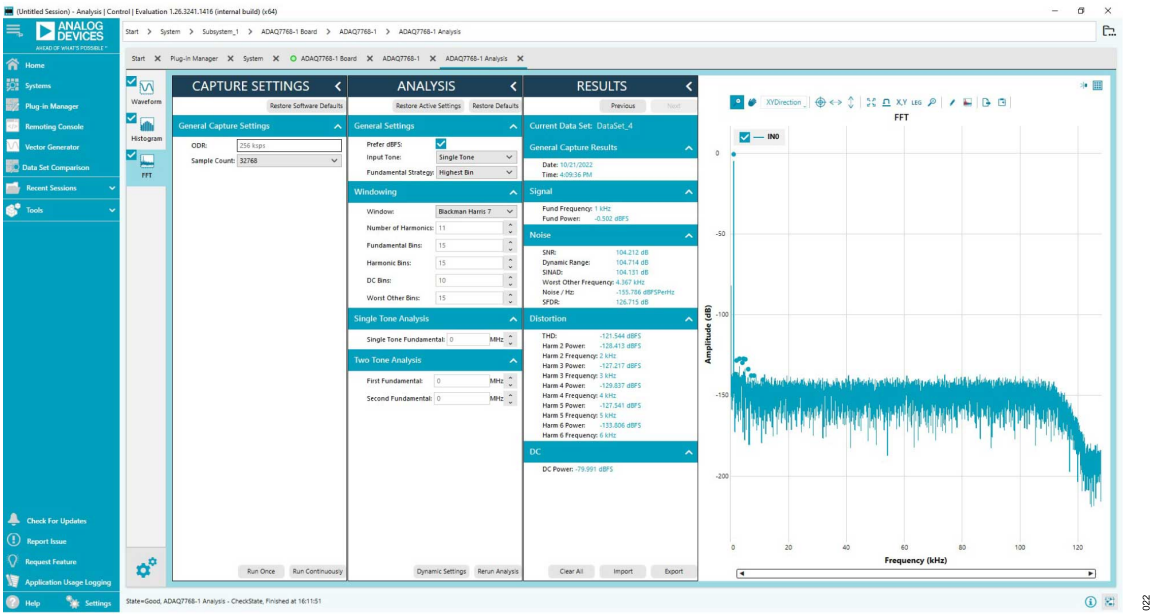


Figure 22. FFT Plot for a Typical AC Measurement, with AFE_GAIN = 1.3 V/V (Gain 2 Mode), Differential Input of 2.98 Vp (-0.5 dBFS) 1 kHz, ODR = 256 kSPS, 32768 Samples

DC Measurement

A sinc3 filter with ODR = 50 SPS is an optimum point to measure a pure DC signal. The sinc notch appears at 50 Hz and can be used to reject the 50 Hz line frequency. Follow these steps to set up the ADAQ7768-1 for a 50 SPS sinc3 filter:

1. Short the inputs (IN+ and IN–) to ground (GND) to measure the RMS noise.
2. In the **Chip View** of the ACE software, click **Filter Configuration**. Use the dropdown to select **Sinc3** (programmable decimation rate), as shown in Figure 23.
3. Configure the Ssinc3 decimation rate by typing '13FF' in the text box near the lower right corner, as shown in Figure 24. This is also reflected in the registers SINC3_DEC_RATE_LSB and SINC3_DEC_ RATE_MSB located in the memory map of the ACE software (Figure 25). Then, click **Apply Changes** for this to take effect.
4. Before clicking on **Run Once**, make sure to adjust the number of samples to collect accordingly. Collecting the default 8192 samples at 50 SPS takes 8192 × 1/50/60 = 2.73 minutes! Start with 1024 samples, which should take about 20 seconds. Generate a new capture using 1024 samples, as shown in Figure 26.
5. The same condition (sinc3 50 SPS) is used to measure low frequency noise, as specified in the data sheet. In the histogram tab, noise is displayed as transition noise in LSB. To compare it with the data sheet's referred to input (RTI) low frequency noise in µV RMS, apply the formula:

$$\begin{aligned} RTI\ \ Noise &= Transition\ \ Noise \times 1\ \ LSB \\ &= Transition\ \ Noise \times \frac{4.096}{2^{24-1} \times AFE\_GAIN} \\ &= Transition\ \ Noise \times \frac{488\ \ nV}{AFE\_GAIN} \end{aligned} \quad (1)$$

6. For example, using Gain6 mode (AFE_GAIN = 20.8 V/V) with measured transition noise = 12.077 LSB = 0.284 µV RMS RTI.

CONFIGURING THE BOARD AND THE ADAQ7768-1

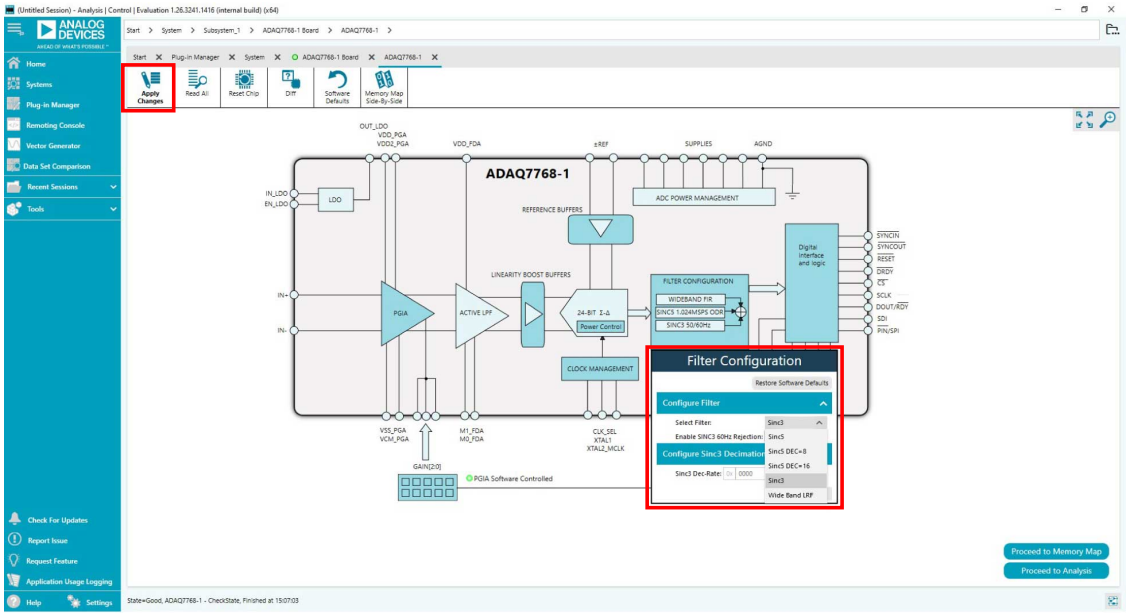


Figure 23. Set the Digital Filter Type

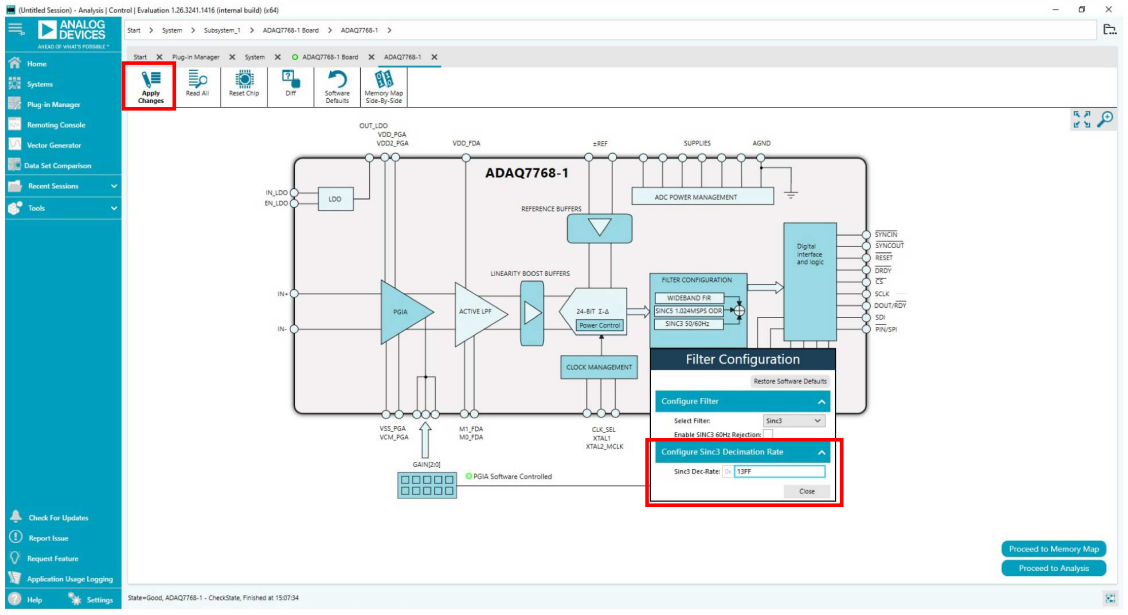


Figure 24. Set the Sinc3 Filter Decimation Ratio

CONFIGURING THE BOARD AND THE ADAQ7768-1

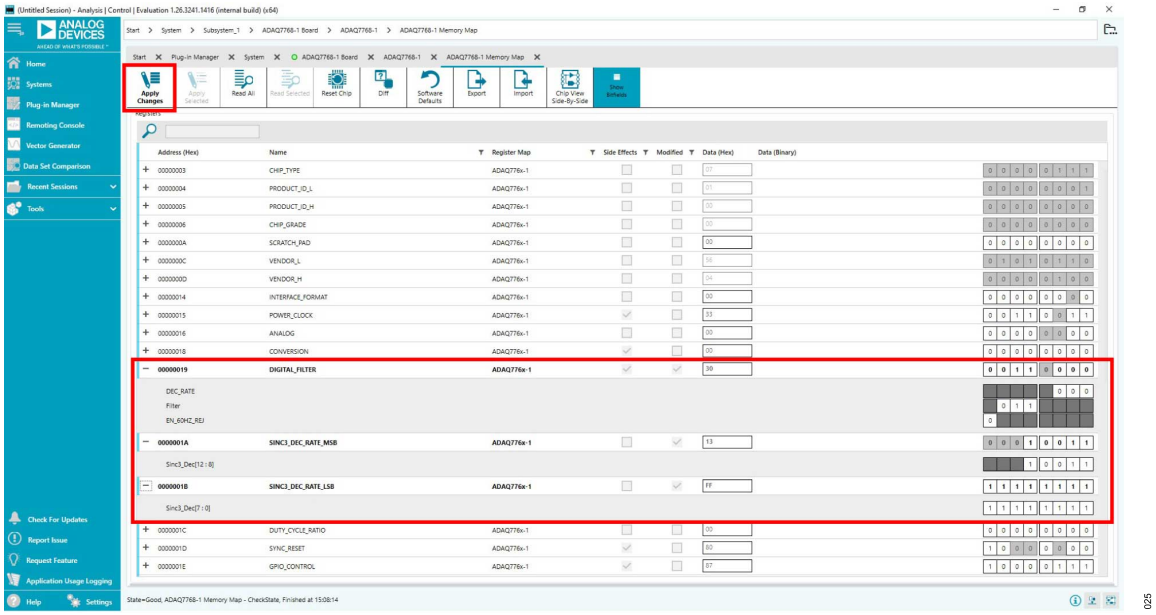


Figure 25. Sinc3 Filter Decimation Ratio Using Memory Map View

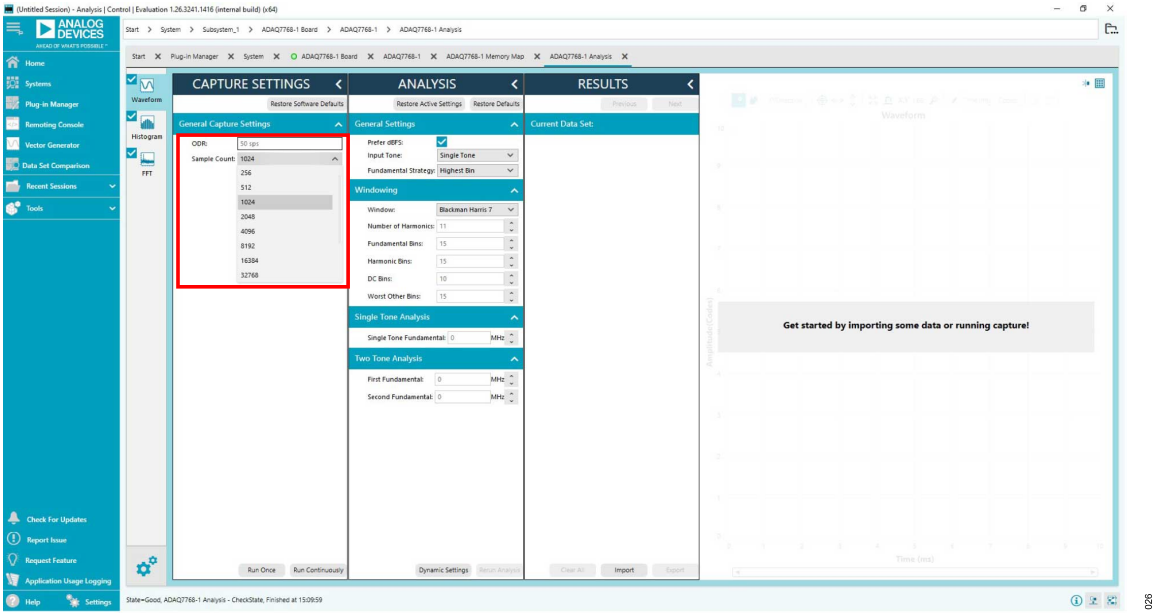
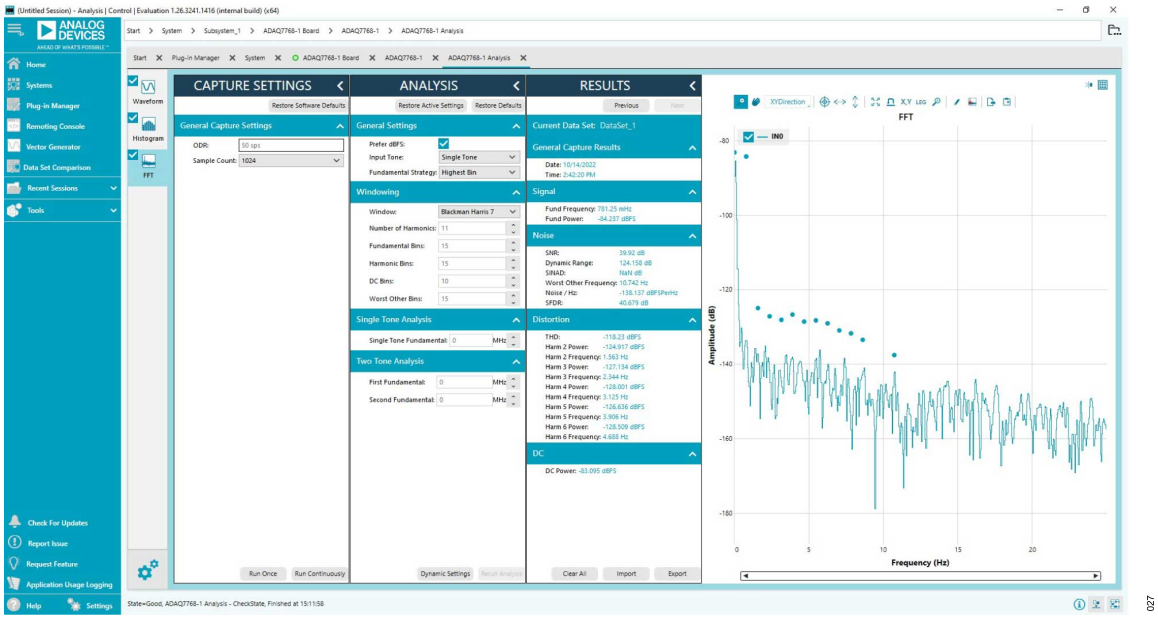


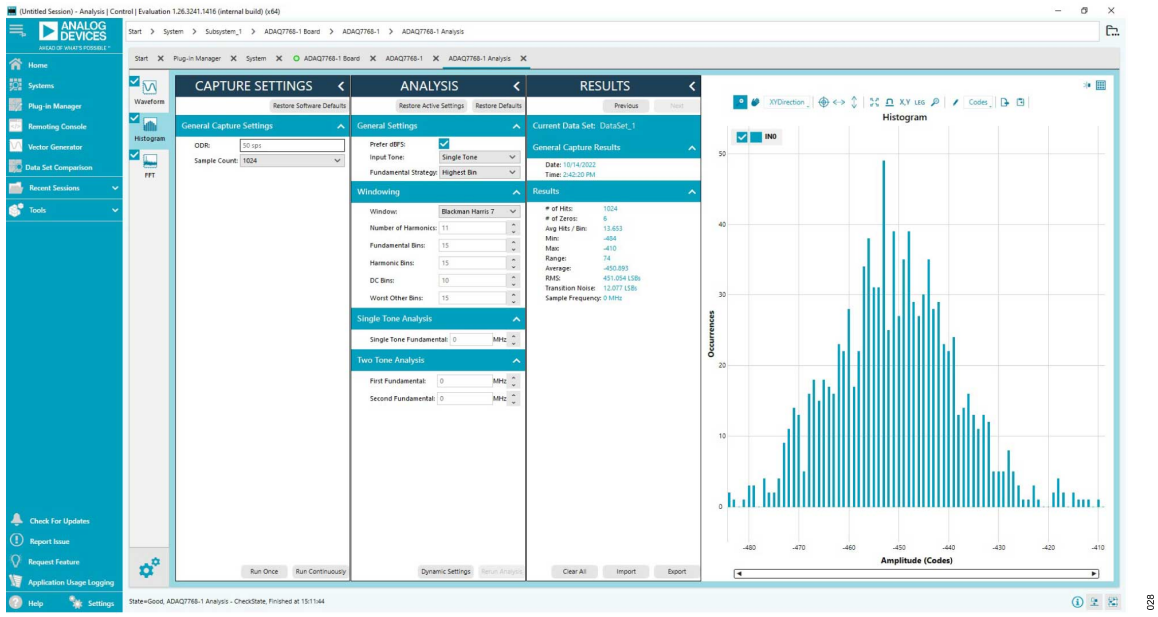
Figure 26. Change the Number of Samples to Collect Per Sample Run

CONFIGURING THE BOARD AND THE ADAQ7768-1



027

Figure 27. FFT Plot for a Typical DC Measurement, with AFE_GAIN = 20.8 V/V (Gain 6 Mode), Inputs Shorted, ODR = 50 SPS, 1024 Samples



028

Figure 28. Histogram of Output Codes, with AFE_GAIN = 20.8 V/V (Gain 6 Mode), Inputs Shorted, ODR = 50 SPS, 1024 Samples

Calculating the SINC3_DEC_RATE Value

By default, this board provides the ADAQ7768-1 with an MCLK of approximately 16.384 MHz. To achieve an ODR of 50 SPS using the sinc3 filter, use the following equation:

$$ODR = \frac{MCLK}{MCLK\_DIV \times DEC\_RATE} \quad (2)$$

Determine the DEC_RATE, assuming the ADAQ7768-1 is using MCLK_DIV = 2:

$$DEC\_RATE = \frac{MCLK}{MCLK\_DIV \times ODR} = 163,840 \quad (3)$$

The sinc3 decimation rate registers, namely, SINC3_DEC_RATE_MSB (0x1A) and SINC3_DEC_RATE_LSB (0x1B), increment the value in the registers by one and then multiply it by 32 to give the actual decimation rate. To set the decimation rate to 163,840, simply follow the equation:

$$Value = \frac{DEC\_RATE}{32} - 1 = 5119$$

CONFIGURING THE BOARD AND THE ADAQ7768-1

Write the equivalent hexadecimal value of 5119 to sinc3 decimation registers. Refer to the ADAQ7768-1 data sheet for more information on the register configuration.

RESET SWITCHES

Press S1 to reset the ADAQ7768-1. Resetting the ADAQ7768-1 resets all the register settings to default values.

A reset switch is also available on the SDP-H1 to reset the interface board. Resetting the digital interface board results in losing communication with the ADAQ7768-1.

Restart the software tool to reinitialize the board.

EVALUATION BOARD SCHEMATIC

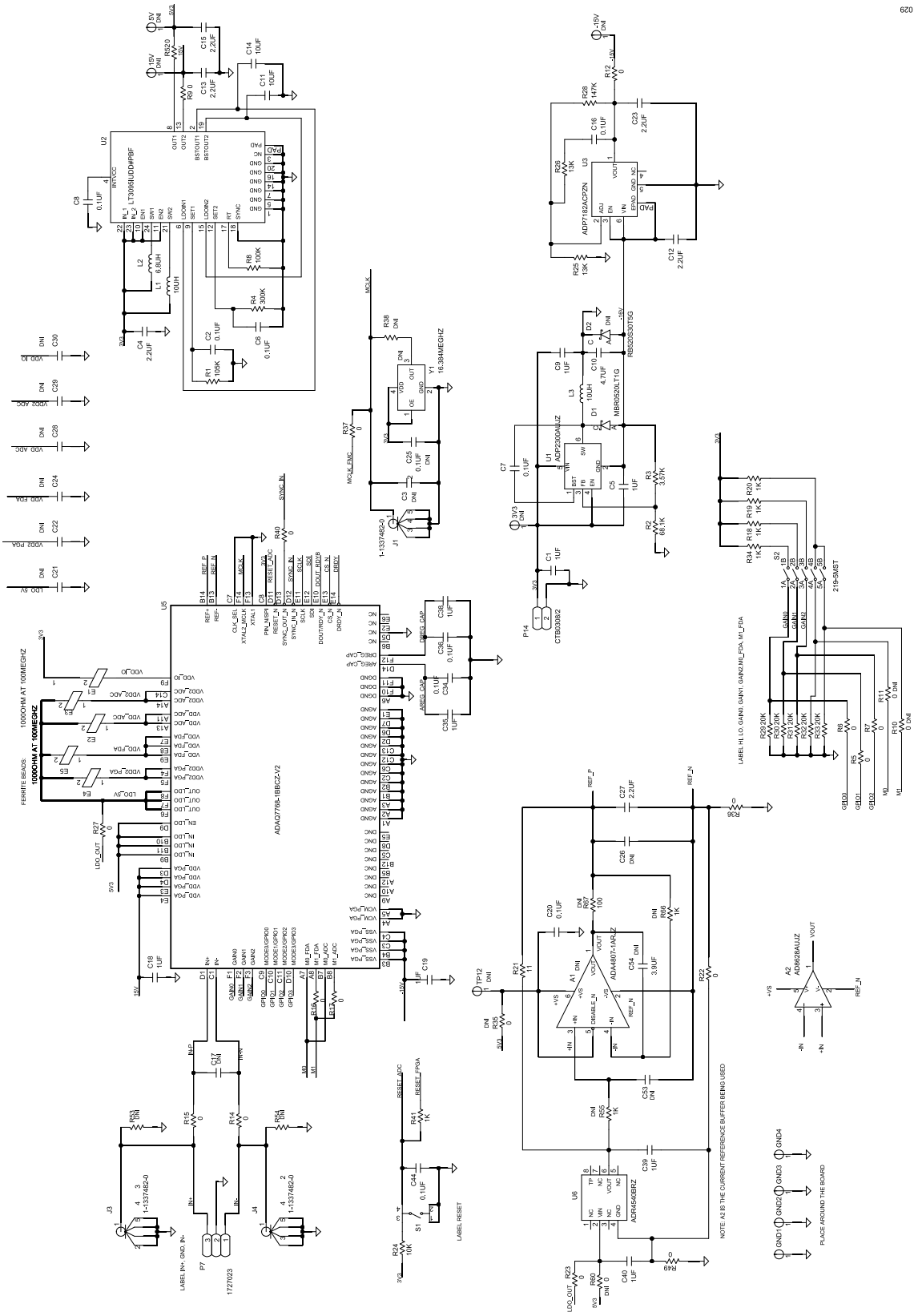


Figure 29. Evaluation Board Schematic 1

EVALUATION BOARD SCHEMATIC

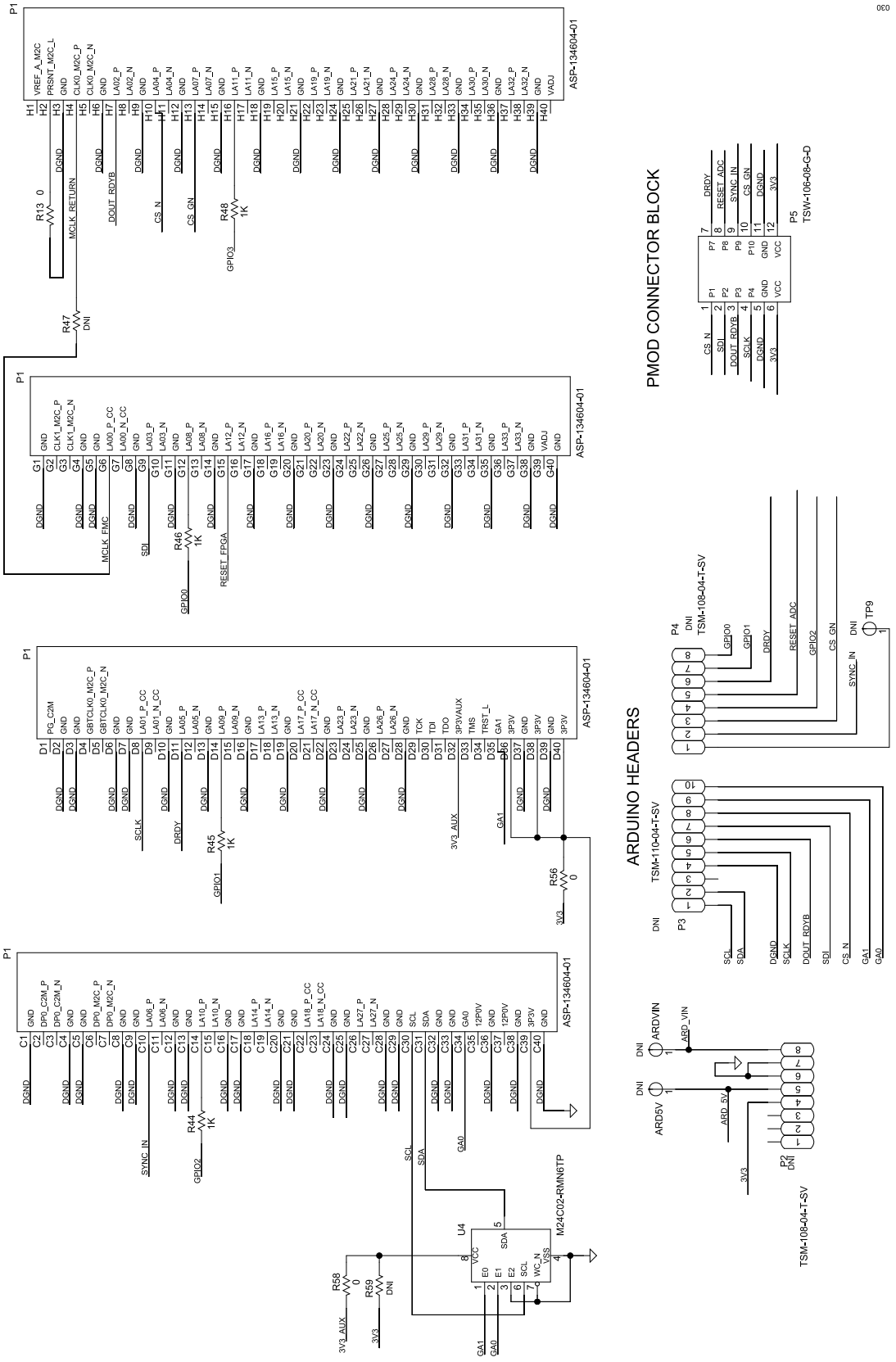


Figure 30. Evaluation Board Schematic 2

EVALUATION BOARD LAYOUT

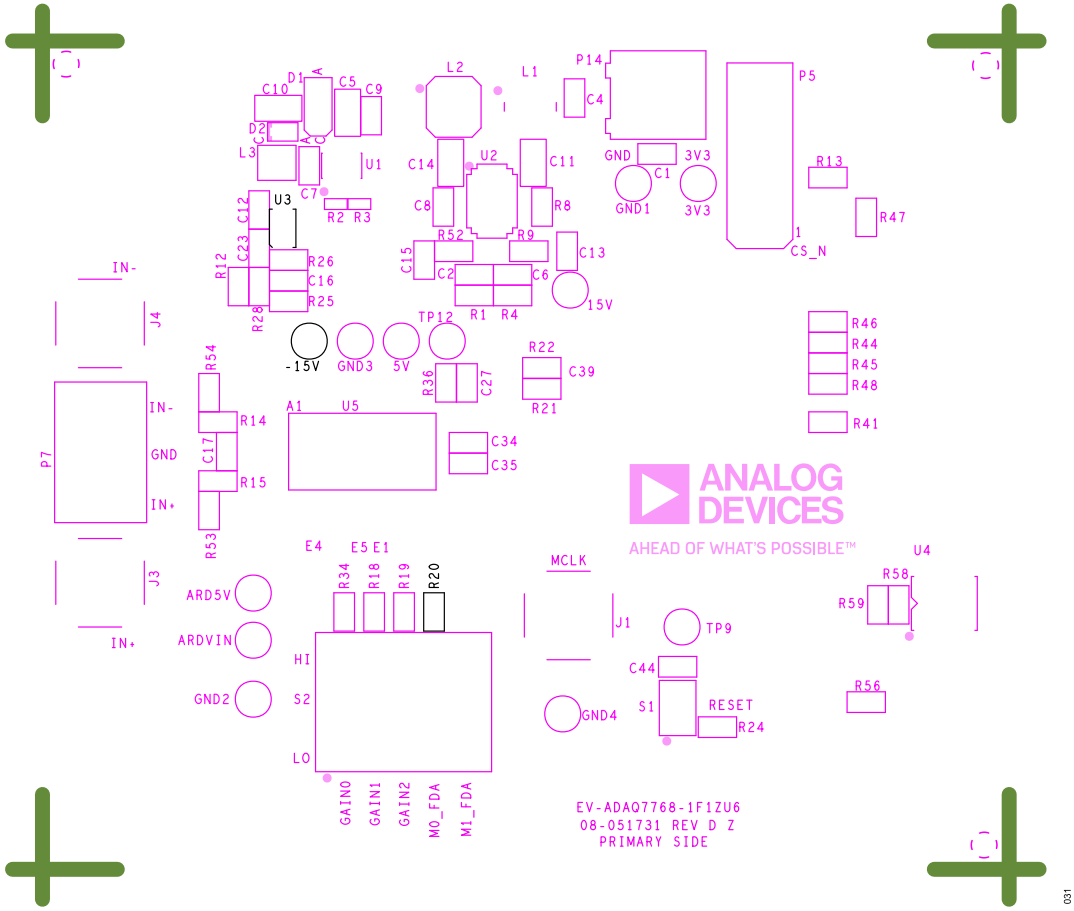


Figure 31. Silkscreen Primary

EVALUATION BOARD LAYOUT

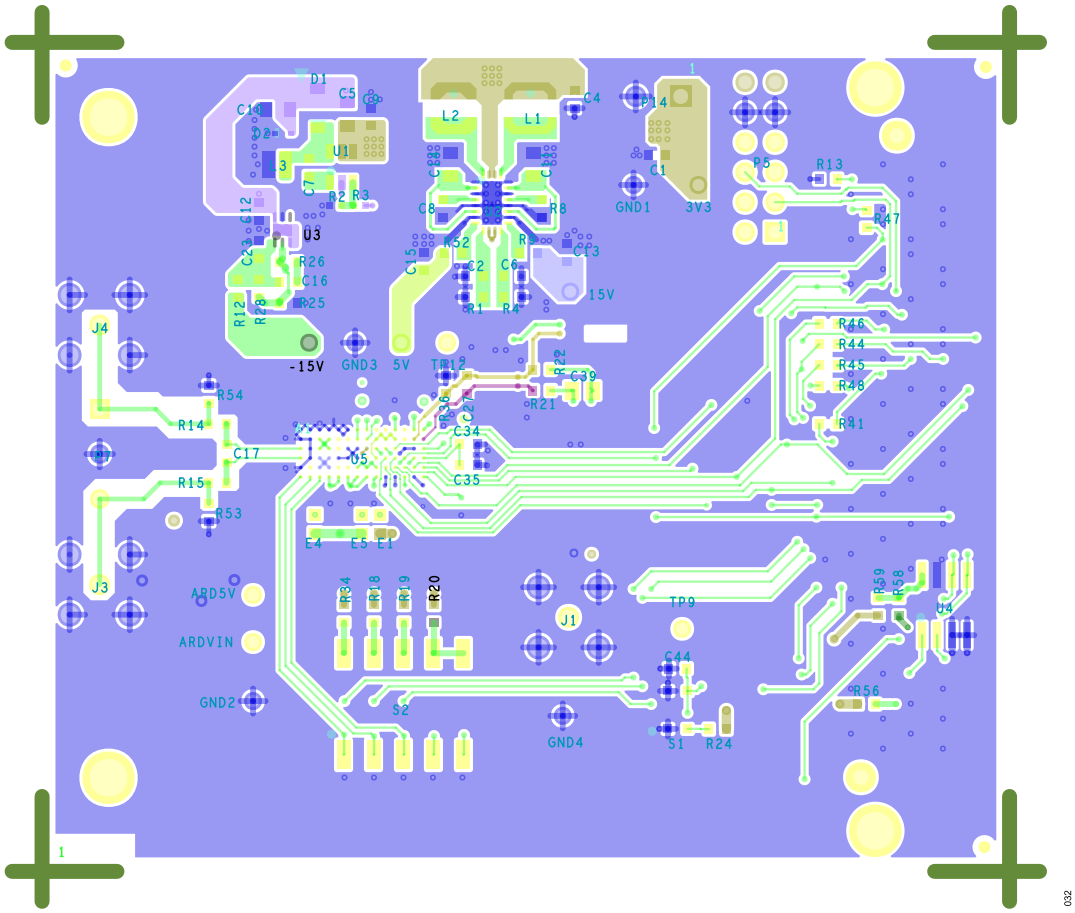


Figure 32. L1 Primary Layer

EVALUATION BOARD LAYOUT

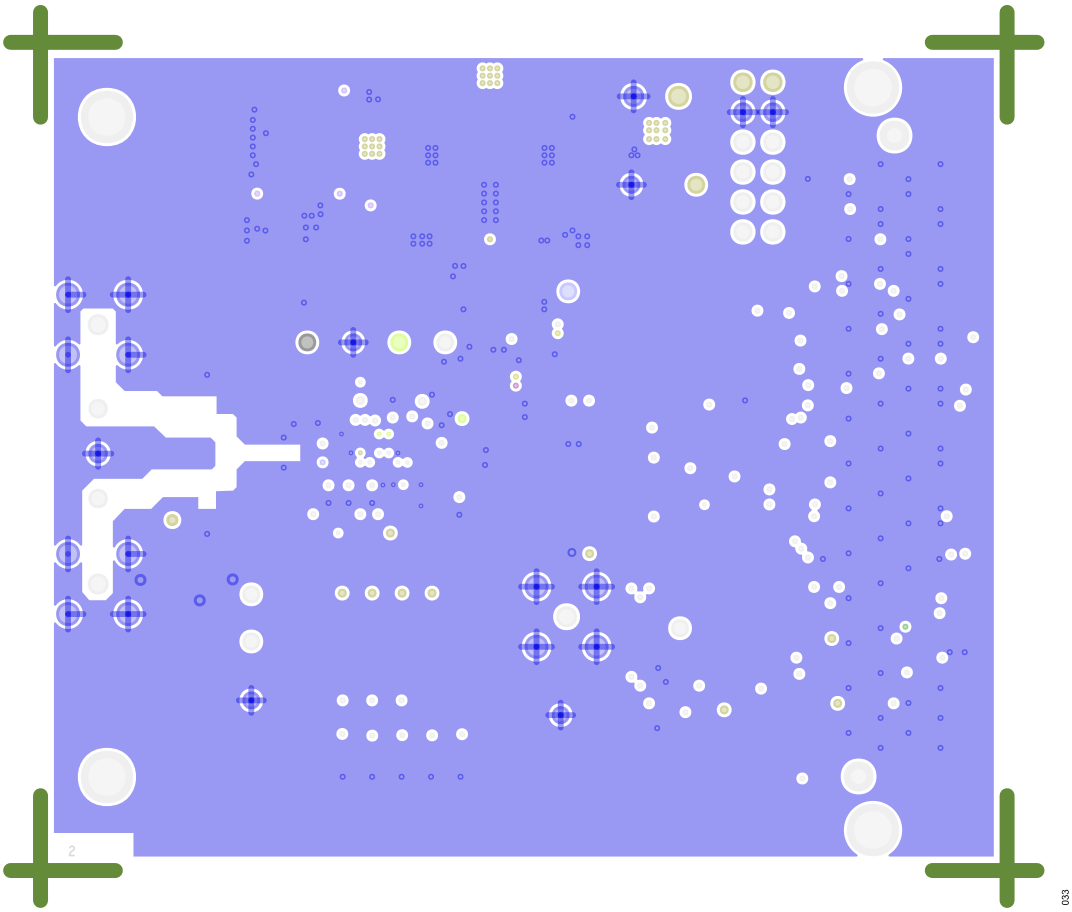


Figure 33. L2 Ground Layer

EVALUATION BOARD LAYOUT

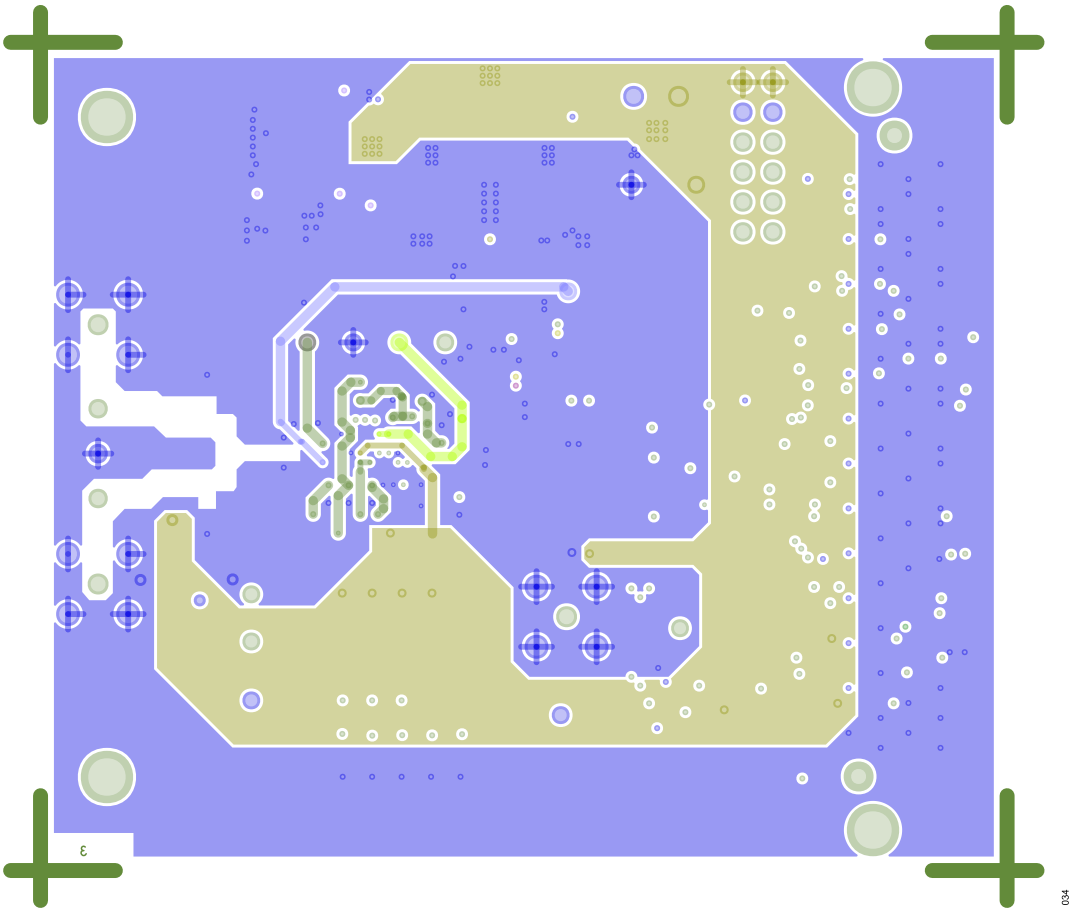


Figure 34. L3 Power Layer

EVALUATION BOARD LAYOUT

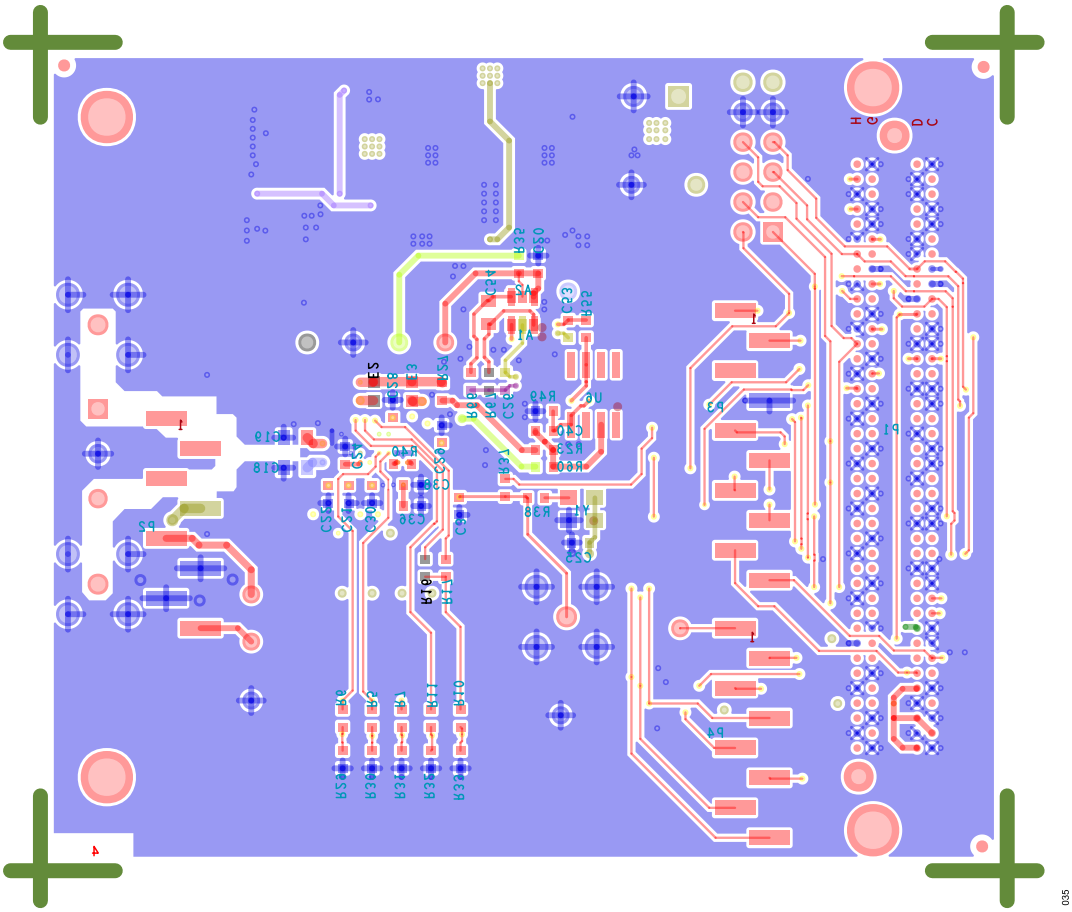


Figure 35. L4 Bottom Layer

EVALUATION BOARD LAYOUT

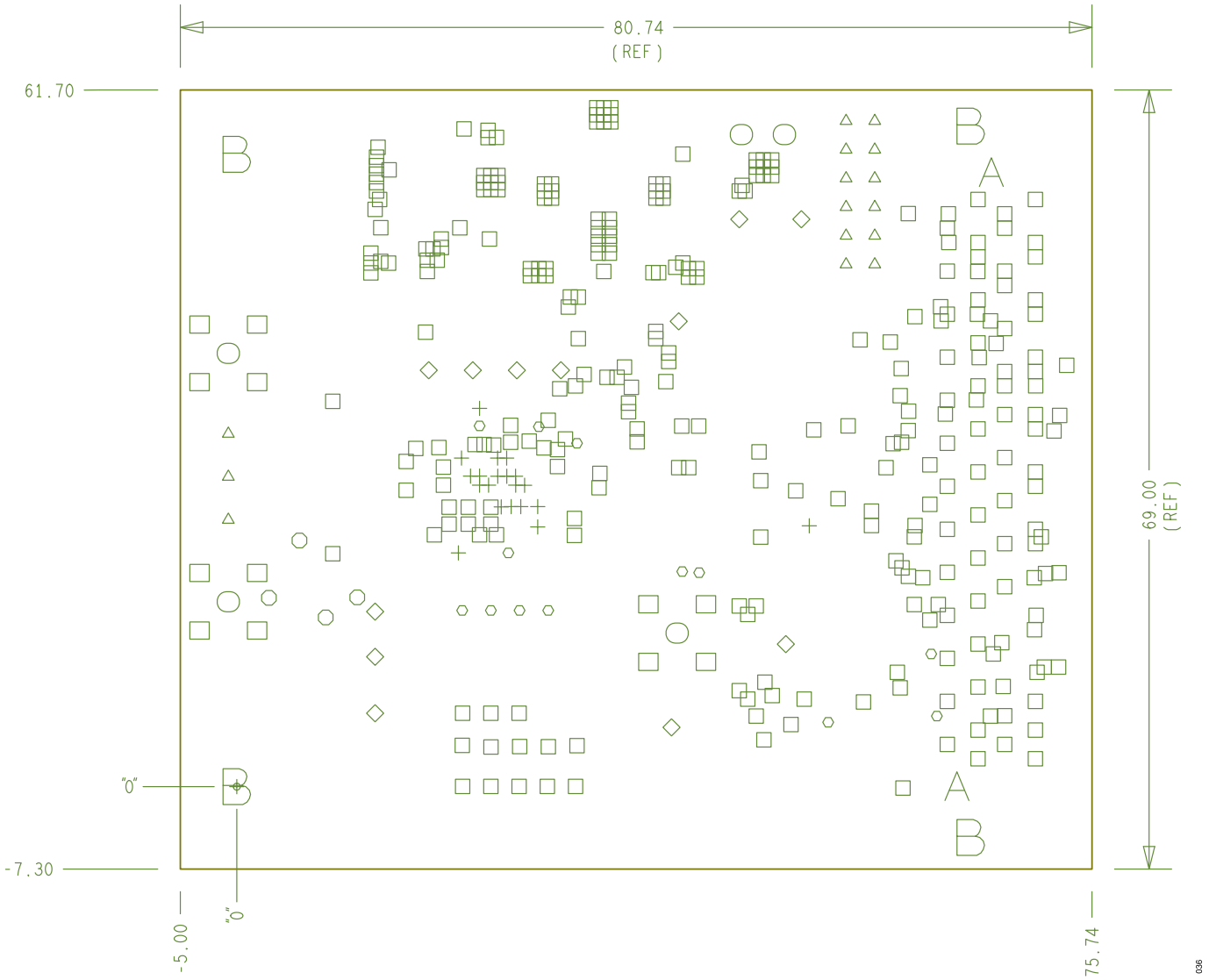


Figure 36. Finish Holes and Board Size

ORDERING INFORMATION

BILL OF MATERIALS

Table 6. Bill of Materials

Quantity	Designator	Description	Value	Manufacturer	Manufacturer Part Number
1	A1	180 MHz rail-to-rail input output amplifier	Not applicable	Analog Devices	ADA4807-1ARJZ-R7
4	C1, C9, C35, C38	Ceramic capacitors, X7R, AC volt, low capacitance change rate	1 µF	KEMET	C0603C105K8RACTU
1	C10	Multilayer ceramic chip capacitor, X7R	4.7 µF	TDK	C2012X7R1E475K125AB
2	C11, C14	Ceramic capacitors, X7R, for general use	10 µF	Murata	GRM21BZ71E106KE15L
3	C12, C13, C23	Ceramic capacitors, X5R, general purpose	2.2 µF	Murata	GRM188R61H225KE11J
2	C4, C15	Ceramic capacitors, X7R, general purpose	2.2 µF	Murata	GRM188R71A225KE15D
10	C2, C6, C7, C8, C16, C34, C36, C39, C40, C44	Ceramic capacitors, 0603, X7R	0.1 µF	KEMET	C0603C104K3RACTU
3	C5, C18, C19	Ceramic chip capacitors, X7R	1 µF	Murata	GCM21BR71E105KA56L
1	C27	Ceramic capacitor, X7S, general purpose	22 µF	TDK	C2012X7S1A226M125AC
1	C54	Ceramic capacitor, X5R, commercial grade	3.9 µF	KEMET	C0805C395K8PACTU
1	D1	Diode Schottky power rectifier, surface-mount device	Not applicable	ON Semiconductor	MBR0520LT1G
1	D2	Diode Schottky barrier	Not applicable	NXP Semiconductors	1PS79SB17
5	E1, E2, E3, E4, E5	Inductor chips, ferrite bead, 0.3 A, 0.39 Ω DC resistance	1000 Ω at 100 MHz	TAIYO YUDEN	BK1608TS102-T
4	GND1, GND2, GND3, GND4	PCB connectors, test point black	Not applicable	Keystone Electronics	5001
3	J1, J3, J4	PCB connectors, Subminiature Version B, jack ST	Not applicable	TE Connectivity Limited	1-1337482-0
1	L1	Shielded power inductor (not recommended for new designs)	10 µH	Coilcraft Incorporated	LPS4018-103MLB
1	L2	Shielded power inductor, 1.5 A, 0.150 Ω DC resistance	6.8 µH	Coilcraft Incorporated	LPS4018-682MRB
1	L3	Shielded power inductor, 0.729 A, 0.459 Ω maximum DC resistance	10 µH	Coilcraft Incorporated	EPL2014-103MLB
1	P1	PCB connector, signal-end male 160 position, for Kitt RF application, use alternate symbol	Not applicable	Samtec	ASP-134604-01
1	P14	PCB connector, terminal black standard, 10 A, 3.81 mm pitch	Not applicable	Camdenboss	CTB0308/2

ORDERING INFORMATION

Table 6. Bill of Materials (Continued)

Quantity	Designator	Description	Value	Manufacturer	Manufacturer Part Number
1	P5	PCB connector, high dynamic range standard male, peripheral module	Not applicable	Samtec	TSW-106-08-G-D
1	P7	PCB connector, term block, 3 position	Not applicable	Phoenix Contact	1727023
1	R1	Precision resistor, thick film chip	105 kΩ	Panasonic	ERJ-3EKF1053V
13	R9, R12, R13, R14, R15, R37, R40, R49, R52, R56, R58, R60, R65	Resistors, film, surface-mount devices 0603	0 Ω	Panasonic	ERJ-3GEY0R00V
5	R5, R6, R7, R16, R17	Resistors, standard thick film chip	0 Ω	Vishay	CRCW06030000Z0EAHP
1	R2	Resistor, standard thick film chip	68.1 kΩ	Panasonic	ERJ-2RKF6812X
1	R24	Resistor, standard thick film chip, R0603	10 kΩ	Panasonic	ERJ-3EKF1002V
2	R25, R26	Resistors, general purpose chip	13 kΩ	YAGEO	RC0603FR-0713KL
1	R28	Resistor, chip, surface-mount device, 0603	147 kΩ	Susumu Corporation Limited	RR0816P-1473-D-17D
5	R29, R30, R31, R32, R33	Resistors, precision thick film chip	20 kΩ	Panasonic	ERJ-3EKF2002V
1	R3	Resistor, precision thick film chip	3.57 kΩ	Panasonic	ERJ-2RKF3571X
6	R34, R41, R44, R45, R46, R48	Resistors, thick film chip	1 kΩ	Multicomp (SPC)	MC0063W060311K
1	R4	Resistor, metal film high release	300 kΩ	Panasonic	ERA-3AEB304V
2	R55, R66	Resistors, metal film chip	1 kΩ	Panasonic	ERA-3AEB102V
1	R67	Precision resistor, thick film chip, R0603	100 kΩ	Panasonic	ERJ-3EKF1000V
1	R8	Resistor, standard thick film chip, for automotive	100 kΩ	Vishay	CRCW0603100KFKEA
1	S1	Tactile switch, microminiature, top-actuated, single-pole single-throw (SPST)-NO	Not applicable	C & K Switches	PTS830 GM140 SMTR LFS
1	S2	Smart switch, 5 position	Not applicable	CTS	219-5MST
1	U1	Non-synchronization step-down DC-DC	Not applicable	Analog Devices	ADP2300AUJZ-R7
1	U2	Dual-channel, low-noise, bias generators	Not applicable	Linear Technology	LT3095IUDD#PBF
1	U3	Low-noise, linear regulator, adjacent output voltage	Not applicable	Analog Devices	ADP7182ACPZN-R7
1	U4	2 KB serial I^2C bus, electrically erasable programmable read-only memory (EEPROM), 1.8 V to 5.5 V	Not applicable	STMicroelectronics	M24C02-RMN6TP
1	U5	24-bit, single-channel precision µModule data	Not applicable	Analog Devices	ADAQ7768-1BBCZ-V2

ORDERING INFORMATION

Table 6. Bill of Materials (Continued)

Quantity	Designator	Description	Value	Manufacturer	Manufacturer Part Number
		acquisition system, preliminary			
1	U8	Ultra-low noise, low-dropout XFET voltage references with current sink and source	Not applicable	Analog Devices	ADR444BRZ

ORDERING INFORMATION

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.