

## FEATURES

- 4-channel LNA, PGA, and AAF**
- 1 direct to ADC channel**
- Programmable gain amplifier (PGA)**
  - Includes low noise preamplifier (LNA)
  - Serial peripheral interface (SPI) programmable gain
  - 16 dB to 34 dB in 6 dB steps
- Antialiasing filter (AAF)**
  - Programmable third order, low-pass elliptic filter (LPF)
  - from 1.0 MHz to 12.0 MHz
- Analog-to-digital converter (ADC)**
  - 12 bits of accuracy up to 72 MSPS
  - Signal-to-noise ratio (SNR): 68.5 dB
  - Spurious-free dynamic range (SFDR): 68 dB at gain = 16 dB
- Low power: 185 mW per channel at 12 bits and 72 MSPS**
- Low noise: 3.5 nV/ $\sqrt{\text{Hz}}$  maximum of input referred voltage noise**
- Power-down mode**
- 72-lead, 10 mm  $\times$  10 mm LFCSP package**
- Specified from  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$**
- Qualified for automotive applications**

## APPLICATIONS

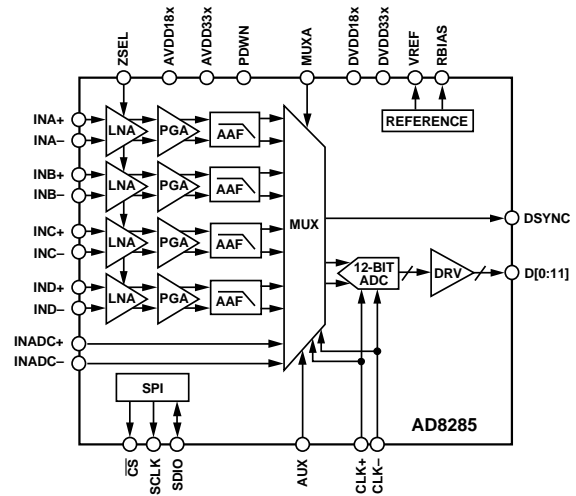
- Automotive radar**
  - Adaptive cruise control
  - Collision avoidance
  - Blind spot detection
  - Self parking
  - Electronic bumper

## GENERAL DESCRIPTION

The AD8285 is designed for low cost, low power, compact size, flexibility, and ease of use. It contains four channels of a low noise preamplifier (LNA) with a programmable gain amplifier (PGA) and an antialiasing filter (AAF) plus one direct to ADC channel, all integrated with a single 12-bit analog-to-digital converter (ADC).

Each channel features a gain range of 16 dB to 34 dB in 6 dB increments and an ADC with a conversion rate of up to 72 MSPS. The combined input referred noise voltage of the entire channel is 3.5 nV/ $\sqrt{\text{Hz}}$  at maximum gain. The channel is optimized for dynamic performance and low power in applications where a small package size is critical.

## FUNCTIONAL BLOCK DIAGRAM



NOTES  
 1. AVDD18x = AVDD18, AVDD18ADC.  
 AVDD33x = AVDD33, AVDD33A, AVDD33B, AVDD33C, AVDD33D, AVDD33REF.  
 DVDD18x = DVDD18, DVDD18CLK. DVDD33x = DVDD33, DVDD33SPI, DVDD33CLK, DVDD33DRV.

Figure 1.

Fabricated in an advanced complementary metal oxide semiconductor (CMOS) process, the AD8285 is available in a 10 mm  $\times$  10 mm, RoHS compliant, 72-lead LFCSP that is specified over the automotive temperature range of  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ .

Table 1. Related Devices

| Part No. | Description  |
|----------|--|
| AD8283   | 6-channel LNA/PGA/AAF, pseudo simultaneous channel sampling with ADC |
| AD8284   | 4-channel LNA/PGA/AAF, sequential channel sampling with ADC          |
| ADA8282  | 4-channel LNA/PGA  |

# AD8285\* Product Page Quick Links

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### **Data Sheet**

- AD8285: Radar Receive Path AFE: 4-Channel LNA/PGA/AAF with ADC Data Sheet

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## REVISION HISTORY

### 9/15—Rev. A to Rev. B

|  |   |
|--|---|
| Added Table 1; Renumbered Sequentially ..... | 1 |
|--|---|

### 10/14—Rev. 0 to Rev. A

|  |    |
|--|----|
| Changes to Addr. (Hex) 0x15, Table 8 ..... | 23 |
| Changes to Ordering Guide .....            | 27 |

### 5/14—Revision 0: Initial Version

## SPECIFICATIONS

### AC SPECIFICATIONS

AVDD18 = AVDD18ADC = 1.8 V, AVDD33 = AVDD33x<sup>1</sup> = AVDD33REF = 3.3 V, DVDD18 = DVDD18CLK = 1.8 V, DVDD33SPI = DVDD33CLK = DVDD33DRV = 3.3 V, 1.024 V internal ADC reference,  $f_{IN} = 2.5$  MHz,  $f_{SAMPLE} = 72$  MSPS,  $R_S = 50 \Omega$ , LNA + PGA gain = 34 dB, LPF cutoff =  $f_{SAMPLE}/4$ , full channel mode, 12-bit operation, temperature =  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ , unless otherwise noted.

Table 2.

| Parameter <sup>2</sup>                   | Test Conditions/Comments  | Min   | Typ         | Max   | Unit                   |
|--|---|-------|-------------|-------|------------------------|
| <b>ANALOG CHANNEL CHARACTERISTICS</b>    |   |       |             |       |                        |
| LNA, PGA, and AAF channels               |   |       |             |       |                        |
| Gain                                     |   |       | 16/22/28/34 |       | dB                     |
| Gain Range                               |   |       | 18          |       | dB                     |
| Gain Error                               |   | -1.25 |             | +1.25 | dB                     |
| Input Voltage Range                      | Channel gain = 16 dB  |       | 0.25        |       | V p-p                  |
|  | Channel gain = 22 dB  |       | 0.125       |       | V p-p                  |
|  | Channel gain = 28 dB  |       | 0.0625      |       | V p-p                  |
|  | Channel gain = 34 dB  |       | 0.03125     |       | V p-p                  |
| Input Resistance                         | 200 $\Omega$ input impedance selected   | 0.180 | 0.230       | 0.280 | k $\Omega$             |
|  | 200 k $\Omega$ input impedance selected   | 160   | 200         | 240   | k $\Omega$             |
| Input Capacitance                        |   |       | 22          |       | pF                     |
| Input Referred Voltage Noise             | Maximum gain at 1 MHz   |       | 1.85        |       | nV/ $\sqrt{\text{Hz}}$ |
|  | Minimum gain at 1 MHz   |       | 6.03        |       | nV/ $\sqrt{\text{Hz}}$ |
| Noise Figure                             | Maximum gain, $R_S = 50 \Omega$ , unterminated  |       | 7.1         |       | dB                     |
|  | Maximum gain, $R_S = R_{IN} = 50 \Omega$  |       | 12.7        |       | dB                     |
| Output Offset                            | Gain = 16 dB  | -60   |             | +60   | LSB                    |
|  | Gain = 34 dB  | -250  |             | +250  | LSB                    |
| AAF Low-Pass Filter Cutoff               | -3 dB, programmable   |       | 1.0 to 12.0 |       | MHz                    |
| Tolerance                                | After filter autotune   | -10   | $\pm 5$     | +10   | %                      |
| AAF Attenuation in Stop Band             | Third-order elliptic filter   |       |             |       |                        |
|  | 2 $\times$ cutoff   |       | 30          |       | dB                     |
|  | 3 $\times$ cutoff   |       | 40          |       | dB                     |
| Group Delay Variation                    | Filter set at 2 MHz   |       | 400         |       | ns                     |
| Channel-to-Channel Phase Variation       | Frequencies up to -3 dB   | -5    | $\pm 0.5$   | +5    | Degrees                |
|  | 1/4 of -3 dB frequency  | -1    |             | +1    | Degrees                |
| Channel-to-Channel Gain Matching         | Frequencies up to -3 dB   | -0.5  | $\pm 0.1$   | +0.5  | dB                     |
|  | 1/4 of -3 dB frequency  | -0.25 |             | +0.25 | dB                     |
| 1 dB Compression                         | Relative to output  |       | 9.8         |       | dBm                    |
| Crosstalk                                |   |       | -70         | -55   | dBc                    |
| <b>POWER SUPPLY</b>                      |   |       |             |       |                        |
| AVDD18, AVDD18ADC                        |   | 1.7   | 1.8         | 1.9   | V                      |
| AVDD33, AVDD33x <sup>1</sup> , AVDD33REF |   | 3.1   | 3.3         | 3.5   | V                      |
| DVDD18, DVDD18CLK                        |   | 1.7   | 1.8         | 1.9   | V                      |
| DVDD33SPI, DVDD33CLK,<br>DVDD33DRV       |   | 3.1   | 3.3         | 3.5   | V                      |
| I <sub>AVDD18</sub>                      | Full channel mode   |       |             | 130   | mA                     |
| I <sub>AVDD33</sub>                      | Full channel mode   |       |             | 130   | mA                     |
| I <sub>DVDD18</sub>                      |   |       |             | 22    | mA                     |
| I <sub>DVDD33</sub>                      |   |       |             | 2     | mA                     |
| Total Power Dissipation Per Channel      | Full channel mode, no signal, typical supply voltage $\times$ maximum supply current; excludes output current |       |             | 185   | mW                     |
| Power-Down Dissipation                   |   |       | 5           |       | mW                     |
| Power Supply Rejection Ratio (PSRR)      |   |       | 1.6         |       | mV/V                   |

| Parameter <sup>2</sup>                               | Test Conditions/Comments  | Min | Typ   | Max      | Unit       |
|--|---|-----|-------|----------|------------|
| ADC  |   |     |       |          |            |
| Resolution   |   |     | 12    |          | Bits       |
| Maximum Sample Rate                                  |   |     | 72    |          | MSPS       |
| Signal-to-Noise Ratio (SNR)                          | $f_{IN} = 1 \text{ MHz}$  |     | 68.5  |          | dB         |
| Signal-to-Noise and Distortion (SINAD)               |   |     | 66    |          | dB         |
| Signal-to-Noise Ratio Full Scale (SNRFS)             |   |     | 68    |          | dB         |
| Differential Nonlinearity (DNL)                      | Guaranteed no missing codes   |     |       | 1        | LSB        |
| Integral Nonlinearity (INL)                          |   |     |       | 10       | LSB        |
| Effective Number of Bits (ENOB)                      |   |     | 10.67 |          | LSB        |
| ADC OUTPUT CHARACTERISTICS                           |   |     |       |          |            |
| Maximum Capacitor Load                               | Per bit   |     | 20    |          | pF         |
| $I_{D\text{VDD}33}$ Peak Current with Capacitor Load | Peak current per bit when driving 20 pF load; can be programmed via the SPI port, if required |     |       | 40       | mA         |
| ADC REFERENCE  |   |     |       |          |            |
| Output Voltage Error                                 | $V_{REF} = 1.024 \text{ V}$   |     |       | $\pm 25$ | mV         |
| Load Regulation                                      | At 1.0 mA, $V_{REF} = 1.024 \text{ V}$  |     | 2     |          | mV         |
| Input Resistance                                     |   |     | 6     |          | k $\Omega$ |
| FULL CHANNEL CHARACTERISTICS                         | LNA, PGA, AAF, and ADC channels   |     |       |          |            |
| SNRFS  | $f_{IN} = 1 \text{ MHz}$  |     |       |          |            |
|  | Gain = 16 dB  |     | 68    |          | dB         |
|  | Gain = 22 dB  |     | 68    |          | dB         |
|  | Gain = 28 dB  |     | 68    |          | dB         |
|  | Gain = 34 dB  |     | 66    |          | dB         |
| SINAD  | $f_{IN} = 1 \text{ MHz}$  |     |       |          |            |
|  | Gain = 16 dB  |     | 67    |          | dB         |
|  | Gain = 22 dB  |     | 68    |          | dB         |
|  | Gain = 28 dB  |     | 67    |          | dB         |
|  | Gain = 34 dB  |     | 66    |          | dB         |
| Spurious-Free Dynamic Range (SFDR)                   | $f_{IN} = 1 \text{ MHz}$  |     |       |          |            |
|  | Gain = 16 dB  |     | 68    |          | dB         |
|  | Gain = 22 dB  |     | 74    |          | dB         |
|  | Gain = 28 dB  |     | 74    |          | dB         |
|  | Gain = 34 dB  |     | 73    |          | dB         |
| Harmonic Distortion                                  |   |     |       |          |            |
| Second Harmonic                                      | $f_{IN} = 1 \text{ MHz}$ at $-10 \text{ dBFS}$ , gain = 16 dB                                 |     | -70   |          | dBc        |
|  | $f_{IN} = 1 \text{ MHz}$ at $-10 \text{ dBFS}$ , gain = 34 dB                                 |     | -70   |          | dBc        |
| Third Harmonic                                       | $f_{IN} = 1 \text{ MHz}$ at $-10 \text{ dBFS}$ , gain = 16 dB                                 |     | -66   |          | dBc        |
|  | $f_{IN} = 1 \text{ MHz}$ at $-10 \text{ dBFS}$ , gain = 34 dB                                 |     | -75   |          | dBc        |
| IM3 Distortion                                       | $f_{IN1} = 1 \text{ MHz}$ , $f_{IN2} = 1.1 \text{ MHz}$ , $-1 \text{ dBFS}$ , gain = 34 dB    |     | -69   |          | dBc        |
| Gain Response Time                                   |   |     | 600   |          | ns         |
| Overdrive Recovery Time                              |   |     | 200   |          | ns         |

<sup>1</sup> x stands for A, B, C, or D.

<sup>2</sup> See the [AN-835 Application Note, Understanding High Speed ADC Testing and Evaluation](#), for a complete set of definitions, and how these tests were completed.

**DIGITAL SPECIFICATIONS**

AVDD18 = AVDD18ADC = 1.8 V, AVDD33 = AVDD33x<sup>1</sup> = AVDD33REF = 3.3 V, DVDD18 = DVDD18CLK = 1.8 V, DVDD33SPI = DVDD33CLK = DVDD33DRV = 3.3 V, 1.024 V internal ADC reference,  $f_{IN} = 2.5$  MHz,  $f_{SAMPLE} = 72$  MSPS,  $R_S = 50$   $\Omega$ , LNA + PGA gain = 34 dB, LPF cutoff =  $f_{SAMPLE}/4$ , full channel mode, 12-bit operation, temperature =  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ , unless otherwise noted.

**Table 3.**

| Parameter <sup>2</sup>                           | Temperature | Min | Typ              | Max           | Unit       |
|--|-------------|-----|------------------|---------------|------------|
| CLOCK INPUTS (CLK+, CLK-)                        |             |     |                  |               |            |
| Logic Compliance                                 |             |     | CMOS/LVDS/LVPECL |               |            |
| Differential Input Voltage <sup>3</sup>          | Full        | 250 |                  |               | mV p-p     |
| Input Common-Mode Voltage                        | Full        |     | 1.2              |               | V          |
| Differential Input Resistance                    | 25°C        |     | 20               |               | k $\Omega$ |
| Input Capacitance                                | 25°C        |     | 1.5              |               | pF         |
| LOGIC INPUTS (PDWN, SCLK, AUX, MUXA, ZSEL)       |             |     |                  |               |            |
| Logic 1 Voltage                                  | Full        | 1.2 |                  | 3.6           | V          |
| Logic 0 Voltage                                  | Full        |     |                  | 0.3           | V          |
| Input Resistance                                 | 25°C        |     | 30               |               | k $\Omega$ |
| Input Capacitance                                | 25°C        |     | 0.5              |               | pF         |
| LOGIC INPUT (CS)                                 |             |     |                  |               |            |
| Logic 1 Voltage                                  | Full        | 1.2 |                  | 3.6           | V          |
| Logic 0 Voltage                                  | Full        |     |                  | 0.3           | V          |
| Input Resistance                                 | 25°C        |     | 70               |               | k $\Omega$ |
| Input Capacitance                                | 25°C        |     | 0.5              |               | pF         |
| LOGIC INPUT (SDIO)                               |             |     |                  |               |            |
| Logic 1 Voltage                                  | Full        | 1.2 |                  | DVDD33x + 0.3 | V          |
| Logic 0 Voltage                                  | Full        | 0   |                  | 0.3           | V          |
| Input Resistance                                 | 25°C        |     | 30               |               | k $\Omega$ |
| Input Capacitance                                | 25°C        |     | 2                |               | pF         |
| LOGIC OUTPUT (SDIO) <sup>4</sup>                 |             |     |                  |               |            |
| Logic 1 Voltage ( $I_{OH} = 800$ $\mu\text{A}$ ) | Full        | 3.0 |                  |               | V          |
| Logic 0 Voltage ( $I_{OL} = 50$ $\mu\text{A}$ )  | Full        |     |                  | 0.3           | V          |
| LOGIC OUTPUT (Dx, DSYNC)                         |             |     |                  |               |            |
| Logic 1 Voltage ( $I_{OH} = 2$ mA)               | Full        | 3.0 |                  |               | V          |
| Logic 0 Voltage ( $I_{OL} = 2$ mA)               | Full        |     |                  | 0.05          | V          |

<sup>1</sup> x stands for A, B, C, or D.

<sup>2</sup> See the [AN-835 Application Note](#), *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions, and how these tests were completed.

<sup>3</sup> Specified for LVDS and LVPECL only.

<sup>4</sup> Specified for 13 SDIO pins sharing the same connection.

**SWITCHING SPECIFICATIONS**

AVDD18 = AVDD18ADC = 1.8 V, AVDD33 = AVDD33x<sup>1</sup> = AVDD33REF = 3.3 V, DVDD18 = DVDD18CLK = 1.8 V, DVDD33SPI = DVDD33CLK = DVDD33DRV = 3.3 V, 1.024 V internal ADC reference, f<sub>IN</sub> = 2.5 MHz, f<sub>SAMPLE</sub> = 72 MSPS, R<sub>S</sub> = 50 Ω, LNA + PGA gain = 34 dB, LPF cutoff = f<sub>SAMPLE</sub>/4, full channel mode, 12-bit operation, temperature = -40°C to +105°C, unless otherwise noted.

**Table 4.**

| Parameter <sup>2</sup>                               | Temperature | Min  | Typ  | Max  | Unit         |
|--|-------------|------|------|------|--------------|
| <b>CLOCK</b>   |             |      |      |      |              |
| Clock Rate   | Full        | 10   |      | 72   | MSPS         |
| Clock Pulse Width High (t <sub>EH</sub> ) at 72 MSPS | Full        |      | 6.94 |      | ns           |
| Clock Pulse Width Low (t <sub>EL</sub> ) at 72 MSPS  | Full        |      | 6.94 |      | ns           |
| Clock Pulse Width High (t <sub>EH</sub> ) at 40 MSPS | Full        |      | 12.5 |      | ns           |
| Clock Pulse Width Low (t <sub>EL</sub> ) at 40 MSPS  | Full        |      | 12.5 |      | ns           |
| <b>OUTPUT PARAMETERS</b>                             |             |      |      |      |              |
| Propagation Delay (t <sub>PD</sub> ) at 72 MSPS      | Full        | 1.5  | 2.5  | 5.0  | ns           |
| Rise Time (t <sub>R</sub> ) <sup>3</sup>             | Full        |      | 1.9  |      | ns           |
| Fall Time (t <sub>F</sub> ) <sup>3</sup>             | Full        |      | 1.2  |      | ns           |
| Data Set-Up Time (t <sub>DS</sub> ) at 72 MSPS       | Full        | 9.0  | 10.0 | 11.0 | ns           |
| Data Hold Time (t <sub>DH</sub> ) at 72 MSPS         | Full        | 1.5  | 4.0  | 5.0  | ns           |
| Data Set-Up Time (t <sub>DS</sub> ) at 40 MSPS       | Full        | 21.5 | 22.5 | 23.5 | ns           |
| Data Hold Time (t <sub>DH</sub> ) at 40 MSPS         | Full        | 1.5  | 4.0  | 5.0  | ns           |
| Pipeline Latency                                     | Full        |      | 7    |      | Clock cycles |

<sup>1</sup> x stands for A, B, C, or D.

<sup>2</sup> See the [AN-835 Application Note](#), *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions, and how these tests were completed.

<sup>3</sup> Not shown in Figure 2.

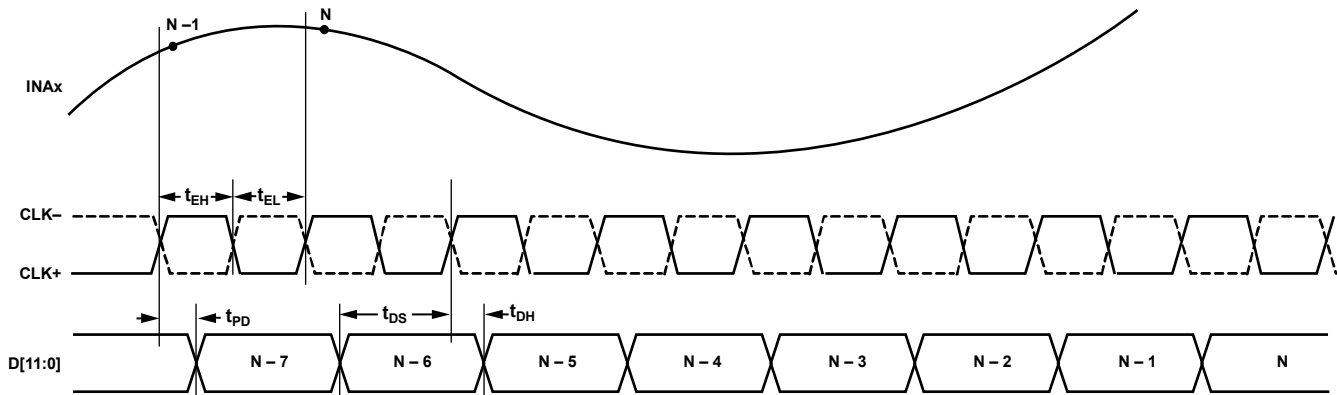


Figure 2. Timing Definitions for Switching Specifications

11982-002

## ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter   | Rating           |
|---|------------------|
| Electrical  |                  |
| AVDD18x <sup>1</sup> to GND                             | −0.3 V to +2.0 V |
| AVDD33x <sup>2</sup> to GND                             | −0.3 V to +3.5 V |
| DVDD18x <sup>3</sup> to GND                             | −0.3 V to +2.0 V |
| DVDD33x <sup>4</sup> to GND                             | −0.3 V to +3.5 V |
| Analog Inputs<br>INx+, INx− to GND                      | −0.3 V to +3.5 V |
| Auxiliary Inputs<br>INADC+, INADC− to GND               | −0.3 V to +2.0 V |
| Digital Outputs<br>D[11:0], DSYNC, SDIO to GND          | −0.3 V to +3.5 V |
| CLK+, CLK− to GND                                       | −0.3 V to +3.9 V |
| PDWN, SCLK, $\overline{CS}$ , AUX, MUXA,<br>ZSEL to GND | −0.3 V to +3.9 V |
| RBIAS, VREF to GND                                      | −0.3 V to +2.0 V |
| Environmental   |                  |
| Operating Temperature<br>Range (Ambient)                | −40°C to +105°C  |
| Storage Temperature<br>Range (Ambient)                  | −65°C to +150°C  |
| Maximum Junction<br>Temperature                         | 150°C            |
| Lead Temperature<br>(Soldering, 10 sec)                 | 300°C            |

<sup>1</sup> AVDD18x = AVDD18 and AVDD18ADC.

<sup>2</sup> AVDD33x = AVDD33A, AVDD33B, AVDD33C, AVDD33D, and AVDD33REF.

<sup>3</sup> DVDD18x = DVDD18, DVDD18CLK.

<sup>4</sup> DVDD33x = DVDD33, DVDD33SPI, DVDD33CLK, DVDD33DRV.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

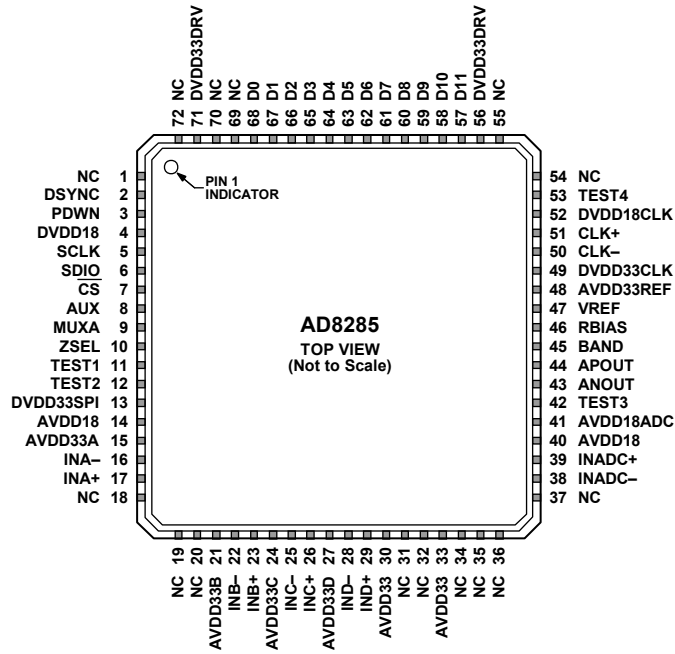
### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**  
 1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.  
 2. TIE THE EXPOSED PAD ON THE BOTTOM OF THE PACKAGE TO THE ANALOG/DIGITAL GROUND PLANE.

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

| Pin No. | Mnemonic  | Description   |
|---------|-----------|---|
| 0       | EPAD      | Exposed Pad. Tie the exposed pad on the bottom of the package to the analog/digital ground plane.   |
| 1       | NC        | No Connect. Do not connect to this pin.   |
| 2       | DSYNC     | Data Output Synchronization.  |
| 3       | PDWN      | Full Power Down. Logic high overrides the SPI and powers down the device. Logic low allows selection of the power down option through the SPI.                  |
| 4       | DVDD18    | 1.8 V Digital Supply.   |
| 5       | SCLK      | Serial Clock.   |
| 6       | SDIO      | Serial Data Input/Output.   |
| 7       | CS        | Chip Select Bar.  |
| 8       | AUX       | Auxiliary. A logic high on AUX switches the AUX channel (INADC+/INADC-) to the ADC. The AUX pin has a higher priority than the MUXA pin.                        |
| 9       | MUXA      | Channel A Select. Logic high forces to Channel A unless AUX is asserted.  |
| 10      | ZSEL      | Input Impedance Select. Logic high overrides the SPI and sets the input impedance to 200 kΩ. Logic low allows selection of the input impedance through the SPI. |
| 11      | TEST1     | Test. Do not use the TEST1 pin; tie it to ground.   |
| 12      | TEST2     | Test. Do not use the TEST2 pin; tie it to ground.   |
| 13      | DVDD33SPI | 3.3 V Digital Supply for SPI Port.  |
| 14      | AVDD18    | 1.8 V Analog Supply.  |
| 15      | AVDD33A   | 3.3 V Analog Supply for Channel A.  |
| 16      | INA-      | Negative LNA Analog Input for Channel A.  |
| 17      | INA+      | Positive LNA Analog Input for Channel A.  |
| 18      | NC        | No Connect. Do not connect to this pin.   |
| 19      | NC        | No Connect. Do not connect to this pin.   |
| 20      | NC        | No Connect. Do not connect to this pin.   |
| 21      | AVDD33B   | 3.3 V Analog Supply for Channel B.  |
| 22      | INB-      | Negative LNA Analog Input for Channel B.  |
| 23      | INB+      | Positive LNA Analog Input for Channel B.  |

| Pin No. | Mnemonic  | Description   |
|---------|-----------|---|
| 24      | AVDD33C   | 3.3 V Analog Supply for Channel C.  |
| 25      | INC-      | Negative LNA Analog Input for Channel C.  |
| 26      | INC+      | Positive LNA Analog Input for Channel C.  |
| 27      | AVDD33D   | 3.3 V Analog Supply for Channel D.  |
| 28      | IND-      | Negative LNA Analog Input for Channel D.  |
| 29      | IND+      | Positive LNA Analog Input for Channel D.  |
| 30      | AVDD33    | 3.3 V Analog Supply.  |
| 31      | NC        | No Connect. Do not connect to this pin.   |
| 32      | NC        | No Connect. Do not connect to this pin.   |
| 33      | AVDD33    | 3.3 V Analog Supply.  |
| 34      | NC        | No Connect. Do not connect to this pin.   |
| 35      | NC        | No Connect. Do not connect to this pin.   |
| 36      | NC        | No Connect. Do not connect to this pin.   |
| 37      | NC        | No Connect. Do not connect to this pin.   |
| 38      | INADC-    | Negative Analog Input for Alternate Channel D (ADC Only).                           |
| 39      | INADC+    | Positive Analog Input for Alternate Channel D (ADC Only).                           |
| 40      | AVDD18    | 1.8 V Analog Supply.  |
| 41      | AVDD18ADC | 1.8 V Analog Supply for ADC.  |
| 42      | TEST3     | Test. Do not use the TEST3 pin; tie it to ground.                                   |
| 43      | ANOUT     | Analog Outputs. The ANOUT pin is for debug purposes only. Leave this pin floating.  |
| 44      | APOUT     | Analog Outputs. The APOUT pin is for debug purposes only. Leave this pin floating.  |
| 45      | BAND      | Band Gap Voltage. The BAND pin is for debug purposes only. Leave this pin floating. |
| 46      | RBIAS     | External Resistor. The RBIAS pin sets the internal ADC core bias current.           |
| 47      | VREF      | Voltage Reference Input/Output.   |
| 48      | AVDD33REF | 3.3 V Analog Supply for References.   |
| 49      | DVDD33CLK | 3.3 V Digital Supply for Clock.   |
| 50      | CLK-      | Clock Input Complement.   |
| 51      | CLK+      | Clock Input True.   |
| 52      | DVDD18CLK | 1.8 V Digital Supply for Clock.   |
| 53      | TEST4     | Test. Do not use the TEST4 pin; tie it to ground.                                   |
| 54      | NC        | No Connect. Do not connect to this pin.   |
| 55      | NC        | No Connect. Do not connect to this pin.   |
| 56      | DVDD33DRV | 3.3 V Digital Supply for Output Driver.   |
| 57      | D11       | ADC Data Output 11 (MSB).   |
| 58      | D10       | ADC Data Output 10.   |
| 59      | D9        | ADC Data Output 9.  |
| 60      | D8        | ADC Data Output 8.  |
| 61      | D7        | ADC Data Output 7.  |
| 62      | D6        | ADC Data Output 6.  |
| 63      | D5        | ADC Data Output 5.  |
| 64      | D4        | ADC Data Output 4.  |
| 65      | D3        | ADC Data Output 3.  |
| 66      | D2        | ADC Data Output 2.  |
| 67      | D1        | ADC Data Output 1.  |
| 68      | D0        | ADC Data Output 0 (LSB).  |
| 69      | NC        | No Connect. Do not connect to this pin.   |
| 70      | NC        | No Connect. Do not connect to this pin.   |
| 71      | DVDD33DRV | 3.3 V Supply for Output Driver.   |
| 72      | NC        | No Connect. Do not connect to this pin.   |

# TYPICAL PERFORMANCE CHARACTERISTICS

AVDD18 = AVDD18ADC = 1.8 V, AVDD33A = AVDD33B = AVDD33C = AVDD33D = AVDD33 = AVDD33REF = AVDD33CLK = 3.3 V, T<sub>A</sub> = 25°C, f<sub>S</sub> = 72 MSPS, R<sub>IN</sub> = 200 kΩ, VREF = 1.024 V.

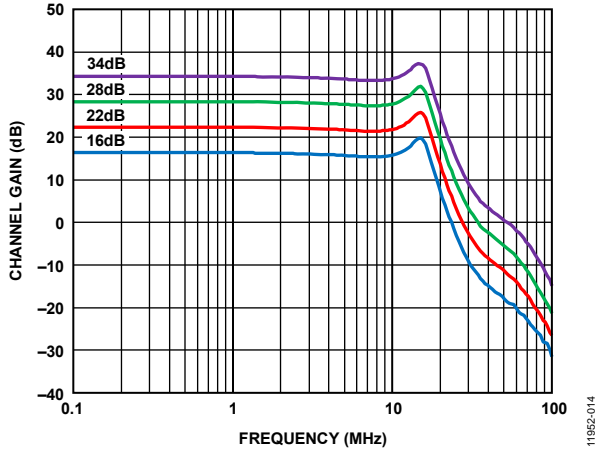


Figure 4. Channel Gain vs. Frequency

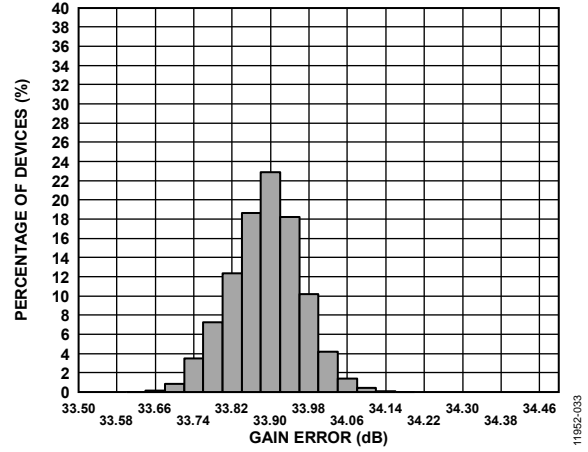


Figure 7. Gain Error Histogram (Gain = 34 dB)

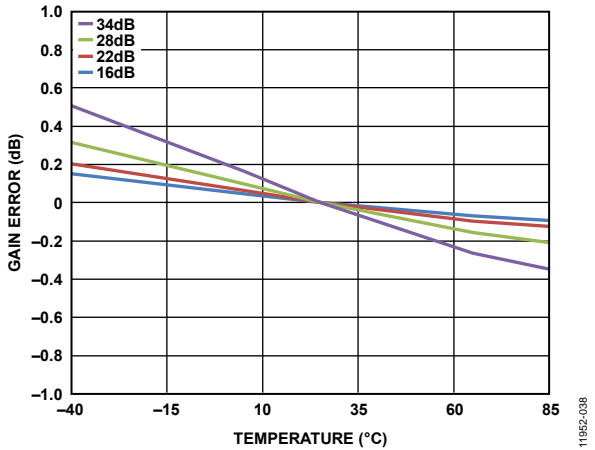


Figure 5. Gain Error vs. Temperature at All Gains

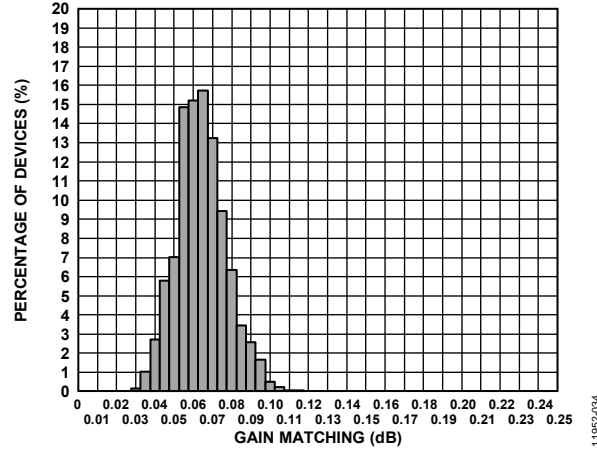


Figure 8. Channel-to-Channel Gain Matching (Gain = 16 dB)

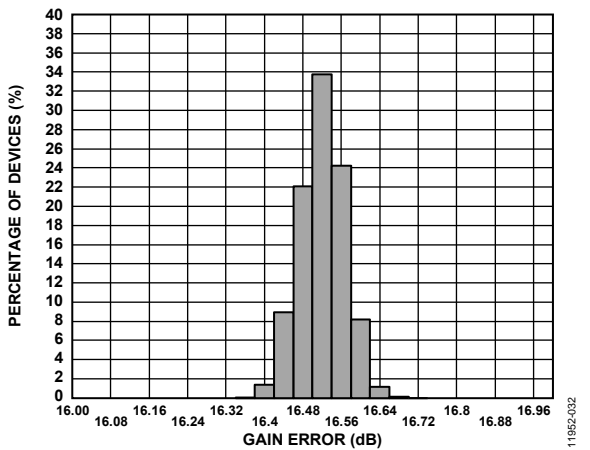


Figure 6. Gain Error Histogram (Gain = 16 dB)

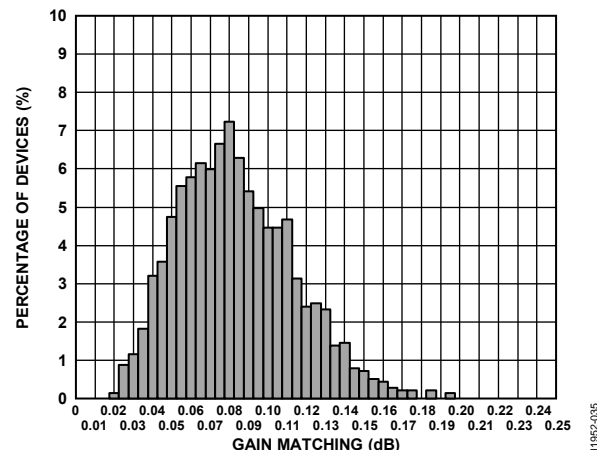


Figure 9. Channel-to-Channel Gain Matching (Gain = 34 dB)

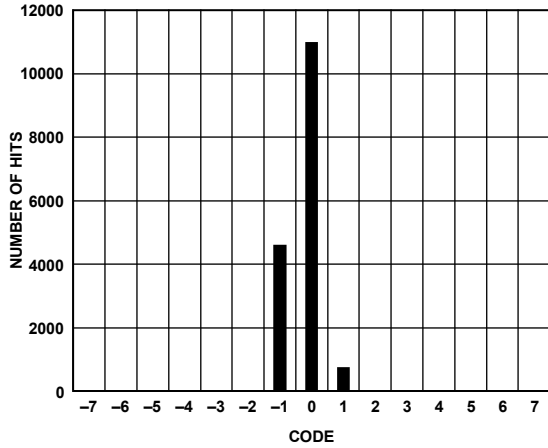


Figure 10. Output Referred Noise Histogram (Gain = 16 dB)

11952-015

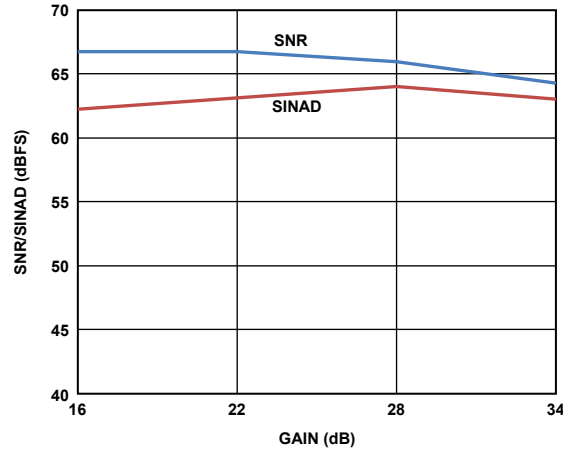


Figure 13. SNR/SINAD vs. Gain

11952-017

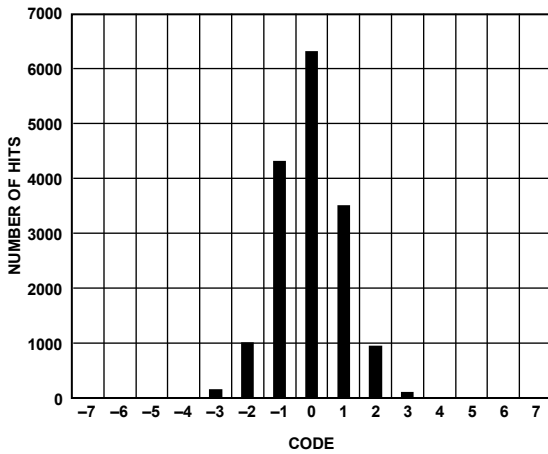


Figure 11. Output Referred Noise Histogram (Gain = 34 dB)

11952-016

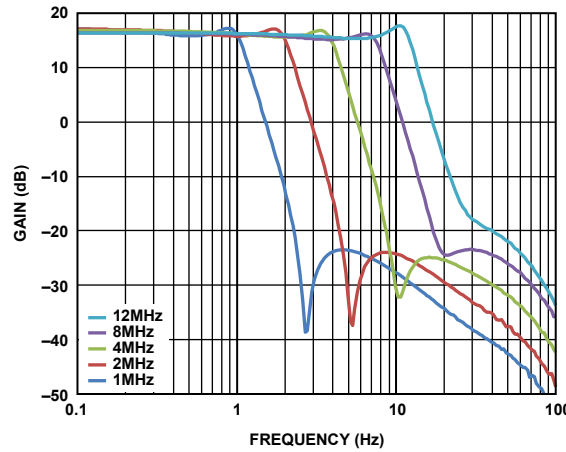


Figure 14. Filter Response

11952-022

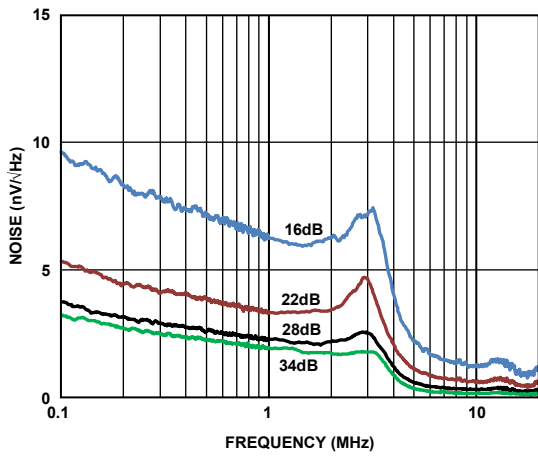


Figure 12. Short-Circuit Input Referred Noise vs. Frequency

11952-030

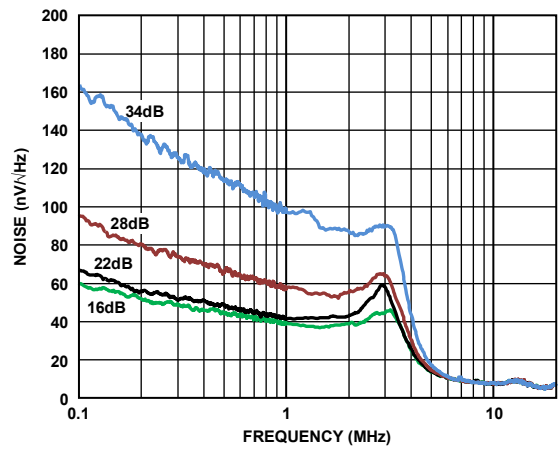


Figure 15. Short-Circuit Output Referred Noise vs. Frequency

11952-031

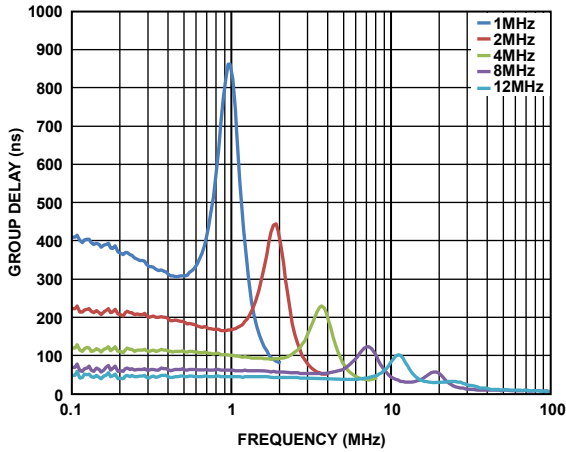


Figure 16. Group Delay vs. Frequency

11952-019

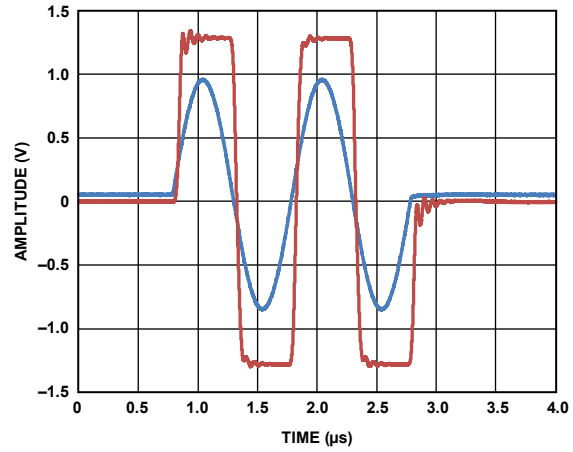


Figure 19. Overdrive Recovery

11952-041

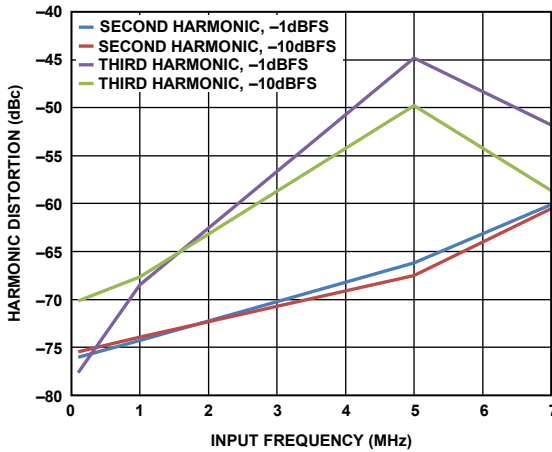


Figure 17. Harmonic Distortion vs. Input Frequency

11952-039

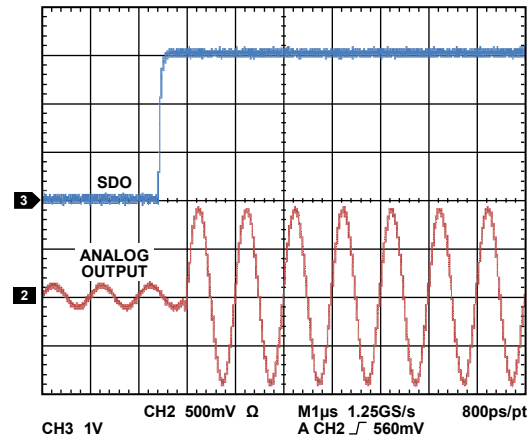


Figure 20. Gain Step Response

11952-024

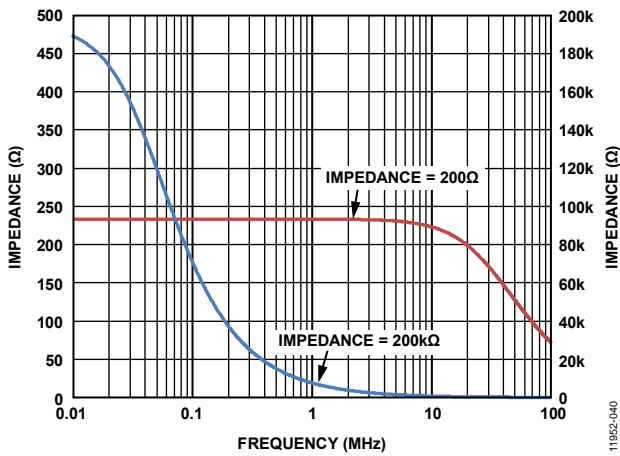


Figure 18.  $R_{IN}$  vs. Frequency

11952-040

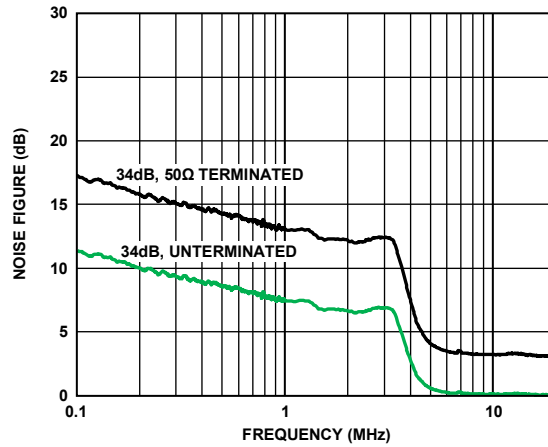


Figure 21. Noise Figure vs. Frequency

11952-042

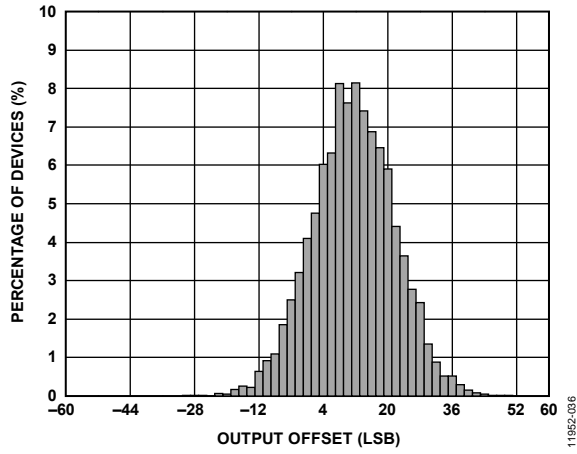


Figure 22. Channel Offset Distribution (Gain = 16 dB)

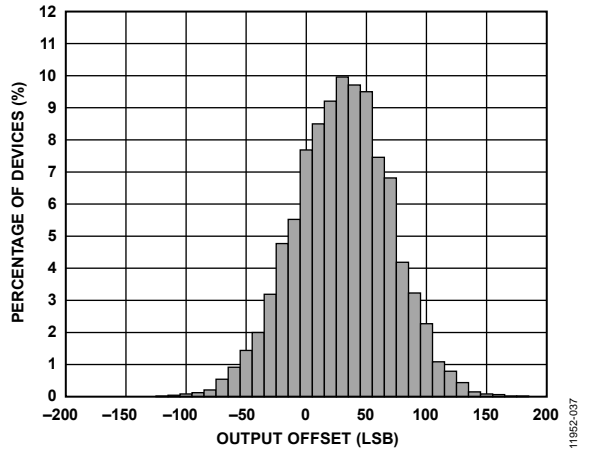


Figure 23. Channel Offset Distribution (Gain = 34 dB)

# THEORY OF OPERATION

## RADAR RECEIVE PATH AFE

The primary application for the AD8285 is a high speed ramp, frequency modulated, continuous wave radar (HSR-FMCW radar). Figure 24 shows a simplified block diagram of an HSR-FMCW radar system. The signal chain requires multiple channels, each including a LNA, a PGA, an AAF, and an ADC with a 12-bit parallel output. The AD8285 provides all of these key components in a single 10 × 10 LFCSP package.

The performance of each component is designed to meet the demands of an HSR-FMCW radar system. Some examples of these performance metrics are the LNA noise, PGA gain range, AAF cutoff characteristics, and ADC sample rate and resolution.

The AD8285 includes a multiplexer (mux) in front of the ADC as a cost saving alternative to having an ADC for each channel. The mux automatically switches between each active channel after each ADC sample. The DSYNC output indicates when Channel A data is at the ADC output and when data for each active channel follows sequentially with each clock cycle.

The effective sample rate for each channel is reduced by a factor equal to the number of active channels. The ADC resolution of 12 bits with up to 72 MSPS sampling satisfies the requirements for most HSR-FMCW approaches.

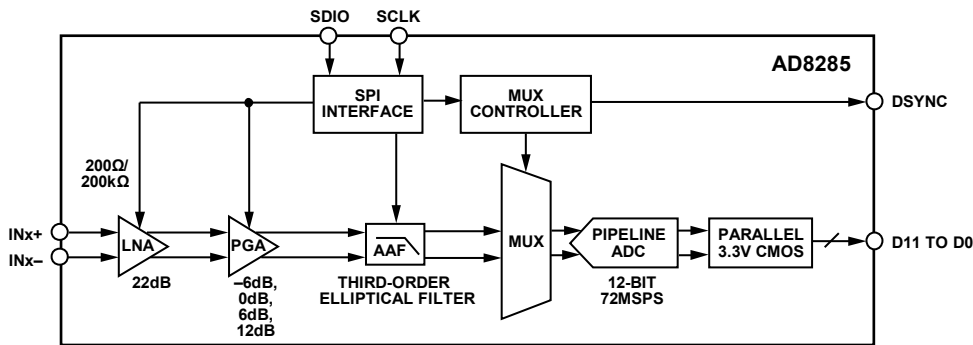


Figure 24. Simplified Block Diagram of a Single Channel

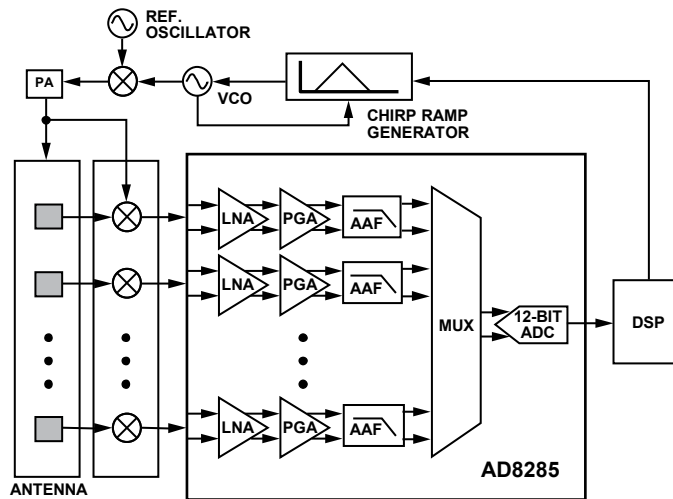


Figure 25. Radar System Overview

## CHANNEL OVERVIEW

Each channel contains an LNA, a PGA, and an AAF in the signal path. The LNA input impedance can be either 200  $\Omega$  or 200 k $\Omega$ . The PGA has selectable gains that result in channel gains ranging from 16 dB to 34 dB. The AAF has a three-pole elliptical response with a selectable cutoff frequency. The mux is synchronized with the ADC and automatically selects the next active channel after the ADC acquires a sample.

The signal path is fully differential throughout to maximize signal swing and reduce even-order distortion including the LNA, which is designed to be driven from a differential signal source.

### Low Noise Amplifier (LNA)

Good noise performance relies on a proprietary ultralow noise LNA at the beginning of the signal chain, which minimizes the noise contributions on the following PGA and AAF. The input impedance can be either 200  $\Omega$  or 200 k $\Omega$  and is selected through the SPI port or using the ZSEL pin.

The LNA supports differential output voltages as high as 4.0 V p-p with positive and negative excursions of  $\pm 1.0$  V from a common-mode voltage of 1.5 V. With the output saturation level fixed, the channel gain sets the maximum input signal before saturation.

Low value feedback resistors and the current driving capability of the output stage allow the LNA to achieve a low input referred noise voltage of 3.5 nV/ $\sqrt{\text{Hz}}$  at a channel gain of 34 dB. The use of a fully differential topology and negative feedback minimizes second-order distortion. Differential signaling enables smaller swings at each output, further reducing third order distortion.

### Recommendation

To achieve the best possible noise performance, it is important to match the impedances seen by the positive and negative inputs. Matching the impedances ensures that any common-mode noise is rejected by the signal path.

### Antialiasing Filter (AAF)

The filter that the signal reaches prior to the ADC is used to band limit the signal for antialiasing.

The antialiasing filter uses a combination of poles and zeros to create a third order elliptical filter. An elliptical filter is used to achieve a sharp roll-off after the cutoff frequency. The filter uses on-chip tuning to trim the capacitors to set the desired cutoff frequency. This tuning method reduces variations in the cutoff frequency due to standard IC process tolerances of resistors and capacitors. The default  $-3$  dB low-pass filter cutoff is 1/3 or 1/4 the ADC sample clock rate. The cutoff can be scaled to 0.7, 0.8, 0.9, 1, 1.1, 1.2, or 1.3 times this frequency through the SPI.

Tuning is normally off to avoid changing the capacitor settings during critical times. The tuning circuit is enabled and disabled through the SPI. Initializing the tuning of the filter must be performed after initial power-up and after reprogramming the filter cutoff scaling or ADC sample rate. Occasional retuning during an idle time is recommended to compensate for temperature drift.

A cutoff range of 1.0 MHz to 12.0 MHz is possible. An example follows:

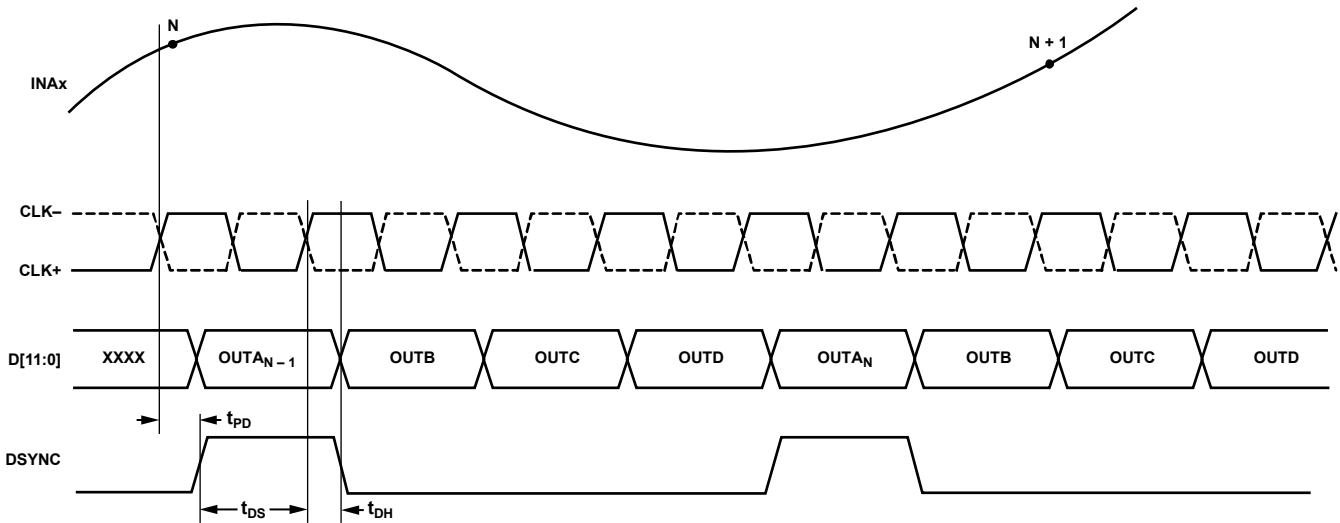
- Four channels selected: A, B, C, and AUX
- ADC clock: 30 MHz
- Per channel sample rate:  $30/4 = 7.5$  MSPS
- Default tuned cutoff frequency =  $7.5/4 = 1.88$  MHz

### Mux and Mux Controller

The mux is designed to scan through each active channel automatically. The mux remains on each channel for one clock cycle, then switches to the next active channel. The mux switching is synchronized to the ADC sampling so that the mux switching and channel settling time do not interfere with ADC sampling.

As shown in Table 9, Address 0x0C (FLEX\_MUX\_CONTROL), Channel A is usually the first converted input; the only exception occurs when Channel AUX is the sole input (see Figure 26 for the timing). Channel AUX is always the last converted input. Unselected codes place the respective channels (LNA, PGA, and filter) in power-down mode unless Address 0x0C, Bit 6 is set to 1. Figure 26 shows the timing of the clock input and data/DSYNC outputs.





NOTES

1. FOR THIS CONFIGURATION, ADDRESS 0x0C, BITS [3:0] IS SET TO 0110 (CHANNEL A, B, C, AND D ENABLED).
2. DSYNC IS ALWAYS ALIGNED WITH CHANNEL A UNLESS CHANNEL A OR CHANNEL AUX IS THE ONLY CHANNEL SELECTED, IN WHICH CASE DSYNC IS NOT ACTIVE.
3. THERE IS A SEVEN-CLOCK CYCLE LATENCY FROM SAMPLING A CHANNEL TO ITS DIGITAL DATA BEING PRESENT ON THE PARALLEL BUS PINS.

11952-006

Figure 26. Data and DSYNC Timing

ADC

The AD8285 uses a pipelined ADC architecture. The quantized output from each stage is combined into a 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on preceding samples. Sampling occurs on the rising edge of the clock. The output staging block aligns the data, corrects errors, and passes the data to the output buffers.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD8285 sample clock inputs (CLK+ and CLK-) with a differential signal. This signal is typically ac-coupled into the CLK+ and CLK- pins via a transformer or by using capacitors. These pins are biased internally and require no additional bias.

Figure 27 shows the preferred method for clocking the AD8285. A low jitter clock source, such as the Valpey Fisher oscillator VFAC3-BHL-50MHz, is converted from single ended to differential using an RF transformer. The back to back Schottky diodes across the secondary transformer limit clock excursions into the AD8285 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD8285, and it preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

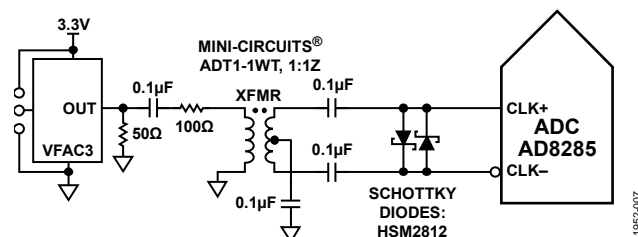
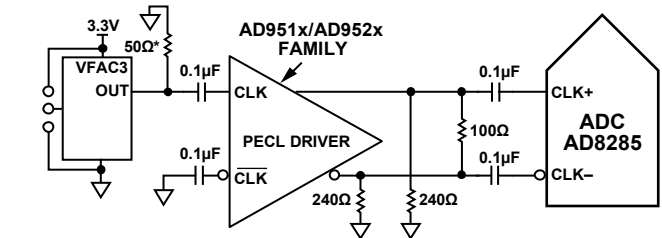


Figure 27. Transformer Coupled Differential Clock

11952-007

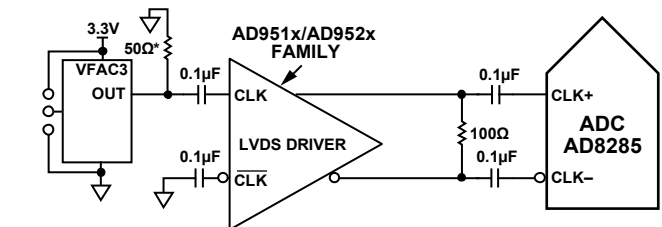
If a low jitter clock is available, another option is to ac-couple a differential PECL or LVDS signal to the sample clock input pins as shown in Figure 28 and Figure 29. The AD9515/AD9520-0 device family of clock drivers offers excellent jitter performance.



\*50Ω RESISTOR IS OPTIONAL.

Figure 28. Differential PECL Sample Clock

11952-008

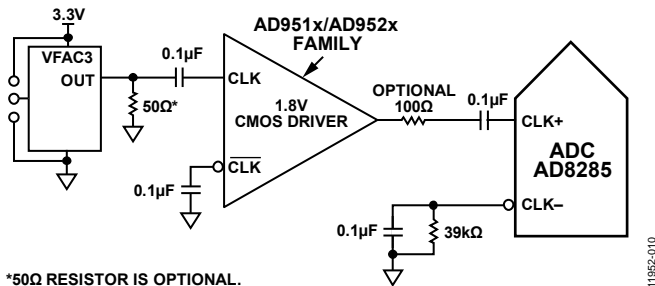


\*50Ω RESISTOR IS OPTIONAL.

Figure 29. Differential LVDS Sample Clock

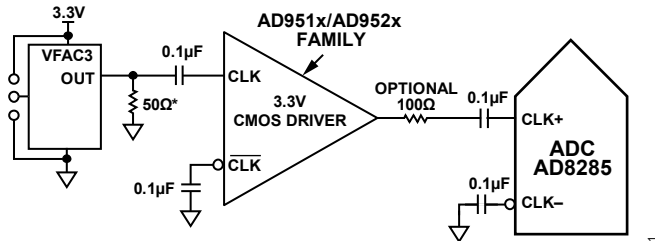
11952-009

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, drive CLK+ directly from a CMOS gate and bypass the CLK- pin to ground with a 0.1 μF capacitor in parallel with a 39 kΩ resistor (see Figure 30). Although the CLK+ input circuit supply is AVDD18, this input is designed to withstand input voltages of up to 3.3 V, making the selection of the drive logic voltage very flexible. The AD9515/AD9520-0 device family can provide 3.3 V inputs (see Figure 31). In this case, 39 kΩ resistor is not needed.



\*50Ω RESISTOR IS OPTIONAL.

Figure 30. Single-Ended 1.8 V CMOS Sample Clock



\*50Ω RESISTOR IS OPTIONAL.

Figure 31. Single-Ended 3.3 V CMOS Sample Clock

## CLOCK DUTY CYCLE CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD8285 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. The DCS allows a wide range of clock input duty cycles without affecting the performance of the AD8285.

When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operating in this mode. See Table 9 for more information about using this feature.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

## CLOCK JITTER CONSIDERATIONS

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency ( $f_A$ ) due only to aperture jitter ( $t_j$ ) can be calculated by

$$\text{SNR Degradation} = 20 \times \log_{10} [1/2 \times \pi \times f_A \times t_j]$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. Intermediate frequency undersampling applications are particularly sensitive to jitter.

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD8285. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources, such as the Valpey Fisher VFAC3 series. If the clock is generated from another type of source (by gating, dividing, or other methods), retime it by the original clock during the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about how jitter performance relates to ADCs.

## SDIO PIN

The SDIO pin is required to operate the SPI. It has an internal 30 kΩ pull-down resistor that pulls this pin low and is only 1.8 V tolerant. If applications require that this pin be driven from a 3.3 V logic level, insert a 1 kΩ resistor in series with this pin to limit the current.

## SCLK PIN

The SCLK pin is required to operate the SPI port interface. It has an internal 30 kΩ pull-down resistor that pulls this pin low and is both 1.8 V and 3.3 V tolerant.

## $\overline{\text{CS}}$ PIN

The  $\overline{\text{CS}}$  pin is required to operate the SPI port interface. It has an internal 70 kΩ pull-up resistor that pulls this pin high and is both 1.8 V and 3.3 V tolerant.

## RBIAS PIN

To set the internal core bias current of the ADC, place a resistor nominally equal to 10.0 kΩ to ground at the RBIAS pin. Using anything other than the recommended 10.0 kΩ resistor for RBIAS degrades the performance of the device. Therefore, it is imperative that at least a 1.0% tolerance on this resistor be used to achieve consistent performance.

## VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the [AD8285](#). This is gained up internally by a factor of 2, setting VREF to 1.024 V, which results in a full-scale differential input span of 2.0 V p-p for the ADC. VREF is set internally by default, but the VREF pin can be driven externally with a 1.0 V reference to achieve more accuracy. However, this device does not support ADC full-scale ranges below 2.0 V p-p.

When applying the decoupling capacitors to the VREF pin, use ceramic low ESR capacitors. These capacitors must be close to the reference pin and on the same layer of the printed circuit board (PCB) as the [AD8285](#). The VREF pin must have both a 0.1  $\mu\text{F}$  capacitor and a 1  $\mu\text{F}$  capacitor connected in parallel to the analog ground. These capacitor values are recommended for the ADC to properly settle and acquire the next valid sample.

## POWER AND GROUND RECOMMENDATIONS

When connecting power to the [AD8285](#), it is recommended that two separate 1.8 V supplies and two separate 3.3 V supplies be used: one supply each for analog 1.8 V (AVDD18x), digital 1.8 V (DVDD18x), analog 3.3 V (AVDD33x), and digital 3.3 V (DVDD33x). If only one supply is available for both analog and digital, for example, AVDD18x and DVDD18x, route the supply to the AVDD18x first and then tap off and isolate it with a ferrite bead or a filter choke preceded by decoupling capacitors for the DVDD18x. The same is true for the analog and digital 3.3 V supplies.

Use several decoupling capacitors on all supplies to cover both high and low frequencies. Locate these capacitors close to the point of entry at the PCB level and close to the device, with minimal trace lengths.

When using the [AD8285](#), a single PCB ground plane is sufficient. With proper decoupling and smart partitioning of the analog, digital, and clock sections of the PCB, optimum performance can be achieved easily.

## EXPOSED PADDLE THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed paddle on the underside of the device be connected to a quiet analog ground to achieve the best electrical and thermal performance of the [AD8285](#). Mate an exposed continuous copper plane on the PCB to the [AD8285](#) exposed paddle, Pin 0. The copper plane must have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. Fill or plug these vias with nonconductive epoxy.

To maximize the coverage and adhesion between the device and the PCB, partition the continuous copper pad by overlaying a silkscreen or solder mask to divide the copper pad into several uniform sections. Dividing the copper pad ensures several tie points between the PCB and the EPAD during the reflow process. Using one continuous plane with no partitions only guarantees one tie point between the [AD8285](#) and the PCB. For more detailed information on packaging, and for more PCB layout examples, see the [AN-772 Application Note](#).

## SERIAL PERIPHERAL INTERFACE (SPI)

The AD8285 serial peripheral interface allows the user to configure the signal chain for specific functions or operations through a structured register space provided inside the chip. The SPI offers added flexibility and customization depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, as documented in the Memory Map section. Detailed operational information can be found in the [AN-877 Application Note, Interfacing to High Speed ADCs via SPI](#).

Three pins define the serial peripheral interface (SPI): SCLK, SDIO, and  $\overline{\text{CS}}$ . The SCLK (serial clock) pin is used to synchronize the read and write data presented to the device. The SDIO (serial data input/output) pin is a dual purpose pin that allows data to be sent to and read from the internal memory map registers of the device. The  $\overline{\text{CS}}$  (chip select bar) pin is an active low control that enables or disables the read and write cycles (see Table 7).

**Table 7. Serial Port Pins**

| Pin                    | Function   |
|------------------------|--|
| SCLK                   | Serial clock. The serial shift clock input. SCLK is used to synchronize serial interface reads and writes.   |
| SDIO                   | Serial data input/output. A dual-purpose pin. The typical role for this pin is as an input or output, depending on the instruction sent and the relative position in the timing frame. |
| $\overline{\text{CS}}$ | Chip select bar (active low). This control gates the read and write cycles.  |

The falling edge of the  $\overline{\text{CS}}$  in conjunction with the rising edge of the SCLK determines the start of the framing sequence. During an instruction phase, a 16-bit instruction is transmitted, followed by one or more data bytes, which is determined by Bit Field W0 and Bit Field W1. An example of the serial timing and its definitions can be found in Figure 32 and Table 8.

In normal operation,  $\overline{\text{CS}}$  signals to the device that SPI commands are to be received and processed. When  $\overline{\text{CS}}$  is brought low, the device processes SCLK and SDIO to process instructions. Normally,  $\overline{\text{CS}}$  remains low until the communication cycle is complete. However, if connected to a slow device,  $\overline{\text{CS}}$  can be brought high between bytes, allowing older microcontrollers enough time to transfer data into shift registers.  $\overline{\text{CS}}$  can be stalled when transferring one, two, or three bytes of data. When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until  $\overline{\text{CS}}$  is taken high to end the communication cycle. This allows complete memory transfers without having to provide additional instructions.

Regardless of the mode, if  $\overline{\text{CS}}$  is taken high in the middle of any byte transfer, the SPI state machine is reset, and the device waits for a new instruction.

In addition to the operation modes, the SPI port can be configured to operate in different modes. For applications that do not require a control port, the  $\overline{\text{CS}}$  line can be tied and held high. This places the remainder of the SPI pins in their secondary mode, as is defined in the SDIO Pin section and the SCLK Pin section. The  $\overline{\text{CS}}$  pin can also be tied low to enable 2-wire mode. When  $\overline{\text{CS}}$  is tied low, SCLK and SDIO are the only pins required for communication. Although the device is synchronized during power-up, caution must be exercised when using this mode to ensure that the serial port remains synchronized with the  $\overline{\text{CS}}$  line. When operating in 2-wire mode, it is recommended to use a 1-, 2-, or 3-byte transfer exclusively. Without an active  $\overline{\text{CS}}$  line, streaming mode can be entered but not exited.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip and read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB- or LSB-first mode. MSB-first mode is the default at power-up and can be changed by adjusting the configuration register. For more information about this and other features, see the [AN-877 Application Note, Interfacing to High Speed ADCs via SPI](#).

### HARDWARE INTERFACE

The pins described in Table 7 constitute the physical interface between the programming device of the user and the serial port of the AD8285. The SCLK and  $\overline{\text{CS}}$  pins function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

This interface is flexible enough to be controlled by either serial PROMs or PIC microcontrollers. This flexibility provides the user with an alternative method, other than a full SPI controller, for programming the device (see the [AN-812 Application Note](#)).

If the user chooses not to use the SPI interface, these pins serve a dual function and are associated with secondary functions when the  $\overline{\text{CS}}$  is strapped to AVDD33 during device power-up. See the SDIO Pin section and SCLK Pin section for details on which pin strappable functions are supported on the SPI pins.

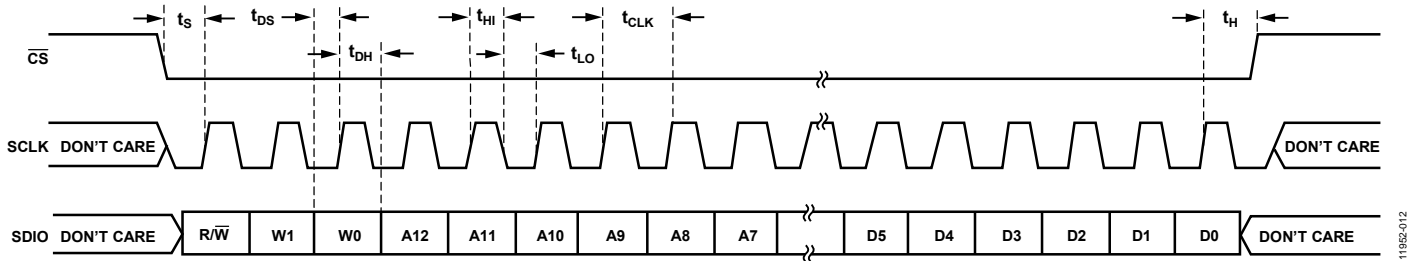


Figure 32. Serial Timing Details

Table 8. Serial Timing Definitions

| Parameter       | Minimum Timing (ns) | Description   |
|-----------------|---------------------|---|
| $t_{DS}$        | 5                   | Setup time between the data and the rising edge of SCLK   |
| $t_{DH}$        | 2                   | Hold time between the data and the rising edge of SCLK  |
| $t_{CLK}$       | 40                  | Period of the clock   |
| $t_s$           | 5                   | Setup time between $\overline{CS}$ and SCLK   |
| $t_h$           | 2                   | Hold time between $\overline{CS}$ and SCLK  |
| $t_{HI}$        | 16                  | Minimum period that SCLK should be in a logic high state  |
| $t_{LO}$        | 16                  | Minimum period that SCLK should be in a logic low state   |
| $t_{EN\_SDIO}$  | 10                  | Minimum time for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 32) |
| $t_{DIS\_SDIO}$ | 10                  | Minimum time for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 32)  |

## MEMORY MAP

### READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into three sections: the chip configuration registers map (Address 0x00 and Address 0x01), the device index and transfer registers map (Address 0x05 and Address 0xFF), and the ADC channel functions registers map (Address 0x04 and Address 0x08 to Address 0x2C).

The leftmost column of the memory map indicates the address (hex) number, and the default value is shown in the second rightmost column. The Bit 7 (MSB) column is the start of the default hexadecimal value given. For example, Address 0x09, the GLOBAL\_CLOCK register, has a default value of 0x01, meaning that Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. This setting is the default for the duty cycle stabilizer in the on condition. By writing a 0 to Bit 0 of this address followed by a 0x01 to the SW transfer bit in Register 0xFF, the duty cycle stabilizer turns off. It is important to follow each writing sequence with a write to the SW transfer bit to update the SPI registers.

Note that all registers except Register 0x00, Register 0x04, Register 0x05, and Register 0xFF are buffered with a master slave latch and require writing to the transfer bit. For more information on this and other functions, consult the [AN-877 Application Note, Interfacing to High Speed ADCs via SPI](#).

### LOGIC LEVELS

An explanation of various registers follows: “bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.” Similarly, “clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

### RESERVED LOCATIONS

Do not write to undefined memory locations except when writing the default values suggested in this data sheet. Consider addresses marked as 0 as reserved, and these addresses must have a 0 written into their registers during power-up.

### DEFAULT VALUES

After a reset, critical registers are automatically loaded with default values. These values are indicated in Table 9, where an X refers to an undefined feature.

Table 9. Memory Map Register

| Addr. (Hex)                         | Register Name    | Bit 7 (MSB)                                    | Bit 6   | Bit 5                                 | Bit 4 | Bit 3   | Bit 2                                     | Bit 1   | Bit 0 (LSB)                                      | Default Value  | Default Notes/ Comments  |
|-------------------------------------|------------------|--|---|---------------------------------------|-------|---|---|---|--|--|--|
| Chip Configuration Registers        |                  |  |   |                                       |       |   |   |   |  |  |  |
| 0x00                                | CHIP_PORT_CONFIG | 0  | LSB first, 1 = on, 0 = off, (default)                                     | Soft reset, 1 = on, 0 = off (default) | 1     | 1   | Soft reset, 1 = on, 0 = off (default)     | LSB first, 1 = on, 0 = off (default)  | 0  | 0x18   | Mirror the nibbles so that LSB- or MSB-first mode is set correct regardless of shift mode. |
| 0x01                                | CHIP_ID          | Chip ID, Bits[7:0]<br>(AD8285 = 0xA2, default) |   |                                       |       |   |   |   |  | Read only  | The default value is the chip ID assigned to the AD8285. This is a read-only register.     |
| Device Index and Transfer Registers |                  |  |   |                                       |       |   |   |   |  |  |  |
| 0x05                                | DEVICE_INDEX     | X  | X   | X                                     | X     | Data Channel D, 1 = on (default), 0 = off   | Data Channel C, 1 = on (default), 0 = off | Data Channel B, 1 = on (default), 0 = off   | Data Channel A, 1 = on (default), 0 = off        | 0x0F   | Bits are set to determine which on-chip device receives the next write command.            |
| 0xFF                                | DEVICE_UPDATE    | X  | X   | X                                     | X     | X   | X   | X   | SW transfer, 1 = on, 0 = off (default)           | 0x00   | Synchronously transfers data from the master shift register to the slave.                  |
| Channel Functions Registers         |                  |  |   |                                       |       |   |   |   |  |  |  |
| 0x04                                | FLEX_RES         | X  | X   | X                                     | X     | X   | X   | Reserved  | Reserved   | 0x0F   | Reserved. Bits must be set to 0x00.  |
| 0x08                                | GLOBAL_MODES     | X  | X   | X                                     | X     | X   | X   | Internal power-down mode, 00 = chip run (default), 01 = full power-down, 11 = reset |  | 0x00   | Determines the power-down mode (global).   |
| 0x09                                | GLOBAL_CLOCK     | X  | X   | X                                     | X     | X   | X   | X   | Duty cycle stabilizer, 1 = on (default), 0 = off | 0x01   | Turns the internal duty cycle stabilizer on and off (global).                              |
| 0x0C                                | FLEX_MUX_CONTROL | X  | Power-down of unused channels, 0 = PD (power-down; default), 1 = power-on | X                                     | X     | Mux input active channels, 0000 = A, 0001 = AUX, 0010 = A and B, 0011 = A and AUX, 0100 = A, B, and C, 0101 = A, B, and AUX, 0110 = A, B, C, and D, 0111 = A, B, C, and AUX |   |   | 0x00   | Selects the mux input channels to use and specifies whether to power down unused channels. |  |

| Addr. (Hex) | Register Name      | Bit 7 (MSB)  | Bit 6 | Bit 5   | Bit 4   | Bit 3  | Bit 2  | Bit 1   | Bit 0 (LSB) | Default Value                        | Default Notes/Comments   |
|-------------|--------------------|--|-------|---|---|--|--|---|-------------|--------------------------------------|--|
| 0x0D        | FLEX_TEST_IO       | User test mode, 00 = off (default), 01 = on, single alternate, 10 = on, single once, 11 = on, alternate once   |       | Reset PN long gen, 1 = on, 0 = off (default)  | Reset PN short gen, 1 = on, 0 = off (default) | Output test mode—see Table 10, 0000 = off (default), 0001 = midscale short, 0010 = +full-scale short, 0011 = –full-scale short, 0100 = checkerboard output, 0101 = PN sequence long, 0110 = PN sequence short, 0111 = one-/zero-word toggle, 1000 = user input, 1001 = 1-bit/0-bit toggle, 1010 = 1× sync, 1011 = one bit high, 1100 = mixed bit frequency (format determined by the OUTPUT_MODE register) |  |   |             | 0x00                                 | When this register is set, the test data is placed on the output pins in place of normal data (local, except for PN sequence).                                       |
| 0x0F        | FLEX_CHANNEL_INPUT | Filter cutoff frequency control, 0000 = $1.3 \times 1/4 \times f_{\text{SAMPLECH}}$ , 0001 = $1.2 \times 1/4 \times f_{\text{SAMPLECH}}$ , 0010 = $1.1 \times 1/4 \times f_{\text{SAMPLECH}}$ , 0011 = $1.0 \times 1/4 \times f_{\text{SAMPLECH}}$ (default), 0100 = $0.9 \times 1/4 \times f_{\text{SAMPLECH}}$ , 0101 = $0.8 \times 1/4 \times f_{\text{SAMPLECH}}$ , 0110 = $0.7 \times 1/4 \times f_{\text{SAMPLECH}}$ , 0111 = not applicable, 1000 = $1.3 \times 1/3 \times f_{\text{SAMPLECH}}$ , 1001 = $1.2 \times 1/3 \times f_{\text{SAMPLECH}}$ , 1010 = $1.1 \times 1/3 \times f_{\text{SAMPLECH}}$ , 1011 = $1.0 \times 1/3 \times f_{\text{SAMPLECH}}$ , 1100 = $0.9 \times 1/3 \times f_{\text{SAMPLECH}}$ , 1101 = $0.8 \times 1/3 \times f_{\text{SAMPLECH}}$ , 1110 = $0.7 \times 1/3 \times f_{\text{SAMPLECH}}$ , 1111 = not applicable |       |   |   | X  | X  | X   | X           | 0x30                                 | Low-pass filter cutoff (global). $f_{\text{SAMPLECH}}$ = ADC sample rate/ number of active channels. Note that the absolute range is limited to 1.0 MHz to 12.0 MHz. |
| 0x10        | FLEX_OFFSET        | X  | X     | 6-bit LNA offset adjustment, 00 0000 for LNA bias high, 01 1111 for LNA mid to high, 10 0000 for LNA mid to low (default), 10 0001 for LNA bias low |   |  |  |   | 0x20        | LNA force offset correction (local). |  |
| 0x11        | FLEX_GAIN_1        | X  | X     | X   | X   | X  | 010 = 16 dB (default), 011 = 22 dB, 100 = 28 dB, 101 = 34 dB |   |             | 0x02                                 | Total LNA + PGA gain adjustment (local)  |
| 0x12        | FLEX_BIAS_CURRENT  | X  | X     | X   | X   | X  | X  | LNA bias, 00 = high, 01 = mid to high (default), 10 = mid to low, 11 = low          |             | 0x09                                 | LNA bias current adjustment (global).  |
| 0x14        | FLEX_OUTPUT_MODE   | X  | X     | X   | X   | X  | 1 = output invert (local)                                    | 0 = offset binary (default), 1 = twos complement (global)                           |             | 0x00                                 | Configures the outputs and the format of the data.   |
| 0x15        | FLEX_OUTPUT_ADJUST | 0 = enable Data Bits[11:0], 1 = disable Data Bits[11:0]  | X     | X   | X   | Typical output rise time and fall time, respectively 00 = 2.6 ns, 3.4 ns 01 = 1.1 ns, 1.6 ns 10 = 0.7 ns, 0.9 ns 11 = 0.7 ns, 0.7 ns (default)   |  | Typical output drive strength 00 = 45 mA 01 = 30 mA 10 = 60 mA 11 = 60 mA (default) |             | 0x0F                                 | Used to adjust output rise and fall times and select output drive strength, limiting the noise added to the channels by output switching.                            |



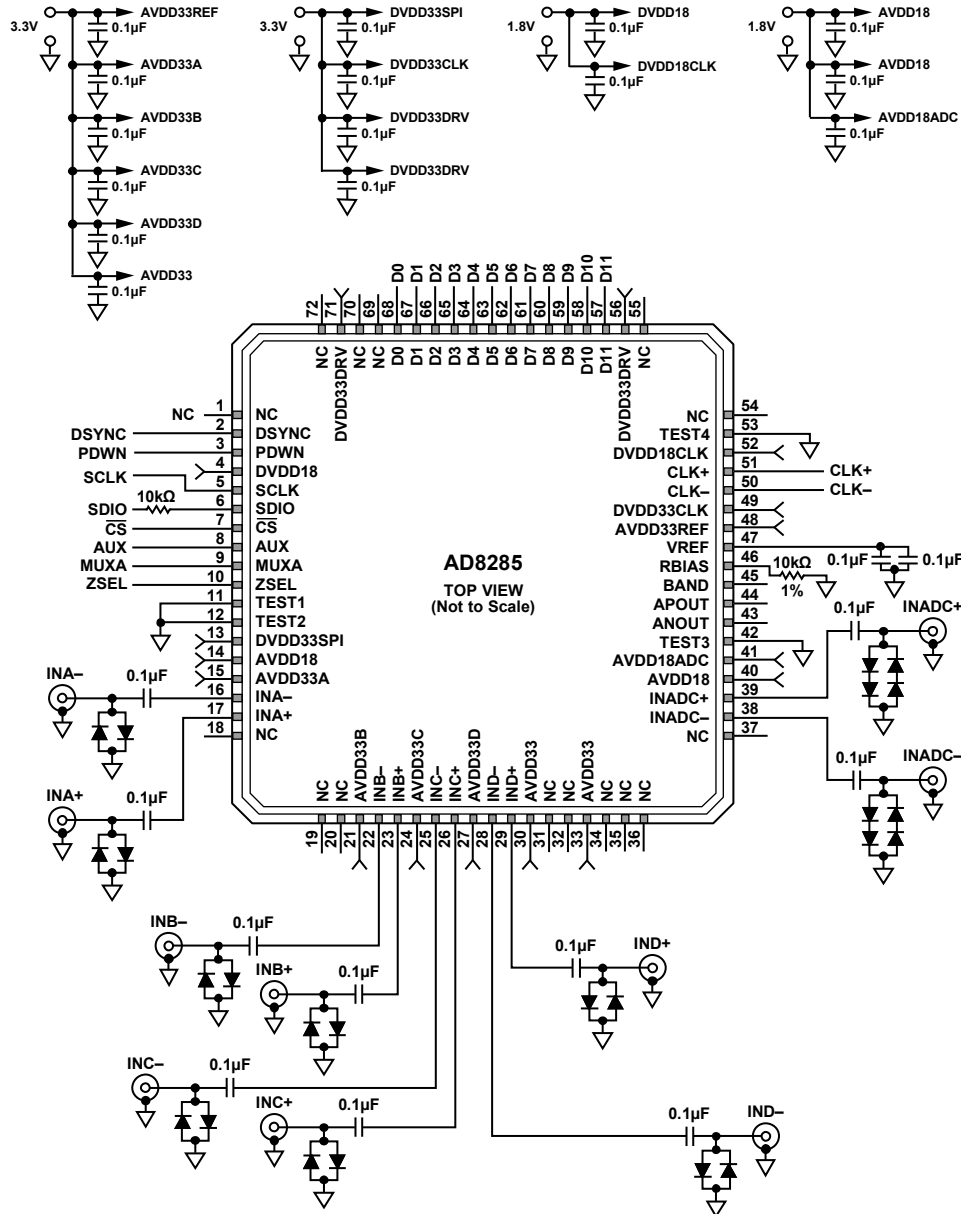
| Addr. (Hex) | Register Name       | Bit 7 (MSB) | Bit 6  | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1  | Bit 0 (LSB)                                    | Default Value | Default Notes/Comments   |
|-------------|---------------------|-------------|--|-------|-------|-------|-------|--|--|---------------|--|
| 0x18        | FLEX_VREF           | X           | 0 = internal reference, 1 = external reference           | X     | X     | X     | X     | 00 = 0.625 V, 01 = 0.750 V, 10 = 0.875 V, 11 = 1.024 V (default) |  | 0x03          | Select internal reference (recommended default) or external reference (global); adjust internal reference. |
| 0x19        | FLEX_USER_PATT1_LSB | B7          | B6   | B5    | B4    | B3    | B2    | B1   | B0   | 0x00          | User-defined Pattern 1, LSB  |
| 0x1A        | FLEX_USER_PATT1_MSB | B15         | B14  | B13   | B12   | B11   | B10   | B9   | B8   | 0x00          | User-defined Pattern 1, MSB  |
| 0x1B        | FLEX_USER_PATT2_LSB | B7          | B6   | B5    | B4    | B3    | B2    | B1   | B0   | 0x00          | User-defined Pattern 2, LSB  |
| 0x1C        | FLEX_USER_PATT2_MSB | B15         | B14  | B13   | B12   | B11   | B10   | B9   | B8   | 0x00          | User-defined Pattern 2, MSB  |
| 0x2B        | FLEX_FILTER         | X           | Enable automatic low-pass tuning, 1 = on (self-clearing) | X     | X     | X     | X     | X  | X  | 0x00          | Refer to the Antialiasing Filter (AAF) section.  |
| 0x2C        | CH_IN_IMP           | X           | X  | X     | X     | X     | X     | X  | 0 = 200 $\Omega$ (default), 1 = 200 k $\Omega$ | 0x00          | Input impedance adjustment (global).   |

Table 10. Flexible Output Test Modes

| Output Test Mode Bit Sequence | Pattern Name          | Digital Output Word 1          | Digital Output Word 2          | Subject to Data Format Select |
|-------------------------------|-----------------------|--------------------------------|--------------------------------|-------------------------------|
| 0000                          | Off (default)         | Not applicable                 | Not applicable                 | Not applicable                |
| 0001                          | Midscale short        | 1000 0000 0000                 | Same                           | Yes                           |
| 0010                          | +Full-scale short     | 1111 1111 1111                 | Same                           | Yes                           |
| 0011                          | -Full-scale short     | 0000 0000 0000                 | Same                           | Yes                           |
| 0100                          | Checkerboard output   | 1010 1010 1010                 | 0101 0101 0101                 | No                            |
| 0101                          | PN sequence long      | Not applicable                 | Not applicable                 | Yes                           |
| 0110                          | PN sequence short     | Not applicable                 | Not applicable                 | Yes                           |
| 0111                          | One-/zero-word toggle | 1111 1111 1111                 | 0000 0000 0000                 | No                            |
| 1000                          | User input            | Register 0x19 to Register 0x1A | Register 0x1B to Register 0x1C | No                            |
| 1001                          | 1-bit/0-bit toggle    | 1010 1010 1010                 | Not applicable                 | No                            |
| 1010                          | 1 $\times$ sync       | 0000 0011 1111                 | Not applicable                 | No                            |
| 1011                          | One bit high          | 1000 0000 0000                 | Not applicable                 | No                            |
| 1100                          | Mixed bit frequency   | 1010 0011 0011                 | Not applicable                 | No                            |

# APPLICATION DIAGRAMS

The typical application diagrams for the AD8285 are shown in Figure 33 and Figure 34. As discussed in the Channel Overview section, the maximum signal swing and the minimum third-order distortion can be achieved when the AD8285 is driven with a fully differential source. The typical connections for this configuration are shown in Figure 33.

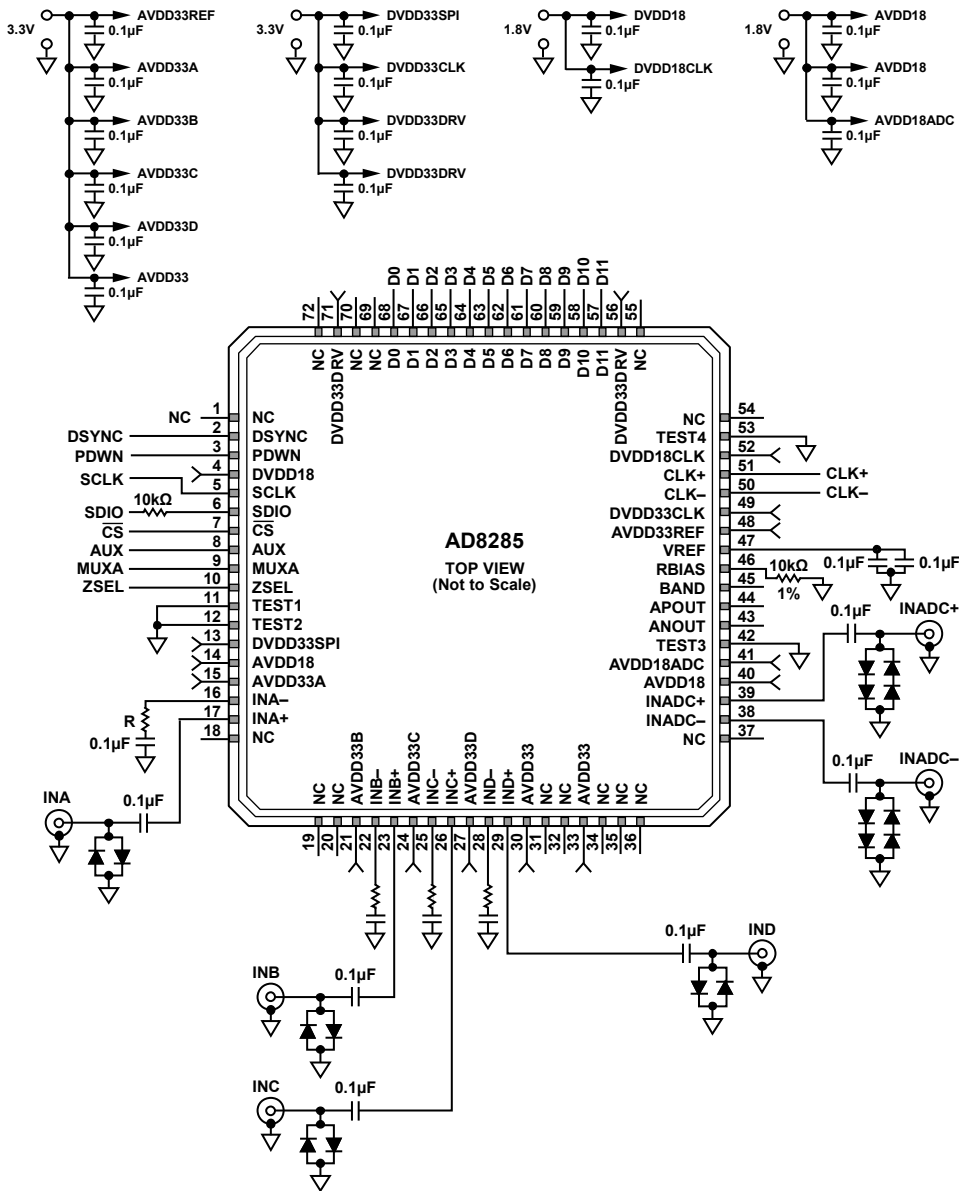


- NOTES**  
 1. ALL CAPACITORS FOR SUPPLIES AND REFERENCES MUST BE PLACED CLOSE TO THE DEVICE.

Figure 33. Differential Inputs Application Diagram

11952-029

The AD8285 can also be driven with a single-ended source, as shown in Figure 34. In this configuration, the negative analog input of each channel is grounded through a resistor and a 0.1 μF capacitor. For optimal operation, this resistor must match the output impedance of the input driver.



- NOTES
1. RESISTOR R (IN<sub>x</sub>- INPUTS) MUST MATCH THE OUTPUT IMPEDANCE OF THE INPUT DRIVER.
  2. ALL CAPACITORS FOR SUPPLIES AND REFERENCES SHOULD BE PLACED CLOSE TO THE DEVICE.

Figure 34. Single-Ended Inputs Application Diagram

11952-100

## OUTLINE DIMENSIONS

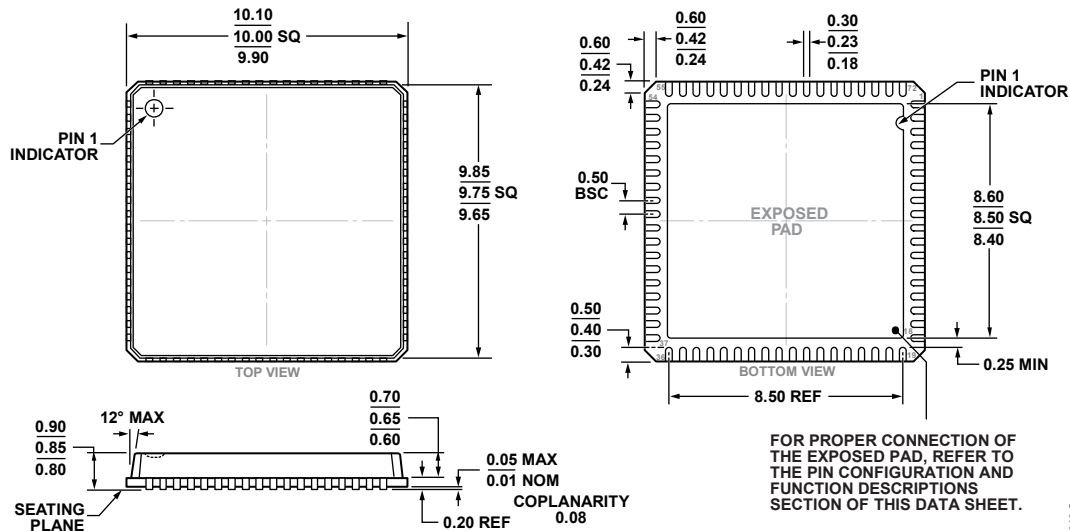


Figure 35. 72-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
10 mm × 10 mm Body, Very Thin Quad  
(CP-72-5)  
Dimensions shown in millimeters

## ORDERING GUIDE

| Model <sup>1,2</sup> | Temperature Range | Package Description                 | Package Option |
|----------------------|-------------------|-------------------------------------|----------------|
| AD8285WBCPZ-RL       | -40°C to +105°C   | 72-Lead LFCSP_VQ, 13" Tape and Reel | CP-72-5        |
| AD8285WBCPZ          | -40°C to +105°C   | 72-Lead LFCSP_VQ                    | CP-72-5        |
| AD8285CP-EBZ         |                   | Evaluation Board                    |                |

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> W = Qualified for Automotive Applications.

## AUTOMOTIVE PRODUCTS

The [AD8285WBCPZ](#) models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.