Modeling Method and Design Optimization for a Soft-Switched DC-DC Converter

Liang Jia, *Member, IEEE*, Srikanth Lakshmikanthan, Xin Li, and Yan-Fei Liu, *Fellow, IEEE*

***Abstract* –High performance cloud computing enables many key future technologies such as artificial intelligence (AI), self-driving vehicle, big data analysis, and the internet of things (IoT), using clustered CPU and GPU servers in the datacenter. To improve the power efficiency and the infrastructure flexibility, the computing industry is adopting 54VDC to power the servers in the open compute racks. In this paper, a new modeling technique for a soft-switched DC-DC converter is presented and suitable to guide optimal design in different applications, for example, 54V to point-of-load (PoL) for the new open compute rack. To improve the model accuracy and reduce the complexity, this paper proposes a reduced order linear differential equation (LDE) based modeling technique to discover 1) the tank resonance involving the output inductor; 2) output current ripple and its impact on power efficiency; 3) the proper on-time control for soft switching; 4) unique bleeding mode under the heavy load; 5) output power capability of the converter; and 6) component tolerance analysis and impact on the performance of the converter. With the power loss estimation, design guideline is provided for a reference design and design improvement based on this new modeling technique. Using the proposed method, great accuracy can be expected in the efficiency estimation. Simulation and experimental results are provided to verify the modeling technique in a 54V-1.2V 25A DC-DC converter prototype.**

***Index Terms*—Converter Modeling, DC-DC Converter, Soft Switching, Open Compute Project**

I. Introduction

One of the popular trends for powering high performance datacenter is to supply the high power demanding workload servers with 54VDC from the open compute racks [1][2][3], taking advantage of lower distribution losses and rack configuration flexibility. While the front-end stage of an AC-DC rectifier achieves power factor correction and regulates the bus voltage to a DC value on the rack busbar (54V typical, the voltage range will be 40V-60V [1], considering regulation tolerance and battery backup mode), DC-DC step-down stage(s) will be required to further convert this bus voltage (and provide galvanic isolation, preferably) to point-of-load (PoL) voltage level, for example 1V.

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Due to the large conversion ratio from 54V-PoL (~1V), two stage designs were conventionally and commonly used, where the first stage will convert 54VDC from the rack to an intermediate bus voltage (often based on LLC resonant or PWM full bridge converter [4][5][6]), for example, 12VDC, and the second stage will be single or multiphase Buck converter to power the PoL from the 12VDC input [10]-[16]. The overall efficiency is limited by the multiplication of the efficiency of the two stages, especially at light load and maximum load [2][17]. New high efficiency two-stage design was proposed in [7][8], where the first stage (PRM) regulates the intermediate bus with ZVS Buck-Boost converter, while the second stage (VTM) runs fixed ratio LLC resonant converter as a DC transformer. However, major drawbacks are 1) no phase shedding for light load efficiency; 2) no sinking capability for dynamic voltage identification (VID) down in CPU VR application due to the ZVS control of PRM; 3) not flexible for power scaling and roughly 100W is the minimum power granularity available and 4) non-isolated design (if isolation is preferred or required).

Recently one stage direct power conversion from 54V-PoL attracts more and more interests to resolve the issues of the two-stage design. A wide range of isolated topologies is available for the high conversion ratio DC-DC application. Firstly, LLC resonant converter could offer good efficiency, however, the input and output voltage variation might compromise the tank optimization and also the dynamic response is a big challenge with the conventional voltage mode control even with improved charge control [20]-[27].

Secondly, zero voltage switching (ZVS) phase shift full bridge (PSFB) can be used in such applications and the current doubler configuration is suitable for high current output especially [28][29]. In Figure 1, it shows the PSFB converter schematic, switches A and B are switched complementary with 50% duty cycle minus a short dead time, and the same condition applies for switches C and D. The PWM signals for switches and key waveform of the converter are shown on the right side of Figure 1. Phase shift control between the two switches pairs A, B and C, D is used for output voltage regulation. L_k is the total leakage inductance of the transformer plus external inductance if any to achieve ZVS in a certain load range [28][29]. SR1 and SR2 are the synchronous rectification FETs. *L1* and *L2* are the output filter inductors to form the current double configuration. The output DC voltage is V_o.

There are a few limitations of ZVS-PSFB [28][29]:

1) Limited and load dependent ZVS range

In order to achieve ZVS on the primary side, leakage inductance L_k energy is required to fully charge/discharge the switching node of each of the legs before the switching on of

the particular FET. Most of the time the switches C and D have more leakage energy due to the involvement of output inductor. But depending on the output load condition, the primary side current i_p is varying, when switches A and B are turning on (at t_0 and t_4). Switches A and B may lose the ZVS turn on, especially at light load. So, in order to maximize the ZVS range at light load, the leakage energy has to be increased at all times, usually resulting in low conversion efficiency.

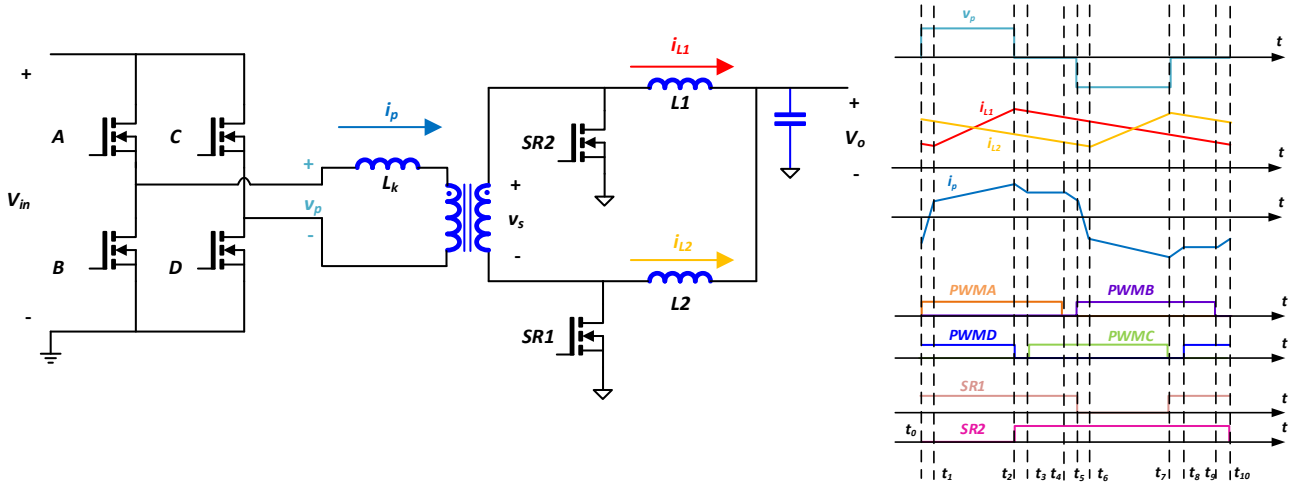

Figure 1 PSFB Converter Schematic

signal for SR in PSFB converter discussed in [28] is duplicated from the primary side gate drive signal (with some fixed propagation delay in gate signal transformer and gate driver), so the body diode is forced to conduct freewheeling current during the operation. The ideal SR driving signal is shown in Figure 1 and some improved PSFB controllers (such as [30]) have dedicated control output signal to implement the proper SR driving to minimize the body diode conduction for better efficiency.

3) Reverse Recovery of SR

In PSFB current doubler converter, when the SR turns off, the freewheeling current will be forced to stop with a high *dv/dt*. Reverse recovery of the SR can be seen and losses will occur as well [31][32]. In even worse situation for high voltage applications, if the *dv/dt* is too high, the induced current $I = C_{db}\frac{dv}{dt}$ or the magnitude of the reverse recovery current passing through R_b is sufficiently large to cause injection across the *p*-body /*n*+ source junction (in Figure 2), the parasitic bipolar transistor may become active. This uncontrolled state of operation usually results in the destruction of the device.

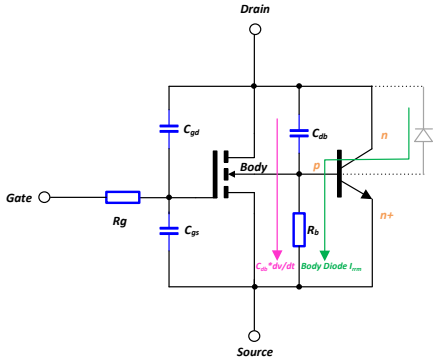

Figure 2 MOSFET simplified structure

2) Secondary SR driving

The reason of using SR to replace diode for high current application is to reduce the high conduction losses of the diode (caused by forward voltage V_f drop). However, the body diode of the FET is not designed for high switching/transient current. So, if the SR is not driven properly and forces the body diode to conduct current for an unnecessary period of time, the efficiency will suffer [28][29]. The conventional gate drive

Thirdly, a half bridge current doubler is proposed in [35] and a full bridge current doubler is mentioned in [36] for 54V-PoL application. The transformer is used for achieving high step-down ratio and isolation. However, the switches of these two topologies suffer from hard switching, resulting in higher switching losses and EMI. So, the switching frequency of the topologies will be limited, as well as the power density, resulting in bigger size of the solution, non-ideal placement on the motherboard and possibly higher power delivery losses. Another limitation for the implementation in [35] is that the output current capability cannot be scaled up by paralleling multiple cells to support higher current demanding payloads.

Also, non-isolated topologies are studied for 54V-PoL direct conversion. For example, in [37] a synchronous Buck converter using GaN FET is studied for a very high ratio step-down power conversion. Due to the super high switching speed of the GaN FET technology, the narrow duty cycle can be achieved. However, the efficiency is still lower compared with a transformer based Buck derived converter. Also, the dynamic performance will be very limited especially for unloading transient, because of the small duty cycle and high conversion ratio. In [38], a sigma converter concept was proposed with a fixed ratio converter and a regulated DC-DC converter (for example Buck converter) stacking up with each other. Ideally, the fixed ratio converter will process all the power efficiently without enabling the regulated converter. However, due to the input range is 40~60 V, the regulated converter will always process a fraction of the total power. Another concern for using the non-isolated converter in data center application is the grounding loop and current between multiple server trays. If an isolated topology can achieve similar or better efficiency, it will be highly preferred.

A new quasi-resonant PSFB converter with constant on-time (COT) control is studied in this paper and with the help

of the secondary side driver, the aforementioned limitations of the conventional PSFB are mitigated.

In this section, DC-DC converters for high down-conversion ratio are reviewed for datacenter application. And the brief review of the conventional phase shift full bridge converter will form the baseline for the future sections to demonstrate the advantages of the new topology with quasi-resonant switching to achieve ZVS or ZVZCS for the primary and secondary switches for superior power efficiency.

This paper is organized as follows. In section II, the operation principles are reviewed for the fundamental of the converter modeling. And due to the unique way of achieving secondary side ZVZCS for the SR and COT control, light and heavy loading conditions are discussed separately. In section III, the issue of the existing technique of modeling is outlined and limitations are highlighted. Equivalent circuits are built for different modes in the quasi-resonant PSFB converter using the proposed method. Design examples are provided in section IV using the proposed modeling technique for a reference design and a design improvement. In section V, simulation and experimental results are demonstrated to verify the modeling. Finally, the conclusion will be drawn.

II. THE PRINCIPLES OF OPERATION OF QUASI-RESONANT PSFB CURRENT DOUBLER

In this section, the basic operations of quasi-resonant PSFB are discussed under light and heavy loading conditions. Unique modes are highlighted and compared with conventional PSFB. And this section provides the fundamental for the proposed modeling method in section III.

A. Quasi-Resonant (QR) PSFB Current Doubler System Implementation

In the system diagram shown in Figure 3, the implementation is outlined. There are three chips within the controller scheme: primary full bridge gate driver, secondary side SR gate driver and the main digital controller. The controller is on the secondary side to improve the transient response performance and sends PWM signals *PWM_AB* and *PWM_CD* to primary side driver via a digital isolator. And the primary side driver outputs *PWM_AB_p* and *PWM_CD_p* to drive the FB. Telemetry information from the primary side will be sent back to the main controller via the digital isolator. The main digital controller also sends *Enable* signal to secondary side gate driver to start detecting zero current and zero voltage events. Output current and voltage will be sensed directly on the secondary side. The control algorithm is constant on-time (COT) control, and the switching frequency will be changed for output voltage regulation. The outstanding difference between this QR-PSFB and the conventional PSFB converter is the resonant capacitor C_{res} added on the secondary side.

B. Basic Operating Modes

In this section, basic modes are discussed for the QR-PSFB topology with COT control and ZVZCS detection using the secondary side SR to highlight the advantages of the new converter. Different modes are defined based on the equivalent circuits and the same mode will have the same equivalent circuit. Key waveforms with timing definitions are shown in Figure 4 and Figure 10 under light load and heavy load conditions. Under light load, there will be two Mode 1 durations, while under heavy load, there is only one Mode 1 duration. For reference in both figures, the waveforms when I_o=0 are shown in solid lines. In order to achieve ZVS on the primary side, the basic condition of i_{park}>0 and t_{shift}>t_{res} has to be met, where i_{park} is called parking current when Mode 1 starts, t_{res} is the resonant period and t_{shift} is the constant on time.

When the output has no loading, the time taken for the i_{res_sec} to reach the i_{L1} level is defined as σ_0 in Figure 4. In steady state, the positive and negative parking current +i_{park} and -i_{park} should have the same absolute value. And the equation (1) is valid in steady state when I_o=0.

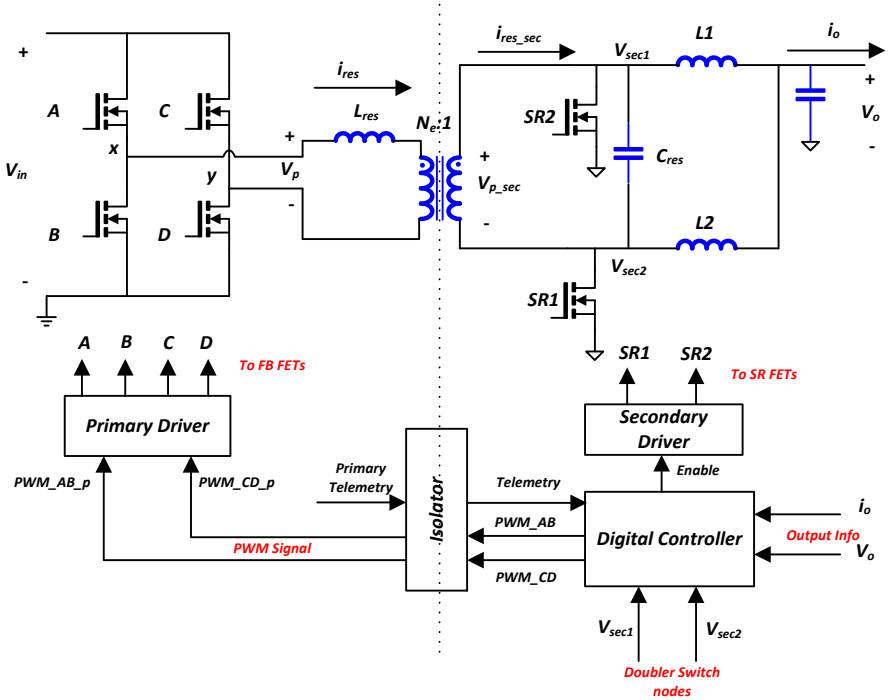

Figure 3 System diagram with main controller and FET drivers

$$t_{shift} = 2\sigma_0 + t_{res} = 2\sigma_0 + \frac{2\pi}{\sqrt{\frac{L_{res\_sec} + L1}{L_{res\_sec} \cdot L1 \cdot C_{res}}}} \quad (1)$$

After applying a load to the output of the converter, it requires a longer time to ramp up i_{res_sec} to reach i_{L1} level in Figure 4, and the additional time required is defined as t_{01}. t_{01} can be calculated in equation (2).

$$t_{01} = \frac{I_o \cdot L_{res}}{2 \cdot N \cdot V_{in}} \quad (2)$$

When $t_{01} > \sigma_0$ is met, we will have an additional operation mode-Mode 3 (i. e. bleeding mode), which only occurs during heavy loading shown in Figure 10 between t_2~t_3. The modes during different intervals are marked in Figure 4 and Figure 10 and the same mode has the same equivalent circuit and model, which will be discussed in section III.

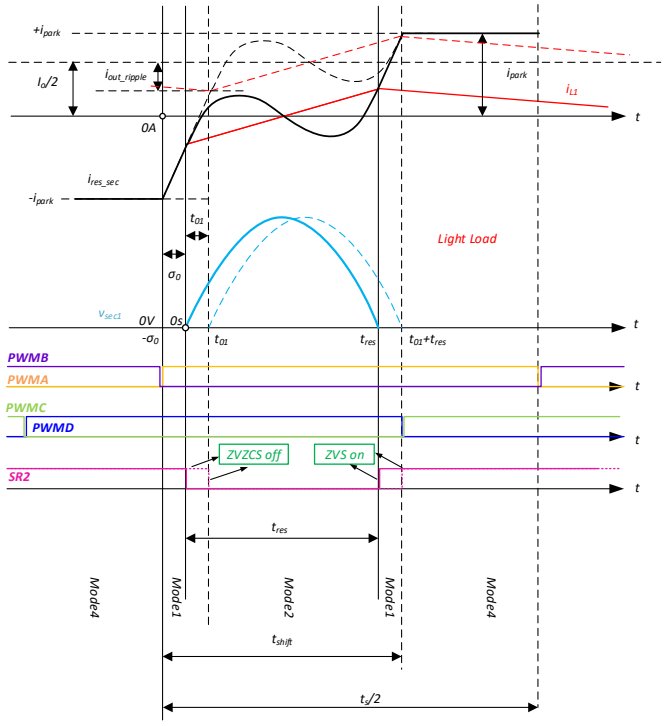

Figure 4 Theoretical waveform for light load of QR-PSFB Converter

Light Load Operation of QR-PSFB Converter ($t_{01}<\sigma_0$)

Mode 1: $-\sigma_0 \le t < t_{01}$

This mode (shown in Figure 7 and Figure 5) is very similar to PSFB converter, high side FET of x phase FET A is turning on while low side FET B is turning off. The negative tank current i_{res} will discharge the equivalent output capacitance of the FET A before the FET A is turned on to achieve ZVS shown in Figure 7. Secondary side SRs are on still, so transformer voltage is clamped to nearly zero. And the primary side current i_{res_prim} is rising with a slew rate of V_{in}/L_{res} and the secondary side current i_{res_sec} is rising with a slew rate of $N*V_{in}/L_{res}$.

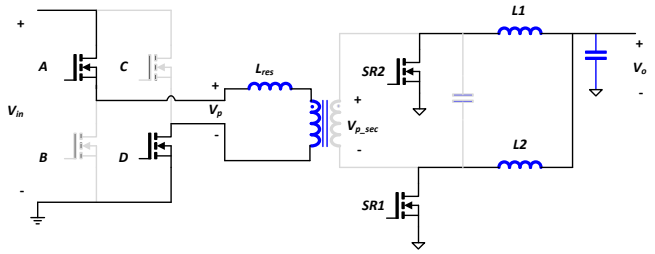

Figure 5 Mode 1 of QR-PSFB Converter

Mode 2: $t_{01} \le t < t_{01}+t_{res}$

This is a unique mode for the new topology shown in Figure 6. The current of the SR is sensed on the secondary side to determine the switching off moment. When the secondary side tank current $i_{res\_sec}=i_{L1}$, the secondary side driver will then turn off the SR FET SR2, so that zero current switching (ZCS) off is achieved. And due to the added resonant capacitor C_{res}, the drain voltage V_{sec1} of SR2 will be rising with a very slow controlled slope, so ZVS is achieved at the same time. And the reverse recovery issue is addressed and the loss is mitigated. Now, the resonance happens in this mode. The sine shape voltage (V_{sec1}-V_{sec2}) across C_{res} is referred as the *bump voltage*. It is critical for the secondary side driver controller to have very small time delay to detect the ZCS moment and turn off the SR. In a practical implementation, there might be some current flowing through the SR FET main channel before turn off, but due to the relatively high resonant capacitance C_{res} is added in the converter, the SR will not have any harmful high voltage spike or ringing at turn off.

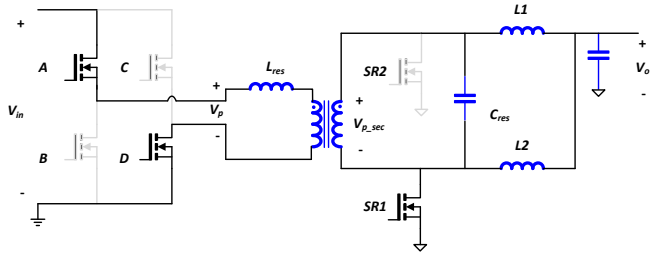

Figure 6 Mode 2 of QR-PSFB Converter

Mode 1: $t_{01}+t_{res} \le t < t_{shift}-\sigma_0$

This mode has the same equivalent circuit as $-\sigma_0 \le t < t_{01}$ in Figure 5. When the voltage across the SR2 V_{sec1} is resonating back to zero, the secondary side driver will turn on SR2 to achieve ZVS on. And the primary side FET A and D are still on, so the transformer voltage is clamped to nearly zero. And the primary side current i_{res_prim} is rising with a slew rate of V_{in}/L_{res} and the secondary side current i_{res_sec} is rising with a slew rate of $N*V_{in}/L_{res}$.

Mode 4: $t_{shift}-\sigma_0 \le t < (t_s/2)-\sigma_0$

When the constant on time t_{shift} expires, the primary side gate will turn off FET D and the positive parking current will discharge the equivalent output capacitance of FET C. After the capacitance is fully discharged and the body diode will conduct. Then the FET C will be turned on with ZVS shown in Figure 9. The parking current will remain nearly constant due to zero clamping voltage on the transformer. The positive i_{park} will help to achieve ZVS on for B FET later.

Due to the similarity of the switching transitions for the other half switching cycle, the details are omitted.

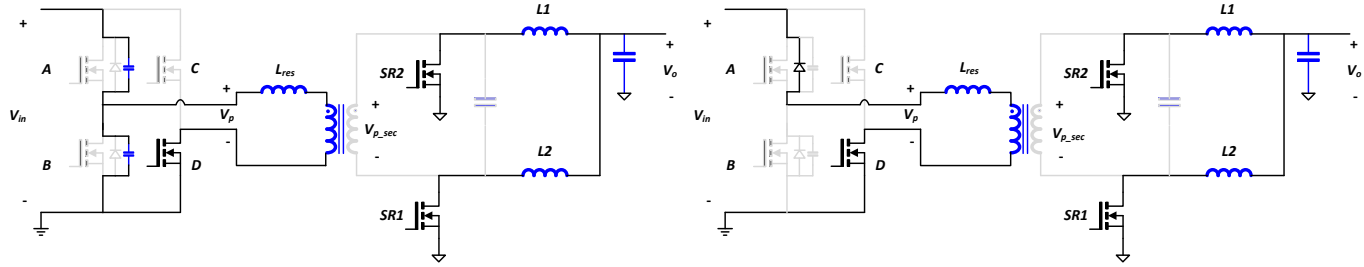

Figure 7 ZVS on of FET A in Mode 1

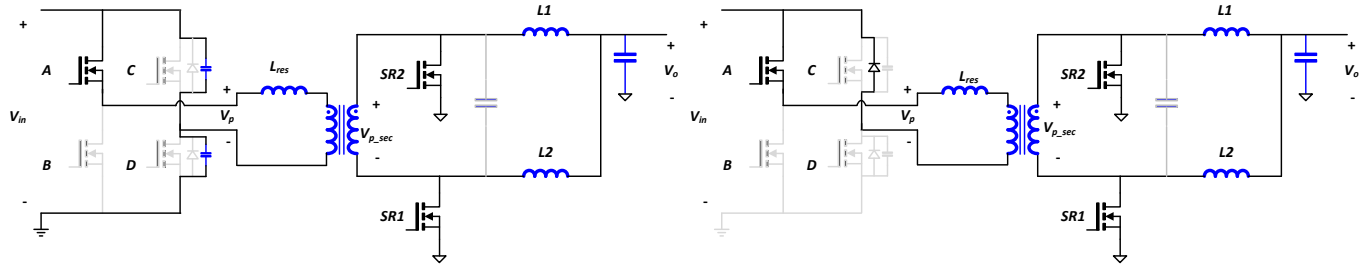

Figure 8 ZVS on of FET C in Mode 4

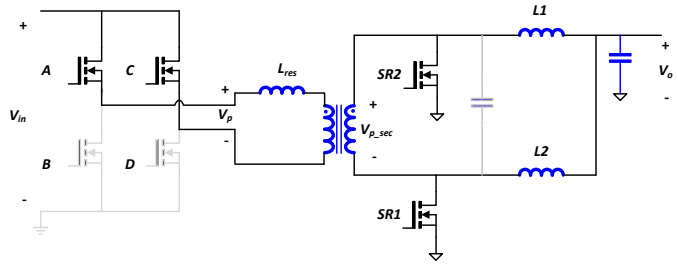

Figure 9 Mode 4 of QR-PSFB Converter

Heavy Load Operation of QR-PSFB Converter ($t_{01}\geq\sigma_0$)

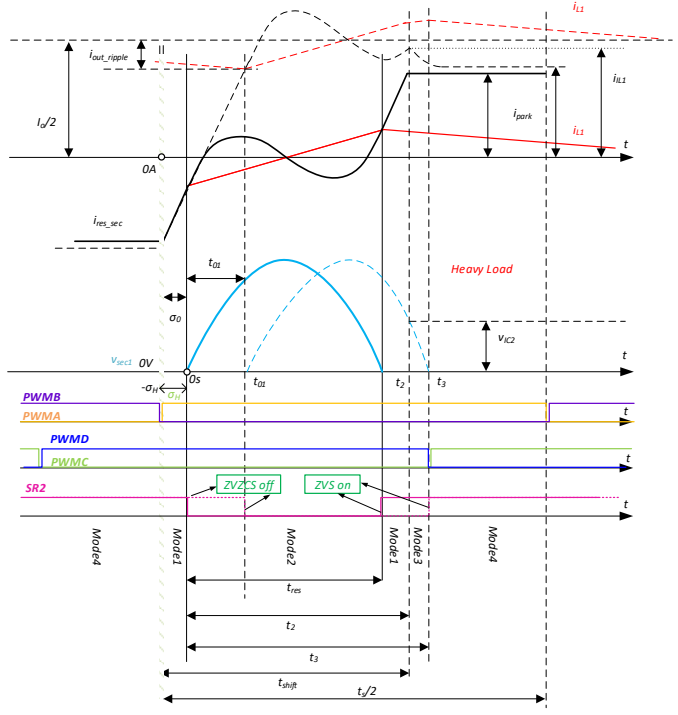

Figure 10 Theoretical waveform for heavy load of QR-PSFB Converter

The theoretical waveform for heavy load operation of the QR-PSFB converter is shown in Figure 10 and the detailed modes of operation are discussed in this section.

Mode 1: $-\sigma_H\leq t<t_{01}$

This mode is the same as light load condition and the FET A is turned on with ZVS and the current i_{res_sec} is ramping up to catch i_{L1}. To differentiate the time interval of σ_0 in the steady state under light load and when I_o=0, the time taken for the i_{res_sec} to reach $-i_{out\_ripple}$ from $-i_{park}$ is defined as σ_H for heavy load condition.

Mode 2: $t_{01}\leq t<t_2$

This mode is the same as light load condition at the beginning, when the secondary side tank current $i_{res\_sec}=i_{L1}$, the secondary side driver will turn off the SR FET SR2, so that ZVZCS off is achieved. However, in heavy load condition, the full resonance will not finish due to constant on time control scheme. So at t_2, the primary side driver will switch off FET D, due to the expiration of t_{shift}. And the time t_2 can be calculated in equation (3).

$$t_2 = t_{shift} - \sigma_H = t_{shift} - \frac{\left(i_{park} - i_{out\_ripple}\right)\cdot L_{res}}{N\cdot V_{in}} \qquad (3)$$

Mode 3: $t_2\leq t<t_3$

This mode is unique in heavy load, and at t_2, the equivalent circuit is shown in Figure 11. The positive i_{park} discharges the output capacitance of FET C until the body diode conducts.

Then the FET C will be turned on with ZVS shown in Figure 12. Different from Mode 4, the SR2 in this mode is off. And in this mode, the tank of L_{res} and C_{res} are discharging to support the output load. The secondary side driver will turn on SR2, when V_{sec1} is discharged to zero to achieve ZVS on.

Mode 4: $t_3\leq t<(t_s/2)-\sigma_H$

At t_3, SR2 is turned on and then this mode is the same as light load condition shown in Figure 9. The parking current will remain nearly constant due to zero clamping voltage on the transformer. The positive $+i_{park}$ will help to achieve ZVS on for B FET later.

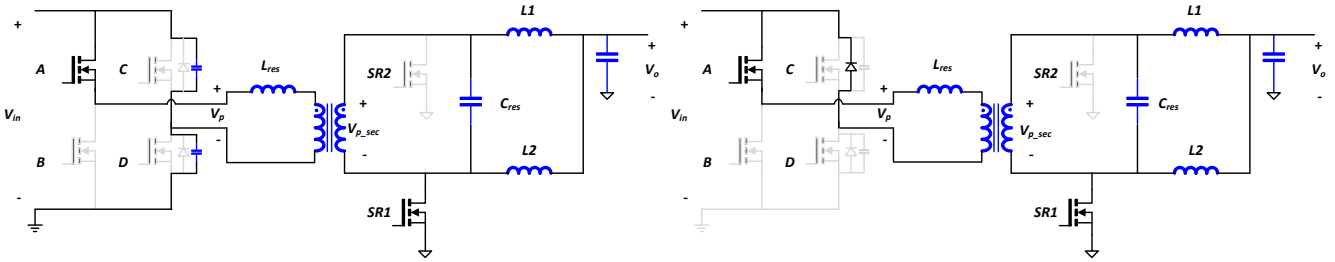

Figure 11 ZVS on of FET C in Mode 3

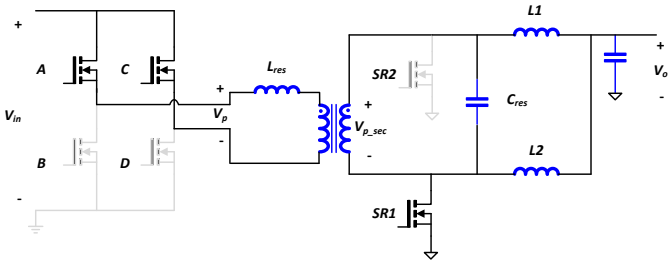

Figure 12 Bleeding Mode of QR-PSFB Converter

Due to the similarity of the switching behavior for the other half switching cycle, the details are omitted for simplicity.

III. MODELING OF QR-PSFB CONVERTER

Although simulation tools can always be used for simulating the switching converters in a much easier way, the circuit parameters remain in non-closed form and it is difficult to tell the impact of a certain design parameter on the results. Also, experiments often take time and additional delay will be expected if magnetics changes are needed. On the other hand, a mathematical model can give us very intuitive information, which can always help the designer to 1) fully understand the operation of the switching states; 2) reduce the number of iterations for optimization in experiments; 3) find worst case/corner case for testing; 4) analyze component tolerance impacts, etc.

In [19], the paper discussed the modeling of a very similar 48V VR converter using second order differential equations, if the output filter inductance is much larger than the resonant inductance. So the output load is modeled as a constant current source and the output inductor is not participating resonance. However, the accuracy is not quite good to match simulation and experiments in low voltage high current PoL voltage regulator (VR) application. In PoL VR application, the output inductor is usually small to improve transient performance, even though it will suffer from bigger output current ripple and *rms* losses [12]. The large current ripple will be filtered by output capacitor banks, which is usually in mF range, to have very low output voltage ripple (for example 1% of V_o). So in this paper, a *new* modeling method is proposed to improve the accuracy of the model, which now includes the output inductor into tank resonance and considers the output current ripple for losses estimation. Due to the relatively big output capacitance, the load can be modeled as a DC voltage source and a load resistor. Compared with a fourth order complete (LCLC) model, this new reduced order model is less complicated but offers very similar accuracy.

Assumptions:

- Transformer is ideal and lossless
- Dead time in the FB and its impact is negligible
- Inductor and capacitor are ideal, no DCR or ESR, etc
- V_s (The reflected voltage of V_p on the secondary side) is an ideal source and all the solid-state switches are ideal
- Output voltage ripple is negligible
- The equivalent model is reflected to the secondary side

So, the secondary side input voltage V_s can be modeled as a DC source or a short circuit, depending on the operation modes. C_{res} is the resonant capacitor. L_{res_sec} is the reflected leakage inductor on the secondary side, where $L_{res\_sec} = \frac{L_{res}}{N_e{}^2}$. N_e is the turns ratio of the transformer. L_1 is the output inductor per phase. Due to the high output capacitance, the output is modeled as DC source and <1% output voltage ripple is ignored, resulting in negligible modeling error but significantly reduced complexity.

Mode 1: Duty cycle loss mode

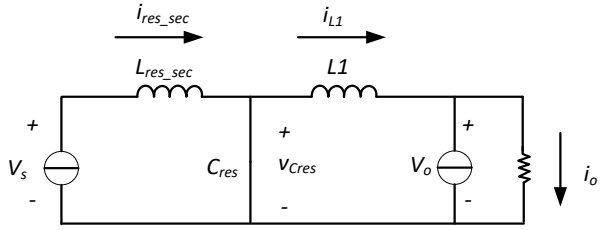

Figure 13 Mode 1 equivalent circuit of proposed model

The duty cycle loss mode of QR-PSFB is the same as the conventional PSFB converter in Figure 13, where the input voltage V_s is applied to the resonant inductor L_{res_sec}. State equations can be written in equation (4):

$$\begin{cases} V_{Lres\_sec} = V_s = \dfrac{V_{in}}{N_e} = L_{res\_sec} \cdot \dfrac{d}{dt} i_{res\_sec}(t) \\ V_{L1} = -V_o = L1 \cdot \dfrac{d}{dt} i_{L1}(t) \end{cases} \tag{4}$$

Mode 2: Power delivery mode

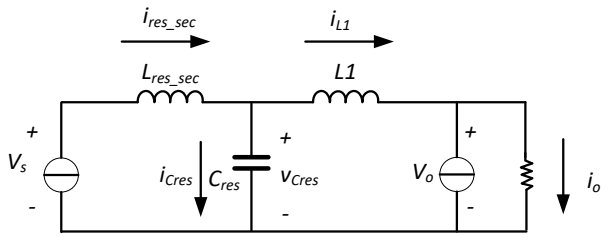

Figure 14 Mode 2 equivalent circuit of proposed model

The SR on the secondary side is released, when i_{res_sec}=i_{L1} and resonance between L_{res_sec}, L_1 and C_{res} happens (in Figure 14). State equations can be written in equation (5) and the initial condition can be calculated in equation (6):

$$\begin{cases} V_s = \dfrac{V_{in}}{N_e} = v_{Lres\_sec}(t) + v_{Cres}(t) \\ v_{Cres}(t) = v_{L1}(t) + V_o \\ i_{Cres}(t) = i_{res\_sec}(t) - i_{L1}(t) \end{cases} \tag{5}$$

$$\begin{cases} v_{Cres0} = 0 \\ i_{res\_sec0} = \dfrac{1}{2} I_o - i_{out\_ripple} \end{cases} \tag{6}$$

Mode 3: Bleeding mode

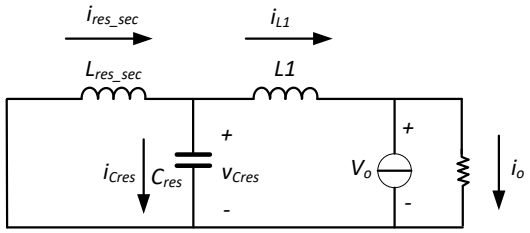

Figure 15 Mode 3 equivalent circuit of proposed model

The bleeding mode is another unique mode of this new topology. Due to the ZVZCS feature of secondary side SR control and driving, when the primary side x or y phase both upper (FET A and C) or lower FETs (FET B and D) are on, the input of the model is a short circuit, while SR is still off. So this mode is called bleeding mode, since L_{res_sec} and C_{res} are now discharging to the load together. State equations are as follows in equation (7), where V_{IC2} and i_{IL1} are the initial conditions of the resonant capacitor voltage v_{Cres} and inductor current i_{Lres_sec} at time t_2 shown in Figure 10 and expressed in equation (8):

$$\begin{cases} v_{Lres\_sec}(t) + v_{Cres}(t) = 0 \\ v_{Cres}(t) = v_{L1}(t) + V_o \\ i_{Cres}(t) = i_{res\_sec}(t) - i_{L1}(t) \end{cases} \tag{7}$$

$$\begin{cases} v_{Cres0} = V_{IC2} = v_{sec1}(t_2) \\ i_{res\_sec0} = i_{IL1} = i_{res\_sec}(t_2) \end{cases} \tag{8}$$

Mode 4: Freewheeling mode

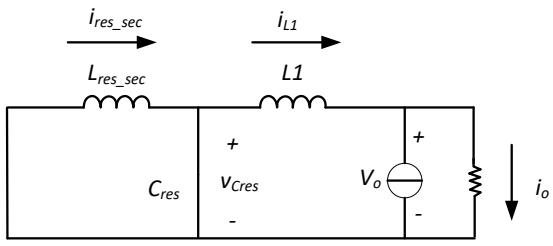

Figure 16 Mode 4 equivalent circuit of proposed model

When V_{sec1}=0 or V_{sec2}=0, the secondary side driver will turn on the SR, so C_{res} is shorted. And i_{res_sec} will remain constant and output inductor current is freewheeling through SRs (in Figure 16). State equations can be written in equation (9):

$$\begin{cases} V_{Lres\_sec} = L_{res\_sec} \cdot \dfrac{d}{dt} i_{res\_sec}(t) = 0 \\ V_{L1} = -V_o = L1 \cdot \dfrac{d}{dt} i_{L1}(t) \end{cases} \tag{9}$$

Solutions of the State Equations

In order to present the system in a closed form, the third order differential equations (4)~(9) have to be solved for each of the modes. The final value of the previous state will be substituted into the next state for initial condition.

In Mode 1, the current $i_{res\_sec}(t)$ will ramp up to $i_{L1}(t)$ level linearly. Then we will enter the Mode 2. The equations for $i_{res\_sec}(t)$ and $v_{Cres}(t)$ can be expressed in (11) and (12), where the equivalent resonant frequency is shown in (10). It is worth mentioning that the inductance $L1$ is involved in the resonance, which is ignored in the model proposed in [19].

$$\omega_{res} = \sqrt{\frac{L_{res\_sec} + L1}{L_{res\_sec} \cdot L1 \cdot C_{res}}} \tag{10}$$

$$\begin{aligned} i_{res\_sec}(t) = {} & \frac{I_{out}}{2} + \frac{\dfrac{V_s}{L_{res\_sec}} - \dfrac{V_s - V_o}{L_{res\_sec} + L1}}{\omega_{res}} \cdot \sin\left(\omega_{res}(t - t_{01})\right) \\ & + \left(i_{res\_sec}(t_{01}) - i_{L1}(t_{01})\right) \cdot \cos\left(\omega_{res}(t - t_{01})\right) + \frac{V_s - V_o}{L_{res\_sec} + L1}(t - t_{01}) \end{aligned} \tag{11}$$

$$\begin{aligned} v_{Cres}(t) = {} & -\left(\frac{L_{res\_sec} \cdot V_o + L1 \cdot V_s}{L_{res\_sec} + L1}\right) \cdot \cos\left(\omega_{res}(t - t_{01})\right) + \\ & \frac{i_{res\_sec}(t_{01}) - i_{L1}(t_{01})}{C_{res}\omega_{res}} \cdot \sin\left(\omega_{res}(t - t_{01})\right) + \frac{L_{res\_sec} \cdot V_o + L1 \cdot V_s}{L_{res\_sec} + L1} \end{aligned} \tag{12}$$

At t=t_{01}, the term $i_{res\_sec}(t_{01})$-$i_{L1}(t_{01})$=0 in equations (10) and (11). Now, we can discover the impacts of all the information of design parameters in i_{res_sec} and v_{Cres}. For example, the i_{res_sec} is a linear function plus a sine function and the peak of i_{res_sec} is a function of V_s, V_o, and the tank elements. For the function of v_{Cres}, the peak will be $2\times\frac{L_{res\_sec} \cdot V_o + L1 \cdot V_s}{L_{res\_sec} + L1}$ and it is worth noting that the peak value of v_{Cres} is not a function of C_{res} after all.

$$i_{L1}(t)=i_{res\_sec}(t)-\left(C_{res}\left(\frac{L_{res\_sec}\cdot V_o+L1\cdot V_s}{L_{res\_sec}+L1}\right)\cdot\omega_{res}\right)\cdot\sin\left(\omega_{res}(t-t_{01})\right)+\left(i_{res\_sec}(t_{01})-i_{L1}(t_{01})\right)\cdot\cos\left(\omega_{res}(t-t_{01})\right) \quad (13)$$

$$i_{res\_sec}(t)=\left(\frac{i_{L1}(t_2)-i_{res\_sec}(t_2)}{L_{res\_sec}+L1}\right)\cdot L1\cdot\cos\left(\omega_{res}(t-t_2)\right)+\frac{\frac{V_o}{L_{res\_sec}+L1}-\frac{v_{Cres}(t_2)}{L_{res\_sec}}}{\omega_{res}}\cdot\sin\left(\omega_{res}(t-t_2)\right)$$
$$-\frac{V_o}{L_{res\_sec}+L1}(t-t_2)+i_{L1}(t_2)-\frac{i_{L1}(t_2)-i_{res\_sec}(t_2)}{L_{res\_sec}+L1}\cdot L1 \quad (14)$$

$$v_{Cres}(t)=\frac{i_{L1}(t_2)-i_{res\_sec}(t_2)}{C_{res}\omega_{res}}\cdot\sin\left(\omega_{res}(t-t_2)\right)+\left(v_{Cres}(t_2)-\frac{L_{res\_sec}\cdot V_o}{L_{res\_sec}+L1}\right)\cdot\cos\left(\omega_{res}(t-t_2)\right)+\frac{L_{res\_sec}\cdot V_o}{L_{res\_sec}+L1} \quad (15)$$

$$i_{L1}(t)=i_{res\_sec}(t)-\left(i_{res\_sec}(t_2)-i_{L1}(t_2)\right)\cdot\cos\left(\omega_{res}(t-t_2)\right)-\left(C_{res}\left(v_{Cres}(t_2)-\frac{L_{res\_sec}\cdot V_o}{L_{res\_sec}+L1}\right)\cdot\omega_{res}\right)\cdot\sin\left(\omega_{res}(t-t_2)\right) \quad (16)$$

If the output load is heavy, after on time t_{shift} expires, v_{Cres} is not reaching zero yet, then Mode 3 (bleeding mode) exists. And the bleeding mode ends when v_{Cres} discharges to zero. Tank current i_{res_sec} and voltage v_{Cres} can be calculated in equations (14) and (15).

The output inductor current can be also derived using equation (16).

In Figure 10, the time t_3 can be solved from equation (17) when the $v_{Cres}(t)$ decays to zero, where k_a, k_b and k_c can be found in equations (18)-(20).

$$k_a\cdot\sin\left(\omega_{res}\cdot t_3\right)+k_b\cdot\cos\left(\omega_{res}\cdot t_3\right)+k_c=0 \quad (17)$$

$$k_a=\frac{i_{L1}(t_2)-i_{res\_sec}(t_2)}{C_{res}\omega_{res}} \quad (18)$$

$$k_b=v_{Cres}(t_2)-\frac{L_{res\_sec}\cdot V_o}{L_{res\_sec}+L1} \quad (19)$$

$$k_c=\frac{L_{res\_sec}\cdot V_o}{L_{res\_sec}+L1} \quad (20)$$

The time t_3 then can be solved using equation (21) for different k_a conditions.

$$t_3=\begin{cases}\dfrac{\arcsin\left(\dfrac{k_c}{\sqrt{k_a^{\,2}+k_b^{\,2}}}\right)-\arctan\left(\dfrac{k_b}{k_a}\right)}{\omega_{res}}+t_2 & k_a<0\\ \dfrac{\arcsin\left(\dfrac{k_c}{\sqrt{k_a^{\,2}+k_b^{\,2}}}\right)-\arctan\left(\dfrac{k_b}{k_a}\right)+\pi}{\omega_{res}}+t_2 & k_a\geq 0\end{cases} \quad (21)$$

Finally, tank current i_{res_sec}, the resonant capacitor voltage v_{Cres} and the output inductor current i_{L1} are shown in Figure 17-Figure 19.

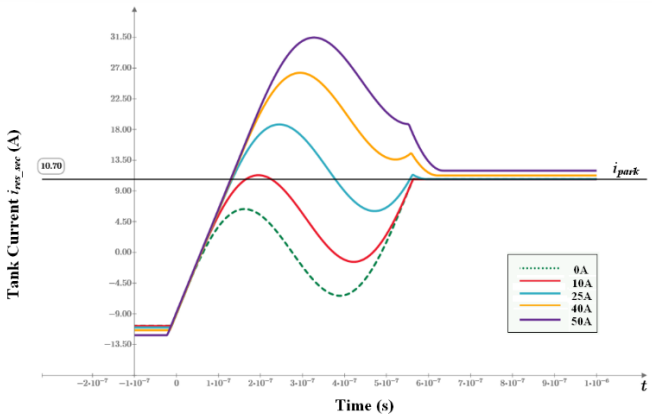

Figure 17 Modeled tank current i_{res_sec} at different output current conditions and V_{in}=54V

In Figure 17, the tank current on the secondary side is modeled and plotted at different operating conditions and V_{in}=54V. From the plots, it reveals that 1) the parking current is very similar across full load range to provide ZVS even at light load; and 2) at heavy load, the bleeding mode occurs, where the i_{res} starts reducing until t_3. It is worth noting that the load independent i_{park} current level (for switches A and B to achieve ZVS in Figure 7) is very different from the conventional ZVS-PSFB converter. In conventional ZVS-PSFB converter, this load dependent current level (i_p at time t_0 or t_4 in Figure 1) is too low at light load to achieve ZVS for switches A and B, but at heavy load this current level becomes too high and introduces more circulating power losses. In the QR-PSFB converter, the i_{park} design parameter can be optimized to provide sufficient energy for ZVS at light load, but avoid unnecessary circulating losses for heavy load. The parking current level and ZVS range for different operating conditions and component tolerances are studied in more details in section IV. A.

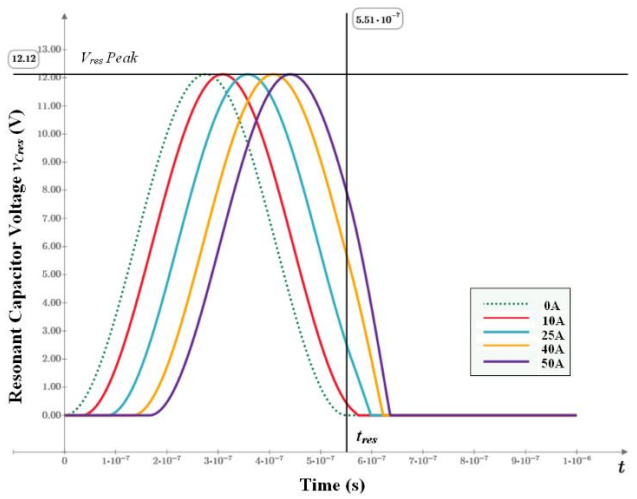

Figure 18 Modeled resonant capacitor voltage v_{Cres} at different output current conditions and V_{in}=54V

The function of $v_{Cres}(t)$ with different output currents I_o (0A~50A) are plotted in Figure 18. For I_o=0A, the dotted green curve has resonance with duration of 551ns and can be calculated using equation (10). While I_o is increasing, the curve will be shifted towards the left in time, the bleeding mode happens after 551ns and we can see the capacitor discharging in different rates at different output loading. The higher the output current, the stronger the bleeding mode will be, so that the capacitor voltage $v_{Cres}(t)$ discharges faster to zero. And the average value of v_{Cres} per phase in the current doubler will be the output voltage.

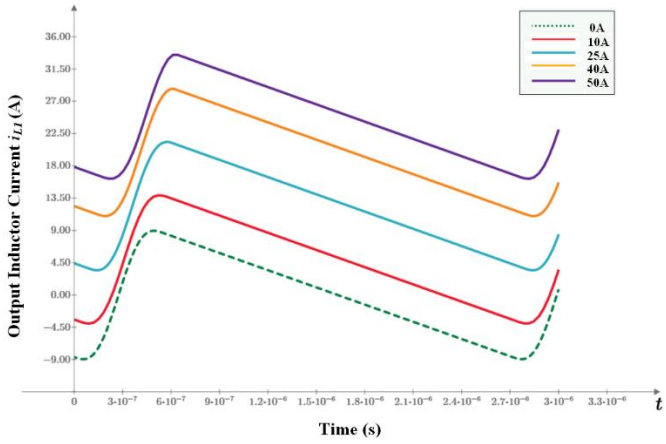

Figure 19 Modeled output inductor current i_{L1} at different output current conditions and V_{in}=54V

The function of $i_{L1}(t)$ with different output currents I_o (0A~50A) are plotted in Figure 19. It is worth noting that the waveform is not exactly the same as PWM converters, such as Buck converter (in PWM converter, the inductor current has triangular waveform). And during Mode 2, the resonance is observed as well in the waveform of $i_{L1}(t)$. Also, for PoL application, the inductance is usually small to improve the dynamic response of the converter [12], therefore, the ripple of output inductor current is rather high (~18Apk-pk) and cannot be ignored anymore [19].

IV. Design with the Proposed Modeling

To start a new design for 54V-1.2V 25A voltage regulator, transformer turns ratio should be selected to properly step down the primary input voltage to around 6~8 V on the secondary of the transformer. In the initial reference design, the turns ratio is set to 7:1. The targeted switching frequency is 300 kHz ~400 kHz and the t_{shift} will be around 550 ns ~ 650 ns. Due to the fast dynamic response requirement in PoL VR application, the output inductor should be relatively small and 150 nH is a typical design value to start with. In this section, optimization of the design process will be presented. It will demonstrate that for the same resonant frequency and similar switching frequency, the higher the L_{res}, the rms current will be reduced in the tank for better efficiency. However, the secondary side stress will be increased and the output power capability will be reduced. So, L_{res} for this application is selected around 2~4µH to achieve a good design trade-off and using equation (1) C_{res} can be calculated. The design example is provided based on the proposed modeling method and the reference design parameter is shown in Table 1.

Table 1 Reference Design Parameter of the application example

Description	Value
Input Voltage, V_{in}	40V-60V, 54V Typical [1]
Output Voltage, V_o	1.2V (+/-10%)
Output Current, I_o	25A
Turns Ratio, N_e	7:1
Resonant Inductance, L_{res}	2.5µH (+/-10%)
Resonant Capacitance, C_{res}	68nF*2+33nF*2=202nF (+/-5%)
Output Inductor, $L1$ and $L2$	150nH (+/-10%)
Output Capacitance, C_o	330µF×1 (SP-CAP) +22µF×30 (MLCC)
Constant on time, T_{shift}	575ns
Primary Side FET (FET A, B, C, D)	75V, 35A, 30mΩ
Secondary Side FET (SR1 and SR2)	30V, 75A, 1.3mΩ, 2 in parallel

A. *Parking Current Level for ZVS*

Sufficient parking current level is an important design parameter for QR-PSFB converter to achieve ZVS on the primary side, however, if the parking current is too high, efficiency will be lower because of high circulating energy. Using the model, we can plot the i_{park} for different working conditions. And due to the lower current slew rate during Mode 1 at V_{in_min}=40V, we need to make sure we have enough parking current and energy to achieve ZVS. And tolerances of the resonant tank elements are considered as well and plotted in Figure 20. It is worth noting that 1) the lowest parking current occurs when all the elements are at their maximum values, and 2) the parking current is nearly constant across the load range.

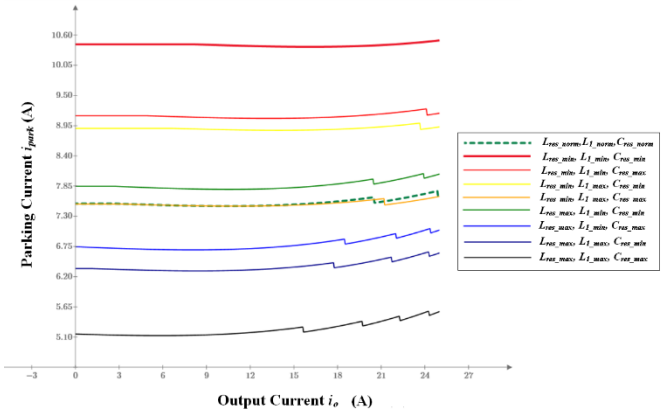

Figure 20 Modeled Parking Current at different working conditions and V_{in}=40V

And using the parking current information, the switching voltage on the primary side V_{sw} can be estimated in equation (22), where C_{eq} is the equivalent output capacitance of the MOSFET. If the parking energy is enough to discharge the output capacitance of the primary side FETs, ZVS turn-on can be achieved and V_{sw}=0, otherwise, there will be a certain level of hard switching.

$$V_{SW} = \begin{cases} V_{in} - \sqrt{\frac{L_{res}}{C_{eq}}} \cdot I_{park} & \left(V_{in} - \sqrt{\frac{L_{res}}{C_{eq}}} \cdot I_{park}\right) > 0 \\ 0 & \left(V_{in} - \sqrt{\frac{L_{res}}{C_{eq}}} \cdot I_{park}\right) \le 0 \end{cases} \quad (22)$$

The hard switching voltage level can be plotted in Figure 21 for different tank parameters considering component tolerance at V_{in}=40V. In most of the cases, ZVS can be achieved across the full load range. The worst case condition occurs when the resonant inductance L_{res}, capacitance C_{res} and output inductance $L1$ are all at the maximum value. There will be less than 10V of hard switching and about 20mW switching loss per FET, which has minor impact on the efficiency, considering this is the absolutely worst case. This means the reference tank design is very robust for ZVS range.

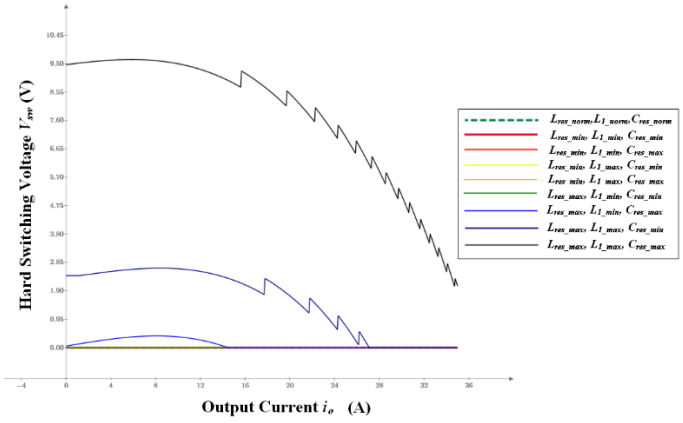

Figure 21 Modeled hard switching voltage at different working conditions and V_{in}=40V.

B. *RMS currents and conduction losses*

Using the model of i_{res} and i_{L1} discussed in section III. 0, *rms* value can be calculated by definition. If needed, we can look at the trend of *rms* current corresponding to any design parameter. In Figure 22, it shows the *rms* of the secondary side current i_{res_sec} at different input voltages and output current conditions. Due to the lowest current ripple at 40V input, the *rms* current of the transformer is the lowest. It indicates the duty cycle and turns ratio design of the converter is very critical to minimize the *rms* losses.

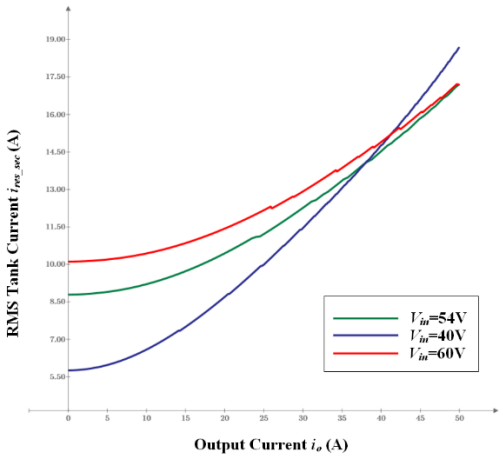

Figure 22 Rms value of secondary side transformer current

Similarly, the output inductor *rms* current can be also calculated and it shows that even when V_{in}=54V, I_o=0A, we have about 5.76A of *rms* current due to the 18Apk-pk current ripple shown in Figure 19. And this 5.76A *rms* current will be missed in the loss estimation, if we use the second-order modeling proposed in [19].

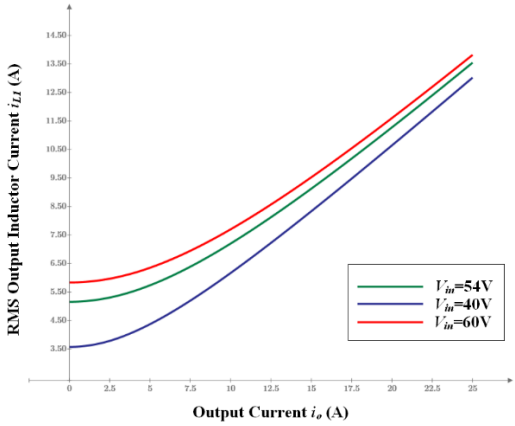

Figure 23 Rms value of output inductor current

By using the $i_{res\_sec}(t)$ and $i_{L1}(t)$ information, the SR current waveform can be obtained in Figure 24. And the *rms* value of the SR current can be calculated for loss estimation as well.

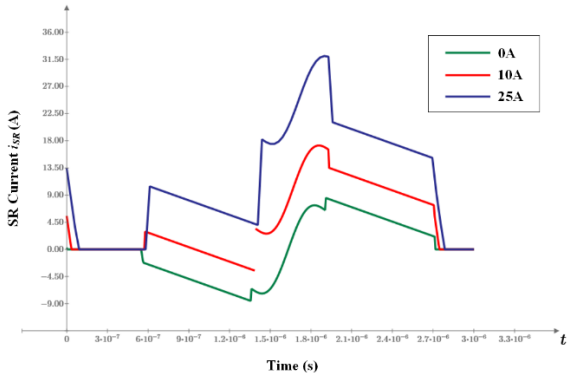

Figure 24 SR FET current waveform at different operating conditions

C. Switching frequency

Using the v_{Cres} model information, it is possible to estimate the switching frequency of the converter under steady state. The average value of the v_{Cres} minus the DCR drop across the output inductor should be the output voltage V_o. So by calculating the integral value of v_{Cres}, that is $\int_{t_{01}}^{t_{01}+t_{res}}(v_{Cres})\cdot dt$ for light load and no load, or $\int_{t_{01}}^{t_3}(v_{Cres})\cdot dt$ for heavy load, the f_{sw} can be estimated as $\frac{V_o+\frac{I_o}{2}DCR}{\int(v_{Cres})\cdot dt}$, which is derived in equation (23), where DCR is the DC resistance of the output inductor.

$$f_{sw}=\begin{cases}\dfrac{V_o+\frac{I_o}{2}\cdot DCR}{\int_{t_{01}}^{t_{01}+t_{res}}\left[v_{Cres}(t)\right]\cdot dt} & (t_{01}\le\sigma_0)\\ \dfrac{V_o+\frac{I_o}{2}\cdot DCR}{\int_{t_{01}}^{t_3}\left[v_{Cres}(t)\right]\cdot dt} & (t_{01}>\sigma_0)\end{cases} \tag{23}$$

This information can be used to select the transformer core material and estimate core loss, FET turn off losses, gate drive losses, etc. Also, in industrial application, f_{sw} is also very important to design front-end EMI filter corner frequency.

D. Transformer Core Loss Estimation

Transformer core loss can be estimated using Steinmetz's equation [33], the k, α and β parameters can be estimated from the core material datasheet. And the flux density at different load conditions can be calculated by equation (24), where A_e is the equivalent core cross section area and N_p is the number of primary side turns. Eventually, the core loss can be estimated in (25), where V_e is the equivalent core volume.

$$B=\begin{cases}\dfrac{N_e\cdot\int_{t_{01}}^{t_{01}+t_{res}}v_{Cres}(t)\cdot dt}{2\cdot N_p\cdot A_e} & (t_{01}\le\sigma_0)\\ \dfrac{N_e\cdot\int_{t_{01}}^{t_3}v_{Cres}(t)\cdot dt}{2\cdot N_p\cdot A_e} & (t_{01}>\sigma_0)\end{cases} \tag{24}$$

$$P_{core}=V_e\cdot k\cdot f^{\alpha}\cdot B^{\beta} \tag{25}$$

E. Switching Losses

Even through the primary side FETs are under ZVS turn-on, however, due to the miller-plateau, the complementary FETs in each of the legs will have turn off losses. We can estimate the turn off losses in equation (26), where t_{off} is the turn off time [29]:

$$P_{sw}=\frac{1}{2}\frac{i_{park}\cdot V_{in}\cdot t_{off}\cdot f_{sw}}{N_e} \tag{26}$$

The gate drive loss can be estimated in equation (27), where V_g is the gate voltage and the Q_g is the total gate charge [29].

$$P_{gate}=V_g\cdot Q_g\cdot f_{sw} \tag{27}$$

F. Output power capability

Due to the unique behavior of secondary side driver, the converter will have the bleeding mode for a heavy load. Before v_{Cres} is fully discharged, we cannot turn on SR on the secondary side or start the next power delivery mode, otherwise, the converter will be damaged. And the main digital controller will prevent this behavior from happening. Based on this limitation, the output voltage and power capability can be estimated. When V_{in} =40V, L_{res}, C_{res} and output inductor $L1$ or $L2$ are at the maximum value, we will have the lowest output power capability. Theoretically, this reference design tank can deliver up to 55A output current, considering the worst case tank value, shown in equation (28), where the function $v_{Cres}(V_{max},t)$ is the resonant capacitor voltage of the tank at the maximum output voltage. Computer program can be used to solve the V_{max} and plot the V-I curve in Figure 25.

$$V_{max}=\begin{cases}\dfrac{\int_{t_{01}}^{t_{01}+t_{res}}v_{Cres}(V_{\max},t)\cdot dt}{2\cdot t_{shift}} & (t_{01}\le\sigma_0)\\ \dfrac{\int_{t_{01}}^{t_3}v_{Cres}(V_{\max},t)\cdot dt}{2\cdot(\sigma_H+t_3)} & (t_{01}>\sigma_0)\end{cases} \tag{28}$$

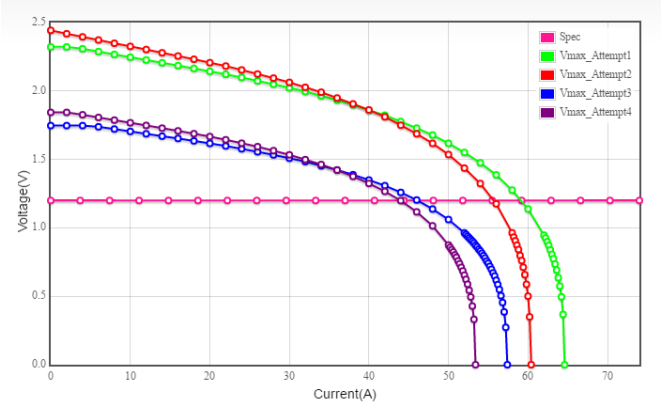

Figure 25 Output power capability curve in different design conditions

To compare with the reference design, another tank parameter is also plotted with worst tolerance case for output capability. It is worth noting that when the turns ratio N_e increases, the output capability will be reduced. However, later we will see that when N_e is higher, the converter is more efficient, because of the reduced *rms* conduction losses on the primary side, so there is a design tradeoff to make when selecting proper N_e for design optimization.

Table 2 Output Capability with different design parameters

Attempt #	V_{in} (V)	N_e	L_{res} (μH)	C_{res} (nF)	$L1$ (nH)	I_{o_max}@1.2V (A)
1	40	7:1	2.5	202	150	59.2
2	40	7:1	2.75	212	165	55.5
3	40	9:1	3.6	202	150	46
4	40	9:1	3.96	212	165	44

V. Simulation and Experimental Verification

Design prototype is built based on the modeling and design guideline proposed in this paper, shown in Figure 26.

The access to secondary side tank current in experiments is very limited, due to the added measurement loop will change the tank characteristics, especially the output inductance. In the

experiments, only primary side current i_{res_prim} and v_{Cres} are measured and shown for the tank information.

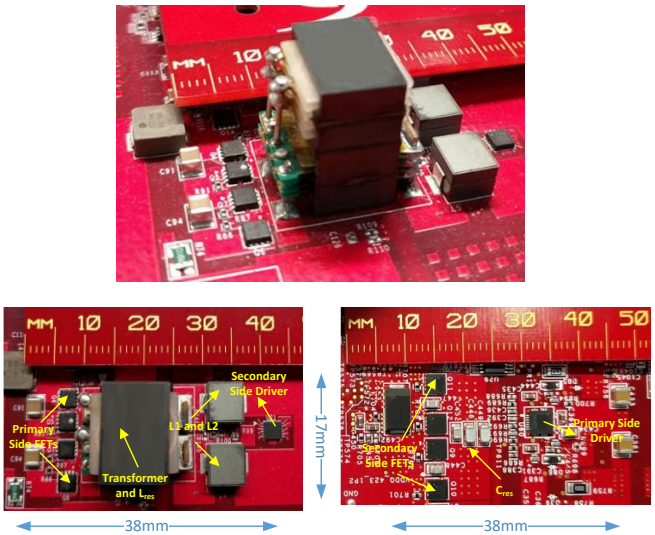

Figure 26 54V-1.2V 25A Prototype picture

G. Comparison of Modeling, Simulation, and Experiment

1. Comparison at I_o =0A

Comparisons are made between the model in [19], the proposed model, simulation and the experimental results for I_o=0A. The summary is listed in Table 3. Simulation results and experiments are shown in Figure 27 and Figure 28. It demonstrates that the proposed model closely matches the simulation and experiments and the result accuracy is improved significantly compared with the model in [19]. And the model in [19] cannot provide the i_{park}, tank voltage V_{Cres} and current i_{res_sec} and switching frequency f_{sw} values correctly, therefore it cannot be used for guiding the design of this converter.

Table 3 Comparison of Modeling, Simulation, and Experiment at I_o=0A

I_o=10A	i_{park} (A)	i_{res_sec} peak (A)	V_{Cres} peak(V)	f_{sw} (kHz)
Model in [19]	-4.6	11.2	15.4	251
Proposed Model	10.7	6.3	12.1	368
Simulation	11	6.5	11.8	377
Experiment	9.6	7.2	12.2	355

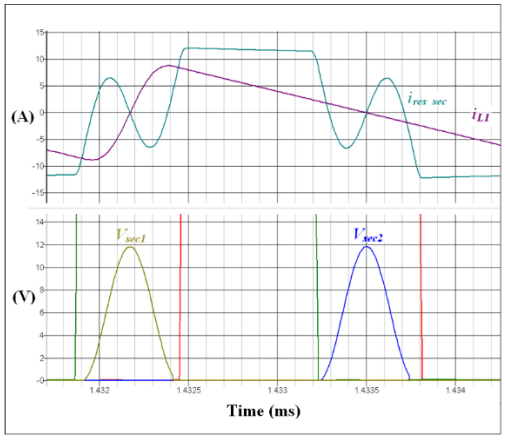

Figure 27 Simulated results: i_{res_sec} peak=6.5A, i_{park}=11A, f_{sw}=377kHz, at I_o=0A

Figure 28 Experimental results: CH1-Yellow: V_p; CH2-Blue: V_{ds} of FET D; CH3-Pink: V_{p_sec}; CH4-Green: -i_{res_prim}; i_{res_prim} peak=1.03A, reflected i_{res_sec} peak=7.2A, i_{park}=9.6A, f_{sw}=355kHz, at I_o=0A;

2. Comparison at I_o =10A

Comparisons are made between the model in [19], the proposed model, simulation and the experimental results for I_o =10A. The summary is listed in Table 4. Simulation results and experiments are shown in Figure 29 and Figure 30. It demonstrates that the proposed model closely matches the simulation and experiments and the result accuracy is improved significantly compared with the model in [19]. And the model in [19] cannot provide the i_{park}, tank voltage V_{Cres} and current i_{res_sec} and switching frequency f_{sw} values correctly, therefore it cannot be used for guiding the design of this converter.

Table 4 Comparison of Modeling, Simulation, and Experiment at I_o =10A

I_o=10A	i_{park} (A)	i_{res_sec} peak (A)	V_{Cres} peak(V)	f_{sw} (kHz)
Model in [19]	-4.4	16.1	15.4	253
Proposed Model	10.7	11.4	12.1	370
Simulation	11.4	11.4	11.8	380
Experiment	10.5	11.2	11.6	370

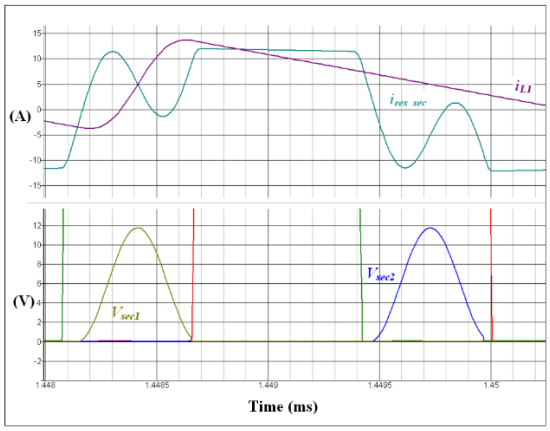

Figure 29 Simulated results: i_{res_sec} peak=11.4A, i_{park}=11.4A, f_{sw}=380kHz, I_o=10A

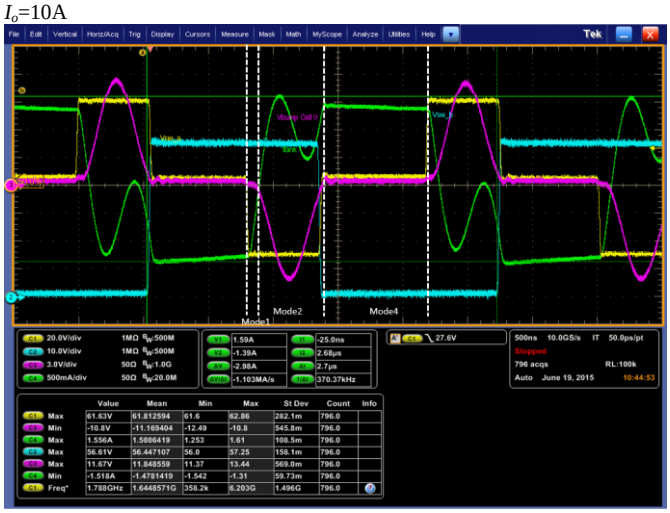

Figure 30 Experimental results: CH1-Yellow: V_p; CH2-Blue: V_{ds} of FET D; CH3-Pink: V_{p_sec}; CH4-Green: -i_{res_prim}; i_{res_prim} peak=1.6A, reflected i_{res_sec} peak=11.2A, i_{park}=10.5A, f_{sw}=370kHz, I_o =10A

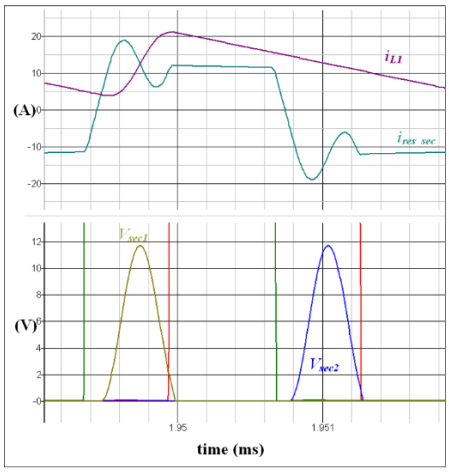

Figure 31 Simulated results: i_{res_sec} peak=18.9A, i_{park}=11.5A, f_{sw}=386kHz, I_o =10A

Figure 32 Experimental results: CH1-Yellow: V_p; CH2-Blue: V_{ds} of FET D; CH3-Pink: V_{p_sec}; CH4-Green: -i_{res_prim}; i_{res_prim} peak=2.54A, reflected i_{res_sec} peak=17.8A, i_{park}=10.5A, f_{sw}=386kHz, I_o=25A

3. *Comparison at I_o =25A*

Comparisons are made between the model in [19], the proposed model, simulation and the experimental results for I_o =25A. The summary is listed in Table 5. Simulation results and experiments are shown in Figure 31 and Figure 32. It demonstrates that the proposed model closely matches the simulation and experiments and the result accuracy is improved significantly compared with the model in [19]. And the model in [19] cannot provide the i_{park}, tank voltage V_{Cres} and current i_{res_sec} and switching frequency f_{sw} values correctly, therefore it cannot be used for guiding the design of this converter.

Table 5 Comparison of Modeling, Simulation, and Experiment at I_o =25A

I_o=25A	**i_{park} (A)**	**i_{res_sec} peak (A)**	**V_{Cres} peak(V)**	**f_{sw} (kHz)**
Model in [19]	-4.1	23.8	15.4	257
Proposed Model	10.7	18.8	12.1	374
Simulation	11.5	18.9	11.8	386
Experiment	10.5	17.8	11.1	386

H. *Efficiency and Losses*

Finally, we have all the information to estimate the efficiency of the design. Modeled efficiency curves are shown in Figure 33 for the reference design in Table 1 at different input voltages.

It is worth noting that at lower input voltages, the efficiency is higher, which indicates a way of optimizing the efficiency of QR-PSFB converter by increasing the effective duty ratio. Therefore, the improved design proposes a higher turns ratio (N_e=9) but at the same time attempts to maintain similar equivalent resonant tank design (L_{res}=3.6μH) seen on the secondary side. And at 25A full load, the improved design offers 1% higher efficiency and more than 10% loss reduction. However, we can observe from the Figure 25 that when N_e is higher, the output capability is lower.

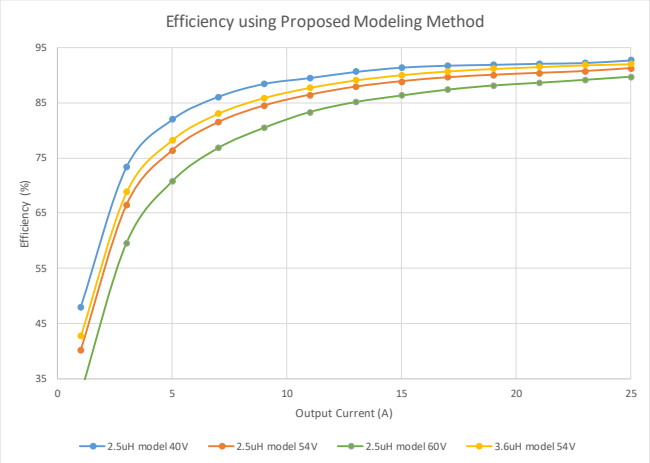

Figure 33 Efficiency curves using the proposed model at different design conditions

Efficiency is measured and compared on the porotype with the reference design and the improved design in Figure 34. The modeled efficiency matches the measured result very well in both of the design cases. And the error is less than 0.2% across the load range.

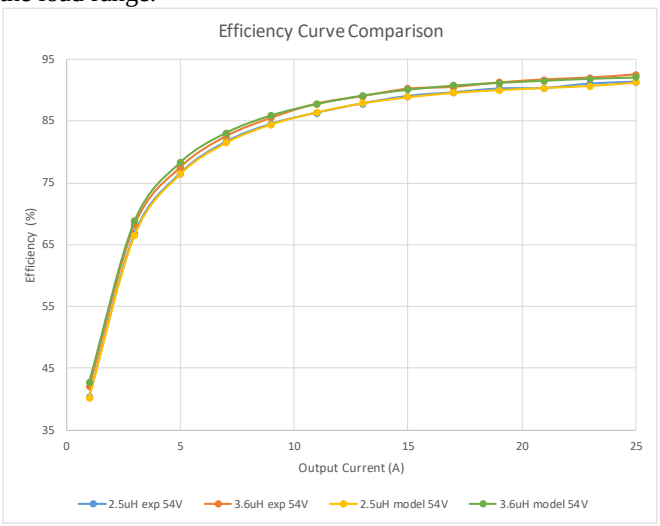

Figure 34 Efficiency comparison between experimental results and proposed model

The modeled power loss breakdown is shown in Figure 35. We can observe that the conduction losses of the transformer and the FETs are the dominant losses, especially at heavy load condition. The "Other" losses are mainly the bias power of the main digital controller.

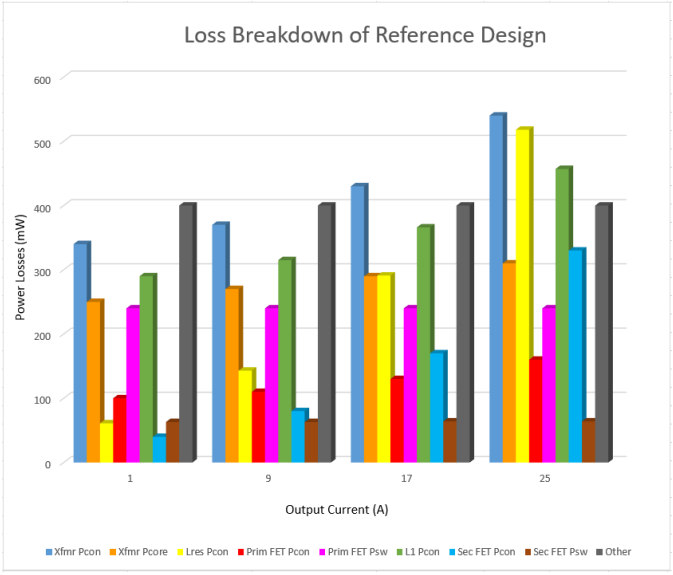

Figure 35 Loss breakdown of the reference design

The modeled power loss breakdown is shown for the improved design in Figure 36. The major loss saving is from the conduction losses of the transformer, resonant inductor L_{res} and primary FETs.

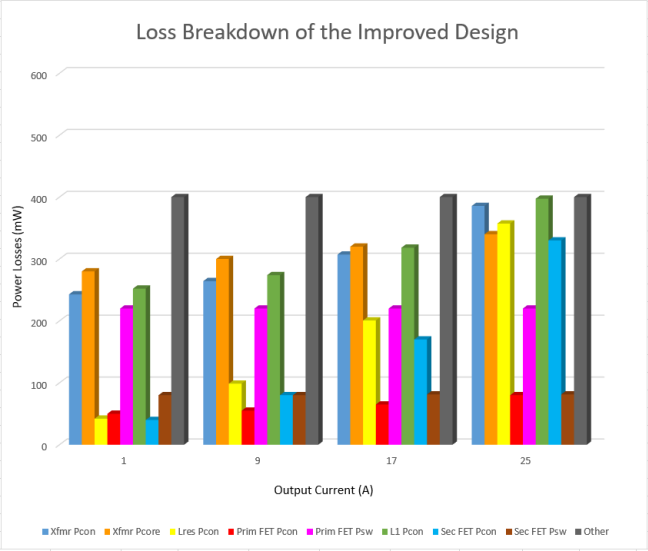

Figure 36 Loss breakdown of the improved design (N_e=9:1, L_{res}=3.6µH)

The loss breakdown comparison between the reference design and the improved design is shown in Figure 37. And transformer conduction loss, resonant inductor conduction loss, and FET conduction loss are respectively reduced in the improved design, mainly due to the rms current reduction. At minimum load, the improved design reduces total power losses by more than 170 mW. While at maximum load, the improved design reduces total power losses by more than 420 mW.

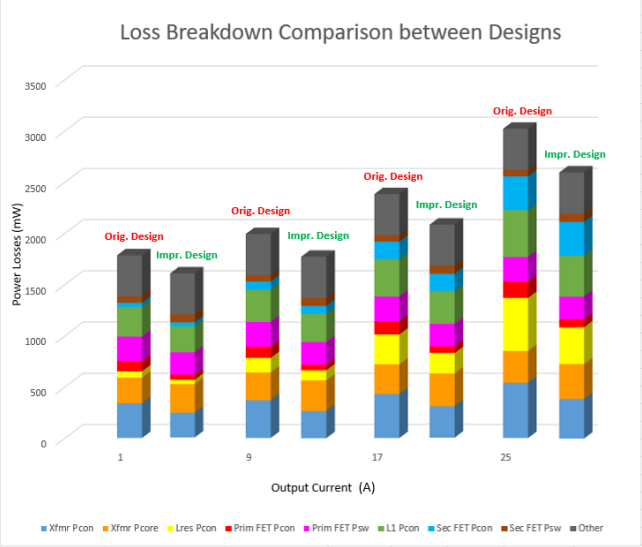

Figure 37 Loss breakdown comparison between the original reference design and the improved design

I. Transient Performance

Due to the quasi-resonant behavior of the resonant inductor L_{res} and capacitor C_{res} (a zero-order capacitor with no dynamics [39], because the capacitor voltage is forced to zero periodically), the dynamic response of this converter is very similar to a Buck derived converter. Therefore, a conventional PID controller can be used for output voltage regulation by controlling the switching frequency for the COT control. When the load transient frequency is above the BW of the converter, the converter loop will not help to reduce the closed loop output impedance of the regulator anymore. Therefore, the decoupling capacitor network or power delivery/distribution network (PDN) design becomes very critical to suppress the output voltage ripples by providing low enough output impedance [11][34]. In PDN and power integrity design, a target impedance is used to set the goal of the output impedance of the power source in the frequency domain [40]-[42]. And the target impedance can be set based on equation (29) [40]-[42], where ΔV_{max} is the allowable output voltage ripple and ΔI_{trans_max} is the maximum current transient step value. For example, if we choose $\Delta V_{max} = 50\ mV$ to leave 10 mV design margin (for 5% of 1.2V, that is 60 mV output voltage ripple or 120 mVpk-pk absolute maximum ripple) and $\Delta I_{trans\_max} = 25\ A$, the target impedance will be 2 mΩ (or ~ -54 dBΩ shown with a dashed green line in Figure 38).

$$Z_{\text{target}} = \frac{\Delta V_{\max}}{\Delta I_{trans\_\max}} \tag{29}$$

Closed loop output impedance is simulated with different design attempt parameters listed in Table 2 and the result is shown in Figure 38. To analyze the converter design parameter impact on the closed loop output impedance, in the simulations, the same PID controller is used (K_p=0.5, K_i=5000, K_d=4×10^{-6}). The system loop crossover frequency is >75 kHz and phase margin is >60 deg for all design attempts. From the result in Figure 38, it is worth noting that when the turns ratio N_e is changed from 7:1 (for example design attempt #1) to 9:1 (for example design attempt #3), the peak closed loop output impedance will become higher around 50 kHz, due to the worse loop response caused by the lower reflected secondary side voltage V_s. With the lower reflected secondary side voltage V_s in higher transformer turns ratio design attempts, the converter response performance, especially for loading transient (from light to heavy load), will be compromised, because 1) the rising slew rate of the output inductor current is decreased; and 2) the steady state duty cycle is closer to the maximum, resulting in limited headroom to further boost the duty cycle. The output inductor impact on the transient performance of QR-PSFB is very similar to the conventional Buck converter. When the output inductor is higher, the transient response of the converter will be degraded and the peak closed loop output impedance will be higher, too.

Therefore, there is a design optimization to make between transient performance and power conversion efficiency. After making the efficiency improvement with higher turns ratio N_e=9:1 and L_{res}=3.6 µH in section I.H, from the output impedance simulation in Figure 38, it shows that it is very marginal to continue the efficiency improvement trend by increasing turns ratio N_e or L_{res} further, as the closed loop output impedance is getting closer to the Z_{target}. However, with turns ratio N_e=9:1 and L_{res}=3.6 µH (in design attempt #3), the Z_{target} can still be met with one 330 µF SP-CAP [43] (Specialty Polymer Aluminum capacitor, self-resonant frequency is ~400 kHz) and thirty 22 µF MLCCs (Multilayer Ceramic Capacitors, self-resonant frequency is ~2 MHz). Further suppression on the output impedance can be made by adding more SP-CAPs, but the solution size and cost will be increased.

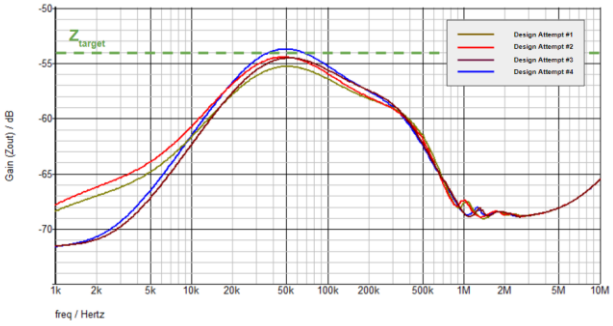

Figure 38 Closed loop output impedance comparison with different design attempt parameters

The transient performance of the prototype is tested with high rate current transient (di/dt>10A/µs) at different load switching frequencies. And the scope is set to fast acquisition, so that we can see multiple transient events. The load tester will report the transient current in a voltage signal with the gain of 15mV/A and 0% to 100% of I_{o_max} is used for load step.

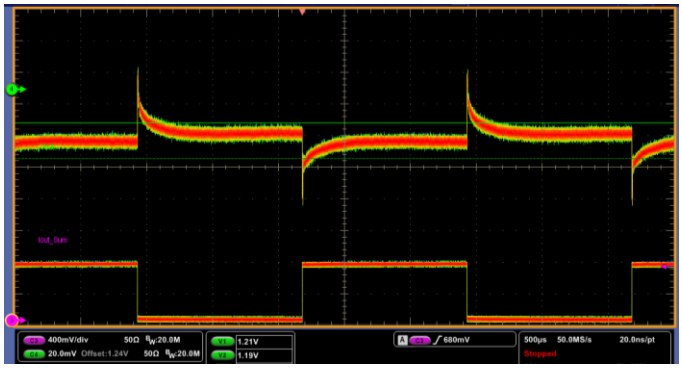

Figure 39 Load transient performance at 400Hz switching, 0-25A, 12.5A/μs (CH3-Pink: current reporting signal for the load tester, 15mV/A; CH4-Green: Output Voltage with 20MHz BW)

The transient performance of the prototype is tested at 400Hz load switching to show the loop response of the converter. The output variation is ~87mVpk-pk.

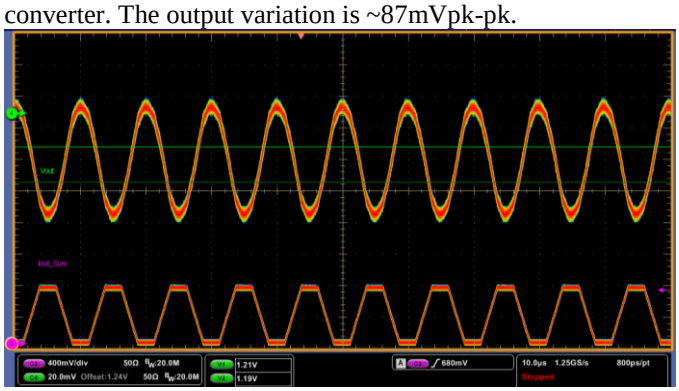

Figure 40 Load transient performance at 100kHz switching, 0-25A, 12.5A/μs (CH3-Pink: current reporting signal for the load tester, 15mV/A; CH4-Green: Output Voltage with 20MHz BW)

The transient performance of the prototype is tested at 100kHz load switching to show the loop response of the converter and this frequency is just over the bandwidth of the converter. The result shows that at 100 kHz, the PDN design is sufficient to meet the target output impedance. The output variation is ~82mVpk-pk. Load transient with frequency sweeping for a wide range of the PDN validation is shown next.

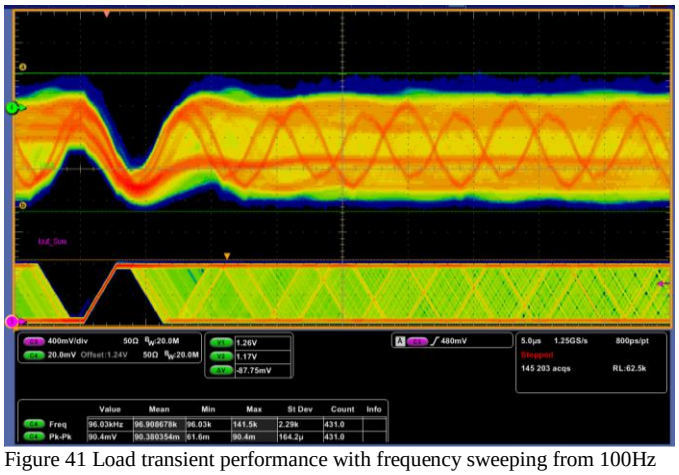

Figure 41 Load transient performance with frequency sweeping from 100Hz to 200kHz, 0-25A, 12.5A/μs (CH3-Pink: current reporting signal for the load tester, 15mV/A; CH4-Green: Output Voltage with 20MHz BW)

To scan the full closed loop output impedance using different switching load [11][34], the scope is set to fast acquisition + infinite persistence mode. We can measure the worst-case output voltage variation is 90.4mVpk-pk across the frequency range of 100Hz to 200kHz, which meets the ±5% of 1.2V (120mVpk-pk absolute maximum ripple) requirement and leaves ~25% performance margin. This matches the simulation result in Figure 38 very well, where the peak closed loop output impedance is -54.5 dB (equivalent to 92mVpk-pk output voltage ripple).

VI. Conclusion

In this paper, a new modeling technique for a QR-PSFB converter is presented. In section II, power architecture for 54V-PoL using 2 stage conversion is reviewed. And the conventional PSFB is reviewed and the issues of this topology are highlighted. In section II, the QR-PSFB with COT control is presented under light and heavy load conditions and this section provides the fundamental for the modeling. Equivalent circuit and state equation are studied for each of the modes in QR-PSFB converter in section III and tank current and voltage information is solved for different operating conditions. Design guidelines are provided for a 54V-1.2V 25A reference design in section IV, including ZVS range, power losses, power capability, and component tolerances. Design improvement is made based on the modeling results and guidance. Simulation and experimental results are provided to verify the modeling technique in a 54V-1.2V 25A DC-DC converter design and confirm the accuracy of the proposed modeling method.

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