Modeling Capacitor Derating in Power Integrity Simulation

Tianjian Lu, Ken Wu, and Zhiping Yang
Google Inc.
1600 Amphitheatre Parkway,
Mountain View, California 94043
Email: lutianjian@gmail.com,
{kenzwu, zhipingyang}@google.com

Jian-Ming Jin
Department of Electrical and Computer Engineering
Univeristy of Illinois at Urbana-Champaign
Urbana, Illinois 61801
Email: j-jin1@illinois.edu

***Abstract*—In this work, we propose a simulation methodology that incorporates derating models of decoupling capacitors for power integrity analysis. The construction of the derating models of decoupling capacitors is based on the impedance measurement and curve fitting method. Three approaches of impedance measurement are compared and the most accurate one is selected to build the derating models. The curve fitting method converts the measured impedance into circuit models. A library file containing the derating models is generated such that it can be repeatedly used for different products at various design cycles. The derating library takes into account the operation conditions such as temperature and DC bias as well as the vendor information. The proposed simulation methodology with the derating library achieves high accuracy, which is demonstrated through correlations with measurements.**

I. Introduction

The design of power distribution networks (PDNs) has become increasingly important in a modern electronic system especially under the trend of system miniaturization and continuous reduction of voltage noise margin. A power distribution network is responsible for delivering clean voltage and current from a voltage regular module (VRM) all the way to transistors through a hierarchy of interconnects. The target impedance [1] based on Ohm's law and calculated from power supply voltage and switching current is considered as one of the most useful quantities in evaluating a PDN. Decoupling capacitors play a critical role in a PDN to maintain the low-impedance path from the VRM to the processor over a broadband [1]–[4]. Decoupling capacitors can also suppress excessive noise on the power rails. However, as the frequency increases beyond a self-resonant frequency, the series loop inductance of a decoupling capacitor dominates and the decoupling capacitor becomes inductive and hence less effective in maintaining a low impedance. Another problem associated with the decoupling capacitors is the derating issue that the decoupling capacitors often function at lower capacitance than their rated specifications. Derating of capacitors takes place under normal working conditions associated with temperature, voltage, and aging, etc. Capacitor derating and its modeling has drawn industry-wide concerns [5]. It is known that in order to speed up the design cycles, advanced modeling and simulation techniques [6], [7] must be employed at the system level. The decoupling capacitor models that are incorporated into a system-level simulation of a PDN have significant impact on the simulation results. An example is shown in Fig. 1. The system-level simulation to calculate PDN impedance takes three types of capacitor models, namely, the ideal model treating each capacitor as a lumped component with its rated capacitance, the derating model based on the operation condition of 1 V and 50 °C, and a second derating model based on the operation condition of 1.5 V and 85 °C. As shown in Fig. 1, the maximum impedance between the ideal model and the derating model of 1 V and 50 °C has a difference of 26% at 10 kHz, whereas at the same frequency the two derating models differ by 16%. The large variance of impedance invoked by capacitor models further demonstrates the importance of incorporating accurate models of decoupling capacitors in the system-level simulation of a PDN.

In this work, we propose a simulation methodology that incorporates a library of capacitor deraing models. The capacitor derating library, associated with operation temperature and voltage and based on impedance measurement and curve fitting, can be repeatedly used for PDN simulation and optimization at different design cycles and for different products. Three methods of impedance measurement with individual characterization fixtures and de-embedding techniques are compared and the most accurate one is selected to construct the derating library. Since circuit models are often preferable in the system-level simulation, a curve fitting method is used to convert the measured impedance into SPICE models. The conversion from impedance network parameters to SPICE models is achieved through gradient-based optimization. Even though rated with the same specifications including capacitance, package size, temperature characteristics, and operation voltage, capacitors from vendors may have distinct impedance. Vendor information has also been taken into account in designing the structure of the derating library especially in determining the nominal case. System-level simulations utilizing the capacitor derating library are carried out for calculating the impedance of PDNs in real products. The accuracy of the proposed simulation methodology is verified through good correlations with measurement.

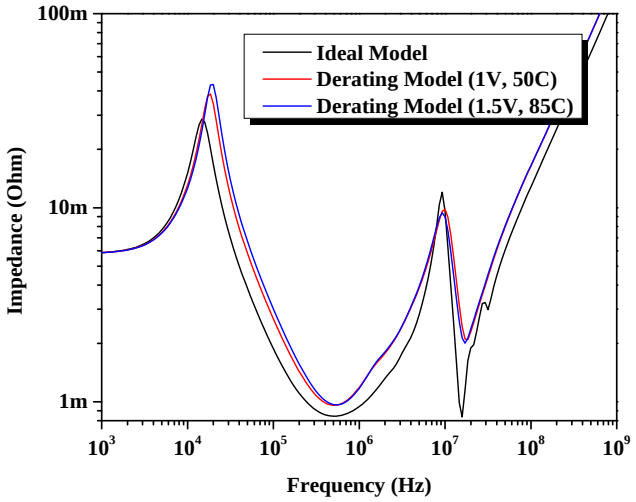


Fig. 1: Simulating the impedance of a PDN by using ideal and derating models of decoupling capacitors. The ideal model treats the capacitor as a single lumped component with its rated capacitance. The simulation with derating models is proposed in this work.

II. Capacitor Derating Models

The proposed system-level simulation incorporates the derating models of decoupling capacitors, which are built upon impedance measurement and curving fitting method. In this section, detailed information of the impedance measurement and fitting methods is provided.

A. Impedance measurement

Three impedance measurement methods of decoupling capacitors are compared, including the method proposed by Intel [8], [9], the approach used by a component manufacturer named vendor A in this work, and the solution from a third-party consultant. Three types of capacitors from vendor A are taken as measurement samples, namely, 0201 1 uF, 0402 10 uF, and 0603 22 uF. Through the comparison, we would like to select the most accurate impedance measurement method to construct the capacitor derating library.

The measurement set-up is illustrated in Fig. 2, which consists of a Keysight E5061B network analyzer, two RF probes of 0.4 mm pitch and two TP150 precision positioners from PacketMicro [10], a microscope, cables, and PCB holders. The SOLT calibration is performed with CalKit TCS60 [10], which achieves the calibration till the tips of the RF probes.

All the three impedance measurement methods under comparison are based on the concept of S-parameter two-port shunt-thru methodology, which is devised for high-frequency PDNs of very low impedance. With the two-port shunt-thru method, the measured impedance within the range of 10% accuracy can be as low as 1 mΩ up to about 3 GHz [11]. In the two-port shunt-thru method, one port launches current to

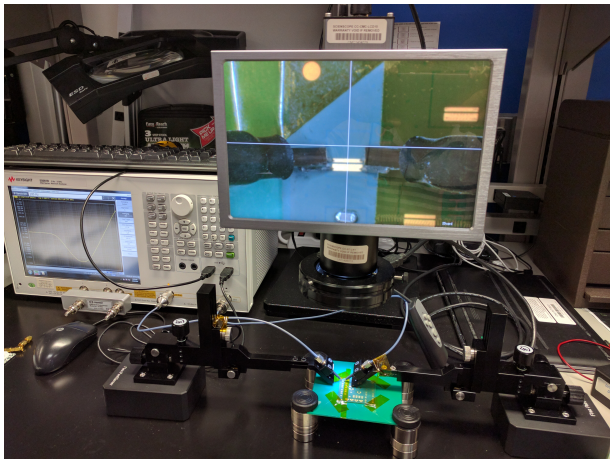


Fig. 2: Impedance measurement set-up consists of Keysight E5061B network analyzer, RF probes, precision positioners, microscope, cables, and PCB holders.

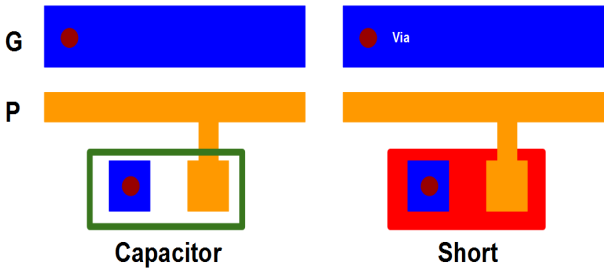


Fig. 3: Test fixtures from Intel for impedance measurement of capacitors. The ground pad is connected to the ground trace through vias. In the short fixture, the power and ground pads to mount the component are shorted together.

he Device Under Test (DUT) and the other port measures the voltage across it. The impedance of the DUT Z_{DUT} can be derived in terms of the measured S_{21}

$$Z_{\text{DUT}} = 25\frac{S_{21}}{1 - S_{21}}, \tag{1}$$

assuming that the port impedance is 50 Ω [11], [12].

To perform the impedance measurement, capacitors have to be mounted on some test fixtures. The test fixture of such purpose from Intel is shown in Fig. 3. In order to obtain the impedance of the capacitor itself, a process, known as de-embedding, has to be performed to remove the effects of traces and vias in the test fixture. The de-embedding of the Intel approach is realized through a short fixture as shown in Fig. 3. Two measurements are performed, one for the impedance of the entire structure with capacitor mounted on as Z_{tot} and one for the impedance of the short fixture as Z_{short}. The impedance of the capacitor itself Z_{cap} can thus be obtained through a subtraction

$$Z_{\text{cap}} = Z_{\text{tot}} - Z_{\text{short}}. \tag{2}$$

It is worth mentioning that if the 3-D geometry of the test fixture for mounting capacitors is available, the de-embedding

can be achieved through a full-wave electromagnetic simulation, which saves the effort of fabricating a short fixture. A wave port can be attached at the location where the capacitor is mounted. The obtained S-parameters from the simulation can then be converted to Z-parameters, with which the de-embedding is performed together with the measured Z_{tot}.

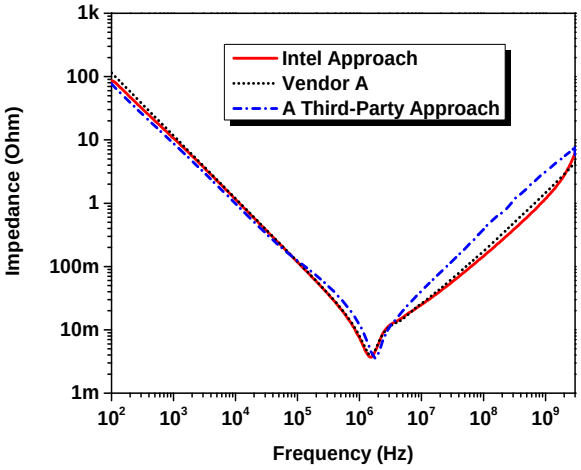
Figure 4 shows the measured impedance versus frequency of the sample capacitors by using the methods from Intel, vendor A, and the third-party consultant. It can be seen from Fig. 4(a) that the in-house measurements using Intel and vendor A approaches achieve good agreement. However, there is a large discrepancy of the measured impedance based on the third-party approach from the other two. The large discrepancy is believed to arise from lacking verifications in the de-embedding test fixtures. Due to the large discrepancy, the impedance curve measured using the third-party approach is only shown in Fig. 4(a) for the 0603 22 uF capacitor.

B. Curve fitting method

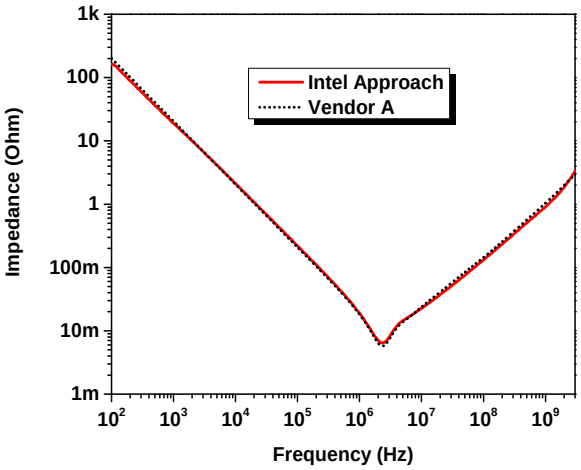
Circuit models are often preferred in the system-level simulation of PDNs. Through the curve fitting method illustrated in this section, the measured impedance of capacitors can be converted to SPICE models. There are three steps involved in the curve fitting method: fixing a circuit topology; tuning the major RLC branch for a good initial guess; and building an object function and selecting the most appropriate optimization method. The fixed circuit topology is shown in Fig. 5, which consists of a major RLC (in series) branch, five RC (in shunt) sections, four RL (in shunt) sections, and four RLC (in shunt) sections. It is known that the simplest SPICE model of a decoupling capacitor consists of three lumped components: the capacitance, the equivalent series resistance (ESR), and the equivalent series inductance (ESL) [13], [14]. Due to the high-order behavior of the measured impedance around the self-resonant frequency, the simple RLC model is insufficient. However, the tuning of the major RLC branch based on the first-order representation of a decoupling capacitor provides a good initial guess for the optimization. The cost function is defined as the weighted summation of the mean values of the relative changes for both magnitude and phase of the complex impedance, which can be written as

$$f = \frac{1}{N}\sum_{i=1}^{N}\left(\alpha_A \frac{A_i - A_{0,i}}{A_{0,i}} + \alpha_\phi \frac{\phi_i - \phi_{0,i}}{\phi_{0,i}}\right), \qquad (3)$$

where A and ϕ represent the magnitude and phase of the impedance, respectively, and α_A and α_ϕ are the corresponding weights in the summation. Gradient-based optimization technique from Keysight Advanced Design System (ADS) is used. The fitting results are shown in Fig. 6 for three sample capacitors from vendor A. The same topology shown in Fig. 5 is used in converting the measured impedance of the three capacitors into SPICE models. It can be seen from Fig. 6 that the fitting results agree well with the measurement results for both magnitude and phase. It is worth mentioning that with the same topology, the fitting result for the capacitor of larger



(a)



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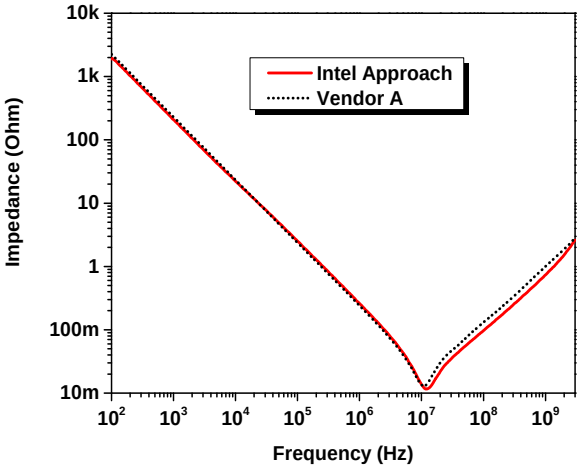


(c)

Fig. 4: Measured impedance with three different approaches of three sample capacitors (a) 0603 22 uF, (b) 0402 10 uF, and (c) 0201 1 uF.

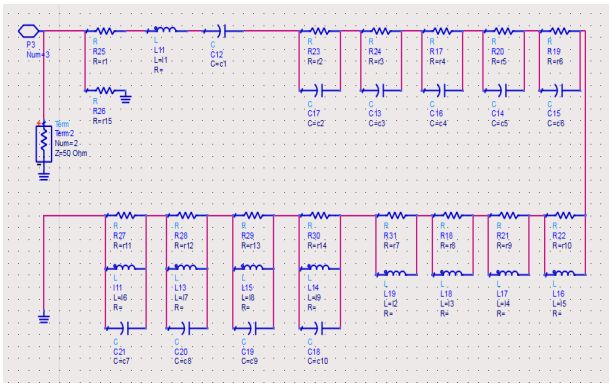


Fig. 5: Fixed circuit topology used for curve fitting.

value has larger discrepancy at low frequencies. The accuracy can be improved by including more branches in the topology.

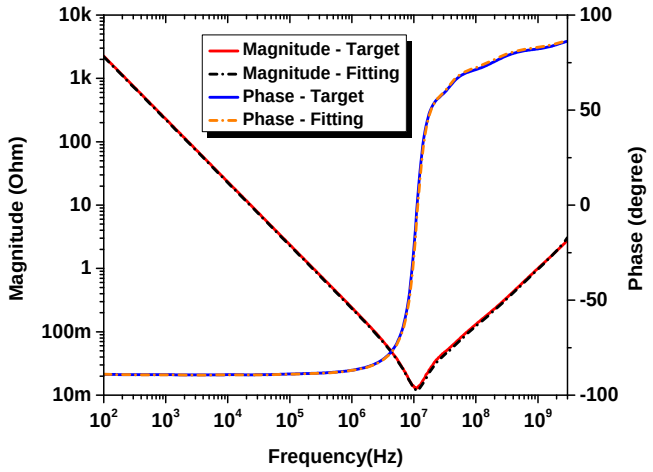
III. System-Level Simulation and Measurement Correlation

Capacitors employed in a PDN are often provided by various vendors. Even though rated with the same capacitance, package size, temperature coefficient, capacitors from different vendors are most likely to have distinct impedance. We have observed that among the three vendors capacitors from vendor A have nominal values in terms of capacitance, ESR, and ESL. Therefore, the derating models based on capacitors from vendor A are chosen as the nominal case in the system-level simulation.

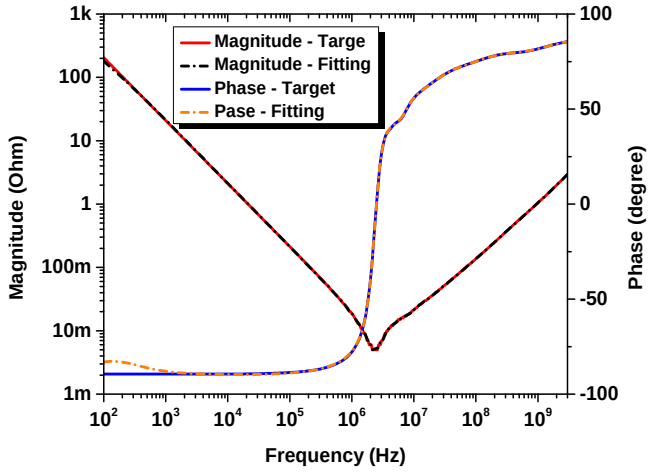
Measurement correlations are performed to verify the accuracy of the proposed simulation methodology with the constructed derating library. The PDNs for six different power domains on a laptop computer were measured and simulated. It can be seen from Fig. 7 that the simulated impedance with the derating library agrees very well with the measurement. In Fig. 7(c), at 10 kHz, the relative difference between the measured and simulated impedance with derating library is about 7%, whereas it is as large as 33% between the measured the simulated impedance with ideal capacitor models. Similarly, for the power domain in Fig. 7(d), the relative difference between the measurement and the simulation with the derating library is 3.4%, whereas it is around 34% between the measurement and the simulation with ideal capacitor models. The measurement correlations not only demonstrate the high accuracy of the proposed simulation methodology, but also prove the necessity and the importance of taking into account capacitor derating in the system-level simulation.

IV. Conclusion

In this work, we propose the system-level power integrity simulations that incorporates the derating models of decoupling capacitors. The derating models of decoupling capacitors are constructed through the impedance measurement and curve fitting method. The impedance measurement is based on the concept of two-port shunt-thru method considering the very low impedance of the high-frequency PDNs under



(a)



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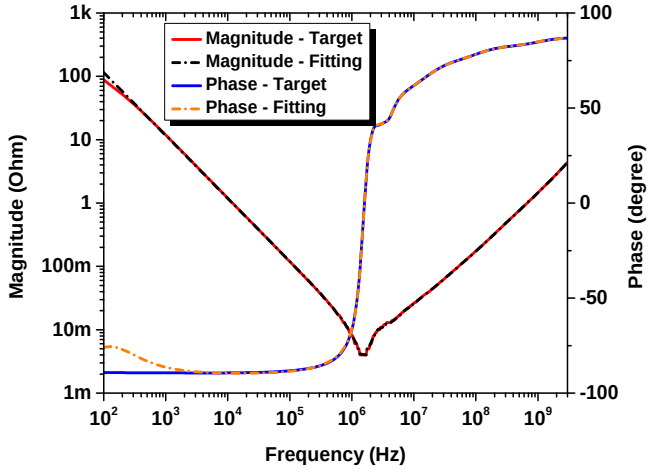
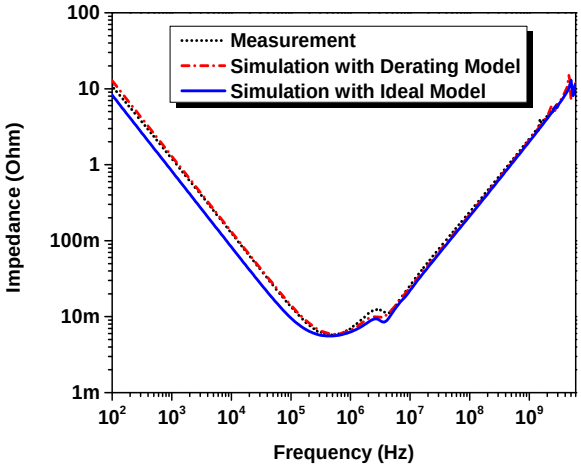
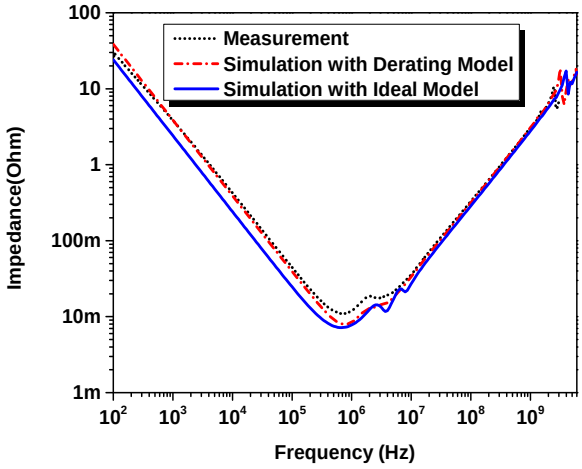


(c)

Fig. 6: Fitting results including both the magnitude and phase for three different capacitors including (a) 0201 1 uF, (b) 0402 10 uF, and (c) 0603 22 uF.



(a)



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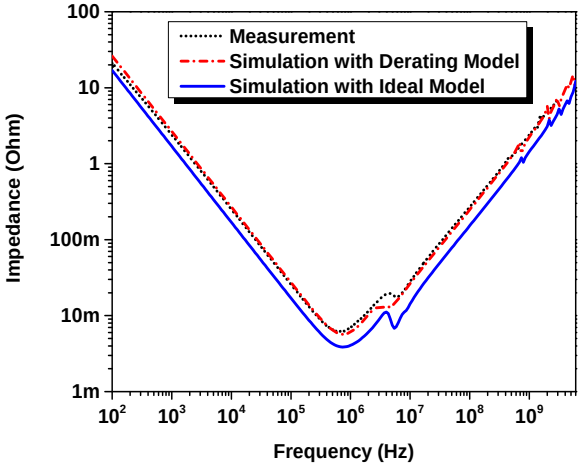

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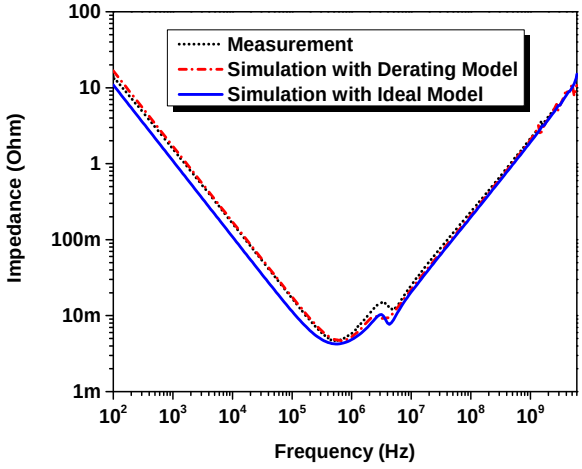

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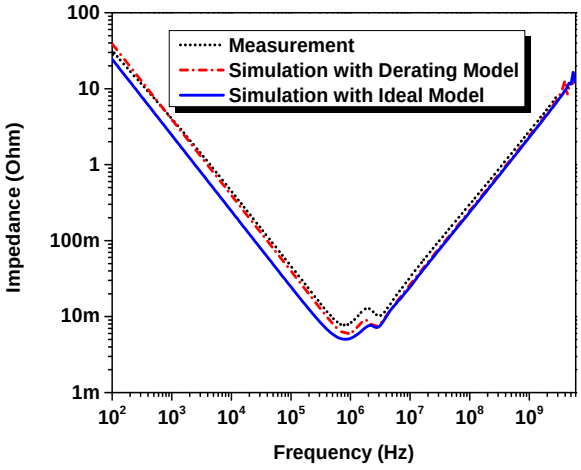
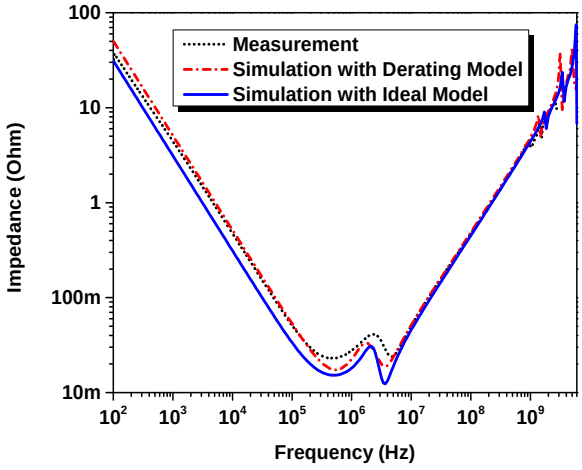


(e)



(f)

Fig. 7: Measurement correlations of the proposed simulation methodology on six different power domains.

investigation. Three methods of impedance measurement from Intel, vendor A, and a third-party consultant are compared and the most accurate one from vendor A is taken to perform the impedance measurement. Since circuit models are often preferred in the system-level simulation, a curve fitting method is employed to convert the measured impedance into circuit models. The fitting method is based on gradient-based optimization with the cost function built with both magnitude and phase of the measured impedance. The accuracy of the proposed simulation methodology is demonstrated through good correlations with measurement performed on the real products. The good agreement between the measurement and the simulation with derating library again demonstrates the importance of considering derating effects of decoupling capacitors in the power integrity simulation.

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