Cascode Switching Modeling and Improvement in Flyback Converter for LED Lighting Applications

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Abstract – Modeling of the cascode switching structure used in Flyback converter for achieving fast startup in the deeply dimmed phase-cut LED driver is presented in this paper. The cascode structure's inherent instability and oscillation issue is modeled and analyzed quantitatively. Three solutions are proposed to stabilize the structure and suppress the unstable voltage oscillation. Solutions are studied using the proposed model for design robustness. And this model can be further applied to the popular new high voltage (for example 650V) cascode GaN FET technology. Experimental results of a 20W phase-cut dimmable LED driver are demonstrated to verify the proposed modeling method and solutions.

***Index Terms*—Cascode Switching, Universal AC Input, Dimmable LED Drivers, Small Signal Model, Flyback Converter Modeling, GaN Power Devices.**

I. INTRODUCTION

A major challenge of phase-cut dimmable LED driver is to turn on the LED at the minimum dimming position [1]-[4]. Many commonly used phase-cut dimmers can provide down to 20 *deg* phase conduction angle at the bottom of the dimming curve [4]. And the voltage level from the input AC line voltage is only about 20-30 V_{rms}, which makes the regular internal HV startup (available in some controller *IC*) with a resistor very inefficient, or it suffers from a very long time of delay to generate the light output. Therefore, a dedicated startup power supply is needed to charge up the V_{cc} of the controller *IC* to initialize the power sequence, shown in Figure 1. The HVFET is highlighted in red and configured as an emitter follower to bias the V_{cc} of the controller during startup. It is worth noting that HVFET is operated in linear mode during this period. After the switching of the converter is established, the winding auxiliary power supply will take over and reverse bias D_s and shut down the startup power supply.

Instead of adding an HVFET for a startup power supply, a very popular implementation is the cascode switching configuration for the Flyback switch [4]. The cascode switching configuration uses an LVFET for startup instead of an HVFET to save the cost difference.

In Figure 2, cascode switching configured Flyback converter is shown. V_{in} charges the gate of the HVFET via a resistor R_g, and the zener Z_g and capacitor C_g maintain the gate voltage to a stable level. During startup, the gate of the HVFET is charged up to Z_g voltage and HVFET operates in the linear mode and V_{cc} voltage will be around (V_{zg}-V_{th}-V_F), where V_{th} is the threshold of the HVFET and V_F is the forward voltage of the D_s. A diode D_g is reversely connected between gate and source to protect the LVFET from over-voltage damage.

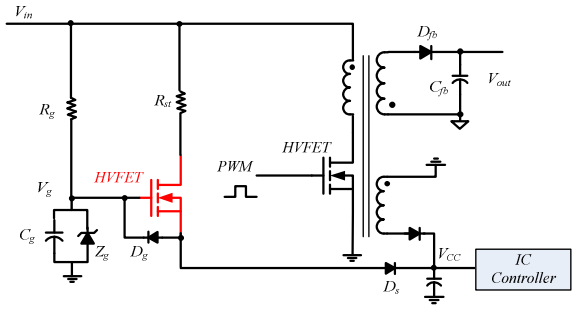


Figure 1 Conventional HV Startup supply with HVFET

When the V_{cc} is charged up to the power-on voltage threshold of the *IC* controller, the *PWM* signal from the *IC* controller will switch on and off the LVFET. When the LVFET is turned on, the drain of the LVFET (the source of the HVFET) will be pulled down to near-zero. The voltage across gate-source of HVFET is V_g and the HVFET will be also turned on. When the LVFET is turning off, the drain voltage of the LVFET (the source of the HVFET) is increasing to V_g-V_{th}. Once the voltage across gate-source of HVFET is lower than V_{th}, HVFET is switched off. It is noticed that this configuration offers faster switching speed compared with a regular gate switching FET, due to the fact of removal of gate charge delay of the HVFET and the high gain/bandwidth of this configuration. The gate-source of HVFET swings from V_g to V_{th}. And the gate charge of the LVFET is significantly lower than the HVFET for the same switching speed.

As the fast switching speed and high bandwidth provided by this configuration, high-frequency oscillation is observed during the hard switching. When the LVFET is switching off, due to the parasitic ringing on the drain-source, the induced AC voltage across gate-source of HVFET will be amplified to the output of the drain-source and this signal will be fed back to the drain-source of LVFET and increase the amplitude of the ringing. When this positive feedback is established, the operation of the Flyback will be improper and the controller *IC* could malfunction due to the high-frequency noise of the cascode switching configuration spreading to auxiliary

winding voltage, current sensing signal, etc. Detailed analysis of this mechanism will be conducted in section II through small signal modeling. Three solutions are studied using the proposed model to suppress the voltage oscillation and stabilize the system in section III. Design parameters are analyzed in section IV for robust operation. Experimental results are demonstrated in section V. Finally, conclusions are drawn and future work is outlined in section VI. The same technique can be applied to analyze the new high-voltage Cascode GaN FET [10], during inductive hard switching.

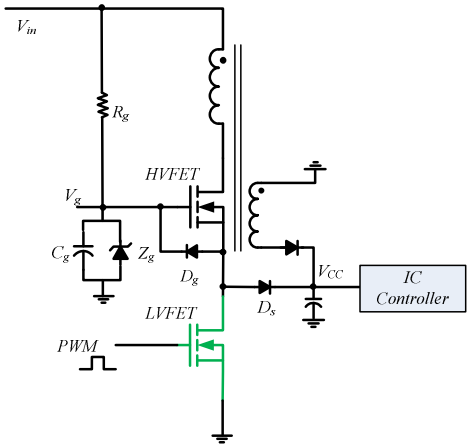


Figure 2 Cascode Switching Configured Flyback converter

II. MODELING OF THE CASCODE SWITCHING

A. *Small Signal Model of the Conventional Cascode Amplifier*

The basic MOS cascode amplifier circuit is shown in Figure 3 (a), where the top MOSFET Q2 is connected in common-gate (CG) configuration and the bottom MOSFET Q1 is set in common-source (CS) configuration [11]. The small signal output equivalent circuit model is shown in Figure 3 (b), where the G_m is the equivalent transconductance and R_o is the output resistance of the circuit model.

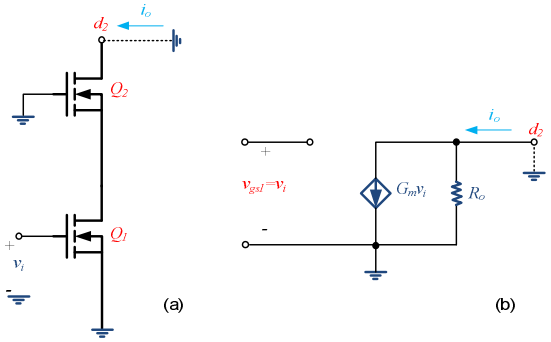


Figure 3 (a) A MOS cascode amplifier prepared for small-signal calculations; (b) output equivalent circuit of the amplifier in (a)

The equivalent transconductance of the model is defined as in (**1**).

$$G_m = \frac{i_o}{v_i} \tag{1}$$

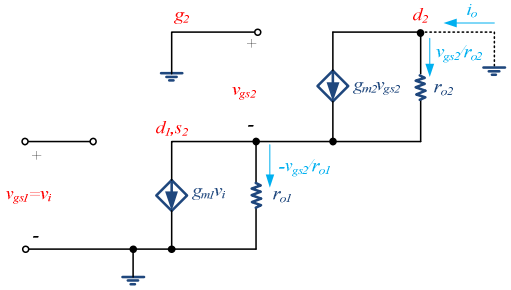


Figure 4 Small signal equivalent circuit of the cascode amplifier

The small signal equivalent circuit of the cascode amplifier is shown in Figure 4. The input signal v_i is the gate-source voltage v_{gs1} of Q_1. g_{m1} and g_{m2} are the transconductances, while r_{o1} and r_{o2} are the output resistance of the FET Q_1 and Q_2 respectively.

At the d_1 or s_2 node, we can write the KCL equation in (**2**).

$$g_{m2}v_{gs} + \frac{v_{gs2}}{r_{o1}} + \frac{v_{gs2}}{r_{o2}} = g_{m1}v_i \tag{2}$$

The output resistances r_{o1} and r_{o2} of the FETs are very high in this application and the equation above (**2**) can be simplified into (**3**).

$$g_{m2}v_{gs2} \approx g_{m1}v_i \tag{3}$$

To derive the transconductance G_m of the model as defined in (**1**), we can virtually short the d_2 node to ground. The output current i_o shown in Figure 3 and Figure 4 can be expressed as equation (**4**).

$$i_o = g_{m2}v_{gs2} + \frac{v_{gs2}}{r_{o2}} = \left(g_{m2} + \frac{1}{r_{o2}}\right)\cdot v_{gs2} \tag{4}$$

Again, since the output resistances r_{o2} of the FET is very high and the equation above (**4**) can be simplified into (**5**), where G_m is equal to g_{m1}. The output resistance of the equivalent circuit shown in Figure 3 can be found (with controlled current source $g_{m1}v_i$ open) in equation (**6**). The CG transistor Q_2 increases the output resistance of the cascode amplifier by the factor of $g_{m2}r_{o2}$, which is its intrinsic gain.

$$i_o = g_{m2}v_{gs2} + \frac{v_{gs2}}{r_{o2}} = \left(g_{m2} + \frac{1}{r_{o2}}\right)\cdot v_{gs2} \approx g_{m2}v_{gs2} = g_{m1}v_i = G_m v_i \tag{5}$$

$$R_o = r_{o1} + r_{o2} + g_{m2}r_{o1}r_{o2} \approx (g_{m2}r_{o2})r_{o1} \tag{6}$$

Finally, the open loop gain of this amplifier can be written as (**7**).

$$A_{vo} = \frac{v_o}{v_i} = -g_{m1}R_o = -(g_{m1}r_{o1})(g_{m2}r_{o2}) \tag{7}$$

B. *5.5.2 New Small Signal Model of the Cascode Switching during off-transition*

To analyze the high-frequency behavior of the cascode structure, the HVFET drain-source capacitance C_{ds} and the miller capacitance $C_{gd} << C_{ds}$ are lumped into C_1 ($\approx C_{oss}$) to simplify the model. In Figure 5 (a) and (b), it shows the equivalent circuit at the moment when the Flyback converter

secondary side diode starts conducting and the voltage on the top side of the leakage inductor L_1 is (V_{in}+N·V_{out}), where V_{in} is the input voltage, N is the transformer turns ratio and V_{out} is the output voltage. Further, the LVFET can be modeled simply as the output capacitance C_2, since its channel has been turned off completely. The HVFET is modeled in Figure 5 (c) using the small signal equivalent circuit [11], where g_m is the transconductance and r_o is the output resistance for Early Effect. All the components used in the model are assumed to be fixed values. The non-linearity and the operation dependency are ignored for simplicity. For example, the output capacitance of the FET C_1 or C_2 is drain-source voltage V_{ds} dependent, but in the proposed model, it is modeled as a fixed value around its DC operating voltage. Similarly, for g_m and r_o, fixed values are used, too. A wide range of parameter values will be studied after the model is established, so all the non-linearity and operation dependency would be covered.

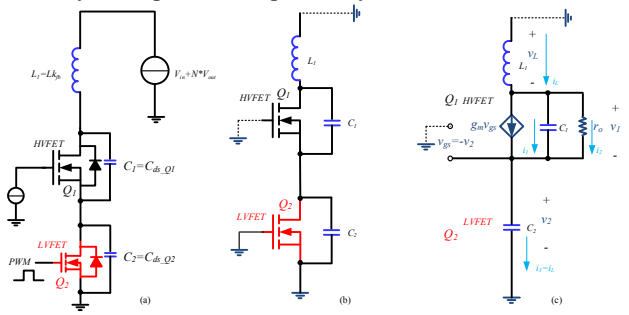


Figure 5 (a) Equivalent circuit for cascode switching Flyback; (b) Off-transition of cascode structure; (c) Small signal model of the cascode switching during off-transition

In Figure 5 (c), we can apply KCL at the source of the HVFET Q_1 in equation (**8**).

$$g_m v_{gs} + \frac{v_1}{r_o} + C_1 \frac{dv_1}{dt} = i_3 = C_2 \frac{dv_2}{dt} = i_L \tag{8}$$

In Figure 5 (c), we can also apply KVL to the equivalent circuit and the equation is written in (**9**).

$$v_L = -(v_1 + v_2) = L_1 \frac{di_L}{dt} \tag{9}$$

Combine equations (**8**) and (**9**), the system diagram can be built in the frequency domain, which is shown in Figure 6 (a). The diagram can be further simplified into the Figure 6 (c).

From the system diagram shown in Figure 6 (c), the characteristic equation can be written in equation (**10**).

$$\begin{aligned} &1+G(s)\cdot H(s)= \\ &s^3 L_1 C_1 C_2 r_o + s^2 L_1 C_2 + s(C_1 r_o + C_2 r_o) + g_m r_o + 1 = 0 \end{aligned} \tag{10}$$

If we consider $V_1(s)$ (V_1 is the V_{ds} voltage of Q_1) as the output of the system, the system diagram can be simplified in Figure 7.

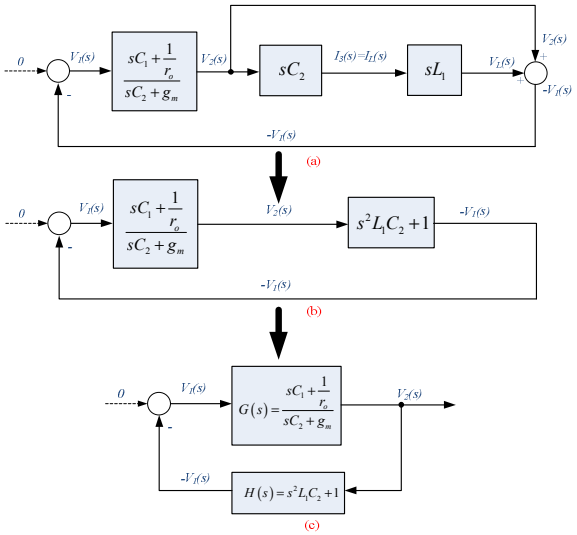


Figure 6 System block diagram and the equivalents in s domain

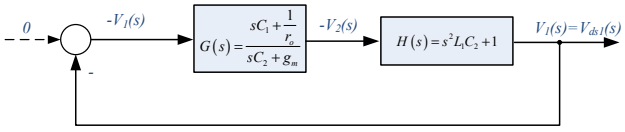


Figure 7 System diagram for $V_1(s)$ as the output variable

The open loop gain $G(s)H(s)$ can be written in (**11**).

$$G(s)\cdot H(s) = \frac{sC_1 + \frac{1}{r_o}}{sC_2 + g_m} \cdot \left(s^2 L_1 C_2 + 1\right) \tag{11}$$

And the analysis results will be shown later in section III.

III. SMALL SIGNAL MODELING OF THE RINGING SUPPRESSION METHODS

The solution A shown in Figure 8 can be modeled using the same method during off-transition and the extra output capacitance C_{ds2} (in green) is added between drain and source of the LVFET Q_2 and in parallel with C_2.

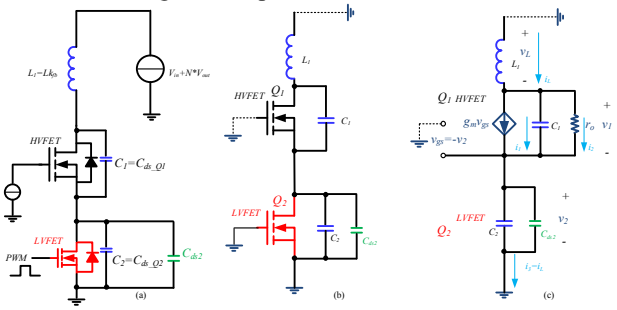


Figure 8 (a) Equivalent circuit for cascode switching Flyback with additional drain-source capacitor on the LVFET, solution A; (b) Off-transition of cascode structure with additional drain-source capacitor on the LVFET; (c) Small signal model of the cascode switching during off-transition with additional drain-source capacitor on the LVFET

The equivalent circuit for cascode switching Flyback with an additional gate-source capacitor in solution C on the HVFET Q_1 is shown in Figure 9. Due to the constant voltage

at the gate of the HVFET Q_1, from small signal AC perspective, the extra gate-source capacitance C_{gs1} will be in parallel with the output capacitance of the LVFET Q_2, as shown in Figure 9 (c). Therefore, the solution A and C are equivalent from a small signal model point of view.

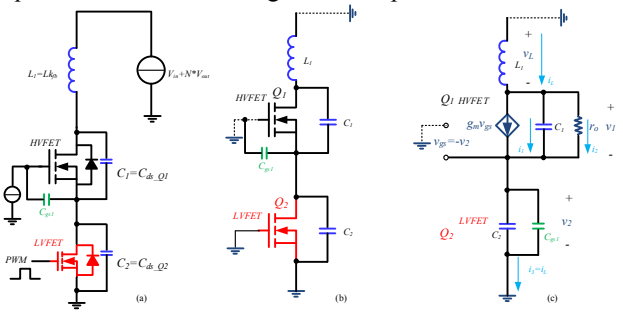


Figure 9 (a) Equivalent circuit for cascode switching Flyback with additional gate-source capacitor on the HVFET, solution C; (b) Off-transition of cascode structure with additional gate-source capacitor on the HVFET; (c) Small signal model of the cascode switching during off-transition with additional gate-source capacitor on the HVFET

Using the system diagram shown in Figure 6 (c), the characteristic equation of the solutions A and C can be written in equation (**12**), where $C_2' = C_2 + C_{gs1}$.

$$\begin{aligned} &1+G(s)\cdot H(s)=s^3L_1C_1C_2'r_o+s^2L_1C_2' \\ &+s\left(C_1r_o+C_2'r_o\right)+g_mr_o+1 \\ &=s^3L_1C_1\left(C_2+C_{gs1}\right)r_o+s^2L_1\left(C_2+C_{gs1}\right) \\ &+sr_o\left(C_1+C_2+C_{gs1}\right)+g_mr_o+1=0 \end{aligned} \tag{12}$$

The equivalent circuit for cascode switching Flyback with RC snubber improvement, which is proposed as solution B is modeled in Figure 10. The RC snubber is added between the drain of HVFET Q_1 to the source of the LVFET Q_2.

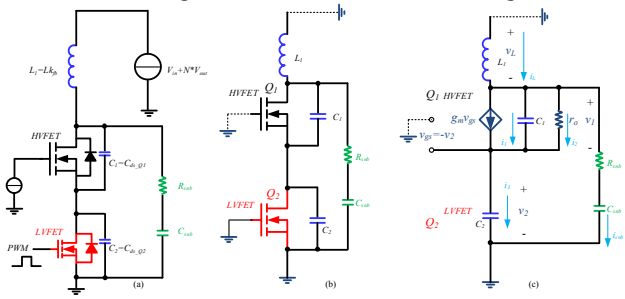


Figure 10 (a) Equivalent circuit for cascode switching Flyback with RC snubber, solution B; (b) Off-transition of cascode structure with RC snubber; (c) Small signal model of the cascode switching during off-transition with RC snubber

System block diagram with RC snubber to suppress the oscillation is shown in Figure 11.

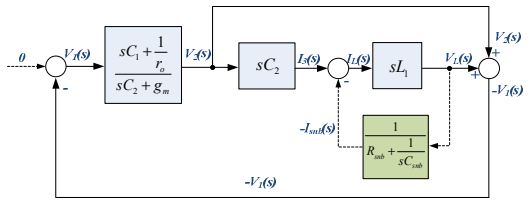


Figure 11 System block diagram with RC snubber R_{snb} and C_{snb}

The characteristic equation can be written in (**13**).

$$\begin{aligned} &s^4L_1C_1C_2C_{snb}R_{snb}r_o+s^3\begin{pmatrix}L_1C_1C_2r_o+L_1R_{snb}C_2C_{snb}+\\L_1r_oC_2C_{snb}+L_1r_oC_1C_{snb}\end{pmatrix} \\ &+s^2\begin{pmatrix}L_1C_2+R_{snb}C_2C_{snb}r_o+R_{snb}C_1C_{snb}r_o\\+gr_oL_1C_{snb}+L_1C_{snb}\end{pmatrix} \\ &+s\begin{pmatrix}C_2r_o+gr_oR_{snb}C_{snb}+\\R_{snb}C_{snb}+C_1r_o\end{pmatrix}+gr_o+1=0 \end{aligned} \tag{13}$$

And the analysis results will be shown later in section IV.

IV. Design Analysis to Stabilize the Cascode Structure

Using MATLAB, the roots of the characteristic equation or the closed-loop system poles in equation (**10**) and (**12**) can be plotted with different design parameters and variables for the original cascode structure and the stabilization solution A and C. There are three poles in the system. The nominal design parameters used in the model are shown in Table 1. In each of the cases, only one design parameter is varying and the rest of the design values are fixed using the nominal values.

Table 1 Design parameters and variation range for the original cascode structure and the stabilization solution A and C

Designator	Nominal Value	Variation Range	Figure #
C_1	120 pF	1 pF ~10 nF	Figure 14
C_2	70 pF	10 pF~100 nF	Figure 15
L_1	10 µH	100 nH~ 20 µH	Figure 16
g_m	0.5	0.1 ~ 1	Figure 17
r_o	150 Ω	1 Ω ~ 300 Ω	Figure 18

The pole locations with the nominal value in the original cascode structure are plotted in Figure 12 and the complex poles are on the right-half plane (RHP), resulting in an unstable system.

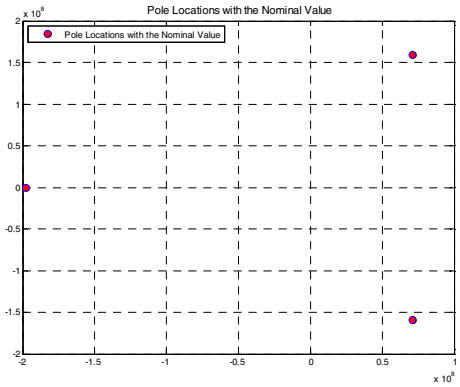


Figure 12 Pole location for the original cascode structure

Also, we can use Bode plot shown in Figure 13 to analyze the system stability. Since the system has no open loop left-half plane (LHP) poles but while the loop gain is higher than 0dB, the phase is reaching 180 *deg* phase line, the system is unstable.

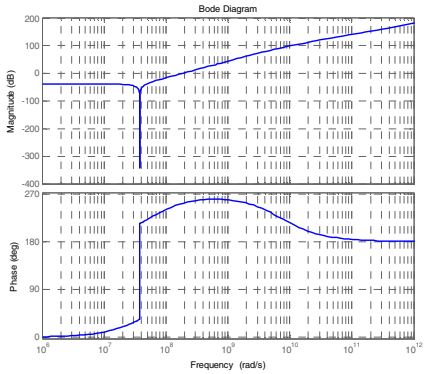


Figure 13 Bode Plot of the original cascode structure

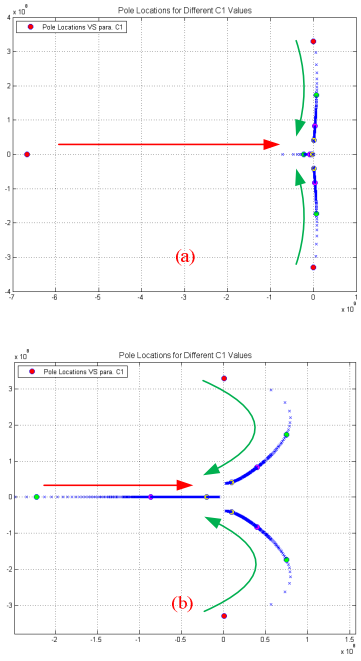


Figure 14 (a) Pole location for C_1 values for solution A and C; (b) zoomed

As shown in Figure 14, with the increasing C_1 values, the real pole is moving along the real axis to the right and the complex poles are walking into the RHP as unstable poles. Therefore, increasing the output capacitance of HVFET Q_1 does not help to resolve the instability issue.

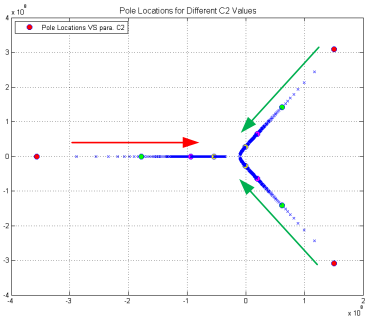


Figure 15 Pole location for C_2 values for solution A and C

As shown in Figure 15, with the increasing C_2 values, the real pole is moving along the real axis to the right. Based on the plot, when C_2>~9 nF, the complex poles are walking into the left-half plane (LHP) as stable poles. This explains the effectiveness of the solution A and C by increasing the equivalent output capacitance of the LVFET.

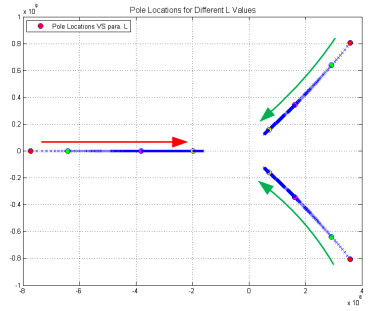


Figure 16 Pole location for L1 values for solution A and C

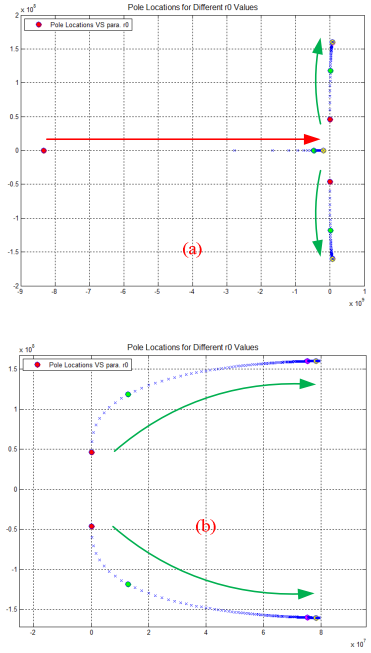


Figure 17 (a) Pole location for r_o values for solution A and C; (b) zoomed

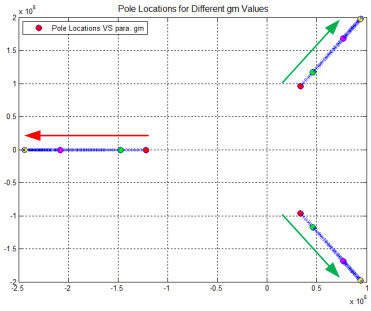


Figure 18 Pole location for g_m values for solution A and C

In real application, L_1 is the leakage inductance of the transformer (usually, L_1 should be minimized to improve

converter performance). r_o and g_m are determined once the power devices are selected. As shown in Figure 16, Figure 17 and Figure 18, with the increasing L_1, r_o and g_m values, the real pole is moving along the real axis to the right. And the complex poles are always in the RHP with the values in the range and the system is unstable.

Table 2 Design parameters and variation range for the stabilization solution B

Designator	Nominal Value	Variation Range	Figure #
C_1	120 pF	1 pF ~10 nF	Figure 20
C_2	70 pF	10 pF~100 nF	Figure 21
L_1	10 µH	100 nH~ 20 µH	Figure 22
g_m	0.5	0.1 ~ 1	Figure 23
r_o	150 Ω	1 Ω ~ 300 Ω	Figure 24
R_{snb}	100Ω	1 Ω ~ 300 Ω	Figure 25
C_{snb}	100 pF	10 pF ~ 200 pF	Figure 26

Using MATLAB, the roots of the characteristic equation or the closed-loop system poles in equation (**13**) can be plotted with different design parameters and variables for stabilization solution B. There are four poles in the system. The design parameters used in the model are shown in Table 2. In each of the cases, only one design parameter is varying and the rest of the design values are fixed using the nominal values.

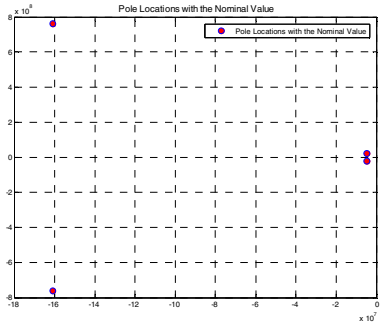
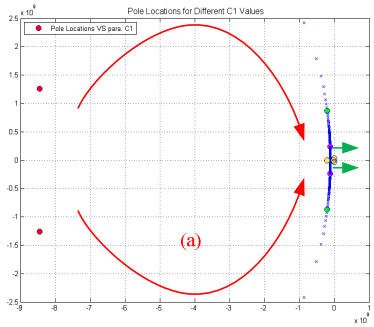


Figure 19 Pole location for the solution B with nominal design values

The pole locations with the nominal value of the solution B are plotted in Figure 19 and all the complex poles are on the LHP, resulting in a stable system.



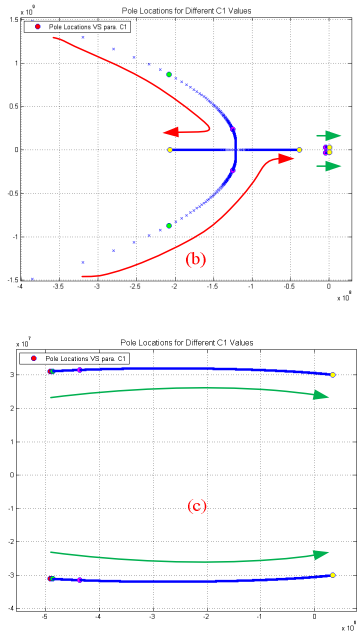


Figure 20 (a) Pole location for C_1 values for solution B; (b) and (c) zoomed

As shown in Figure 20, with the increasing C_1 value, one pair of the complex poles will become real poles. However, the other pair of the complex poles will walk into RHP and the system will be unstable again when C_1 (the output capacitance of Q_1) is larger than ~ 8.5nF.

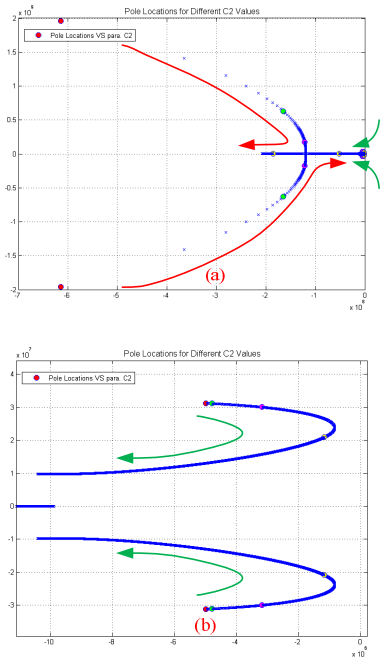


Figure 21 (a) Pole location for C2 values for solution B; (b) zoomed

As shown in Figure 21, with the increasing C_2 value, one pair of the LHP complex poles will become LHP real poles. And the other pair of the LHP complex poles will stay in the LHP and the system remains stable. When the C_2 >~6 nF, the

second pair of complex poles shown in Figure 21 (b) are moving towards left again and the system is more stable.

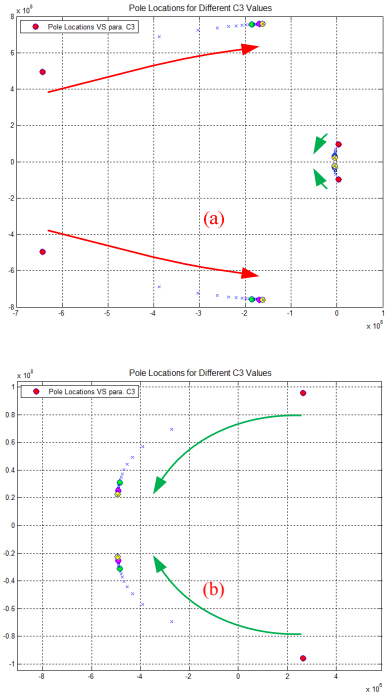


Figure 22 (a) Pole location for C_3 (C_{snb}) values for solution B; (b) zoomed

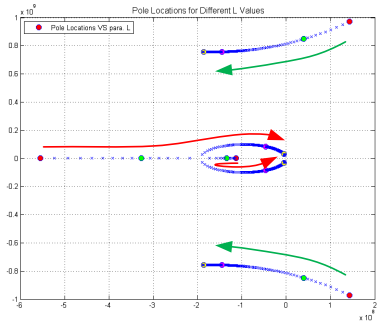


Figure 23 Pole location for L_1 values for solution B

As shown in Figure 22, with the increasing C_3 (or C_{snb}) value, one pair of the complex poles will move towards right side but remain in LHP. And the other pair of the complex poles will walk into the LHP and the system becomes stable. When the C_3 >~40 pF, the second pair of complex poles shown in Figure 22 (b) are moving towards left and the system is more stable. But the RC snubber circuit power loss needs to be considered to select the optimal value.

For the leakage inductance L_1 design parameter, the pole locations are plotted in Figure 23. With increasing L_1, two real poles will meet and separate into a pair of complex poles moving to the right side. And the RHP complex poles are moving into LHP. However, the higher leakage L_1 is undesirable, due to higher power loss and worse EMI results.

As shown in Figure 24, the increasing resistance for the snubber R_{sub} will move two complex poles to the right and the other two to the left. Again, the parameter R_{sub} will also impact on the power loss.

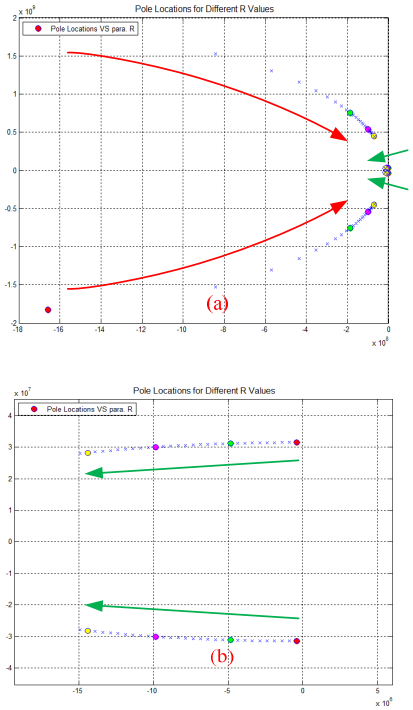


Figure 24 (a) Pole location for R (R_{snb}) values for solution B; (b) zoomed

As shown in Figure 25 and Figure 26, with the increasing r_o and g_m values, the complex poles are always in the LHP with the values in the design range and the system is stable.

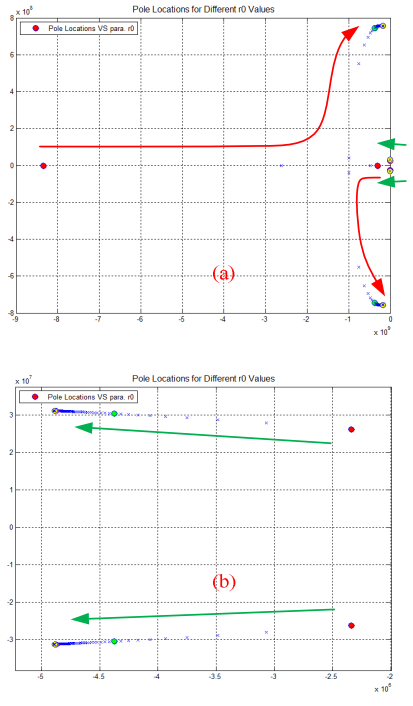


Figure 25 (a) Pole location for r_o values for solution B; (b) zoomed

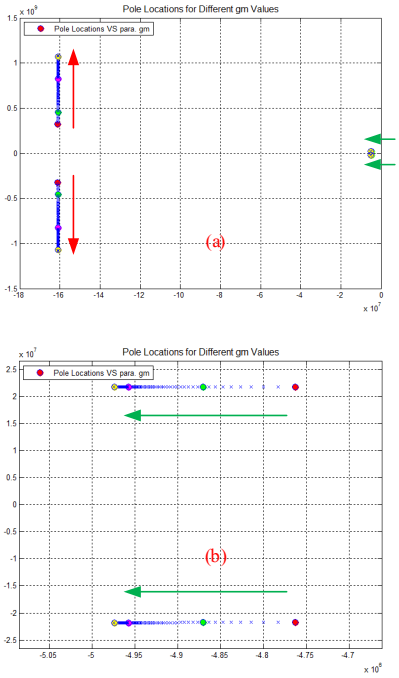


Figure 26 (a) Pole location for g_m values for solution B; (b) zoomed

V. EXPERIMENTAL RESULTS AND VERIFICATIONS

The modeled unstable behavior is observed in the experiments in Figure 27, especially, during the startup of the power stage, when the RCD clamping circuit is not well established into steady state yet. This unstable switching node ringing often causes the control scheme to be malfunctioning and start up flash of LED light output.

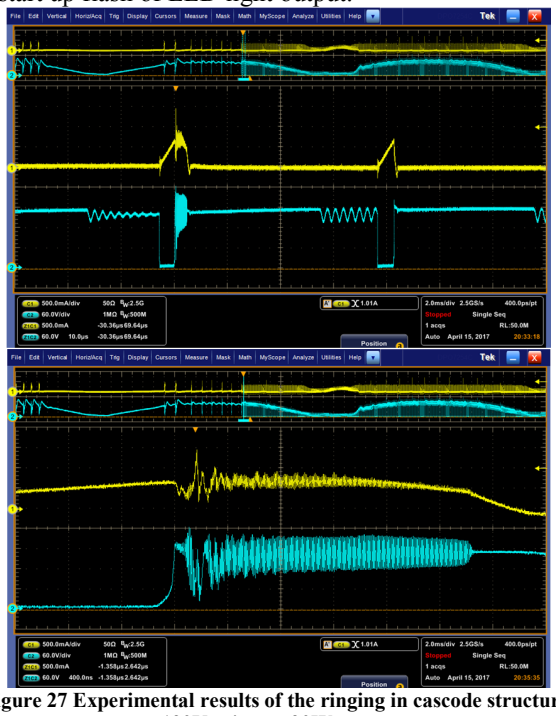


Figure 27 Experimental results of the ringing in cascode structure, 120Vac input, 20W output

The experimental result is shown in Figure 28 with the oscillation suppression solution A (C_{gs1}=10 nF) and B (C_{snb}=100 pF, R_{snb}=100 Ω) implemented. And the switching waveform is oscillation free.

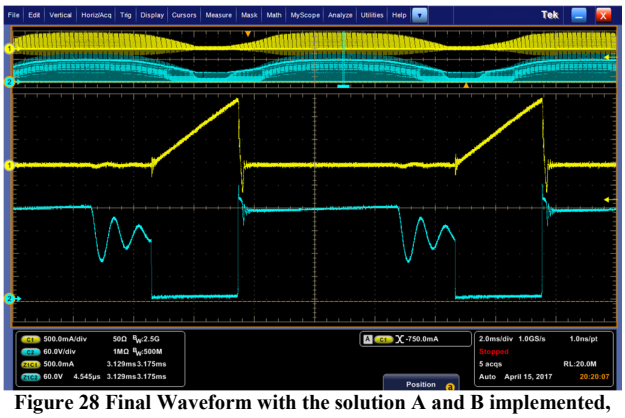


Figure 28 Final Waveform with the solution A and B implemented, 120Vac input, 20W output

VI. CONCLUSIONS

For phase-cut dimmable LED lighting application, to achieve fast start up in the deep dimming condition, cascode switching Flyback converter is a cost-effective solution. Furthermore, to resolve the unstable voltage oscillation, a new small signal model is built to explain the root cause of the issue. Solutions are inspired and proposed to stabilize the cascode configuration. Experimental results of a 20W LED driver are show to verify the model and the solutions.

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