A 6 μ W per Channel Analog Biomimetic Cochlear Implant Processor Filterbank Architecture With Across Channels AGC

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Abstract—A new analog cochlear implant processor filterbank architecture of increased biofidelity, enhanced across-channel contrast and very low power consumption has been designed and prototyped. Each channel implements a biomimetic, asymmetric bandpass-like One-Zero-Gammatone-Filter (OZGF) transfer function, using class-AB log-domain techniques. Each channel's quality factor and suppression are controlled by means of a new low power Automatic Gain Control (AGC) scheme which is coupled across the neighboring channels and emulates lateral inhibition (LI) phenomena in the auditory system. Detailed measurements from a five-channel silicon IC prototype fabricated in a 0.35 μm AMS technology confirm the operation of the coupled AGC scheme and its ability to enhance contrast among channel outputs. The prototype is characterized by an input dynamic range of 92 dB while consuming only 28 μW of power in total ($\sim 6~\mu\mathrm{W}$ per channel) under a 1.8 V power supply. The architecture is well-suited for fully-implantable cochlear implants.

Index Terms—Analog integrated circuits, automatic gain control, cochlear implant, lateral inhibition, low power, spectral enhancement.

I. INTRODUCTION

VER the past 30 years, cochlear implants (CIs) have developed from a device that was thought impossible for speech recognition and useful only for sound perception to an established clinical device for restoring partial hearing to deaf people. In the near future CIs will become fully implantable: all the external components of a CI system (e.g., the microphone and its speech processor) will be implanted except for a remote controller required to be external for the programming of the implanted part. As a result, CI users will be indistinguishable in appearance from normal hearing people, which can boost their self-confidence and improve third-party attitudes to them; such improvements have already been witnessed with state-of-the-art hearing aids which are placed inside the ear canal and are thus invisible or nearly invisible. Other benefits include: 1) fewer

Manuscript received October 21, 2013; revised February 14, 2014; accepted April 24, 2014. Date of publication July 23, 2014; date of current version January 23, 2015. This paper was recommended by Associate Editor S.-C. Liu.

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Digital Object Identifier 10.1109/TBCAS.2014.2325907

limitations to CI users' daily activities, 2) restoring access to the directional amplification function of the pinna by means of the microphone placed inside the ear canal, and 3) eliminating the constraints in the data bandwidth of the RF link transmitting the processed microphone input to the implanted electrodes.

The filterbank architecture presented in this work, termed "OZGF-with-LI", is intended for use in such CI systems. Each channel implements the One-Zero-Gammatone-Filter (OZGF) [1] while the novel automatic gain control (AGC) scheme, coupled across channels, emulates lateral inhibition (LI) phenomena in the auditory system. The OZGF was adopted as it can provide a good model of auditory filtering with only three parameters [1], [2] while the LI is regarded as an important biological spectral-enhancement mechanism which may partly account for the high robustness of the normal auditory system to noise [3]–[6]. The architecture performs multi-channel syllabic compression while preserving well across-channel contrast and hence the original spectral features of the system input. This is an advantage over the compression schemes used in current CIs, which tend to degrade spectral contrast through an asymmetric amplification over channel-specific frequency regions (i.e., the valleys in the spectrum and the corresponding weak-amplitude channels are strongly amplified in relative terms so that they are concurrently audible with weakly amplified spectral peaks and the corresponding "strong" channels; this side effect reduces the differences between channel outputs) [7]-[9].

This paper details a novel ultra-low-power analog VLSI implementation of this filterbank, explicitly designed to meet stringent power requirements compatible with fully implantable CI processors. Our filterbank does not intend to replicate the "exact" biological operations of the auditory system, which can be a complex and power hungry task [10]; instead, it aims to achieve a good trade-off between bio-fidelity and power consumption. Our implementation opts for an analogue solution rather than its digital counterpart because the former is known to provide considerable saving in both power consumption and silicon area compared to the latter when the precision required at the output is low [11]: typically, a CI processor's channel bandwidth is a few kHz at most and a patient's dynamic range (DR) is only 3–20 dB.

In the proposed implementation, the input DR together with the power consumption of each channel were optimized with micropower companding techniques [12]–[20] including log-domain filters biased dynamically via the AGC (syllabic companding). For each channel the biasing of the log-domain filter stages varies adaptively according to a coupled and weighted

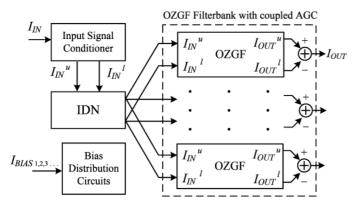


Fig. 1. Overall architecture of the analog OZGF-with-LI system.

measure of its output signal combined with the neighboring channel output signals. In this way, basic dynamics of the LI mechanism are modeled in the form of soft local processing linking different channel-specific frequency regions.

This paper is organized as follows. Section II provides an overview of the proposed system. Section III and Section IV detail its two major building blocks: the OZGF filterbank and the coupled AGC, respectively. Section V presents in detail results measured from a silicon IC prototype fabricated in a 0.35 im AMS CMOS process. Section VI provides a summary of the present findings and concludes.

II. SYSTEM OVERVIEW

Fig. 1 shows the block diagram of the proposed system. Each channel employs a pseudo-differential class-AB log-domain architecture. A geometric mean splitter (GMS) [17] is employed as a global input signal conditioner which serves to split a bi-directional input signal I_{IN} into a pair of complementary, unidirectional and positive ones $(I_{IN}{}^u$ and $I_{IN}{}^l)$ such that $I_{IN} = I_{IN}{}^u - I_{IN}{}^l$. An input-distribution network (IDN) formed by both PMOS and NMOS cascode current mirrors distributes $I_{IN}{}^{u,l}$ to different channels. Each of $I_{IN}{}^u$ and I_{IN}^{l} is filtered by a log-domain class-A filter. A subtraction is finally performed on the outputs to create a linearly filtered version of the input I_{IN} , i.e., $I_{OUT} = I_{OUT}^u - I_{OUT}^l$ where I_{OUT}^{u} and I_{OUT}^{l} are the two output signals generated from the "upper" and the "lower" class-A branches (denoted by the superscripts u and l) respectively. Similar to the IDN, biasing currents (I_{BIAS}) are supplied throughout the system by means of distribution networks.

Fig. 2 details the implementation of each channel. A cascade of four $2^{\rm nd}$ -order responses are controlled by a coupled feedback AGC scheme regulating the quality factor Q of each stage, not merely according to its corresponding channel output but also in accordance with neighboring channel outputs. The AGC input signal is first processed by an envelope detector. Subsequently the extracted envelope signal is weighted, coupled with other four envelope signals from the neighboring channel outputs, and then processed to generate the Q-decision signal.

III. OZGF FILTERBANK

In contrast to [21] where the realisability of the OZGF transfer function was verified, here the order of the cascaded

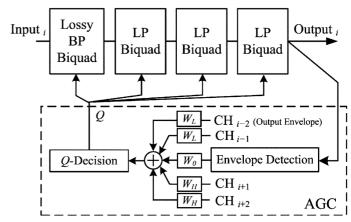


Fig. 2. Block diagram of a 4th-order OZGF channel with the coupled AGC block to regulate its stage quality factor Q (BP: bandpass; LP: lowpass; the channel index ranges from i-2 to i+2).

filter stages is rearranged in such a way that the cascade begins with a lossy bandpass (BP) (two poles and one zero) biquadratic stage followed by lowpass (LP) stages. Hence it is feasible to implement a programmable channel filter order N by using an output multiplexer to select one of the LP stage outputs from the filter cascade while the overall channel response corresponds to an N-th order OZGF transfer function.

Each channel is synthesized by means of log-domain circuits employing MOS transistors that operate in their weak-inversion region and arranged in a class-AB topology. The log-domain filtering technique [19]–[23] has been shown to be able to provide wide DR solutions even under low power supply voltages while the DR can be further extended by adopting a class-AB design approach (realized via a pseudo-differential architecture in this work as noted earlier), which is known to be able to offer a good trade-off between DR, linearity, noise and power consumption [17], [18].

Transistor-level details on the OZGF synthesis can be found in [21]. The lossy BP and LP biquad transfer functions are codified by

$$\frac{I_{OUT}^{LP}}{I_{IN}} = \frac{I_{OUT2}^{u} - I_{OUT2}^{l}}{I_{IN}^{u} - I_{IN}^{l}} \\
= \frac{\left(\frac{I_{0}}{nCV_{T}}\right)^{2}}{s^{2} + \frac{\left(\frac{I_{0}}{nCV_{T}}\right)^{2}}{\left(\frac{I_{0}}{I_{Q}}\right)} s + \left(\frac{I_{0}}{nCV_{T}}\right)^{2}} \\
\frac{I_{OUT}^{2P1Z}}{I_{IN}} = \frac{I_{OUT1}^{u} - I_{OUT1}^{l}}{I_{IN}^{u} - I_{IN}^{l}} \\
= \frac{\left(\frac{I_{0}}{nCV_{T}}\right) \left[s + \frac{I_{Z}}{nCV_{T}}\right]}{s^{2} + \mu \frac{\left(\frac{I_{0}}{nCV_{T}}\right)^{2}}{\left(\frac{I_{0}}{I_{Q}}\right)} s + \eta \left(\frac{I_{0}}{nCV_{T}}\right)^{2}} \tag{2}$$

where I_0 and I_Z are the two DC biasing current values which determine the pole and the zero frequencies via $\omega_0 = I_0/nCV_T$ and $\omega_Z = I_Z/nCV_T$, respectively. The quality factor is determined via $Q = I_0/I_Q$. The quantities n, C and V_T are the

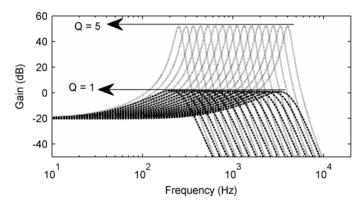


Fig. 3. Simulated frequency responses of 16 OZGF channels with Q=5 (solid line) and Q=1 (dotted line), whose centre (peak) frequencies (CF) are equally spaced along a logarithmic axis that ranges from 250 Hz to 4000 Hz when Q=5 and 205 Hz to 3280 Hz when Q=1, as illustrated in Fig. 4.

subthreshold slope parameter (typically between 1 and 2), the capacitance and the thermal voltage (25 mV @ T = 300 K), respectively. In (2), $\mu = 1 + I_Z/I_Q$ and $\eta = 1 + (I_Z/I_0) \cdot (I_Q/I_0)$; the two coefficients result in a deviation of (2) from an ideal lossy BP biquad's response. Nevertheless, this deviation occurs only at one filter stage and will not affect the overall response significantly when the filter order is fairly high (e.g., N=4)—a typical case for yielding desirable sharp high frequency roll-off [21].

This work realized a complete OZGF filterbank by arranging class-AB $4^{\rm th}$ -order OZGF channels in parallel and adding a bias-distribution network to specify the parameters I_0 and I_Z (and hence the pole and zero frequencies) individually for each channel while within each channel I_Q is controlled by the AGC. The OZGF channels are logarithmically scaled in the frequency domain by scaling the biasing currents correspondingly in the following way: the desired centre frequency (CF) range of the filterbank is divided into a number of small sub-ranges so that within each sub-range logarithmic channel CF spacing and the corresponding biasing currents can be approximated by a linear spacing without sacrificing accuracy significantly. In this way, the bias distribution can be implemented by linearly scaling the width of MOS transistors in groups of current mirrors.

For a CF range of 250 to 4000 Hz (4 octaves) in the case of a 16-channel filterbank, the above biasing scheme can provide <1% deviation from a logarithmic spacing. For example, the logarithmically-spaced CFs of the $7^{\rm th}$ to $11^{\rm th}$ channels, which equal 758, 912, 1097, 1320 and 1587 Hz (a subrange of ~ 1 octave), can be approximated as 760, 913, 1095, 1314 and 1577 Hz (corresponding to a scaling factor of 1.2); the resulting relative deviations are only 0.28%, 0.14%, 0.17%, 0.42% and 0.65% respectively. The five channels using this biasing scheme have been fabricated on an IC silicon prototype, whose details are provided later in Section V.

Fig. 3 shows the simulated frequency responses of a complete 16-channel OZGF filterbank ($C=20~\mathrm{pF}$) whose channel are spaced logarithmically. Fig. 4 details its CF distribution, which exhibits a linear dependence on I_0 ranging from 1.25 to 20 nA. As I_0 varies, two different Q values were realized by setting $I_Q=0.2I_0$ for Q=5 and $I_Q=I_0$ for Q=1 while I_Z was set to $0.1I_0$, yielding a "tail" of the response curve at frequencies

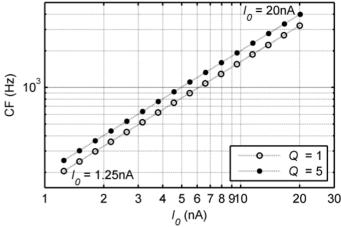


Fig. 4. Simulated CF distribution (corresponding to the response peaks in Fig. 3) across the 16 OZGF channels and the corresponding biasing current I_0 varying from 1.25 nA to 20 nA uniformly on the logarithmic x-axis.

well below the CFs, which has a fixed DC gain of -20 dB. Fig. 4 also shows that the CFs of Q=1 deviate from the ones of Q=5 by approximately 20%. As the Q and hence peak gain decreases, the CF decreases as well, which corresponds to a biorealistic shift of the OZGF response peak towards lower frequencies [1].

It should be stressed that realizing different channel CFs by tuning of biasing currents can save silicon area in comparison to scaling the capacitance of the cascade biquads (especially when realizing low channel CFs). The tuning can also facilitate the post-implantation fitting of CIs [24] when these biasing currents are digitally programmable for each channel.

IV. COUPLED AGC

We have adopted a *Q*-control law implemented via the AGC which is quasi-logarithmically compressive as follows:

$$I_Q = I_{tail} \tanh \left[\beta \ln \left(\frac{I_{CP} + I_{th}}{I_{0_control}} \right) \right].$$
 (3)

The quantities I_{tail} , $I_{0_control}$ and I_{th} represent three biasing currents while β is a positive factor that depends on practical implementation and will be defined later on. The signal I_{CP} of the i-th channel is an envelope signal derived from this channel output (denoted as I_{EDi}) and the neighboring ones (denoted as $I_{EDi\pm 1}$ and $I_{EDi\pm 2}$) in the following manner:

$$I_{CPi} = f(I_{EDi}, I_{EDi+1}, I_{EDi+2}, I_{EDi-1}, I_{EDi-2})$$
 (4)

where $f(\cdot)$ denotes a linear or nonlinear coupling function and will be defined later. In terms of (3), and with $I_{th}=K\,I_{0_control}$ (K is a proportionality constant), the K value and I_{tail} determines the minimum I_Q value and hence the maximum Q corresponding to $I_{CP}=0$. I_{tail} alone determines the maximum I_Q and hence the minimum Q since the hyperbolic tangent function saturates to 1 for a large I_{CP} while $I_{0_control}$ controls the AGC sensitivity.

The block-level realization of (3) and (4) by means of the AGC circuits is shown in Fig. 5. The i-th channel output I_{OUTi} is first processed by an envelope detector consisting of a quasi-

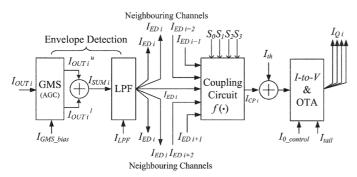


Fig. 5. Block diagram of the coupled AGC circuits within each channel (the subscripts i, i+1, i+2, i-1 and i-2 denote channel indexes).

full-wave rectifier operating based on the output combination of a GMS, and an LPF that follows to smooth the output I_{SUMi} . The biasing currents for the two building blocks are I_{GMS_bias} and I_{LPF} respectively, and I_{LPF} controls the time constant of the LPF. The extracted envelope signal $I_{ED\ i}$ and those from the neighboring channels ($I_{EDi\pm 1}$ and $I_{EDi\pm 2}$) are then combined together yielding I_{CPi} from the coupling circuit which implements the function $f(\cdot)$ in (4). Simultaneously, the mirrored copies of $I_{ED\ i}$ are delivered to the neighboring channel AGCs for the same processing. The coupling circuit offers four different sets (S_0 – S_3) of weighting factors to choose from for the coupling signals in (4); a DC bias I_{th} is added to I_{CPi} to realize the thresholding involved in (3).

To implement the logarithmic and hyperbolic functions in (3), I_{CPi} is converted to a voltage signal via the exponential I-V characteristic of weakly-inversed MOS transistors; this voltage signal is then converted back to current through an operational transconductance amplifier (OTA) consisting of transistors that operate in weak inversion, yielding a hyperbolic tangent transfer characteristic. The I-to-V circuit and the OTA are incorporated in a compact architecture where the two biasing currents $I_{0_control}$ and I_{tail} control the sensitivity and upper-limit of the AGC transfer characteristic respectively.

Subsequently, the OTA output signal I_{Qi} is scaled with I_{0i} (using current mirrors) for different channels to ensure that all the channel AGCs set the same Q range $[Q_{\min}Q_{\max}]$ governed by (5) and (6) (derived from (3)) where $K = I_{th}/I_{0_control}$.

$$Q_{\text{max}} = \frac{I_0}{I_{Q(\text{min})}} = \frac{I_0}{\{I_{tail} \tanh[\beta \ln(K)]\}}$$
 (5)

$$Q_{\min} = \frac{I_0}{I_{Q(\max)}} \approx \frac{I_0}{I_{tail}} \tag{6}$$

All the scaling functions presented in this work have been realized by one or more pairs of MOS transistors with different device sizes within each pair (i.e., current mirrors with different scaling factors). The scaled output I_{Qi} is mirrored to generate four copies for the four biquad stages of the $4^{\rm th}$ -order OZGF.

The AGC scheme essentially implements a dynamic-biasing of each channel by changing I_Q ; this is a technique known as syllabic companding, which can potentially optimize power dissipation and output SNR when used in analogue signal processors [13], [14]. The following subsections provide details on each building block of the AGC and show measured results of the complete AGC. Table I lists the device sizing, the filter ca-

TABLE I
DEVICE SIZING AND PARAMETER SETTING

Topology	IDN	GMS (global)	OZGF	GMS (AGC)	ОТА	Coupling Circuits*
$W/L_{(PMOS)}$	300 μm/1.5 μm					
$W/L_{(NMOS)}$	60 μm/8 μm 15μm/4μn					15µm/4µm
V_{DD}	1.8 V					
C_{OZGF}	20 pF					
C_{LPF}	10 pF					
I_{0}	5.8 nA					
I_Z	580 pA (i.e., $I_Z = 0.1I_0$)					
I_{tail}	7 nA					
I _{GMS bias}	20 nA (global); 30 nA (AGC)					
I_{LPF}	18 nA					
I_{th}^{\dagger}	$-33.5 \text{ nA } (S_0); -36 \text{ nA } (S_1, S_2, S_3)$					
I _{0 control}	21 nA (S ₀); 19 nA (S ₁ , S ₂ , S ₃)					

^{*}The dimensions refer to the minimum device size in Fig. 9.

[†] The negative sign refers to sinking of I_{th} from I_{CP} .

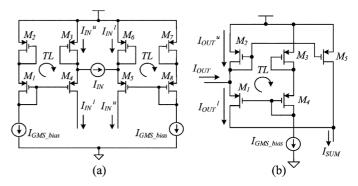


Fig. 6. (a) Balanced GMS architecture used as the global input conditioner (I_{IN} denotes a bidirectional input current signal). (b) Single-ended GMS architecture (compatible with the channel output) used as a full-wave rectifier in the AGC. Both architectures are formed by weakly inversed PMOS transistors.

pacitance and all the biasing current values. In the AGC circuits, the body terminal of each PMOS transistor is connected to its respective source terminal (not shown in the schematics).

A. Quasi-Full-Wave Rectification Using Geometric Mean Splitter (GMS)

A geometric mean splitter (GMS) is employed as the global input conditioner for class-AB operation. Fig. 6(a) shows its standard translinear (TL) implementation with I_{IN} being a floating current source which, in practice, was realized by means of two grounded AC current sources at a 180° phase difference with each other. The implementation involves two TL loops (formed by M_1 – M_4 and M_5 – M_8 which are assumed matched) governed by

$$I_{IN} = I_{IN}^{u} - I_{IN}^{l}$$

$$I_{GMS_bias}^{2} = I_{IN}^{u} \cdot I_{IN}^{l}.$$
(7)

Based on (7), the two generated complementary signals can be expressed as follows:

$$I_{IN}^{u,l} = \frac{1}{2} (\sqrt{4I_{GMS_bias}^2 + I_{IN}^2} \pm I_{IN}).$$
 (8)

In (8), both $I_{IN}^{\ u}$ and $I_{IN}^{\ l}$ are strictly positive because of the presence of the biasing term $4I_{GMS_bias}^{\ 2}$, and are comple-

mentary to each other. Furthermore, they tend to the DC bias I_{GMS_bias} for small input swings, whereas for input swings much larger than I_{GMS_bias} , their peak values tend to I_{IN} . Therefore, the DR can be very wide in principle. In practice, an upper limit for the DR exists since for each TL loop, the PMOS transistors must be ensured to always operate in weak-inversion (WI) regime, which in turn dictates a maximum allowable signal swing at the input for a given device size. Nevertheless, we can extend the upper limit of the WI region with careful device sizing.

According to (8), a summation of $I_{IN}^{\ u}$ and $I_{IN}^{\ l}$ gives

$$I_{SUM} = \sqrt{4I_{GMS_bias}^2 + I_{IN}^2}.$$
 (9)

 I_{SUM} is thus a positive signal with a lower limit at $2I_{GMS_bias}$. It becomes a full-wave rectified version of I_{IN} when I_{IN} is much larger than I_{GMS_bias} . This suggests a "hidden" advantage of the GMS: if its two output signals are combined in common mode, the resulting topology can act as a quasi- full-wave rectifier and a compressor (imposing a positive lower-limit on the combined signal) simultaneously. We have exploited this advantage in the AGC implementation through a single-ended circuit topology shown in Fig. 6(b), which contains only one TL loop formed by M_1 – M_4 while governed by equations similar to (7)–(9) (just replace $I_{IN}{}^{u,l}$ with $I_{OUT}{}^{u,l}$). Note that a current mirror is added to sense $I_{OUT}{}^{u}$ to facilitate the summation operation $I_{OUT}{}^{u} + I_{OUT}{}^{l}$.

It should be clarified that there are topologies that can exactly implement the absolute-value function, e.g., precision full-wave rectifiers. Nevertheless, such rectification was not considered so critical for the overall functionality of our AGC. The present GMS topology can be regarded as a good compromise between performance and circuit complexity.

B. The LPF Smoothing

The GMS used in the AGC is followed by a $1^{\rm st}$ -order LPF to smooth the rectified signal I_{SUM} , extracting its envelope. An important consideration in the design of this LPF is to determine its time-constant. Our computational modeling via MATLAB reveals that the proposed AGC requires long time constants to ensure minimized spectral distortions caused by multi-channel compression. In fact, previous studies have showed negative effects of fast-acting compression on speech intelligibility [8], [25]. Therefore, long time constants τ were employed and scaled with the channel pole frequency f_0 in such a way that the LPF's corner frequency $1/\tau$ equals to $f_0/40$, and thus high-frequency channels are characterized by shorter time constants.

There is a potential difficulty that may be encountered in an attempt to obtain very long time constants for low-frequency channels without consuming too much silicon area, since large capacitors tend to be required. Utilization of the Miller effect may help as it can provide increased effective capacitance, but the resulting power consumption may be also higher due to the heavy use of active components for high gain amplification. For a good compromise between area and power consumption, we chose a simple log-domain integrator solution proposed in [26]

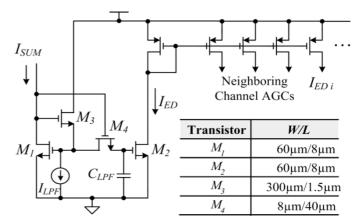


Fig. 7. The 1st-order log-domain LPF (adapted from [26]) used in the AGC for smoothing.

and shown in Fig. 7. The transistors M_1 and M_2 are matched, while M_3 and the current source I_{LPF} form a level-shifter shifting the gate voltage of M_4 relative to that of M_1 . Mirrored copies of the output $I_{ED\ i}$ are fed to the neighboring channel AGCs. All the transistors operate in saturation and weak inversion except that M_4 is allowed to operate in its triode regime. While the floating transistor M_4 acts as a nonlinear pseudo-resistor electronically tunable via the level-shifter, the M_4 - C_{LPF} circuit is analogous to an RC circuit of the same topology.

The time constant is determined as follows (assuming leakage currents are negligible; M_3 and M_4 are matched except for their aspect ratios) [26]

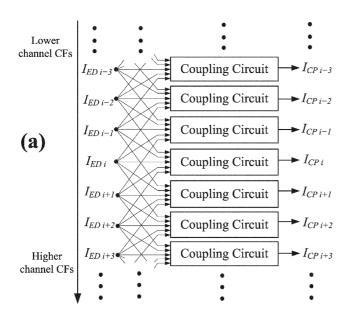
$$\tau = C_{LPF} \cdot \frac{2\pi V_T}{I_{LPF} \cdot \frac{\frac{W_4}{L_4}}{\frac{W_3}{L_2}}} \tag{10}$$

where V_T is the thermal voltage while W_3/L_3 and W_4/L_4 are the aspect ratios of M_3 and M_4 respectively.

The presence of the two aspect ratios in (10) suggests that besides adjusting the capacitance and/or the DC bias, long time constants are obtainable through relative sizing of the devices. For smoothing, this is an advantage over traditional log-domain integrators (e.g., that used in [21]), where time constants are not dependent on relative transistor sizing. For instance, assuming $W_3/L_3=300/1.5$ and $W_4/L_4=8/40$ (see the table in Fig. 7), then the ratio of W_4/L_4 to W_3/L_3 is 1/1000 and the resulting time constant τ becomes one thousand times that obtained from merely adjusting the DC bias and the capacitance in traditional log-domain integrators. Our desired time constant for the lowest-frequency channel ($f_0=250~{\rm Hz}$) is 160 ms while other higher-frequency channels requires shorter time constants.

C. AGC-Coupling Network and Circuits

Fig. 8(a) illustrates the proposed AGC-coupling network for distributing the envelope signal I_{ED} across channels $(i, i \pm 1 \text{ and } i \pm 2)$ as indicated by the arrows, and Fig. 8(b) shows its pared-down version used for a five-channel fabricated silicon IC prototype corresponding to the $7^{\rm th}$ to $11^{\rm th}$ channels of the 16-channel filterbank shown in Fig. 3 (details on this prototype are provided in Section V). In Fig. 8(b), the $9^{\rm th}$ channel (i=9)



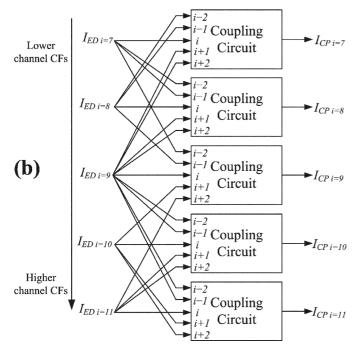


Fig. 8. (a) The proposed AGC coupling scheme for a filterbank composed of a number of channels, each being surrounded by four neighboring channels (two of lower and two of higher CFs). (b) The AGC coupling scheme adopted for the pared-down, five-channel fabricated silicon IC prototype corresponding to the 7th to 11th channels of the 16-channel filterbank shown in Fig. 3.

realizes the proposed AGC coupling scheme in an exact manner since, being the "middle" channel of the five (i=7 to 11), is surrounded by four channels; for balance of the distribution of the practical implementation, the $8^{\rm th}$ and $10^{\rm th}$ channels' AGCs receive inputs only from their immediate neighboring channels while the $7^{\rm th}$ and $11^{\rm th}$ channels' AGCs receive "one-sided" inputs from their two most proximal channels.

The coupling circuit, which processes the distributed I_{ED} to generate I_{CP} , is detailed in Fig. 9. The different device aspect ratios indicated there represent relative sizing of these devices,

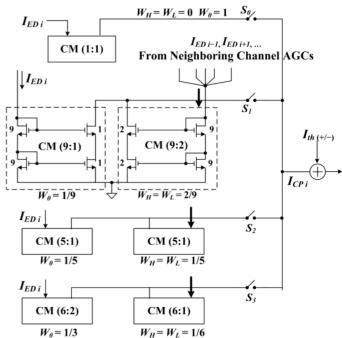


Fig. 9. The AGC coupling circuit with four different sets of weighting (S_0-S_3) implemented using relative-sized current mirror (CM) blocks. The S_0 scheme corresponds to the AGC coupling-off case.

which implements the weighting factors W_H , W_L and W_0 in the coupling function as follows (bear in mind (4)):

$$I_{CPi} = W_H(I_{ED\ i+1} + I_{ED\ i+2}) + W_L(I_{ED\ i-1} + I_{ED\ i-2}) + W_0I_{ED\ i} \quad (11)$$

where the subscripts H and L denote the weighting for higher and lower frequency channels respectively. For simplicity, we set $W_H = W_L$ so that coupling signals from the neighboring channels' AGCs can be combined together for weighting, as illustrated by the bold arrows in Fig. 9. The weighted signals are multiplexed into I_{CP} via four switches S_0 – S_3 , corresponding to four different sets of weighting factors (for convenience, we use S_0 – S_3 hereinafter to represent the four sets). S_0 corresponds to the AGC uncoupled case ($W_H = W_L = 0$, $W_0 = 1$ and thus $I_{CP} = I_{ED}$), which was employed as the reference case for comparison. From S_1 to S_3 , less and less "weights" are allocated to neighboring channel AGC signals by reducing the ratio of $W_{H,L}$ to W_0 . To ensure that the four different coupling sets provide the same DC bias level for I_{CP} , the weighting factors were chosen so that their sum is always equal to one for S_1 – S_3 (i.e., $2W_H + 2W_L + W_0 = 1$). Another DC biasing current I_{th} is added to I_{CP} to implement the term $I_{CP} + I_{th}$ in (4). I_{th} can be negative via current subtraction so that there is more flexibility to adjust the already existing bias level (determined by I_{GMS_bias}) of I_{CP} .

D. Integrated I-to-V and OTA

The logarithmic and hyperbolic tangent-functions involved in (3) were implemented together using the simple architecture shown in Fig. 10. The two diode-connected transistors M_1 and M_2 operate in weak inversion and are connected respectively

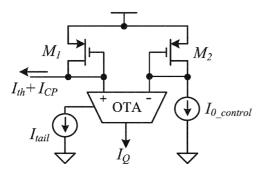


Fig. 10. The integrated I-to-V and OTA.

to the differential inputs V_+ and V_- of a standard OTA, which gives (assuming the two transistors are matched)

$$V_{+} - V_{-} = nV_{T} \ln \left(\frac{I_{CP} + I_{th}}{I_{0_control}} \right). \tag{12}$$

Therefore, M_1 and M_2 together provide a logarithmic *I-to-V* conversion to facilitate the OTA subthreshold operation, which yields I_Q as follows:

$$I_Q = I_{tail} \tanh\left(\frac{V_+ - V_-}{2nV_T}\right) \tag{13}$$

where I_{tail} is the biasing (tail) current. By substituting (12) into (13), the resulting I_Q has the same form as (3); the factor of 1/2 in (13) corresponds to the factor β in (3), i.e., $\beta = 0.5$, which can be lumped into the constant K' in (14) as the power of 0.5 for setting the upper limit of the Q-range in practice.

E. AGC Simulation and Measured Results

Table I lists the device sizing and parameter settings of each building block (except the LPF's sizing already contained in Fig. 7). The I_0 value corresponds to that used for the $9^{\rm th}$ channel (i.e., i=9 and $CF=1100~{\rm Hz}$) in the 16-channel simulation, and was used as the reference channel on the fabricated 5-channel chip. The other channels are fed by logarithmically scaled copies of this value. Such a manner of scaling across channels was also applied to I_Z for obtaining $I_Z=0.1I_0$ and to I_{LPF} for obtaining the desired time constant $\tau=40/f_0$. The two reference values used for the respective scaling of I_Z and I_{LPF} are listed in Table I and the corresponding distribution networks are merely copies of that used for I_0 . All the channel AGCs have the same parameter settings except for I_{LPF} scaled for different channels, and have their Q-range specified in the following way (bear in mind (5) and (6) where $\beta=0.5$):

$$Q_{\min} \approx \frac{I_0}{I_{tail}} = 0.83$$

$$Q_{\max} = \frac{I_0}{\{I_{tail} \tanh[0.5 \ln(K)]\}} = \frac{I_0}{\{I_{tail} \tanh[\ln(K')]\}} = 7$$
(14)

where $K'=K^{0.5}$ and $K=(2I_{GMS_bias(AGC)}+I_{th})/I_{0_control}$. Note that the two different combinations of I_{th} and $I_{0_control}$ values shown in Table I yield the same K

TABLE II
MEASURED PERFORMANCE OF THE OZGF-WITH-LI SYSTEM

Peak Gain	50 dB with < 1% THD		
Channal CEa	Q = 1	610, 740, 880, 1050, 1280 Hz	
Channel CFs	Q = 5	760, 920, 1100, 1320, 1590 Hz	
Input DR @CF	92 dB with <5% THD		
Noise Floor	Min.	9.6 pA @ CF = 250 Hz	
Noise Floor	Max.	35.3 pA @ CF = 4 kHz	
Total on-chip Capacitance	1650 pF		
Chip Area	$4.5 \text{ mm} \times 4.5 \text{ mm} (20.25 \text{ mm}^2)$		
Static Power Consumption	28 μW (overall system), 7 μW (AGC only)		

and hence the same $Q_{\rm max}$ for both the AGC uncoupled and coupled cases S_0 – S_3 . As a consequence, approximately the same input DR has been achieved for the two cases in our fabricated system.

Note that Q_{max} in (14) will be actually smaller than 7 as the AGC input (I_{OUT}) can never reach zero and it should be over the noise floor and hence detectable. Specifically, in our fabricated system, the lower-limit of the AGC input signal was set to 25 nA in accordance with the measured noise floor. With the parameter settings shown in Table I, the AGC scheme maps this value to a maximum biquad Q of 5 (corresponding to a $\sim 50~\mathrm{dB}$ peak gain) and hence a minimum allowable (detectable) input signal of 80 pA which is over the noise floor, 35.3 pA, measured in the worst case (see Table II). On the other hand, for a large I_{OUT} of 400 nA, the AGC sets a low Q value of 1 via $I_O = I_0 = 5.8 \text{ nA}$. A further increase in I_{OUT} (e.g., within the μA -range) eventually results in a saturated low Q value of $0.83 (I_{Q(\max)} \approx I_{tail} = 7 \text{ nA})$. To accommodate a large I_{OUT} , the device sizing of the AGC circuits allows for weak-inversion operation of MOS transistors at current signal levels up to several μ As so that their logarithmic conformity is ensured for the TL-based GMS and the log-domain LPF (thus its DR is $\sim 40 \, \mathrm{dB}$ relative to the lower limit, $2I_{GMS_bias(AGC)}$, set by (9)).

Fig. 11 shows typical simulated waveforms at the outputs of the AGC building blocks. The input I_{OUT} is a sinusoidal current signal of 400 nA. I_{SUM} is a quasi-full-wave rectified version of I_{OUT} (on a small DC bias). I_{ED} is the extracted envelope signal. The final output I_Q is a quasi-DC signal with $I_Q = I_0$ giving Q = 1.

Fig. 12 shows the measured parametric LPF response, whose corner frequency is electronically tunable via I_{LPF} . By setting $I_{LPF} = 4 \text{ nA}$, the time constant can be as long as 167 ms for the lowest-frequency channel ($f_0 = 250 \text{ Hz}$).

Fig. 13 shows the measured DC responses of the overall AGC (corresponding to its quasi-DC output). These curves represent the parametric I_{CP} -to- I_Q transfer characteristic [(codified by (3)] whose initial parameter settings are those listed in Table I. Bear in mind (3), the following can be observed:

- 1) I_{tail} determines the saturating level of the characteristic. Its linear scaling results in a linear scaling of the I_Q value for a given I_{CP} value, which is consistent with (3).
- 2) Compared to I_{tail} , varying either $I_{0_control}$ or I_{th} has a smaller effect on the large I_{CP} region (hundreds of nA to 1 μ A) of the transfer characteristic. Especially for different I_{th} values, the characteristic remains almost unchanged in that region because I_{th} becomes negligible for

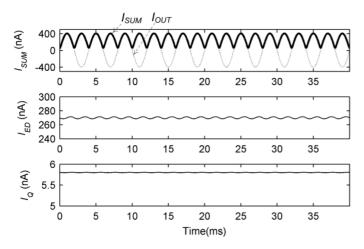


Fig. 11. Simulated waveforms generated at different stages of the AGC (via S_0) giving Q=1. The fine line on the top panel represents the AGC input (i.e., channel output, or I_{OUT}) while the bold line represents the GMS output I_{SUM} . I_{CP} is not shown in the figure since it is equal to I_{ED} in the S_0 case.

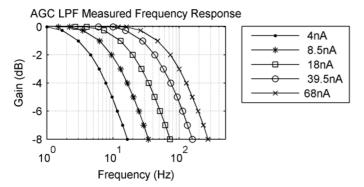


Fig. 12. Measured frequency responses of the LPF in the AGC with varying I_{LPF} . The corresponding -3 dB frequencies are 6.25 Hz, 13 Hz, 27 Hz, 57.5 Hz and 100 Hz, and are linearly related to the I_{LPF} values. These frequencies correspond to the AGC time constants ($\tau=40/f_0$) of the $1^{\rm st}$, $5^{\rm th}$, $9^{\rm th}$, $13^{\rm th}$ and $16^{\rm th}$ channels of the simulated filterbank respectively when Q=5.

very large I_{CP} values in (3). The transfer characteristic becomes highly dependent on the two parameters at smaller I_{CP} values.

- 3) Different combinations of $I_{0_control}$ and I_{th} values, if carefully manipulated to ensure the same K value in (14), yield a family of I_{CP} versus I_Q curves converging to a single point. In this way, the Q-range can be kept fixed while the AGC sensitivity is adjustable via $I_{0_control}$.
- 4) All the transfer curves are quasi-logarithmic as suggested by (3) and have non-zero and strictly positive lower-ends where the minimum I_{CP} equals to a DC offset generated at the GMS [i.e., $2I_{GMS_bias(AGC)}$].

The above observations demonstrate the AGC characteristic to be compressive and electronically tunable; its lower limit is determined by a ratio between the two DC biasing currents of the I-to-V [i.e., $(2I_{GMS_bias(AGC)} + I_{th})/I_{0_control}$] while the upper limit is determined by the OTA tail-current I_{tail} .

V. COCHLEAR FILTERBANK CHIP MEASUREMENTS

Fig. 14 shows a die photo of the 5-channel filterbank system fabricated in a standard 0.35 μ m AMS 2P/4M CMOS process.

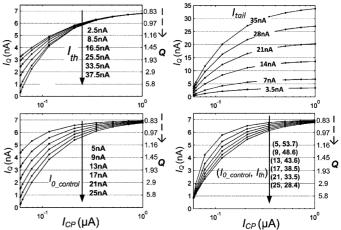


Fig. 13. Measured parametric I_{CP} -to- I_Q transfer characteristic for varying I_{th} , I_{tail} and $I_{0_control}$ values. The plot in the lower right corner shows that a fixed minimum I_Q is obtainable at $I_{CP}=0.06~\mu A$ when varying $I_{0_control}$ and I_{th} simultaneously (denoted as $(I_{0_control},I_{th})$ in nA). Q decreases as I_Q increases as indicated by a downward dashed arrow on the right-hand-side (RHS) y-axis where the ticks of Q values correspond to their I_Q counterparts on the left-hand-side (LHS) y-axis, when $I_0=5.8$ nA as listed in Table I.

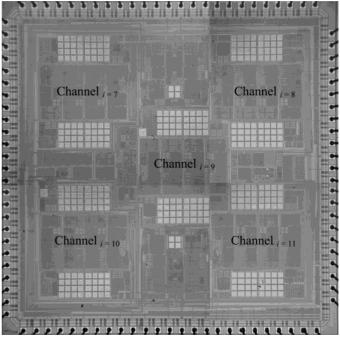


Fig. 14. A die photo of the 5-channel OZGF-with-LI system chip.

The five on-chip channels correspond to the $7^{\rm th}$ to $11^{\rm th}$ ones of the simulated 16-channel filterbank. Table II summarizes the measured performance of this $4.5~{\rm mm} \times 4.5~{\rm mm}$ chip.

A. Device Sizes and Layout

Table I codifies the optimized device sizes for each building block of the system. For those blocks with functionality strongly relying on the exponential V-I characteristic of the constituent MOS transistors, their sizes were carefully chosen to ensure the WI operation. For instance, a large aspect ratio of W/L=300/1.5 was employed to maintain the log-conformity of the

transistors in the OZGF biquads for a μA -range of their drain currents.

Besides higher DR, linearity was also optimized via device sizing. To preserve the external linearity in log-domain filtering, the device sizing should guarantee that each transistor within the biquads acts as a translinear element, whose transconductance is linearly related to the current it carries. We thus adopted a small transistor length L together with a large width W to maximize the linear range of the $\ln(I_{DS})$ versus V_{GS} transfer characteristic since its slope corresponds to the transconductance. Too small L causing the channel-length modulation effects were avoided. We found a good trade-off when L was about four times the feature size.

From the perspective of current matching, large device areas have been used to optimize the standard deviation of the drain current mismatch. Special efforts to optimize the matching were also made during the layout phase by means of inter-digitization and common-centroid techniques. Such approaches were considered important since the pseudo-differential architecture of the class-AB channels calls for excellent matching between the two class-A paths denoted by the superscripts u and l in Fig. 1; any path mismatch would lead to increased distortion of the channel output. Thus each "upper" transistor was interdigitised with each corresponding "lower" counterpart to form matched transistor pairs within each class-AB biquad. Moreover, each pair was arranged in a two-dimensional common-centroid array with symmetry axes both horizontally and vertically.

B. Measurement Setup

The floating current source I_{IN} in Fig. 6(a) was realized by means of two Keithley 6221 precision AC/DC current sources, which were programmed via their GPIB interfaces and were externally triggered to generate two AC current waveforms that had an exact 180° phase shift relative to each other. The two current waveforms were carefully calibrated by fine tuning their relative phases and amplitudes so as to minimize the mismatch between them since this affects the performance of the GMS input stage. The two current source outputs were connected to the source terminals of M_4 and M_5 respectively in Fig. 6(a), realizing the floating current source. The channel outputs were measured using standard Op-amp based I-to-V converters followed by a Standford Research $1 \, \mathrm{mHz}$ -to- $100 \, \mathrm{kHz}$ spectrum analyzer SR785 ($1 \, \mathrm{M}\Omega$ input resistance).

C. Frequency Response Results

The fabricated five channels were calibrated in such a way that their nominal CFs correspond to those of the $7^{\rm th}$ to $11^{\rm th}$ channels of the simulated 16-channel filterbank as listed in Table II. The measured frequency responses are obtained with an input sinusoid of fixed amplitude and varying frequency, and they refer to iso-intensity response curves. For convenience, the indices $i=7{-}11$ are used to denote the five channels hereafter.

Fig. 15(a) shows the Q tunability and hence the peak gain of the channel of i=9 for different input strengths. For clarity, the measured OZGF response traces locate with equal increments (12.5 dB) in the peak gain. Observe that these traces correspond to unequal dB increments in input levels. This nonlinearity arises from the quasi-logarithmic transfer characteristic

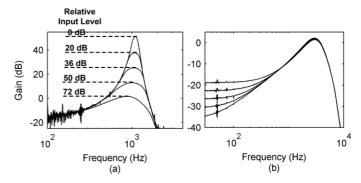


Fig. 15. OZGF channel measured frequency responses for the AGC coupling-off case (S_0) : (a) gain-tunability with the maximum peak gain set at ~ 50 dB (corresponding to Q=5) for i=9, and each trace corresponds to a different input signal strength in dB (annotated on the dashed lines) relative to the minimum input signal of 80 pA (corresponding to the maximum peak gain); (b) Low-frequency-tail tunability via varying I_Z as $0.1I_0$, $0.063I_0$, $0.04I_0$, $0.025I_0$ and $0.016I_0$ downwards respectively (note that the "glitch" at the low-frequency region of the measured response curves is 50 Hz pickup).

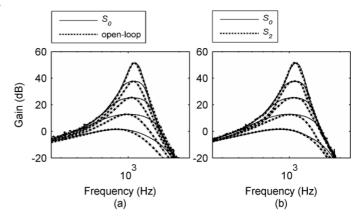


Fig. 16. A comparison of measured frequency responses with different AGC schemes for i=9: (a) open-loop versus closed-loop (S_0) ; (b) AGC coupling ON (S_2) versus OFF (S_0) . The corresponding input levels for S_0 are the same as those listed in Fig. 15 while those for S_2 are 0 dB, 28 dB, 45 dB, 60 dB and 85 dB (relative to the minimum input level, 80 pA) at the peak gains (with equal increments of 12.5 dB).

of the AGC. Details on the gain adaption with the input will be given as input-gain transfer curves later in Fig. 20.

Fig. 15(b) confirms the tunability of the low-frequency tail with the biasing current I_Z as this bias determines the location of the zero of the transfer function relative to the pole via I_0/I_Z [see (2)]. For clarity, the responses were measured for large signals and hence low Q values so that the SNR at the out-of-passband tail is not too low. Observe that the CF and filter gain are not affected much by the variation of the low-frequency tail despite the foregoing design deviation from an ideal lossy BP biquad transfer function [bear in mind the quantities in (2)].

Fig. 16 compares OZGF frequency responses (i=9) measured for different AGC schemes. The open-loop case was realized by disconnecting the channel output from the AGC via on-board switches while the Q value was set manually via I_Q to have peak gains matched with the other cases. The closed-loop case shown in Fig. 16(a) corresponds to the AGC scheme S_0 , in which multichannel compression is performed alone. Observe that the AGC-induced multichannel compression broadens the response curves compared with the open-loop case. This is due

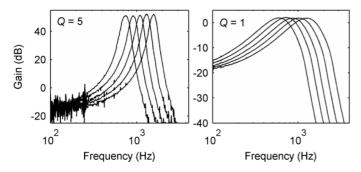


Fig. 17. Measured frequency responses of the five fabricated and CF-calibrated OZGF channels when the AGC scheme S_1 is ON for Q=5 and Q=1.

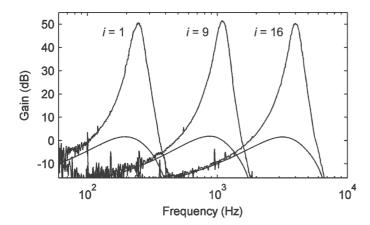


Fig. 18. Tunability and gain adaptation of the response over the frequency range of the simulated 16-channel filterbank (see Fig. 3).

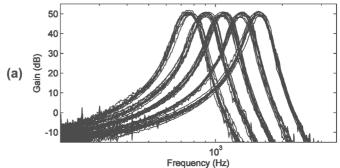
to the asymmetric amplification performed over frequencies; that is, the frequency region with weak spectral content (far away from the filter's CF) gets enhanced relative to the intense one (close to the CF). Note however that such an asymmetry decreases when the signal strength sensed by the AGC is as low as the threshold of the AGC transfer characteristic, resulting in a maximum peak gain of $\sim 50~\mathrm{dB}$.

It is interesting to see in Fig. 16(b) that the compressed OZGF responses are sharpened and thus have improved frequency selectivity in the AGC coupling-on case S_2 , which emulates the LI mechanism sharpening the frequency tuning in the auditory system [27], [28]. Note that the effects of compression together with spectral enhancement (thanks to the emulated LI) decrease as the AGC input strength approaches the transfer characteristic threshold, resulting in approximately the same response curves with $\sim 50~\mathrm{dB}$ peak gains.

Fig. 17 shows the measured frequency responses of the fabricated and CF -calibrated five channels for the coupled AGC scheme S_1 with two different Q values. Observe that the responses exhibit quite stable characteristics in all these cases.

Fig. 18 shows frequency tunability and gain adaption measured results when the fabricated channels are configured (via tuning I_0) as the 1st, 9th & 16th channels of the simulated 16-channel filterbank.

Fig. 19 shows variability results measured across a total of 15 chips. For the five channels (i = 7 to 11), their respective mismatch in the gain does not exceed 4 dB [see Fig. 19(a)] while



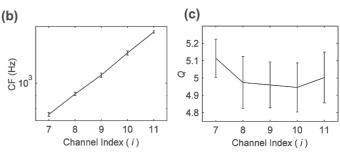


Fig. 19. Measured across-chip (15 chips) variability results for the fabricated channels of i=7 to 11. (a) Across-chip frequency responses. (b) CF mismatch error bars. (c) Q mismatch error bars. For the five channels, the relative standard deviations (RSD) are 1.75%, 1.47%, 1.84%, 1.79%, and 1.05% for the CF and 2.16%, 3.01%, 2.66%, 2.87% and 2.93% for the quality factor Q.

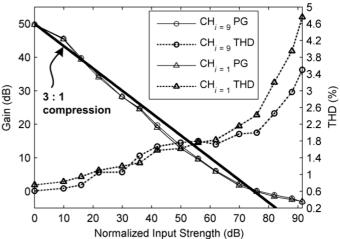


Fig. 20. Plots of the measured peak gain (PG) at the CF and the corresponding THD versus input strength (normalized with respect to the minimum, 80 pA) of $\text{CH}_{i=1}$ and $\text{CH}_{i=9}$ for the uncoupled AGC scheme S_0 . The bold line indicates a reference slope of -2/3 corresponding to 3:1 compression of input level to output level.

the standard deviations of the CF and Q are less than 1.9% and 3.1% respectively in relative terms [see Fig. 19(b) and 19(c)]. A digitally programmable system can minimize such offsets via offset calibration bits.

D. Linearity Performance

The maximum allowable total harmonic distortion (THD) for the system was specified at 5% over the whole input-strength range. This THD figure was chosen as suggested in [21], [29], [30] for the desirable linearity performance for CIs.

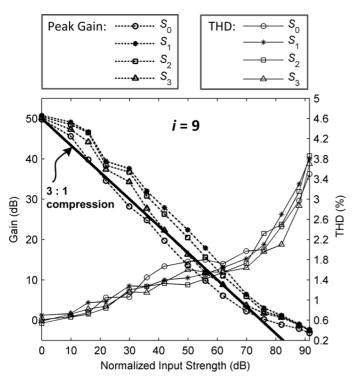


Fig. 21. Plots of the measured adaptive peak gain at the CF (dotted line) and the corresponding THD (solid lines) versus channel input strength (normalized with respect to the minimum, $80 \, \mathrm{pA}$) of $\mathrm{CH}_{i=9}$ for the four different AGC weighting schemes $(S_0 - S_3)$. The bold line without markers indicates a reference slope of -2/3 corresponding to 3:1 compression of input level to output level.

Our measurements focus on investigating how the measured output THD varies when the filter peak gain changes adaptively with the input level because of the AGC and according to the four different sets of weighting (S_0-S_3) . Attention was also paid to different channels; that is, whether the THD is affected by different biasing conditions for obtaining different CFs. The measured results are shown in Figs. 20 and 21. The peak gain decreases with an increase in the input strength for both channels of i=1 and i=9 while the corresponding THD at the CF gradually increases over the whole input-strength range. The AGC scheme provides approximately 3:1 compression of input level to output level as illustrated by the reference slope.

Observe in Fig. 20 that the peak gain versus input strength curve derived for the S_0 case is the same for both i=1 and 9 because of the scaling of the AGC output I_Q with I_0 . On the other hand, the difference between the THD in the two cases starts to become noticeable as the input strength reaches the μ A-range (> 80 dB relative to the minimum 80 pA) where the i=1 case gives a output THD of 4.76% for a 3 μ A (\sim 92 dB) input tone while the THD of i=9 is lower at 3.5%. For i=16, the measured THD values (not shown here) are even lower for the μ A-range input where they are at 1.7%, 2.5% and 2.8% for an input level at 1 μ A, 2 μ A and 3 μ A respectively. The results confirm the good class-AB operation of the circuits.

The THD difference across channels can be due to different biasing conditions: small DC (or quasi-DC in the case of I_Q) biasing currents for obtaining low CFs force some transistors forming the translinear loops of the biquads to deviate (due

to small V_{GS}) from their optimum $\ln(I_{DS})$ - V_{GS} linear range which ensures logarithmic conformity. This case is likely to be worsened by the use of large W/L to extend the upper limit of the WI range, which further decreases V_{GS} . For a certain biasing current range required for the desired CFs, it seems difficult to optimize the THD for both the higher- and lower-end of the WI range by simply adjusting the transistor sizes. Such optimization can be facilitated by means of tuning the capacitors in the biquads simultaneously at the expense of some area.

Observe in Fig. 21 that for all the weighting sets S_0 – S_3 , the channel (i=9) provides approximately the same peak gain of $\sim 50~\mathrm{dB}$ for an 80 pA $(0~\mathrm{dB})$ input and the same one of $-3~\mathrm{dB}$ at $3~\mu\mathrm{A}(\sim 92~\mathrm{dB})$ input. This was achieved by manipulating the AGC parameters (especially the combination of $I_{0_control}$ and I_{th}) to yield the same Q_{max} and Q_{min} respectively for S_0 – S_3 . The resulting THD values for S_0 – S_3 are close to each other, and the difference does not exceed 0.6% over the whole inputstrength range which spans across more than 4.5 decades.

E. Input Dynamic Range (DR)

In this work, the definition of input DR was associated with a) a given maximum allowable output THD, which corresponds to the upper limit of the input level, and b) the input noise floor, which sets the lower limit—the minimum input level should be set above this limit for good signal integrity. The measured DR, which takes into consideration the AGC's contribution, was calculated as the ratio of the maximum input level giving $\sim 5\%$ THD with $Q_{\rm min}\approx 0.85$ over the minimum input with $Q_{\rm max}=5$.

The worst and best THD cases were found to happen at the lowest (i = 1) and highest (i = 16) CF channels respectively, whose corresponding maximum allowable input levels for < 5% THD are 3 μA and 5 μA . The measured noise floors (RMS values) of the two "boundary" channels and other channels are listed in Tables III and IV. Note that these figures were measured for the minimum allowable input signal, an 80 pA input tone, which gives $Q_{\rm max}=5$ via the calibrated AGC. In other words, the minimum input signal level was specified, as mentioned earlier, to exceed the noise floor even in the worst case where i = 16 and 80×0.707 (RMS) > 35.3 pA. Also note that different channels have different noise floor levels. These differences arise from different biasing conditions (which also account for the THD differences): the small DC biasing currents yield better noise performance of low-CF channels compared with high-CF ones. On the other hand, the noise floor is approximately the same for S_0 – S_3 and the open-loop case (whose Qvalue was set manually equal to those regulated by the AGC). This finding suggests that the noise contribution of the AGC is very small relative to the overall system noise, which is likely because the AGC output is a quasi-DC signal which is out of the channel passband.

In summary, the system input DR for S_0 – S_3 is 92 dB with < 5% THD, although the difference among channels exists (< 6 dB). This DR figure has taken into consideration the worst THD and the worst noise-floor cases which happen at the lowest (i=1) and highest (i=16) CF channels respectively.

F. Single-Tone Test

The above tests have shown the ability of the emulated LI to sharpen the OZGF response. We now look into how this effect is distributed across channels via a single-tone test. This test was performed concurrently with the THD measurements for i=9: we measured at the neighboring channels' (i=7,8,10 and 11) output amplitudes of the copies of the test tone. The output tone amplitudes normalized with respect to that of i=9 are plotted versus input amplitudes normalized with respect to the minimum amplitude of $80~\mathrm{pA}$ in Fig. 22. Observations that:

- 1) The output amplitudes of the neighboring channels are suppressed relative to that of i=9 (being negative in dB) because of the frequency selectivity of each channel.
- 2) The suppression for i=8 and i=10 is less than for i=7 and 11 as the passbands of the former are closer to that for i=9
- 3) The suppression for i = 7 is larger than for other channels as the test tone is located at the high-frequency roll-off side of its corresponding channel CF.
- 4) The suppression is larger in the AGC coupling-on (S_1-S_3) cases than in the coupling-off (S_0) case.
- 5) The suppression becomes successively stronger from S_3 to S_1 as more and more "weights" are given to the neighboring channel signals in the coupling function (11).
- 6) The extent of suppression decreases as the input amplitude increases since each channel frequency selectivity degrades when Q decreases via the compressive action of the AGC. Thus the four AGC schemes provide very similar extents of suppression for a large input signal.

The above observations (4) and (5) reveal that the emulated LI is able to enhance across-channel contrasts and thus provide a more channel-specific spectral response pattern for a certain filterbank input signal. This is further supported by the results of our complex-tone test presented next.

G. Complex-Tone Test

The test input is a complex tone synthesized from five pure tones at 720, 900, 1080, 1320, and 1560 Hz with normalized amplitudes of -10, 0, -10, 0, and -10 dB. These frequencies were set to be close to the CF of i=7 to 11 (Q=5) respectively. The fundamental frequency of this complex tone is of 60 Hz.

Fig. 23 plots the output RMS levels measured for different channels (normalized with respect to the maximum one among the five) and for different input RMS levels in 10 dB increments. Observe that the AGC coupling schemes (S_1-S_3) enhance the difference among the channel outputs. The emulated LI mechanism manifests itself in the following way: the two stronger constituent tones corresponding to i=8 and 10 have the effect of suppressing the other weaker neighboring tones corresponding to i=7, 9 and 11. The suppression gets successively stronger from S_3 to S_1 and weaker as the input level increases across two decades. These observations are consistent with the single-tone test findings.

Fig. 24 shows the increase in the across-channel contrast of i=7, 9 and 11 relative to i=8 and 10, averaged over the input RMS levels. The maximum average increase (20 dB) is seen with S_1 at i=7 while the worst case (8 dB) corresponds

TABLE III
MEASURED NOISE FLOOR FOR DIFFERENT CHANNELS

Channel Index i	$CF(Hz)_{when Q=5}$	Noise Floor (pA)
1	250	9.6
7	760	14.3
8	920	16.4
9	1100	17.8
10	1320	19
11	1590	21
16	4000	35.3

TABLE IV
MEASURED NOISE FLOOR FOR THE FOUR AGC SCHEMES AND THE
OPEN-LOOP CASE

AGC Scheme	Noise Floor (pA) for $i = 9$
S_{θ}	17.8
S_I	17.62
S_2	17.7
S_3	17.9
Open-loop	17.58

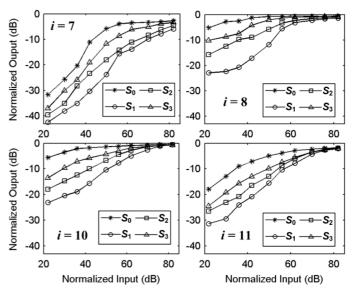


Fig. 22. Single-tone output versus input amplitudes of the neighboring channels (i = 7, 8, 10 and 11) normalized with respect to the channel of i = 9. The input amplitude is normalized with respect to the minimum, 80 pA.

to S_3 at i=11; the increase is slightly smaller at the higher CF channel (i=11), which can be accounted for by the OZGF passband asymmetry (i.e., the frequency selectivity is lower at the low frequency side of the CF, and thus this channel gets less suppression from those of i=8 and 10).

VI. SUMMARY AND CONCLUSION

This work presents an ultra-low-power analog system which provides speech preprocessing of increased biofidelity in CIs. Thanks to the use of weak-inversion transistors, the 5-channel silicon IC prototype consumes only $28 \mu W$. Most

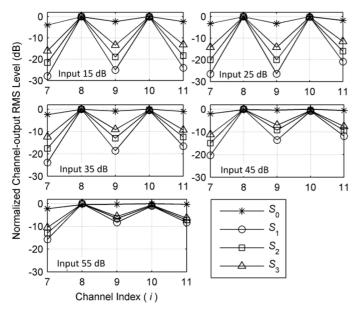


Fig. 23. Output RMS levels versus channel, measured at different input RMS levels (in dB relative to the RMS value of the minimum input amplitude 80 pA, i.e., ~ 57 pA). The output RMS levels are normalized with respect to the maximum level (0 dB) among i=7 to 11.

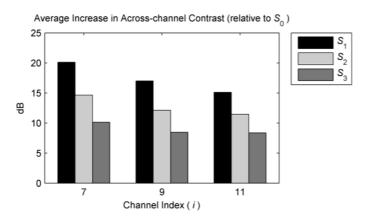


Fig. 24. Increase in the across-channel contrast (S_1-S_3) relative to S_0) averaged over the input RMS levels (15–55 dB relative to the RMS value of the minimum input amplitude 80 pA, i.e., ~ 57 pA).

likely this figure will be 3 times higher for a 16-channel version of the present design, thereby allowing full implantation inside the human body along the lines of the nice works presented in [29], [30]. The 16-channel version would occupy $\sim 7.5~\text{mm} \times 7.5~\text{mm}$, an area comparable to that of an ultra-low power analog 16-channel CI processor reported in [30], which occupies 9.58 mm \times 9.23 mm. Area can be saved by using smaller capacitance when realizing the CFs of higher-frequency channels, and this potential saving becomes larger when the targeted frequency range is wider (e.g., from 250 Hz to 8 kHz, as opposed to a range of 250 Hz to 4 kHz, for 16 channels).

One of the most attractive aspects of this work is probably the VLSI realization of lateral inhibition (LI) via low power and compact coupled AGC circuits. The results measured from the IC prototype show that the design has the ability to reproduce this biological property, which is known to enhance the spectral features of sound and may improve hearing performance in noisy listening environments. The emulated LI manifests itself as the sharpening of the frequency response and increased across-channel contrasts. We believe that the VLSI-compatible way of emulating the LI, presented in this work, provides a good trade-off between bio-fidelity and power consumption, since it only needs one specially built AGC block to implement the coupling function and thus does not significantly increase the overall system's area and power consumption (the AGC consumes 7 μ W, only 25% of the total power of the system). In summary, while being well compatible with fully implantable CI systems of the future, the proposed system is characterized by closer biomimicking of signal processing (asymmetry in passband, level-dependent properties and LI), which has been suggested as one of the future directions for CIs [31], [32].

In future we aim at incorporating more channels (e.g., a total of 16 channels) and eventually developing the prototype into a complete OZGF-with-LI based CI processor including a microphone preamplifier preceding the filterbank, stimulation circuits (e.g., [33]) and digital-to-analog converters for realizing programmability. We also consider it useful to introduce a broadband AGC (e.g., [34]) between the preamplifier output and the filterbank input in this processor since the overall AGC performs compression resulting in a smaller required DR (e.g., 40–60 dB) for the filterbank. In this case, the silicon area can be optimized by: 1) scaling down the transistor sizes since large aspect ratios were employed in the present design to extend the maximum allowable current signal under subthreshold MOS operation to μ A-range yielding a wide DR; 2) adopting class-A micropower log-domain designs which can achieve a moderate DR of 50-60 dB as reported in [29] while saving half the transistor/capacitor area of the present class-AB design which provides a wide input DR of over 90 dB thanks to the pseudo-differential architecture containing two class-A paths; 3) using lower order OZGFs (and hence less biquads in the cascade) at the expense of bio-fidelity (e.g., the emulated sharp frequency tuning in the cochlea). Third-order OZGFs (N=3, as opposed to N= 4 used in the prototype) can preserve adequately basic auditory response profiles.

As the total number of channels in the filterbank increases (e.g., from 16 to 32), more neighboring channel outputs (e.g., $i\pm 3$) are likely required to be fed into the AGC so that the emulated LI results in spectral enhancement not too local around the spectral peaks (corresponding to "strong" channels), in the frequency domain. This can extend the use of the coupled AGC in future CI systems whose channel numbers will likely be largely increased for improving spectral resolution and hence CI users' listening performance in noise [35], [36]. In addition, the AGC coupling sets $(S_1 - S_3)$ with different weighing factors, which were chosen mostly from the perspective of practical implementation in this work, may be further optimized in terms of their resulting effects on listeners' listening performance to acoustic signals processed by the "OZGF-with-LI" strategy.

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