Optimal trajectory control for parallel single phase H-bridge inverters

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***Abstract*— We describe a novel inverter control method that solves an optimization problem during each switching interval to closely follow a virtual impedance control law. We report droop behavior over a wide range of applied loads and power sharing among multiple inverters.**

I. Introduction

The modern power grid is stabilized in part by large amounts of rotating inertia with the equivalent of many seconds of energy storage [2], [3]; this feature is typically absent on a small microgrid which underlies the challenge of designing systems that can rapidly respond to load changes [4], [5]. To meet an objective of responding in less than one AC cycle, we propose to design a tight, single loop control algorithm that implements a virtual impedance law that droops voltage with increased load, thereby ensuring stability on short time scales. On the conventional power grid, the Independent Systems Operator controls power dispatch from a small number of very large sources; on a microgrid we anticipate that optimal power flow algorithms [6], [7] will suggest the desired amounts of real and reactive power sourced by many small sources across a schedule throughout which load, price, and capacity all vary with time. To allow many small power sources to share varied amounts of real and reactive power, we propose a mapping of scheduled power to a virtual Thévinin source that gets updated as power schedules change. This ensures optimal resource sharing on a timescale of minutes to hours.

II. System model and control objective

A. System model

A DC voltage source is the energy source in the model because PV and batteries are common on microgrids. To convert DC into AC, we use H-bridge inverters with output LCL filters. LCL filters introduce an LC resonance to the system, which adds additional complexity from a control perspective, but if properly managed, the LCL filter can provide excellent harmonic suppression with high power conversion efficiency [8]. Successful usage of the LCL filter has been reported in grid-connected PV inverters [9] as well as grid-connected voltage-source converters [8], [10] to name two of many areas. After the output LCL filter, an inverter is connected to a single phase AC power bus, which may be islanded (weak) or grid-tied (stiff); we postulate the the number and type of devices on the common electrical bus is unknown to the controller.

Fig. 1 shows the inverter configuration and the parameter and signal notations.

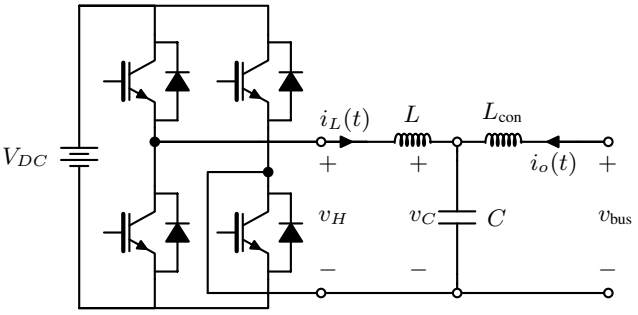

Fig. 1: System model

We assume an ideal H-bridge; therefore, the control input, $v_H(t)$, applied to the LCL filter can be $+V_{DC}, 0$, or $-V_{DC}$. See Fig. 2 for each configuration.

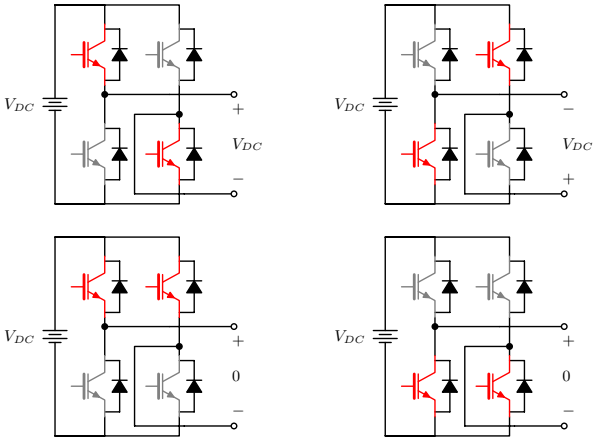

Fig. 2: Bang-off-bang configuration of H-inverter.

B. Control objective

There are many control techniques for generating AC from a DC source such as pulse width modulation (PWM) control, PID control [11], proportional resonant control [12], boundary control [13], and linear quadratic regulator [14] (LQR) to name a few. Microgrids have control objectives requiring particular attention:

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The published version can be found in [1], and DOI of the published version is 10.1109/CDC.2015.7402498.

1) **Frequency regulation**: Many sources must operate at a common frequency and voltage phase without a synchronizing clock.
2) **Voltage regulation**: The root mean square (RMS) value of the output voltage of the inverter should be in a predetermined range to ensure system safety, reliability and performance.
3) **Plug and play operation**: Loads and sources can be seamlessly connected to or disconnected from microgrids.
4) **Accurate P, Q and V_{bus} dispatch**: Each power source has a *nominal* real power and reactive power dispatch schedule; collectively, all sources on the same power bus have a *nominal* scheduled output voltage. This schedule may be optimized economically.
5) **Wide range of operating region**: The microgrids must robustly tolerate abrupt changes. For example, serving a very light load (almost open circuit) that transitions to a grid-tied or a near-short circuit load. Moreover loads need to vary, connect and disconnect from the microgrid on a short time scale ($\leq$ 1 AC cycle) without explicit communication with sources.
6) **Parallel inverters with different capacity**: Power sources in microgrids can have a different capacity, and the controller for each inverter should operate in a predictable manner.
7) **Fast transient response**: The microgrid may have a insignificant rotating inertia compared to the conventional grid. Therefore, the controller is required to enter the steady state mode in a relatively short time, for example within one or two cycles.

A conventional inverter control technique may fail to achieve some of the above objectives. For example, open loop PWM control cannot handle the wide range of operating conditions, and PID control requires significant gain tuning whenever the system configuration changes (*e.g.*, changing nominal power dispatch schedules, adding source/load, connecting to the grid). A conventional output current controller for PV inverters [9] may not operate in the open circuit condition, and the parallel Uninterruptible Power Supply inverter controller [15] may fail to achieve load sharing among sources with different capacity.

III. Control architecture

To achieve the objectives above, we propose the following control architecture. We assume that a periodic (*e.g.* every 15 minutes) power dispatch schedule for nominal source operation has been determined using communication between sources and loads in the microgrid. For example, one can use distributed Optimal Power Flow (OPF) solvers [7], [16] to obtain the dispatch schedule.

A primary control task is to stabilize the grid during unscheduled events. While explicit communication can find a good *nominal* operating point schedule, limited communication bandwidth prevents sufficiently rapid coordination to handle fast (*e.g.* 8 msec) disturbances.

To respond on short time scales, we coordinate controllers using the bus voltage - a mechanism commonly called *droop*. Voltage drop below nominal signals insufficient power supply, so the power sources are expected to supply more power. Similarly, voltage rise signals oversupply, so the power sources are expected to decrease output. As we mentioned, the bus RMS voltage should be in the pre-described region, so we assume that the bound is given by $[V_{\text{min}}, V_{\text{max}}]$, and the RMS value of the nominal bus voltage $|V_{\text{nom}}|$ is in this interval. We typically require this region to be $\pm 10\%$ of the nominal RMS bus voltage; practically, the range is determined by what grid appliances can handle safely and efficiently.

Multiple power sources will each adjust power supply in response to the voltage deviation from the nominal bus voltage, but not by equal amounts because their scheduled outputs and their overall power capacities may differ. Since we do not mimic the synchronous generators using our controller, the conventional $P-\omega$, $Q-V$ relationships are not necessarily true in this context.

Commonly PLL grid frequency and phase synchronization are used to eliminate unintended inverter reactive power. For simplicity, the work presented here models the PLLs across inverters with synchronized internal clocks. Further research can investigate active PLLs in such a configuration

A. Ideal behavior: Virtual impedance

Virtual impedance and droop has been used before [17], [18]; it is simply controlling power electronic sources to follow Ohm's law even though their physical components do not do so inherently. The corresponding ideal Thévenin source is shown in Fig. 3 below; the key point is that the droop voltage across the virtual impedance serves as implicit power sharing signaling between controllers on timescales faster than they can communicate explicitly. A new facet we introduce is to use the dispatch schedules $[(P_o, Q_o)_{m,n}, V_{\text{nom},n}]$ for multiple inverters m on the power bus and multiple schedule intervals n to prescribe *both* virtual impedance settings $\hat{Z}_{v,m,n}$ and reference voltage phasors $\hat{V}_{\text{ref},m,n}$ for each inverter and schedule interval. Here we use the hat symbol to distinguish ideal source parameters and signals from actual hardware component parameters such as physical inductors and capacitors and actual voltage and current measurements. The reference voltage $\hat{v}_{\text{ref}}(t) = \sqrt{2}|\hat{V}_{\text{ref}}|\sin(2\pi f t + \angle\hat{V}_{\text{ref}})$ where f is the grid frequency.

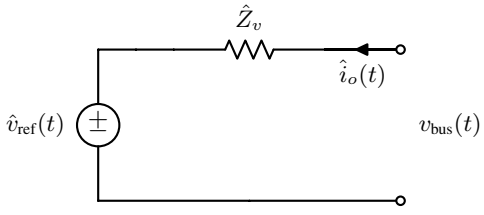

Fig. 3: Ideal Thévenin source. We note that our current sign convention in Fig. 1 and Fig. 3 points toward the source (power delivered is negative) following the convention in Kraning et al [7].

To define the Thévenin equivalent, we apply the following design choices:

a) When the bus voltage phasor V_{bus} is equal to $V_{\text{nom},n}$, each inverter outputs its respective complex power $S_{o,m,n} = P_{o,m,n} + jQ_{o,m,n}$. The output current phasor $\hat{I}_{o,nom}$ of each device at V_{nom} is (m and n subscripts dropped):

$$\hat{I}_{o,nom} = \frac{V_{\text{nom}} - \hat{V}_{\text{ref}}}{\hat{Z}_v},$$

and therefore the apparent power is

$$S_o = V_{\text{nom}} \hat{I}^*_{o,nom}.$$

V_{nom} is identical for every device on the same power bus. For an islanded microgrid the phase angle $\angle V_{\text{nom}}$ is arbitrary (grid forming); but, for a connected bus, both the amplitude and phase are determined by power flow optimization. Connection to a stiff power grid, for example, requires that $V_{\text{nom}} = V_{\text{grid}}$ (grid following).

b) To meet the design objective above, we have choices for both $\hat{V}_{\text{ref}}$ and $\hat{Z}_v$. We set $|\hat{V}_{\text{ref}}| = V_{\text{max}}$ for all m power sources on the bus. This defines the open circuit bus voltage magnitude.

c) $\angle \hat{V}_{\text{ref}} = \angle V_{\text{nom}}$ for all m power sources on the bus. This ensures that when $|V_{\text{bus}}| = V_{\text{max}}$ the output power of the device is close to zero provided $\angle V_{\text{bus}} \approx \angle V_{\text{nom}}$.

Hence, the virtual impedance used in what follows is

$$\hat{Z}_{v,m,n} = \frac{V^*_{\text{nom}} \left(V_{\text{nom}} - \hat{V}_{\text{ref},m,n} \right)}{S^*_{o,m,n}}.$$

There is a larger design space for virtual source definition. For example, our algorithm continuously estimates the bus voltage phasor $V_{\text{bus}}(t)$ in order to determine what output power

$$P_{m,n} + jQ_{m,n} = \frac{V_{\text{bus}}(V_{\text{bus}} - \hat{V}_{\text{ref},m,n})^*}{\hat{Z}^*_{v,m,n}}$$

to source. An interesting design rule (not yet explored) is $\angle \hat{V}_{\text{ref}} = \angle V_{\text{bus}}(t)$ which would curtail all apparent power when $|V_{\text{bus}}| = V_{\text{max}}$.

B. Optimal trajectory generation

Now, having the ideal Thévenin source *setting*, the next step is to design a controller that closely follows that behavior using the inverter dynamics. Our control technique consists of two steps. The first step is to compute the ideal filter inductor current and the filter capacitor voltage waveforms that simulate the ideal Thévenin source and the second step is to find an input, $v_H(t)$, that induces a close approximation to those waveforms in the physical components of the inverter.

In this section, we focus on the first step. From the system model (See Fig. 1), we have the following dynamics:

$$L \frac{di_L}{dt} = v_H - v_C \tag{1}$$

$$C \frac{dv_C}{dt} = i_L + i_o \tag{2}$$

$$L_{\text{con}} \frac{di_o}{dt} = v_{\text{bus}} - v_C. \tag{3}$$

Here all the quantities are physical ones. Using the above inverter dynamics, we approximate the behavior of the ideal Thévenin source using the phasor droop control law

$$\hat{I}_o = \frac{V_{\text{bus}} - \hat{V}_{\text{ref}}}{\hat{Z}_v}. \tag{4}$$

We measure $v_{\text{bus}}(t)$, from which we then determine the phasor, V_{bus} (details below). Recognizing that $\hat{I}_o$ is a phasor quantity, the ideal behavior, what we call the *objective trajectory*, for the output current can be determined from its corresponding waveform,

$$\hat{i}_o(t) \approx \sqrt{2} |\hat{I}_o| \sin(\omega t + \angle \hat{I}_o),$$

where $\omega = 2\pi f$. Likewise, working from equation 3, we can determine the ideal phasor $\hat{V}_c$ for the filter capacitor voltage,

$$\hat{V}_c = V_{\text{bus}} - j\omega L_{con} \hat{I}_o,$$

as well as its corresponding *objective trajectory*

$$\hat{v}_c(t) \approx \sqrt{2} |\hat{V}_c| \sin(\omega t + \angle \hat{V}_c).$$

Continuing to apply equations (2) and (1) we can progress from right to left through the LCL filter in Fig.1 to derive the phasors and objective trajectories for $\hat{I}_L$ and $\hat{V}_H$.

Thus once we have determined the phasor, $\hat{V}_{\text{bus}}$, from sampled bus voltages, then we uniquely determine all of the phasor quantities and ideal objective trajectories. If at this point we were to apply an average value control algorithm, we could take the objective trajectory for $\hat{v}_H(t)$ and switch the H-bridge in Fig.1 to approximate $\hat{v}_H(t)$ during each switching interval. Results using this approach are not reported here; but were explored to a limited degree and provided encouraging results for the dispatch of scheduled power. In this paper, we describe a *dual goal controller* that optimally follows both the $\hat{i}_L$ and $\hat{v}_C$ trajectories closely. The reasoning behind this is to give the controller behavior that is current-source-like in the short circuit condition and voltage-source-like in the open circuit condition.

Now we propose two different approaches for converting continuous time signals to discrete time signals for ease of implementation: a phasor method and a discrete time filter method.

1) Phasor method: Our RMS bus voltage phasor estimator works by the principle of weighted least square fitting. Let $v_{\text{bus}}[k]$ be the kth sample of v_{bus}, and h be the sampling time. Then $v_{\text{bus}}[k] = v_{\text{bus}}(kh) = \sqrt{2}|V_{\text{bus}}| \sin(\omega kh + \angle V_{\text{bus}}) = \mathbf{Re}(\sqrt{2}V_{\text{bus}}) \sin(\omega kh) + \mathbf{Im}(\sqrt{2}V_{\text{bus}}) \cos(\omega kh)$.

Using x and y to represent $\mathbf{Re}(\sqrt{2}V_{\text{bus}})$ and $\mathbf{Im}(\sqrt{2}V_{\text{bus}})$ we solve the following least square problem:

$$\underset{x,y}{\text{minimize}} \quad \sum_{n=0}^{k} \gamma^{k-n} (v_{\text{bus}}[k] - x \sin(\omega kh) - y \cos(\omega kh))^2$$

Here γ is a discounting factor that assigns more importance to the recent observations, and we choose $\gamma = 0.99$.

Let x_k, y_k be the solution of the above optimization. Then the estimated V_{bus} at time kh is given by $\mathbf{Re}(V_{\text{bus}}) = x_k$,

and $\mathbf{Im}(V_{\text{bus}}) = y_k$. Notice that x_k, y_k can be obtained using the following analytic formula.

$$\begin{bmatrix} x_k \\ y_k \end{bmatrix} = (A_k^T W_k A_k)^{-1} A_k^T W b_k,$$

where

$$\begin{aligned} A_k &= \begin{bmatrix} \sin(\omega kh) & \cos(\omega kh) \\ \sin(\omega(k-1)h) & \cos(\omega(k-1)h) \\ \vdots & \vdots \\ 0 & 1 \end{bmatrix} \\ b_k &= \begin{bmatrix} v_{\text{bus}}[k] \\ v_{\text{bus}}[k-1] \\ \vdots \\ v_{\text{bus}}[0] \end{bmatrix} \\ W_k &= \mathbf{diag}\{1, \gamma, \cdots, \gamma^k\}. \end{aligned}$$

However, this batch update is computationally demanding and not suitable for our fast time scale controller. Using the Sherman-Morrison formula, we can derive an incremental update rule for x_k, and y_k, which is a more suitable algorithm for our controller [19]. Recall that x_{k+1}, y_{k+1} is given by

$$\begin{bmatrix} x_{k+1} \\ y_{k+1} \end{bmatrix} = (A_{k+1}^T W_{k+1} A_{k+1})^{-1} A_{k+1}^T W b_{k+1}.$$

Let $\Theta_k = (A_k^T W_k A_k)^{-1}$, and $A_{k+1} = \begin{bmatrix} a_{k+1}^T \\ A_k \end{bmatrix}$, where $a_{k+1}^T = \begin{bmatrix} \sin(\omega(k+1)h) & \cos(\omega(k+1)h) \end{bmatrix}$. Then $A_{k+1}^T W_{k+1} A_{k+1} = a_{k+1} a_{k+1}^T + \gamma A_k$, and

$$\begin{aligned} \Theta_{k+1} &= (a_{k+1} a_{k+1}^T + \gamma A_k)^{-1} \\ &= \frac{1}{\gamma}\Theta_k - \frac{1}{\gamma^2 + \gamma a_{k+1}^T \Theta_k a_{k+1}} \Theta_k a_{k+1} a_{k+1}^T \Theta_k. \end{aligned}$$

In addition, let $c_k = A_k^T W b_k$. Then

$$c_{k+1} = \gamma c_k + v_{\text{bus}}[k+1] a_{k+1},$$

and

$$\begin{bmatrix} x_{k+1} \\ y_{k+1} \end{bmatrix} = \Theta_{k+1} c_{k+1},$$

which shows a better computational complexity compared to the batch update.

2) Discrete time filter method: Based on the system model, (1) - (3) and the ideal Thévenin source equation (4), we can compute the Laplace transform of the ideal filter inductor current as well as the ideal capacitor voltage:

$$\begin{aligned} \hat{I}_o &= \hat{Y}_v(V_{\text{bus}} - \hat{V}_{\text{ref}}) \\ \hat{V}_C &= V_{\text{bus}} - sL_{\text{con}}\hat{I}_o \\ \hat{I}_L &= sC\hat{V}_C - \hat{I}_o \\ \hat{V}_H &= sL\hat{I}_L + \hat{V}_C, \end{aligned}$$

where $\hat{Y}_v = \frac{1}{\hat{Z}_v}$. Since the microcontroller can only use discrete time signals, we propose a discrete time filter method to simulate the above transfer functions. The main idea is to approximate $sX(s)$ using

$$sX(s) \approx \frac{1}{h}(x[k] - x[k-1]), \tag{5}$$

where h is a sampling time.

For the virtual impedance $\hat{Z}_v(j\omega)$, we take an admittance form $\hat{Y}_v(j\omega) = G_d + j\omega B_d$, We can assume that $G_d \geq 0$, otherwise the behavior of inverter would be to absorb active power from the load, which makes no sense. On the other hand, there is no assumption on B_d. Depending on the sign of B_d, the ideal Thévenin source can show the inductive or capacitive behavior. If $B_d > 0$, then we take $\hat{Y}_v(s) = G_d + s|B_d|$, and if $B_d < 0$, then we take $\hat{Y}_v(s) = G_d + \frac{1}{s}|B_d|$.

Since

$$\hat{I}_o = \hat{Y}_v(s)(V_{\text{bus}} - \hat{V}_{\text{ref}}).$$

we have,

$$\hat{I}_o(s) = \begin{cases} G_d(V_{\text{bus}} - \hat{V}_{\text{ref}}) + s|B_d|(V_{\text{bus}} - \hat{V}_{\text{ref}}) & \text{if } B_d > 0 \\ G_d(V_{\text{bus}} - \hat{V}_{\text{ref}}) + \frac{1}{s}|B_d|(V_{\text{bus}} - \hat{V}_{\text{ref}}) & \text{if } B_d < 0. \end{cases}$$

Therefore if $B_d > 0$, then we have the Proportional-Derivative controller, and if $B_D < 0$, then we have the Proportional-Integral controller for $\hat{i}_o$.

By using (5), we have

$$\begin{aligned} \hat{i}_o[k] =& K_p(v_{\text{bus}}[k] - \hat{v}_{\text{ref}}[k]) + K_i h \left(\sum_{n=0}^{k-1} v_{\text{bus}}[n] - \hat{v}_{\text{ref}}[n] \right) \\ &+ K_d \frac{1}{h} \{ (v_{\text{bus}}[k] - \hat{v}_{\text{ref}}[k]) \\ &\qquad - (v_{\text{bus}}[k-1] - \hat{v}_{\text{ref}}[k-1]) \}, \end{aligned}$$

where $K_p = G_d$, $K_i = -\min\{0, B_d\}$, and $K_d = \max\{0, B_d\}$. In addition,

$$\begin{aligned} \hat{v}_C[k] &= v_{\text{bus}}[k] - \frac{L_{\text{con}}}{h}(\hat{i}_o[k] - \hat{i}_o[k-1]) \\ \hat{i}_L[k] &= \frac{C}{h}(\hat{v}_C[k] - \hat{v}_C[k-1]) - \hat{i}_o[k] \\ \hat{v}_H[k] &= \frac{L}{h}(\hat{i}_L[k] - \hat{i}_L[k-1]) + \hat{v}_C[k] \end{aligned}$$

We can also add bandpass filter to $v_{\text{bus}}[k]$ if necessary, to reject measurement noise.

C. Optimal control for trajectory following

Once we compute the ideal trajectory of $\hat{i}_L$ and $\hat{v}_C$, the next step is to make a switching decision (bang-up, bang-off, bang-down) for the time interval $[t_k, t_{k+1}]$, where $t_k = kh$. We made design choices as follows:

a) $v_H = 0$ (bang-off) at the start of each interval.
b) At an optimized time within $[t_k, t_{k+1}]$ the controller can switch only once to either $+V_{DC}$ or $-V_{DC}$.
c) The control action for the time interval $[t_k, t_{k+1}]$ is computed during the time interval $[t_{k-1}, t_k]$.

The first and second choice limit the computational complexity and keeps the switching rate within practical limits (current about 10 kHz). The third choice allows the microcontroller to collect and estimate all the necessary signals as well as compute the objective trajectory, and make a switching decision in $[t_{k-1}, t_k]$ so that the control action for $[t_k, t_{k+1}]$ is ready at $t = t_k$. This third choice makes the controller causal so that we can actually implement our control policy using the hardware.

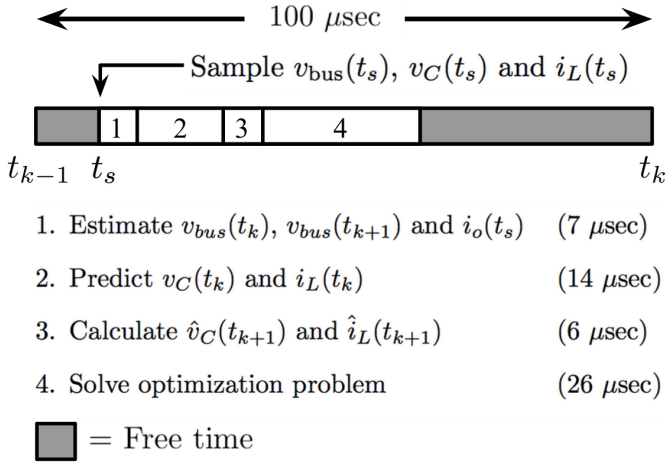

Fig. 4: An example of firmware timing results.

Since we use a microcontroller with finite processing capability to implement our control algorithm, we need to simplify the algebra as much as possible so that the computations can fit within the switching interval. Implemented in firmware on a TI C2000, we obtained compute times (highly unoptimized) illustrated in Fig. 4

Recall that based on the switching decision, bang-up, bang-off, bang-down, the output voltage of the H-bridge inverter will be approximately $V_{DC}, 0, -V_{DC}$ respectively subject to voltage drops across switching components. To choose the optimal switching decision, we use the Model Predictive Control scheme with the objective function being the integral of the weighted squared error of $i_L(t)$ and $v_C(t)$ from the objective trajectory:

$$\begin{aligned} \underset{u,\Delta t}{\text{minimize}} \quad & \int_{t_k}^{t_{k+1}} (i_L(t) - \hat{i}_L(t))^2 + \rho(v_C(t) - \hat{v}_C(t))^2 dt \\ \text{subject to} \quad & (1) - (3) \\ & u \in \{+V_{DC}, -V_{DC}\}, \quad 0 \le \Delta t \le h \\ & v_H(t) = u\mathbf{1}(t - t_k - \Delta t) \end{aligned} \tag{6}$$

where ρ is the scaling parameter, and $\mathbf{1}(t)$ is the Heaviside step function that is 0 for $t < 0$, and 1 for $t \ge 0$. Notice that this MPC is being solved by the microcontroller during the time interval $[t_{k-1}, t_k]$ because of our design choice. The decision variable in the above MPC is "when" (Δt) to switch during the time interval $[t_k, t_{k+1}]$, and "where" (u) to switch among $\{+V_{DC}, -V_{DC}\}$. In addition, if the optimal control action is not to switch during the interval $[t_k, t_{k+1}]$, then $\Delta t = h$ so that the switching direction, u, is irrelevant.

However the problem (6) is intractable, because $v_{\text{bus}}(t)$ is also coupled with $i_o(t)$ with the unknown load dynamics. In other words, unless the load characteristic is completely known, the internal model of the above MPC problem, which treats $i_o(t)$ as an independent variable, does not capture the actual dynamics of the entire system. Moreover, to compute the ideal trajectory, $\hat{i}_L(t)$ and $\hat{v}_C(t)$, we need the bus voltage and the output current over $[t_k, t_{k+1}]$. Since we solve (6) at time t_{k-1}, we can only access to the signals up to $t = t_{k-1}$, *i.e.*, the above MPC is not causal. Finally, to enumerate the objective value, the controller needs to solve the corresponding differential equation in (6), which may be prohibitive because of limited computing power of the microcontroller.

To overcome these challenges, we simplify the MPC problem (6). Firstly, we approximate $v_{\text{bus}}(t)$ using a linear function:

$$\tilde{v}_{\text{bus}}(t) := v_{\text{bus}}[k-1] + (t - t_{k-1})(v_{\text{bus}}[k-1] - v_{\text{bus}}[k-2]).$$

Since $v_{\text{bus}}[k-1]$ and $v_{\text{bus}}[k-2]$ are availabe at $t = t_k$, we can generate $\tilde{v}_{\text{bus}}(t)$ at time $t = t_{k-1}$.

Secondly, we also approximate $\hat{i}_L(t)$ and $\hat{v}_C(t)$ by linear functions:

$$\begin{aligned} \tilde{i}_L(t) &:= \hat{i}_L[k-1] + (t - t_{k-1})(\hat{i}_L[k-1] - \hat{i}_L[k-2]), \\ \tilde{v}_C(t) &:= \hat{v}_C[k-1] + (t - t_{k-1})(\hat{v}_C[k-1] - \hat{v}_C[k-2]). \end{aligned}$$

Since $\hat{i}_L[k-1], \hat{i}_L[k-2], \hat{v}_C[k-1], \hat{v}_C[k-2]$ only need $v_{\text{bus}}(t)$ for $t \le t_{k-1}$, $\tilde{i}_L(t)$ and $\tilde{v}_C(t)$ can be easily computed at $t = t_{k-1}$. The use of these two approximation makes the MPC problem (6) causal.

Finally, we use a polynomial approximation of $i_L(t), v_C(t)$ and $i_o(t)$. If we treat $v_H(t)$ as an input, then we can use the matrix exponential with the convolution operator to obtain the analytic formula of $i_L(t), v_C(t)$, and $i_o(t)$. Specifically, let

$$A := \begin{bmatrix} 0 & -\frac{1}{L} & 0 \\ \frac{1}{C} & 0 & \frac{1}{C} \\ 0 & -\frac{1}{L_{\text{con}}} & 0 \end{bmatrix} \qquad B := \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \\ 0 & \frac{1}{L_{\text{con}}} \end{bmatrix}.$$

Then the closed form expression of $\begin{bmatrix} i_L, v_C, i_o \end{bmatrix}$ in (6) is given by

$$\begin{aligned} \begin{bmatrix} i_L(t) \\ v_C(t) \\ i_o(t) \end{bmatrix} = \; & e^{A(t-t_{k-1})} \begin{bmatrix} i_L(t_{k-1}) \\ v_C(t_{k-1}) \\ i_o(t_{k-1}) \end{bmatrix} \\ & + \int_{t_{k-1}}^{t} e^{A(t-t_{k-1}-\tau)} B \begin{bmatrix} v_H(\tau) \\ v_{\text{bus}}(\tau) \end{bmatrix} d\tau, \end{aligned}$$

for $t_{k-1} \le t \le t_{k+1}$. Recall that $v_{\text{bus}}(t)$ for $t \ge t_{k-1}$ is unknown a $t = t_{k-1}$. Therefore we replace $v_{\text{bus}}(\tau)$ with $\tilde{v}_{\text{bus}}$. $v_H(t)$ for $t_{k-1} \le t \le t_k$ is known at $t = t_{k-1}$ because the control action for the interval $[t_{k-1}, t_k]$ is ready at $t = t_{k-1}$. On the other hand, for $t_k \le t \le t_{k+1}$, $v_H(t)$ is determined by the controller through the MPC scheme. To avoid the computational complexity of matrix exponential, we use the quadratic polynomial to approximate the above dynamics based on Taylor series expansion:

$$\begin{aligned} \begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_C(t) \\ \tilde{i}_o(t) \end{bmatrix} = (I + (t - t_{k-1})A + \frac{(t-t_{k-1})^2}{2} A^2) \begin{bmatrix} i_L(t_{k-1}) \\ v_C(t_{k-1}) \\ i_o(t_{k-1}) \end{bmatrix} \\ + \int_{t_{k-1}}^{t} (I + (t - t_{k-1} - \tau)A) B \begin{bmatrix} v_H(\tau) \\ \tilde{v}_{\text{bus}}(\tau) \end{bmatrix} d\tau \end{aligned} \tag{7}$$

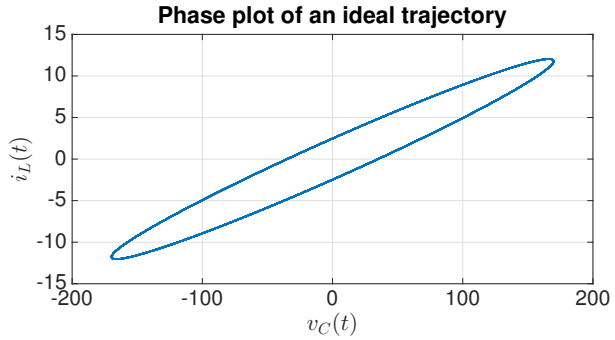

Fig. 5: An example of a phase plot of ideal trajectory.

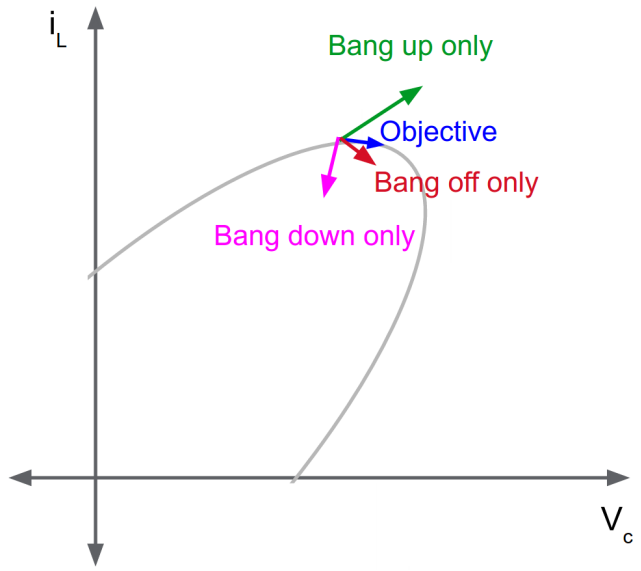

Fig. 6: Impact of control action in the phase plot. In this example, the bang-off is the optimal control choice, because it is closest to the phase plot of the ideal trajectory.

Now we present the simplified version of (6):

$$\underset{u,\Delta t}{\text{minimize}} \quad \int_{t_k}^{t_{k+1}} (\tilde{i}_L(t) - \check{i}_L(t))^2 + \rho(\tilde{v}_C(t) - \check{v}_C(t))^2 dt$$
$$\text{subject to} \quad (7), \quad u \in \{+V_{DC}, -V_{DC}\}, \quad 0 \le \Delta t \le h.$$

With these substitutions, the signals in the above MPC can be computed using the quantities that are available at $t = t_k$, therefore we can obtain u and Δt that minimizes the cost.

Fig. 5 shows an example of a phase plot of ideal trajectory, and Fig. 6 shows the impact of control action in the phase plot. In this case, the bang-off is the optimal input because it error between the ideal trajectory and the predicted trajectory under the control action is minimum among three choices. Here we choose $\Delta t = 0$ for an illustrative purpose.

IV. Simulation Results

In this section, we present simulation results. We summarize the model parameters in Table I.

T_s	100 μs	V_{DC}	240 V	V_{nom}	120 V RMS
L	2.30 mH	C	44.2 μF	L_{con}	1.15 mH

TABLE I: Model parameters, $V_{\max} = 200$ V RMS

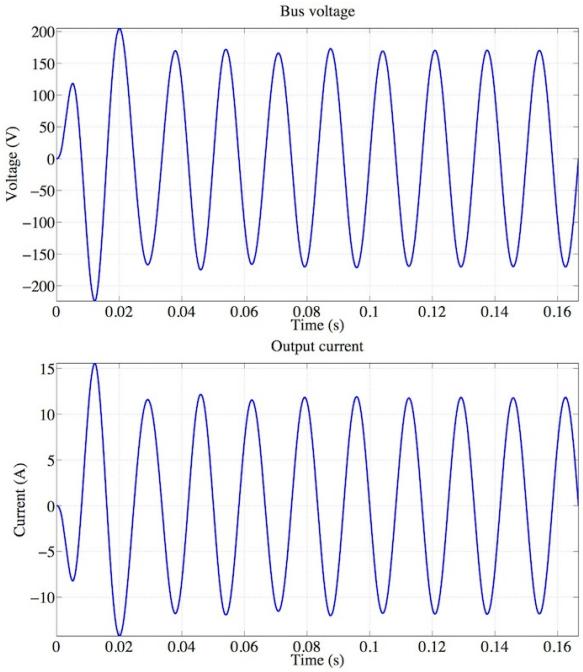

Fig. 7: The output current and the bus voltage from single source single load configuration with discrete time filter method. $V_{\text{bus}} = 122.3102$ V RMS and $I_{\text{o}} = 8.4147$ A RMS, and $P = 1.092$ kW.

A. One source, one load

First we consider a single source serving one load, beginning from a cold start ($v_{bus} = i_o = 0$). The nominal bus voltage is 120 V RMS, and the source is expected to supply 1.0 kW. Therefore the ideal output current is 8.333 A RMS. Here we use a resistive virtual impedance, and according to our sign convention, the bus voltage and the output current should have 180° phase difference. Figs. 7 and 8 show the first 10 AC cycles of output voltage and current from startup with the discrete time filter and phasor methods respectively.

Notice that the phasor method overshoots more in both current and voltage than the discrete time method but also shows faster convergence (within 2 AC cycles from cold start) and greater V and P accuracy. This initial simulation result is reflects well toward design objectives 1, 2, 4 and 7 in section II.B; however, concerning design objective 1, the sources simulated use synchronized internal clocks as noted above.

To test the disturbance behavior of our controller (design objectives 5 and 7), we next vary the load resistance in time, and check the voltage droop behavior of our controller. Here we present the phasor based controller, but the discrete filter based controller shows similar performance. Fig. 9 shows 10 AC cycles each of scheduled 1 kW load, interleaved with

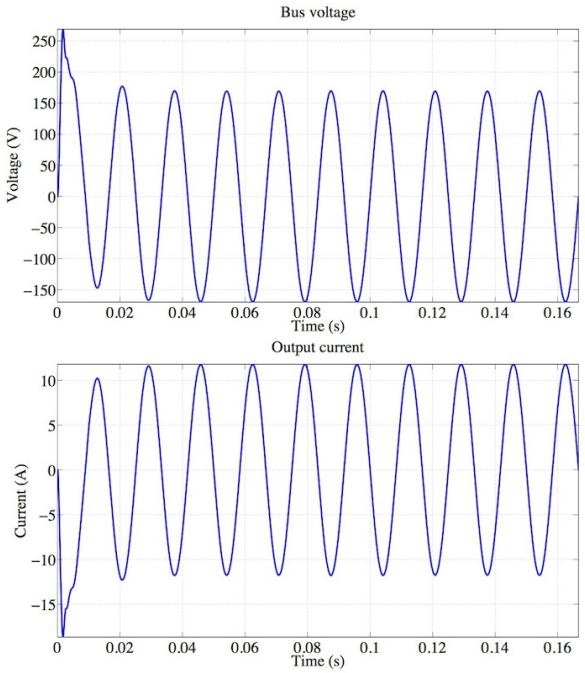

Fig. 8: The output current and the bus voltage from single source single load configuration with the phasor method. $V_{\text{bus}} = 120.1356$ V RMS and $I_{\text{o}} = 8.3445$ A RMS, and $P = 1.013$ kW.

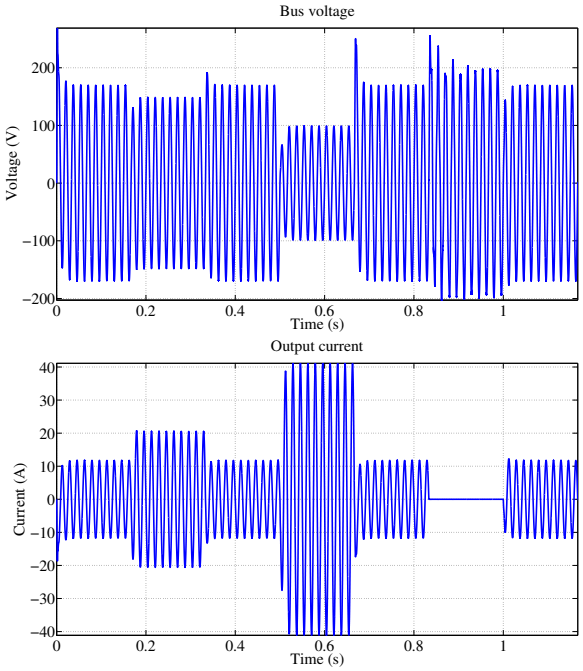

Fig. 9: The output current and the bus voltage from single source time varying load configuration with the phasor method. Note that bus voltage follows expected droop behavior.

10 cycles of 1.5x, 2x and open circuit load. We observe the controller current and voltage converging within 1 AC cycle except in the open circuit condition, wherein the voltage takes about 6 cycles (100 msec).

B. Two sources, one load

To additionally test design objectives 3 and 6, we configure two parallel inverters scheduled to share current in a $4 : 1$ ratio. This is done by assigning appropriate virtual impedances without any special tuning in the controller. Note that, by comparison, PID controllers might require extensive tuning of gain parameters. Fig. 10 shows currents and voltages simulated with the discrete time filter method. The two controllers start cold and stabilize within two AC cycles; as noted in section III; however, each controller's PLL is modeled with a synchronized internal clock, hence this simulation run was not a complete test of design objective 3.

Finally, to simultaneously inform design objectives 1 through 7, we vary the load characteristic in time with the same two parallel inverters to check the transient behavior of our controller. Figs. 11 shows power sharing between two inverters for the same interleaved load variation (1.5x, 2x, 0x) using 10 AC cycles duration for each interval. Here we use the discrete time filter method, but the phasor method shows the similar result. We observe some voltage noise and a small amount of reactive power exchange between the inverters in the short circuit condition; otherwise, the behavior follows the Thévenin source objective.

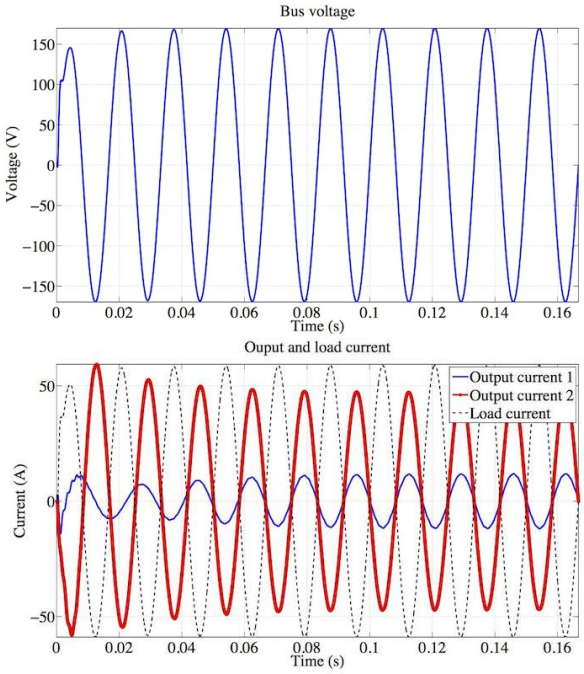

Fig. 10: Output currents and bus voltage from the two source single load configuration with the discrete time filter method.

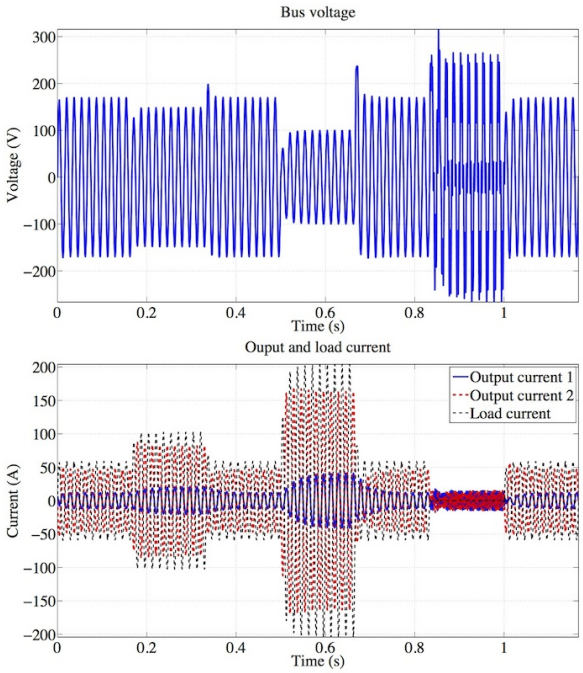

Fig. 11: Output currents and bus voltage from the two source single load configuration with the discrete time filter method.

V. Conclusion and Future Work

In this paper, we adapt the concept of inverter virtual impedance control technique to demonstrate a novel inverter control architecture for microgrids that is compatible with the real and reactive power dispatch schedules produced by an optimal power flow solver. The H-bridge controller tries to follow ideal Thévenin equivalent state space trajectories by solving an optimal control problem within each switching interval. The control design is modularized which helps to incrementally improve the performance of the controller. We tested in simulation the controller's ability to meet seven design objectives formulated specifically for microgrid devices. Preliminary hardware implementation shows that the controller's compute modules can execute within a 100 μsec time interval.

Authors acknowledge that space and time constraints prevented description of our simulations of reactive power. Future work may relax the need for a synchronized time base with PLLs and extend the algorithm for split and three phase inverters. The authors intend to open source the simulation and firmware codes later this year and invite inquiries from interested parties.

Acknowledgement

The authors thank to Matt Wytock for providing an efficient implementation of the least square estimation, and Nicholas Moehle for implementation and helpful discussions.

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