

# Automating Capacitor Part Selection with Dual-Objective Optimization

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**Abstract**—This paper presents a novel framework for optimizing capacitor selection in electronic design using multi-objective linear constrained optimization techniques. We demonstrate the effectiveness of this approach in minimizing cost and board area while meeting critical performance requirements and extend the framework to an economic model of optimal capacitor utilization at the design- or multi-design level.

## I. INTRODUCTION

Multi-layer ceramic capacitors (MLCCs) are essential components in modern electronics, serving critical functions in power, RF, and analog circuits. The rapidly expanding MLCC market [1] offers designers a vast selection of package sizes, voltage ratings, and performance characteristics. However, effectively navigating this complex design space to optimize component selection presents a significant challenge.

Capacitor selection often involves balancing competing objectives: minimizing cost and minimizing board area. These objectives are typically in tension, and traditional manual selection methods may not identify optimal solutions.

While the selection methods in this paper do not completely replace human intervention in all cases, several simple capacitor selection tasks are found to be solvable or provide the human designer an efficient starting-point. The scope of the models presented in this paper include optimization of cost and placement area for the following design settings:

- $C_{\text{eff}}$  (a minimum derated capacitance requirement),
- $|Z_i|$  targets (impedance envelope),
- Combined PDN (power distribution network) model with  $|Z_i|$  targets.

We believe that certain design contexts benefit from the use of each of these formulations. However, the scope of this article is not to rigorously document the potential applications.

## II. SELECTING MLCCs FOR $C_{\text{EFF}}$ REQUIREMENTS

### A. Defining the capacitance constraint

When designing power systems, it's common to encounter specifications that require a minimum effective capacitance  $C_{\text{eff}}$ , as seen in datasheets like [4] and [5]. This value represents the capacitance of a component after accounting for derating, which is a reduction in capacitance due to factors like DC voltage bias. To ensure designs meet these requirements, engineers often keep a database of  $C_{\text{eff}}$  values for various capacitors across different DC bias levels. This allows them to

select a combination of components that meet the necessary capacitance requirement.

The task is to select some mix of capacitors that together have at least  $C_{\text{eff}}$  total derated capacitance. For  $I$  possible capacitor part types, this constraint can be written as:

$$\sum_i^I C_i N_i \geq C_{\text{eff}} \quad (1)$$

where  $N_i \in \mathbb{Z} \quad \forall i$   
and  $N_i \geq 0 \quad \forall i$

where  $C_i$  is the derated capacitance of part  $i$  at the DC bias voltage target and  $N_i$  is the number of part  $i$  in the solution set.

The available parts  $i$  should be pre-filtered by application based on usability in that setting. Common design filters of this type include:

- Maximum part height to avoid interference with other parts in the product,
- Minimum part voltage rating selected to maximize the useful life of the part [2] [3],
- Temperature, voltage and aging stability of capacitance (influencing dielectric material choice),
- Approved manufacturers in the supply chain setting.

### B. Defining our preference model

Beyond the electrical constraints, electronics manufacturers pursue dual minimization objectives: cost and board area of the solution. As volumetric density of capacitance generally increases capacitor cost, we expect the efficient frontier of the feasible region of our optimization to be convex, as shown in Figure 1.

Each dot represents a unique solution to the capacitance constraint (1). Along the Pareto frontier shown, different solutions might be chosen that match the desired trade-offs and goals of the design. For example, a smart watch design might choose a smaller-area design at higher cost than would a server rack design where space is not at a premium.

One approach to formalizing the different preferences applications might have is a simple linear scalarization, where we minimize the objective function:

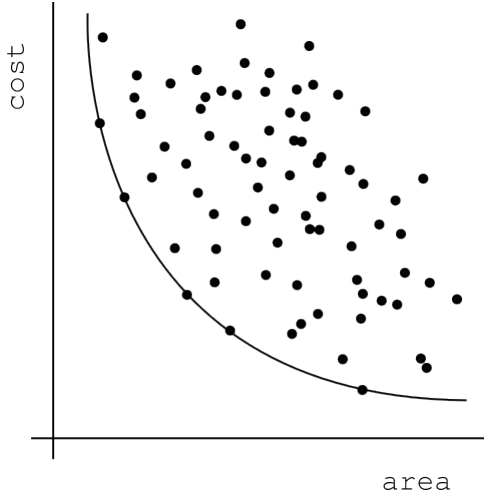


Fig. 1. Simplified expected solution space for capacitor optimization problems with Pareto frontier drawn.

$$\sum_i^I (Ka_i + b_i)N_i \quad (2)$$

where  $a_i$  represents the economic cost - in currency - of capacitor part  $i$  and  $b_i$  represents the capacitor placement area. The value of  $K$  represents the designer's willingness to trade off cost with solution area. It is a fixed value that the designer provides the model. Smaller values of  $K$  should be used in situations where designers are more willing to pay for miniaturization.

Beyond cost and area as objectives for capacitor selection, our objective function could also include weighted operational dimensions which out of the scope of this paper, such as :

- Part sourcing risk,
- Footprint compatibility with possible substitutes (modeled as an option-to-switch value),
- A factor adjusting for the discount of commonizing part selection across applications within the same product.

### C. Solving with examples

Using standard integer-constrained linear optimization methods, we can easily minimize (2) under the constraint of (1). Our decision variables are each  $N_i$ , the number of each type of capacitor part in the solution.

As a thematic example, we will satisfy  $C_{\text{eff}} \geq 4\mu F$  with the following options derated at 3.3V:

Subject to the objective function (2), we can sweep  $K$  to simulate a variety of designer preferences, and calculate an ideal capacitor strategy with a branch-and-bound linear integer optimization solver. The result of this optimization step is seen in table II.

For a graphical representation of this optimization process, see figure 7 at the end of this paper.

TABLE I  
HYPOTHETICAL CAPACITOR OPTIMIZATION OPTIONS

| part # | Description          | $\mu F$ at 3.3V | Cost    | Area $\text{mm}^2$ |
|--------|----------------------|-----------------|---------|--------------------|
| A      | $1\mu F$ 0201 6.3V   | 0.35            | \$0.002 | 0.7                |
| B      | $2.2\mu F$ 0201 6.3V | 0.85            | \$0.003 | 0.7                |
| C      | $1\mu F$ 0201 10V    | 0.45            | \$0.003 | 0.7                |
| D      | $2.2\mu F$ 0201 10V  | 0.95            | \$0.004 | 0.7                |
| E      | $2.2\mu F$ 0402 6.3V | 0.90            | \$0.003 | 1.3                |
| F      | $4.7\mu F$ 0402 6.3V | 1.70            | \$0.007 | 1.3                |
| G      | $2.2\mu F$ 0402 10V  | 1.00            | \$0.005 | 1.3                |
| H      | $4.7\mu F$ 0402 10V  | 1.95            | \$0.008 | 1.3                |

TABLE II  
EXAMPLE CAPACITOR OPTIMIZATION SOLUTIONS BASED ON PREFERENCE

| K     | 0.5 | 1 | 2 |
|-------|-----|---|---|
| $N_A$ | 0   | 0 | 0 |
| $N_B$ | 1   | 3 | 5 |
| $N_C$ | 0   | 0 | 0 |
| $N_D$ | 0   | 0 | 0 |
| $N_E$ | 0   | 0 | 0 |
| $N_F$ | 2   | 1 | 0 |
| $N_G$ | 0   | 0 | 0 |
| $N_H$ | 0   | 0 | 0 |

## III. SELECTING CAPACITORS FOR IMPEDANCE ENVELOPES

### A. Defining the impedance envelope problem

When capacitors are used in filtering applications across wide a frequency spectrum, the *impedance envelope* model is often used for selecting capacitors and simulating power delivery.

The impedance envelope is a function  $Z(f)$  that represents the minimum impedance to ground a port requires. The impedance includes paths through copper, regulator control loops, and passives. Capacitor selection addresses the mid-frequencies of the PDN - between the regulator and PCB layout regions. Impedance envelopes are often derived from voltage range specifications ( $V_{\min}$ ,  $V_{\max}$ ) at power rail loads [6].

Whether selecting capacitors manually or with computer-aided optimization methods, it is a prerequisite task of the designer to isolate the targeted impedance mask region to address with capacitors. Once this is done, the designer can represent the capacitor-region mask into  $M$  discrete terms:

$$|Z|_{f_m} < T_{Z@f_m} \quad (3)$$

for  $m = 1, 2, \dots, M$

The impedance magnitude of the capacitor solution at frequency  $f_n$  must be lower than the target impedance mask value  $T_{Z@f_m}$  for all  $n$  discrete impedance mask points.

Ignoring the real effects of resonance, as is typically done in the manual capacitor selection phase of design, we can leverage the following relationship between parallel capacitors:

$$\frac{1}{|Z|_{f_m}} \approx \sum_i^I \frac{N_i}{|Z|_{i@f_m}} \quad (4)$$

for  $m = 1, 2, \dots, M$

The approximation (4) combines the parallel impedances at  $f_m$  of the solution set into a single effective impedance at  $f_m$ . Although this sets us up to solve the same kind of optimization problem as in section I, notice that (4) is non-linear, so it cannot be used directly.

Instead, we will use *admittance* - the reciprocal of impedance - in order to solve the system with fast linear methods:

$$|Y|_{f_m} > T_{Y@f_m}, \quad (5)$$

for  $m = 1, 2, \dots, M$

$$|Y|_{f_m} \approx \sum_i^I N_i |Y|_{i@f_m} \quad (6)$$

for  $m = 1, 2, \dots, M$

With (5) and (6), we add  $M$  more constraint inequalities to our linear system, but we can solve it identically, optimizing for a weighted scalar objective function trading off cost and area.

### B. Summarizing a mixed impedance envelope and $C_{\text{eff}}$ linear model

A common challenge faced by electronic designers involves selection of capacitors on a power rail subject to the minimum derated capacitance requirement of a voltage regulator and an impedance envelope demanded by the power rail's load(s).

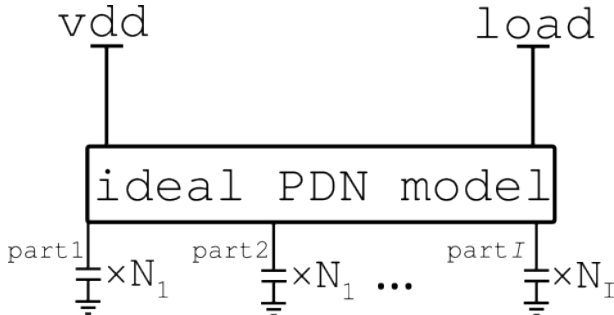


Fig. 2. Regulator-and-load topology with ideal PDN.

We will assume an ideal PDN model, that is, no parasitic impedance from  $vdd$  to  $load$ , or from capacitor to capacitor.

Our optimization problem is formulated as:

$$\begin{aligned} & \text{select } N_i \text{ for } i = 1, 2, \dots, I \\ & \text{in order to minimize } \sum_i^I (K a_i + b_i) N_i, \\ & \text{subject to} \\ & \sum_i^I C_i N_i \geq C_{\text{eff}} \text{ and} \\ & \sum_i^I N_i |Y|_{i@f_m} > T_{Y@f_m} \text{ for } m = 1, 2, \dots, M \end{aligned} \quad (7)$$

The simple, idealized model of (7) will produce results for  $N_i$  which can inform the electronic designer's capacitor selection strategy.

### C. Mixed impedance envelope capacitor selection example

As a stylistic example, we will consider a capacitor selection challenge with the following constraints:

$$\begin{aligned} & \text{Select } N_i \text{ for } i = 1, 2, \dots, I \\ & \text{in order to minimize } \sum_i^I (K a_i + b_i) N_i, \\ & \text{subject to the constraints:} \\ & \sum_i^I C_i N_i \geq 12 \mu\text{F at } V=1.15 \text{ Volts,} \\ & \sum_i^I N_i |Y|_{i@100\text{KHz}} > \frac{1}{0.1\Omega}, \\ & \sum_i^I N_i |Y|_{i@1\text{MHz}} > \frac{1}{0.01\Omega}, \\ & \sum_i^I N_i |Y|_{i@10\text{MHz}} > \frac{1}{0.005\Omega}, \\ & \sum_i^I N_i |Y|_{i@100\text{Mhz}} > \frac{1}{0.01\Omega}, \\ & \sum_i^I N_i |Y|_{i@1\text{GHz}} > \frac{1}{0.1\Omega} \end{aligned} \quad (8)$$

With a library of  $I =$  several hundred available parts, we can solve this linear optimization problem for a given  $K$  in under 10 milliseconds with standard linear solvers.

By sweeping  $K$  in 40 log-spaced steps between 0.01 and 100, we can generate a number of efficient solutions which can be plotted in cost, area 2D space as an efficient frontier:

Each of the red dots in Figure 3 is a unique solution  $N_i$  for  $i = 1, 2, \dots, I$ . The solutions shown range from having 2 to 5 unique capacitor parts included ( $N_i > 0$  for 2 to 5 unique  $i$ ), and up to 14 total parts ( $\sum_i^I N_i \geq 14$ ). From our experience, most generated solutions are unlikely to be found by human search.

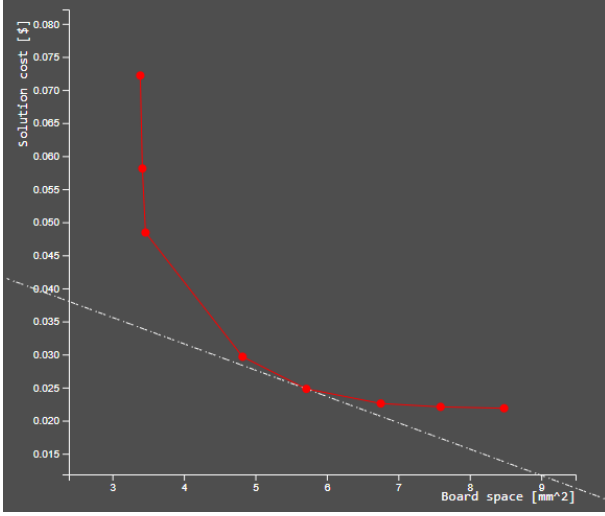


Fig. 3. Efficient frontier solutions found for the optimization problem 8 using a real reference part library. The tangency line for  $K = 2.51$  (the designer is willing to save a penny by increasing solution size by 2.51 square millimeters).

Since the solutions are generated so quickly, designers can easily run ad-hoc studies analyzing the cost (in cents and board space) to a solution by doing the following and re-running the optimization:

- adding a new part to the database,
- restricting the maximum height of the solution,
- modifying the preference between cost and board space ( $K$ ).

While this process greatly automates the search for solutions, each solution must be validated with real resonance and PDN modelling.

#### D. Adding a simple non-ideality to the PDN model

Our model in the above section will optimize the selection set within an unrealistic assumption of an ideal PDN. The physical layout of the product's conductors will define the impedance of our PDN. Given a mature design, we can simulate all of the relevant port-to-port PDN impedances with numerical methods, as is standard in the industry.

Early in the product development stage, we may choose to implement a crude approximation of our PDN. In modern electronics, capacitors are often placed on the side of the PCB opposite the load port, making the capacitor placement-to-load impedance dominated by the series impedance of the via structure between them.

In the above schematic, we will use the  $Z_m$  values to pre-transform the individual part's effective impedances:

$$|Z|_{i@f_m}^* = |Z|_{i@f_m} + Z_m \quad \text{for } m = 1, 2, \dots, M \quad (9)$$

We will also pre-transform the load impedance targets:

$$T_{Z@f_m}^* = T_{Z@f_m} - Z_L \quad \text{for } m = 1, 2, \dots, M \quad (10)$$

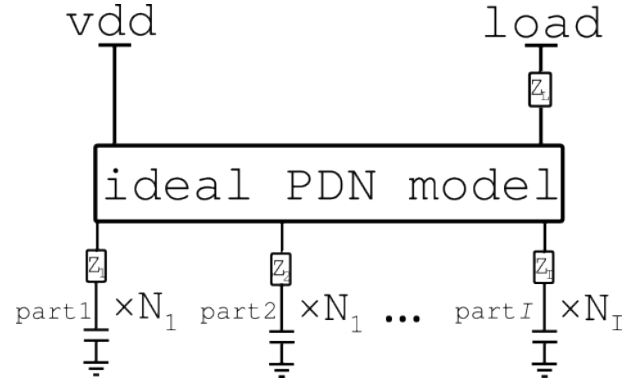


Fig. 4. Regulator-and-load topology with capacitor and load series impedance.

We observe that if  $Z_L > T_{Z@f_m}$ , the solution becomes infeasible, as expected. Re-solving the linear optimization problem with  $T_{Z@f_m}^*$  and  $|Z|_{i@f_m}^*$ , we achieve a capacitor selection set that is constrained by a more realistic set of PDN targets without introducing any non-linearity into the model.

## IV. SELECTING CAPACITORS WITHIN MORE ROBUST PDN MODELS

### A. Basic placement location-informed optimization models

Further elaborating on our ideal PDN model, we can model a parasitic impedance  $Z_{jk}$  between candidate placement locations  $j$  and  $k$ . Having introduced placement locations into our model, it is useful to also specify impedance spec requirements per location, as would be the case for a regulator with multiple loads connected by a shared PDN. Each capacitor placement area affects the effective impedance at every other location's load as well as its own.

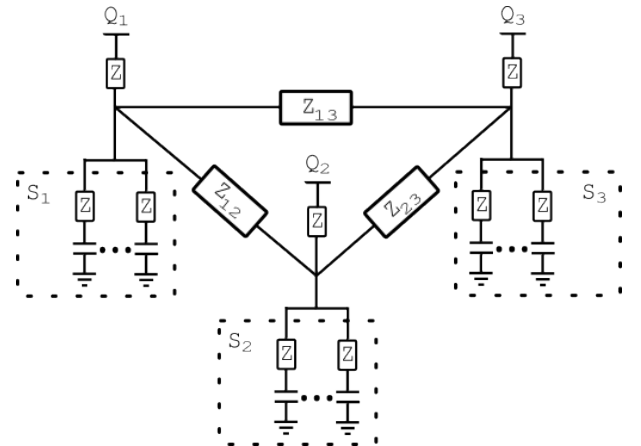


Fig. 5. Placement-location selection problem schematic.

In general, we can think of  $J$  possible locations for capacitor placement. Each spec location  $Q_j$  in the diagram has its own impedance envelope requirement:

$$\begin{aligned}
&|Z|_{f_m @ j} < T_{Z @ f_m @ j} \\
&\text{for } m = 1, 2, \dots, M \\
&\text{for } j = 1, 2, \dots, J
\end{aligned} \tag{11}$$

Opportunities for capacitor placement with no corresponding local impedance mask requirement can be modeled with an infinite impedance mask. This tactic can be used when considering placement of capacitors in a region of the PCB central to several loads or distant from any load in particular.

Our number of decision variables gets multiplied by the number of candidate placement areas. We now have  $I \times J$  decision variables, each notated  $N_{ij}$ .

In product design, though each capacitor costs the same (economically speaking) per location, we may value the placement area more dearly in one location than the other. For this reason, we can model our objective to minimize function as

$$\sum_j \sum_i (K_j a_i + b_i) N_{ij} \tag{12}$$

where the designer assigns the values of  $K_1, K_2, \dots, K_J$  according to the relative cost of placement area in that location. For instance, a relatively congested placement area  $j$  will have a relatively small  $K_j$ .

For the following modelling, we will assume the pre-transformations of section III.D have already been made. By solving the impedance circuit, we can model our impedance envelope constraints as:

$$\begin{aligned}
&|Y|_{f_m @ j} > T_{Y @ f_m @ j} \\
&\text{for } m = 1, 2, \dots, M \\
&\text{for } j = 1, 2, \dots, J
\end{aligned}$$

$$\text{where } |Y|_{f_m @ j} = \sum_i N_{ij} Y_{i @ f_m} + \sum_{k \neq j} \frac{1}{\frac{1}{Y_{jk}} + \frac{1}{\sum_i N_{ik} Y_{i @ f_m}}} \tag{13}$$

This does not seem to us to be linearizable, either in impedance or admittance forms. We are left with a mixed-integer non-linear (smooth) programming task (MINLP).

Solving this optimization problem with available open source solvers such as gekko [7] yields promising solutions that automatically trade off designer placement preferences with cost and area of the solution.

#### B. Expanding the design search space to include PDN impedances

Equation (13) as described has the decision variable formulation:

$$\text{select } N_{ij} \quad \forall i, j \quad \text{where } i \neq j \tag{14}$$

However, we can trivially expand our selection space to also include:

$$\text{select } Y_{ij} \quad \forall i, j \quad \text{where } i \neq j \tag{15}$$

In this more complicated formulation, the optimization model selects admittances between capacitor placement areas. Beyond the selection space expansion, we must make a corresponding constraint and objective function formulation.

In our PDN design, the admittance between ports will be a function of the copper geometry between the ports, including proximity to return planes. Heuristically, we may simplify the issue to:

$$Y_{ij} = f(D_{ij}, W_{ij}) \tag{16}$$

where  $D_{ij}$  is the distance between ports (fixed with respect to the model), and  $W_{ij}$  is the copper width of the run of copper between ports. The implementation of the function  $f$  is left for further work, but should account for factors of the design such as the PCB stackup. Especially at higher frequencies the admittance will depend on more complicated geometric interactions that cannot be modeled in such a simple optimization model.

In this formulation, we depend on the designer to assign preference  $L_{ij}$  weights to each  $W_{ij}$  relative to  $K$  in equation (17) in order to scalarize it, making the new objective function:

$$\sum_j \sum_i ((K_j a_i + b_i) N_{ij} + L_{ij} W_{ij}) \tag{17}$$

#### V. QUANTITATIVE PART DEMAND EXERCISE

Electronic designers often need to evaluate MLCC suppliers' part offerings for potential to use in their designs. By scaling the methodology presented in this paper to an entire design, we can precisely determine our quantity demanded for a part at a given price, or our *capacitor demand curve* for an entire design or multiple designs.

Suppose we have  $P$  circuit applications, each with an efficient solution vector  $N_p$  for each circuit. Our demand curve for a part  $i$  can be written as:

$$Q(C_i) = \sum_p N_{pi} \tag{18}$$

where  $N_{pi}$  is the number of capacitors of part  $i$  used in application  $p$  when its cost is  $C_i$ . The shape of  $Q(C_i)$  must be weakly decreasing. Since the demand curve is a series of sums of optimization results, we can understand it as encoding important information about the opportunity cost of this part relative to others in our database.

We can use the generated demand curve in several ways:

- By finding the intersection with our supply curve (e.g. volume discount), we can determine the optimal quantity of the part used.
- Knowing the x-intercept of the demand curve, we can quickly eliminate certain parts based on their suppliers' quoted price.

- By calculating the area under the demand curve and above the price, we can estimate the whole-device cost savings by introducing a new part. This savings accurately accounts for the opportunity cost of the part swaps.

Figure 6 illustrates the supply and demand model for a single part  $i$  within an electronic design. It shows how the generated demand curve for a part can be used to find the intersection with the supply curve the firm faces (which may include volume discounts) to determine the optimal quantity of the part to be used. The graph also depicts the unit price at this optimal usage level.

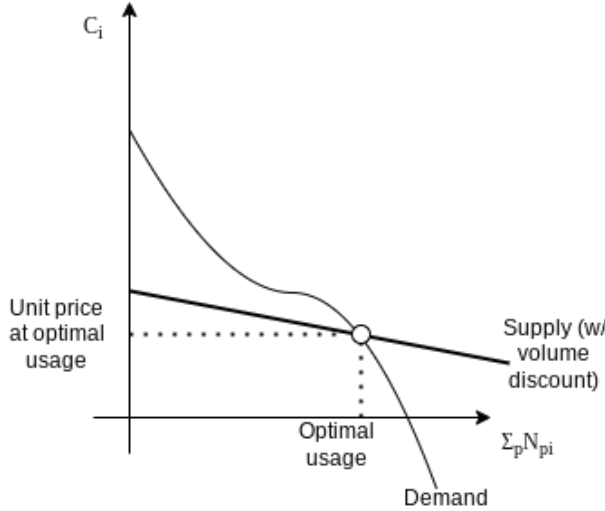


Fig. 6. Supply and demand model for a single part  $i$  within an electronic design.

## VI. DISCUSSION

We have presented a spectrum of optimization frameworks, from simple linear  $C_{\text{eff}}$  optimization to non-linear triple-objective models with geometric placement area considerations. For each framework presented, we have commented on the usefulness and accuracy of the selection methods, with the simplest models being the most useful in the current state of the art, and the more complicated models needing more future investment to become useful.

We believe there is immense opportunity to leverage these models to economize and efficiently pack capacitors in electronic designs. The quality of the model's output is not dependant on the human designer's selection intuition, but rather on the accuracy of a part library database and the appropriate electrical constraints.

In future works, we hope to examine the appropriateness of the heuristics (4) and (16) in a wide range of applications. We also hope to integrate capacitor selection models into larger auto-designing workflows.

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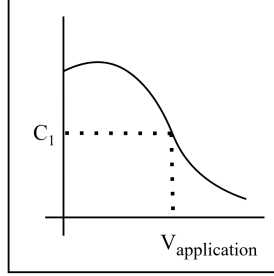
## Setup

Filter entire library of capacitors to  $I$  options based on physical and electrical suitability in the application.

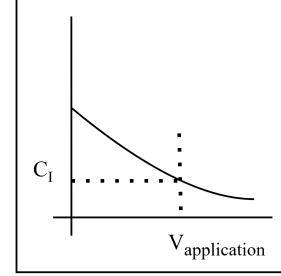
Database of all capacitors.



Get  $C_i$ , the derated capacitance at the application voltage for each candidate part type.



...



Find the unit cost  $a_i$  of each part type.

$[a_1, \dots, a_I]$

Find the board area consumed  $b_i$  by each part type.

$[b_1, \dots, b_I]$



## Optimization

Select all  $N_i$ , the number of capacitors of type  $i$  to use in the solution, which minimize the objective function.

$[N_1, \dots, N_I]$

Objective function where designer selects an appropriate  $K$ . Solve as a standard linear optimization problem

$$\text{minimize} \quad \sum_i^I (K a_i + b_i) N_i$$

Apply a  $C_{\text{eff}}$ , minimum effective derated capacitance, constraint for the application.

$$\text{where} \quad \sum_i^I C_i N_i \geq C_{\text{eff}}$$

Fig. 7. The optimization process for  $C_{\text{eff}}$  optimization.