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Influence of Dielectric and Active layer Thickness on MgZnO Thin Film Transistor Electrical Characteristics

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Abstract

From last decades, Thin Film Transistors Technology uses low-k dielectric material as an insulator. Insulator thickness plays an important role in device dimension. The insulating layer also known as the gate oxide separates the gate electrode from the channel region of the transistor. If the insulating layer is too thin, there is a greater chance that electrons can tunnel through the oxide layer, leading to leakage current. To mitigate this issue, various techniques are used such as the introduction of high-k dielectrics, which have a higher dielectric constant, allowing for thicker insulating layers to be used while maintaining the same capacitance. To gain better transistor characteristics without reducing oxide thickness use high-k dielectric instead of SiO_2 to reduce leakage current and improve gate oxide capacitance. In this work the electrical performances of the $Mg_xZn_{1-x}O$ Thin film transistors are analyzed and compared. Mg is a high direct bandgap (7.7 eV) material that alter the electrical and optical properties of a transistor. $Mg_xZn_{1-x}O$ (20% of Mg and 80% of ZnO) Thin film transistor's electrical characteristics with different dielectric materials and variations in channel thickness is measured. First variation with different insulator e.g., $SiO_2(K \sim 3.9)$, $Si_3N_4(K \sim 7.9)$, $Al_2O_3(K \sim 9)$, and $HfO_2(K \sim 25)$ dielectrics are done. Then thickness of the active layer is varied as 30 nm, 50 nm, and 70 nm for all the four dielectric materials. Drain characteristics and transfer characteristics are good for 30 nm active layer thickness along with HfO_2 dielectric material. The optimized threshold voltage, subthreshold slope, mobility, and I_{ON}/I_{OFF} ratio are 0.66 V, 0.067 V/decade, 6.44 $cm^2/V.s$, and 10^9 respectively are obtained after simulating the $Mg_{0.2}Zn_{0.8}O$ Thin Film Transistor on TCAD tool. Due to high I_{ON}/I_{OFF} ratio low threshold voltage and good mobility this type of thin film transistor finds its viability in display devices, photodetectors, etc.

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Keywords: Thin film transistor, Mg, ZnO, Active layer

INTRODUCTION

Thin film transistors (TFT's) based on metal oxide semiconductor ZnO has a significant role in transparent electronics, photonics, optoelectronics, spintronics, and gas sensors applications [1]. ZnO having a wide bandgap material of 3.34 eV with a hexagonal wurtzite structure and has a large excitation binding energy of 60 meV [2]. Bandgap greater than 3.1 eV provides visible transparency. Metal oxide semiconductor (ZnO) with bandgap 3.34 eV and it provides optical transmittance

greater than 85% in the visible region so that it is useful for UV photodetector [3]. For transparent electronic applications ZnO based TFT's are considered as the most promising semiconductor material. Traditionally, hydrogenated amorphous silicon (a-Si:H) is used as the base TFT material owing to its advantages of simple developing procedure and deposition parameters. But, its use is restricted in the TFT applications due to its lower mobility values (eff < 1 $cm^2/V\ s$) as it suffers low switching speed which is the foremost requirement for TFT displays. Therefore, tunable bandgap from 3.37 eV to 7.8 eV and improved electrical characteristics can be obtained by using composition of Mg into ZnO, so that it can also be useful for UV photodetector [4]. The lower standard electrode potential (SEP) for Mg is -2.37 E°, and for Zn is -0.76 E°. Mg could be more easily oxidized than ZnO because Mg-O bond does not easily loose the oxygen vacancies. Mg might be a better option to suppress the oxygen vacancy in the zinc oxide active layer. Due to similar ionic radii (Zn^{2+}: 0.60 Å and Mg^{2+}: 0.57Å), results show that there is not large lattice distortion when Mg^{2+} substitution in the Zn^{2+} site [5]. Due to composition of Mg in ZnO to form the Mg_xZn_{1-x} has enhanced the thermal and electrical properties of ZnO based thin film transistors [4]. Mg and its doping in TFTs is used as a dielectric layer, buffer layer, and active channel layer [6].

Highlights

- Transfer characteristics of TFT with different dielectric material studied.
- Output characteristics of TFT with different dielectric material with varying gate voltage studied.
- Transfer characteristics of TFT with variation in active layer thickness studied.
- Output characteristics of TFT with variation in active layer thickness studied.
- Transfer and output characteristics of TFT with optimum parameter studied.

Active layer crystal quality is also affected by the presence of Al_2O_3 insulating layer. The effect is was analyzed by Wang et al. [7].

TFT The photo-electrical properties investigation reported using high-K dielectric in $Mg_xZn_{1-x}O$ TFT by Jyun -Yi Li. et al. [8].

The main objective of this work is to analyze the effect of the insulator and thickness of the active layer on the electrical performance of $Mg_{0.2}Zn_{0.8}O$ TFT. In this paper an bottom gate top contact $Mg_{0.2}Zn_{0.8}O$ TFT is designed and compared the electrical characteristics. Results measured for different insulators SiO_2(K ~ 3.9), Si_3N_4(K ~ 7.9), Al_2O_3(K ~ 9), and HfO_2(K ~ 25) [9] along with variation in active layer thickness as 30 nm, 50 nm, 70 nm of a TFT is done. Generally, the silicon dioxide (SiO_2) dielectric has used a gate oxide material in TFT. Thin-film transistors size can be reduced by decreasing the thickness of SiO_2 which increases the oxide capacitance. But the reduction in the thickness of dielectric causes an increase in the leakage current, thus, result in high power consumption. Therefore, an alternative that is high-K dielectric can be used which reduces the leakage current and low power consumption without decreasing the thickness of the dielectric. This means replacing the low dielectric constant with the high-K dielectric constant can solve this issue [10].

In section 2 the modelling parameter required for TFT's electrical characteristics are explained. Simulation parameter for measuring the electrical characteristics for TFT are discussed in section 3. Section 4 is based on the analysis of results. The electrical performance of TFT is measured in terms of threshold voltage (V), SS(V/dec), mobility (cm^2/V. s), and I_{ON}/I_{OFF} ratio.

MODELING FOR DIELECTRIC AND TFT'S ELECTRICAL CHARACTERISTICS

From last decades, Thin Film Transistors Technology used SiO_2 as insulator. Thin film Transistors electrical performance depends on various parameter like, insulator material, insulator thickness, active layer thickness, channel length, W/L ration and many more. The insulating layer also known as

the gate oxide separates the gate electrode from the channel region of the transistor. If the insulating layer is too thin, there is a greater chance that electrons can tunnel through the oxide layer, leading to leakage current. To mitigate this issue, various techniques are used such as the introduction of high-k dielectrics, which have a higher dielectric constant, allowing for thicker insulating layers to be used while maintaining the same capacitance. To analyze transistor electrical performance without reducing oxide thickness use high-k dielectric instead of SiO_2 to reduce leakage current and improve gate oxide capacitance. The oxide capacitance is denoted as

$$C_{ox} = \frac{K_{ox}\varepsilon A}{T_{ox}} \tag{1}$$

Where K_{ox} is insulator material constant, relative permittivity in Vacuum is denoted as ε, A is channel area means product of L(length) and W(width) of TFT and T_{ox} is the thickness of dielectric [10]. The oxide capacitance of gate given in Eq. (1) can also be written as

$$C_{ox} = \frac{\varepsilon_{ox} LW}{T_{ox}} \tag{2}$$

Where $\frac{\varepsilon_{ox}}{T_{ox}}$ denote per unit area capacitance

$$C_{ox} = (C_{ox})_U LW \tag{3}$$

Where U=per unit area capacitance, replacing with a high-K dielectric to increase the per-unit area capacitance so the overall capacitance is increased. Thus, the drain current also increases.

$$\boldsymbol{C_{K_{ox\_high}}} = \frac{\boldsymbol{K_{ox\_high}\varepsilon A}}{\boldsymbol{T_{K_{ox\_high}}}} \tag{4}$$

Eq.(4) can be written as

$$C_{K_{ox\_high}} = \frac{K_{ox\_high}\varepsilon LW}{T_{K_{ox\_high}}} \tag{5}$$

Where $\boldsymbol{K_{ox\_high}}$ is dielectric constant of high-k dielectric material. Where $\frac{\boldsymbol{\varepsilon_{K_{ox\_high}}}}{\boldsymbol{T_{K_{ox\_high}}}}$ denote per unit area capacitance.

$$C_{K_{ox\_high}} = ((C_{K_{ox\_high}})_U LW) \tag{6}$$

Where $C_{K_{ox\_high}}$ is the capacitance of high-K dielectric. Replacing C_{ox} with $C_{K_{ox\_high}}$ increases the capacitance per unit area therefore, overall capacitance is increases. Hence drain current also increases. The drain current (I_D) of the TFT under different operating region-linear and saturation regions is obtained using Eqns. (7) and (8).

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{7}$$

Where $V_{DS} < V_{GS} - V_T$ (linear region) and

$$I_D = \mu_n C_{ox} \frac{W}{2L}[(V_{GS} - V_T)^2] \tag{8}$$

for $V_{DS} \geq V_{GS} - V_T$ (saturation region)

In this equation μ_n represent the mobility, C_{ox}, V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage, W represent channel width and L represent channel length [11]. The threshold voltage V_T is obtained by fitting a straight line to the square root of the I_D versus V_{GS} curve.

The drain current (I_D) of the device for high-K dielectric is

$$I_D = \mu_n C_{K_{ox\_high}} \frac{W}{2L}[(V_{GS} - V_T)^2] \quad (9)$$

μ_n (field effect mobility) can be obtained by taking slope of the square root of drain current [12].

$$Slope = \frac{d\sqrt{I_D}}{dV_{Gs}} \quad (10)$$

The Eq. for slope is modified by putting the value of Eq. (8) in Eqns. (10) and is defined as Eq. (11).

$$Slope = \left(\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\right)^{\frac{1}{2}} \quad (11)$$

The mobility μ_n can be obtained by using Eq. (12).

$$\mu_n = \frac{(slope)^2 2L}{C_{ox}W} \quad (12)$$

Subthreshold slope indicates how fast switching operation takes place from off state to above threshold regime. Subthreshold slope (SS) value should be less than 1 for fast switching operation.

$$SS = \frac{dV_{GS}}{d(\log I_D)} \quad (13)$$

I_{ON}/I_{OFF} ratio determined through the transfer characteristics by taking maximum to minimum current of the device.

The study combines the carrier transport equation, continuity equation, and Poisson's equation. The equation use the drift diffusion (DD) model to calculate results, which is a conventional model of carrier transportation. There are other alternative models such as Hydrodynamics (HD) and Energy valence (EV) in the TCAD library. To determine carrier distribution and mobility, the study uses the Fermi-Dirac statistics model along with a field-dependent mobility model. The Fermi-Dirac statistics model is used to describe the behavior of electrons and holes in a semiconductor at thermal equilibrium, while the field-dependent mobility model accounts for the dependence of mobility on the electric field strength [13].

DESIGN AND SIMULATION PARAMETER FOR TFT

TFT are electronics devices used in displays, sensors and other applications that require control of electrical signal. The structure of TFT can be classified into two categories: Staggered architecture and Coplanar architecture. Staggered architecture refers to the placement of source electrode/drain electrode and insulator layer located at the opposite side of channel, while coplanar architecture refers to their placement on the same side of the channel. The TFT structure proposed in this paper is an inverted staggered bottom gate, which means that the gate electrode is placed at the bottom and the source/drain electrodes are located on opposite side of the channel from the gate electrode and channel layer. This structure requires fewer fabrication steps and reduces access resistance due to the active semiconductor layer [14]. The active layer used in the proposed structure is a composition of 20% Mg and 80% ZnO. The substrate used is n-type Si, and to form a gate contact, position of Aluminum is selected at the back side of Si substrate. Insulator layers such as SiO_2, Si_3N_4, Al_2O_3, and HfO_2 are placed upon the Si substrate, followed by the $Mg_{0.2}Zn_{0.8}O$ active channel layer with varying thicknesses of 30 nm, 50 nm, and 70 nm. Finally Al is placed on active layer for obtaining top contact from source and drain. The electrical characteristics of the TFT with different active layer thicknesses are compared to study their performance.

Electrical parameters such as drain current, I_{ON}/I_{OFF} ratio, threshold voltage, sub-threshold slope, and field-effect mobility have been obtained, under the variation of dielectric material and channel thickness. The electronic parameters of MgZnO required for the simulation purpose is taken from TCAD inbuilt library which is mentioned in Table 1.

Table 1. Material parameter assumed for simulation of $Mg_{0.2}Zn_{0.8}O$ TFT [15]

Parmeter	Value
Bandgap, E_g (300)	3.93 eV
Affinity, ζ	3.8 ev
Dielectric Constant, ∈	8.49
Electron Mobility, m_n	16 cm^2/V.s
Hole Mobility, m_p	4 cm^2/V.s
Effective density of states in the conduction band, Nc	1.76×10^{19} cm^{-3}
Carrier life time (s)	9×10^{-9}s

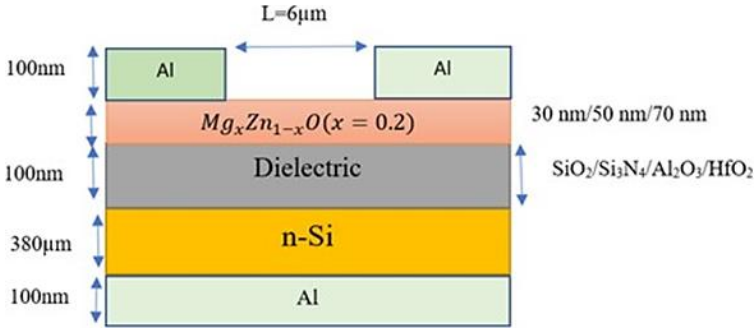


Figure 1. Bottom gate Top contact $Mg_{0.2}Zn_{0.8}O$ TFT structure

RESULT AND DISCUSSION

The transfer and drain characteristics of designed TFT is analyzed for different insulator and active layer thickness variation i.e.,30 nm, 50 nm, 70 nm with constant channel length (L) = 6 µm, and Width (W) = 30 µm. In Figure 2(a) shows transfer characteristics of TFT with different insulator material and different channel thickness at constant drain to source voltage (VDS) of 2V. From Figure 2(a), it is observed that raise in drain current with an increase in dielectric constant from SiO2(K ~ 3.9), Si_3N_4(K ~ 7.9), Al_2O_3(K ~ 9), and HfO_2(K ~ 25). Therefore, while the relative permittivity of the insulator plays an important role in determining the performance of a transistors. It affects the overall operation of the transistors by influencing the threshold voltage and on-state current. The higher the dielectric constant of the insulator, the drain current is increasing [10]. This behavior can be explained by Eqns.(4) and Eqns. (9) because due to high-k dielectric material overall gate oxide capacitance increases hence drain current increases. From Figure 2(b) it is analyzed that increase in drain current with decreases in active layer thickness from 70 nm, 50 nm and 30 nm. As the $Mg_{0.2}Zn_{0.8}O$ thickness increases the electrical parameter change as a result of high resistivities due to increased thickness and long path from source to drain formed. Further an increase in thickness, the Mg content increases thus the probability of an increase in interstitial scattering defects so Mg becomes an impurity scattering center when carries pass through. It can increase the effective mass of the carrier and hence mobility is reduced [4]. Extraction of threshold voltage can be calculated by a linear fit on the square root of the drain current characteristics. The threshold voltage (V_T) is obtained by fitting a straight line to the square root of the I_D versus V_{GS} curve from Figure 2 (a).

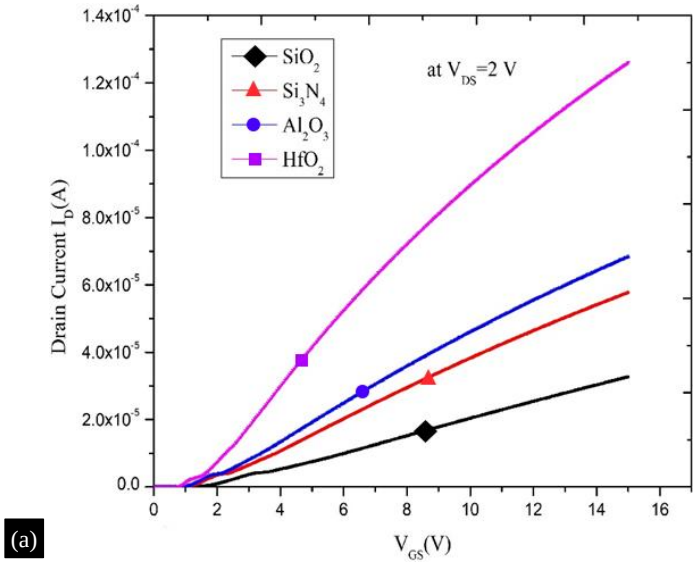
Hence, the devices with 30 nm as an active layer with HfO_2 dielectric obtain the best electrical performance, with field effect mobilities of 6.44 $cm^2/V.s$, threshold voltage(V_T) of 0.66 V, subthreshold slope (SS) of 0.067 V/dec, and an I_{ON}/I_{OFF} ratio of 10^9.

Figure 3 shows the drain characteristics using different dielectrics such as SiO_2(K ~ 3.9), Si_3N_4(K ~ 7.9), Al_2O_3(K ~ 9), and HfO_2(K ~ 25). From these characteristics it is noticed that drain current (I_D) increases with increase in V_{DS} for all dielectrics. This demonstrates that the inverted staggered bottom gate TFT operates in enhancement mode, which enhances its electrical properties.

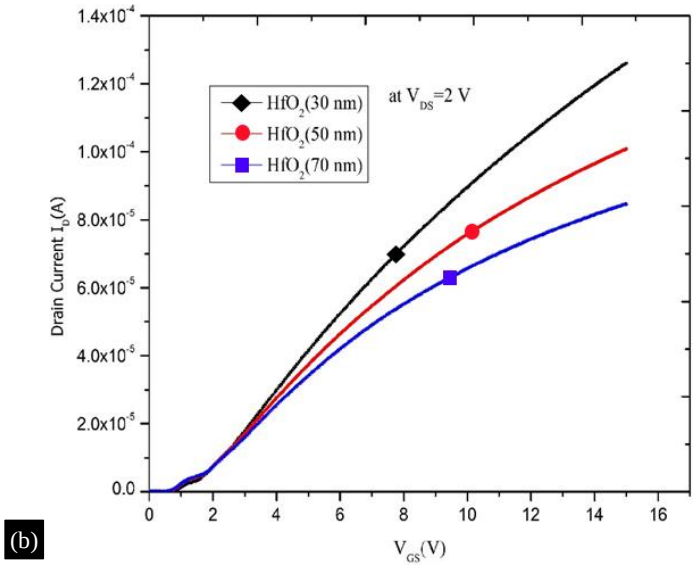
Figure 4(a) and (b) represent the transfer and drain characteristics of high-K dielectric (HfO_2) ($K \sim 25$) at different drain and gate voltage. Characteristics show transistors operating in the enhancement mode The results of the drain current (I_D) obtained using simulation and the calculated values using Eqs. (7) and (8) are comparable to each other.

Table 2 illustrates that the high-K dielectric lowers the threshold voltage by 21.92% for SiO_2 to Si_3N_4, 6.74% for Si_3N_4 to Al_2O_3 and 20.48% Al_2O_3 to HfO_2 respectively as dielectric material, and higher I_{ON}/I_{OFF} ratio and lower SS.

From the results shown in Table 3 that the mobility increases when increases in channel thickness from 30 nm to 50 nm, but there is decrement in the mobility when the channel thickness is reached to 70 nm. This is due to the Mg content increases thus the probability of an increase in interstitial scattering defects so Mg becomes an impurity scattering center when carries passes through. It can increase the effective mass of the carrier and hence mobility is reduced [4]. Thus 30 nm channel thickness is selected for achieving high ratio I_{ON}/I_{OFF} which is required for fast switching applications.



(a)



(b)

Figure 2. (a)Transfer characteristics of TFT with different dielectric at V_{DS} = 2 V (b) Transfer characteristics for 30 nm, 50 nm, 70 nm channel thickness using HfO_2 at V_{DS} = 2 V.

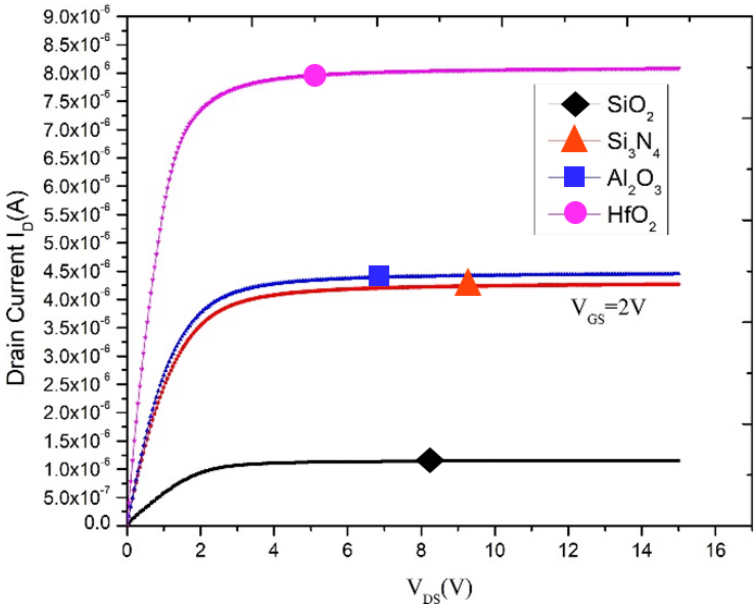
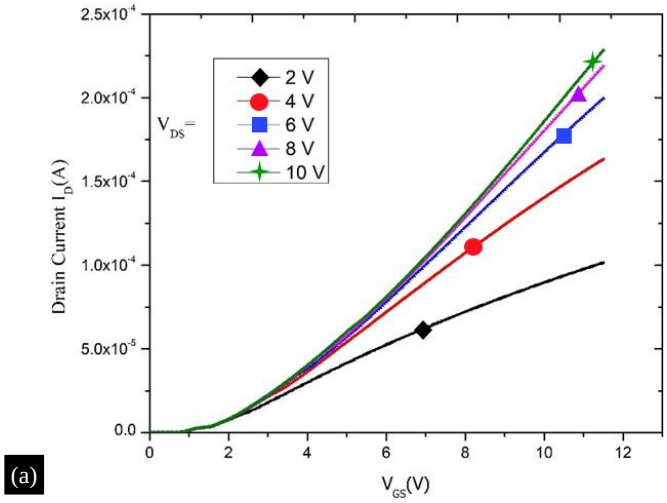
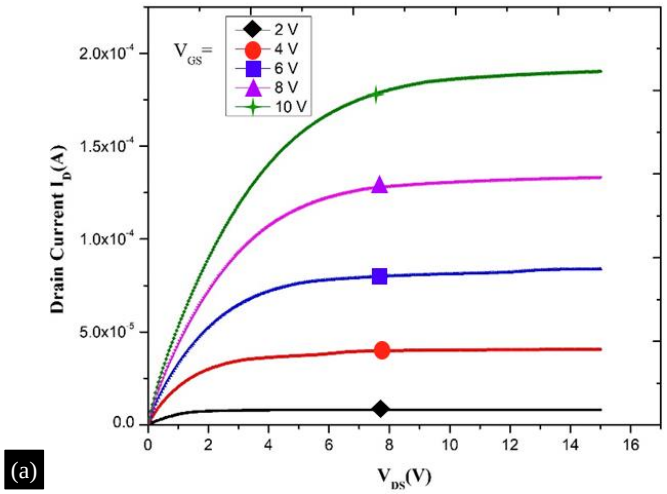


Figure 3. Drain characteristics for various dielectric at V_{GS} = 2 *V*.



(a)



(a)

Figure 4. (a) and (b) shows Transfer and drain characteristics at V_{DS}= 2 V to 10 V and V_{GS} = 2 V to 10 V of HfO_2 with 30 nm thickness of active layer.

Table 2. Results of $Mg_{0.2}Zn_{0.8}O$ TFT with different dielectric

Dielectric	V_T (V)	SS (V/dec)	Mobility (μ_n)cm^2/V.s	I_{ON}/I_{OFF}
SiO_2 (K ~ 3.9)	1.14	0.2066	0.732739	10^5
Si_3N_4 (K ~ 7)	0.89	0.0800	2.13131	10^7
Al_2O_3 (K ~ 9)	0.83	0.0739	2.81287	10^8
Hf O_2 (K ~ 25)	0.66	0.0671	6.44477	10^9

Table 3. Results of TFT using *Hf* O_2 dielectric with various thickness

Parameter	30 nm	50 nm	70 nm
Threshold voltage (V)	0.66	0.55	0.45
SS(V/dec)	0.067	0.068	0.070
Mobility(μ_n) $cm^2/V.s$	6.44	6.73	6.22
ION/IOFF	6.40×10^9	1.17×10^9	2.14×10^8

Table 4. Comparison of results with already reported results

Reference [ ]	V_T (V)	SS (V/dec)	Mobility (μ_n)$cm^2/V.s$	I_{ON}/I_{OFF}
H. Q. Huang et al. [6]	27.6	*NR	1.85	10^6
ChangPeng Wang et al. [7]	0.70	0.138	6.70	10^6
Jyun-Yi Li et al. [8]	4.2	0.29	7.73	1.2×10^7
Jyun-Yi Li et al. [4]	3.1	0.80	5.65	10^5
J. S. Wrench et al. [16]	7.1	*NR	4	1.6×10^6
This Work	**0.66**	**0.067**	**6.44**	**10^9**

A comparison of the proposed $Mg_{0.2}Zn_{0.8}O$ based TFT structure with other reported structures having electrical performance is referenced in Table 4. In all reported results effects of different dielectric, variation in thickness of active channel layer, buffer layer are reported. This work shows lower threshold voltage, lower SS, good saturation mobility, and high I_{ON}/I_{OFF} current ratio with miniaturization of the dimension of the device. As compared to the reported result in literature the proposed TFT, gives a lower threshold voltage and I_{ON}/I_{OFF} ratio is high lower threshold voltage and higher Ion/Ioff ratio which is essential for fast switching devices.

CONCLUSIONS

In this paper, bottom gate top contact $Mg_{0.2}Zn_{0.8}O$ TFT has been simulated has been performed using TCAD simulator. TFT's performance is measured for varying dielectric material ($SiO_2/Si_3N_4/Al_2O_3/HfO_2$) and channel thickness (30 nm/50 nm/70 nm. Various electrical performance parameters like threshold voltage, I_{ON}/I_{OFF} current ratio, SS, and mobility are analyzed and compared to optimize the device dimensions. Adevice with high-K dielectric (HfO_2) and 30 nm active channel layer thickness with channel length giving the better results as compared to other dimension in the term of TFT's performance. A device with 30 nm active channel layer thickness with HfO_2 dielectric material having 0.66 V threshold voltage, 0.067 SS(V/dec), 6.44 $cm^2/V.s$ mobility, and 10^9 I_{ON}/I_{OFF} ratio. Lower threshold voltage turns on the TFT and starts current flow and high *on/off* ratio for fast

switching between from off state to on state. So it can conclude based on results this type of TFT can be used in such applications as display devices, photodetectors, etc.

Declaration Funding
NA

Conflicts interest/Competing Interests
No conflict of interest is involved

Data Availability
Data is available with the corresponding author and can be produced if required.

Authors' Contributions
- Manju Choudhary performed the simulation of TFT with all parameter variation.
- Lava Bhargava and C.Periasamy checked the result with variation.
- Pooja Choudhary edited the manuscript.

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