

A New Topology of Parallel Current Source Applied for Li-Ion Battery Charger

Hao Nguyen-Van^{1,2}, Minh Nguyen¹, Loan Pham-Nguyen^{1*}

¹ Hanoi University of Science and Technology, No. 1 Dai Co Viet, Hai Ba Trung, Ha Noi, Viet Nam

² Quynhon University, No. 170 An Duong Vuong, Quy Nhon, Binh Dinh, Viet Nam

Received: March 13, 2017; accepted: June 9, 2017

Abstract

In this paper, a design approach of long-life Li-Ion battery charger is presented. To produce charging current according to the Li-Ion battery charging process, a new topology of parallel current source is proposed. This topology allows to attain low trickle current in the pre-charge state while the large current state can be guaranteed at high level and that results in a significant reduction of damage to Li-Ion battery. Moreover, the charging mode control signals are more stable by introducing a hysteresis comparator into the charging mode controller. This Li-Ion battery charger is designed based on 0.13 μm CMOS technology and simulated by Cadence. The post-layout simulation results shown a good performance in which the charging process is terminated at a battery voltage of 4.2 V and a charging current of 43 mA. The simulated trickle current is approximately 203 μA and the maximum charging current reaches 975 mA. The designs offer an average power efficiency of 92.2 % is obtained with battery voltage varying from 2.9 V to 4.2 V.

Keywords: Li-Ion battery, Charging circuit, Charging mode controller, Parallel current source

1. Introduction

Nowadays, Li-Ion battery is widely used in electronic devices such as laptop, smartphone, camera and electric vehicles because of its advantages over other types of rechargeable battery. The Li-Ion batteries [1] offer high recharge cycle (1000 cycles), high energy density, and no memory effect. Especially, it also has notably low self-discharged rate (2 % to 8 % per month) as well as a wide range of operating condition (charge at $-20\text{ }^{\circ}\text{C}$ to $60\text{ }^{\circ}\text{C}$, discharge at $-40\text{ }^{\circ}\text{C}$ to $65\text{ }^{\circ}\text{C}$). The required cells for a battery of a given voltage can also be reduced since single cells of Li-Ion battery operate in the range of 2.5 V to 4.2 V, approximately three times that of NiCd and NiMH cells. In order to achieve good lifetime and reliability, a standard Li-Ion battery adopts three charging modes of [2-5] which are shown in Fig. 1 and can be described as follows:

Constant trickle current (TC) mode: when battery voltage is lower than V_L , the charging current is maintained at a constant low value ($0.1C$) to prevent the battery from being damaged by overheating. C stands for capacity of battery and its unit is Ampere-hour (Ah).

Constant large current (LC) mode: when battery voltage is in between V_L (2.9 V) and V_H (4.2 V), the battery is charged with high constant current ($0.2C - 1C$) to reduce charging time.

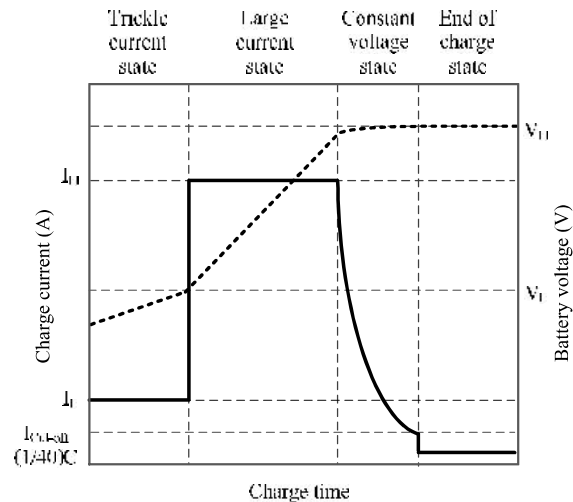


Fig. 1. Li-Ion battery charging modes

Constant voltage (CV) mode: when battery voltage reaches its specification value V_H , the charging current is degraded to a value lower than a predicted cut-off current ($0.02C - 0.07C$). Consequently, the battery will reach its full capacity and the charging process is completed.

Many research papers have proposed different CMOS-based architectures of Li-Ion battery charger which are mainly designed to work at constant supply voltage. But these designs have a large difference between supply and battery voltage that increase power consumption of power MOSFET used as a current source thus reducing power efficiency of charging system [3-8]. In order to improve power efficiency, the supply voltage of charging circuit will adapt to battery voltage by using a controlled supply

* Corresponding author: Tel.: (+84) 983.205.761
Email: loan.phamnguyenthanh@hust.edu.vn

voltage circuit [9-11]. However, in these researches, only one power MOSFET which plays the role of main current source is used. This MOSFET with constant dimension (fixed channel width and length) limits the current range at two different charging modes (TC, LC) when adaptive supply voltage is applied. According to the Li-Ion battery charging diagram, the charging current at TC mode must be remained low for long battery lifetime but high enough at LC mode for fast charging time. Therefore, our proposed parallel current source allow to meet this requirement. Two power MOSFETs connected in parallel is implemented to maximize charging current at LC mode while keeping the trickle current unchanged by enabling only one of these two MOSFETs. Moreover, the proposed design can also address another issue regarding charging mode transition time. The variation of battery voltage according to minor voltage drop on internal resistance (Equivalent Series resistance - ESR) of Li-Ion battery will affect system performance due to chattering in mode control signal. Thus, the simple internal hysteresis comparator with the amount of hysteresis voltage approximately several hundred millivolts is also used to prevent the charging system from this chattering.

In section 2, the structure and operation of proposed Li-Ion battery charger will be discussed with key focus on charging mode controller and current source. The circuit design of components is presented in section 3. The post-layout results are described in section 4 and the conclusions are given in section 5.

2. Charger descriptions

2.1. System Architecture

The architecture of charging system is shown in Fig. 2 which consists of two main blocks: battery charging circuit and controlled supply voltage circuit. The supply voltage is always kept at 0.3 V, higher than the battery voltage to enhance power efficiency

of battery charger. In this paper, the battery charging block is designed to feed different charging currents into battery following strictly the profile shown in Fig. 1 to avoid damage to Li-Ion battery. This block includes five sub-circuits: charging mode controller, reference current generator, charging current controller, parallel current source and current sensor.

The charging mode controller detects the value of battery voltage to generate suitable control signals for the charging process and so V_{TC} , V_{LC} and V_{CV} are mode control signals and activated in the mode TC, LC and CV, respectively. The reference current generator produces required reference current which is controlled by mode control signals from charging mode controller. Meanwhile, the charging current controller compares this reference current with sensing current from the current sensor to generate voltage signals for controlling parallel current source and determining the end of charge state. The detail of operation principle of the battery charging block is described below.

2.2. Charging mode controller

In charging process, the charging mode controller which is a logic control system determines the battery voltage to create control signals as charging mode control and transmission gate control. As shown in Fig. 3, the battery voltage is compared with the reference voltages V_H , V_L by two comparators C_1 and C_2 , respectively. The output signals, also considered as control signals, are sent into logic circuit (I_1 - I_5) in order to produce mode control signals V_{TC} , V_{LC} , V_{CV} and control signals V_{S1} , V_{S2} which are used to select the current sources I_{Ch1} , I_{Ch2} by turning on/off two transmission gates in the charging current controller. Once the battery voltage reaches its full capacity, the feedback signal V_{End} from charging current controller is activated then signals V_{S1} , V_{S2} are turned off as charging process is terminated. The states of each signal of charging mode controller are listed in table 1.

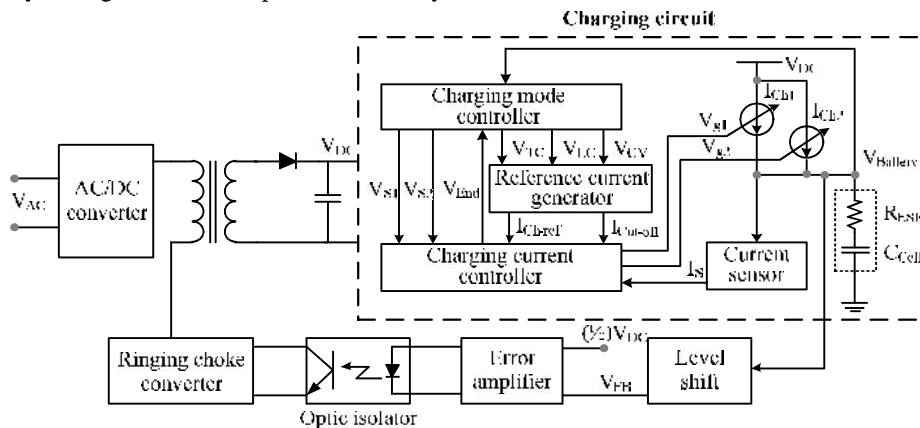


Fig. 2. System architecture

Table 1. Charging mode control functions

Conditions	V_{TC}	V_{LC}	V_{CV}	V_{End}	V_{S1}	V_{S2}
Constant trickle current	H	L	L	L	H	L
Constant large current	L	H	L	L	H	H
Constant voltage	L	L	H	L	H	H
End of charge	L	L	H	H	L	L

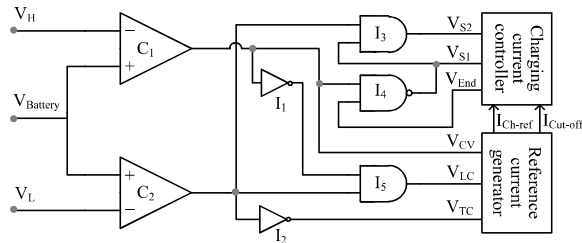


Fig. 3. Charging mode controller

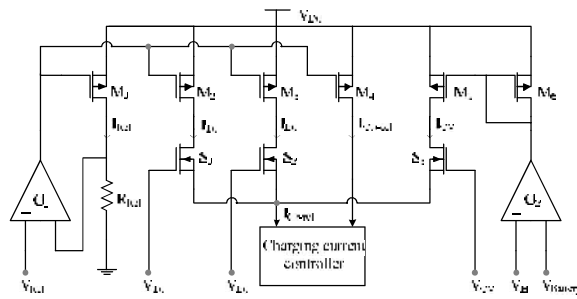


Fig. 4. Reference current generator

2.3. Reference current generator

In reference current generator (Fig. 4), the reference circuit including operational amplifier O_1 and PMOS transistor M_1 and resistor R_{ref} produces constant current I_{ref} which equals to V_{ref}/R_{ref} . The reference currents I_{TC} , I_{LC} , $I_{Cut-off}$, generated from the current mirror system ($M_1:M_2-M_4$), are proportional to the current I_{ref} . These currents are used as reference corresponding to different charging states such as trickle current, large current, and the end of charge state. However, for constant voltage charging state, the reference current I_{CV} is created differently and its value decreases from high level (I_{LC}) to low level ($I_{Cut-off}$). In this state, an operational amplifier O_2 and a current mirror circuit consisting of two PMOS transistors M_5 , M_6 are implemented so that when battery voltage reaches 4.2 V, the current I_{CV} starts to be generated in the constant voltage mode. For each charging mode, the current I_{TC} or I_{LC} or I_{CV} is sent to the charging current controller through three switches S_1 , S_2 and S_3 which are controlled by the mode control signals V_{TC} , V_{LC} and V_{CV} , respectively.

2.4. Charging current controller

The charging current controller is illustrated in Fig. 5. In this structure, the current comparator including NMOS transistors M_5 , M_7 and an operational transconductance amplifier O_1 compares reference current I_{Ch-ref} from the reference current generator with sensed current I_S from the current sensor. The output voltage of this comparator V_g varies with the change of input currents I_{Ch-ref} , I_S and it is connected to the lowest voltage level of transmission gate block consisting of M_1 , M_3 and M_2 , M_4 . These transmission gates are controlled by control signals V_{S1} and V_{S2} from the charging mode controller as mentioned in subsection 2.2. Finally, the output of charging current controller, voltages V_{g1} and V_{g2} are created at each charging mode providing different gate voltages to the parallel current source because their values strongly depend on the voltage V_g . Moreover, a mirror circuit (M_6 , M_7) compares directly sensed current I_S with reference current $I_{Cut-off}$ to activate the end of charge state. Especially, when I_S is detected to be lower than $I_{Cut-off}$, V_{End} is pulled up to high level and feedback to the charging mode controller. Then, the control signals V_{S1} and V_{S2} turn the transmission gates off, and the charging process is terminated.

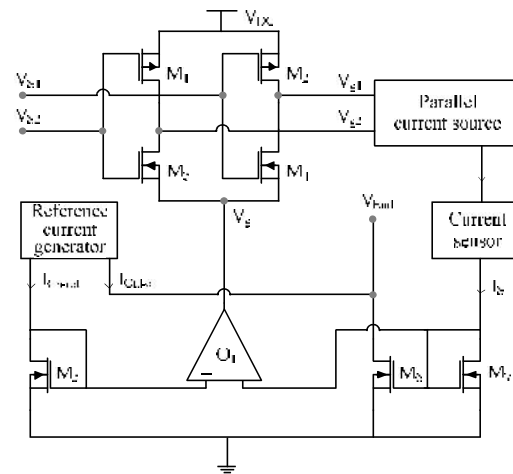


Fig. 5. Charging current controller

2.5. Current source and current sensor

In this sub-circuit, the parallel current source is designed so that just one current source is used for the TC mode and then both sources are used for the LC mode. As shown in Fig. 6, the power PMOS transistors M_{P1} , M_{P2} , which are considered as current sources, are used to provide charging current for the Li-Ion battery. Besides, PMOS transistors M_{S1} and M_{S2} play the role of the current sensors. The operational amplifier O_1 is used to keep drain voltage of M_{Si} equal to the battery voltage $V_{Battery}$. As a result, the current of this sensed transistor is always

proportional to the current of the power transistor by the ratio $1/N$, where N is 5000. This technique enables the charging currents at both TC and LC modes to satisfy this standard of Li-Ion battery. It comes from that while the trickle current can be scaled down further by reducing (W/L) ratio of M_{P1} to guarantee the lifetime of battery, the large current also can reach $0.5C$ or higher by increasing (W/L) ratio of M_{P2} .

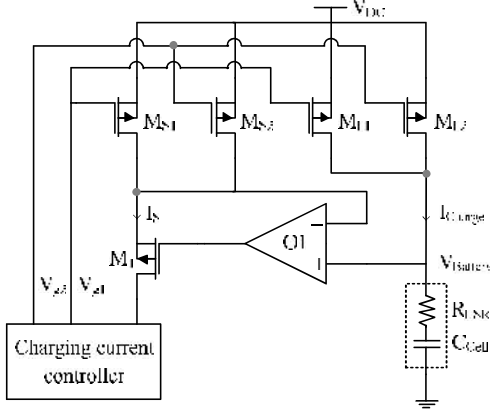


Fig. 6. Current source and current sensor

3. Design components

3.1. Hysteresis comparator

The battery voltage always increases during the charging process, therefore the hysteresis comparator is applied in charging mode controller to eliminate the chattering output signal for improving stability of charging mode control signals. The circuit implementation of this comparator [12] is shown in Fig. 7. In which, the differential stage (M_1 - M_7) with positive feedback to provide a high gain as it is given by (1)

$$A_v = \frac{\sqrt{K_{n1}(W/L)_1} \cdot 1}{\sqrt{K_p(W/L)_3} \cdot 1 - \alpha} \quad (1)$$

where, $\alpha = (W/L)_5/(W/L)_3 = (W/L)_6/(W/L)_4$, is the positive feedback factor.

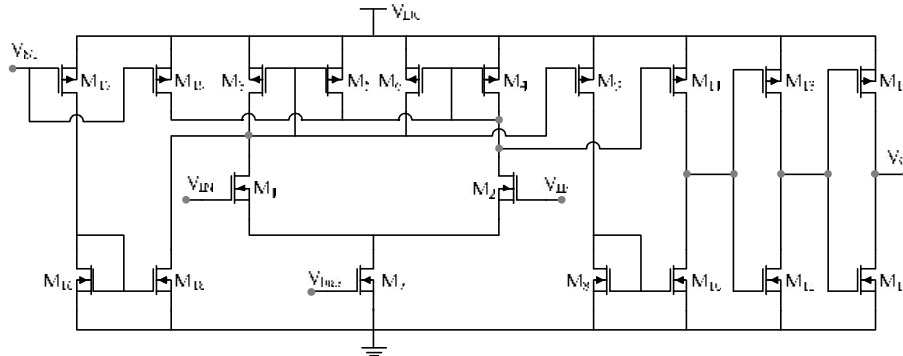


Fig. 7. Schematic of the hysteresis comparator

In this situation, the positive feedback factor α is greater than 1 turning this stage into a Schmitt trigger circuit with the amount of hysteresis voltage determined by (2)

$$V_{hys} = 2 \sqrt{\frac{I_7}{K'_{n1}(W/L)_{1,2}} \frac{\sqrt{\alpha} - 1}{\sqrt{1 + \alpha}}} \quad (2)$$

where, transconductance parameter $K'_{n1} = \mu_n C_{ox} / 2$.

The push-pull stage is implemented by using MOS transistors M_8 - M_{11} , which is a differential-to-single-ended output converter. The inverter chains M_{12} - M_{15} are added to increase the response of the comparator's output signal. In addition, the start-up circuit (M_{16} - M_{19}) is used to set the initial state thanks to the control signal V_{st} activated at low voltage. In this design, the comparator is designed so that the hysteresis voltage V_{hys} is approximately 200 mV that guarantees the stability of charging mode control signal in the charging process.

3.2. Operational amplifier

To generate the reference current with accurate control of the charging current, the operational amplifier (OA) in the current sensor and reference current generator must be designed to satisfy the requirements such as small offset voltage, wide range of output swing and especially wide range of supply voltage. For instance, the OA in the current sensor with small offset voltage is required to keep sensing current always proportional to the charging current. The two-stage operational amplifier [13-14] is designed as shown in Fig. 8, which includes the differential stage (M_1 - M_5) and the high-gain stage (M_6 - M_7). Accordingly, the gain of this OA can be found as shown in (3) and minimum offset voltage easily achieved when the DC balance condition in (4) is satisfied.

$$A_v = g_{m1} g_{m7} R_I R_J \quad (3)$$

where, g_{m1}, g_{m7} are transconductance of MOS transistors M_1 and M_7 ; $R_{I1} \alpha R_{I2}$ are the output resistance of the amplifier stages.

$$\frac{2(W/L)_4}{(W/L)_5} = \frac{(W/L)_7}{(W/L)_6} \quad (4)$$

$$\frac{(W/L)_{8,1}}{(W/L)_{6,7}} = \frac{I_{8,1}}{I_{6,7}} \quad (5)$$

In addition, the simplest frequency compensator is also implemented by miller capacitor C_c and PMOS transistor M_{11} considered as it is a nullifying resistor. A reference circuit (M_8 - M_{10}) is used to identify the operational region of PMOS transistor M_{11} that allow compensator to operates properly with dynamic characteristic of OA. Besides, the size of the MOS transistors M_8, M_{10} must be proportional to the MOS transistors M_6, M_7 as explained in (5).

3.3. Operational transconductance amplifier

Because the parasitic capacitance on gate terminal of power MOSFETs to ground is high, it is considered to be a load capacitor in the charging current controller. Therefore, an operation transconductance amplifier (OTA) [15] is perfectly suited to the requirements of current comparator such as operating voltage range, high gain, and stability for closed-loop. The circuit implementation of this OTA is shown in Fig. 9, which includes the differential stage (M_1 - M_6) with the gain enhancement technique and the push-pull output stage (M_{10} - M_{13}). Accordingly, the gain of OTA can be described following (6) and the dominant pole is determined by the output resistance R_{II} and the load capacitor C_L as refer to (7). This design confirms that OTA in the closed-loop configuration will be more stable with large load capacitor.

$$A_v = g_{m1,2} K R_{I1} \quad (6)$$

$$\omega_{3d} = \frac{1}{R_{I1} C_L} \quad (7)$$

where, $g_{m1,2}$ is the transconductance of NMOS transistor M_1 or M_2 ; R_{I1} is the output resistance of the push-pull stage; The coupling factor

$$K = (W/L)_1 / (W/L)_3 = (W/L)_1 / (W/L)_4$$

4. Simulation results

The battery charger is designed to work within the battery voltage range from 2 V to 4.2 V. In order to reduce the transient analysis time for this simulation, the initial battery voltage and supply voltage are set at 2.7 V and 3 V, respectively. The battery capacity is chosen at 2000 mAh, RC series circuit represents the battery source and value of V_L and V_H are 2.9 V and 4.2 V, respectively.

Figure 10 describes the layout of battery charger with an area of about 0.25 mm x 0.142 mm. The simulation results of proposed charger using Cadence software are shown in Fig. 11-13. The charging mode control signals without chattering are illustrated in Fig. 11. The simulation result confirms that the state of mode control signals is only changed when the battery voltage reaches approximately 2.9 V and 4.2 V, respectively.

The waveforms of charging current and battery voltage are presented in Fig. 12. It is shown that the battery voltage increased from 2.7 V to 4.2 V (Li-Ion battery is full of capacity). The charging current in constant trickle current mode is 203 mA which is close to 0.1C, and the maximum charging current in constant large current mode is 975 mA. The charging process is completed when the charging current in constant voltage mode reaches cut-off value of about 43 mA.

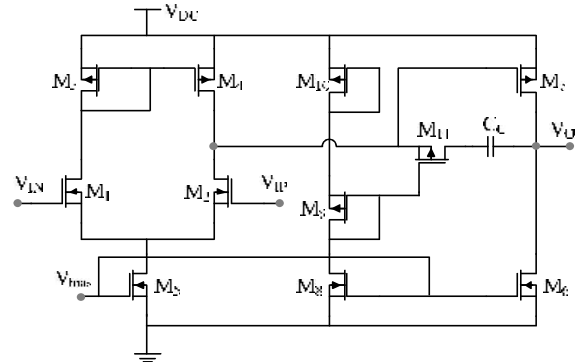


Fig. 8. Schematic of two-stage operational amplifier

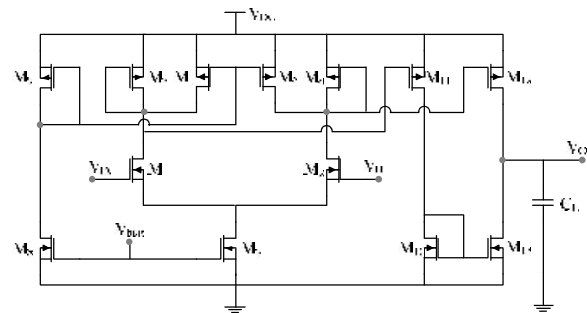


Fig. 9. Schematic of operational transconductance amplifier

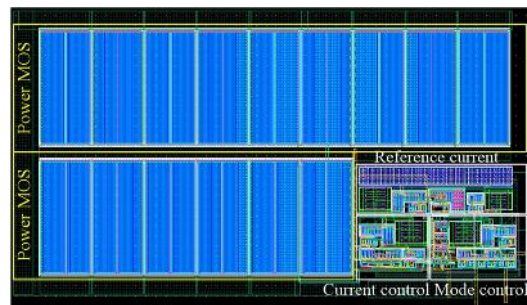
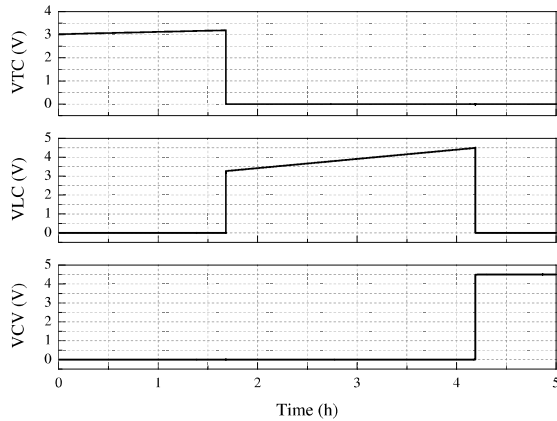
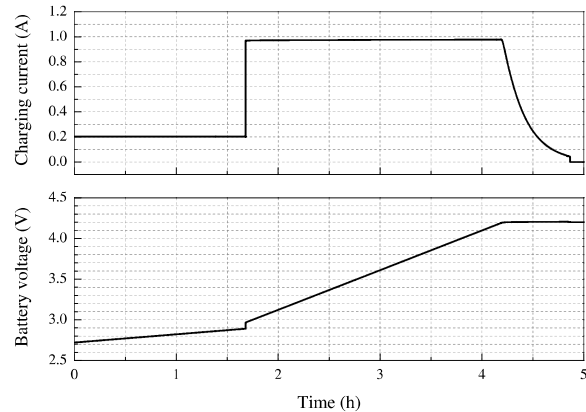
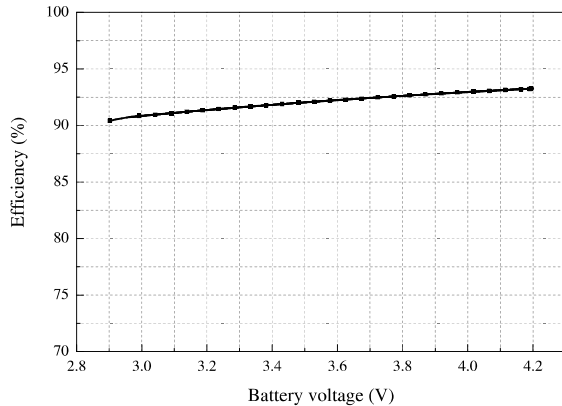


Fig. 10. The layout graph of battery charger

Table 2. Comparison sheet

Parameter	[4]	[8]	[10]	[11]	This work (Simulation)
Technology	TSMC 0.35 μm	TSMC 0.35 μm	TSMC 0.35 μm	0.18 μm 1P6M	TSMC 0.13 μm
Power supply voltage	5 V	5 V	2.3 V - 4.5 V	4.8 V - 5.0 V	2.3 V - 4.5 V
Average power efficiency	67.89 %	67.4 %	91.2 %	79 %	92.2 %
Trickle charging current	325 mA	304 mA	300	74 mA	203 mA
Large charging current	710 mA	711 mA	698 mA	450 mA	975 mA
Output voltage	2.5 V - 4.2 V	2.0 V - 4.2 V	2.0 V - 4.2 V	NA - 4.2 V	2.0 V - 4.2 V

**Fig. 11.** Simulation results of the charging mode control signal**Fig. 12.** Simulation results of charging current and battery voltage**Fig. 13.** The power efficiency of battery charger

As shown in Fig. 13, the average power efficiency of battery charger can achieve 92.2 %. The performance of Li-Ion battery charger is presented in table 2 in comparison with state-of-the-art studies. It is obvious that the proposed architecture has higher charging current in keeping low trickle current during charging process. In other words, it offers shorter charging time without compromising battery's safety.

5. Conclusion

A Li-Ion battery charger with parallel current source has been designed using TSMC 0.13 μm CMOS technology. This parallel current source is flexible for the choice of current range from trickle to large current. In this design, the large current at LC is chosen at 0.5C and gets the value of 975 mA. Moreover, if the charging current is defined at 1C, the large current can reach the value of 2 A with low trickle current of 200 mA. The charging circuit operates in a supply voltage range of 2.3 V to 4.5 V and its output voltage is from 2 V to 4.2 V. The post-layout simulation results show that the charging mode control signals are stable during the mode transition times. The result suggests that it is a promising candidate to operate effectively in noise environments. Three kinds of charging current according to trickle current, large current and constant voltage mode are very suitable for Li-Ion batteries. It guarantees for prolonging battery lifetime. The average power efficiency of this proposed charger in constant large current mode is about 92.2 %.

References

- [1] D. Linden, and T. B. Reddy, Handbook of batteries, ch. 35, pp. 35.2, New York: McGraw-Hill, 2002.
- [2] S. Dearborn, "Charging Li-ion batteries for maximum run times," Power Electron. Technol. Mag., Apr. (2005), pp. 40-49.
- [3] C. C. Tsai, C. Y. Lin, Y. S. Hwang, W. T. Lee, and T. Y. Lee, "A multi-mode LDO-based Li-ion battery charger in 0.35 μ m CMOS technology," in Proc. IEEE Asia-Pacific Conference on Circuits and Systems, Dec. 2004, pp. 49-52.
- [4] Y. S. Hwang, S. C. Wang, F. C. Yang, and J. J. Chen, "New compact CMOS Li-Ion battery charger using charge-pump technique for portable applications," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 54 (4), Apr. (2007), pp. 705-712.
- [5] C. H. Lin, H. W. Huang, and K. H. Chen, "Built-in resistance compensation (BRC) technique for fast charging Li-ion battery charger," in Proc. IEEE Custom Integrated Circuits Conference, Sept. 2008, pp. 33-36.
- [6] B. Do Valle, C. T. Wentz, and R. Sarpeshkar, "An Area and Power-Efficient Analog Li-Ion Battery Charger Circuit," in IEEE Transactions on Biomedical Circuits and Systems, vol. 5 (2), Apr. (2011), pp. 131-137.
- [7] H. Y. Yang, T. H. Wu, J. J. Chen, Y. S. Hwang, and C. C. Yu, "An omnipotent Li-Ion battery charger with multimode controlled techniques," in Proc. IEEE 10th International Conference on Power Electronics and Drive Systems (PEDS), Apr. 2013, pp. 531-534.
- [8] C. C. Tsai, "A reduced Li-Ion battery charger for portable applications," in Proc. 2013 Ninth International Conference on Natural Computation (ICNC), Jul. 2013, pp. 1718-1722.
- [9] M. Chen, and G. A. Rincon-Mora, "Accurate, Compact, and Power-Efficient Li-Ion battery charger circuit," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 53 (11), Nov. (2006), pp. 1180-1184.
- [10] J. J. Chen, F. C. Yang, C. C. Lai, Y. S. Hwang, and R. G. Lee, "A high-efficiency multimode Li-Ion battery charger With variable current source and Controlling previous-stage supply voltage," in IEEE Transactions on Industrial Electronics, vol. 56 (7), July (2009), pp. 2469-2478.
- [11] P. H. V. Quang, H. T. Thanh, and J. W. Lee, "A Fully integrated multimode wireless power charger IC with adaptive supply control and Built-In resistance compensation," in IEEE Transactions on Industrial Electronics, vol. 62 (2), Feb. (2015), pp. 1251-1261.
- [12] R. Gregorian, Introduction to CMOS Op-Amps and Comparators, ch. 5, pp. 196-197, New York: Wiley, 1999.
- [13] P. E. Allen, and D. R. Holberg, CMOS analog circuit design, ch. 6, pp. 286-298, New York: Oxford Univ. Press, 2012.
- [14] J. Mahattanakul, and J. Chutichatuporn, "Design procedure for two-stage CMOS opamp with flexible noise-power balancing scheme," in IEEE Trans. Circuits and Syst. I, Reg. Papers, vol. 52, no. 8, Aug. (2005), pp. 1508-1514.
- [15] R. J. Baker, CMOS: Circuit design, Layout, and Simulation, ch. 24, pp. 796-797, New Jersey: Wiley, IEEE Press, 2010.