Clock Generator for Wide-band Delta-Sigma ADCs

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Abstract

*In this paper, a new design of clock generator applied for high-speed and wide-band receiver is discussed. The circuit generates 4 local oscillators (LO) at frequency f_{LO} = 0.5*f_{CLK} from input clock frequency f_{CLK}, which is in the range of 800 MHz – 12 GHz; and 8 phases Φ, by selecting 3 bits S_0 S_1 S_2, at sampling frequency f_S = 400 MHz—425 MHz. LO clocks and Φ phases are designed to satisfy the strict requirements such as falling/rising time, non-overlapping, pulse width and synchronization, power consumption (<20 mW). The proposed clock generator is implemented in CMOS 65nm and simulated in Cadence at TT/85 °C.*

Keywords: Clock generator, Wide-band, ADC

1. Introduction

Nowadays, demand for direct receiver is increasing rapidly as the never-ending user requirements are going higher and higher for accessing speed and bandwidth [1]. Moreover, the bulky and multi-step design of traditional heterodyne architecture receivers are no longer suitable for recent technology trends that require tiny and low-power devices such as IoT communications. Among new design approaches, Direct Delta-Sigma Receiver (DDSR) has been emerging as an attractive solution for new RX architectures [2]. Despite many studies about DDSR, more works still need to be done on implementation reliability of standalone high-speed and wideband receiver. In the published papers, clock generator has not been well covered even though it is one of the most important parts in a high speed and wideband DDSR involving system accuracy, linearity and power consumption. In this paper, an on-chip clock generator is proposed for a high-performance receiver and more specifically a 4th-order DT-DDSR [3] (Fig. 1). Due to the symmetry of I and Q branches in DDSR, only I branch structure is shown for the sake of simplicity.

One of the key features of the architecture is loop filter clock which is used as divided LO clock allowing loop filter to operate at the lower frequency Fs over a wide-range of LO frequency (400 MHz to 6 GHz in this study).

This clock generator is used in a wide-band DSDR with input clock frequencies ranging from 800 MHz – 12 GHz. Deriving from the wideband delta-sigma ADC architecture presented in Fig.1, the four LO clock signals and 8 phases Φ using in base-band loop filter are created from clock generator to determine the system synchronization and linearity which are vital criteria in DSDR [4]. The specifications of LO clock signals and base band phases are listed in Table 1.

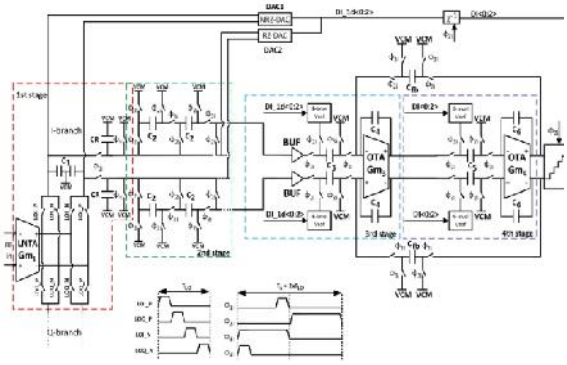

Fig. 1. 4th-order Direct Delta-Sigma Receiver.

In a DSDR, there are 2 symmetrical branches I/Q with a delay of 0.25T_{LO} in Q branch against I branch. LO clock signals must be designed to satisfy the synchronization requirements. Figure 2 describes detailed specifications of these signals in the case of T_S = 2T_{LO}.

There are two kinds of the clock signals: LO clock and loop filter clock. The LO clock drives the mixer switches at a frequency range of 0.4 GHz - 6.0 GHz. The loop filter clock drives the loop filter switches, the quantizer, and the DACs at low speed ranging from 0.4 GHz to 0.425 GHz. The loop filter clock is a division of the LO clock to synchronize the feedback signal with the feed-in signal as well as to

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relax design constraints of the loop filter. There is an external clock source running at a frequency range of 0.8 GHz – 12.0 GHz, and it is required a clock generator to create two other clocks. A signal CLK_SEL<0:2> is used to select the division ratio of the LO/Fs. As there are 8 different ratios, a 3-bit binary code is adopted for this control signal. As shown in Fig. 2, the LO clock is a non-overlapping 4-phase one including LOI_P, LOI_N, LOQ_P, and LOQ_N. Each phase has 25% duty-cycle of TLO. The rising and falling times of the LO clock are very small at 10 ps due to the short integrating period, especially at 6.0 GHz LO.

Table 1. Specifications of LO Clock in TT/85 °C

Parameters	LO clock	Loop filter clock
No. of Phases	4	8
Duty-Cycle	25%	
Non-overlapping	YES	YES
Voltage High (V_H)	1.2 V	1.2 V
Voltage Low (V_L)	0 V	0 V
Rising time(T_Rise)	14 ps	100 ps
Falling time(T_Fall)	14 ps	100 ps
Frequency range	0.4, 0.85, 1.2, 2.1, 2.4, 3.6, 4.0, 6.0 GHz	400-425 MHz, division of LO by 1, 2, 3, 5, 6, 9, 10, 15

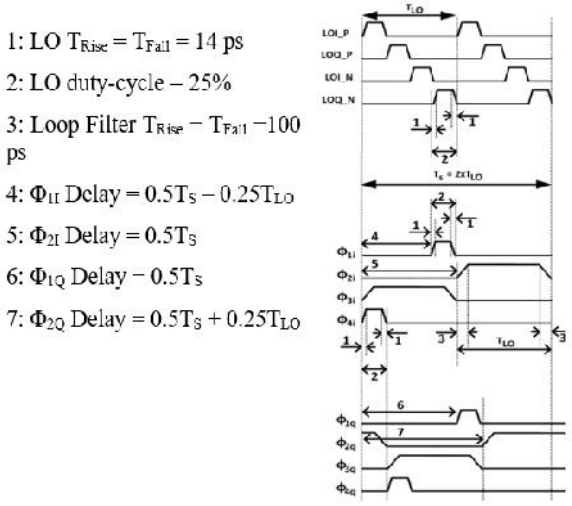


Fig. 2. Specifications with $T_S = 2T_{LO}$.

The loop filter clock is also a non-overlapping 4-phase one: ϕ1i- ϕ4i and ϕ1q- ϕ4q for I branch and Q branch, respectively. ϕ1q- ϕ4q is a delay-by-TLO/4 version of ϕ1i- ϕ4i. The two phases ϕ2i (ϕ2q) and ϕ3i (ϕ2q) are very relaxed with 50% duty-cycle of Ts. Their rising time and falling time are also relaxed at 100 ps. The two phases ϕ1i (ϕ1q) and ϕ4i (ϕ4q) are more challenging as their high time is equal to the one of the LO clock. Moreover, their rising and falling times are also limited to 14 ps to ensure the synchronization of the 1st integrator with both the LO clock and the loop filter clock.

2. Clock generator descriptions

2.1. System Architecture

The clock generator described in Fig. 3 consists of 3 main blocks: DIV1_2, LO_GEN and LF_GEN. DIV1_2 block generates 4 LO clock signals with 50% duty-cycle from input clock. These four signals are utilized in LO_GEN block to create 4 LO signals with 25% duty-cycle. Q_P and Q_N are 25% pulse width delayed signals of IP and IN, respectively. Q_P, Q_N and input clock signal are fed into LF_GEN block generating 8 phase Φ.

It is noticed that, flip-flop is an essential reused cell in these circuits which requires careful design to reduce power consumption but increase circuit accuracy. Dynamic Transmission Gate (DTG) flip-flop and Current Mode Logic (CML) are commonly used in high-frequency circuit design (Fig. 4). For high-speed DDSR architecture, optimization of power consumption at very high frequencies is a crucial task. Table. 2 shows the comparison between DTG and CML flip-flop in DDSR that emphasizes the advantage of DTG against CML flip-flop.

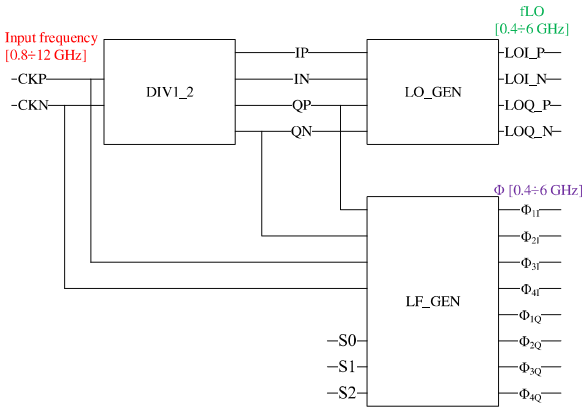


Fig. 3. Clock generator top module

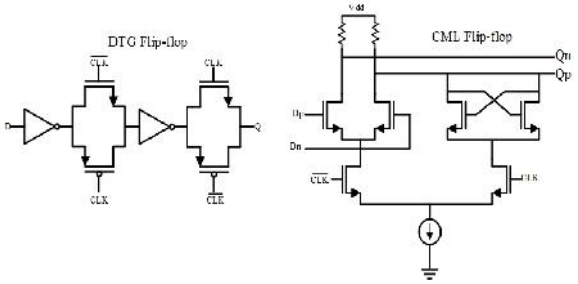


Fig. 4. CML and DTG Filip-flop schematic

Table 2. Power dissipation of clock generators using DTG versus CML

f_{LO} (GHz)	**DTG (mW)**	*CML (mW)*
0.4	**2.8**	*15.6*
0.85	**4.1**	*17.5*
1.2	**5.5**	*19.2*
2.1	**8.5**	*22.7*
2.4	**9.2**	*24.1*
3.6	**13.3**	*28.7*
4.0	**14.5**	*30.7*
6.0	**21.1**	*38.3*

2.2. DIV1_2 & LO_GEN

DIV1_2 is a block to divide clock for 2 which consists of two DFF as described in Fig. 5. DFF is a Transmission Gate Latch to determine delays at P and N outputs which are identities in comparing with the input signal.

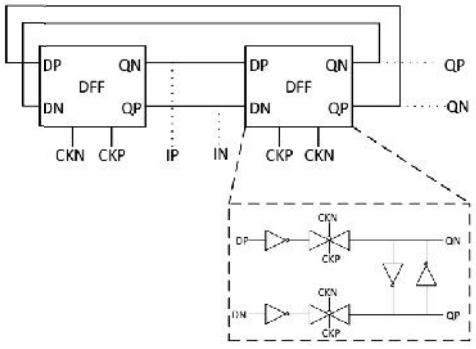
The synchronization at P and N outputs is critical to create 4 LO signals in LO_GEN block, while the circuit for LO_GEN block is simply made of AND digital cells as the following equations: LOI_P = IN.QN; LOQ_P = IP.QN LOI_N = IP.QP and LOQ_N = IN.QP. The optimization of AND gate sizes is careful carried-out following duty-cycle of LO signals. The LO signals duty-cycle is 25% as described in the system design.

2.3. LF_GEN

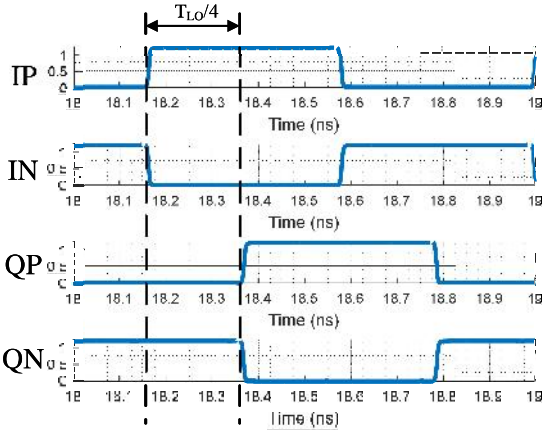
The 8 Φ phases with frequencies of 400-425 MHz are formed from LO_GEN block. The 4 phases Φ_{2I}, Φ_{2Q}, Φ_{3I}, Φ_{3Q} are described in Fig. 6. 3-bit selection S[0:2] is to choose N dividing factor using in Divider to create these phases at 400-425 MHz range regardless the input clock frequency. The detail selection is shown in Table 3.

Table 3. Selection of Divider coefficient

f_{CLK} (GHz)	f_{LO} (GHz)	S_0	S_1	S_2	N	f_S (MHz)
0.8	0.4	0	0	0	1	400
1.7	0.85	0	0	1	2	425
2.4	1.2	0	1	0	3	400
4.2	2.1	0	1	1	5	420
4.8	2.4	1	0	0	6	400
7.2	3.6	1	0	1	9	400
8.0	4.0	1	1	0	10	400
12	6.0	1	1	1	15	400



(a)



(b)

Fig. 5. a) DIV1_2 structure. b) output waveforms of DIV_2

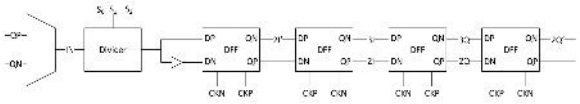


Fig. 6. Φ_2, Φ_3 generator

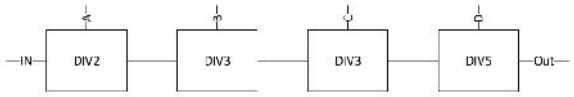
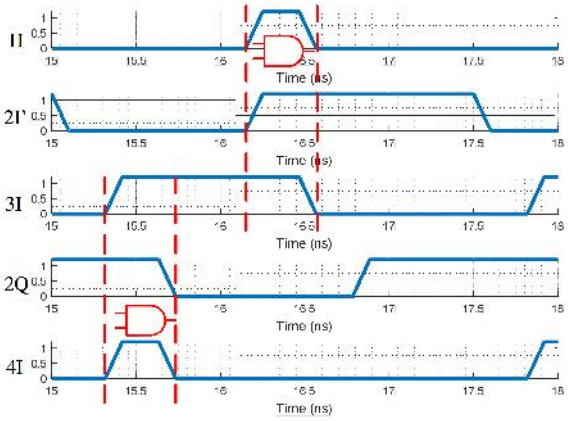


Fig. 7. Structure of a divider

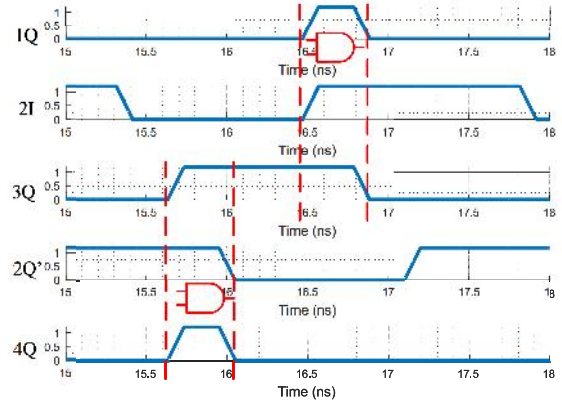
Divider structure is described as in Fig.7. Thus the dividing factors are multiple of 2, 3 or 5, the Divider is formed from divider-by-2 (DIV2), divider-by-3 (DIV3) and divider-by-5 (DIV5) blocks [4]. Moreover, these dividers have enable signal to select output signal which can be either input signal or divided input signal. If enable signal is high the output clock is divided by the indicated factor. And if the enable signal is low the input signal is passed to output clock without being divided. A, B and C enable signals are functions of 3-bit selection S[2:0] in respond to dividing factor in Table 3.

The principle of generating Φ_1 and Φ_4 phases can be described in Fig. 8. The synchronization of LO and

LF is a challenge in designing the circuit. It is noticed from Fig. 2 that rising edges of Φ_{3I} should be synchronized with rising edges of LOI_P. Referring to the principle of generating LOI_P, the LOI_P must be synchronized with rising edges of QN. Then, in order to synchronize Φ_{3I} and LOI_P, it is required that Φ_{3I} and QN are synchronized as well.



(a)



(b)

Fig. 8. a) Φ_{1I}, Φ_{4I} waveforms b) Φ_{1Q}, Φ_{4Q} waveforms

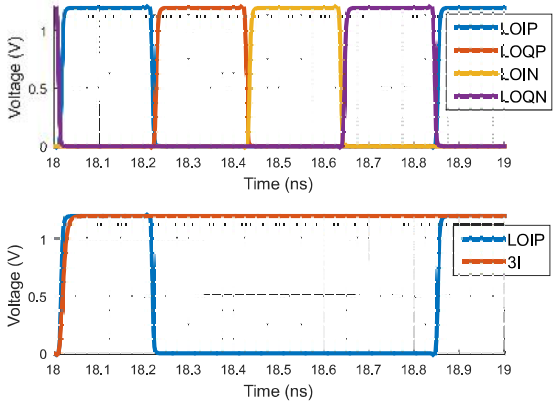


Fig. 9. LO signal waveforms and synchronization of IP & 3I

3. Simulation result

This circuit is implemented using CMOS 65nm technology and simulated using Cadence Spectral Environment at condition TT/85°C. The clock frequency is selected at 2.4 GHz. Fig. 9a shows 4 LO signals with duty cycle of 25%, V_H = 1.2V, V_L = 0V and non-overlapping. As it can be seen from Fig. 9b, 4 LO signal waveforms satisfy the required synchronization of LOI_P and Φ_{3I} waveforms.

8 LF phase signals can be observed in Fig. 10. Synchronization can be clearly remarked from Φ_3, Φ_1 and Φ_4 in both I-branch and Q-branch.

Table 4 summarizes the performance of clock generator using CMOS 65nm technology. The simulated results confirms that the proposed circuit meets technical requirement of the design.

Table 4. Features of proposed clock-generator

Features	*Value*
Technology	TSMC 65nm
Supply Voltage	1.2 V
T_Rise, T_Fall of LO	10.4 ps
T_Rise, T_Fall of Φ	22.2 ps
Non-overlap	YES
V_High	1.2 V
V_Low	0 V

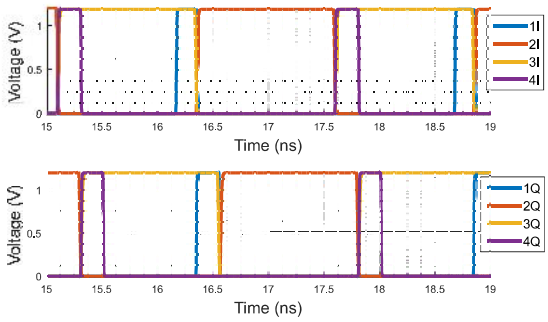


Fig. 10. I and Q - LF phase signal waveforms.

4. Conclusion

Clock generator is designed and verified in CMOS 65nm technology, using supply voltage of 1.2V. The simulation result shows the high accuracy of clock generator, that meet the requirement in high-speed and wide-band (0.4 – 6 GHz) direct receiver using delta-sigma ADC architecture. The proposed clock generator offers a relatively low power consumption of about 20 mW at the highest operation frequency of 6 GHz.

Acknowledgment

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References

[1] K. Koli., “A 900-MHz Direct Receiver in 65-nm CMOS,” IEEE Journal of Solid-State Circuits, vol. 45, no. 12, pp. 2807–2818, Dec 2010.

[2] M. Englund., “A Programmable 0.7-to-2.7GHz Direct Receiver in 40nm CMOS,” Solid-State Circuits, IEEE Journal of, vol. PP, no. 12, pp. 1–12. 2015.

[3] M. T. Nguyen, C. Jabbour and V. T. Nguyen, "A flexible receiver using ΔΣ modulation," 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 1470-1473.

[4] Francesco Barale “Frequency Dividers Design For Multi-GHz PLL Systems”, Georgia Institute of Technology, page 13-33, August. 2008