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Fully DSP-Based Control of an Active Voltage Conditioner

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Abstract

One of the main problems in low voltage (LV) networks is related to sensitive load voltage stabilization close to the nominal value. This paper presents the analysis, design, and implementation of a back-to-back converter based active voltage conditioner for low voltage (LV) distribution grids to compensate short-term voltage sags or swells. The proposed voltage regulator contains an indirect AC/DC/AC converter and uses linear control associated with the pulse width modulation technique. To verify the practical usefulness of the proposed novel concept, a 5kVA three-phase prototype active voltage conditioner has been constructed, and the control system has been implemented based on 32-bit floating-point digital signal processor (DSP) TMS320F28377s. The effectiveness of the proposed method is demonstrated through the comprehensive experimental results.

Keywords: Active voltage conditioner, digital signal processor (DSP), voltage stabilization

1. Introduction

The voltage oscillations such as concavity due to earth fault of 1 phase have the proportion of 68% and 19%, 13% is corresponding with 2-phase, 3-phase in a short period of time (a few grid periods up to tens of seconds). These oscillations will cause damage and interrupt some electrical and electronic equipment. If these equipment play important roles, the entire production line may be stopped. In addition, if the load is the data processing system, it can result in disruption or information losses, which can also have serious consequences. Active Voltage Conditioner (AVC) is the most appropriate solution to overcome voltage oscillations problem in low voltage grid [1-3]. The AVC system consists of a grid-side converter (Shunt converter) and a load-side converter (Series converter) connected via a DC circuit, and a transformer connected in series between the load, source. The diagram of AVC is shown in Fig. 1. In that, the load-side converter uses a 3-bridge common DC voltage diagram to compensate voltage fluctuation for each phase, the grid-side converter is a 3-phase voltage source inverter operating in active rectifier mode that allows bidirectional energy exchange between the grid and the DC circuit to compensate voltage sag and swell.

The control system for the active voltage conditioner is divided into two parts: the active rectifier control is implemented based on the grid-voltage oriented vector principle [4], the control part of the load-side converter uses scalar control principle for each H-bridge circuit to ensure creating 120-degree-difference phase voltages exactly according to [5-7]. These control structures have also been implemented on the DSP (digital signal processor) card of Texas Instrument, which shows a good and reliable dynamic response for grid voltage fluctuations. However, these works have not indicated how to simultaneously integrate control structures using DSP for 3-phase active voltage conditioner, including control structures for the grid-side converter and load-side converter. Therefore, this paper will propose the active voltage conditioner control system including regulator digitization, DSP resource, and working time frame allocation. In this system, each DSP will take on a control structure and the DSPs will link together through CAN communication standard, so the active voltage conditioner control system will be more reliable and upgradeable.

2. Active Voltage Conditioner Control Structure

The control structure of the grid-side converter is designed on a closed synchronous system dq^+ and dq^- oriented to the grid voltage. Grid-side converter control consists of two current loops and a DC-voltage loop. DC voltage controller is used to stabilize the voltage on the capacitor and regulate the reference values for current controllers. The current loops control both the positive and negative sequence components, the value of this current component is calculated based on the grid voltage phase angle according to the phase-locked loop algorithm, combined with the decoupled double synchronous reference frame (decoupled double synchronous reference frame phase-locked loop - DDSRF PLL). PI controller parameters for the current loop circuit are designed in the frequency domain considering the model of the LCL filter circuit and the control system delay, the parameters of PI controller for the DC loop circuit are designed according to the characteristics of the quadratic oscillator [4].

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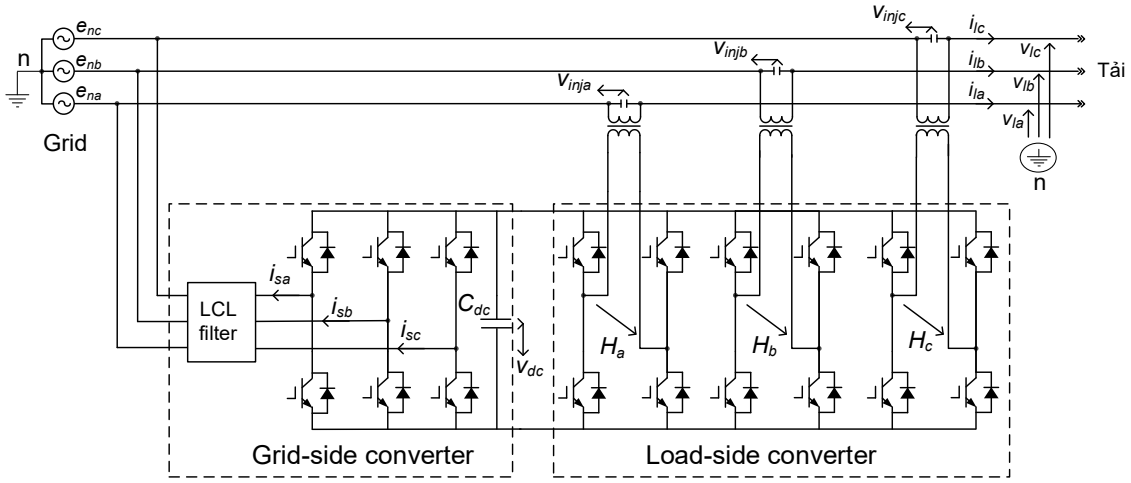


Fig. 1. Three-phase AVC diagram

The control structure for the load-side converter implements the principle of scalar control for each H-bridge circuit in voltage mode, the PR controller is used to eliminate static deviations for the voltage loops. The PR controller parameters for the voltage loop are designed in the frequency domain based on the desired phase margin (PM) and magnitude (GM). The reference values of the voltage loops are calculated based on the difference between the desired r.m.s.voltage value (for example 220 Vac) and the r.m.s. voltage of the grid. In addition, the SOGI PLL algorithm (Second-order generalized integrator based phase-locked loops) is used to synchronize each of the grid voltage phases [5].

Equivalent circuits converted to the secondary side of transformer are determined according to (1):

$$Z_{eqS} = \left(\frac{r_p}{N^2} + r_s\right) + j\left(\frac{x_{\sigma p}}{N^2} + x_{\sigma s}\right) = R + j\omega_1 L_\sigma, \quad (1)$$

where: N is the ratio of the transformer, r_p and r_s are the internal resistance of the primary and secondary winding, x_p and x_s are the primary and secondary dissipation reactance. The transfer function of the voltage needed to be compensated and the modulation coefficient for each phase is determined according to (2).

$$G_{mv}(s) = \frac{v_{inja}(s)}{m_a(s)} = \frac{1}{N^2}\frac{V_{dc}}{s^2 L_\sigma C + sRC + 1}. \quad (2)$$

The PR controller has a resonant frequency same with the grid voltage fundamental frequency ω_1, so the PR transfer function has the following form:

$$G_{PR}^c(s) = k_{pr} + \frac{k_r s}{s^2 + (\omega_1)^2} \quad (3)$$

The cutoff frequency ω_c (selected in a range of 500Hz ÷ 600Hz) is 10 times larger than the fundamental frequency (50Hz), then the PR controller magnitude at the cutoff frequency approximately equals to k_p, and the coefficient k_p is obtained:

$$\left|G_{PR}^c(j\omega)\right|_{\omega=\omega_c}\left|G_{mv}(j\omega)\right|_{\omega=\omega_c} = 1$$
$$\rightarrow k_{pr} \approx \frac{1}{\left|G_{iv}(j\omega)\right|_{\omega=\omega_c}} \quad (4)$$

Coefficient k_r is determined based on the selected phase margin (30º ÷ 60 to choose from) and is calculated by (5).

$$k_r = \frac{\tan(A_c)\,k_p\left(\omega_1^2 - \omega_c^2\right)}{\omega_c} \quad (5)$$

where: $A_c = PM_c - \left[G_{mv}(j\omega)\big|_{\omega=\omega_C} + 180^0\right]$

To implement in the microcontroller, the Laplace operators in the regulators need to be approximated to the Z domain to obtain the differential equations [5,6]. The PR regulator needs to consider delay when installed on the DSP (at least one sampling cycle), the PR regulator transfer function is rewritten in (6).

$$G_{PR}^c(s) = k_{pr} + k_r\frac{\cos(\theta_d)s - \omega_1\sin(\theta_d)}{s^2 + (\omega_1)^2} \quad (6)$$

where: $\theta_d = \omega_1 N T_s$ (N is an integer and is chosen to be 1), T_s – sampling period of PR regulator, h – harmonic order).

The PR regulator is rewritten in Z domain as (7).

$$G_{PR}^d(z) \approx k_{pr} + k_r T_s\frac{-\cos\theta_d + \left(\cos\theta_d - \omega_1 T_{s\_PR}\sin\theta_d\right)z}{z^2 + \left(\omega_1^2 T_{s\_PR}^2 - 2\right)z + 1} \quad (7)$$

In the grid-side converter control structure, the PI controller is discretized by the Tustin method [9].

$$G_{PI}^d(z) \approx k_{p\_PI} + k_{i\_PI}\frac{T_{s\_PI}}{2}\left(\frac{z+1}{z-1}\right) \quad (8)$$

DSP digital signal processors are known as special microcontrollers with the capability of

executing control algorithms that require high computational volume, with very high accuracy and speed.

Developed for power electronic converter control fields for a wide range of applications, the DSP TMS320F28377s is a 32-bit static comma microcontroller of the new C2000 family of Texas Instruments. This microcontroller series allows operation with quartz frequency up to 200MHz, in addition, the 32-bit floating point arithmetic engine called CLA (Control Law Accelerator) for computational processing is integrated on the microcontroller, to execute the control algorithm in parallel with performing other tasks on CPU. From the architecture of this TMS320F28377s DSP series, 2 control structures for the grid-side and load-side converter are implemented on each DSP and the DSPs are linked via CAN communication in Fig. 2. CAN communication is highly stable due to message detection and error handling, the possibility that a message will not be detected is very low (4,7.10^{-11} baud rate). Communication using differential signal transmission has reduced the impact of electromagnetism, besides, using only 2 wires on the transmission line makes the pairing system simpler and safer.

Fig. 3 shows the program structure diagram on the DSP for the grid-side converter. DSP uses 3 PWM channels including channels PWM6, PWM7, PWM8 to control the IGBT of the power circuit. Grid-side currents i_{sa}, i_{sb}, i_{sc} are measured by current sensors of LEM company, phase grid voltages e_{na}, e_{nb}, e_{nc} and DC voltage are passed through the measuring circuit, then sent to ADC channels A0, A1, A2 A3, B0, B1, B2 of DSP for signal reading. In addition, the DSP uses GPIO 63 and GPIO 64 to control the capacitor charge circuit during the start-up for the grid-side converter, the GPIO 72 and GPIO 73 are used for CAN communication function to connect to Master.

In DSP, 2 CPU and ClA cores are implemented parallelly. The CPU has to initialize ADC, PWM, CLA, CAN peripherals and the system's data acquisition and monitoring operations are also performed in CPU. The CLA performs ADC reading, executes control loops, phase-locked loop block and updates the modulation coefficient value for the register of PWM 6, PWM 7, PWM 8.

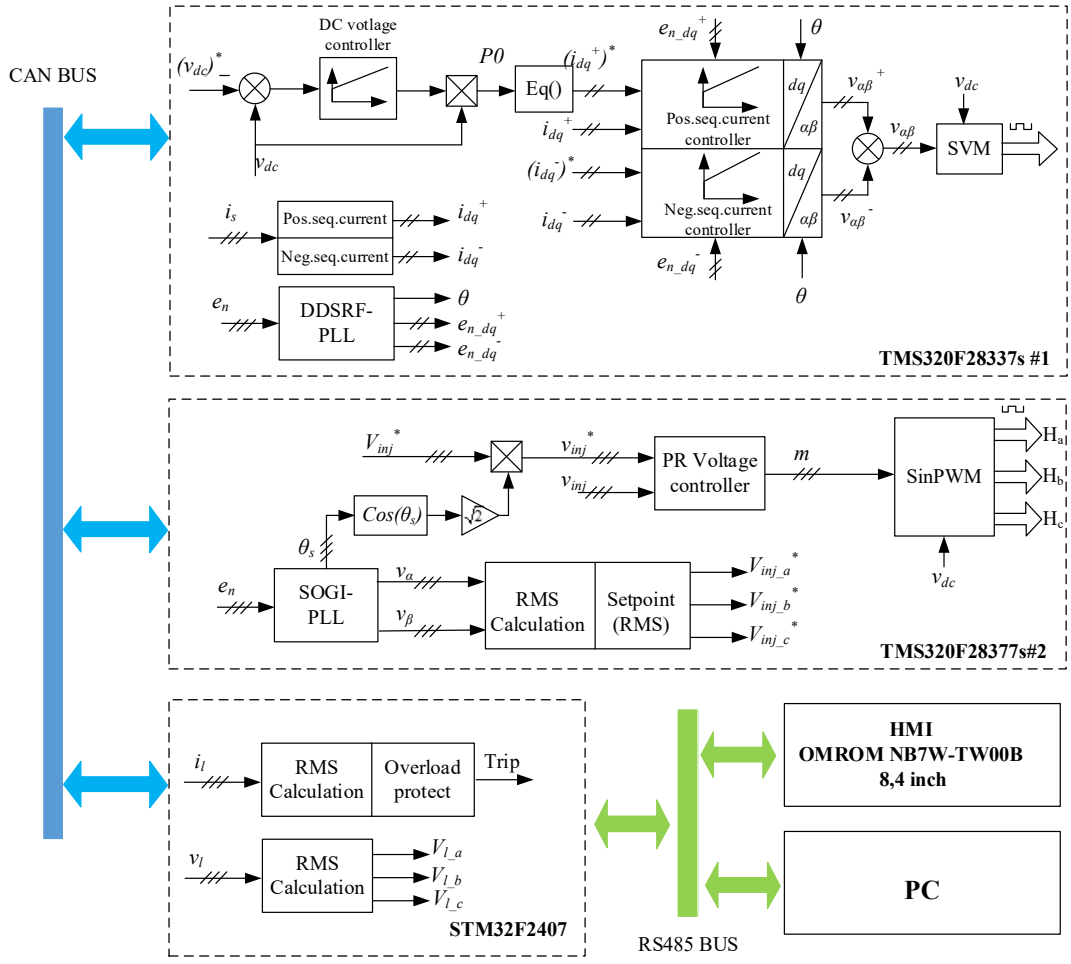


Fig. 2. Active voltage conditioner (AVC) control structure using 2 DSPs linked via CAN communication

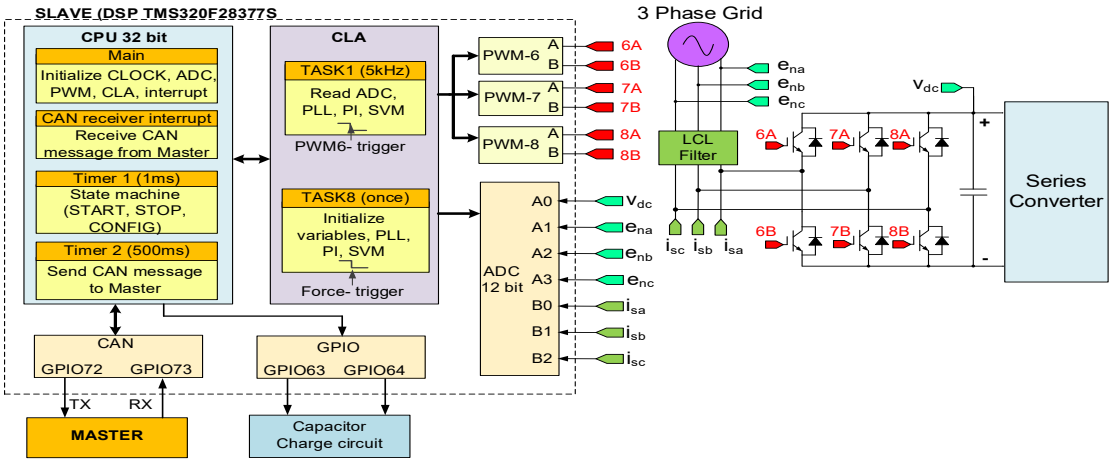


Fig. 3. Program structure on DSP for Shunt Converter.

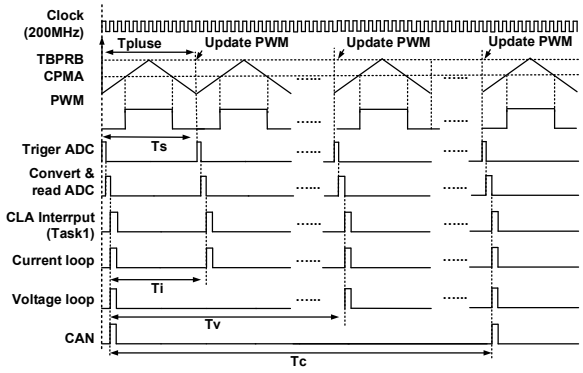


Fig. 4. Time frame on DSP for Shunt Converter

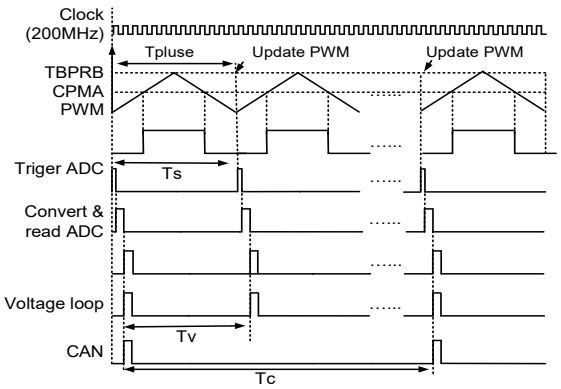


Fig. 5. Time frame on DSP for Series Converter

The program timeframe on the DSP for the grid-side converter is depicted in Fig. 4. The PWM channel (PWM6) generates pulses at 5kHz, which produces an ADC trigger event when PWM counter is zero. ADC channels A0, A1, A2, A3, B0, B1, B2 convert analog signals (v_{dc}, e_{na}, e_{nb}, e_{nc}, i_{sa}, i_{sb}, i_{sc}) to digital signals. At the end of the ADC conversion, an event is used to trigger the program in the CLA interrupt (task1). In CLA interrupt, current controller is executed with a sampling cycle (T_i), which equals to the pulse generator cycle (T_{pulse}) - 200 µs, voltage controller on DC capacitor is executed with sampling cycle (T_v) which is 10 times the current controller sampling cycle - 2 ms. After finishing the computation in CLA, the modulation coefficient is updated to registers of PWM6, PWM7, and PWM8. In the CPU, the DSP transmits the CAN messages to the BUS with a cycle (T_c) of 500 ms. Received CAN messages are executed in CAN received interrupt routine.

Fig. 6 shows the program structure diagram on the DSP for load-side converter. The DSP uses 6 PWM channels including PWM6 and PWM7, PWM8 and PWM9, PWM10 and PWM11 to generate pulses that control the IGBT, respectively for H_a phase, H_b phase, and H_c phase. Three-phase grid voltages e_{na}, e_{nb}, e_{nc}, three compensated voltages v_{inja}, v_{injb}, v_{injc} and DC voltage v_{dc} are passed through the measuring circuit, then fed to ADC channels A0, A1, A2, A3, B0, B1, B2 of DSP for signals reading. GPIO 72 and GPIO 73 are used for CAN communication function to connect the slave to Master. Similar to grid-side converter, DSP uses 2 CPU and CLA implemented parallelly.

The program timeframe on the DSP for the load-side converter is illustrated in Fig. 5. The PWM channel (PWM6) generates pulses at 5kHz which produces an ADC trigger event when the PWM counter is zero. ADC Channels A0, A1, A2, A3, B0, B1, B2 convert analog signals (v_{dc}, e_{na}, e_{nb}, e_{nc}, v_{inja}, v_{injb}, v_{injc}) to digital signals. At the end of the ADC conversion, an event is used to trigger the program in the CLA interrupt (task1). In CLA interrupt, the voltage controller is executed with sampling cycle (T_v), which equals to pulse generator cycle (T_{pulse}) - 200 µs. After finishing the computation in CLA, the modulation coefficient is updated to registers of PWM 6, PWM7, PWM8, PWM9, PWM10 and PWM11. For communications, CAN message from Slave circuit of Series converter are also transmitted with the same cycle as Shunt converter (Tc) - 500 ms.

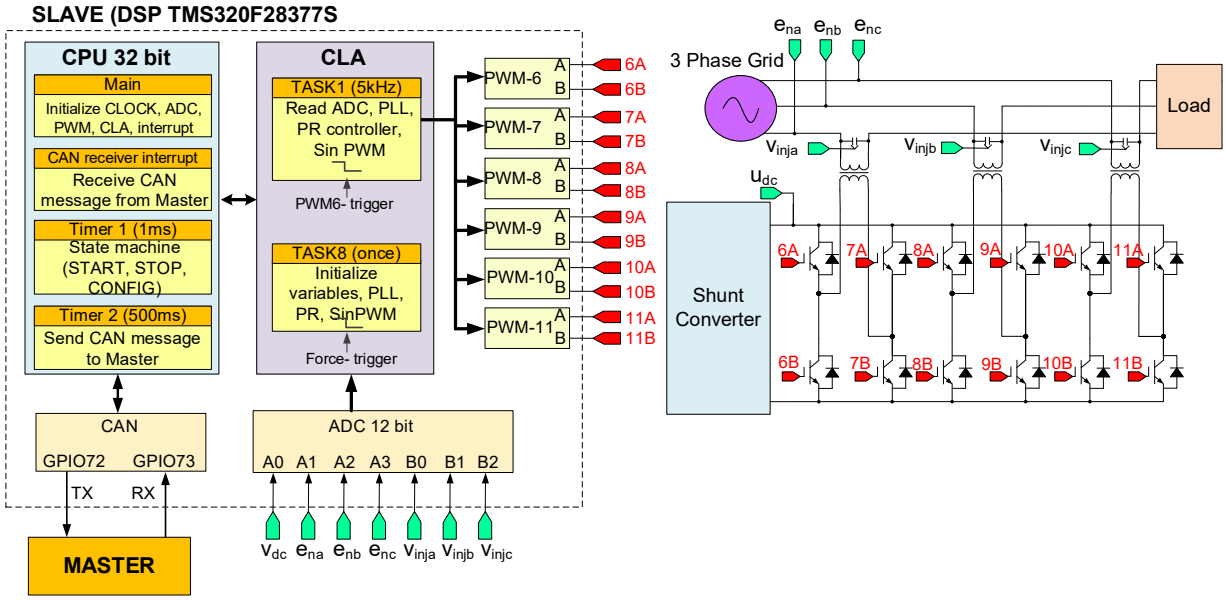


Fig. 6. Program structure on DSP for Series Converter

3. Experimental Model and Result

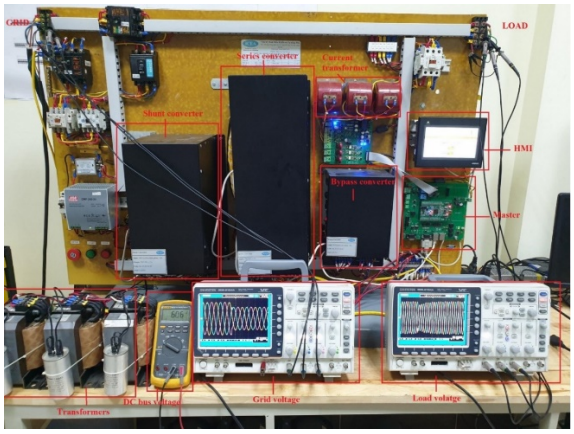
Parameters in the active voltage conditioner with a power of 5 kVA are shown in Table 1.

Table 1. Experimental parameters [8]

Grid-side and load-side converter	
IGBT	IGBT SKM75GB176D
Driver	IC HCPL316J
Current measurement	Current transducer LEM LA55-P/SP1
Isolated IC for voltage measurement	IC HCPL7800A
Control card	DSP TMS320F28377s launchpad
Transformer parameters	Power: 4.5kVA Turns ratio: 2:1
Control center	
Load current measurement	IC ACS712 5A Current Transformer 50A/5A
Isolated IC for voltage measurement	IC HCPL7800A
Control and data acquisition card	Kit STM32F407 Discovery

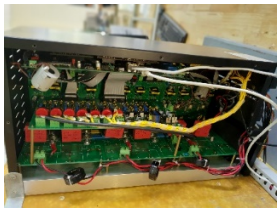
Voltage sag can be created by generating a three-phase or two-phase or 1-phase short circuit via resistors, the short-circuit resistance and reactance are calculated. The system voltage will be dropped due to the power limitation of the 5 kVA isolated transformer located at source-side. The voltage drop value varies based on the resistance adjustment of each phase, in the range of 0 - 10 Ω.

AVC control system is designed according to MASTER - SLAVE structure, connected by CAN communication. In this structure SLAVE is the TMS320F28377S DSP signal microprocessors which execute control structures for each grid-side and load-side converter as shown in Fig. 2. MASTER is a digital microprocessor, The STM32F407 Discovery Kit signal collects data to display and command control signals for the SLAVE.



a) Experimental model AVC 5kVA.

b) Grid-side converter



c) Load-side converter

Fig. 7. Active voltage conditioner 5kVA.

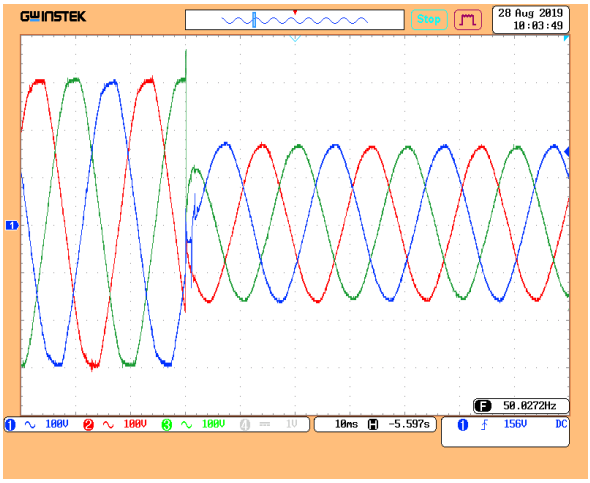
Monitoring and data collection level MASTER solves control problems, such as setting parameters for regulators, setting operating modes to allow AVC to compensate voltage sag and swell when the grid voltage is not within the range from 90% ÷ 110% of the nominal value, measure the load current to determine the overload protection for the system, collect and display data on HMI.

The AVC is tested with 3 cases of voltage sag. In all cases, the DC voltage remains the same at 600 Vdc.

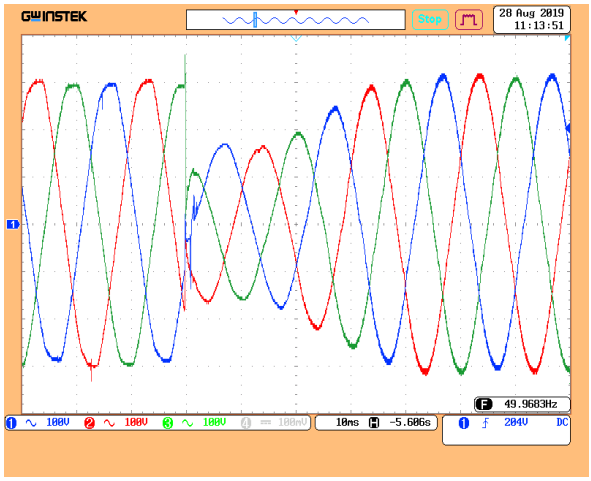
Case 1: 3-phase voltage sag, each phase voltage has r.m.s.value before being sagged is 226.2 V; 225.3 V; 225.7 V, respectively. The system creates all 3-phases sag simultaneously in 10 seconds with corresponding values for each phase 134.9 V; 135.1 V; 135.2 V. When the AVC system operates, the load voltage is restored to 224.4 V; 224.7 V; 225.7 V. The maximum recovery voltage deviation is 0.8%, the voltage recovery time is 40 (ms).

Case 2: 1-phase voltage sag, the voltage of each phase has r.m.s.value before being sagged is 225.3 V; 224.4 V; 224.8 V, respectively. The system creates a voltage sag of phase A, reduces the voltage to 101.6 V in 10 seconds, voltage of phase B and phase C remain unchanged. When the AVC system operates, the A-phase load voltage is restored to 225.7 V. The maximum recovery voltage deviation is 0.18%, the voltage recovery time is 40 (ms).

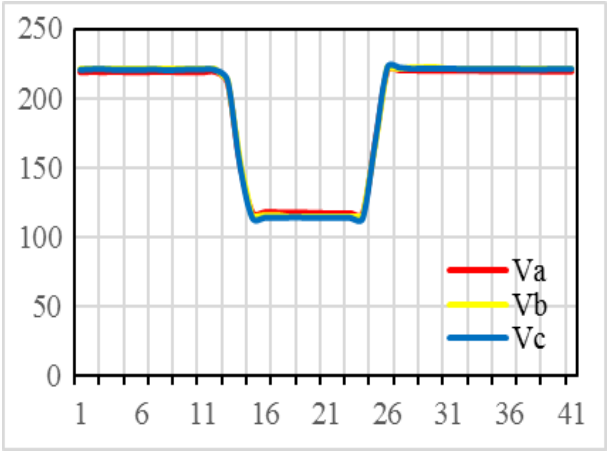
Case 3: 3-phase voltage swell, the voltage of each phase has r.m.s. value before being increased is 225.3 V; 224.8 V; 224.4 V, respectively. Autotransformer increases voltage values to 258.1 V; 257.7 V; 258 V in 10 seconds. When the AVC system operates, the load voltage is restored to 225.3 V; 225.3 V; 224.9 V.



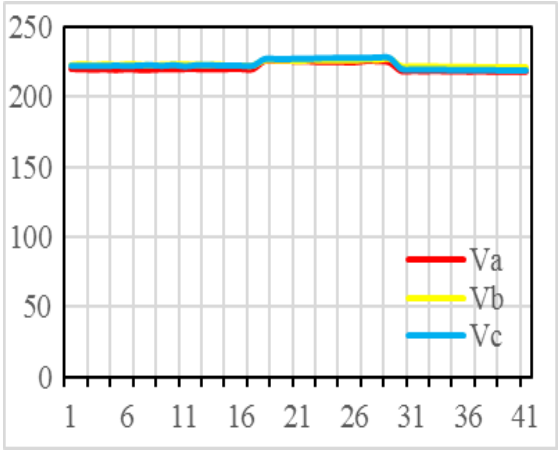
a) Grid voltage (100V/div, 10ms/div)



b) Load voltage (100V/div, 10ms/div)

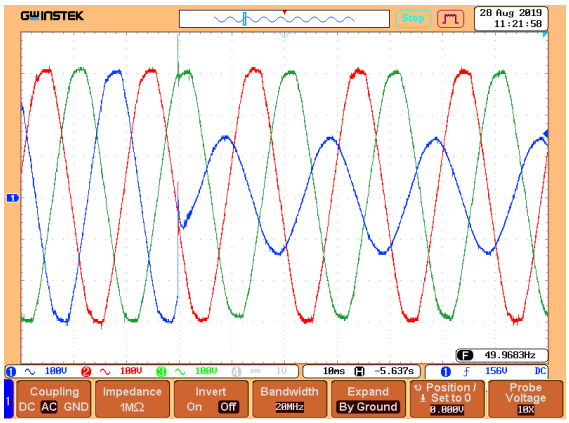


c) R.m.s. value of grid voltage measured by CW140.

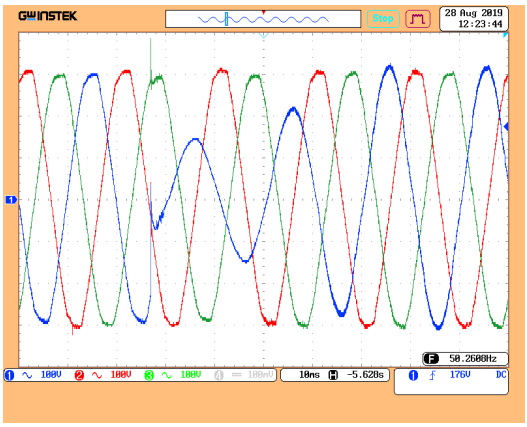


d) R.m.s. value of load voltage measured by CW140.

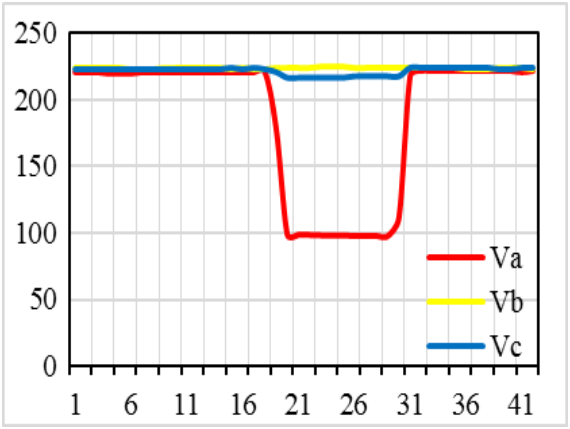
Fig. 8. Grid voltage and load voltage in case of 3-phase voltage sag.



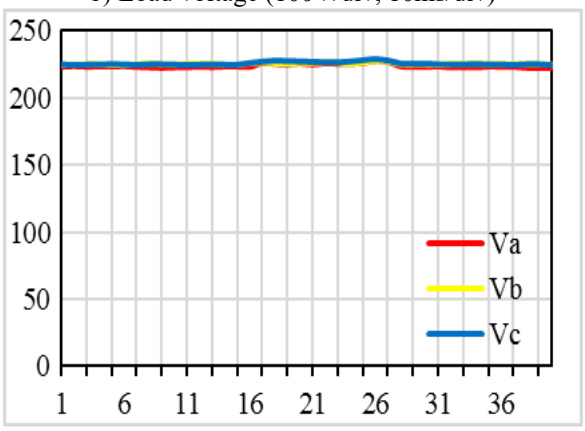
a) Grid voltage (100V/div, 10ms/div)



b) Load voltage (100V/div, 10ms/div)

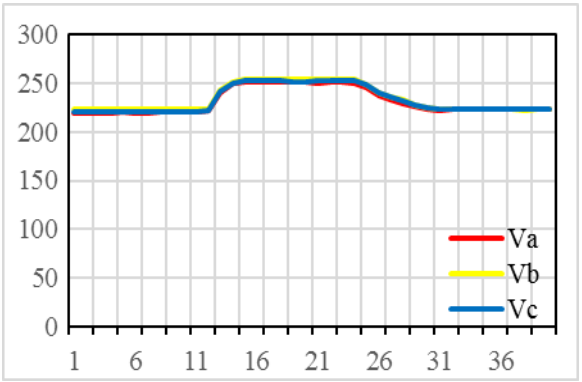


c) R.m.s. value of grid voltage measured by CW140.

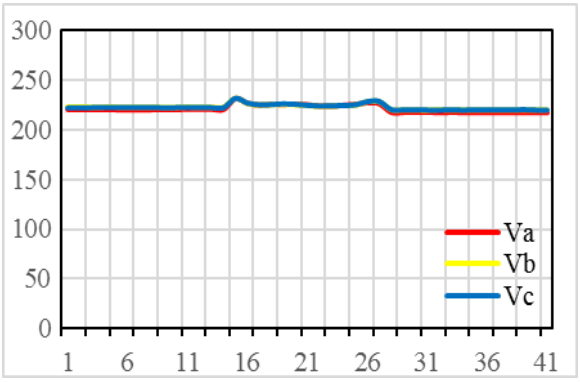


d) R.m.s. value of load voltage measured by CW140.

Fig. 9. Grid voltage and load voltage in case of 1-phase voltage sag.



a) Grid voltage



b) Load voltage

Fig. 10. R.m.s. value of voltage measured by CW140 in case of 3-phase voltage swell.

4. Conclusion

The paper has presented a three-phase active voltage conditioner structure that is capable of stabilizing the load voltage when the grid voltage fluctuates. The control and communication system of the active voltage conditioner is fully implemented by digital signal processing DSP. The results show that the load voltage can be steadily adjusted to follow the rated value within two grid voltage cycles, the deviation of voltage less than 1%.

Acknowledgements

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