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Batch Furnace Chemical Vapor Deposition of Pure Boron Layers on Si and GaN Substrates for Low-Leakage-Current Diode Fabrication

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Abstract

Boron deposition on both n-Si and n-GaN in the temperature range 250 - 500 °C, has been shown to form diodes with low saturation currents, i.e., electron injection from the n-substrate into the B-layer was efficiently suppressed. Moreover, down to 3-nm-thick B-layers on Si were shown to form a material barrier to Al, opening the possibility of fabricating Au-free gates for gallium-nitride high-electron-mobility transistors (GaN HEMTs). Several different chemical- and physical-vapor deposition (CVD/PVD) methods for depositing B have been studied for fabricating p^+n-like Si diodes, called PureB diodes, all with comparable results. In this paper, the deposition of B-layers from diborane in a CVD batch furnace system is evaluated, particularly for use as a barrier material to enable Al-contacting of GaN diodes. These Al-B diodes could provide an option for fabricating low-leakage diodes that are compatible with complementary metal-oxide-semiconductor (CMOS) processing at industrially attractive high throughput. The bulk B has high resistivity, which, combined with the fact that non-uniformities in the nm range, are typical due to gas depletion along the furnace tube and gives uncontrollable, often high diode series resistance. A simulation study shows that Al-B could, nevertheless, be used as a gate stack in HEMTs for low-frequency power applications.

Keywords: Boron, gallium-nitride, silicon, chemical vapor deposition, diodes, HEMTs, gate resistance.

1. Introduction

In this paper, first experiments are presented for the use of chemical vapor deposition (CVD) to deposit boron layers on n-GaN substrates as a material barrier for the fabrication of stable aluminum-contacted diodes. Investigations of such Al-B GaN diodes were motivated by the unique B-layer properties revealed by PureB silicon technology research [1, 2] where nm-thin boron films were deposited on Si by either CVD or physical vapor deposition (PVD). For the first, at temperatures from 250 to 500 °C, where no significant bulk B-doping of Si is expected, p^+n-like diodes were formed with low saturation currents, i.e., electron injection from the n-substrate into the B-layer was efficiently suppressed. A similar beneficial bonding of B to GaN substrate surfaces was not directly expected, but a second exceptional property was of particular interest: B-layers on Si displayed excellent robustness and stability, both chemically and optoelectrically [2, 3]. These properties led to rapid commercialization of PureB Si photodiode detectors for extreme ultraviolet lithography (EUV) instrumentation and advanced electron microscopy systems.

The electrical properties of PureB Si diodes have been studied using the simple process flow illustrated in Fig. 1. In the last 2 steps, the Al is removed in the diode center for application as a photodiode [4]. The p-region formed by the B-layer has a high Gummel number that can be reached only in bulk deep-diffused junctions with depths greater than about 100 nm [5]. In contrast, PureB diodes can have a metallurgic junction depth as low as zero because the p-type region is formed by very stable negatively-charged B-Si bonds at the interface [6]. This fixed negative charge attracts holes to the interface at a concentration far beyond what could be achieved by bulk doping, so a high electric field repels electrons from the contact, resulting in very low saturation currents.

Several different CVD and PVD methods were investigated for the B deposition on Si, including batch furnace CVD. For B-layers processed around 400 °C, the PureB diodes had almost identical electrical characteristics in terms of electron saturation current density and sheet resistance of the hole layer formed at the B-Si interface. This is seen in Fig. 2, where these parameters are compared for all deposition methods. The best experimental values are shown for (a) the electron saturation current density, J_{se}, and (b) sheet resistance, R_{SH}, as a function of deposition/anneal

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temperature, for PureB diodes with B-layers fabricated in single-wafer CVD, batch furnace LPCVD/ULPCVD, molecular beam epitaxy (MBE) and EBPVD deposition systems; ring-shaped diodes with A = 0.21 mm^2 [7].

All in all, the PureB Si diode research has been very focused on studying tunnel-thickness layers, i.e., effectively less than ~3 nm thick when metalized. The main reason for this is that the resistivity of the amorphous boron itself is very high with values from about 1 to 10 kΩ-cm [8]. In the literature, other CVD layers of B have been reported to be semiconductors with p-type doping in the 10^{16} - 10^{18} cm^3 range [9, 10], with the amorphous nature of the films resulting in very low lifetimes and mobilities.

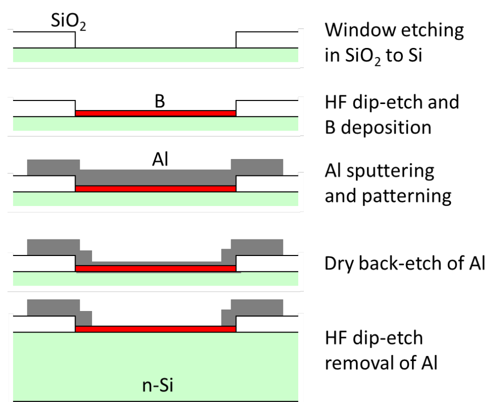


Fig. 1. Basic PureB Si diode process flow using aluminum as anode metallization

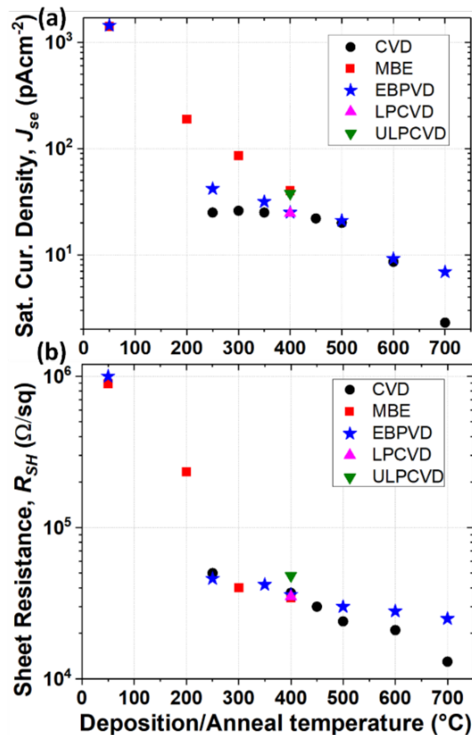


Fig. 2. Comparison of B-Si junctions fabricated by different deposition methods.

Of particular interest for GaN devices was the fact that the chemical resilience of B-layers included their successful application as a material barrier to metals such as Al, Au, and Cu [11] even for layers as thin as 3 nm. Thus, there was an opportunity to replace Ni-Au with Al-B gates in GaN HEMTs to achieve better complementary metal-oxide-semiconductor (CMOS) compatibility and long-term reliability [12, 13]. In addition, the high Schottky diode current levels diminish the useful operating range of high-electron-mobility transistors (HEMTs). Extensive research has therefore been directed towards the development of metal-insulator-semiconductor (MIS) gates using dielectrics such as Al_2O_3 and SiN_x [14]. However, the quality of these layers is not comparable to that of oxides used in CMOS processing, and dielectric thickness in the 20 - 30 nm range must often be used to reach useful breakdown voltages. The additional gate series capacitance reduces the transconductance, g_m, of the HEMT, so in high-speed microwave HEMTs, thinner dielectrics are used, and some level of gate leakage must be tolerated [15].

An additional concern when using MIS gates is the stability of the dielectrics and their interface with the GaN. Upon electrical stress, traps can be created and cause bias-sweep dependent pinch-off voltage, V_P. In PureB Si photodiodes such instability has not been observed. This was in contrast to devices with dielectric surface layers, where traps formed at/near the interface with the Si due to exposure to radiation or electrical stress, would in fact degrade optical responsivity and increase leakage currents [16].

Earlier experiments with B-layers deposited on GaN by MBE confirmed that it was indeed a barrier to Al metallization [17]. In addition, the fabricated Al-B GaN diodes displayed very low saturation currents, decades lower than Al Schottky diodes. For use as HEMT gates, the Al-B diodes can be seen as an intermediate between high-current Schottky and insulating MIS gates. The B-layer reduces the otherwise high Schottky currents by decades, resulting in a low-saturation-current diode. While the B is not insulating, it does have very high resistivity, the effect of which is evaluated here through simulations.

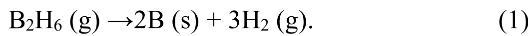
In PureB Si research, the focus has mainly been on B deposition by CVD in commercial single-wafer reactors, where very well-controlled nm-thin layers can be grown. Here we experiment with batch furnace CVD because it is more accessible for research on non-Si, odd-sized substrates like our 3×3 cm^2 GaN samples. Moreover, there was interest in the development of a tool that would be of importance to industry as it is suitable for high throughput production.

2. Batch Furnace CVD Boron Deposition

A batch furnace dedicated ultra-low-pressure CVD (ULPCVD) system was developed for the

deposition of B on Si. As described in [18], this was done by modifying a low-pressure CVD (LPCVD) system with a connection to a turbopump. The precursor was 5% diborane (B_2H_6) which was diluted in argon (Ar) as carrier gas. With the turbopump, a chamber pressure as low as 10^{-7} mbar could be reached, which minimized contamination by oxygen and water introduced with the wafers. During deposition, the working pressure was kept at 0.0013 mbar. As illustrated in Fig. 3, the wafers were loaded into a 28 cm-long quartz boat. Deposition temperatures from 300 to 450 °C were studied, and gas depletion across the wafers was found to be the major source of non-uniformity from wafer to wafer. On a single wafer, about 10% higher B thickness was found at the wafer edge as compared to the center.

The overall chemical reaction is:



$$B_2H_6\ (g) \rightarrow 2B\ (s) + 3H_2\ (g). \qquad (1)$$

where the gas and solid phases are denoted by (g) and (s), respectively. Prior to loading into the CVD system, the Si substrates were cleaned with 1% hydrofluoric (HF) acid to remove the native oxide and achieve H-passivation of the Si surface. This prevented native oxide regrowth during transport of the samples and the system stabilization before deposition. The system was then pumped down to the 10^{-5} to 10^{-6} mbar range, followed by temperature stabilization in N_2 at a pressure of 1 mbar to bring the sample temperature to the set point more quickly. After this, the system was again pumped down and the B_2H_6 flow was turned on.

The adsorption of B is hampered by any H attached to the Si surface, which, inopportunely, does not readily desorb at temperatures below 500 °C. Accordingly, the incubation time was found to vary considerably. For example, great B-thickness variations were seen for stabilization times varying from 30 min to 1 h. Prolonged stabilization time is not desirable because it increases the risk of oxygen contamination. A stabilization time of 1 h was used and several samples deposited from 300 to 400 °C were analyzed by X-ray photoelectron spectroscopy (XPS). For all samples, the oxygen content was very low, in the 0.5% to 2% range, with no clear peak at the Si surface. Moreover, with 1 h stabilization, the layer thickness was proportional to the deposition time, confirming that the sample temperature was stabilized after this time.

In the Si experiments, patterned wafers with windows to the Si through an oxide isolation layer were used. On such patterned wafers, the thickness of the B-layer would presumably be more uniform because the deposition on thermal oxide has a much longer incubation time, i.e., nucleation centers for B-adsorption are largely absent [19]. Therefore, gas depletion, which is responsible for thickness non-uniformity, is reduced.

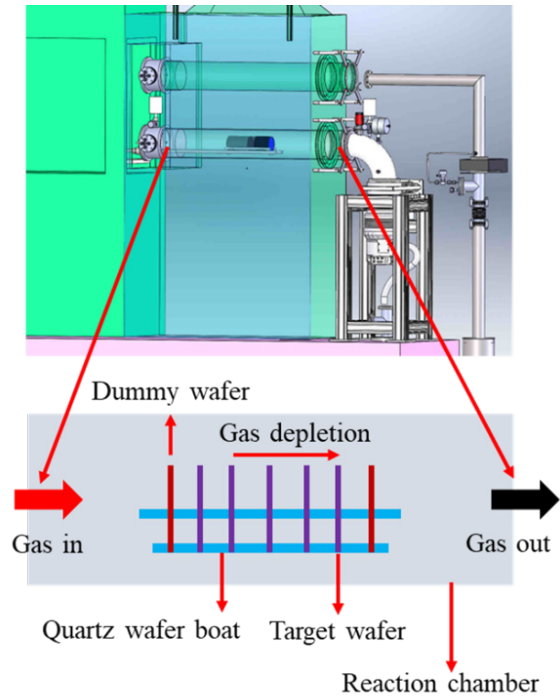


Fig. 3. Schematic of ULPCVD system.

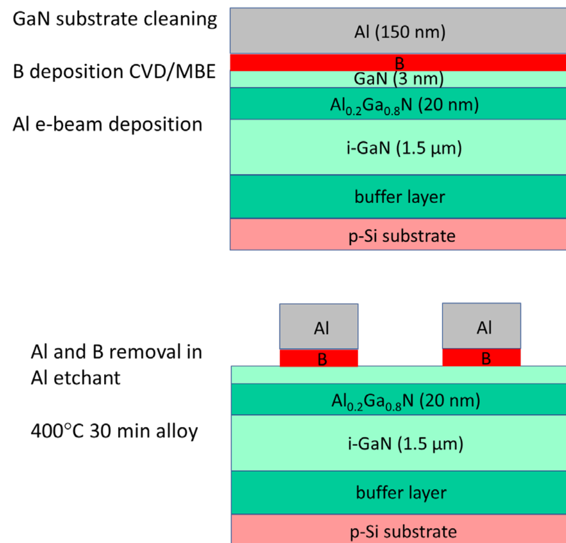


Fig. 4. Basic process flow for fabricating GaN diodes with Al-B contacting.

On Si substrates, the thickness of the B-layer could be determined by spectroscopic ellipsometry (SE) [2]. This was not possible on GaN substrates because, as shown in Fig. 4, wafers with an AlGaN layer were used, which makes the interpretation of SE measurements difficult. Therefore, a non-patterned Si sample was processed in addition to the GaN samples, and the B-thickness extracted from Si SE was used as the target value for GaN deposition. The incubation time on GaN could also not be determined in these initial experiments, but it was suspected that it might be

longer so that the B-layer would be thinner than the target value.

The gas depletion effect and poorly controlled incubation time meant that the nm-thin layers often desired for diode fabrication could not be fabricated reliably. Adsorption of B on the glass furnace tube is also expected to negatively affect reproducibility by increasing gas depletion. In such hot-wall systems, even though B does not readily deposit on high-quality SiO_2, B deposition on even a scant distribution of nucleation centers can lead to B-coverage that promotes further adsorption. Therefore, using a much lower B_2H_6 partial pressure than was possible in our system would be preferable.

3. Al-B GaN Diodes

The first GaN diodes with Al-B anodes were fabricated using MBE B-layers, as reported in [17]. The basic process, also used for CVD B deposition, is illustrated in Fig. 4. The substrates were diced from production-grade high-quality GaN-on-Si wafers. The buffer layer was covered with a stack of 1.5 µm intrinsic GaN, 20 nm $Al_{0.2}Ga_{0.8}N$, and a capping layer of only 3 nm GaN.

Before B deposition, the GaN substrates were ultrasonically cleaned in acetone and isopropyl alcohol for 5 min to remove any organic contaminants, and then given a dip in HNO_3:HCl (1:3) followed by rinsing in deionized water and blow drying with N_2. The B was deposited on non-patterned samples to avoid any processing of the virgin GaN that could modify the surface structure. A 7-nm-thick B-layer was deposited on each of the MBE samples at temperatures from 250 to 400 °C. For the CVD sample, a deposition temperature of 450 °C was used, and the target B-thickness was 10 nm. Contacts were processed by e-beam evaporation of 150 nm Al that was patterned by optical lithography and wet etching in Al etchant that also removed the B-layer. All samples were given a final 400 °C alloy for 30 min.

Compared to batch furnace CVD, and other CVD deposition techniques, the advantage of MBE and other e-beam or sputter techniques, is that the B is deposited from a source at a known rate. In this case, the source was a Knudsen effusion cell of elemental B and the base pressure in the deposition chamber was 10^{-11} mbar. Therefore, the B thickness was substrate independent and well-controlled, whereas with CVD it is strongly affected by system-/chemistry-dependent incubation times and growth rates. Moreover, with MBE but not with CVD, a substrate temperature as low as 50 °C could be used during deposition and the results showed that deposition/post-anneal temperatures of around 400 °C were beneficial for the Al-B GaN diode performance.

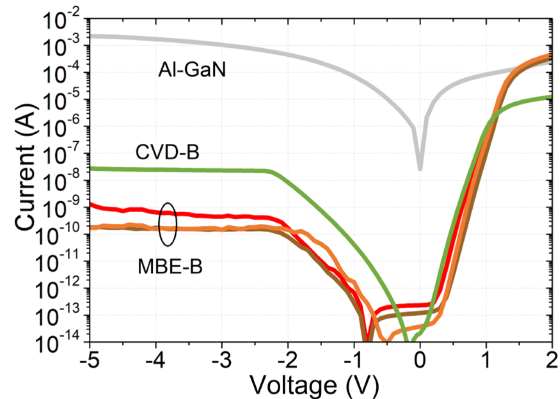


Fig. 5. Diode *I-V* characteristics for GaN diodes processed as shown in Fig. 4.

The resulting diode *I-V* characteristics are shown in Fig. 5, without B-layer, with CVD-B grown at 450 °C, and with MBE-B grown at substrate temperatures of 250 °C, 350 °C, and 400 °C. All diodes were given a final alloy for 30 min at 400 °C. Diode dots with a diameter = 200 µm. Measurements were performed by contacting the cathode at the back of the substrates to the chuck of a probe station. This resulted in a variable, quite high series resistance because the cathode current must flow along the sides of the sample and through the two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction to reach the n-region below the diode anode under test. The anode was directly contacted by a probe needle on the front side of the wafer. The high series resistance did not attenuate the diode current in the low voltage region where it is clear that B-layer devices have decades lower current levels than those of the Schottky diode formed by depositing Al directly on the GaN.

In the diode *I-V* characteristics, the V_P corresponds to the point where the reverse current saturates because the AlGaN and i-GaN layers become fully depleted [20]. For the present devices, the value of V_P is 2 V. The bias-sweep dependence of V_P was checked by performing several sweeps of V_g from negative to positive and vice versa. Apart from a small burn-in effect, there were no measurable shifts in V_P. Much more extensive stress measurements are, however, needed to truly assess the stability of the Al-B diodes.

4. Effects of B-layer Series Resistance in GaN Devices

The B-layer resistivity will vary with the deposition equipment and conditions used, but in PureB Si devices it was consistently found to be high. Therefore, to avoid a high, detrimental series resistance when the Si was contacted through a B-layer, tunneling thickness in the 2 - 3 nm range was implemented. Such thin B-layers were routinely incorporated in Si (photo)diodes with the desired robustness and low series resistance [1, 8].

On GaN, tunneling layers have not yet been demonstrated. For GaN diodes fabricated for high currents, it would clearly be important to limit the B-layer series resistance to values below those of the n-GaN contacts. Compared to Si, even state-of-the-art n-GaN contacts have high resistivity, in the 10^{-5} Ω-cm range which is 2 - 3 decades higher than common Si values. Currently, n-GaN contacts typically have a series resistance of about 1 Ω-mm. In comparison, each 1 nm of bulk B in a 1 µm × 1 mm diode, would represent a series resistance in the 10-100 Ω-mm range. This would therefore dominate and limit the current driving capability of the diode. For tunneling B-layers, the values measured on Si were about 0.1 Ω-mm. If such low values also prove valid on GaN, B may well prove to be an attractive material barrier also in GaN diodes.

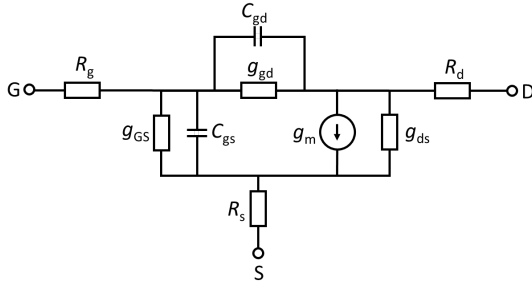


Fig. 6. Linearized small signal HEMT model.

In GaN HEMTs with an Al-B gate, the role of the gate series resistance, R_g, can be seen in the small-signal model shown in Fig. 6. Unlike the source and drain resistance, R_s and R_d, the R_g does not affect the drain current I_d directly, but only indirectly through the attenuation of the gate current, I_g. This occurs at high forward voltages where the voltage drop over the gate reduces the gate-source/-drain voltages, V_{gs}/V_{gd}. Consequently, g_m is reduced. In high-speed microwave HEMTs, the cut-off frequency, f_t, and maximum oscillation frequency, f_{max}, are the main figures of merit. They can be formulated in terms of the small signal components as:

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2}$$

$$f_{max} = \frac{f_t}{2\sqrt{(R_i + R_s + R_d)g_{ds} + (2f_t)R_g C_{gd}}} \tag{3}$$

where R_i is the charging resistance [21]. Therefore, the f_{max} is directly reduced by R_g, and thick B-layers would not be desirable in high-speed power HEMT applications.

In many other power HEMT applications, designed for low-frequency operation, a high R_g, does not limit performance. The effect on the transfer characteristics was explored by simulations in Synopsys Sentaurus Device [22] technology computer-aided design (TCAD) software. Results are shown in Fig. 7. It was assumed that the Al-B diode could be simulated as a Schottky diode with a high metal work function, Φ_M, in series with a resistor R_g representing the B-layer. The B-layer device is represented by Φ_M = 4.8 eV and R_g = 0 to 10 kΩ. Source and drain contacts were placed at the edges of the 2DEG with 2 µm separation to a 1-µm-long gate electrode with zero contact resistance. The experimental *I-V* diode characteristics were approximated by adjusting the tunneling mass and the distribution of generation-recombination centers at the interface in the gap between the gate and source/drain. In this way, a V_P and I_g very similar to the experimental values were obtained.

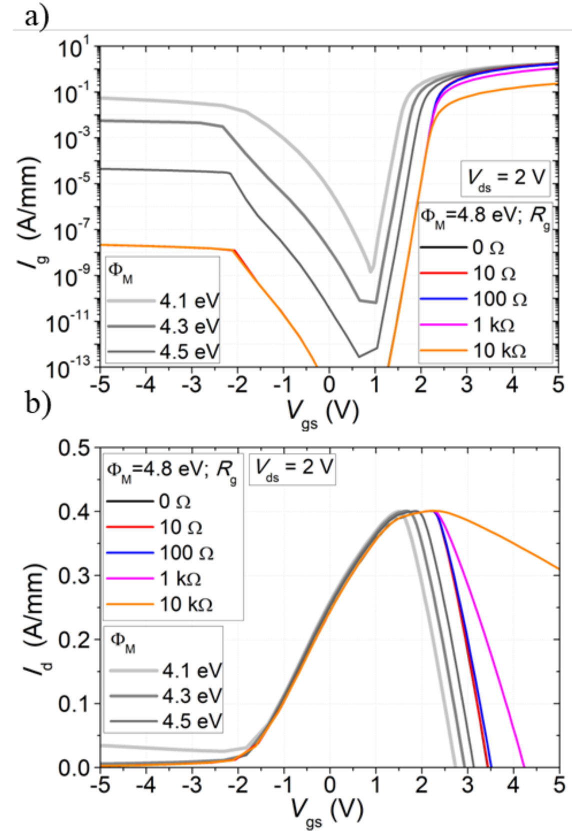


Fig. 7. HEMT simulations of gate diode *I-V* (a) and transfer (b) characteristics for V_{ds} = 2 V, and Φ_M = 4.1, 4.3, and 4.5 eV.

The simulated transfer characteristics confirm that R_g only has an effect when high forward current is flowing through the gate. The decades lower forward I_g in the B-layer diodes extends the region where I_d is at its maximum and, when R_g is increased, the fall-off of I_d is inhibited by the reduction of the intrinsic gate voltage.

5. Conclusion

These first experiments with CVD B-layers deposited as a material barrier in Al-contacted GaN diodes confirm earlier results with MBE layers that B cannot only prevent Al reactions with the GaN, but

also reduce the diode current levels by decades. However, in the batch furnace CVD system developed here, the deposition conditions entail long incubation times and significant gas depletion, resulting in nm-large non-uniformity of the B-layer thickness. Therefore, layers with tunneling thickness, necessary for low series resistance in Al-B GaN diodes, could not be grown reproducibly, and the presented diodes had several nm-thick B-layers. For use as gates in low-frequency power HEMT, simulations showed that the potentially high series resistance of Al-B gates could be acceptable and the advantages of a low-leakage, CMOS-compatible gate could be exploited.

Acknowledgments

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