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A Generalized Space Vector Modulation for Cascaded H-Bridge Inverters under Faulty Conditions

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Abstract

In this research, a new space vector modulation control algorithm is proposed to increase the reliability and the accuracy of the cascaded H-bridge multilevel inverters in case of faulty situations where one or several power cells do not function. When one or more switches of a cell are opened or shorted, that cell is considered faulty. By giving a detailed analysis on the impact of the faulty power cells on the voltage space vectors, the inapplicable voltage vectors are removed precisely. Consequently, the optimal redundant switching states are chosen such that the highest possible output voltage can be achieved. In addition, the balance of the three phases line-to-line voltage and current are maintained. The proposed algorithm is also generalized so that it can be applied to any level of H-bridge inverters. The validity of the method is verified by numerical simulations using MATLAB Simulink with an 11-level cascaded H-bridge inverter.

Keywords: Cascaded H-bridge inverter; space vector modulation (SVM); fault tolerant operation of CHB multilevel inverters

1. Introduction

Multi-level inverters have been widely used in industrial applications with high voltage range, large capacity due to following advantages: lower total harmonics distortion (THD) at output current/voltage waveform, lower voltage drop and stress on power switches, low *dv/dt* and high reliability since the faulty module can be bypass in several particular situation [1,2]... The topology of cascaded H-bridge multilevel inverter (CHB) is described in detail in [3-8]. In comparison with the diode - clamped topology, CHB-based inverter is more popular in industry due to its high modularization, as well as its ability to use the redundancy voltage vectors to solve the multi-objective optimization problem [9].

With a large number of power switches and complicated topology, modulation strategy for multi-level inverters is a challenge, especially when the number of levels is high. Among all modulation strategies, the space vector modulation (SVM), which has been widely used for conventional 3-phase inverters, can also be applied to CHB topology with the superior performance although high computational cost is required. By using SVM, the multiple-objectives problems such as: switching state optimization, load–source neutral voltage minimization, capacitor voltage balance, phase voltage balance can be implemented thoroughly by utilizing redundancy voltage vector [10-15]. Recently, thanks to the generalized SVM algorithm [16-20], the implementation of SVM for H-bridge inverter with any number of levels on digital control platform has become much easier.

As the number of levels is increased, e.g., in medium and high voltage applications, the possibility of malfunction caused by faulty power switches is unavoidable [9]. Normally, the inverter is disconnected from the line/load by the protection system, resulting in a sudden stop of motors which may cause other serious problems, e.g., water hammer in pump system. Besides, if the inverter continues to work under faulty conditions, the output voltage can be unbalanced, leading to motor failure after operating for a long period of time. Therefore, modulation strategy in faulty conditions to maintain proper operation of the inverter is a challenging issue.

The "bypass cell" method which bypasses the cell that contains the faulty switches is suggested in [21]. This method is quite simple, easy to implement, and can generate balance voltage between phases. However, the corresponding cells in the other phases must also be removed, leading to the reduction of the output voltage. To overcome this drawback, the neutral point shifting method has been proposed [22,23], in which, only the faulty cell is removed. As a result, the output voltage is usually larger than "bypass cell" method. Space vector modulation technique is also proposed in [24] and has the same performance as

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the neutral point shifting method. However, both methods are complicated, especially when the number of levels increases. Therefore, most researches are only based on inverters with limited levels.

In this research, an improvement of the generalized SVM method for the cascaded H-bridge multilevel inverter under faulty conditions is proposed. The proposed method guarantees that multiple-objectives such as: switching loss optimization, maximum output voltage, and output phase voltage balance can be achieved.

2. An Analysis on CHB under Fault Condition and Power Circuit Reconfiguration Method

2.1. CHB structure with bypass switches

The typical configuration of a CHB inverter with bypass switches is shown in Fig. 1. Each power module is called a cell. And the CHB inverter is formed by connecting multiple cells in cascade for each phase. Since each cell is equipped with a bypass switch, the faulty cells can be removed as illustrated in Fig. 2..

2.2. Output Voltage Effects under Fault

According to [5], the output voltage vectors of the CHB is arranged as shown in Fig. 3. When an error occurs, some switching combination is not possible because the relevant power cell is removed. The lack of switching combination makes some voltage vectors cannot be implemented, forming a layer of faulty space voltage vectors.

Fig. 4 depicts some typical examples of space vectors when one or more cells of the CHB is fail. The triangles represent the faulty vector that is unusable for the modulation. The position of faulty space vectors is summarized in Table 1. It can be seen that when a cell in phase A corrupted, some space vectors in sectors I, III, IV, and VI are affected, while the vectors in sectors II and V are not affected.

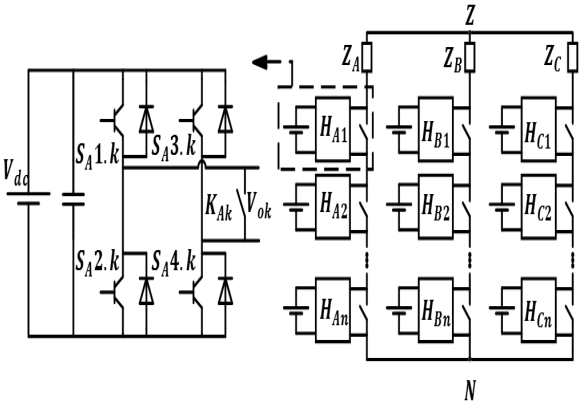

Fig. 1. a. CHB with bypass switches. b. A cell in detail

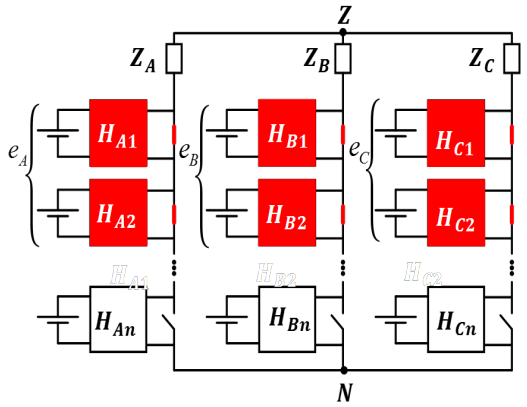

Fig. 2. Inverter when errors occur.

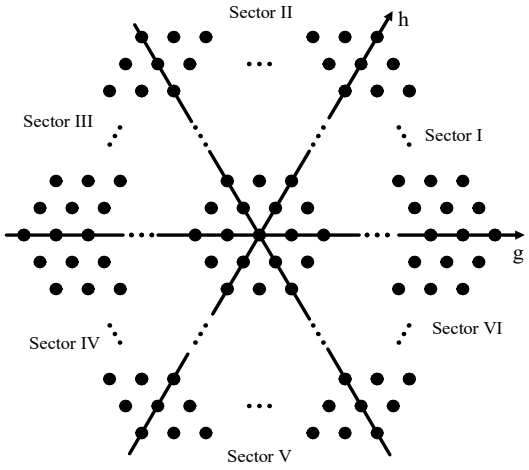

Fig. 3. Voltage space vectors of CHB with *M* levels.

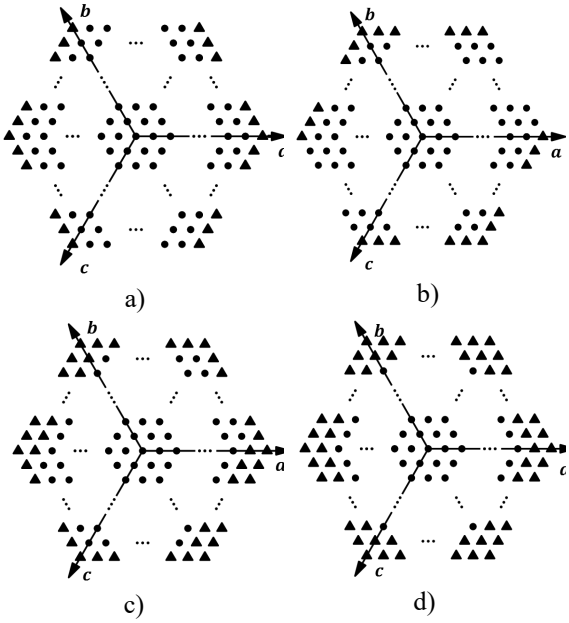

Fig. 4. The effects of output voltage vectors under faulty conditions. (a) Output voltage vectors when cell A1 is faulty. (b) Output voltage vectors when cell B1 is faulty. (c) Output voltage vectors when cell A1 and B1 are faulty. (d) Output voltage vectors when cell A1, B1 and C1 are faulty.

Table 1. Location of space vectors affected by faulty cells.

Sector affected	Inverter phases with faulty power cells		
	Phase A	Phase B	Phase C
I	Yes	No	Yes
II	No	Yes	Yes
III	Yes	Yes	No
IV	Yes	No	Yes
V	No	Yes	Yes
VI	Yes	Yes	No

3. SVM Method for CHB with any Level Under Faulty Conditions.

To ensure that the CHB operates properly despite the existence of a faulty power cell, an improvement of the generalized SVM method [5] is proposed, which consists of the following steps:

- Calculating new reference voltage
- Locating the reference voltage
- Determining the modulation period
- Determining the switching state
- Specifying optimized switching order, switching combination of the switches.

In comparison with [5], step 1 and step 4 need to be modified because of the influence of faulty cells. The remaining steps are preserved. Therefore, this paper only focuses on step 1 and step 4.

3.1. Calculating New Reference Voltage

When faulty power cells occur, some unachievable switching combinations are formed, creating a group of faulty voltage vectors. At this point, creating desired output voltage vectors may not be available if faulty vectors are used in the modulation algorithm. Therefore, the purpose of this section is to determine the number of defective layers, the maximum voltage value that can be modulated, thereby calculating the value of new reference voltage.

Number of faulty space voltage vector layers per sector is obtained by equation (1).

$$\begin{cases} e_I = e_A + e_C \\ e_{II} = e_B + e_C \\ e_{III} = e_A + e_B \\ e_{IV} = e_A + e_C \\ e_V = e_B + e_C \\ e_{VI} = e_A + e_B \end{cases} \quad (1)$$

where $e_{I...VI}$ are the number of faulty vector layers of sector I…VI.

The maximum number of faulty vector layers in vector space is determined as:

$$e_{\max} = \max(e_A + e_B; e_A + e_C; e_B + e_C) \quad (2)$$

The maximum possible amplitude of reference voltage corresponds to the radius of the inscribed circle of the largest hexagon which is not affected by the faulty vectors, as illustrated in Fig. 5:

$$v'_{\max} = \frac{1}{\sqrt{3}} V_{dc} (M - 1 - e_{\max}) \quad (3)$$

where M is the level of the CHB.

After determining v'_{max}, the new reference voltage v_{ref}' can be obtained by the algorithm in Fig. 6.

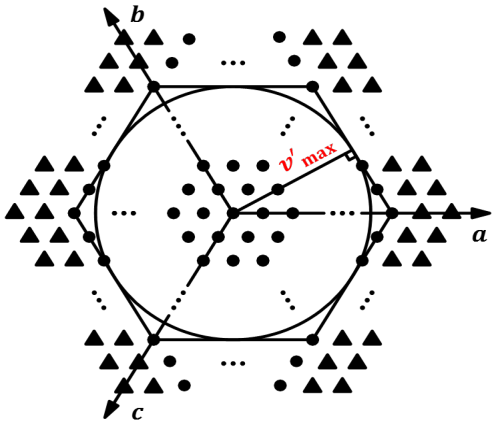

Fig. 5. Calculating the maximum voltage vector can be achieved in faulty CHB.

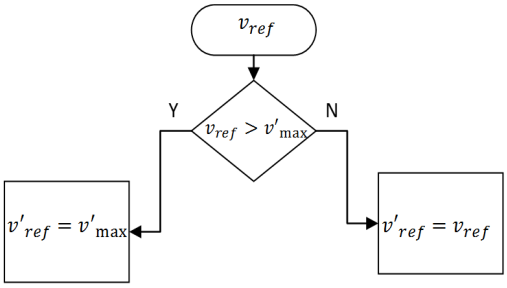

Fig. 6. Alogrithm flowchart for determining reference voltage v_{ref}' under faulty conditions.

3.2. Determining Switching States in Faulty Conditions

When there are e_A, e_B, e_C faulty cells on phase A, B and C, repectively, the converter needs to be reconstructed by shorting these faulty cells. Thereby, the voltages can be created as follows:

$$\begin{cases} V_{AN} = k_{AN}.V_{dc} \\ V_{BN} = k_{BN}.V_{dc} \\ V_{CN} = k_{CN}.V_{dc} \end{cases} \quad (4)$$

Table 2. Specifying level of phases and k selection in sectors $(k_0=k_g+k_h)$

	Sector					
	I	II	III	IV	V	VI
$\begin{bmatrix} k_g \\ k_h \end{bmatrix}$	$\begin{bmatrix} k_{AN}-k_{BN} \\ k_{BN}-k_{CN} \end{bmatrix}$	$\begin{bmatrix} k_{AN}-k_{CN} \\ k_{BN}-k_{AN} \end{bmatrix}$	$\begin{bmatrix} k_{BN}-k_{CN} \\ k_{CN}-k_{AN} \end{bmatrix}$	$\begin{bmatrix} k_{BN}-k_{AN} \\ k_{CN}-k_{BN} \end{bmatrix}$	$\begin{bmatrix} k_{CN}-k_{AN} \\ k_{AN}-k_{BN} \end{bmatrix}$	$\begin{bmatrix} k_{CN}-k_{BN} \\ k_{AN}-k_{CN} \end{bmatrix}$
$\begin{bmatrix} k_{AN} \\ k_{BN} \\ k_{CN} \end{bmatrix}$	$\begin{bmatrix} k \\ k-k_g \\ k-k_g-k_h \end{bmatrix}$	$\begin{bmatrix} k-k_h \\ k \\ k-k_g-k_h \end{bmatrix}$	$\begin{bmatrix} k-k_g-k_h \\ k \\ k-k_g \end{bmatrix}$	$\begin{bmatrix} k-k_g-k_h \\ k-k_h \\ k \end{bmatrix}$	$\begin{bmatrix} k-k_g \\ k-k_g-k_h \\ k \end{bmatrix}$	$\begin{bmatrix} k \\ k-k_g-k_h \\ k-k_h \end{bmatrix}$
k	$\max \begin{bmatrix} -n+e_A \\ -n+k_g+e_B \\ -n+k_0+e_C \end{bmatrix}$	$\max \begin{bmatrix} -n+k_h+e_A \\ -n+e_B \\ -n+k_0+e_C \end{bmatrix}$	$\max \begin{bmatrix} -n+k_0+e_A \\ -n+e_B \\ -n+k_g+e_C \end{bmatrix}$	$\max \begin{bmatrix} -n+k_0+e_A \\ -n+k_h+e_B \\ -n+e_C \end{bmatrix}$	$\max \begin{bmatrix} -n+k_g+e_A \\ -n+k_0+e_B \\ -n+e_C \end{bmatrix}$	$\max \begin{bmatrix} -n+e_A \\ -n+k_0+e_B \\ -n+k_h+e_C \end{bmatrix}$

Table 3. Coordinates of voltage vectors in sector I.

$$k=\max(-n+\mathrm{e}_A;-n+k_g+e_B;-n+k_g+k_h+e_C)$$

		P_1	P_2	P_3	P_1^+
D_1	$\begin{bmatrix} k_g \\ k_h \end{bmatrix}$	$\begin{bmatrix} k_g \\ k_h \end{bmatrix}$	$\begin{bmatrix} k_g+1 \\ k_h \end{bmatrix}$	$\begin{bmatrix} k_g \\ k_h+1 \end{bmatrix}$	$\begin{bmatrix} k_g \\ k_h \end{bmatrix}$
	$\begin{bmatrix} k_{AN} \\ k_{BN} \\ k_{CN} \end{bmatrix}$	$\begin{bmatrix} k \\ k-k_g \\ k-k_g-k_h \end{bmatrix}$	$\begin{bmatrix} k+1 \\ k-k_g \\ k-k_g-k_h \end{bmatrix}$	$\begin{bmatrix} k+1 \\ k-k_g+1 \\ k-k_g-k_h \end{bmatrix}$	$\begin{bmatrix} k+1 \\ k-k_g+1 \\ k-k_g-k_h+1 \end{bmatrix}$
		P_2	P_3	P_4	P_2^+
D_2	$\begin{bmatrix} k_g \\ k_h \end{bmatrix}$	$\begin{bmatrix} k_g+1 \\ k_h \end{bmatrix}$	$\begin{bmatrix} k_g \\ k_h+1 \end{bmatrix}$	$\begin{bmatrix} k_g+1 \\ k_h+1 \end{bmatrix}$	$\begin{bmatrix} k_g+1 \\ k_h \end{bmatrix}$
	$\begin{bmatrix} k_{AN} \\ k_{BN} \\ k_{CN} \end{bmatrix}$	$\begin{bmatrix} k+1 \\ k-k_g \\ k-k_g-k_h \end{bmatrix}$	$\begin{bmatrix} k+1 \\ k-k_g+1 \\ k-k_g-k_h \end{bmatrix}$	$\begin{bmatrix} k+2 \\ k-k_g+1 \\ k-k_g-k_h \end{bmatrix}$	$\begin{bmatrix} k+2 \\ k-k_g+1 \\ k-k_g-k_h+1 \end{bmatrix}$

where:

$$\begin{cases} k_{AN} \in \overline{-n+e_A;\mathrm{n}-\mathrm{e}_A} \\ k_{BN} \in \overline{-n+e_B;\mathrm{n}-\mathrm{e}_B} \\ k_{CN} \in \overline{-n+e_C;\mathrm{n}-\mathrm{e}_C} \end{cases} \quad (5)$$

To determine the switching combinations that generate unfaulty voltage vector on vector space, steps can be done as following.

With sector I: Consider a voltage vector which has the coordinates $[v_g; v_h]$ illustrated in Fig. 7. This voltage vector can be represented by the equations (6) as follows:

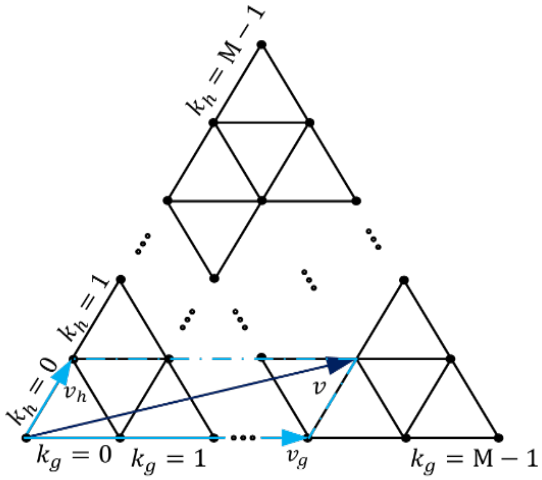

Fig.7. A sector I voltage vector representation.

$$\begin{cases} v_g = \frac{2}{3}V_{dc}k_g = \frac{2}{3}V_{dc}\left(k_{AN} - k_{BN}\right) \\ v_h = \frac{2}{3}V_{dc}k_h = \frac{2}{3}V_{dc}\left(k_{BN} - k_{CN}\right) \end{cases} \quad (6)$$

From (6), we can write:

$$\begin{bmatrix} k_g \\ k_h \end{bmatrix} = \begin{bmatrix} \left(k_{AN} - k_{BN}\right) \\ \left(k_{BN} - k_{CN}\right) \end{bmatrix} \quad (7)$$

with k_A=k, (7) can be rewritten on abc coordinate:

$$\begin{bmatrix} k_g \\ k_h \end{bmatrix} \Rightarrow \begin{bmatrix} k_{AN} \\ k_{BN} \\ k_{CN} \end{bmatrix} = \begin{bmatrix} k \\ k - k_g \\ k - k_g - k_h \end{bmatrix} \quad (8)$$

However, these coordinates must satisfy (5), as (9):

$$\begin{cases} -n + e_A \le k \le n - e_A \\ -n + e_B \le k - k_g \le n - e_B \\ -n + e_C \le k - k_g - k_h \le n - e_C \end{cases} \quad (9)$$

From (9), (10) is given:

$$\begin{cases} -n + e_A \le k \le n - e_A \\ -n + k_g + e_B \le k \le n + k_g - e_B \\ -n + k_g + k_h + e_C \le k \le n + k_g + k_h - e_C \end{cases} \quad (10)$$

That means k must satisfy (11):

$$\max\begin{Bmatrix} -n + e_A \\ -n + k_g + e_B \\ -n + k_g + k_h + e_C \end{Bmatrix} \le k \le \min\begin{Bmatrix} n - e_A \\ n + k_g - e_B \\ n + k_g + k_h - e_C \end{Bmatrix} \quad (11)$$

In other sectors, the states can be determined exactly same way as above, by replacing $\begin{bmatrix} k_g \\ k_h \end{bmatrix}$ in sector I by respective coordinates of these sectors, which are summarized in Table 2.

By implementing the optimized switching algorithm applied for faulty cell conditions, the result can be achieved in Table 3.

4. Simulation Results

To verify the correctness and effectiveness of the proposed method, simulation on Matlab – Simulink software is implemented. Specifically, the algorithm is applied to 11-level CHB inverter, the DC voltage on each cell U_{DC} = 60V, reference voltage U_A = 330sinωt, the phases are balance as the phase angles difference are 120^0. Faulty cells are assumed as shown in Table 4. Error is generated by making a switch of the faulty cell open, other switches keep operating normally.

Table 4. Error assumption in 11-level CHB.

	Pha xảy ra lỗi		
Thời gian (s)	A	B	C
0 - 0,05	0	0	0
0,05 - 0,1	H_{A1}	0	0
0,1 - 0,15	H_{A1}	$H_{B1}; H_{B3}$	$H_{C1}; H_{C3}; H_{C5}$

Simulation results:

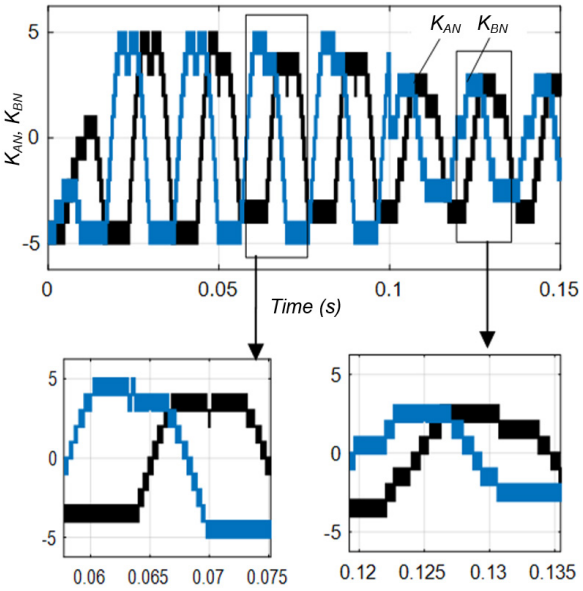

Fig. 8. Level state on phase A and phase B with error handling algorithm.

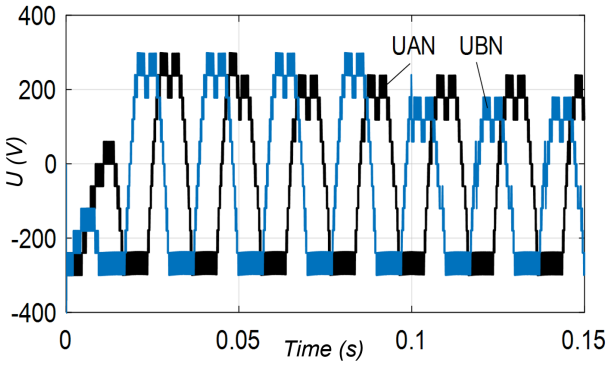

Fig. 9. Output voltage on phases: U_{AN} and U_{BN} without error handling algorithm.

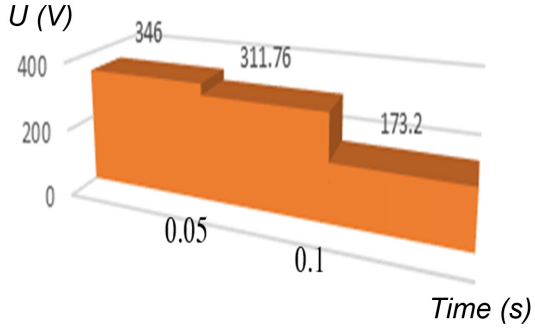

Fig. 10. Maximum output voltage of CHB under faulty conditions.

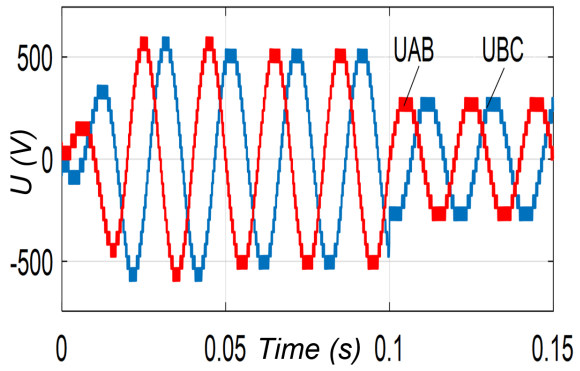

Fig. 11. Line voltage waveform: U_{AB} and U_{BC} with error handling algorithm.

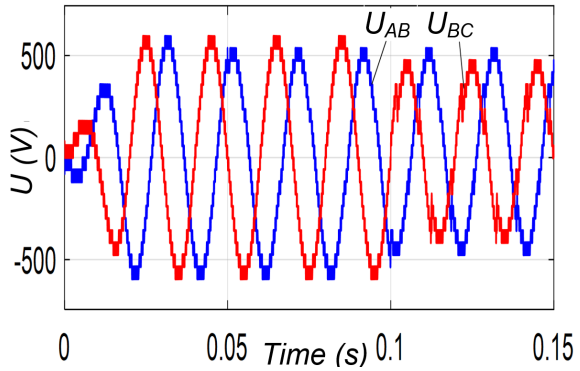

Fig. 12. Line voltage waveform: U_{AB} and U_{BC} without error handling algorithm.

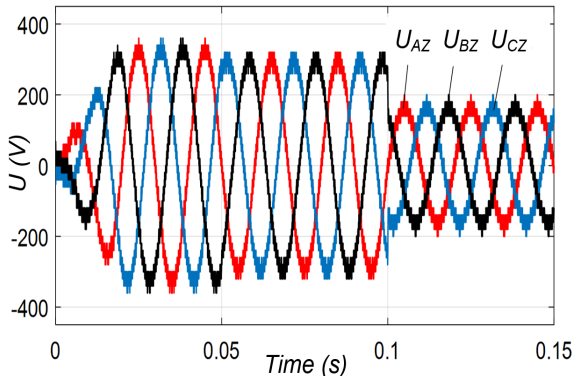

Fig. 13. Output voltage on load: U_{Az}; U_{Bz}; U_{Cz} with error handling algorithm.

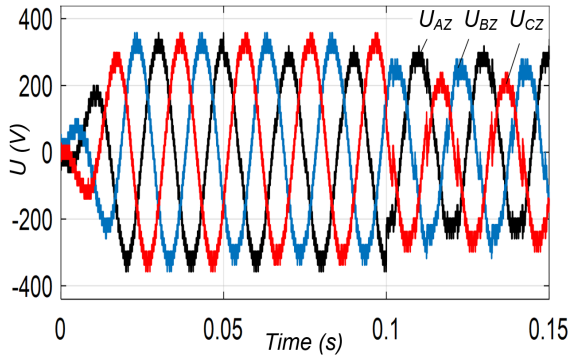

Fig. 14. Output voltage on load: U_{Az}; U_{Bz}; U_{Cz} without error handling algorithm.

In terms of phase output voltage, we can clearly see as Fig. 8, when phase A fails between 0.05 - 0.1s, the error handling algorithm removed the -5, 5 level of the A-phase voltage corresponds to 1 faulty power cell. Similarly, with phase B, for the period from 0.01 to 0.15 s, levels -5, -4, 4, 5 have been removed, corresponds to 2 faulty cells. When there is no error handling algorithm, the modulated voltage waveform U_{AN}, U_{BN}, U_{CN} depicted in Fig. 9 from 0 to 0.05 seconds. However, the real voltage on phase has lost a level with 1 faulty power cell, which causes the output voltage to be unbalanced as shown in Fig 9.

Fig. 10 shows that with the error handling algorithm, the output voltage has the smallest drop. Specifically, in the time interval from 0.05s - 0.1s there is 1 layer of faulty space voltage vectors, maximum output voltage compared to normal condition is 90%. There are 5 faulty layers from 0.1s to 0.15s, the output voltage reaches 50%. Fig. 11 and 13 show that the voltage waveform on the load U_{AZ}, U_{BZ}, U_{CZ} and line voltage U_{AB}, U_{BC} are perfectly balanced when an error occurs.

When the algorithm for error handling is not implemented, if an error occurs, the output voltage of the inverter will be unbalanced as shown in Figure 12, 14. Particularly, with short circuit power switches error, DC power supply is short-circuited, causing danger for the inverter. With the error handling algorithm, by adding auxiliary components and implementing new modulation technique, the inverter could continue to work with both short circuit and open circuit switches errors.

5. Conclusion and Further Development

This paper has proposed a space vector modulation method for cascaded H-bridge inverter structure in case of power cell malfunction. The proposed algorithm has achieved the following results. First, the faulty cell is bypassed so that the system can continue to work properly. Second, the output voltage attenuation is minimized in comparison with the "bypass cell" method where cells are bypassed on all three phases. In addition, the given algorithm ensures the balance of three phases. Finally, the proposed method with optimized switching sequence can easily be applied to cascaded H-bridge inverter with arbitrary-levels. The proposed method is verified by numerical simulation using Matlab-Simulink.

Acknowledgments

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