JST: Smart Systems and Devices
Volume 32, Issue 1, January 2022, 067-075

A Configurable Direct Delta-Sigma Converter for Frequency Division Duplex (FDD) Bands from 0.4 GHz to 3.6 GHz

Loan Pham-Nguyen[1*], Nguyen Thien Viet[1], Dinh Thi Kim Phuong[2]
[1] *Hanoi University of Science and Technology, Hanoi, Vietnam*
[2] *Hanoi University of Industry, Hanoi, Vietnam*
[*] *Email: loan.phamnguyenthanh@hust.edu.vn*

Abstract

This paper presents a novel design of 5th order direct delta-sigma receiver for multi-band multi-standard wireless applications. The receiver is designed to cover Frequency Division Duplex (FDD) bands from 0.4 GHz to 3.6 GHz with a configurable bandwidth of 3.84 MHz (WCDMA), and 9.0/13.5/18/37 MHz (LTE-10M/15M/20M/37M) complying with 3GPP specifications. The configuration is implemented and controlled by a digital controller. System modelling in MATLAB is carried out to tune the key design parameters aiming to optimize noise figure (NF) and linearity of the receiver. The post-simulation results of the receiver show a good match with that of the MATLAB receiver model, an NF of 2.5 dB, an in-band (IB) third-order intercept point (IIP3) of −15 dBm, an out-of-band (OOB) IIP3 of 0 dBm, and a peak signal-to-noise-and-distortion ratio (SNDR) of 58 dB. The receiver is designed in 65-nm CMOS technology with a 70-mA static current and a 1.2-V voltage supply.

Keywords: Continuous time, delta-sigma, multi-band, multi-standard, RF ADC, RF sampling, oversampling, wideband receiver.

1. Introduction

Nowadays, the rapid expansion of data traffic in RF communication standards, such as Wifi, 3G, LTE, LTE CA, has been driving the demand for flexible receivers, granting user access to multiple services simultaneously. Therefore, the receivers employed for these services are required to work at variable center frequency, configurable bandwidth, and high linearity. This requirement can be solved by the flexibility of digital-intensive RF front-end to adapt specific solutions by software-defined operations. As a result, reducing the number of analog blocks or digitizing them becomes crucial tasks.

A digital-intensive RF receiver can be classified into three different types: RF sampling, Sub-sampling, and Delta-Sigma Modulator (DSM). Among the state-of-the-art DSM-based architectures, the direct Delta-Sigma receiver (DDSR) combining the analog front-end and Delta-Sigma Analog-to-Digital Converter (ADC), is considered as the most suitable candidate for wireless applications [1, 2, 3, 4]. This architecture offers promising advantages such as high resolution, high dynamic range, and low complexity. There are two approaches that can be used to design DDSR, they are Discontinuous-time (DT) and Continuous-time (CT) modes. The CT DDSR is more attractive due to its flexibility in the operation of switching from one frequency band to another one [4, 5]. In addition, CT DDSR is also known for attractive properties like variable channel bandwidth, low noise figure, high linearity, and flexible selectivity that can be adapted and configured to the requirement of many communication standards. Also, for low-power applications, CT DDSR is more suitable. In CT DDSR, the required gain-bandwidth product (GBW) is in the range of sampling frequency f_s, meanwhile, GBW must be five times of f_s in DT one [2].

Configurable bandwidths, low noise and high linearity are the key features to evaluate the performance of DDSR. As in [1], a *1st* order CT receiver is proposed with an oversampling rate (OSR) of 16 and a peak SNDR of $51\ dB$ for LTE band where the RF frequency is covered only from $0.6 - 3\ GHz$. A *2nd* and *3rd* order DDSR are investigated in [2], higher peak SNDR of $67\ dB$ is achieved with a broad RF frequency band from $0.4 - 4\ GHz$. However, the proposed system is only studied at schematic level. In [4], a sampling rate of 100 is adopted that leads to complexity for circuit design to obtain only a reasonable SNDR of $50\ dB$ for a *4th* order receiver. In this paper, a *5th* order CT DDSR investigated from system level to transistor level is proposed. A *5th* order modulator may bring on complexity for design; however, that allows the system to operate at a low OSR of only 16. The system frequency range can cover from $0.4 - 3.6\ GHz$, including several mobile standards, such as WCDMA, LTE, and LTE CA.

ISSN: 2734-9373
https://doi.org/10.51316/jst.155.ssad.2022.32.1.9
Received: June 21, 2021; accepted: October 12, 2021

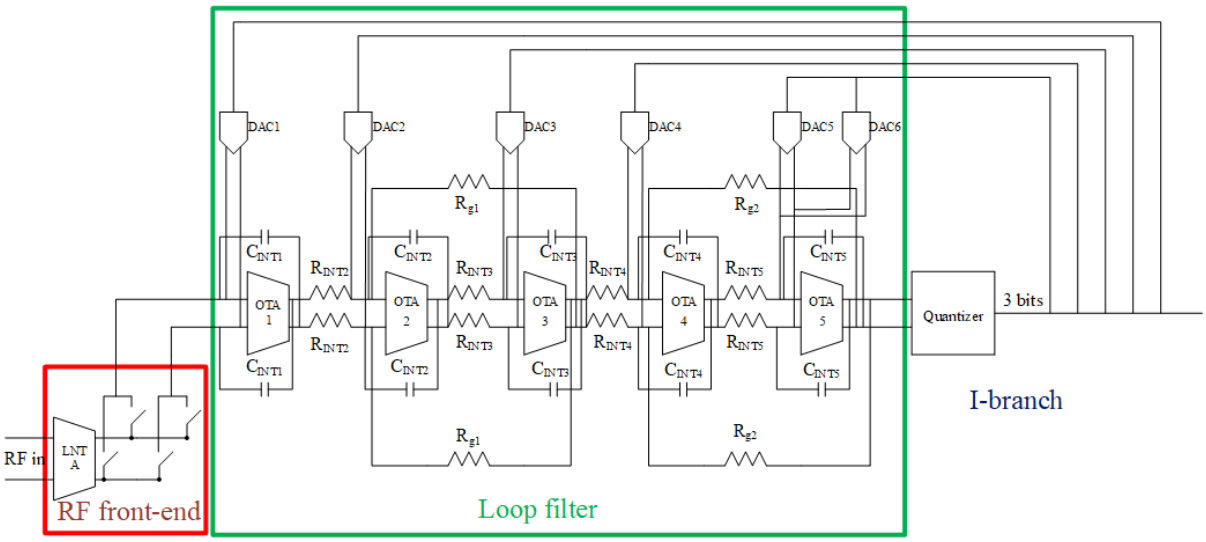

Fig. 1. I-Branch structure of 5^{th} order Continuous-Time Delta-Sigma Receiver

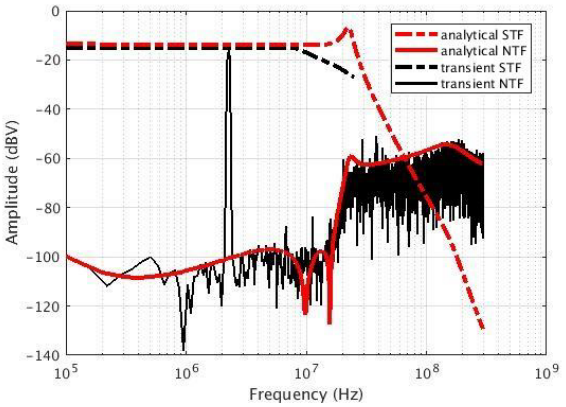

Fig. 2. The STF, NTF analysis of analytical model vs. Cadence Spectre simulation at system level

Table 1. Sampling frequency according to five mobile standards defined by 3GPP

Standard	WCD -MA	LTE			LTE CA
Bandwidth (MHz)	1.92	4.5	6.75	9	18.5
Sampling freq. (MHz)	61.44	144	216	288	592

This paper is organized as follows. The receiver architecture and design methodology are discussed in Section 2. System design is then detailed in Section 3. Section 4 presents the post simulation results of the whole receiver then the paper is concluded in Section 5.

2. Design Methodology

According to the requirements of standard protocols for mobile applications (3GPP) [6, 7, 8] as shown in Table 1 and following the design methodology in the previous work in [4], the system level is developed and studied in Cadence Spectre to evaluate the top-level specifications of our proposed 5^{th} order CT DDSR. The I branch of our proposed receiver is presented in Fig. 1. The 5^{th} order is selected for its optimal aspects of high dynamic range, the requirement of low oversampling rate of 16, and high peak SQNR of 64 dB for mobile frequency range from 400 MHz to 3.6 GHz.

The MATLAB analytical model in [4] is applied to determine the signal transfer function (STF), noise transfer function (NTF), and the component parameters of system sub-circuits such as the integrator of loop filter, the Digital-to-Analog converters (ADC), etc. The analytical simulation results are compared with the transient results of the second model realized in Cadence Spectre (Fig. 2). It can be seen that NTFs and STFs of those models show a good match in which fundamental components in the transient NTF are excluded.

The PSS-PAC/PNOISE system analysis allows to define the component parameters such as ON resistance of switches, transconductance of Low Noise Transconductance Amplifier (LNTA) and each integrator stage in the loop filter. To define the design targets of sub-blocks integrated with the receiver, their component parameters are swept until reaching the system targets for NF, and linearity, that is validated in the analytical model. Finally, the transient simulation for the whole receiver is performed to validate the selection of architecture.

3. System Design

Fig. 1 illustrates the complete I branch of our 5^{th} order CT DDSR. The analog front-end consists of LNTA and passive mixer where the input signal is amplified and demodulated. The signal is then sampled, integrated, and quantized by the baseband blocks comprising a loop filter of five stages and a quantizer. The digital quantized output signal is then fed back to each stage of the loop filters through the Digital-to-Analog Converter (DAC). The design of these sub-blocks will be discussed in detail as follows.

3.1. Low Noise Transconductance Amplifier

Apart from the integrated resistors and switches, LNTA can be considered as the main contribution of thermal noise to the whole system. Different LNTA topologies may have various impacts on thermal noise, however the LNTA transconductance gain G_m causes mostly the degradation of noise figure (NF) as can be seen in (1). The excess noise factor β, accounting for the minor contributors, equals to $32/3$ based on our experiments with the 6-nm CMOS technology, where the reference impedance R_S is 50Ω.

$$NF \approx 10 \times log\ log\ \left(\frac{\beta}{G_m \times R_S}\right) \quad (1)$$

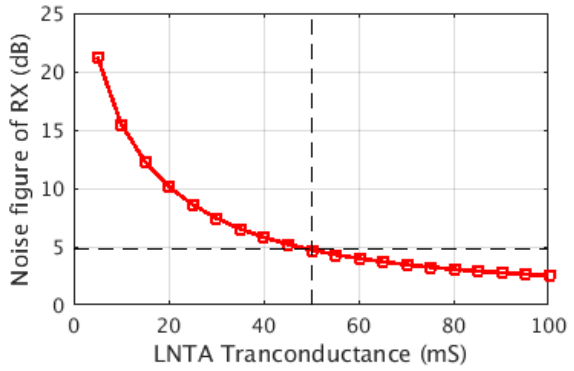

Fig. 3. Analysis of LNTA transconductance gain vs. NF of receiver for LTE 18.5 MHz.

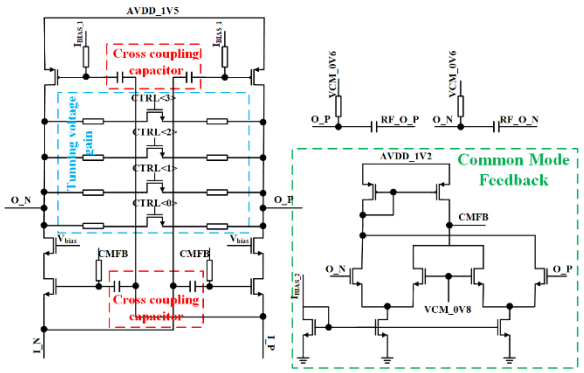

Fig. 4. LNTA schematic design

In this work, it is prioritized to design the system with respect to the standard requirements of the highest baseband, hereby the LTE CA. In other words, once the design meets the target for the highest band, it will certainly comply with the lower bands. Fig. 3 shows the trade-off between the LNTA transconductance gain and the noise figure of the receiver model. The transconductance gain should be selected at $50\ mS$ to achieve the desired noise figure of $4.75\ dB$ for the LTE CA with the standard bandwidth of 18.5 MHz.

The implementation of LNTA at the transistor level is presented in Fig. 4. A common gate with cross-coupling capacitor is employed for its high linearity and a common-50Ω-differential-input impedance [9]. As the LNTA operates in a wide frequency range of $0.4 - 3.6\ GHz$, it is required to tune the voltage gain which is controlled by four switches and series resistors in the feedback loop. Cascode topology with PMOS current source is employed to achieve high voltage gain. In order to improve NF, output common mode voltage is also set at $0.8\ V$ applying a common mode feedback circuit. The LNTA post-simulation results show a good match with the design requirements where the voltage gain reaches $21\ dB$ at $3.6\ GHz$, NF is only $3.3\ dB$ for LTE CA band ($3.6\ GHz$) as shown in Fig. 5.

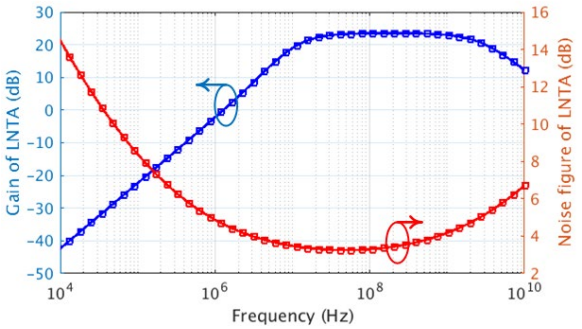

Fig. 5. Post-simulation results of LNTA

3.2. Loop Filter

3.2.1. Integrator

The loop filter comprises five stages of integrators. The block diagram of an i^{th} continuous-time integrator, consisting of an OTA, a resistor R_i and a capacitor $C_i, i = 2 \ldots 5$, is shown in Fig. 6. The PSS-PAC/PNOISE simulation is also carried out to determine the component parameters of the i^{th} integrator which is similar to the aforementioned analysis of LNTA. The integrator resistors are firstly scanned to achieve optimized values of noise figure and linearity of the receiver. The integrator capacitors are then defined so that the equation shown in the first column in Table 2 is satisfied for each bandwidth of each integrator from the 2^{nd} to 5^{th} stage. The component sizing constraints are also taken into

consideration. The values of the resistor and capacitor should be smaller than 50 $k\Omega$ and 10 pF, respectively. An example of linearity and NF analysis to select the optimal resistor value for the second integrator is shown in Fig. 7. The resistor R_2 is set at 5 $k\Omega$ to obtain the best NF (smaller than 4.8 dB) and linearity (greater than -12.5 dB) for the capacitor of the second stage integrator. Table 2 summarizes the value of resistors R_i and capacitors C_i defined for each i^{th} integrator.

As shown in Table 2, a large range of capacitors for each integrator is required for diverse bandwidth from 1.92 MHz to 18.5 MHz (e.g., a required variation from 4 to 38.5pF for capacitor C_1). This causes significant constraints to design the switching control intrading off with area to select a certain capacitor corresponding to one band for each integrator stage. To design the switching control, a structure of small unit capacitor stacking in array is proposed as shown in Fig. 8. The capacitance value is controlled by 4-bit thermal code F(0:3). Considering the process and temperature variation, the unit capacitance should be tuned in a large scale of about $\pm 40\%$ around the center value to compensate for the disparity of resistors or capacitors. The tuning is controlled digitally by a 5-bit binary code B(0:4).

Table 2. Integrating resistors (in $k\Omega$) and capacitors (in pF) for five bandwidth options.

Operating BW (MHz)	**1.92**	**4.5**	**6.75**	**9**	**18.5**
$C_1 = 4 \cdot 592MHz / F_S$	38.5	16.4	11.0	8.2	4
$C_2 = 1 / a_1 F_S R_2$	19.6	8.4	5.6	4.2	2.0
$C_3 = 1 / a_2 F_S R_3$	16.4	7	4.7	3.5	1.7
$C_4 = 1 / a_3 F_S R_4$	9.5	4.0	2.7	2.0	1
$C_5 = 1 / a_4 a_5 F_S R_5$	0.77	0.33	0.22	0.17	0.08
$R_2 = R_3 = R_4 = 5$			$R_5 = 10$		
$R_{g1} = R_2 \frac{a_1}{g_1} = 14.7$			$R_{g2} = R_4 a_3 \frac{a_5}{g_2} = 114.2$		

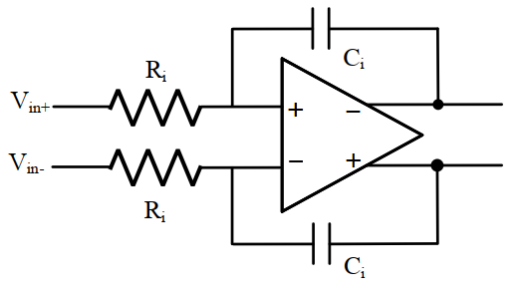

Fig. 6. Continuous-times integrator for i^{th} stage

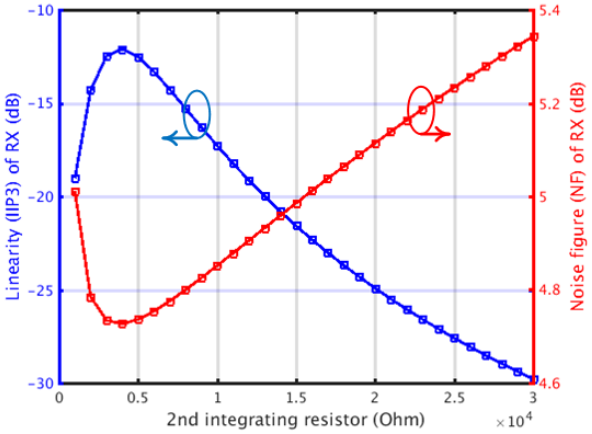

Fig. 7. Analysis of NF and IIP3 of Receiver vs. 2^{nd} integrating resistor

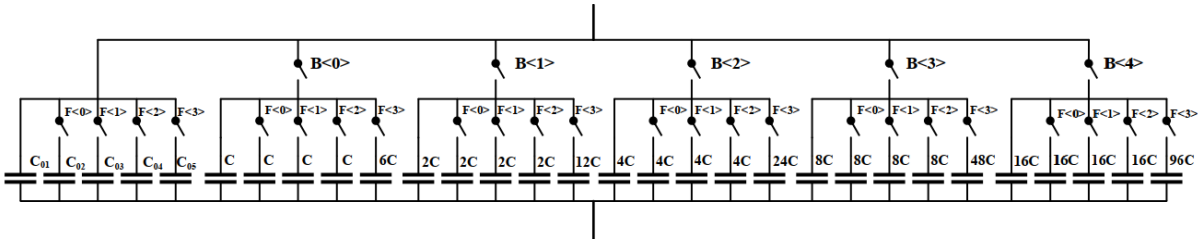

Fig. 8. Configurable integrating capacitor architecture

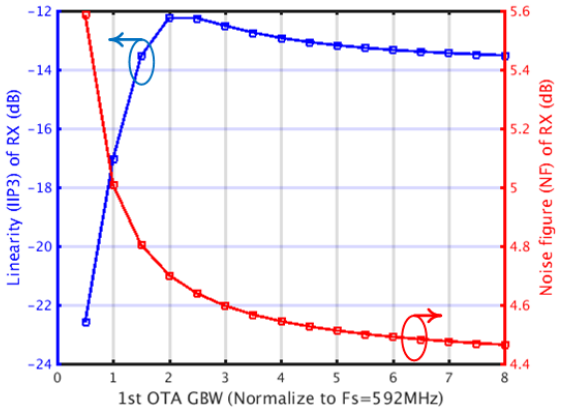

Fig. 9. Analysis of NF and IIP3 of receiver for LTE CA vs. *1st* OTA GBW

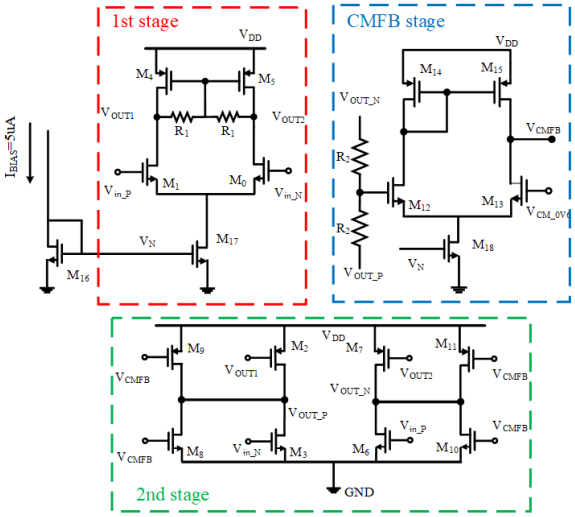

Fig. 10. Non-capacitor compensation feedforward OTA

.

The gain-bandwidth product (GBW) of OTA is also determined by observing the variation of the noise figure (NF) and linearity of the system-level model. Fig. 9 shows the variation of NF and linearity of system as a function of GBW of the first OTA that is normalized to switching frequency f_s at LTE CA band. The worst NF occurs at the highest baseband bandwidth of 18.5 MHz and the choice of GBW of each OTA stage is in trade-off with system linearity. The GBW normalization is determined at about 1.8 where linearity reaches $-12\,dB$ with a good NF smaller than 3.5 dB while ensuring a reasonable power consumption. As shown in Fig. 10, a non-capacitor compensation OTA architecture in [10] is developed and implemented in this work. As one integrator stage works for different bands, its transconductance is also tuned following the value of its capacitor so that they satisfy the equation (2). Besides, the tuning of OTA transconductance can be controlled by thermal code. That activates different unit cells of the i[th] stage of OTA resulting in variation of OTA transconductance according to different operating frequencies.

$$\frac{g_{M1}}{C_{VOUT1}} = \frac{1}{R_{OUT\_N} \times R_{Load}} \tag{2}$$

where g_{M1} is the transconductance of the input pair, C_{VOUT1} is the output capacitance of the *1st* stage, R_{OUT_N} and R_{Load} are the OTA output resistance and load resistance, respectively.

3.2.2. Digital-to-Analog Converter (DAC)

The integrator capacitors are charged and discharged by the output current of the DAC block, which are controlled by the feedback loop from quantizer. The system requires 6 DACs to load 5 integrators. The difference between these DACs is their load capacitors (integrator capacitors), which results in different nominal output currents (Table 3). Any process and temperature variation will lead to the mismatch of DAC output currents and then introduce harmonic and noise to the system. To evaluate the performance of DAC, it is essential to study the impact of self-mismatch of DAC current to the system condition. Hence, variables with random distribution are added to each current of DAC cell to emulate the self-mismatch. Transient simulations with random self-mismatch distribution are then carried out. Fig. 11 shows an example on the impact of current mismatch from 0.5% to 2% of the first DAC to the degradation of SNDR of the system. It shows that to achieve a SNDR higher than 50 dB, the allowable self-mismatch of the *1st* DAC should be smaller than 1%. Similar transient simulation analysis is carried out for other DACs. The self-mismatch limit of these six DACs so that the receiver still meets the SNDR target is summarized in Table 3.

Table 3. 1σ current self-mismatch specification of DACs

DAC	*1st*	*2nd*	*3rd*	*4th*	*5th*	*6th*
Nominal current (μA)	1.052	0.842	1.266	1.013	0.45	1.065
Mismatch	1%	1%	2%	2%	3%	3%

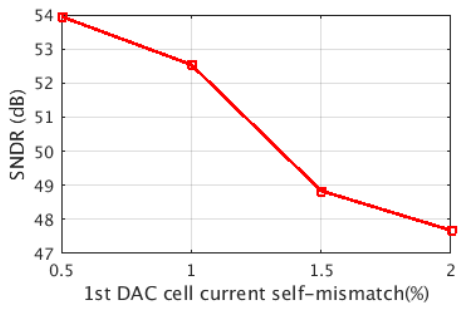

Fig. 11. Analysis of *1st* DAC cell's current self-mismatch in Cadence Spectre

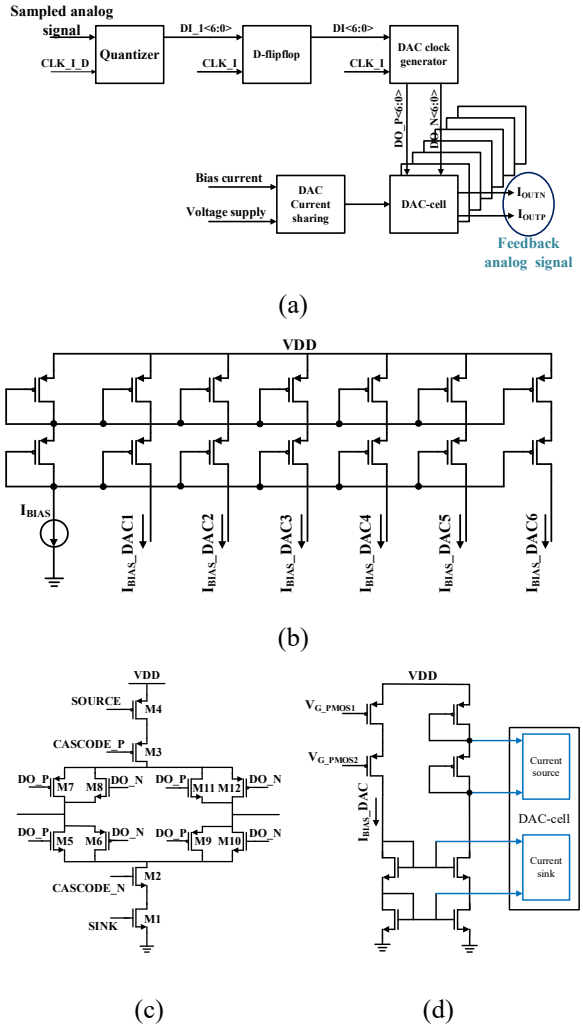

Fig. 12. (a) Block diagram of one DAC (b) Current sharing block to provide bias current to 6 ADCs (c) Schematic of one DAC-cell (d) Illustration of biasing circuit to DAC cell

Fig. 12 shows the block diagram of one DAC (a), its sub-blocks including the current sharing circuit (b), the structure of one DAC_cell (c), and its biasing circuit (d). One DAC consists of a biasing circuit, seven DAC_cells and one clock generator. The DAC_cells are controlled by the 7-bits DO_P(N)<6:0> that are generated from the output of quantizer DI_i<6:0>. These signals are synchronized with the main clock signal by using D-flipflop and clock generator. Besides, these subblocks ensure that the controlled bits DO_P and DO_N are out of phase and their timing parameters, i.e., delay, rising, and falling edge, are smaller than one period of sampling clock. The clock generator is presented in Fig. 13. The inverter circuit in the upper branch ensures the opposite phase of two output signals (DO_P and DO_N) from two branches. The delay is adjusted by the buffers. The synchronization with the main clock is guaranteed by the transmission gates.

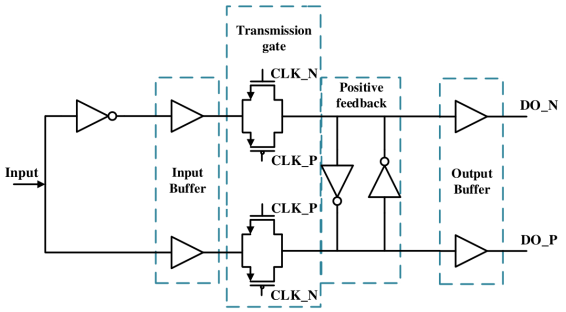

Fig. 13. DAC clock generator sub-block

The conventional dynamic weighted averaging (DWA) is applied to implement digital synchronization. This technique allows to conduct a periodic selection of DAC cells [11], which draws on a 1^{st} order shaping of the DAC mismatch error. That offers an improvement of linearity and voltage resolution. In this work, a conventional DWA is applied to ease the requirement of DACs self-mismatch by a factor of 8 for the main DACs and a factor of 4 for the others. The simulation results show that, in the typical corner conditions, the DWA delay is about $200\,ps$ and requires a small area of about $420\,\mu m^2$ for both branches.

3.2.3. RC Calibration

An RC calibration is a replica of a tuning circuit and is used to detect the process variations and then it provides an accurate tuning control word code to compensate for process variations in the tuning circuit as applied in loop filters. The RC time constant can be tuned in either active or passive ways. The former implements a continuous tuning scheme that adjusts the transconductance of OTAs while the latter varies R or C within a set of discrete values. In this work, RC tuning topology is adopted for its high linearity where the OTA transconductance is designed at constant and the circuit accuracy is ensured by a reasonable number of tuning bits of five.

A modification of [12] is applied to implement the auto tuning RC calibration, as shown in Fig. 14. The structure of bank capacitors and 5-bit controlled word is set to be similar to one of integrator capacitors to obtain the same range of process variations. For high-speed application, a regenerative latch is used for the 2^{nd} stage of the comparator (Fig. 15) instead of a D-type Flip Flop applied in [12]. In addition, the resistor ladder value is selected to ensure the minimum self-mismatch of each resistor. The reference voltages V_{REF1} and V_{REF2} are set to reduce the design complexity of comparator CMP and operational amplifier (Opamp) circuits. This RC passive tuning circuit operates in four phases: reset, integrate, compare, and increase. A constant current I_C through M_1 is generated thank to the negative feedback loop

from V_S to the Opamp inverting terminal. This current is applied to charge the capacitor bank. The voltage V_o is set to equal to V_{REF1}. Initially, the n-bit control word is set to "zeros" to turn off all the switches of C_{BANK}. During the integrate phase, the current I_C is integrated over the capacitor bank and the voltage $V_o(t)$ is set as

$$V_o(t) = V_{DD} - \frac{V_{REF2}}{R_{REF}C_{BANK}}t. \quad (3)$$

The voltage of V_o depends on the capacitance value of C_{BANK} that is controlled by the n-bit counter. At the end of each integration phase, V_o is compared to the reference voltage V_{REF1} and the counter counts up to increase the capacitance value of C_{BANK} until V_o reaches V_{REF1}. The process is repeated until the value of $R_{REF}C_{BANK}$ is equal to the expected RC time constant, so this voltage V_{REF1} can be then expressed as follows:

$$V_{REF1} = V_{DD} - V_{REF2}) \quad (4)$$

After the counting phase, the voltage in C_{BANK} resets, then the circuit starts again a new period. Continuously, the value of C_{BANK} increases until the comparator output switches to a high level. Once the counter stops counting, this 5-bit calibration word is used to tune the control bit B(0:4) of the capacitor array.

4. System Post-Simulation Results

The full layout design of our proposed 5^{th} order direct ΔΣ receiver is presented in Fig. 16. It includes all the sub-blocks from RF front-end to the loop filters, quantizer, digital tuning circuit and RC calibration circuit. Different post-simulations are carried out to observe the main features of the receiver i.e., SNDR, SFDR for different mobile standards from 400 MHz to 3.6 GHz. Fig. 17 shows the post-simulation results for the worst case of LTE CA band where the input power is set at -52 dBm, and we can obtain a good SNDR of 58.8 dB and SFDR reaches 78.7 dB. In other words, the whole design band meets the 3GPP requirements for 3G/4G mobile standards.

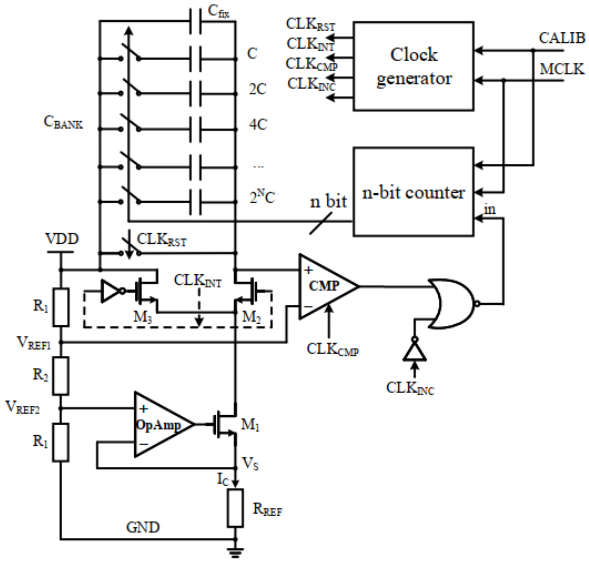

Fig. 14. Architecture of the auto-tuning circuit.

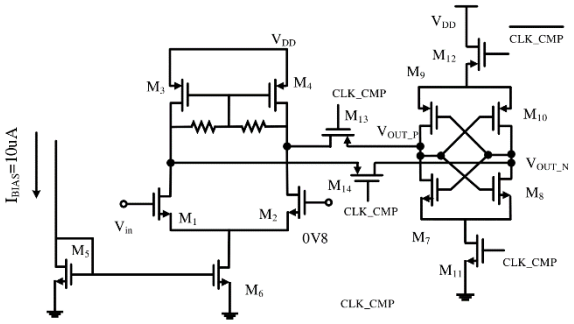

Fig. 15. Full schematic of comparator using generative latch.

Table 4. Benchmark.

Parameter	[1]	[2]	[4]	This work
Topology (DSM)	1^{st} order	$2^{nd}/3^{rd}$ order	4^{th} order	5^{th} order
RF frequency	$0.6-3$ GHz	$0.4-4$ GHz	-	$0.4-3.6$ GHz
OSNR	16	25	100	16
Peak SNDR @ 20 MHz	$47-51$ dB	67 dB @10 MHz	50 dB	59 dB
Area	2 mm^2	schematic	system	4.6 mm^2

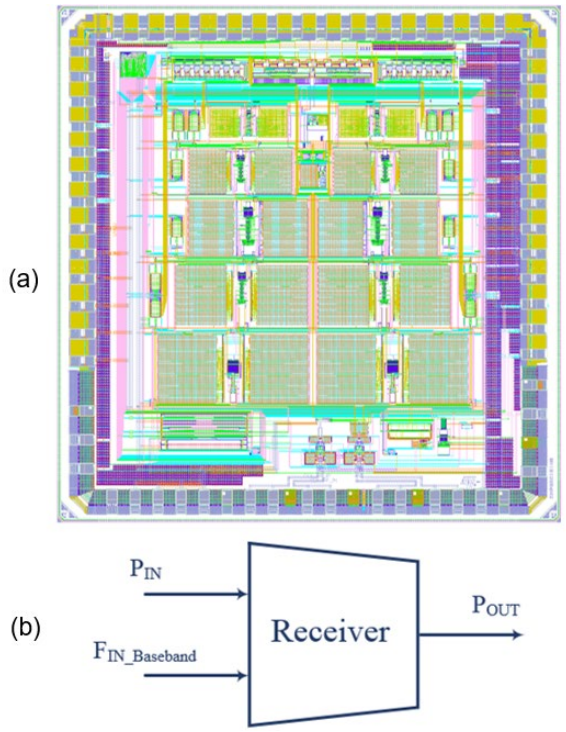

Fig. 16. (a) Layout of 5^{th} order continuous time direct $\Delta\Sigma$ receiver (b) Testbench.

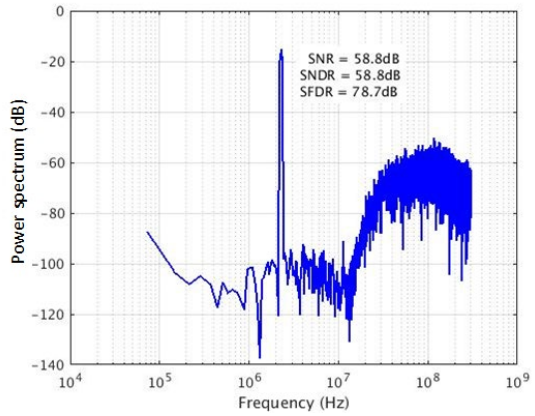

Fig. 17. PSD analysis with $P_{IN} = -52\ dBm$ at 18.5 MHz baseband.

Table 4 shows the benchmarking of our proposed design with other research results. Our receiver covers a large frequency range with the reasonable OSR of 16 compared to 100 in [4] and 25 in [2]. A good SNDR is achieved for the worst case of LTE CA band compared to only $47 - 51\ dB$ in [1]. Higher SNDR is observed in [2], but their band is limited at 10 MHz compared to 18.5 MHz as in our work.

5. Conclusion

This paper represents the first direct delta-sigma receiver of high order and complexity that supports both 3G and 4G mobile standards. The Cadence Spectre model and schematic design are demonstrated to achieve the target performance. The Cadence simulation results show good correlation with the MATLAB NTF simulation that confirms our selection of architecture and system parameters, i.e., OSR, modulator order. In addition, a configurable bandwidth is also implemented and controlled by the digital controller. The post-simulation shows that the proposed receiver satisfies the requirement of 3G/4G covering a larger mobile band with reasonable OSR and good SNDR in comparison with current studies.

Acknowledgments

This material is based upon work supported by 36/FIRST/1a/HUST. Special thanks to Prof. Hanh-Phuc Le for his fruitful discussions.

References

[1]. X. Liu and A. Nejdel, A 65 nm CMOS wideband radio receiver with ΔΣ-based A/D-converting channel-select filters, IEEE Journal of Solid-State Circuits, vol. 51, no. 7, pp. 1566-1578, July 2016 https://doi.org/10.1109/JSSC.2016.2553022.

[2]. M. T. Nguyen, C. Jabbour and V. T. Nguyen, A flexible receiver using ΔΣ modulation, 2016 IEEE International Symposium on Circuits and Systems (ISCAS), 2016 https://doi.org/ 10.1109/ISCAS.2016.7527535.

[3]. M. Englund, K. B. Östman, O. Viitala, M. Kaltiokallio, K. Stadius, K. Koli and J. Ryynänen, A programmable 0.7–2.7 GHz direct ΔΣ receiver in 40 nm CMOS, IEEE Journal of Solid-State Circuits, vol. 50, no. 3, pp. 644-655, March 2015 https://doi.org/ 10.1109/ISSCC.2014.6757517.

[4]. M. T. Nguyen, C. Jabbour, S. M. Homayouni, D. Duperray, P. Triaire, V. T. Nguyen, System design for direct RF-to-digital ΔΣ receiver, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 10, pp. 1758-1770, October 2016 https://doi.org/10.1109/TCSI.2016.2589542.

[5]. K. Koli, S. Kallioinen, J. Jussila, P. Sivonen and A. Parssinen, A 900-MHz direct delta-sigma receiver in 65-nm CMOS, IEEE Journal of Solid-State Circuits, vol. 45, no. 12, pp. 2807-2818, December 2010 https://doi.org/ 10.1109/JSSC.2010.2075270.

[6]. 3GPP, Digital Cellular Telecommunications System, Mobile Station Conformance Specification, 2013. [Online]. Available: https://www.3gpp.org/ftp/Specs/archive/51_series/51.010-1/.

[7]. 3GPP, LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment Radio Transmission and Reception, 2013. [Online]. Available: https://www.3gpp.org/ftp/Specs/archive/36_series/36.101/.

[8]. 3GPP, Universal Mobile Telecommunications System; User Equipment Radio Transmission and Reception (FDD), 2013. [Online]. Available: https://www.3gpp.org/ftp/Specs/archive/25_series/25.101/.

[9]. L. Duipmans, R. E. Struiksma, E. A. M. Klumperink, B. Nauta, F. E. v. Vliet, Analysis of the signal transfer and folding in N-path filters with a series inductance, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 1, pp. 263-272, January 2015 https://doi.org/10.1109/TCSI.2014.2354772.

[10]. B. K. Thandri and J. Silva-Martinez, A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors, IEEE Journal of Solid-State Circuits, vol. 38, no. 2, pp. 237-243, February 2003 https://doi.org/10.1109/JSSC.2002.807410.

[11]. R. Baird and T. Fiez, Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 42, no. 12, pp. 753-762, 1995 https://doi.org/10.1109/82.476173.

[12]. B. Xia, S. Yan, and E. Sanchez-Sinencio, An RC time constant auto-tuning structure for high linearity continuous-time ΔΣ modulators and active filters, IEEE Transactions on Circuits and Systems I: Regular Papers, pp. 2179-2188, 2004 https://doi.org/10.1109/TCSI.2004.836852.