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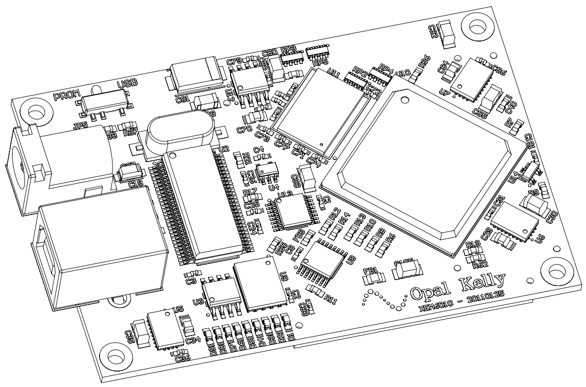

# *XEM6010 User's Manual*

A compact (75mm x 50mm) integration board featuring the Xilinx Spartan-6 FPGA, High-Speed USB 2.0, and on-board DDR2 memory.

The XEM6010 is a compact USB 2.0 FPGA integration module featuring the Xilinx Spartan-6 FPGA, 1 Gb (64 Mx16-bit) DDR2 SDRAM, high-efficiency switching power supplies, and two high-density 0.8-mm expansion connectors. The high-speed USB 2.0 interface provides fast configuration downloads and PC-FPGA communication as well as easy access with our popular FrontPanel application and SDK. A flexible, multiple-output PLL is also provided on-board..

Software, documentation, samples, and related materials are

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Revision History:

| Date | Description |
|---|---|
| 20110301 | Initial release. |
| 20110317 | Minor updates. |
| 20110406 | Added note and reference regarding LVDS output restriction for Spartan-6. |
| 20110818 | Fix minor typo in pinout table. L59N_1 changed to L49N_1 |
| 20110926 | Added sections on MUXSEL and I2C_SCL / I2C_SDA treatment. |
| 20120216 | Added another table to the BRK6110 connections section. |
| 20121128 | Added key storage information for newer PCB revision. |
| 20140402 | Added remarks about Pins reference. |
| 20141202 | Fix JP3-7 reference in the XEM3050 Migration information. |
| 20150303 | Added additional Pins information. |

# Contents

# Introducing the XEM6010

The XEM6010 is a compact FPGA board featuring the Xilinx Spartan-6 FPGA and high-speed USB 2.0 connectivity. Designed as a full-featured integration system, the XEM6010 provides access to over 110 I/O pins on its 484-pin Spartan-6 device and has a 128-MiByte DDR2 SDRAM available to the FPGA. The XEM6010 is designed for medium-sized FPGA designs with a wide variety of external interface requirements.

## PCB Footprint

A mechanical drawing of the XEM6010 is shown at the end of this manual. The PCB is 75mm x 50mm with four mounting holes (M2 metric screws) spaced as shown in the figure. These mounting holes are electrically isolated from all signals on the XEM6010. The two connectors (USB and DC power) overhang the PCB by approximately 4mm in order to accommodate mounting within an enclosure.

The XEM6010 has two high-density 80-pin connectors on the bottom side which provide access to many FPGA pins, power, and JTAG.

### BRK6110 Breakout Board

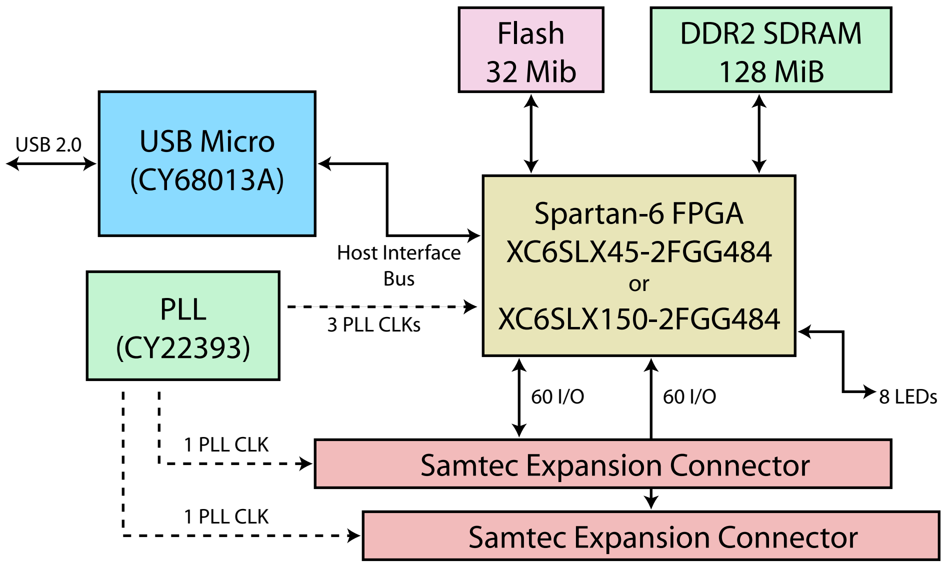
A simple breakout board (the BRK6110) is provided as an optional accessory to the XEM6010. This breakout board provides DC power and easy access to the high-density connectors on the XEM6010 by routing them to lower-density 2mm-spaced thru-holes. The breakout board also provides a convenient reference for building boards that will mate to the XEM6010.

Opal Kelly reserves the right to change the form-factor and possibly pinout of the BRK6110. Therefore, unlike the XEM6010, it is not intended or recommended for production integration.

Full schematics and Gerber artwork files for the BRK6110 are provided free of charge. If your application depends on the existing form-factor, you may reproduce this board from these documents.

A mechanical drawing of the BRK6110 is also shown at the end of this document.

## Functional Block Diagram




## FPGA

The XEM6010 is offered in two variants. These two variants are identical except for the FPGA provided. The table below lists some of the differences between the two devices. Please consult the Xilinx documentation for a more thorough comparison.

| Feature | XEM6010-LX45 | XEM6010-LX150 |
|---|---|---|
| FPGA | XC6SLX45-2FGG484C | XC6SLX150-2FGG484C |
| Slice Count | 6,822 | 23,038 |
| D Flip-Flops | 54,576 | 184,304 |
| Distributed RAM | 401 Kib | 1,355 Kib |
| Block RAM | 2,088 Kib | 4,824 Kib |
| DSP Slices | 58 | 180 |
| Clock Management Tiles | 4 | 6 |

## Power Supply

The XEM6010 is designed to be operated from a 5-volt power source supplied through the DC power jack on the device or the expansion connectors on the bottom of the device. This provides power for the three high-efficiency switching regulators on-board to provide 3.3v, 1.8v and 1.2v. 0.9v is derived from the 3.3-volt supply using a small low-dropout (LDO) regulator for use as a DDR2 termination voltage. Each of the three switching regulators can provide up to 2A of current.

### DC Power Connector

The DC power connector on the XEM6010 is part number PJ-102AH from CUI, Inc. It is a standard "canon-style" 2.1mm / 5.5mm jack. The outer ring is connected to DGND. The center pin is connected to +VDC.

## High-Speed USB 2.0 Interface

The XEM6010 uses a Cypress CY7C68013A FX2LP USB microcontroller to make the XEM a USB 2.0 peripheral. As a USB peripheral, the XEM is instantly recognized as a plug and play peripheral on millions of PCs. More importantly, FPGA downloads to the XEM happen blazingly fast, virtual instruments under FrontPanel update quickly, and data transfers are much faster than the parallel port interfaces common on many FPGA experimentation boards.

## On-board Peripherals

The XEM6010 is designed to compactly support a large number of applications with a small number of on-board peripherals. These peripherals are listed below.

### Cypress CY22393 PLL

A multi-output, triple-PLL clock generator can provide up to five clocks, three to the FPGA and another two to the expansion connectors JP2 and JP3. The PLL is driven by a 48-MHz signal output from the USB microcontroller. The PLL can output clocks up to 150-MHz and is configured through the FrontPanel software interface or the FrontPanel API.

### 128-MByte Word-Wide DDR2 Synchronous DRAM

The XEM also includes a 128-MiByte DDR2 SDRAM with a full 16-bit word-wide interface to the FPGA. This SDRAM is attached exclusively to the FPGA and does not share any pins with the expansion connector. The maximum clock rate of the SDRAM is 333 MHz. With the -2 speed grade of the Spartan-6, the maximum clock rate is 312.5 MHz for a supported peak memory bandwidth of 10 Gb/s.

The DDR2 SDRAM is a Micron MT47H64M16HR-3:G (or compatible).

### Serial Flash Memory

A 32 Mib serial flash device (Numonyx M25P32-VME6G or equivalent) provides on-board configuration memory for the FPGA as well as general non-volatile storage for your design.

### LEDs

Eight LEDs and are available for general use as debug outputs.

## Expansion Connectors

Two high-density, 80-pin expansion connectors are available on the bottom-side of the XEM6010 PCB. These expansion connectors provide user access to several power rails on the XEM6010, the JTAG interface on the FPGA, and 124 non-shared I/O pins on the FPGA, including several GCLK inputs.

The connectors on the XEM6010 are Samtec part number: BSE-040-01-F-D-A. The table below lists the appropriate Samtec mating connectors along with the total mated height.

| Samtec Part Number | Mated Height |
|---|---|
| BTE-040-01-F-D-A | 5.00mm (0.197") |
| BTE-040-02-F-D-A | 8.00mm (0.315") |
| BTE-040-03-F-D-A | 11.00mm (0.433") |
| BTE-040-04-F-D-A | 16.10mm (0.634") |
| BTE-040-05-F-D-A | 19.10mm (0.752") |

## FrontPanel Support

The XEM6010 is fully supported by Opal Kelly's FrontPanel Application. FrontPanel augments the limited peripheral support with a host of PC-based virtual instruments such as LEDs, hex displays, pushbuttons, toggle buttons, and so on. Essentially, this makes your PC a reconfigurable I/O board and adds tremendous value to the XEM6010 as an experimentation or prototyping system.

### Programmer's Interface

In addition to complete support within FrontPanel, the XEM6010 is also fully supported by the FrontPanel SDK, a powerful C++ class library available to Windows, Mac OS X, and Linux programmers allowing you to easily interface your own software to the XEM.

In addition to the C++ library, wrappers have been written for C#, Java, and Python making the API available under those languages as well. Sample wrappers are also provided for Matlab and LabVIEW.

Complete documentation and several sample programs are installed with FrontPanel.

# Applying the XEM6010

## Powering the XEM6010

The XEM6010 requires that this supply be clean, filtered, and within the range of 4.5v to 5.5v. This supply must be delivered through the +VDC pins on the two device's two expansion connectors or the DC power connector..

The expansion bus has several power supply pins, described below:

- +VDC is provided by an external device to the XEM6010. It must be a clean, filtered supply within the range of +4.5 volts and +5.5 volts.
- +3.3v is the output of a 2-Amp switching regulator on the XEM6010.
- +1.8v is the output of a 2-Amp switching regulator on the XEM6010.
- +1.2v is the output of a 2-Amp switching regulator on the XEM6010.
- +VCCO0 is the bank-0 I/O voltage to the FPGA. Factory default is +3.3v
- +VCCO1 is the bank-1 I/O voltage to the FPGA. Factory default is +3.3v

### Power Budget

The table below can help you determine your power budget for each supply rail on the XEM6010. All values are highly dependent on the application, speed, usage, and so on. Entries we have made are based on typical values presented in component datasheets or approximations based on Xilinx power estimator results. Shaded boxes represent unconnected rails to a particular component. Empty boxes represent data that the user must provide based on power estimates.

The user may also need to adjust parameters we have already estimated (such as FPGA $V_{CCO}$ values) where appropriate.

| Component(s) | 1.2v | 1.8v | 3.3v |
|---|---|---|---|
| USB 2.0, PLL | | | 320 mW |
| DDR2 | | 600 mW | 250 mW |
| FPGA VCCINT | | | |
| FPGA VCCAUX | | | 250 mW |
| FPGA VCCO3 (DDR2), est. | | 250 mW | |
| FPGA VCCO2 (USB), est. | | 250 mW | |
| FPGA VCCO0,1 | | | |
| **Total:** | | | |
| **Available:** | 2,400 mW | 3,600 mW | 6,600 mW |

## Example XEM6010-LX150 FPGA Power Consumption

XPower Estimator version 12.3 was used to compute the following power estimates for the VCCINT supply. These are simply estimates; your design requirements may vary considerably. The numbers below indicate approximately 70% to 80% utilization.

| Component | Parameters | VCCINT |
|---|---|---|
| Clock | 150 MHz GCLK - 70,000 fanout | 384 mW |
| Clock | 100 MHz GCLK - 70,000 fanout | 256 mW |
| Logic (DFF) | 150 MHz, 70,000 DFFs | 380 mW |
| Logic (DFF) | 100 MHz, 70,000 DFFs | 232 mW |
| Logic (LUT) | 150 MHz, 32,000 Combinatorial, 1,000 SR, 1,000 RAM | 287 mW |
| Logic (LUT) | 100 MHz, 32,000 Combinatorial, 1,000 SR, 1,000 RAM | 191 mW |
| BRAM | 18-bit, 100 @ 150 MHz, 100 @ 100 MHz | 237 mW |
| DSP | 150 MHz, 140 slices | 78 mW |
| MCB | 150 MHz | 85 mW |
| Misc. | DCM, PLL, etc. | 100 mW |
| | **Total:** | 2,230 mW |
| | **Available:** | 2,400 mW |

## Supply Heat Dissipation (IMPORTANT!!)

Due to the limited area available on the small form-factor of the XEM6010 and the density of logic provided, heat dissipation may be a concern. This depends entirely on the end application and cannot be predicted in advance by Opal Kelly. Heat sinks may be required on any of the devices on the XEM6010. Of primary focus should be the FPGA (U10) and SDRAM (U11). Although the switching supplies are high-efficiency, they are very compact and consume a small amount of PCB area for the current they can provide.

If you plan to put the XEM6010 in an enclosure, be sure to consider heat dissipation in your design.

# Host Interface

There are 26 pins that connect the on-board USB microcontroller to the FPGA. These pins comprise the host interface on the FPGA and are used for configuration downloads. After configuration, these pins are used to allow FrontPanel communication with the FPGA.

If the FrontPanel okHost module is instantiated in your design, you must map the interface pins to specific pin locations using Xilinx LOC constraints. This may be done using the Xilinx constraints editor or specifying the constraints manually in a text file. Please see the sample projects included with your FrontPanel installation for examples.

## MUXSEL

MUXSEL is a signal on the XEM6010 which selects the signal path to the FPGA programming signals D0 and CCLK. When low (deasserted), the FPGA and USB microcontroller are connected. When high (asserted), the FPGA and PROM are connected.

In normal USB-programmed operation, JP5 is in the USB position connecting the FPGA and USB microcontroller at all times. This allows USB-based programming of the FPGA and subsequent USB communication with the FPGA design after configuration.

In order to allow the SPI to configure the FPGA, JP5 must be in the PROM position.. In order to deassert MUXSEL post-configuration, your design must deassert MUXSEL. This allows the FPGA design to properly startup and allows for communication over USB even after the PROM has configured it.

The end result is that your FPGA design should tie HI_MUXSEL to 0. This is the case regardless of how the design was configured (via PROM or USB). For example, in Verilog:

```
assign hi_muxsel = 1'b0;
```

## I²C Connections

The FPGA on the XEM6010 is attached to the I²C lines from the USB microcontroller. In order to avoid contention with the I²C bus, these lines should be set to high-impedance within your design. If this is not done, FrontPanel may timeout or hang when trying to communicate with the XEM6010, particularly when programming the on-board PLL.

The following lines in your UCF (contraints) file will attach pull-ups to the I²C lines:

```
NET "i2c_sda"   LOC = "AB9"   | IOSTANDARD="LVCMOS33" | PULLUP;
NET "i2c_scl"   LOC = "Y9"    | IOSTANDARD="LVCMOS33" | PULLUP;
```

In addition, you will need to set these signals to high-impedance in your HDL. Here is an example of how to do this in Verilog:

```
assign i2c_sda = 1'bz;
assign i2c_scl = 1'bz;
```

# SPI Flash

The SPI flash on the module is a Numonyx M25P32-VME6G or equivalent. It can be programmed (using the FlashLoader sample) with an FPGA configuration bitfile to configure the

FPGA on boot. To boot the FPGA from flash, the switch JP5 must be slid to the "PROM" position. To boot the FPGA using FrontPanel, the switch must be slid to the "USB" position. In both cases, FrontPanel communication is available after configuration completes.

| Flash Pin | FPGA Pin |
|---|---|
| C | W12 |
| S | T5 |
| D | AB15 |
| Q | Y15 |

### FlashLoader Sample

The FlashLoader sample is installed with your FrontPanel installation. It is a simple command-line utility that you can use to program the SPI flash with an FPGA configuration file. Please see the Samples directory for more information.

You can also load a configuration file to the Flash using your own HDL, of course. There is nothing special about the way our FlashLoader sample loads the configuration file into the Flash.

## LEDs

There are eight LEDs on the XEM6010. Each is wired directly to the FPGA according to the pin mapping tables at the end of this document.

The LED anodes are connected to a pull-up resistor to +3.3VDD and the cathodes wired directly to the FPGA on Bank 2 with a bank I/O voltage of 3.3v. To turn ON an LED, the FPGA pin should be brought low. To turn OFF an LED, the FPGA pin should be at logic '1'.

## DDR2 SDRAM

The Micron DDR2 SDRAM is connected exclusively to the 1.8-v I/O on Bank 3 of the FPGA. The tables below list these connections.

| DDR2 Pin | FPGA Pin |
|---|---|
| CK | H4 |
| $\overline{\text{CK}}$ | H3 |
| CKE | D2 |
| $\overline{\text{CS}}$ | C3 |
| $\overline{\text{RAS}}$ | K5 |
| $\overline{\text{CAS}}$ | K4 |
| $\overline{\text{WE}}$ | F2 |
| LDQS | L3 |
| $\overline{\text{LDQS}}$ | L1 |
| UDQS | T2 |
| $\overline{\text{UDQS}}$ | T1 |
| LDM | L4 |
| UDM | M3 |
| ODT | J6 |
| A0 | H2 |
| A1 | H1 |
| A2 | H5 |
| A3 | K6 |
| A4 | F3 |
| A5 | K3 |
| A6 | J4 |
| A7 | H6 |
| A8 | E3 |

| DDR2 Pin | FPGA Pin |
|---|---|
| A9 | E1 |
| A10 | G4 |
| A11 | C1 |
| A12 | D1 |
| BA0 | G3 |
| BA1 | G1 |
| BA2 | F1 |
| D0 | N3 |
| D1 | N1 |
| D2 | M2 |
| D3 | M1 |
| D4 | J3 |
| D5 | J1 |
| D6 | K2 |
| D7 | K1 |
| D8 | P2 |
| D9 | P1 |
| D10 | R3 |
| D11 | R1 |
| D12 | U3 |
| D13 | U1 |
| D14 | V2 |
| D15 | V1 |

## Clock Configuration (Source Synchronous)

The DDR2 clocking is designed to be source-synchronous from the FPGA. This means that the FPGA sends the clock signal directly to the SDRAM along with control and data signals, allowing very good synchronization between clock and data.

## Memory Controller Blocks

Spartan-6 has integrated memory control blocks to communicate with the external DDR2 memory on the XEM6010. This is instantiated using the Xilinx Core Generator (memory interface generator, or MIG) to create a suitable memory controller for your design. You should read and become familiar with the DDR2 SDRAM datasheet as well as MIG and the core datasheet. Although MIG can save a tremendous amount of development time, understanding all this information is critical to building a working DDR2 memory interface.

The XEM6010 provides 1.2v as VCCINT. According to the memory controller block documentation, the Spartan-6, -2 speed grade can operate memory to 312.5 MHz with this internal voltage.

## MIG Settings

The following are the settings used to generate the MIG core for our RAMTester sample using Xilinx Core Generator. These settings were used with ISE 12.2 and MIG 2.3. Note that settings may be slightly different for different versions of ISE or MIG.

| | | |
|---|---|---|
| Frequency | 312.5 MHz | |
| Memory Type | Component | |
| Memory Part | MT47H64M16XX-3 (1Gb, x16) | |
| Data Width | 16 | |
| Enable DQS Enable | CHECKED | |
| High-temp self-refresh | DISABLED | |
| Output drive strength | Reducedstrength | |
| RTT(nominal) | 50 ohms | [default] |
| DCI for DQ/DQS | CHECKED | |
| DCI for address/control | CHECKED | |
| ZIO pin | Y2 | |
| RZQ pin | K7 | |
| Calibrated Input Selection | Yes | |
| Class for address/control | Class II | |
| Debug signals | Your option | |
| System clock | Differential | |

# JTAG

The JTAG connections on the FPGA are wired directly to the expansion connector JP2 on the XEM6010 to facilitate FPGA configuration and ChipScope usage using a Xilinx JTAG cable. The BRK6110 has these signals connected to a 2-mm header compatible with the Xilinx JTAG cable.

# Key Memory Storage (LX150 only, PCB revision 20120510 and newer)

Note: This information is valid only for PCB revisions 20120510 and newer.

The Spartan-6 FPGA supports design security using AES decryption logic and provides two methods for encryption key memory storage. The first is a volatile memory storage supported by an external battery backup supply voltage (VBATT). The second is a one-time programmable eFUSE. The XEM6310 design supports both types of key storage with user-modification required.

For quantity purchases of 50 or more units, please contact Opal Kelly (sales@opalkelly.com) to discuss factory installation of these components.

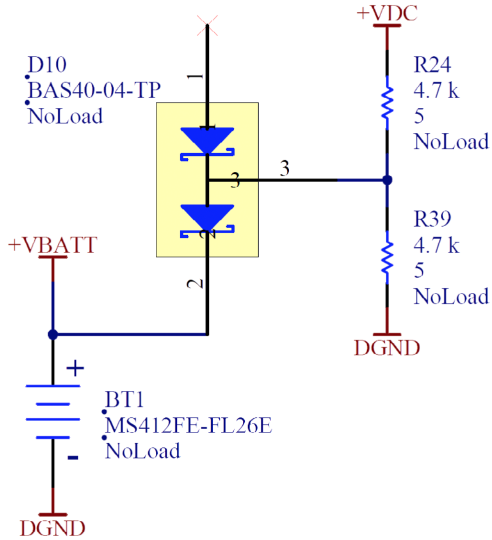
## Volatile Encryption Key Storage (VBATT)

A small lithium rechargeable battery and three support components can be installed to provide VBATT to the FPGA when the XEM is unpowered. This will preserve the contents of the FPGA's volatile key storage so long as VBATT remains over the threshold specified in the Spartan-6 documentation. Please see the Xilinx *Spartan-6 FPGA Configuration User Guide* (UG380) for more details. Alternatively, VBATT may be provided through JP2-3. In this case, BT1 should not be installed.

The applicable schematic section and components required to support this functionality are shown below.

| RefDes | Manufacturer | Manufacturer P/N | Comment |
|---|---|---|---|
| BT1 | Seiko Instruments | MS412FE-FL26E | 3V, 1mAh lithium battery |
| D10 | Micro Commercial | BAS40-04-TP | Schottky Diode, SOT23 |
| C11 | Generic | 0.1 µF, SM-0402 | Decoupling |

| RefDes | Manufacturer | Manufacturer P/N | Comment |
|---|---|---|---|
| R24, R39 | Generic | 4.7 kΩ, 5%, SM-0402 | |
| R41 | Generic | 0 Ω, SM-0402 | Connects VBATT to JP2-3 |




### Non-Volatile Encryption Key Storage (eFUSE)

Non-volatile storage of the encryption key is also possible by programming the Spartan-6 eFUSE via JTAG. Please see the Xilinx *Spartan-6 FPGA Configuration User Guide* (UG380) for more details.

To program the eFUSE, you must first install the components listed in the table below. You must also provide an external resistor (RFUSE) between JP2-12 and GND. The value of this resistor is specified in the Xilinx *Spartan-6 Datasheet* (DS162) between 1129 Ω and 1151 Ω.

| RefDes | Manufacturer | Manufacturer P/N | Comment |
|---|---|---|---|
| C10 | Generic | 0.1 µF, SM-0402 | Decoupling |
| R40 | Generic | 0 Ω, SM-0402 | Connects FPGA VFS to +3.3v |
| R42 | Generic | 0 Ω, SM-0402 | Connects FPGA RFUSE to JP2-12 |

## Expansion Connectors

Opal Kelly Pins is an interactive online reference for the expansion connectors on all Opal Kelly FPGA integration modules. It provides additional information on pin capabilities, pin characteristics, and PCB routing. Additionally, Pins provides a tool for generating constraint files for place and route tools. Pins can be found at the URL below.

http://www.opalkelly.com/pins

## JP2

JP2 is an 80-pin high-density connector providing access to FPGA Bank 1. Several pins (38, 40, 54, 58, 59, 61, 77, and 79) of this connector are wired to global clock inputs on the FPGA and can therefore be used as inputs to the global clock network.

Pin JP2-10 is connected to the VREF pins of Bank 1.

Pin mappings for JP2 are listed at the end of this document in the "Quick Reference" section. For each pin, the corresponding board connection is listed. For pins connected to the FPGA, the corresponding FPGA pin number is also shown. Finally, for pins routed to differential pair I/Os on the FPGA, the FPGA signal names and routed track lengths have been provided to help you equalize lengths on differential pairs.

## JP3

JP3 is an 80-pin high-density connector providing access to FPGA Banks 0 and 1. Several pins (42, 44, 59, 61, 64, 66, 77, and 79) of this connector are wired to global clock inputs on the FPGA and can therefore be used as inputs to the global clock network.

Pin mappings for JP3 are listed at the end of this document in the "Quick Reference" section. For each pin, the corresponding board connection is listed. For pins connected to the FPGA, the corresponding FPGA pin number is also shown. Finally, for pins routed to differential pair I/Os on the FPGA, the FPGA signal names and routed track lengths have been provided to help you equalize lengths on differential pairs.

## Setting I/O Voltages

The Spartan-6 FPGA allows users to set I/O bank voltages in order to support several different I/O signalling standards. This functionality is supported by the XEM6010 by allowing the user to connect independent supplies to the FPGA VCCO pins on two of the FPGA banks.

By default, ferrite beads have been installed that attach each VCCO bank to the +3.3VDD supply. If you intend to supply power to a particular I/O bank, you MUST remove the appropriate ferrite beads. Power can then be supplied through the expansion connectors.

The table below lists details for user-supplied I/O bank voltages

| I/O Bank | Expansion Pins | Ferrite Bead |
|---|---|---|
| 0 | JP3-36, 56 | FB2 |
| 1 | JP2-35, 55 | FB1 |

## Considerations for Differential Signals

The XEM6010 PCB layout and routing has been designed with several applications in mind, including applications requiring the use of differential (LVDS) pairs. Please refer to the Xilinx Spartan-6 datasheet for details on using differential I/O standards with the Spartan-6 FPGA.

Note: LVDS output on the Spartan-6 is restricted to banks 0 and 2. LVDS input is available on all banks. For more information, please refer to the *Spartan-6 FPGA SelectIO Resources User Guide* from Xilinx.

### FPGA I/O Bank Voltages

In order to use differential I/O standards with the Spartan-6, you must set the VCCO voltages for the appropriate banks to 2.5v according to the Xilinx Spartan-6 datasheet. Please see the section above entitled "Setting I/O Voltages" for details.

### Characteristic Impedance

The characteristic impedance of all routes from the FPGA to the expansion connector is approximately 50-Ω.

### Differential Pair Lengths

In many cases, it is desirable that the route lengths of a differential pair be matched within some specification. Care has been taken to route differential pairs on the FPGA to adjacent pins on the expansion connectors whenever possible. We have also included the lengths of the board routes for these connections to help you equalize lengths in your final application. Due to space constraints, some pairs are better matched than others.

### Reference Voltage Pins (VREF)

The Xilinx Spartan-6 supports externally-applied input voltage thresholds for some input signal standards. The XEM6010 supports these VREF applications for banks 0 and 1:

For Bank 0, the four VREF pins are routed to expansion connector JP3 on pins 48, 51, 62, and 65. Note that all four must be connected to the same voltage for proper application of input thresholds. Please see the Xilinx Spartan-6 documentation for more details.

For Bank 1, the four VREF pins are connected to a single pin on expansion connector JP2, pin 10.

## BRK6110 Breakout Board

The BRK6110 is a simple two-layer "breakout board" which can be used to evaluate or transition to the XEM6010. It provides standard 2-mm thru-hole connections to the 0.8-mm high-density connectors on the XEM6010 and a DC power connector (2.1mm/5.5mm, center positive) for providing +VDC to the XEM6010. Please visit the Pins reference for the XEM6010 for pin mapping details.

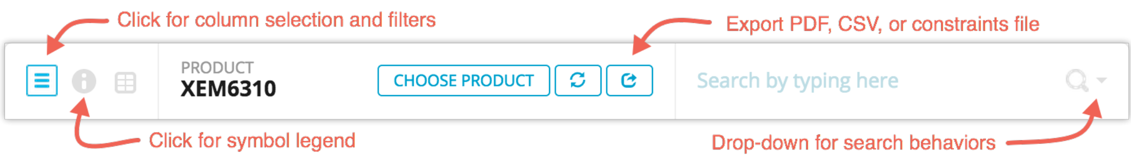
## Pins

Opal Kelly Pins is an interactive online reference for the expansion connectors on all Opal Kelly FPGA integration modules. It provides additional information on pin capabilities, pin characteristics, and PCB routing. Additionally, Pins provides a tool for generating constraint files for place and route tools. Pins can be found at the URL below.

**http://www.opalkelly.com/pins**

### Toolbar

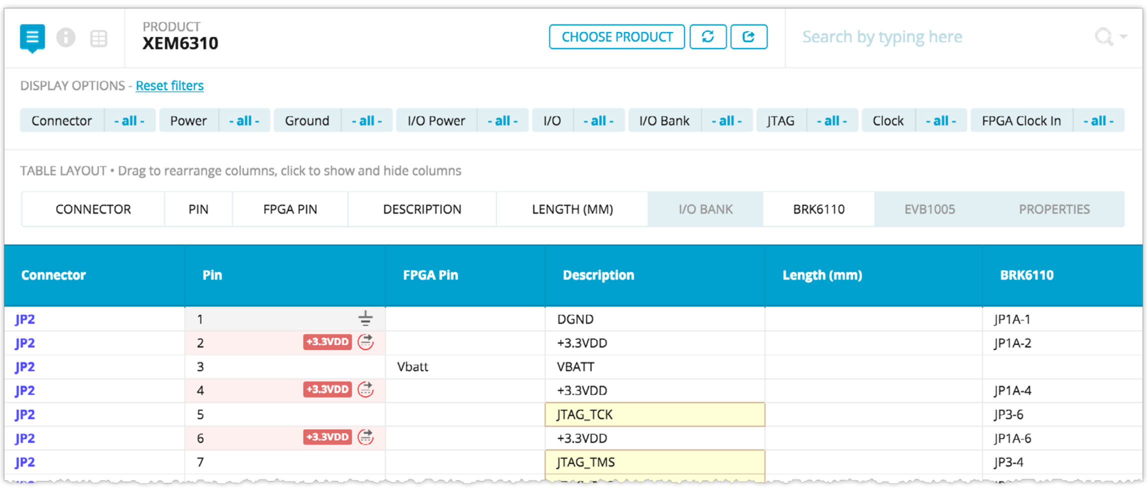
The toolbar at the top of a Pins product page has a number of features. Explore a bit; you won't break it.




## Pin Lists

As the primary reference for Opal Kelly integration module expansion connectors, Pin Lists contain a comprehensive table of the FPGA-to-Connector data including connector pin, FPGA pin, signal description, routed length (when applicable), breakout board pin mapping, FPGA I/O bank, and other properties.

By default, not all data columns are visible. Click on the "Toggle Filters" icon at the top-left to select which columns to show. Depending on the specific module, several additional columns may be shown. The data in these columns is always exported when you export the pin list to CSV.




## Filters

You can hide or show the additional information associated with each signal by clicking on the icon at the top left ("Toggle Filters"). Use these filters to limit the visible pin listing to particular subsets of signals you are interested in.

## Search

You can search the pin list using the search entry at the top-right. Click on the magnifying glass drop-down to adjust the function of the search to one of:

- Highlight - Highlights search results only.
- Hide Matching - Hides rows where search matches are found.
- Show Only Matching - Shows only rows where a search match is found.

## Export (PDF, CSV, Constraints Files)

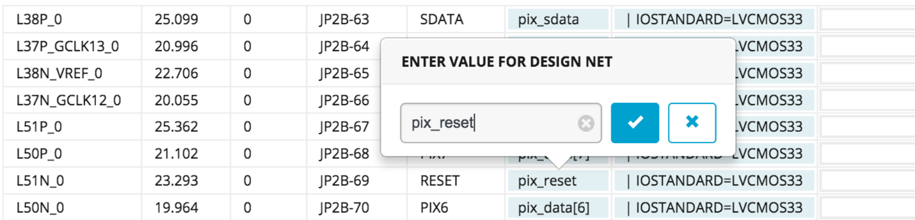
The export button near the search entry allows you to export the pin list in several formats. PDFs can be viewed or printed. CSV can be loaded into a spreadsheet application or manipulated with scripts. Constraints files can be used as inputs to Xilinx and Altera synthesis and mapping tools.

The constraints files include additional mapping information for other peripherals on the module such as memory, clock oscillators, and LEDs.

## Peripherals

A Pins Peripheral is a project definition where you can enter your top-level HDL design nets to have Pins generate a complete constraint file for you.

When you create a Peripheral, you will select a target integration module. The Peripheral is paired to this module so that the design parameters match the features and expansion capabilities of the module.




### Specifying Net Names

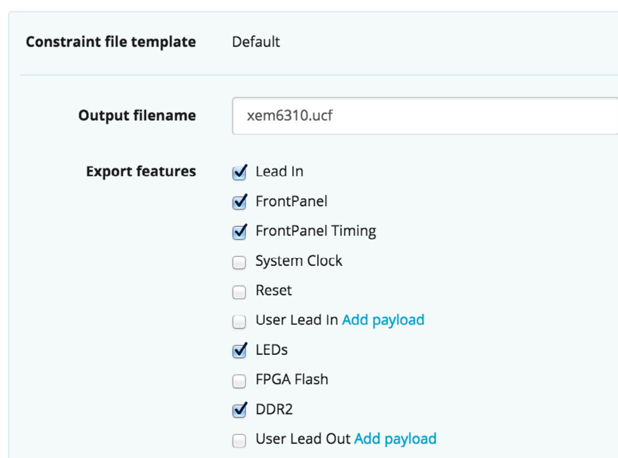
The Pin List view for a Peripheral includes three additional, editable columns:

- Design Net - The name of the signal as it appears in your top-level HDL.
- Constraints - Text that is inserted into the constraints file for that signal.
- Comment - Additional comment text that is added to the constraints file.

These additional data are merged with the default Pin List constraints file prior to export. The result is a constraints file complete with net names that can be used with your FPGA development flow.

### Export Features

Enable the specific module features you would like to appear in the exported constraints file. When a feature is enabled, Pins will export the constraints appropriate to that feature such as pin locations. When a feature is disabled, Pins will skip that portion.




The User Lead In and User Lead Out sections allow you to add custom payloads (your own constraints) that will be added to the exported constraints file. Additional timing constraints or comments can be added here.

# Migrating from the XEM3010 to the XEM6010

The XEM6010 was designed to be as compatible as possible with our XEM3010 in order to facilitate customer design migration with minimal changes. The physical dimentions and connector footprints are identical. The differences between these two products are highlighted below.

## Four I/O Banks → Two I/O Banks

The Spartan-3 device used on the XEM3010 has eight I/O banks, four of which are routed to the expansion connectors. Each of these four has selectable I/O bank voltages. The Spartan-6 device on the XEM6010 only has four total I/O banks, two of which are routed to the expansion connectors. This is a consideration in designs where multiple I/O bank voltages were used.

Note: LVDS output on the Spartan-6 is restricted to banks 0 and 2. LVDS input is available on all banks. For more information, please refer to the *Spartan-6 FPGA SelectIO Resources User Guide* from Xilinx.

## 32 MiB SDR SDRAM → 128 MiB DDR2 SDRAM

The XEM3010 has 32 MiB of on-board single-data-rate SDRAM. The XEM6010 replaces this with a faster, higher-capacity 128-MiB double-data-rate SDRAM. The Spartan-6 also has an internal memory control block (MCB) which provides a DDR2 controller to designs without consuming significant FPGA fabric.

## Two Pushbuttons → No Pushbuttons

Due to space constraints, the XEM6010 does not have on-board pushbuttons.

## Expansion Connector Differences

The following table lists the expansion connector differences:

| XEM3010 | XEM6010 |
|---|---|
| JP2-3 is +2.5VDD | JP2-3 is a no-connect |
| JP2-10 is a no-connect | JP2-10 is VREF_BANK1 |
| JP2-35 is +VCCO3 | JP2-35 is +VCCO1 |
| JP2-55 is +VCCO2 | JP2-55 is +VCCO1 |
| JP3-7 is a no-connect | JP3-7 is +1.8VDD |
| JP3-36 is +VCCO6 | JP3-36 is +VCCO0 |
| JP3-56 is +VCCO7 | JP3-56 is +VCCO0 |

## JTAG Connectivity

The XEM3010 has a header for connecting the Xilinx JTAG Platform Cable. Boards attached to the XEM3010 expansion connectors see TCK, TMS, TDI as inputs and TDO as an output. Therefore, from the perspective of the attached board, the XEM3010 is the JTAG controller.

The XEM6010 does not have a header for the Xilinx Platform Cable. This role has been migrated to the BRK6110 or other attached board. Boards attached to the XEM6010 provide TCK, TMS, TDI as outputs to the XEM6010 and receive TDO as an input from the XEM6010. Therefore, from the perspective of the attached board, the XEM6010 is a JTAG device.

# Migrating from the XEM3050 to the XEM6010

The XEM6010 was designed to be as compatible as possible with our XEM3010 in order to facilitate customer design migration with minimal changes. As a result, the XEM6010 is also positioned to replace the XEM3050 in many applications. Depending on logic requirements, the XEM6010-LX45 or XEM6010-LX150 could replace the XEM3050.

## Four I/O Banks → Two I/O Banks

The Spartan-3 device used on the XEM3050 has eight I/O banks, four of which are routed to the expansion connectors. Each of these four has selectable I/O bank voltages. The Spartan-6 device on the XEM6010 only has four total I/O banks, two of which are routed to the expansion connectors. This is a consideration in designs where multiple I/O bank voltages were used.

Note: LVDS output on the Spartan-6 is restricted to banks 0 and 2. LVDS input is available on all banks. For more information, please refer to the *Spartan-6 FPGA SelectIO Resources User Guide* from Xilinx.

## 64 MiB SDR SDRAM → 128 MiB DDR2 SDRAM

The XEM3050 has 64 MiB of on-board single-data-rate SDRAM available as two 32 MiB devices. The XEM6010 replaces this with a faster, higher-capacity 128-MiB double-data-rate SDRAM. The Spartan-6 also has an internal memory control block (MCB) which provides a DDR2 controller to designs without consuming significant FPGA fabric.

## Synchronous SRAM Removed

The XEM6010 does not have the 9 MiB synchronous SRAM that is on the XEM3050.

## Expansion Connector Differences

The following table lists the expansion connector differences:

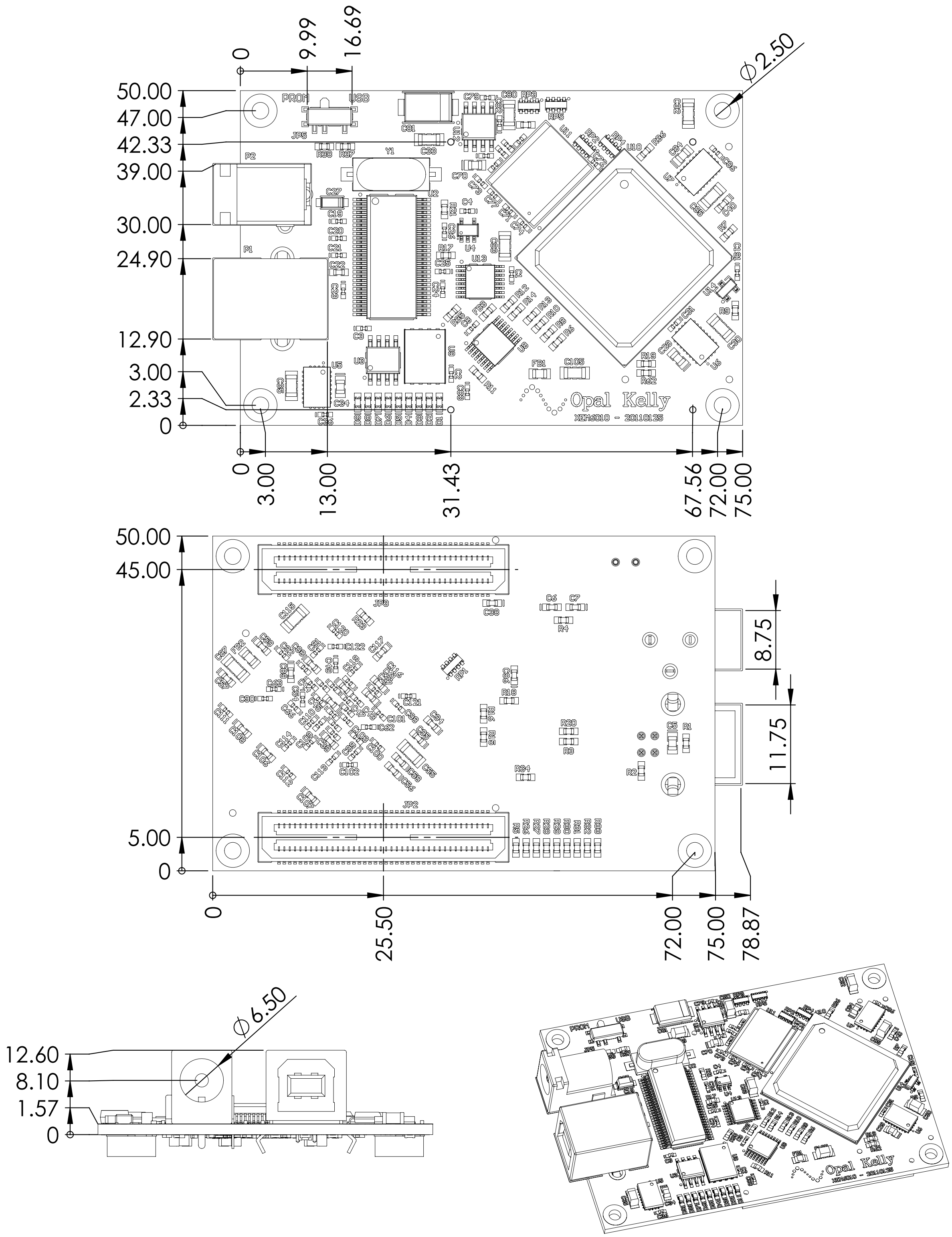
| XEM3050 | XEM6010 |
|---|---|
| JP2-3 is +2.5VDD | JP2-3 is a no-connect |
| JP2-10 is a no-connect | JP2-10 is VREF_BANK1 |
| JP2-35 is +VCCO3 | JP2-35 is +VCCO1 |
| JP2-55 is +VCCO2 | JP2-55 is +VCCO1 |
| JP3-7 is SYS_CLK6 | JP3-7 is +1.8VDD |
| JP3-36 is +VCCO6 | JP3-36 is +VCCO0 |
| JP3-56 is +VCCO7 | JP3-56 is +VCCO0 |

## JTAG Connectivity

The XEM3050 has a header for connecting the Xilinx JTAG Platform Cable. Boards attached to the XEM3050 expansion connectors see TCK, TMS, TDI as inputs and TDO as an output. Therefore, from the perspective of the attached board, the XEM3050 is the JTAG controller.

The XEM6010 does not have a header for the Xilinx Platform Cable. This role has been migrated to the BRK6110 or other attached board. Boards attached to the XEM6010 provide TCK, TMS, TDI as outputs to the XEM6010 and receive TDO as an input from the XEM6010. Therefore, from the perspective of the attached board, the XEM6010 is a JTAG device.

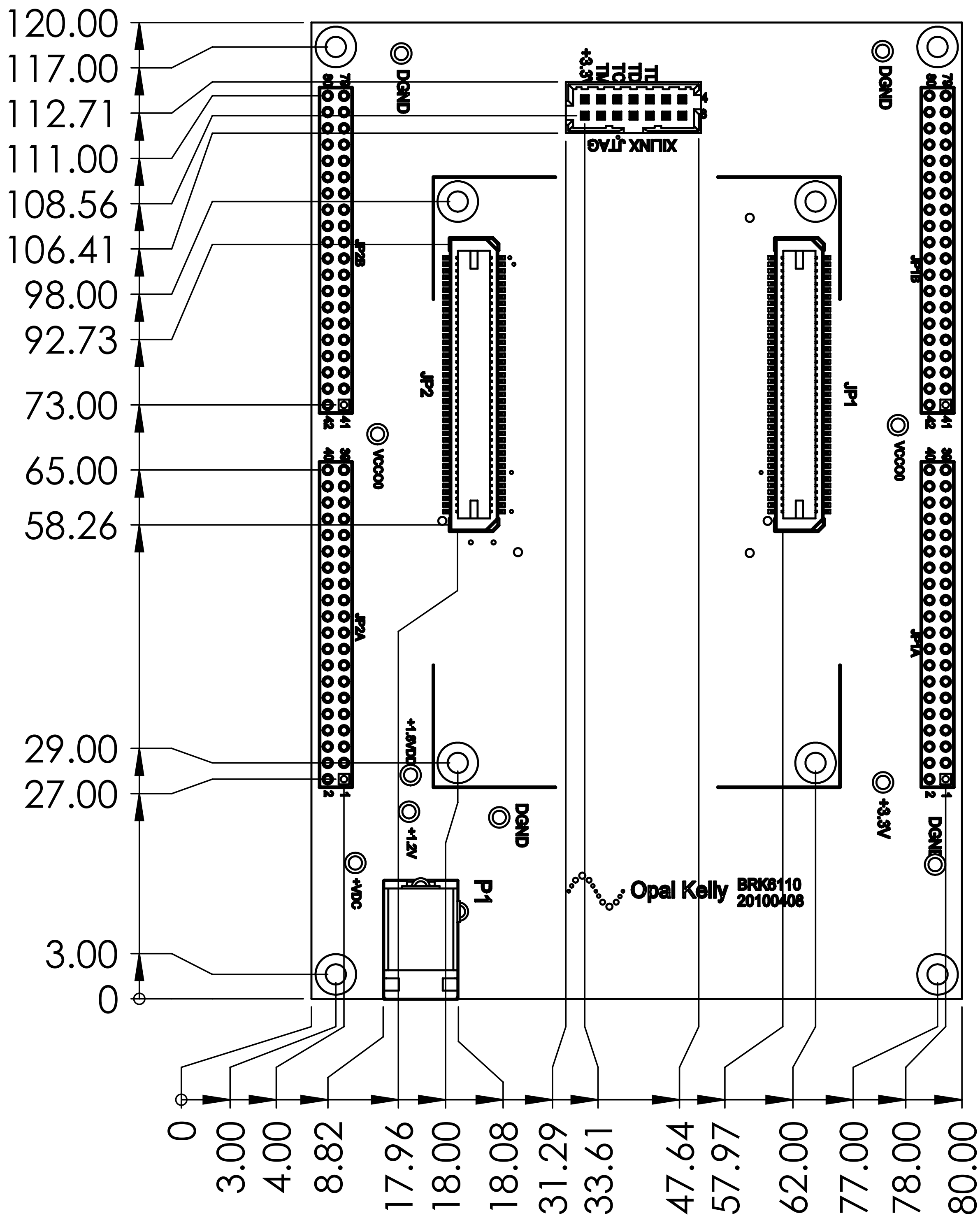
# XEM6010 Mechanical Drawing




All dimensions in mm

# BRK6110 Mechanical Drawing

All dimensions in mm.



# XEM6010 Quick Reference

| JP2 Pin | Connection | FPGA Pin | Length (mm) |
|---|---|---|---|
| 1 | DGND | | |
| 3 | - | | |
| 5 | JTAG_TCK | | |
| 7 | JTAG_TMS | | |
| 9 | JTAG_TDI | | |
| 11 | SYS_CLK4 | | |
| 13 | DGND | | |
| 15 | G16 | L9P_1 | 36.709 |
| 17 | G17 | L9N_1 | 35.889 |
| 19 | H19 | L34P_1 | 39.405 |
| 21 | H18 | L34N_1 | 36.649 |
| 23 | F16 | L10P_1 | 36,915 |
| 25 | F17 | L10N_1 | 37.537 |
| 27 | J17 | L36P_1 | 34.164 |
| 29 | K17 | L36N_1 | 32.463 |
| 31 | K16 | L21P_1 | 28.716 |
| 33 | J16 | L21N_1 | 29.917 |
| 35 | +VCCO1 | | |
| 37 | V21 | L52P_1 | 16.564 |
| 39 | V22 | L52N_1 | 16.617 |
| 41 | T21 | L50P_1 | 22.866 |
| 43 | T22 | L50N_1 | 21.947 |
| 45 | P21 | L48P_1 | 23.070 |
| 47 | P22 | L48N_1 | 22.213 |
| 49 | M21 | L46P_1 | 25.990 |
| 51 | M22 | L46N_1 | 24.527 |
| 53 | L20 | L45P_1 | 22.274 |
| 55 | +VCCO1 | | |
| 57 | L22 | L45N_1 | 20.797 |
| 59 | H21 | L41P_GCLK9_1 | 25.953 |
| 61 | H22 | L41N_GCLK8_1 | 25.014 |
| 63 | F21 | L37P_1 | 28.198 |
| 65 | F22 | L37N_1 | 26.589 |
| 67 | D21 | L31P_1 | 32.225 |
| 69 | D22 | L31N_1 | 31.347 |
| 71 | B21 | L19P_1 | 31.387 |
| 73 | B22 | L19N_1 | 30.050 |
| 75 | A21 | L20N_1 | 33.836 |
| 77 | J20 | L43P_GCLK5_1 | 24.102 |
| 79 | J22 | L43N_GCLK4_1 | 24.092 |

| JP2 Pin | Connection | FPGA Pin | Length (mm) |
|---|---|---|---|
| 2 | +3.3VDD | | |
| 4 | +3.3VDD | | |
| 6 | +3.3VDD | | |
| 8 | JTAG_TDO | | |
| 10 | VREF_1 | Bank 1 VREF | |
| 12 | - | | |
| 14 | DGND | | |
| 16 | G19 | L33P_1 | 60.218 |
| 18 | F20 | L33N_1 | 56.677 |
| 20 | H20 | L38P_1 | 52.874 |
| 22 | J19 | L38N_1 | 52.611 |
| 24 | D19 | L29P_1 | 47.404 |
| 26 | D20 | L29N_1 | 46.630 |
| 28 | F18 | L30P_1 | 39.799 |
| 30 | F19 | L30N_1 | 40.267 |
| 32 | M16 | L58P_1 | 27.342 |
| 34 | L15 | L58N_1 | 29.284 |
| 36 | DGND | | |
| 38 | K20 | L40P_GCLK11_1 | 29.040 |
| 40 | K19 | L40N_GCLK10_1 | 28.878 |
| 42 | U20 | L51P_1 | 23.279 |
| 44 | U22 | L51N_1 | 21.883 |
| 46 | R20 | L49P_1 | 26.161 |
| 48 | R22 | L49N_1 | 24.437 |
| 50 | N20 | L47P_1 | 26.759 |
| 52 | N22 | L47N_1 | 25.105 |
| 54 | M20 | L42P_GCLK7_1 | 21.180 |
| 56 | DGND | | |
| 58 | L19 | L42N_GCLK6_1 | 24.854 |
| 60 | K21 | L44P_1 | 24.187 |
| 62 | K22 | L44N_1 | 23.603 |
| 64 | G20 | L39P_1 | 27.676 |
| 66 | G22 | L39N_1 | 26.067 |
| 68 | E20 | L35P_1 | 31.492 |
| 70 | E22 | L35N_1 | 30.055 |
| 72 | C20 | L32P_1 | 33.935 |
| 74 | C22 | L32N_1 | 32.266 |
| 76 | A20 | L20P_1 | 34.325 |
| 78 | DGND | | |
| 80 | DGND | | |

| Host Interface Pin | FPGA Pin |
|---|---|
| HI_IN[0] | Y12 |
| HI_IN[1] | AB20 |
| HI_IN[2] | AB7 |
| HI_IN[3] | AB8 |
| HI_IN[4] | AA4 |
| HI_IN[5] | AB4 |
| HI_IN[6] | Y3 |
| HI_IN[7] | AB3 |
| HI_OUT[0] | Y19 |
| HI_OUT[1] | AA8 |
| HI_INOUT[0] | AB12 |
| HI_INOUT[1] | AA12 |
| HI_INOUT[2] | Y13 |
| HI_INOUT[3] | AB18 |
| HI_INOUT[4] | AA18 |
| HI_INOUT[5] | V15 |
| HI_INOUT[6] | AB2 |
| HI_INOUT[7] | AA2 |
| HI_INOUT[8] | Y7 |
| HI_INOUT[9] | Y4 |
| HI_INOUT[10] | W4 |
| HI_INOUT[11] | AB6 |
| HI_INOUT[12] | AA6 |
| HI_INOUT[13] | U13 |
| HI_INOUT[14] | U14 |
| HI_INOUT[15] | AA20 |
| HI_MUXSEL | AA22 |
| HI_AA | W11 |

| LED | FPGA Pin |
|---|---|
| D2 | Y17 |
| D3 | AB17 |
| D4 | AA14 |
| D5 | AB14 |
| D6 | AA16 |
| D7 | AB16 |
| D8 | AA10 |
| D9 | AB10 |

| PLL Pin | Clock Name | Connection |
|---|---|---|
| CLKA | SYS_CLK1 | FPGA - AB13 |
| CLKB | SYS_CLK2 | FPGA - Y11 |
| CLKC | SYS_CLK3 | FPGA - AB11 |
| CLKD | SYS_CLK4 | JP2-11 |
| CLKE | SYS_CLK5 | JP3-8 |
| XBUF | N/A | Not Connected |

# XEM6010 Quick Reference

| JP3 Pin | Connection | FPGA Pin | Length (mm) |
|---|---|---|---|
| 1 | +VDC | | |
| 3 | +VDC | | |
| 5 | +VDC | | |
| 7 | +1.8VDD | | |
| 9 | +3.3VDD | | |
| 11 | +3.3VDD | | |
| 13 | +3.3VDD | | |
| 15 | W20 | L60P_1 | 52.024 |
| 17 | W22 | L60N_1 | 53.341 |
| 19 | U19 | L70P_1 | 49.434 |
| 21 | V20 | L70N_1 | 50.801 |
| 23 | C5 | L2P_0 | 27.507 |
| 25 | A5 | L2N_0 | 27.626 |
| 27 | D14 | L49P_0 | 41.204 |
| 29 | C14 | L49N_0 | 37.149 |
| 31 | E16 | L66P_0 | 36.786 |
| 33 | D17 | L66N_0 | 37.192 |
| 35 | DGND | | |
| 37 | D7 | L32P_0 | 23.590 |
| 39 | D8 | L32N_0 | 24.146 |
| 41 | L17 | L61P_1 | 44.830 |
| 43 | K18 | L61N_1 | 44.133 |
| 45 | D6 | L3P_0 | 18.185 |
| 47 | C6 | L3N_0 | 17.482 |
| 49 | A3 | L1P_HSWAPEN_0 | 13.928 |
| 51 | A4 | L1N_VREF_0 | 13.018 |
| 53 | B8 | L6P_0 | 18.615 |
| 55 | DGND | | |
| 57 | A8 | L6N_0 | 17.038 |
| 59 | B10 | L34P_GCLK19_0 | 20.080 |
| 61 | A10 | L34N_GCLK18_0 | 18.748 |
| 63 | C13 | L38P_0 | 25.099 |
| 65 | A13 | L38N_VREF_0 | 22.706 |
| 67 | C15 | L51P_0 | 25.362 |
| 69 | A15 | L51N_0 | 23.293 |
| 71 | C17 | L64P_0 | 27.660 |
| 73 | A17 | L64N_0 | 25.374 |
| 75 | A18 | L65N_0 | 25.971 |
| 77 | C11 | L35P_GCLK17_0 | 18.067 |
| 79 | A11 | L35N_GCLK16_0 | 18.060 |

| JP3 Pin | Connection | FPGA Pin | Length (mm) |
|---|---|---|---|
| 2 | DGND | | |
| 4 | +1.2VDD | | |
| 6 | +1.2VDD | | |
| 8 | SYS_CLK5 | | |
| 10 | USB_SCL | | |
| 12 | USB_SDA | | |
| 14 | DGND | | |
| 16 | T19 | L74P_1 | 38.591 |
| 18 | T20 | L74N_1 | 40.628 |
| 20 | P17 | L72P_1 | 39.602 |
| 22 | N16 | L72N_1 | 33.852 |
| 24 | M17 | L71P_1 | 34.813 |
| 26 | M18 | L71N_1 | 34.914 |
| 28 | P18 | L73P_1 | 36.711 |
| 30 | R19 | L73N_1 | 39.280 |
| 32 | D9 | L7P_0 | 30.242 |
| 34 | C8 | L7N_0 | 26.971 |
| 36 | +VCCO0 | | |
| 38 | D10 | L33P_0 | 26.222 |
| 40 | C10 | L33N_0 | 25.323 |
| 42 | D11 | L36P_GCLK15_0 | 26.539 |
| 44 | C12 | L36N_GCLK14_0 | 26.506 |
| 46 | D15 | L62P_0 | 33.337 |
| 48 | C16 | L62N_VREF_0 | 32.259 |
| 50 | B6 | L4P_0 | 12.838 |
| 52 | A6 | L4N_0 | 12.356 |
| 54 | C7 | L5P_0 | 17.275 |
| 56 | +VCCO0 | | |
| 58 | A7 | L5N_0 | 12.741 |
| 60 | C9 | L8P_0 | 17.926 |
| 62 | A9 | L8N_VREF_0 | 14.028 |
| 64 | B12 | L37P_GCLK13_0 | 20.996 |
| 66 | A12 | L37N_GCLK12_0 | 20.055 |
| 68 | B14 | L50P_0 | 21.102 |
| 70 | A14 | L50N_0 | 19.964 |
| 72 | B16 | L63P_0 | 24.506 |
| 74 | A16 | L63N_0 | 22.571 |
| 76 | B18 | L65P_0 | 26.046 |
| 78 | DGND | | |
| 80 | DGND | | |