

The SN5405 is obsolete and no longer is supplied.

SN54LS05, SN54S05 SN7405, SN74LS05, SN74S05 HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

SDLS030A – DECEMBER 1983 – REVISED NOVEMBER 2003

- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

- Dependable Texas Instrument Quality and Reliability

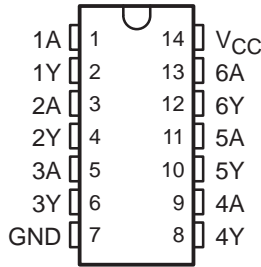
SN5405, SN54LS05, SN54S05 . . . J PACKAGE

SN7405 . . . N PACKAGE

SN74LS05 . . . D, DB, N, OR NS PACKAGE

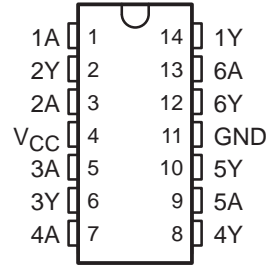
SN74S05 . . . D, N, OR NS PACKAGE

(TOP VIEW)



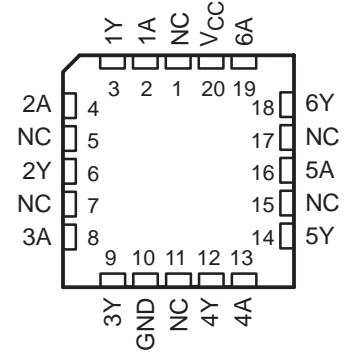
SN54LS05, SN54S05 . . . W PACKAGE

(TOP VIEW)



SN54LS05, SN54S05 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain six independent inverters. To perform correctly, the open-collector outputs require pullup resistors. These devices may be connected to other open-collector outputs to implement active-low wired-OR or active-high wire-AND functions. Open-collector devices often are used to generate high V_{OH} levels.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	PDIP – N	Tube	SN7405N	SN7405N	
			SN74LS05N	SN74LS05N	
			SN74S05N	SN74S05N	
	SOIC – D	Tube	SN74LS05D	LS05	
			Tape and reel		SN74LS05DR
			Tube	SN74S05D	S05
				Tape and reel	
SOP – NS	Tape and reel	SN74LS05NSR	74LS05		
		SN74S05NSR	74S05		
–55°C to 125°C	CDIP – J	Tube	SNJ54LS05J	SNJ54LS05J	
			SNJ54S05J	SNJ54S05J	
	CDIP – W	Tube	SNJ54LS05W	SNJ54LS05W	
			SNJ54S05W	SNJ54S05W	
	LCCC – FK	Tube	SNJ54LS05FK	SNJ54LS05FK	
SNJ54S05FK			SNJ54S05FK		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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INSTRUMENTS

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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SN7405, SN74LS05, SN74S05
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

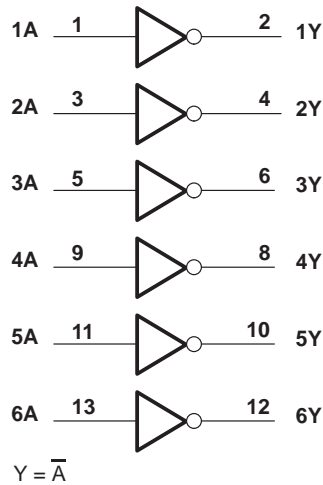
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FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, and NS packages.

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recommended operating conditions

	SN5405			SN7405			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5405			SN7405			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
I _{OH}	V _{CC} = MIN, V _{OH} = 5.5 V V _{IL} = 0.8 V V _{IL} = 0.7 V						0.25	mA
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V			40			40	µA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-1.6			-1.6	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		6	12		6	12	mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V		18	33		18	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	A	Y	R _L = 4 kΩ	C _L = 15 pF		40	55	ns
t _{PHL}			R _L = 400 Ω			8	15	



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recommended operating conditions

		SN54LS05			SN74LS05			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage				0.7			V
V _{OH}	High-level output voltage				5.5			V
I _{OL}	Low-level output current				4			mA
T _A	Operating free-air temperature	-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS05			SN74LS05			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IK}	V _{CC} = MIN, I _I = -18 mA				-1.5			V	
I _{OH}	V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 5.5 V				0.1			mA	
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V	I _{OL} = 4 mA		0.25		0.4		V	
		I _{OL} = 8 mA				0.35			
I _I	V _{CC} = MAX, V _I = 7 V				0.1			mA	
I _{IH}	V _{CC} = MAX, V _I = 2.7 V				20			µA	
I _{IL}	V _{CC} = MAX, V _I = 0.4 V				-0.4			mA	
I _{CCH}	V _{CC} = MAX, V _I = 0 V				1.2		2.4		mA
I _{CCL}	V _{CC} = MAX, V _I = 4.5 V				3.6		6.6		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A	Y	R _L = 2 kΩ, C _L = 15 pF	17		32	ns
t _{PHL}				15		28	



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recommended operating conditions

	SN54S05			SN74S05			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
V _{OH} High-level output voltage			5.5			5.5	V
I _{OL} Low-level output current			20			20	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54S05			SN74S05			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN,	I _I = -18 mA			-1.2			-1.2	V
I _{OH}	V _{CC} = MIN,	V _{OH} = 5.5 V					0.25		mA
		V _{IL} = 0.8 V							
		V _{IL} = 0.7 V			0.25				
V _{OL}	V _{CC} = MIN,	V _{IH} = 2 V, I _{OL} = 20 mA			0.5			0.5	V
I _I	V _{CC} = MAX,	V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX,	V _I = 2.7 V			50			50	µA
I _{IL}	V _{CC} = MAX,	V _I = 0.5 V			-2			-2	mA
I _{CCH}	V _{CC} = MAX,	V _I = 0 V		9	19.8		9	19.8	mA
I _{CCL}	V _{CC} = MAX,	V _I = 4.5 V		30	54		30	54	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

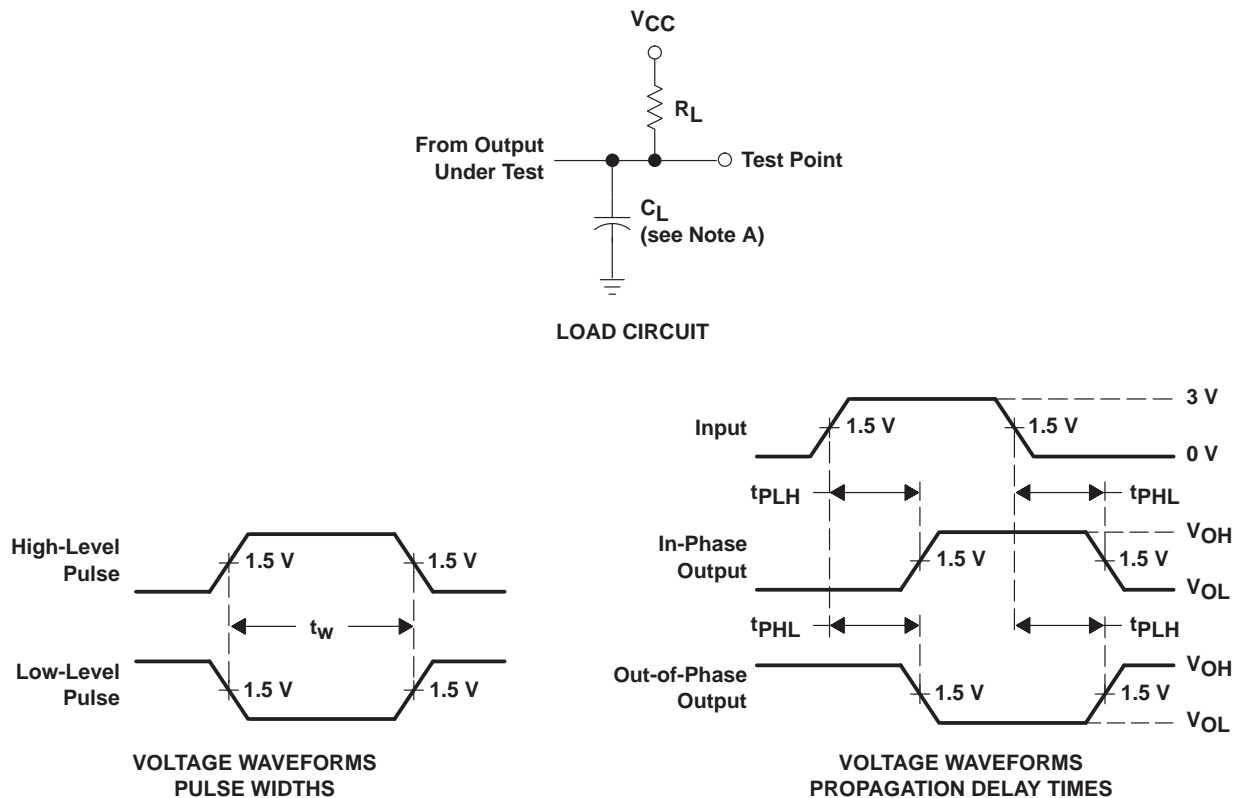
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	A	Y	R _L = 280 Ω	C _L = 15 pF	2	5	7.5	ns
t _{PHL}					2	4.5	7	
t _{PLH}				C _L = 50 pF	7.5	ns		
t _{PHL}					7			



PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 AND 54S/74S DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, and:
 For Series 54/74, $t_r \leq 7$ ns, $t_f \leq 7$ ns.
 For Series 54S/74S, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.

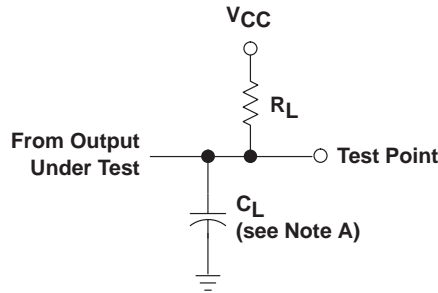
Figure 1. Load Circuit and Voltage Waveforms

**SN54LS05, SN54S05
SN7405, SN74LS05, SN74S05
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS**

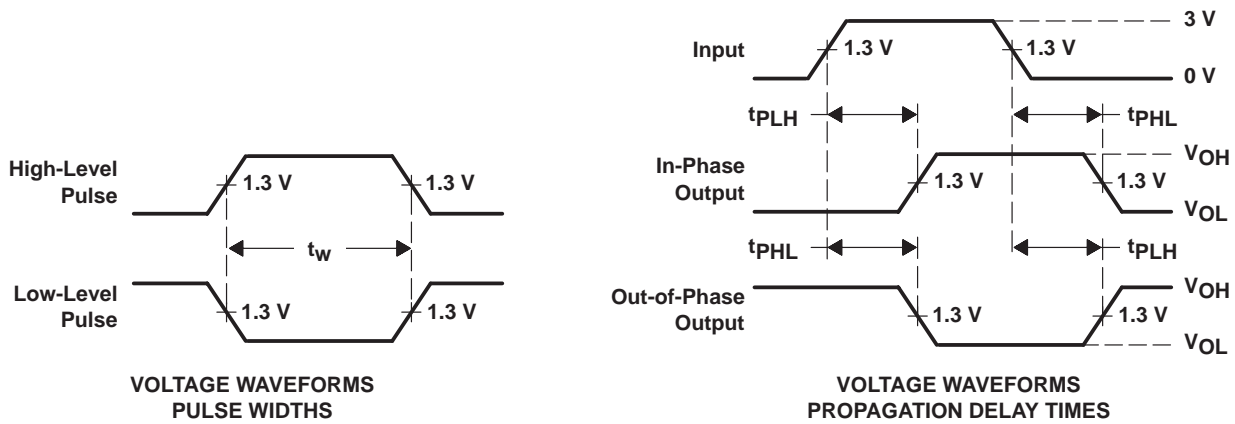
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**PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES**



LOAD CIRCUIT



- NOTES: A. C_L includes probe and jig capacitance.
 B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

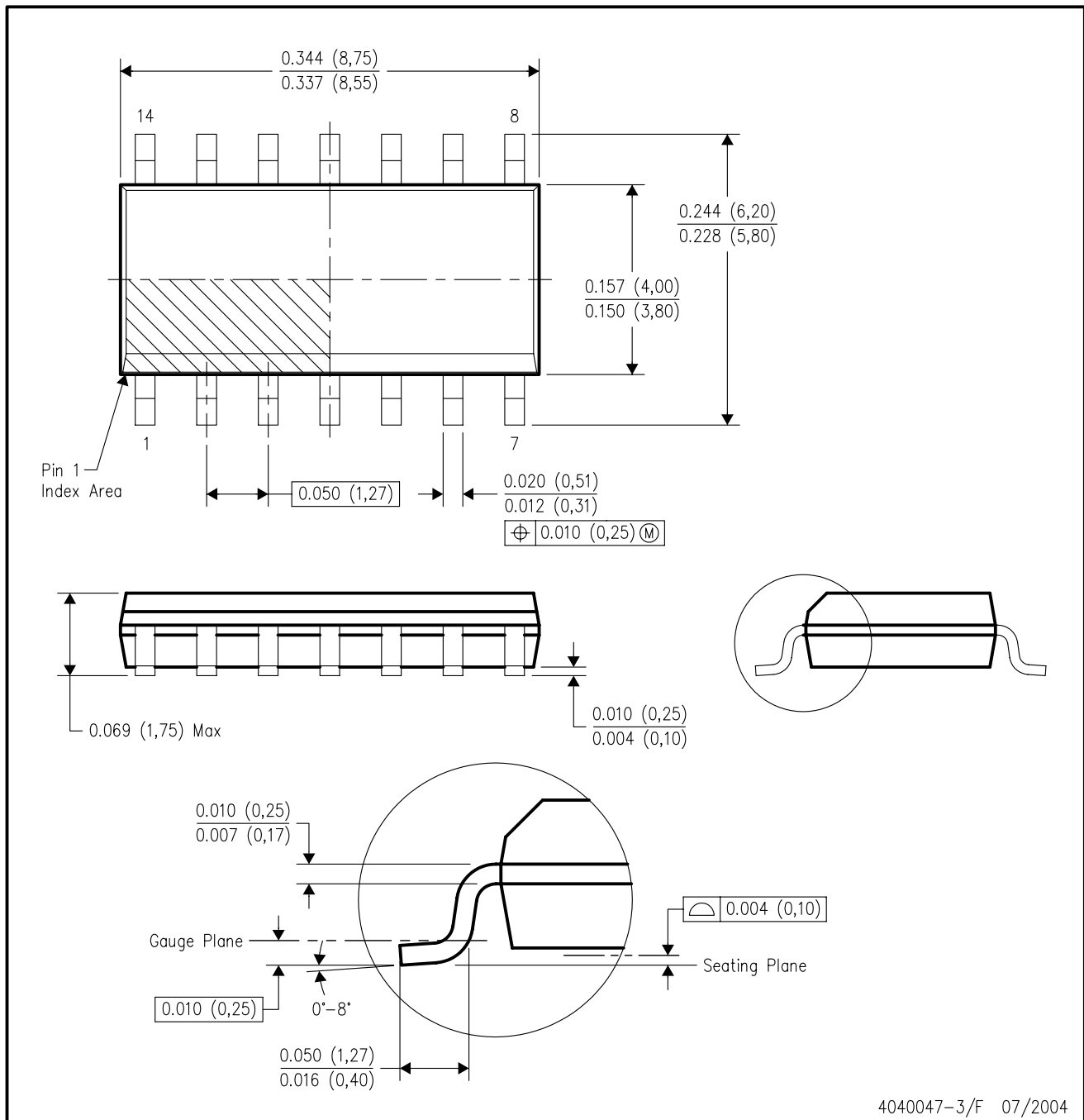


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

4040065 /E 12/01

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