Creating an R&D Ecosystem, p. 16

UP Media Group

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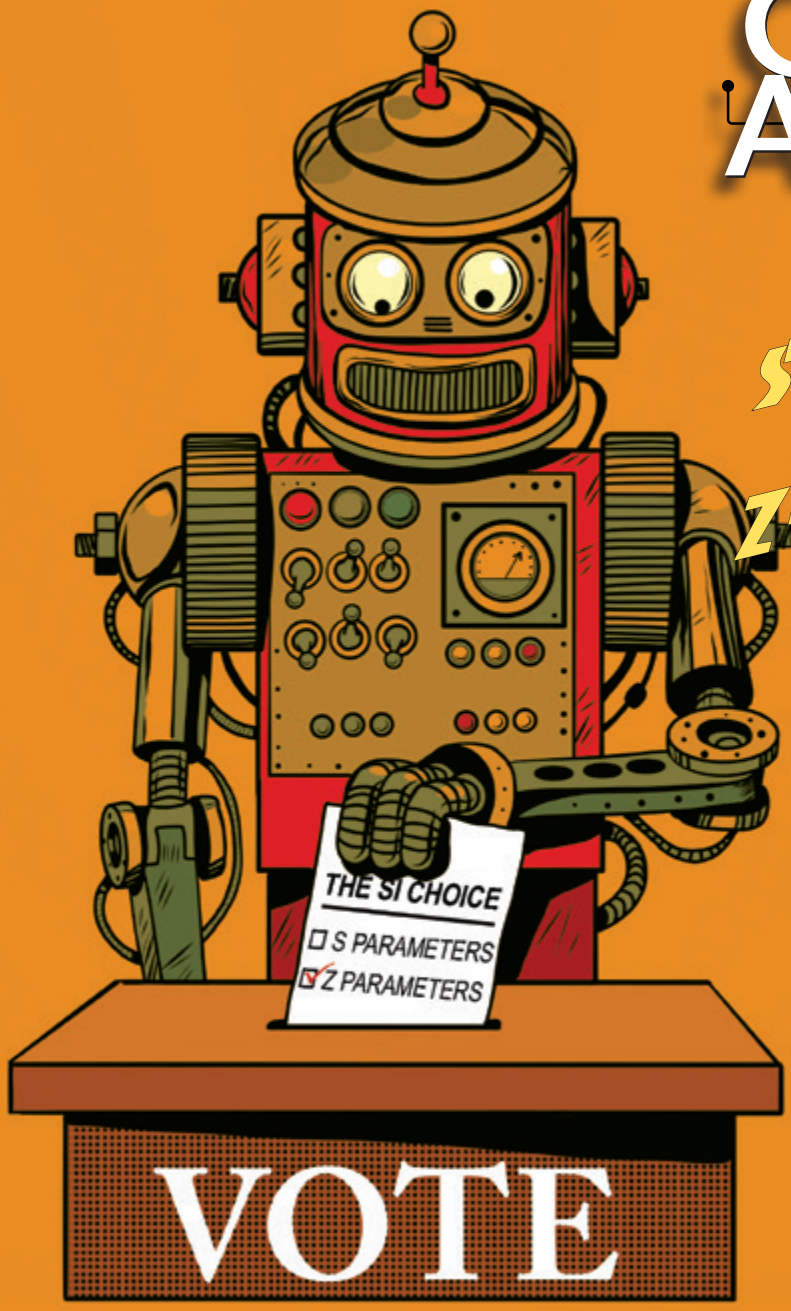
November 2020

PRINTED CIRCUIT DESIGN & FAB

CIRCUITS ASSEMBLY



S-PARAMETERS vs. Z-PARAMETERS: THE SI CHOICE

Accessing Edge Rates

How to HDI

X-ray Inspection of LTS Joints

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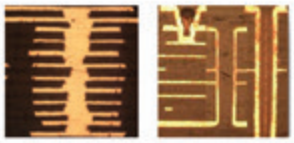
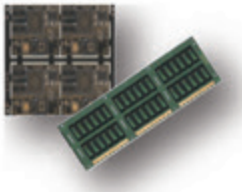
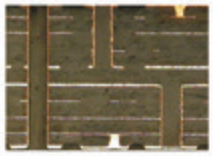
/ SSD Module

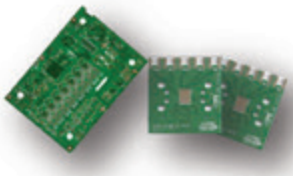


IOT / Build-up Board





Semiconductor TEST B'd
& 5G Network System



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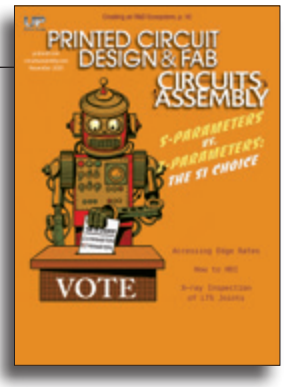

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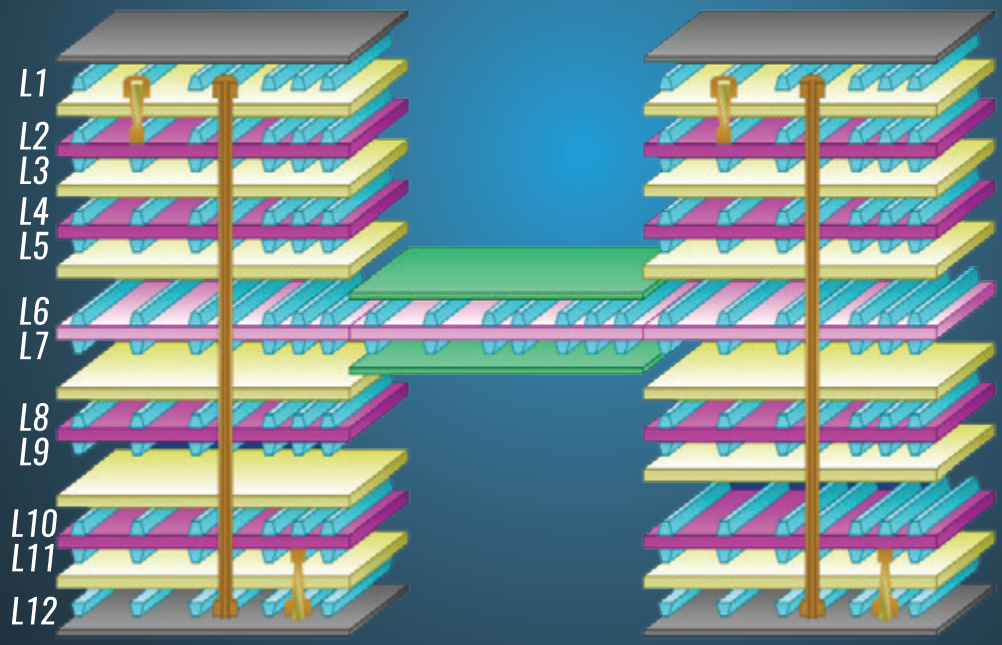

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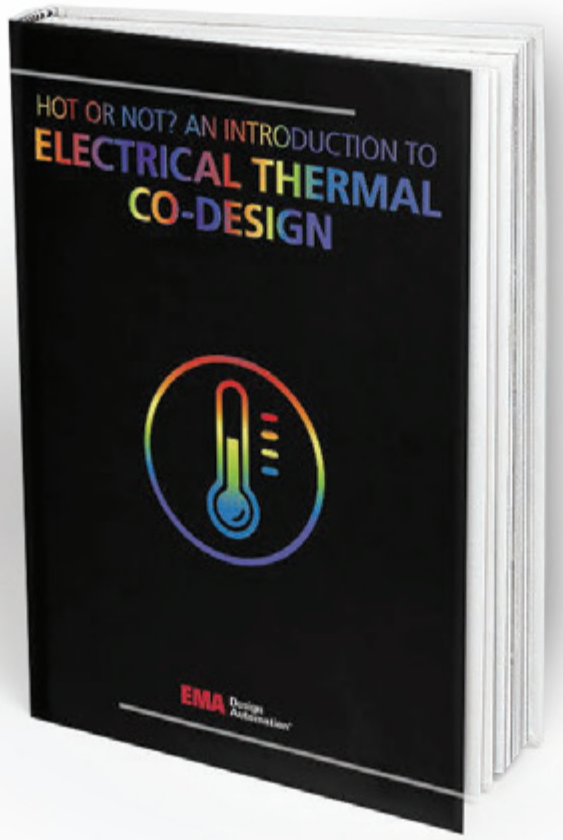

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MIKE BUETOW
EDITOR-IN-CHIEF

Resolved: A New Policy for Tech Planning is Needed

MORE THAN 160 years ago, eons before Facebook and Twitter were conceived, a pair of candidates to represent Illinois in the US Senate engaged in a series of debates. As they barnstormed their way around the state, incumbent Democrat Stephen Douglas and his Republican challenger Abraham Lincoln faced off in the heat and rain in front of thousands of citizens.

Known today as The Great Debates of 1858, the respective candidates used the time to frame their positions on the leading issues of the day.

When this issue hits inboxes and mailboxes, this year's US presidential election will (hopefully) be determined. Among the revelations of the just-ended race is that the format for the presidential debates is all wrong.

No one will mistake President Trump or his challenger, Joe Biden, for Douglas and Lincoln. Their predecessors had erudition and wide-ranging oratorical skills that seem quaint in today's era of tweets and sound bites. But the format bears revival.

That's because no matter who your preferred candidate is, the structure of the debates is inherently allergic to communicating the real issues.

The Lincoln-Douglas debates lasted three hours apiece. One candidate would speak for 60 minutes. His counterpart would speak for 90 minutes. Then the first speaker would get 30 more minutes to respond.

That's a format that's designed to weed out weak, unprepared minds. You can't fake your way through an hourlong argument. You have to explain your position and why it is the correct one.

Today's forums are more barroom insult-fests than debates. Moderator questions are dispositioned with preplanned talking points. Don't know much about a subject? No problem: bluff for 10 seconds, then use the remaining time to attack your challenger. Bonus points if you manage to hit the media with the same dart.

The prospective Leader of the Free World need not be an expert on everything, but they should show evidence of being able to synthesize reams of information and condense that into recognizable, coherent policy. Voters need evidence of in-depth understanding and strategy for areas critical to Americans. And that includes manufacturing and technology.

To be sure, most candidates running for national office pander to the twin ideals that manufacturing is essential to the American economy and technology leadership critical to world power. Once in office, however, the needle pointing to the status quo rarely budges.

As we note in this month's article on cloned semiconductors, China has made dominance in that sector a lynchpin of its national plan. Meanwhile, the respective US strategies are unclear at best.

I say enough with the lip service and pandering. Enough with the toothless resolutions and seat-of-the-pants policy-making that leave businesses around the world confused and lenders rattled. America needs a standing committee tasked with devising realistic goals and tactics for helping the nation retain its tech leadership and regain its standing as a manufacturing powerhouse. Said committee needs to be made of a truly representative sample of industry; it cannot be just Microsoft and Intel. Small manufacturers, companies that do not control supply chains but rather function at their mercy, need to be represented.

And members cannot be chosen on the basis of political donations. They must represent critical industries, and their terms on the committee should be timed to begin and end outside the election cycles. Deliverables would include revolving five and 10-year plans, markers for gauging success, and annual progress reports to Congress. Even better, they would have a budget to buy time on the national networks to broadcast their findings. If it's so important to the US, it deserves an hour or so a year of television time.

In their era, of course, Lincoln and Douglas didn't have to compete with a nonstop football schedule or the latest reality dating show. Today's video game attention spans might not acclimate to the level of detail a lengthy discourse on labor laws or public-private consortia might entail. But we can raise the bar over the trite, incomplete dissemination of information in use today.

It's time to take a page from our past. The candidates won't care for it, but if the goal is to elect representatives who will back up their campaign rhetoric, raising the barrier to entry just might be the ticket to getting the attention the industry needs after the ballots are counted.

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PCDF People

Aismalibar named **Steven Calvert** field applications engineer.

Bowman appointed **Frank Giuliani** quality assurance engineer. He has a bachelor's in electrical engineering and was previously a support engineer for Bruker and Oxford Instruments.

Fluidity Technologies named **Keven Coates** senior electrical engineer. He previously was a development engineer for seven years at Geospace Technologies and also spent 18 years at TI.

NCAB Group named **Peter Kruk** CEO, replacing **Hans Ståhl,** who retired. He was previously president of the EMEA region at Dometic Group, and president of Stoneridge Electronics.

NCAB Group Finland named **Ari-Pekka Tenko** managing director. He comes to NCAB after 10 years at Ascom, where he was country manager and head of sales.

NCAB Group USA welcomed **Donna Lagasse** as general manager/sales director of its Northeast US division. She was a business development manager at Sparton and has held sales and operation leadership roles at Sanmina, Data Electronic Devices, TTM Technologies and Raytheon.

Siemens promoted **Jay Gorajia** to director global services, Lifecycle Management and Digital Manufacturing Solutions. He has more than 20 years' experience in software sales, strategy and management with Valor, Mentor and Siemens.

Sunshine Global Circuits named **Karl Doebbert** regional sales manager for Texas and the Southeastern US.

PCDF Briefs

AT&S is developing a robust and resilient interconnect concept for a high-performance computer chip for autonomous driving.

Azul and **DuPont** have partnered to introduce "next-generation 3-D printing technologies" to the electronic materials industry.

Board Shark PCB named **Power Component Sales** manufacturers' representative in New England and upstate New York.

PCB East Returns at Customers' Request

ATLANTA, GA – In response to customer demand, PCB East returns to Boston for 2021 for the first time since 2009. The three-day technical conference takes place May 10-12, 2021, in Marlborough, MA. The event includes a one-day exhibition on May 11.

"PCB East is a much-needed opportunity for the design community to get together and check out the latest technology," said Mike Buetow, editor in chief, PCD&F/CIRCUITS ASSEMBLY and conference director, PCB East. "The show is expected to include a range of suppliers from the ECAD, PCB design service, fabrication and assembly supply chain. As Covid-19 has slowed national travel, locally-focused events like PCB East have become vital networking and selling opportunities."

UP Media Group seeks abstracts for the event, which will include presentations of two, 3.5 and seven hours. Papers and presentations must be noncommercial in nature and should focus on technology, techniques or methodology.

Abstracts of 100 to 500 words and speaker biographies should be submitted to UP Media Group at https://pcbeast.com/abstract-submission-guidelines by Dec. 11, 2020.

Anyone may submit an abstract to present a course at PCB East 2021, and presenters may present more than one paper or teach more than one course. A separate abstract must be submitted for each course.

If selected, a detailed presentation outline and final paper or presentation is due Apr. 2, 2021. Selected presenters receive access to the entire technical conference and the proceedings. (MB)

IPC Releases Medical Apps Addendum to Specification for Rigid PCBs

BANNOCKBURN, IL – IPC in October released IPC-6012EM, *Medical Applications Addendum* to *IPC-6012E, Qualification and Performance Specification for Rigid Printed Boards*.

The IPC D-33AM Task Group developing IPC-6012EM realized there are two different focuses for electronics in the medical device industry sector: the high-volume production of standard-sized PCBs for medical diagnostic equipment applications and the miniature high-density PCBs for small devices, often human body implantable.

"We understand the medical industry utilizes electronics in laser surgical devices, radiation emitting devices, x-ray machines, ultrasound devices and implantables where product failure can result in the high risk of injury to the patient," said John Perry, IPC director of printed board standards and technology. "IPC recognized the industry's desire for more stringent printed board fabrication requirements than can be provided within the current IPC Class 3 Performance class for these types of medical devices. The IPC D-33AM Task Group was created to develop an addendum to the base IPC-6012E printed board performance specification that addresses those technological needs."

IPC-6012EM is the first addendum to an IPC specification that makes use of a new design level "D," which was created to address the miniaturization level of medical devices. This new design level "D" goes beyond the typical feature sizes of what is typically considered HDI and addresses conductor width/spaces below 60µm, as well as via structures below 100µm.

Many regulatory requirements provided by both the US Food and Drug Administration and the European Union help ensure the safety and security of human beings and animals with respect to not only human and veterinary drugs and biological products, but also electronic medical devices. Examples include the EU Medical Device Directive, EU Active Implantable Medical Devices Directive and the EU Commission Regulations.

As noted by Andres Ojalill, IPC technical staff liaison to the IPC D-33AM Task Group, "IPC-6012EM has been written to streamline the production of high reliability printed boards for medical devices in accordance with regulations mentioned above so there are no gaps between technical and regulatory requirements." (CD)

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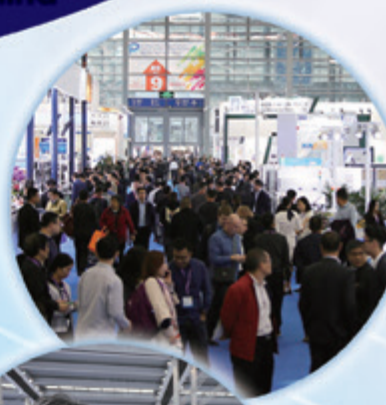

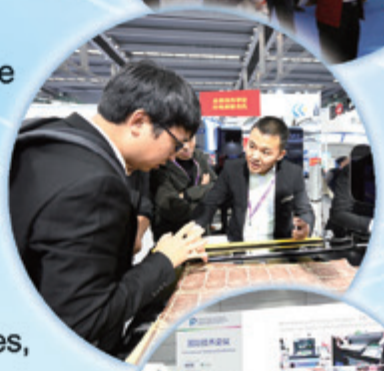

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Compal is using **Ansys** tools to automate simulation data processing to accelerate R&D cycles for its 5G laptops.

Eltos bought a **Pluritec** Inspecta Combo HP x-ray drill, Duo milling machine, and a **Dynachem** Smartlam 5200 cut sheet laminator.

Keysight and **Rohm** announced a PathWave advanced design system-compatible workspace that enables designers to perform pre-compliance testing on virtual prototypes of switched-mode power supply designs.

Mutual-Tek Industries, a Taiwanese printed circuit board supplier, will lay off about 600 workers in Taiwan and close all its production lines there due to a slowdown in orders from a major client.

NCAB Group has developed a tool that identifies some common mistakes, the implications these may have on the finished PCB and how to avoid them.

Toradex has licensed **Altium's** Geppetto modular design tool.

Trackwise Designs signed a three-year agreement worth up to £38 million to manufacture and supply flexible printed circuit boards to a UK manufacturer of electric vehicles.

VDMA and **ZVEI,** together with **Bitkom** and 20 companies from the mechanical engineering and electrical industry, have founded the "Industrial Digital Twin Association" (IDTA) as a user organization for Industry 4.0.

CA People

BTU promoted **Rob DiMatteo** to director of sales – Americas. He has more than 28 years of extensive experience in surface mount assembly, customer support and product development.

Chidinma Imediegwu, a graduate student at the Georgia Institute of Technology, has been selected as the winner of the 2020 Charles Hutchins Educational Grant.

Neways Electronics announced COO **Adrie van Bragt** will leave the company at year-end by mutual agreement.

Raytheon promoted **Ted Shpak** to senior director of quality and mission assurance.

SMTA cited **Lenora Clark** with its 2020 Member of Technical Distinction Award.

Z-zero, Mentor Collaborate on Stackup Data Exchange

REDMOND, WA – Z-Zero has teamed with Mentor to add bidirectional data exchange capabilities to its printed circuit board stackup software. The development is said to bridge the gap between designers and fabricators for the exchange of material-based stackups.

Stackup data captured in Z-Zero's software are moved from OEM to the fabrication, assembly and test phases and back again based on Siemens' ODB++Design open data structure.

The goal, Z-Zero said in a press release, is to provide the accurate PCB material parameters crucial during the design, signal-integrity simulation, and new product introduction (NPI) process.

"Z-planner Enterprise software, combined with ODB++Design, is a product-ready 'shift-left' solution that helps design teams speed time to market by tasking the stackup format to collect all proposed stackup solutions into the originating ODB++Design product model," the firms said in a joint press release. "This solution enables users to more quickly and efficiently compare alternative stackup proposals, ensuring that each fabricator proposal satisfies design requirements. The development provides a path for OEM design teams to move stackup design-level details to fabricators, and the fabricator stackup proposals back to the OEM, via a consistent format and process."

Z-Zero is a software startup founded in 2018 by Bill Hargin, who writes the "Material Matters" column for PCD&F.

ODB++Design is among the industry's most common data exchange formats, with a reported 63,000 users worldwide.

"The ODB++Design product model for PCB stackup design is the most comprehensive approach to stackup communication, generation and validation that I've seen," said Hargin. "The new stackup container available in Siemens ODB++Design, combined with Z-planner Enterprise software, provides the ability to support several stackup proposals from multiple suppliers for review, selection and comparison."

Max Clark, business unit manager of Valor NPI and Valor Parts Library (VPL) for Mentor, added that the combination of the Z-Zero tool and the Mentor platform "lends itself to future enhancements, including the potential of comprehensive digital twins of all PCB fabrication materials and processes. By merging the virtual and physical worlds, Siemens' digital twins for PCB manufacturing enable customers to design and test new products in digital form before moving forward with manufacturing, and in the process fixing problems much earlier in the development cycle." (MB)

Dixon to Open 3d Handset Assembly Plant

NOIDA, INDIA – Dixon Technologies is opening a third cellphone assembly plant in January, its 11th manufacturing facility overall.

The EMS company will invest RS 750 million (US$10.3 million) on the new plant, according to reports.

"We will be starting operations in January in our third handset factory, which will increase our total capacity from 30 million units per month to 80 million units per month in the first year," said Sunil Vachani, chairman, Dixon.

The new plant will create more than 4,000 jobs, including 900 in the first year. (CD)

Lacroix Expands in Poland, France

KWIDZYN, POLAND – Lacroix Electronics is adding 16,000 sq. m. to its factory here, according to reports. The existing plant is 14,000 sq. m. The firm says the extra space will be used for research and development and production.

The current building focuses on the automotive market, while the extension will be dedicated to industrial and home automation.

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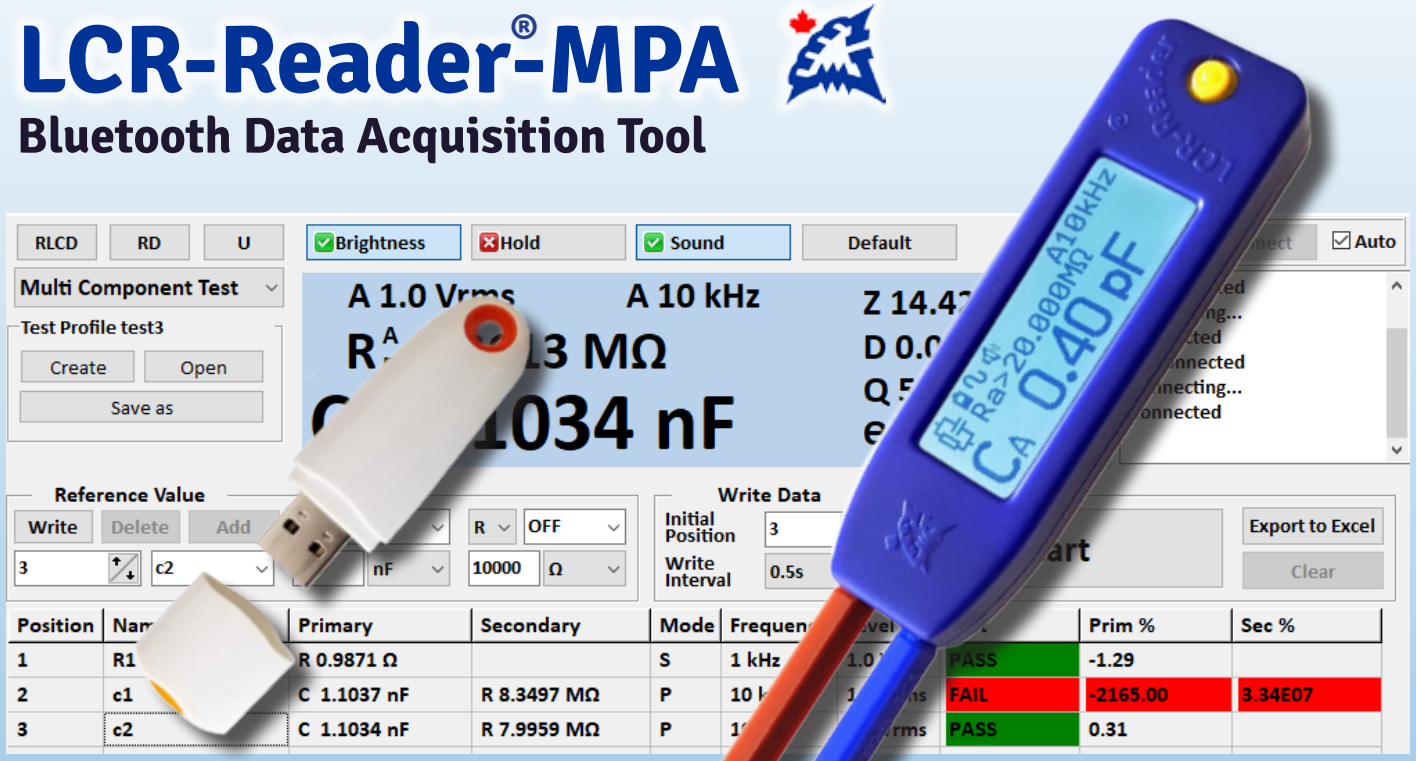

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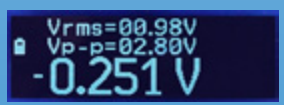

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SMTA awarded **Sabrina M. Rosa-Ortiz** the 2020 Joann Stromberg Student Leadership Scholarship.

CA Briefs

Apple, Google and others are shifting production to prepare for a "decoupled" global market in response to the US campaign to cut China from the tech supply chain.

Apple has sued Canadian electronics recycling company **Geep** after it was caught illegally selling over 100,000 Apple devices that were supposed to be recycled.

AMD reportedly is in advanced talks to acquire rival chipmaker **Xilinx.**

Checksum joined with **Integration Alliance** to distribute its in-circuit testers in Southwestern Ontario and other parts of Canada.

Circuitwise Electronics Manufacturing has won a new contract with **Siemens.**

Cisco named **Flex** recipient of the Cisco 2020 Excellence in Sustainability Award.

Continental has approved structural measures at its locations in Aachen, Karben, and Regensburg, Germany, as well as the termination of its JV with **Osram.**

ECA installed a **MIRTEC** MV-3L AOI.

Foxconn Technology says it has joined forces with a fellow Taiwanese hardware firm to delve further into electric vehicle production.

Frost & Sullivan named **Europlacer** Global Company of the Year in the SMT pick & place sector for 2020.

Huawei has built up stakes in Chinese semiconductor companies and other tech businesses, as the world's largest telecom equipment maker bolsters its supply chain in the face of pressure from the US.

HumiSeal announced successful testing of its UV40 conformal coating to ISO 10993-5 cytotoxicity standards.

The **India Cellular and Electronics Association (ICEA)** formed a capital goods committee to address technology gaps in the EMS and cellphone sectors in the country, according to reports. **Foxconn India** managing director Josh Foulger will head the committee.

Intel Federal announced a three-year agreement with **Sandia National Laboratories** to explore the value of neuromorphic computing for scaled-up computational problems.

Intel has won a second-phase contract in a project aimed at helping the US military make more advanced semiconductors within the United States.

Intensifying US-China tensions are driving Beijing to accelerate its push for semiconductor self-sufficiency. China's 14th 5-year plan running 2021-2025 will focus its IC industry development on third-generation semiconductors such as GaN and SiC.

Mycronic received an order for a complete MYPro Line solution comprising two fully automated and complete assembly lines, including intelligent component storage and software.

NXP Semiconductors has opened a factory in Arizona to manufacture chips used in 5G telecommunications equipment.

Scanfil's plant in Sieradz, Poland, the EMS provider's biggest manufacturing plant, recently received an update to its machine park with several large purchases.

SEMI and a coalition of 40 industry organizations sent a letter to European Commission President Ursula von der Leyen calling for decisive action to solve implementation issues within the European Union Waste Framework Directive, specifically the Substances of Concern in Products (SCIP) database.

Tesla is suing the Trump Administration over tariffs on a computer chip and other parts it imports from China, joining an increasingly long list of similar lawsuits filed by hundreds of companies, including automakers **Ford, Mercedes-Benz** and **Volvo.**

TDK-Lambda announced plans for a £11.5 million investment to redevelop its power supply manufacturing factory in Ilfracombe, England, with new SMT equipment.

"The extension of the Lacroix Electronics plant in Poland is wonderful news for our customers. The shift will help us optimize our production capacities and position ourselves on new business opportunities. The proximity of the two plants, with just a 500-meter distance, gives meaning to our daily industrial activity," said Andrzej Mrozik, Kwidzyn general director.

The polish site acquired two new automated SMT lines, which will be installed by the end of 2020.

In addition, the company's smart electronic factory Symbiose is under construction in France. The 19,000 sq. m. plant is expected to be completed by the end of 2021, increasing Lacroix's industrial capacity 60%.

"Symbiose is an integral part of our strategic plan. Convinced that technological performance, social innovation and respect for the environment can go hand in hand, we are pursuing this major project in this spirit," said Stéphane Klajzyngier, executive managing director of Lacroix Electronics.

CEP Technologies Expands Cleaning, Tape-and-Reel in TX

SAN ANTONIO – CEP Technologies is expanding its technical cleaning and tape-and-reel operations at its manufacturing facility here to support the EMI/RFI shielding market in the US and Mexico.

"Devices and circuit boards are becoming smaller and faster, with strict electromagnetic compatibility requirements," said CEP president Ken Kaufmann Jr. "And there is a continuing need for better interference control. If manufacturers hope to bring new devices and finished products to market, custom shielding will be a big part of that. Metal shields offer a trusted and durable solution. Given how many electronic and communications devices are packed into nearly every product made these days, shields can't merely be designed well; they need to be manufactured with care to minimize the risk of EMI and RFI on devices."

CEP produces custom shielding components that suppress and prevent internally generated signals and external ambient temperatures from interfering with equipment operations. Its two-piece covers and frames protect PCB components. (CD)

METALS INDEX

MILITARY REBOUND

Trends in the U.S. electronics equipment market (shipments only).	% CHANGE JUN.	JUL.	AUG.	YTD%
Computers and electronics products	-0.3	4.1	-0.1	2.1
Computers	0.2	-2.8	-0.4	-10.3
Storage devices	-4.9	2.9	1.1	41.9
Other peripheral equipment	-14.5	23.7	5.5	9.7
Nondefense communications equipment	-0.4	9.2	1.7	8.2
Defense communications equipment	1.1	-3.8	6.5	1.8
A/V equipment	13.9	10.7	-3.6	-11.1
Components[1]	0.0	4.5	-0.6	9.0
Nondefense search and navigation equipment	1.0	1.2	-0.7	-6.2
Defense search and navigation equipment	0.2	1.7	-3.2	2.8
Medical, measurement and control	0.2	1.2	2.0	-2.8

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, Oct. 2, 2020

US MANUFACTURING INDICES

	MAY	JUN.	JUL.	AUG.	SEP.
PMI	43.1	52.6	54.2	56.0	55.4
New orders	31.8	56.4	61.5	67.6	60.2
Production	33.2	57.3	62.1	63.3	61.0
Inventories	50.4	50.5	47.0	44.4	47.1
Customer inventories	46.2	44.6	41.6	38.1	37.9
Backlogs	38.2	45.3	51.8	54.6	55.2

Source: Institute for Supply Management, Oct. 1, 2020

KEY COMPONENTS

	APR.	MAY	JUN.	JUL.	AUG.
Semiconductor equipment billings[1]	18.7%	13.5%	14.4%	26.7%[r]	32.5%[p]
Semiconductors[2]	6.13%	4.82%	4.9%	4.23%[r]	4.94%[p]
PCBs[3] (North America)	1.19	1.10	1.12	1.00	0.94
Computers/electronic products[4]	5.44	5.44	5.44	5.28[r]	5.25[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]evised

Hot Takes

- **The number of vehicles** capable of at least Level 1 autonomy will increase from 31.4 million units in 2019 to 54.2 million units in 2024, a five-year CAGR of 11.5%. (IDC)
- **Total microprocessor sales** are forecast to grow 1.4% in 2020 to nearly $79.3 billion, following a 2.4% decline in 2019. (IC Insights)
- **Germany area PCB sales** slumped 17% in the second quarter from a year ago thanks to a Covid-19 lull. (ZVEI)
- **Sales of software for PCB and MCM design** fell 0.3% year-over-year in the second quarter to $243.5 million, only the second year-over-year dip in the past 19 quarters. (ESDA)
- **Taiwan-based notebook PCB specialists** expect a stronger-than-ever fourth quarter this year, bolstered by persistent demand for notebooks supporting a stay-at-home economy.
- **TV panel shipments** for 2020 are projected to reach 267.5 million units, a 6.2% decrease year-over-year. (TrendForce)
- **Quarterly TV shipments** reached a historical high of 62.1 million units in the third quarter on a 20% increase in demand in North America and deferred shipments due to Covid-19. (TrendForce)
- **Global robotic process automation** software revenue is projected to reach $1.89 billion in 2021, an increase of 19.5% from 2020. (Gartner)
- **Economic momentum** is slowing and future growth will likely be more difficult to come by. (IPC)
- **Vendor revenue in the worldwide server market** grew 20% year-over-year to $24 billion during the second quarter. (IDC)

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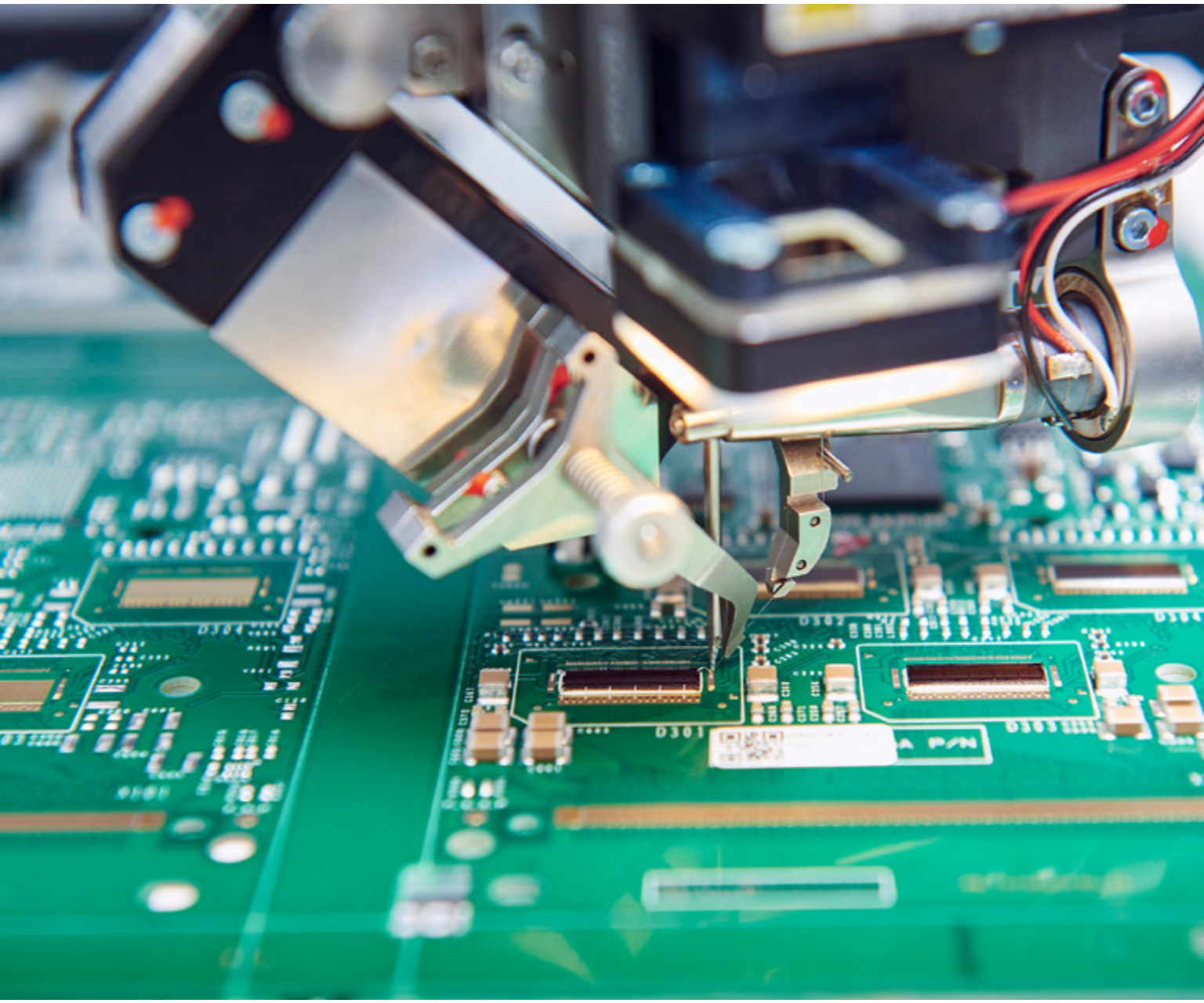

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Talent Search

The pandemic created a unique environment for finding talented employees.

LOOKING BACK ABOUT a year ago, the challenge that kept you awake at night was people. More precisely, where and how to find people to hire – people with talent, a work ethic and interest in a long-term career manufacturing electronics. 2020, of course, has brought a slew of new concerns, and made us adaptable to what is described as the "new normal." But surprise! Right up there with how many face masks, hand sanitizer and Plexiglas partitions are available in the stockroom, staffing remains the major concern for business leaders.

The focus on people certainly has taken some twists and turns through this year. During the first six months, many were focused on how to retain the workforce they had. To be sure, potential health issues, social distancing, work-from-home protocols and other necessary obstacles displaced new talent acquisition, and jolting headlines on unemployment claims, especially in the hospitality and retail sectors, forced business leaders to consider when the next shoe would drop and the order board would dry up. Thankfully – or maybe luckily – most manufacturing, and especially electronics manufacturing, has remained surprisingly "normal," and customers, employees and suppliers have recalibrated as necessary.

The underlying concerns a year ago are still with us, however. Over the next few years, an unprecedented number of experienced baby boom generation workers will retire. Those workers, for the most part, will walk out the door with a lifetime of industry experience, a work ethic that thrived on challenge and understanding how to work hand-in-hand with people on the shop floor. Talent that invented, refined and innovated – often on the fly – in entrepreneurial and structured corporate environments. The number of workers that will need to be replaced is staggering. More important, the transfer of talent and knowledge that should be taking place – right now – for a smooth transition is extreme and real.

So, as we gain experience dealing with this unusual year and begin to refocus on fundamentals such as where and how to find new talent, we may be able to take advantage of the current environment to actually improve our chances, and do so far more quickly than it might have taken just a year ago.

Managers searching for talent over the past few years often grumble that millennials lack interest in manufacturing jobs. They seem more interested in positions in the service sector. This stream of thought has also encompassed the opinion that the next generation too often lacks the commitment to really learn processes. They seek quick answers via an internet search, rather than doing a deep dive to fully understand all the issues necessary to find a good answer.

In the pandemic environment and upturned economy, however, maybe changes are taking place that could result in some previously unforeseen opportunities.

As some sectors of the economy contract and those displaced realize their jobs may never come back, an opportunity exists to hire dedicated workers looking for long-term security. Yes, people in this situation certainly will require training. But investing in training workers who have demonstrated dedication to their employer and offer the maturity to focus on long-term success, even at the expense of starting over, may be a bargain and well worth the commitment. With retail, travel and hospitality industries feeling the brunt of the unemployment numbers in this skewed economic downturn, those industries may be a great place to look when recruiting people for the years ahead.

Colleges and universities are another area that has been turned upside down. Gone, or significantly altered, are internship opportunities previously available to many students, especially in technical and science majors. For many, taking a job for the summer, or possibly a semester off, may be attractive. Savvy employers could fill short-term needs, while identifying workers for longer-range employment once they complete their degrees. Students and schools may never be more open to hands-on experience, especially at smaller companies.

Recent college graduates offer another hiring opportunity. This year has not offered a great economy to enter the workforce. Many companies have reduced or eliminated hiring. Many recent graduates have rethought what they want to do, with an emphasis to stay closer to home and consider safer careers for the long-term. This makes a career in manufacturing far more attractive for recent graduates than in past years. Equally, for businesses, especially smaller ones, the current environment is far easier in which to compete with the big players for interested and available college graduates.

Change can take place on more than one side of an equation. For almost all managers, this past year has forced unpredictable and constant change and has honed our ability to adapt. It has opened our eyes to look at the same situation in a new way. Everyone can be flexible. A hiring opportunity exists because of the pandemic economy, displaced employees seeking security, and hiring managers being a tad more flexible than in the past. It's a winning combination for hiring talented employees. ▫

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R&D: The Roots of the Manufacturing Tree

Can we build on past successes of cost and task sharing?

Much attention is focused on the importance of boosting electronics manufacturing in the US, but in a recent interview, Emmanuel Sabonnadiere, CEO of CEA-Leti, called R&D the roots of the tree of manufacturing. What a great analogy. Without successful R&D in the electronics industry, successful manufacturing is not possible. Creating the best ecosystem to foster R&D is key.

Recent analysis from IC Insights describes the semiconductor business as defined by rapid technological changes, and high levels of investment are needed in new materials, innovative manufacturing processes for increasingly complex chip designs, and new advanced packaging and assembly methods. Yet the industry has seen a slowdown in R&D spending since the 1980s (**FIGURE 1**).

The US is experiencing an especially unsettling trend. A report published by the Information Technology and Innovation Foundation ranked the US 24th out of 34 countries among the Organization for Economic Cooperation and Development, plus Brazil, Russia, India and China (BRIC). The US tax cut bill passed and signed into law in 2017 repealed a company's ability to expense R&D costs in the first year. The subsequent five-year amortization provision dropped the US ranking to 32. Federal and state support for R&D is one-third what China offers its companies.[1]

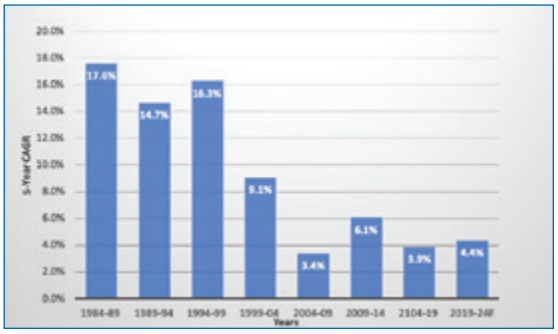

FIGURE 1. Semiconductor R&D spending will nudge up after slowing. (Source: IC Insights)

More than just money. Funding is a necessary but incomplete condition for successful R&D. In many cases, high levels of R&D spending clearly pay off. TSMC consistently spends heavily on R&D and is reaping the benefits. TSMC spent a record $3 billion on R&D in 2019, roughly 8.5% of its sales that year. This represents an increase from ~$2.65 billion in 2017 and $2.75 billion in 2018. Advanced technology nodes consistently account for half the company's revenue, and TSMC is the recognized foundry leader and is considered a leader in the development of advanced packaging.

Yet spending alone is not enough. Intel invested $12.74 billion in R&D in 2016, $13.04 billion in 2017, $13.54 billion in 2018 and $13.36 billion in 2019. The company has achieved numerous advancements, but missed timely commercialization of its 7nm semiconductor technology node this year.

Adequate R&D spending is required, but obviously more than just money is needed. Good management, excellent researchers, a well-developed research strategy, and good communication among the researchers are critical.

In the late 1980s, Professor Yasuo Tarui, manager of the cooperative lab for Japan's 1976 VLSI Research Project, explained in an interview how all these were essential to the success of the collaborative effort of the five companies: Fujitsu, Hitachi, Mitsubishi Electric, NEC and Toshiba. The Japanese government-funded project enabled development of the domestic IC industry, including the equipment infrastructure, with key suppliers including Canon, Nikon and Olympus. Success was measured in the number of patents granted and, eventually, market share.

Access to talent is one of the five factors for executives when deciding where to locate new manufacturing sites, according to a Deloitte study.[2] Around the world, many organizations lament the difficulties of attracting talent for technical jobs and research staff. IMEC's Eric Beyne points to even greater long-term challenges in motivating young students to follow a STEM orientation in middle and high schools. He also notes a low number of females in various tracks. Fortunately for the fields of bioengineering and medical studies, Beyne notes, women are a growing majority. Many young people want a more balanced professional and personal life, according to CEA Leti, but many of its young researchers are excited about contributing to society. Organizations such as SEMI are working to encourage STEM education and participation, but clearly continued efforts are needed.

Grading research organizations. Can government and organizations leverage R&D dollars, and how do we measure success? For companies, market share or revenue generation may be a good measure of success-

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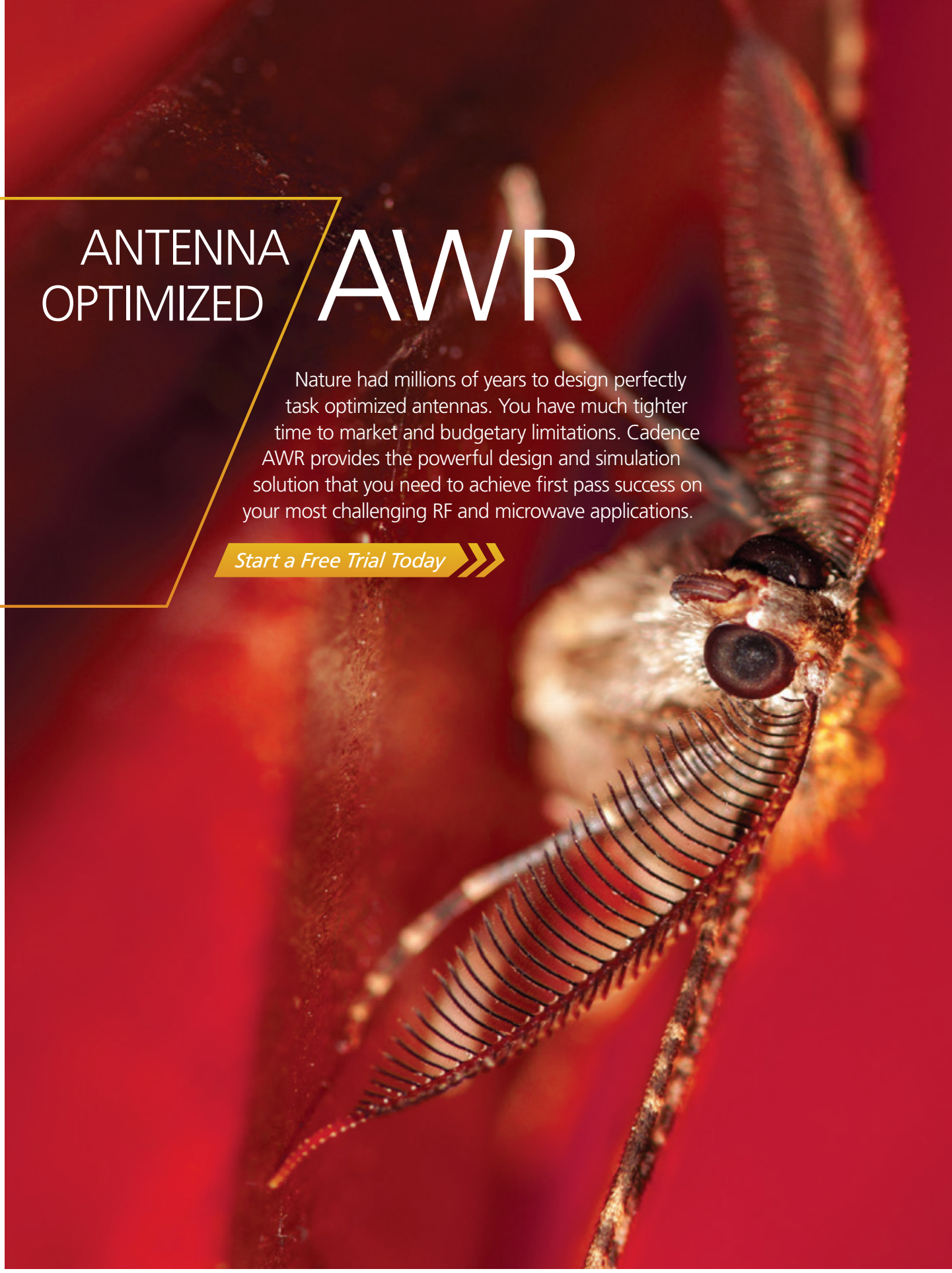

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ful R&D spending, but what about today's public funds? How is success measured? Global research institutes measure R&D success using a variety of metrics.

Asia organizations have explored collaborative research to enhance the success of their electronics industry. The Industrial Technology Research Institute (ITRI) in Taiwan receives 50% of its funding from the government and 50% from industry partnerships. It runs on a goal-oriented, proposal-based system. Some projects are defined top-down, meaning a group of government scientists determines the topic, and ITRI fills in the subtopics. At the beginning of the project, key initiatives are specified, and metrics such as spinoffs or patents are used. ITRI concurs that recruiting talented researchers can be challenging. International partnerships are sometimes included. In Singapore, the Institute of Microelectronics (IME) A*STAR has many industrial partners. IME models and samples processes on equipment located at member companies. Cooperation from companies headquartered outside of Singapore is common.

China's government is committed to building its own infrastructure in the semiconductor industry and developing alternatives to foreign technology suppliers. With the US tightening sales of components and equipment to Chinese companies, the domestic government is intensifying its efforts. In 2014 China announced a plan to accelerate its efforts in 14nm finFET memory and packaging. Then in 2015 China announced its "Made in China 2025" project targeting increased domestic semiconductor content in 10 areas: IT, robotics, aerospace, shipping, railways, electric vehicles, power equipment, materials, medicine, and machinery.[3] Yangtze Memory Technologies (YMTC) is one success story. The company has entered the 3-D NAND market with a 64-layer device and is developing a 128-layer version. Wafer-to-wafer bonding is used to fabricate the memory. Among the several national programs is one in advanced packaging. The National Center for Advanced Packaging (NCAP), located in Wuxi, has a number of projects, but it is too early to measure its success.

France's CEA-Leti is not fully funded by government monies and seeks industry partner relationships to conduct the rest of its research. Success is measured in revenue generated through licenses, economic impact with respect to startups, and job creation. CEA-Leti also looks at the annual number of patent filings and licenses. CEO Sabonnadiere indicates startups are an important measure of value creation. The contribution of startups has been borne out in many studies, including my own graduate work examining job creation by small high-tech companies.

The Fraunhofer Institutes in Germany conduct government-funded research to promote cutting-edge research and developments. More than one-third is contract research funding. A proposal-based system is used for industry partnerships with scientific institutes. The metric for success is meeting the promised deliverables.

In Belgium, IMEC's revenue comes from industrial research and local government funding. Metrics for success include the number of publications in peer-reviewed journals and leading conferences, number of patents, number of doctoral students, number of contracts and the value with local companies, and creation of spinoff companies.

Is greater collaboration needed? Many collaborative efforts in the US have shared the costs of research. These include Microelectronics and Computer Technology Corp. (MCC), the first pre-competitive research institute in the US, established in the early 1980s. This was followed by Sematech, a nonprofit consortium focused on R&D for chip manufacturing in the late 1980s. Sematech was merged into the State University of New York (SUNY) Polytechnic Institute in 2015.

The costs of advancing to the next semiconductor node and building future computer and telecommunication systems are increasingly expensive. Innovative solutions to leverage the required R&D are necessary. Cutting-edge R&D is expensive, and in July 2019 CEA-Leti, IMEC and Fraunhofer announced they would collaborate on future research. One of the first projects is the development of Edge AI. This development is important for European countries where privacy concerns limit the amount of data consumers want to have stored in the cloud. Leveraging resources across multiple organizations, while challenging, could potentially speed development by partitioning the workload.

Final thoughts. Our industry is facing challenging times with trade wars and isolationist rhetoric among countries. A strong R&D foundation and ecosystem development will enable the tree of manufacturing to flourish despite bouts of stormy weather. There are many challenges to achieving great developments in transportation, medicine, communication, and computing. A strong manufacturing based is required, but clearly the foundations of that manufacturing base need to be addressed. Past experiences offer many lessons. Crucial needs include adequate funding, a talent pool, good management with vision for the future, and an understanding of the challenge. Despite the challenges, this writer remains hopeful that well thought-out measures will allow our industry's shared goals to be achieved. □

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3. M. Lapedus, "China Speeds Up Advanced Chip Development," semiengineering.com, Jun. 22, 2020.

High Density Interconnect Printed Circuit Boards: How to HDI

Why a 3-N-3 stackup is the sweet spot.

JOHN BURKHERT JR. is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.

THE LEADING CAUSE of HDI requirements comes from the chip vendors. The original ball grid array packages supported regular vias. Little by little, the pins got cozier. The 1.27mm pitch became 1mm, then 0.8 down to 0.65mm center-to-center. This was the final node where plated through-hole (PTH) vias was an option.

The next step down is 0.5mm class BGAs. We can still use a through-via embedded in the solder pad, but there are two issues. One, the via must be filled and capped to produce a flat surface that doesn't permit solder to drain away during reflow (**FIGURE 1**). The other is that the typical "8/18" via has a finished hole size of 0.2mm and a capture pad of 0.45mm. On a 0.5mm pitch device, that leaves 50µm for a trace and an airgap on either side of the trace. That's not practical.

A microvia is the first step into the HDI pool. The primary benefit is that microvias are, er, micro! Besides their smaller size, the real benefit is that microvias span one layer pair. You can "drill" from layer 1 to layer 2 and fan out on layer 2 to a PTH via for the rest of the routing. That is the simplest implementation of HDI. (It may be obvious to most, but I'll take a moment to point out the "drilling" is performed with a laser.)

Actually, two lasers are better than one. One wavelength cuts through copper, and another does a great job cutting into dielectric material but mostly reflects off the copper. Fabricators zap through the metal with an ultraviolet neodymium-doped, yttrium-aluminum-garnet (Nd:YAG) laser, then switch to the infrared CO_2 laser to penetrate the insulation layer. Once it hits the innerlayer-2 metal, it stops pulsing without burning through the metal.

This is key. Even if stacking microvias to go from layer 1 to layer 3, use the pad on layer 2 as a target for the laser. There is a slight cost to stacking microvias. I used the penny-pinching staggered-microvia method on the Chromecast PCB. The drawback there is it eats up a little more of the traditional layer 2 ground plane. It took a few hours to implement the fabricator's request to do so. When you're selling millions and millions of widgets, pennies matter. Note that in HDI boards, the ideal location for the ground plane isn't necessarily layer 2 (**FIGURE 2**).

Besides the size difference and the single-layer span is another factor to understand before designing a PCB with microvias. Once the hole is

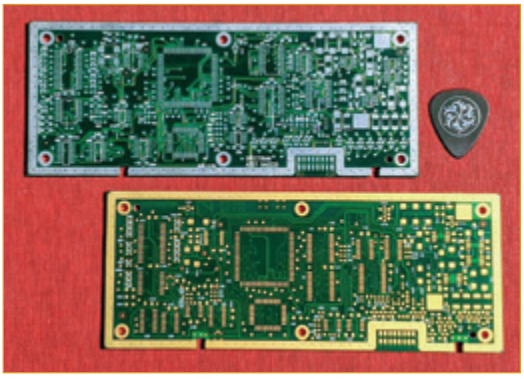


FIGURE 1. The DSP side of a mixed-signal PCB. Note that ENIG finish is preferred to HASL of the first iteration above. The via-in-pad flatness improves with gold plating.

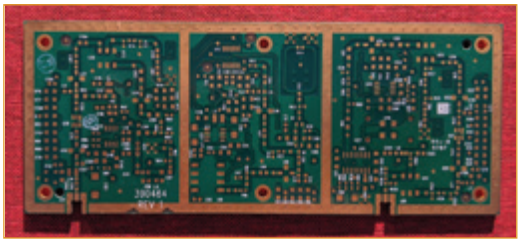


FIGURE 2. The thicker RF traces are required to accommodate test points without impedance issues. Traces can be thick only if the reference plane is a few layers deeper into the board.

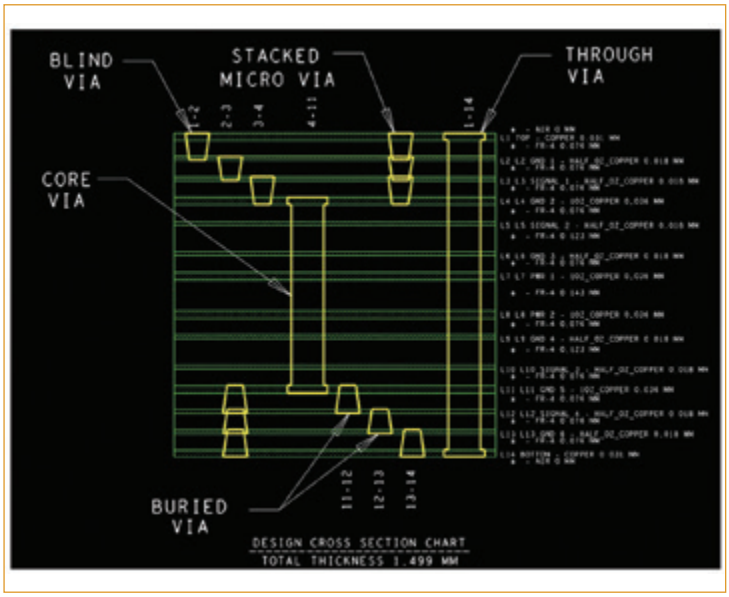


FIGURE 3. A 14-layer 3-N-3 stackup, not necessarily to scale.

ablated of material, it must be plated. It's next to impossible to plate a deep and narrow hole, so the dielectric material must be very thin to use a microvia. The ratio is somewhere between 0.6:1 and 1:1. Making the finished hole size the same as the dielectric thickness would be the leading edge and likely impossible for most fabricators. You really want the material to be thinner than the hole diameter.

The "core" of the solution: Core vias. Thin dielectrics are always in demand. Just as certain consumer products cost more these days, there may be some lead-time and price pressure on HDI-friendly materials. Balance between cost and performance comes with limited use of the microvias. I say a 3-N-3 stackup is the sweet spot. Let me unpack the 3-N-3 thing. You start with a board that is *n* layers thick. For the purposes of discussion, we'll say *n*=4. The threes indicate the number of layers added around the core.

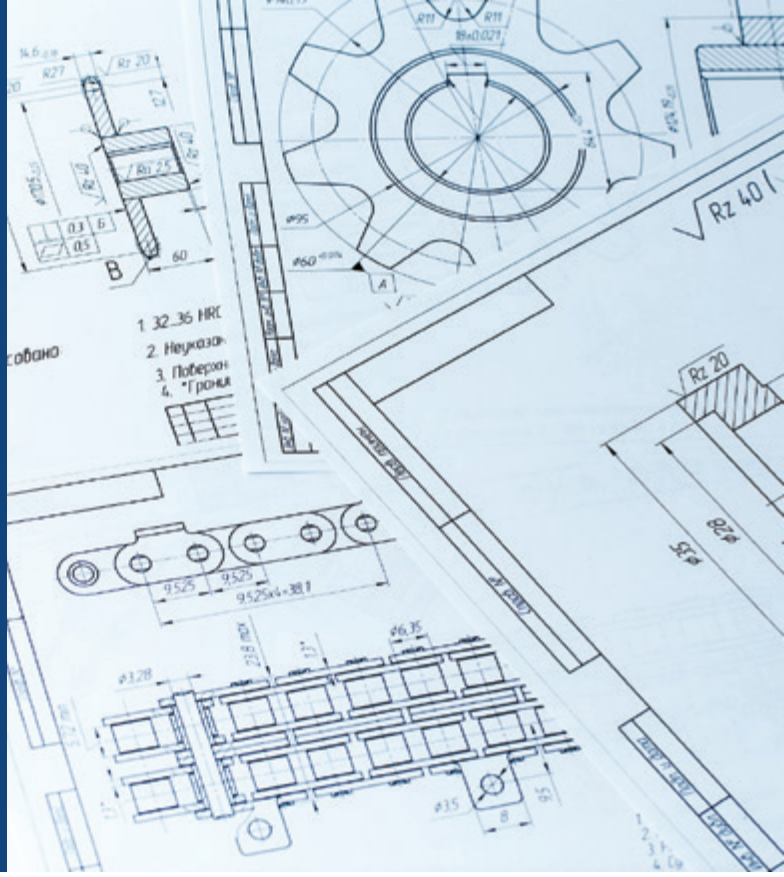
The shop will fabricate a four-layer board in the conventional way using PTH via geometry. That board will become the central core of the finished board. Then it laminates one more layer on each side of the four layers. Those layers are about 50µm thick to support the 75 to 100µm vias. That's done again and again, laminating and lasering, until you end up with three laser via layers, four mechanical via layers and three more laser via layers, for a total of 10 layers (**FIGURE 3**).

The main cost driver besides the thin prepreg layers is the lamination cycles. Starting with two, four, six or more core layers isn't as big a deal. That's why the common terminology lumps all of those core stackups as n number of layers. It's putting the board into the press again and waiting while it all gels together under the heat and pressure that drives cost. Presses are normally the most expensive pieces of equipment in the factory. They aren't as fast as drills or plating tanks. A shop with one press has a bottleneck and has to price HDI boards accordingly.

My favorite stackup. One cool hack is to fabricate the core of the HDI board with thin dielectrics on the outer layers and create microvias on the core before moving to the second lamination cycle. This is referred to as a 2-N-2 plus stackup. It requires one fewer trip to the press than a 3-N-3 version. The penalty is that the core via extends one layer more toward the top and bottom of the stackup. The layers where the core via protrudes are usually good layers for ground planes.

From a routing perspective, having vias that span 1-2, 2-3, 3-4, 4-7, 7-8, 8-9, and 9-10 can solve most vexing fan-out issues. Many boards can be done with less technology, and some may require microvias all the way through the board. By that point, the board is packed with components on both sides and probably has fine-pitch BGA devices with a thousand or more pins. When you finish one of those types of boards, the feeling of accomplishment washes over you, and your carpal tunnels like a tidal wave. Have fun with that. ❑

Do you just feel like there's got to be a better way?



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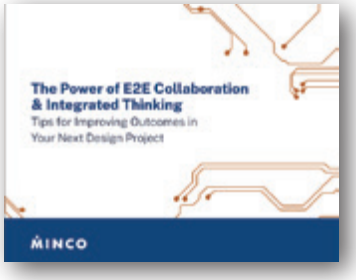

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Local Chapters: Making Sense(s) Out of Virtual Meetings

Why online get-togethers don't have to "stink."

THIS MONTH I share a few thoughts on the formation of our chapters and commentary from of a few of the PCEA staff regarding their thoughts on where the chapters are and where we need to go. Next, PCEA chairman Steph Chavez shares some encouraging words for these extended times of Covid. So our readers will not miss a beat, I include our list of professional development opportunities and events and close with a preview of what is in store for the column next month.

PCEA Updates

Like you, I need to find ways to engage in normal activities without the comfort of normal surroundings. I mean, the surroundings are normal – I've been working at home – but my activities are not normal. In fact, they are highly abnormal for a social person like me who, if tested, would surely red-line the *extroverted*, *sensing* and *feeling* indicators of the Myers-Briggs type indicators.

I often describe many of the events I attend as times in which I "eat, sleep and breath" the subject matter. And until recent times, the context of this meme has always been based on my body and its senses being less than 6' [1.8288m] from the substance I am eating, dreaming about or breathing in.

I know many of you out there are the same way. I read email from you, hear you on the phone and see and talk to you in virtual meetings. We're attending virtual conferences and tuning into online webinars more often than ever, but we don't seem as happy as when we used to get together physically. Why?

Do you realize what is missing? During a Zoom meeting "aha!" moment, it struck me that as our industry struggles to reach out and fill in the blanks of normal business routines using online means, we are only stimulating two of our five general senses. Of the five general senses – hearing, seeing, taste, touch and smell – only the senses of hearing and sight are activated during a virtual meeting.

It almost seems this character flaw in our new meeting protocol has been passed over by novice virtual meeting organizers on purpose! After all, not having to deal with three of the five senses means it is virtually impossible to present an online meeting that is in poor *taste*, doesn't *touch* the audience and downright *stinks*, right?

Presently, I suppose we are doing the best we can, and I applaud all the individuals and organizations in our industry who are creating some really outstanding content for our online meetings and training.

In the meantime, PCEA chapter leaders are looking forward to chapter meetings that will again address all the senses for more inspiring, collaborative educational experiences. Here's a taste of what they are thinking.

I have heard our Orange County chapter president, Scott McCurdy, describe past chapter meetings as a time when members can come to together, share some food and converse casually, to catch up personally and then be enlightened by a guest presenter who may have brought many samples concerning the topic of discussion to be passed around the audience during the presentation.

FIGURE 1. Chapter leaders include (top, l-r) Tim Mullen, Kelly Dack, Steph Chavez, (bottom, l-r) Olga Scheglov, and Scott McCurdy.

I recently got together with Scott and PCEA chairman and Phoenix chapter representative Steph Chavez to speak with a couple of our chapter leaders, Olga Scheglov from Toronto and Tim Mullen from Seattle, who are preparing for a time when we can get back to the traditional local chapter meeting.

Tim is looking forward to and preparing for local chapter meetings because he recalls the success the meetings had by bringing an abundance of local electronics industry sponsors and presenters in contact with their local membership. Tim mentions the chapter has access to a 68-seat amphitheater for its meetings

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and will have no lack of sponsors and presenters.

Olga is an electrical engineer living in Toronto who has many years of experience associating with local chapter members in Canada. She is excited about the PCEA chapter running again in Toronto. Olga indicates that many of her colleagues, not just PCB designers but engineers and technicians, are anticipating when meetings will start again and are excited to network and hear how the format will evolve.

Scott is looking forward to a restart of what is arguably the largest PCEA chapter. Scott says a bad day for an Orange County (So Cal) PCEA chapter meeting is when "only" 50 to 75 people attend. They are used to the synergy experienced when 100-plus attend and attribute it to the quality stream of sponsors and presenters in the area.

I asked what their wish list would be for their chapter to receive before they can again open and meet.

Scott wishes for a 4-minute video he can blast to call members new and old back to their chapter meetings.

Tim wishes for more help at the local board level to help with the details involved in coordinating rich meetings for the members.

Olga wishes for more advertising materials to help explain and promote the PCEA in Canada.

Steph wishes for this Covid challenge to subside so all the people who work for the organization he chairs can get back to full use of their senses and follow their passion to help collaborate, inspire and educate our electronics industry.

Chapter Presidents

Active:

- Orange Co., CA: Scott McCurdy
- Silicon Valley, CA: Bob McCreight
- San Diego, CA: Luke Hausherr
- Seattle, WA: Tim Mullins
- Phoenix, AZ: Randy Kumagai
- Research Triangle Park (RTP): Randy Faucette
- Nogales, Mexico: Villalba Gonzalez, Roberto Ivan
- Monterey, Mexico: Luis Saracho

Forming:

- New England, NH: Scott Miler, Ryan Primmer
- No. IL/So. WI: Anaya Vardya, David Carmody
- Columbus, OH: Nicole Pacino, Jody Waltzer
- Ontario, Canada: Tomas Chester, Olga Scheglov
- Albuquerque, NM: Brian Iorio

Message from the Chairman

I cannot believe we are now in the last several months of the year. The holiday season is just around the corner! It's hard to believe most of us are still working from home and probably will be through the end of the year. Yet, we are clearly in full swing and thriving in today's virtual world. Who would have ever thought we'd be here in this isolation and for this long? The industry is still moving forward, and there sure is a lot of activity going on. Since large group face-to-face meetings are not happening throughout the industry, virtual events continue to be the norm. We just saw PCB West come and go. Our virtual PCEA booth at this show saw its fair share of activity, as expected under these conditions. Kudos to UP Media for holding this large virtual event where they continued to offer great industry content as they always do! PCB West, SMTA, SMTAI, Siemens' Realize Live, Altium Live, CadenceLive, DesignCon, EDI Con, and many large industry events continue to adapt and are still taking place. They are just taking place virtually now. Webinars are coming along at full strength, as most of our mailboxes are flooded with these invites, one after another.

All our local, regional, and global PCEA chapters are doing their part and adapting as well. Since we are no longer able to meet face to face until who knows when, webinars, teleconferences, e-mails, and IM chats are the way things are continuing to happen. As the saying goes, "Where there is a will, there is a way." Our chapters are doing just that. Our Silicon Valley chapter recently held its first ever virtual event with great success. Several other PCEA chapters will soon follow their footsteps in the virtual world. I am excited to see how the PCEA leadership, along with each of the chapters, are meeting today's challenges to remain active and evolving in these tough times. Refer to our column and the PCEA website to stay up-to-date with up-and-coming industry events. Many webinars are offered for "free," so take advantage of them as you can. If you have not yet joined the PCEA collective, I highly encourage you to do so by visiting our website, pce-a.org, and becoming a PCEA member.

I continue to wish everyone and their families health and safety.

Warmest regards,
Steph

Next Month:

A group of dynamic women leaders in the printed circuit industry is leading the PCEA. In next month's column, find out who these leaders are and read their ideas for advancing your career by becoming involved with the PCEA.

Upcoming Events

- Apr. 13-15, 2021: DesignCon (San Jose, CA)
- May 10-12, 2021: PCB East (Marlborough, MA)
- May 11-13, 2021: IPC High-Reliability Forum 2021 (Baltimore, MD)
- Jun. 7-10, 2021: Zuken Innovation World (Scottsdale, AZ)
- Aug. 31-Sept. 3, 2021: PCB West (Santa Clara, CA)
- Nov. 10, 2021: PCB Carolina (Raleigh, NC)

Spread the word. If you have a significant electronics industry event you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Conclusion

We must not let our senses of taste, touch and smell atrophy as we engage virtually for the time being. For now, to successfully reach those with whom we wish to truly communicate, we must figure out ways to activate all their senses. Will you blandly explain to your audience that applying too much heat

to a PCB causes failures like "delamination?" Or will you perhaps go the extra mile for those in your audience who have not smelled the odor of burnt FR-4 material by sending out samples of damaged boards prior to your presentation?

If we do not get back to onsite visits, tours and meetings soon, a tactic such as this to engage the senses could make a critical difference between virtually reaching your audience – or not.

With our PCEA chapter leaders, I am hopeful our local meetings will be able to start up soon. Local sponsors, great presenters, pizza, salad and even live hugs and fist bumps are terrible things to waste.

See you next month or sooner!

How Previous Industrial Revolutions Can Help Us Approach This One

Embrace Industry 4.0 for cleaner, healthier lives.

INDUSTRIAL ELECTRONICS IS a stealthy but enormously valuable business. Approaching one-quarter of all PCBs manufactured worldwide are for industrial applications, including not only equipment for use in factories but activities such as construction and power generation. In Europe, about 40% of electronic production is destined for industrial applications.

Though cost-conscious, industrial companies appreciate the importance of investing in advanced technology to secure their market position and take advantage of new opportunities. While investing is critical for survival, early adopters can gain a significant competitive edge. This is increasingly the case as the fourth industrial revolution – Industry 4.0 – continues to transform activities.

It's good news for product innovators. Although development can be expensive and the pace fast, the value of cutting-edge industrial electronics tends to be high, and differentiating features that deliver extra value for customers can attract a premium.

As energy policies change, with renewable sources providing an increasing proportion of the total we consume, power conversion has become a huge part of the industrial electronics landscape. During my time in the industry, I've seen this sector expand from almost zero to arguably the most important aspect of industrial electronics. Aided by rapid advancements in power-semiconductor technologies – in terms of monolithic integration, device performance and packaging, and wide-bandgap technologies – power conversion has become incredibly efficient, stable and reliable.

The rewards for better-engineered products drive power designers to optimize system performance at every level from the substrate upwards. Insulated metal substrate (IMS) technology has brought valuable gains to power design, enabling smaller units to handle more power, while at the same time increasing reliability and greatly reducing or, in some cases, eliminating noisy cooling fans and ugly, bulky fins.

While LED lighting is arguably a more widely known application for IMS, the range and diversity of dielectric characteristics and base-layer properties available to designers allow fine-tuning to hit the cost and thermal-performance targets of industrial power-conversion applications. Among these, formable substrates are an exciting class of IMS. While we can immediately see their value in helping solid-state lighting solutions comply with established form factors, the recent successful commercialization of wide-bandgap GaN Mosfets is taking industrial power supplies to a whole new level of miniaturization that could see formable substrates become prominent here, too.

Under the heading of Industry 4.0, the influx of cyber-physical systems and smart devices into industrial enterprises represents perhaps the greatest development opportunity of our time. While there is hope and vision, there is also fear of smart automation, and robotization of roles currently performed by people. There are worries about employment and the effects on society. We will certainly be challenged to rethink our ideas about what it is to be human. But let's take a look at the effects of earlier industrial revolutions.

Automation has certainly swept away traditional jobs, which is a perennial fear among observers. On the other hand, the effects on cost and quality of manufactured goods have created new products that improve quality of life and made them affordable. While we may be wary of stoking rampant consumerism, we should value the effects of the technologies that allow us to experience cleaner, healthier homes, safe and affordable transport, and improved workplace safety.

The effects of industrialization on prosperity and human life expectancy are a matter of record. We can look back over the past 200 years or so since industrialization began and see the average annual GDP per capita in the US and China is about 20 times greater today. In the same period, the average human life expectancy has more than doubled. There are regional differences, of course, and we must continue to pursue distributing these improvements more evenly.

Similarly, we believe over 80% of the world's population now has access to electricity. That still leaves some 1.4 billion people without the advantages electricity can bring: particularly, a stable source of lighting that can assist study and education that does not require burning unhealthy, potentially unsafe kerosene lamps or candles in the home. Consider no homes had access to electricity in the 1800s. We are not finished yet.

Another improvement I can draw attention to is currently some 80% of the world's one-year-olds receive at least one immunization against serious and potentially fatal diseases such as measles and polio. Polio immunization is a subject I'm particularly close to as a member of the Rotary Organization, a founding partner of the Global Polio Eradication Initiative.

continued on pg. 23

ALUN MORGAN
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You Don't Always Need S-PARAMETERS

Consider these alternatives for advanced PCB design and analysis. by ZACHARIAH PETERSON

These days, I try to keep up with interesting signal integrity discussions on forums, SI listservs, and LinkedIn. After reading a recent question about PDN models and parasitic extraction on SI-lists, I made the comment (paraphrased) that "S-parameters are overgeneralized." Someone might rightly ask for clarification, and PCD&F seems the right forum to address this.

The point of the comment is this: S-parameters are not always the most conceptually satisfying mathematical tool – nor the only tool – for analyzing in every situation. Other designers might disagree with this and that's fine; if you can garner important design insights from S-parameters, rather than some other parameter set, then so be it. My goal isn't to knock S-parameters, but alternatives have more useful mathematical properties, or a more satisfying conceptual meaning, in certain situations.

Once you start modeling ultra-high-speed signals in causal channels (e.g., 100G and faster channels under 802.3 standards), be careful which parameters you choose to describe the impulse response, as well as how these are manipulated in the frequency domain. This is where the physical interpretation of various network analysis parameters is critical, especially given the extensive mathematical work on causal modeling found in the research literature. This is a topic near and dear to my heart, and it just happens to be the subject of one of my upcoming IEEE papers. My hope is the budding SI engineer will know of some other important mathematical tools for network analysis, especially as the digital world creeps further into the mmWave regime.

Some Alternatives to S-Parameters

I won't get deep into the mathematical definition of S-parameters here as the description is available in many textbooks and online resources. Introductory readers are encouraged to read *Microwave Engineering* by David M. Pozar[1] for an introduction to network analysis.

Before going into alternative parameter sets, why is there such a focus on using S-parameters? It helps to look at the history of microwave circuits to better understand why these parameters get so much attention and to understand the context under which they were developed.

The person responsible for developing the mathematical framework that would eventually be called "S-parameters" depends on which resource you look through online. The earliest mention I've seen is in the context of microwave circuit design, in a 1920 article by Campbell and Foster.[2] Most SI engineers were probably taught the definition formalized by Kurokawa in his seminal 1965 article.[3]

These parameters are so often used because they define two important quantities in microwave circuit design: Reflected and total power loss as a traveling electromagnetic wave interacts with a load component. As it turns out, when these two quantities are broadband functions of frequency, they also happen to be quite important in understanding digital circuits on long interconnects. They are also often used, as they can be easily determined directly from measurements (e.g., time-domain reflectometry). Therefore, it is understandable designers use these parameters in analytical modeling and circuit design.

Unfortunately, you'll be hard-pressed to find two resources that provide the same definitions of S-parameters, simply because different references rarely refer to the same system in their definitions. It's not that everybody has it wrong, but each resource presents its definition as the only definition without stating in which system the definition applies, creating plenty of confusion. Different definitions sometimes get used in systems where they don't apply because the context for different definitions is absent.

There are different parameter sets for describing N-port networks; these may be more conceptually relevant in different situations and they can be converted back to S-parameters if needed. Pozar[1] includes some useful formulas for converting between S-parameters and other parameter sets, but these formulas are not universal, and I do not recommend following the conversions in his textbook without deeper investigation. Perhaps the best resource I've found is Caspers[4] (see page 87), which provides S-parameter definitions for a variety of 2-port networks, which can then be generalized to N-port networks.

To show where S-parameters are not so mathematically useful for analytical modeling, let's look at two alternative parameter sets and how they fit into some common modeling tasks.

Network Analysis and Transmission Lines: Use ABCD Parameters

There are three reasons you might want to use ABCD parameters for analytical modeling of general networks or transmission line models:

1. Simple intermediate parameter set. When working on analytical models for transmission lines, I prefer ABCD parameters. I'm not the only person who feels this way; there are many studies in which ABCD parameters are used to determine transmission line and network model parameters from measured impulse responses. (See Zhang, *et al*[5] for an excellent example.) In fact, because you can convert between ABCD parameters and S-parameters (Caspers[4]), it makes sense to work with ABCD parameters as an intermediate parameter set during analysis, especially when fitting measured responses (S-parameters) back to model descriptions (ABCD parameters) for a network or transmission line.

2. Cascading is easy. When I first read about ABCD parameters, I thought the definition was backward. Why would the input current/voltage need to be regressed back from the output? This definition aids cascading. Due to the order in which matrix multiplication is defined, we can simply multiply successive ABCD matrices for cascaded network elements to get an ABCD parameter matrix for the entire network. For my work in analytical descriptions of transmission line behavior, this is extremely useful, particularly when we have shunt circuit elements, stubs, branches, or other structures on an interconnect.

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_i \begin{bmatrix} V_{i+1} \\ I_{i+1} \end{bmatrix}$$

By induction

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \prod_{i=1}^{N-1} \left(\begin{bmatrix} A & B \\ C & D \end{bmatrix}_i \right) \begin{bmatrix} V_N \\ I_N \end{bmatrix}$$

EQ. 1. ABCD parameter matrix for a cascaded network.

Eq. 1 was derived by induction, and you can prove by induction that all the mathematical properties governing an individual ABCD matrix also apply to the ABCD matrix for a cascaded network. Sometimes it helps to look at this process visually. This multiplication process for a cascaded network is shown in **FIGURE 1**. Note a similar definition does not exist for S-parameters in cascaded networks.

3. Direct calculation of transfer functions and impulse response. In my opinion, this is the major strength of ABCD parameters: It's easy to calculate the system's voltage-to-voltage transfer function directly from ABCD parameters. In fact, you can derive the transfer function in terms of the source and load termination impedances for a network with known ABCD matrix, including cascaded ABCD matrices:

$$H(\omega) = \frac{Z_L}{AZ_L + B + CZ_SZ_L + DZ_S}$$

EQ. 2. Transfer function calculation from ABCD parameters.

Once you have the transfer function, you can calculate a causal impulse response for the network. See Kurokawa[3] for the procedure used to enforce causality in a transfer function. Note that this procedure is defined in the case where the material properties (i.e., substrate dispersion and copper roughness) also have causal representations.

PDN Design: Use Z-Parameters

Although the term power integrity suggests you should focus on "power" as invoked in S-parameters, PDN design focuses on target impedance, and for good reason. When a digital IC draws current during switching, ripple on the PDN is proportional to impedance. The current pulse drawn by the IC is broadband, and in this way, the PDN impedance measured between different ports is a transfer function that converts the transient current into a transient voltage.

This is embodied in the Z-parameter matrix, which is arguably the best way to describe the impedance in an n-port PDN. The mathematical definition is shown in Eq. 3.

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1n} \\ Z_{21} & Z_{22} & \cdots & Z_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{n1} & Z_{n2} & \cdots & Z_{nn} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \end{bmatrix}$$

EQ. 3. Z-parameter matrix for an n-port PDN.

In Eq. 3, the diagonal elements ($i = j$) are self-impedance values, and the off-diagonal elements ($i \neq j$) are called transfer impedance values, which describe coupling between two ports in the network. For a PDN, this describes how the ripple seen at port i is related to the current drawn into port i and all other ports $j \neq i$.

The challenge here is in developing causal Z-parameters with sufficient resolution to capture PDN resonances while ensuring causality. For a brief primer on this topic, look at Huddar[6]. Provided your Z-parameters are causal, you can determine ripple in the time-domain by converting the Z-parameters into impulse response functions and calculating the convolution, just as is the case with a transfer function.

Summary

Two examples where an alternative parameter set is useful in analytical SI and PI modeling are presented. These parameter sets have conceptual advantages (Z-parameters) and mathematical advantages (ABCD parameters) that aid construction of analytical models for a PDN and transmission lines on a PCB. In both cases, causality is a critical factor to be verified when working with high-speed signals on interconnects. This issue of enforcing causality is not confined to ABCD parameters or Z-parameters; the same issue affects modeling of impulse response functions for S-parameters, and it remains an active research topic to this day. Despite these problems in enforcing causality, the two S-parameter alternatives I've discussed here have repeatedly shown their worth in advanced PCB design and analysis, both mathematically and conceptually. □

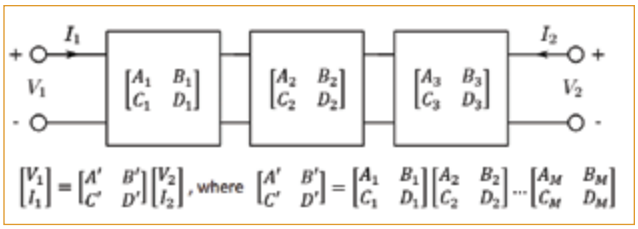

FIGURE 1. Cascaded ABCD network definition. The equation shows a cascaded matrix with M 2-port networks.

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Material Gains, continued from pg. 20

The WHO declared type 2 and type 3 poliovirus eradicated and just last month reported transmission of wild poliovirus has officially been stopped in all 47 countries of its African region. Efforts must, however, continue worldwide to combat the type 1 virus and prevent any resurgence.

As we consider the effects of Industry 4.0 on employment, living conditions, and even our understanding of what it is to be human, I want to mention one more statistic. The late Hans Rosling's book *Factfulness* tells us the number of playable guitars per million people has risen from about 200 in 1962 to 11,000 in 2014, and the trend is accelerating.

As an indicator of human well-being, Rosling's metric has drawn both admiration and criticism. It might suggest more of us have time to pursue our inclinations toward creativity and expression. If industrial robots take over jobs we may not have liked but felt we needed, what does our growing affinity for the guitar say about us? Do we want to be artists or workers? Human nature being what it is, some of us are attracted to the technical challenges in learning and playing, while others prefer to experiment and compose as they go. Most probably do both, but to differing degrees. The fourth industrial revolution will give us the choice to an extent never possible before. □

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It's About Time: Let's Automate HIGH-SPEED CONSTRAINTS

IC vendors should make edge rates easily available for inclusion in PCB design libraries. by CHARLES PFEIL

PCB layout will eventually be fully automated. Although the effectiveness of automated place-and-route algorithms has declined over the years as designs became more complex, all the ECAD companies have been successfully automating other areas of the design process.

Now the age of artificial intelligence (AI) for ECAD has arrived. Jitx, DeepPCB, Luminovo and Celus already have design-related products using AI. Zuken, Mentor, Altium and Cadence have ongoing development projects applying AI methods. Many obstacles must be overcome. Yet an aspect of PCB layout is ripe for automation today, even without AI.

There is an opportunity for high-speed constraints to be automated. My book *High-Speed Constraint Values*[1] provides all the equations and methods ECAD companies can use to accomplish this goal, without AI. A significant obstacle is preventing automation of high-speed constraints, however.

Two concerns. The title of this piece, "It's About Time," is a double-entendre. The first interpretation of that phrase refers to the essential variable that determines if a net will have high-speed problems. The second interpretation refers to the fact that it is about time the IC and PCB industries focus on making that essential variable easily available.

Essential variable. The first step to determine if a net will have signal integrity and/or EMI problems is to calculate the critical length. If the interconnect exceeds the critical length, those problems must be managed, or the circuit will most likely fail. The edge rate is the essential variable needed to determine the critical length.

$$\text{Critical Length [in]} = \frac{\text{EdgeRate x LightSpeed}}{\sqrt{\text{DielectricConstant}}} = \frac{Tr \times C}{\sqrt{\varepsilon_r}} = \frac{Tr \times 11.8\ [\text{in/ns}]}{\sqrt{\varepsilon_r}}$$

The edge rate is the fastest time for a signal to transition from low to high (rise time) or from high to low (fall time). Usually, the rise time (Tr) is faster than the fall time (Tf) and that is why Tr is commonly used to represent the edge rate.

Technically, the edge rate is more akin to the slew rate rather than the rise and fall times. Over many years, however, the PCB design industry has adopted edge rate as the term to express the faster of the rise and fall times.

The time used in all the equations applied to manage high-speed design, as provided in IBIS and Spice models, is the 20% to 80% range for the rise or fall time of the voltage output signal (**FIGURE 1**).

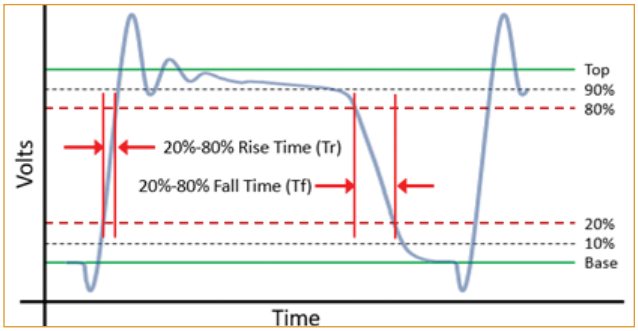

FIGURE 1. 20% to 80% edge rates.

Once it has been established a net exceeds its critical length based on its edge rate, then constraints need to be created to manage the PCB layout to mitigate or eliminate the negative effects. The following constraints require the edge rate in an equation to determine the effective value for the constraints:

- Group length matching
- Differential pair skew
- Differential pair phase matching
- Same layer crosstalk
- Adjacent layer crosstalk
- Same net coupling
- Max stub length vias
- Max stub length traces.

Also, as a result of a net becoming a transmission line because it exceeds its critical length, these concerns need to be

managed using constraints or layout methods:

- Signal return path
- Differential pair stitch vias
- Impedance management vias
- Impedance management traces
- Via anti-pad size
- Differential pair via-via spacing.

Early access to edge rates. All our industry experts say the edge rate is the essential variable for high-speed constraints, and they also agree it is not easy to get that data. It's about time the IC industry makes the edge rate easily available so the PCB layout industry can incorporate it into their component libraries.

Yes, the IBIS models provide the edge rates in the [Ramp] section. However, getting those models in a timely manner is the problem. For newer components, the models are not released except under NDA and for those with established relationships, which layout designers rarely have. Some data in the IBIS models are considered intellectual property (IP), and it is appropriate to protect that data. However, should the edge rates be considered IP? I suggest not.

If IC manufacturers release the max rise and fall time data as soon as their components become available, they can be used to create high-speed constraints and properly guide layout methods.

Proposed ramp file format. This format should be relatively easy to extract from any IBIS model to create a new file. The idea is to restrict the data to the minimum needed. Note that I have also included the R_load from the [Ramp] section to enable designers to know the target impedance for the interconnect. An example is below. Do you think this is IP?

```
File Name = <IBIS_name>.ramp
[Pin] signal_name model_name
10 LVTTL_F ttl2f1
11 LVTTL_S ttl2s1
|
|
[Model] ttl2f1
| variable max
dV/dt_r     0.6908/1.4129e-10
dV/dt_f     0.8030/2.7626e-10
R_load = 50.0000
|
[Model] ttl2s1
| variable max
dV/dt_r 0.6908/7.9422e-10
dV/dt_f 0.8030/1.2896e-09
R_load = 50.0000
```

I am asking readers to consider what can be done to facilitate making edge rates easily available. Please send ideas or comments to me at pcbconstraints@gmail.com and I will follow up. ❑

CHARLES PFEIL has spent over 50 years in the PCB industry as a designer, owner of a service bureau, and in engineering management and product definition roles at Racal-Redac, ASI, Cadence, PADS, VeriBest, Mentor Graphics, and Altium. He was the original product architect of Expedition PCB, and an inventor of Team PCB, XtremePCB, XtremeAR, and the Sketch Router. He previously authored *BGA Breakouts and Routing.*

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Attack of the CLONES

A trillion-dollar industry remains exposed to knockoff parts that are sometimes electrically superior to the real thing.

by MIKE BUETOW

Thousands of words have been written on the preponderance of fake parts. Scores of solutions have been presented, from x-raying suspect devices to using boundary scan software to applying DNA taggants to authentic components at OCM factories, not to mention that old destructive standby cross-sectioning.

Organizations such as SAE have written standards governing inspection and test procedures, workmanship criteria, and even training and certification requirements on the art of counterfeit device detection.[1] The US government has codified use of detention and prevention measures in its annual defense budget.

And yet …

Why are counterfeits still so prevalent in the electronics supply chain?

According to Tom Sharpe, vice president and founder of component distributor SMT Corp., and a leading expert on cloned devices and the methods used to make them, the problem has morphed from bucket shops in Shenzhen markets to a massive conspiracy with the implicit support of at least one national government, namely China.

China has long since determined the path to economic dominance lies in controlling the semiconductor industry. The nation codified this in its *Made in China 2025* blueprint, which calls for 70% of its demand for chips to be domestically sourced in five years. It has a long way to go. Per IC Insights, China imports at least $100 billion worth of devices, more than its own factories can make (**FIGURE 1**).[2] The outsized denominator of imported chips, Sharpe asserts, motivates China to take liberties with foreign IP in pursuit of market leadership.

Writing in the *Journal of International Commerce* and Economics last year, John VerWey noted China's relationship with the US makes the former "… both its most important customer and, if China's industrial plans are successfully realized, its next rival."[3] Yet China's semiconductor foundries are years behind the leading edge as established by Samsung, TMSC and perhaps Intel. And the costs to close the gap are rising. Per a report by McKinsey & Co., "designing a 5nm chip costs about $540 million for everything from validation to IP qualification,"[4] a sum about three times the cost to develop a 10nm chip and 1.5 times the amount for a 7nm chip. "We expect that R&D costs will continue to escalate, especially for leading-edge products," the authors wrote, adding that foundry startup and tooling costs are more than $5 billion for 5nm production. (By contrast, SMIC, China's leading domestic chipmaker, is reportedly capable of only 14nm chip builds.)

Thus, experts believe, when tasked with developing semiconductor dominance but lacking the talent or funding to close the gap using conventional means, China is taking a big shortcut.

Indeed, Sharpe is among those who say the problem of cloned devices has become state supported, if not state sponsored. Sure enough, more than a decade ago, executives at NEC were stunned to learn of a parallel company manufacturing copies of the electronics maker's products in China and Taiwan.[5] The vast conspiracy involved more than 50 factories.

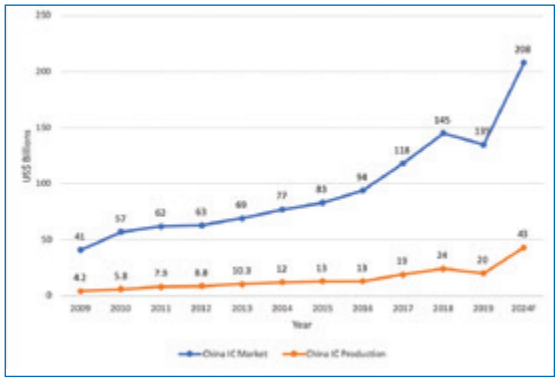

FIGURE 1. China IC consumption vs. domestic production trends. (Source: IC Insights)

In a phone interview with PCD&F/CIRCUITS ASSEMBLY in September, Sharpe said cloning continues to go on in broad daylight, and the knockoffs are in some cases built to even tighter tolerances than the authentic parts.

"Cloning is in the open, and the parts generally look and smell right," he said. "It's coming from factories whose

purpose is to make knockoffs. And they are getting better. These knockoffs have different electrical characteristics that test closer to the manufacturer's spec than the part from the manufacturer itself. If the manufacturer's spec says, say, +/-5, the manufacturers are +/-4, and the clones will be 0 or +/-1."

The approaches taken to spot the fakes are myriad. The simplest way is visual inspection, using either manual or machine methods. At this point, all but the worst fakes can beat optical inspection. RFID tags and optical strips looked promising a decade ago, but cloners quickly learned how to duplicate them, often almost immediately after the originals came to market. Applied DNA Sciences developed a gene-based taggant in which unique molecular-based markers are attached to authentic chips.[6] Our discussions suggest

'They Are Coming from Factories Whose Purpose is to Make Knockoffs'

Even in 2020, counterfeits remain an industry-wide issue. Cloned devices expert Tom Sharpe discussed his take on the problem and how it will be rectified with PCD&F/CIRCUITS ASSEMBLY editor in chief Mike Buetow in September.

MB: We have heard of counterfeit electronic components for at least 20 to 25 years. In 2006, *The New York Times* reported on a scam involving nearly 20 factories in China to basically recreate NEC.[5] And, no doubt, many companies have tried to put in procedures to limit such parts from their supply streams. Yet, most experts feel the volume of fake parts has increased, and the counterfeiters are better than ever. Is that correct?

TS: The problem continues to grow and is much more dangerous today in my opinion. Fifteen to 20 years ago it was the resident Chinese harvesting OCM chips from e-scrap as their component feedstocks. Over the past 10 years China has shifted very significant financial, technological and human resources to becoming a standalone semiconductor superpower.

We have seen a decline in the number of "traditional" counterfeits (OCM refurbished product made to look new), although there is still plenty of these older counterfeits out there. What we are seeing now is a big spike in "cloned" devices. Over this same period SMT has identified well over 100 functional clones representing many different OCM device families. These devices are newly manufactured and carefully designed to both look and function similar to OCM parts. We surmise the Chinese government put a damper on the traditional chip counterfeiters because they were hitting China in the pocketbook by competing for many of the same customers.

MB: We've heard of fake parts being made on legitimate lines at legitimate companies – the so-called fourth shift – but there would have to be records of material use and line utilization hours and employees coming and going. Semi foundries are a multibillion dollar expense, so the wafer equipment companies would know where their lines are being sold. So, who is making them?

TS: Cloning is largely in the open within the Chinese electronics industry, and the parts generally look and smell right, but unfortunately, besides obvious reliability concerns we don't know what is in them. It's not the fourth shift. It's coming from factories whose purpose is to make knockoffs, and they are getting better.

These knockoffs have different electrical characteristics that test closer to the manufacturer's spec than the part from the manufacturer itself. If the manufacturer's spec says, say, +/-5, the manufacturers are +/-4 or 3, and the clones will be 0 or +/-1.

MB: The US government has written anticounterfeiting measures into its budget legislation. The 2012 National Defense Authorization Act requires the Department of Defense and other government agencies "detect and avoid counterfeit parts in the military supply chain." What impact has this had?

TS: The flow down of NDAA 2012 had a very positive impact when it reached the open market suppliers and forced them to compete by increasing quality processes significantly. Ironically it was around this same time of heightened counterfeit awareness and increased inspection process that SMT first noticed the presence of cloned electronic device counterfeits in the marketplace. Finding clones is a process within the process. The process to find traditional counterfeits pre-2012 loosely focused on detecting refurbished/altered OCM parts. The standards were not written around finding factory-fresh and functional cloned devices. The vast array test processes within the AS6171 standard is the best currently available for clone identification purposes.

Battelle Labs has developed the Barricade System which can instantly create an "electronic fingerprint" of a device and classify it as authentic or counterfeit.

MB: When you say fingerprint, what do you mean?

TS: In the case of the Barricade System, it's creating a 3-D graph and plotting that device from hundreds of electrical data points generated by Barricade's proprietary software algorithms. Electrically the clones may function very similar, the same or even closer to the OCM test spec, but on a 3-D graph plot clones cluster in a different universe from their OCM authentic counterpart.

MB: There's a host of testing protocols and equipment out there for spotting fakes: high-voltage testing of dielectric withstand voltage, cross-sections, JTAG software readings, EDS, DNA marking, x-ray, and so on. Where is the detection technology headed?

TS: The good news is these various test systems all employ slightly or vastly different detection technologies – and most importantly they are competing. I seriously doubt there will ever be a single "silver bullet" authentication test system for all device types so it is extremely important many different entities are attacking the problem from different directions. I believe one or more of these systems will be at the forefront of counterfeit chip detection and tampering detection in the very near future.

Battelle contacted SMT in 2014 to say they had an electronic chip authentication system under development and they wanted to run both authentic and corresponding counterfeit/clone devices from SMT through their beta system to determine if they were on the right track. After two years in development, they were looking to see if their system would be even 70% accurate in identifying one chip type from the next. At the completion of a day of testing their system was 90% accurate in identifying traditional refurbished counterfeits and 100% accurate in identifying clones. These results got my attention in comparison to at least a dozen or more anti-counterfeit systems I had personally reviewed prior to Barricade.

The high-rel entities that have the biggest need for a fast chip identification technology most certainly include DoD and the Defense & Aerospace industry as a whole (in essence our warfighters and national security). But there are also several other "high-rel" industries which would also greatly benefit, such as medical, energy, telecom and automotive, to name just a few. If history is a good indication of the future, we can certainly count on the counterfeiter to continue getting better and therefore the threat level higher.

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OCMs are reluctant to add steps to their processing lines, however. Destructive tests such as microsectioning are slow and expensive, better for lab analysis than at incoming inspection. Fakers are beating scanning electron microscopy and energy dispersive spectroscopy (SEM-EDX) methods through use of identical surface elements and authentic die. Chung *et al* propose a series of test methods specifically for MLCC compliance verification, ranging from capacitance temperature examination, high-voltage testing of dielectric withstand voltage and insulation resistance, among others.[7]

Sharpe is bullish on a system from Battelle, the research institution. Battelle's Barricade system measures the power sensor in the device under test (DUT), looking for unintended emissions, and measures the current as transistors are turned on and off. It then creates a 3-D graph that shows the DUT against a database of "enrolled" parts – known authentic devices that have been received directly from the OCM or an authorized distributor.

Check out a demo of the **Battelle Barricade System** in the digital edition.

According to Tom Bergman, program manager in the Cyber Security Unit at Battelle, "Barricade uses test stimulus consisting of a series of test vectors to the DUT, which can be impulses or a clock and combinational logic input, to provide an input to that device to cause the device do something, like switch a transistor.

"We're looking for characteristics that are inherent in the fabrication of that device. It's really a combination of the resistors, the packaging, the wirebond … that whole system has noise characteristics that we record and compare to device data of devices we previously tested."

To account for naturally occurring variations in legitimate devices, Battelle acquires parts from two or more different lots, makes its measurements and waveforms, and tunes the analysis to show that device's unique characteristics. The Battelle system is being used by SMT Corp., the US Air Force Research Laboratory and Navy (Crane), and licensees are sought for broader distribution of the equipment and database.

A few years ago, Sharpe and Bergman conducted a test on cloned voltage regulators.[8] They started with authentic versions from authorized distributors. According to Bergman, "Battelle developed configurations to be able to see the difference in lot codes. Then we gave (Sharpe) a sequence of tests to run against that part. SMT Corp. did datasheet testing with those parts and found they could not detect some of the clones with their benchtop testing unless they exercised those parts over an extreme temperature range. That's a pretty complicated test. They had to build a test fixture, temperature cycle them all, and record all the data and analyze them. They then ran those same parts through Barricade, and all those cloned devices appeared as outliers.

"If you have a part enrolled in your database and want to know if the DUT is a counterfeit or clone, Barricade is probably 99% accurate that the part does not belong," Bergman told PCD&F/CIRCUITS ASSEMBLY. Nevertheless, he concedes that if the part has a slightly different lot code, it makes for a more difficult test and authentication. "Say it's a microcontroller: there might be differences in how many timers are in the part, so those parts would be different internal configurations and may be easier to distinguish."

With so many choices and few means to conduct internal benchmarks, where does the industry turn? The answer may come from academia. The University of Maryland Center for Advanced Life Cycle Engineering (CALCE) is helping coordinate a controlled study of electronic test technologies in conjunction with various labs and companies. That study is expected to wrap up in November.

All the above begs the question, if the cloned devices are so good, why bother sniffing them out? Money. US companies exported just under $50 billion worth of semiconductors in 2019, according to the SIA. The segment is one of the five largest US exports overall, and that doesn't account for the many billions more parts US companies make overseas for offshore customers. Every dollar spent on clones is money taken directly from the OCM's pockets, money that could go to funding the next generation of chips and continued American technology leadership.

There's nothing fake about that. ▫

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Advanced Packages and New 5G Technologies Will Drive PORTABLE PRODUCTS

SLPs with lines and spaces <35µm are ahead. by URMI RAY

Ed.: This is the ninth of an occasional series by the authors of the *2019 iNEMI Roadmap.* This information is excerpted from the roadmap, available from iNEMI (inemi.org/2019-roadmap-overview).

The iNEMI Roadmap defines portable and wireless devices as "high-volume consumer products for which cost is the primary driver, including handheld battery-powered products driven by size and weight reduction."

A significant portion of this sector continues to be dedicated to the relatively mature but still evolving and growing smartphone/phablet/tablet. Although the market segment is mature, the content and functionality of premium tier smartphones are increasing exponentially with the adoption of artificial intelligence (AI) and machine learning (ML). A major emerging growth area in this sector is personal activity monitors, or wearable electronics, which are becoming widely adopted, especially among the more urban and suburban areas of the US and other advanced nations.

The primary trends in the smartphone category can be summarized as follows:

- Adoption of 5G mmWave standards and disruptive changes in design, materials, assembly processes and test protocols.
- More functionality in smaller, tighter form factors.
- 3-D sensing, virtual reality (VR) and augmented reality (AR) sophistication.
- New display technology such as foldable displays.
- Advanced node semiconductors for mobile processors.
- Convergence of printed circuit board (PCB) and substrate technologies (substrate-like PCBs) – finer line, space, smaller via sizes.
- Memory technology evolution (bandwidth and density).
- Advanced packaging (heterogeneous integration and system-in-package), 2.5D and embedded die.
- New electromagnetic and radio frequency (RF) shielding techniques.
- Challenges to overcome thermal challenges for power hungry functionalities.
- Efficient battery technologies.
- Supply chain consolidation and changing landscape.
- New inspection and metrology innovation.

The major constraint in the portable and wireless sector is cost. Consumers continue pushing for increased functionality, smaller form factor, and thinner and lighter portable devices, but at lower costs. Added capabilities such as face recognition, high-resolution displays and multiple cameras are requiring more storage, larger and more powerful batteries, and more complex ICs.

In response, OEMs serving this sector are looking to utilize embedded passive and active components, system-in-package (SiP), system-on-chip (SoC), or any other means to densely pack ICs with increased functionality. There is also a push for single-chip transceivers and multi-RF transceivers to reduce space and power consumed by transceivers. In addition, use of substrate-like PCBs (SLPs), defined loosely as lines and spaces <35µm, is expected to be a major trend, especially for portable and wearable devices.

The key attributes of portable/mobile market sector semiconductors, especially for smartphones, are fab nodes driven by low-leakage and low-power requirements.

Emergence of multiband RF front-end modules (RFFEMs) is another major trend. These modules contain many different ICs, including power amplifiers (PAs), transceivers, antenna tuners, switches, and use of diverse semiconductor technologies, such as GaAs, CMOS, silicon-on-insulator (SoI), etc.

Within the portable product sector are fundamentally different product types. Wireless-based products such as mobile phones tend to have a greater percentage of discrete components (or modules) to fine-tune frequency matching and filtering functions. Processor-based products such as gaming devices use a greater proportion of ICs and fewer discrete components to achieve functionality. This is reflected in the lead count per component. Design of processor-based products usually presents more challenges in the design of the interconnect substrate because of routing between high I/O devices. The difference between these product types is narrowing, however, due to convergence and electronic component integration. Although handheld products are becoming dominated by those with wireless connectivity, their circuit design has increasingly become more digital in nature due to converging applications into the device and the increasing digitization and continuous

integration of many previously analog design approaches.

New Wireless Standard: 5G

The most disruptive changes in the portable and wireless sector are expected to be driven by the transition from 4G LTE-based communication to 5G mmWave-based protocols, which will drive many new innovations and partnerships in the value chain.

The ballooning consumption of data everywhere in the world has created an extreme need for bandwidth. Smartphones generate close to 90% of total mobile data traffic, a figure that is projected to reach 95% at the end of 2024. As monthly usage per smartphone increases, total mobile data traffic is predicted to rise at a compound annual growth rate (CAGR) of 31% over the forecast period, reaching 136 exabytes (EB) per month by the end of 2024.

The 3rd Generation Partnership Project (3GPP) standards group (3gpp.org) for several years has been making technology and cost tradeoffs to find the optimal solution for spectral allocation, thus opening the relatively "uncrowded" space above 6GHz. The result is the introduction of standards in phases so deployment can also be planned in a phased manner.

Wireless Integration and 5G

Advancement of mobile cellular standards is driving adoption of most mobile/portable devices. In fewer than 30 years, standards have moved from 2G to 5G (**FIGURE 1**). Given the momentum in the market, forecasts for 5G subscriptions have been increased to 1.9 billion subscriptions for enhanced mobile broadband by the end of 2024, accounting for over 20% of all mobile subscriptions at that time (**FIGURE 2**). The peak of LTE subscriptions is projected for 2022, at around 5.3 billion subscriptions, with the number declining slowly thereafter. LTE will remain the dominant mobile access technology by subscription for the foreseeable future, however, with nearly 5 billion subscriptions projected by the end of 2024.

Technology Challenges

Significant challenges exist in 5G mmWave implementation, especially in commercial mobile packages. These can be summarized as follows:

- Materials (substrates, metal and dielectric losses, packaging).
- Passive devices (filters, tuners, radiators).
- Active devices (silicon versus III-V compound semiconductor).
- Integration/packaging techniques
  - Antenna-in-package
  - Antenna-on-chip.
- Wideband signal processing.
- Challenges to achieve required bandwidth, primary-ambient extraction, linearity, latency.
- Analog versus digital versus digital beamforming.
- Massive multiple-input multiple-output (MIMO).
- mm-Wave testing challenges
  - More integration means less known good die – yield concerns
  - Over-the-air (OTA) testing and calibration.

Materials. Next-generation 5G communications solutions require ultra-low-loss laminate materials and PCBs/substrates for efficient design and manufacturing. These materials pose challenges, however. For example, there is no consistent methodology for measuring transmission loss or Df/Dk, especially for higher frequencies (e.g., 30-100GHz). Many different approaches are used, requiring different fixtures and test methods, sample preparation, and/or data analysis/extraction. iNEMI's 5G/mmWave Materials Assessment and Characterization project is addressing this issue by developing guidelines/best practices for a standardized measurement and test methodology that can be shared with industry and relevant standards organizations (https://community.inemi.org/content.asp?contentid=639).

Test requirements. The major test challenges are related to the portable/mobile platform, especially RF tests and the challenges related to 5G in the mmWave ranges. Significant changes are expected in automatic test equipment (ATE) platforms, including the possibility of OTA testing, cooling for transceiver testing and emergence of more system-level testing. ▫

URMI RAY is a project manager for iNEMI, focusing on 5G initiatives. This article was excerpted from the Portable & Wireless Product Emulator Group (PEG) chapter of the *2019 iNEMI Roadmap.*

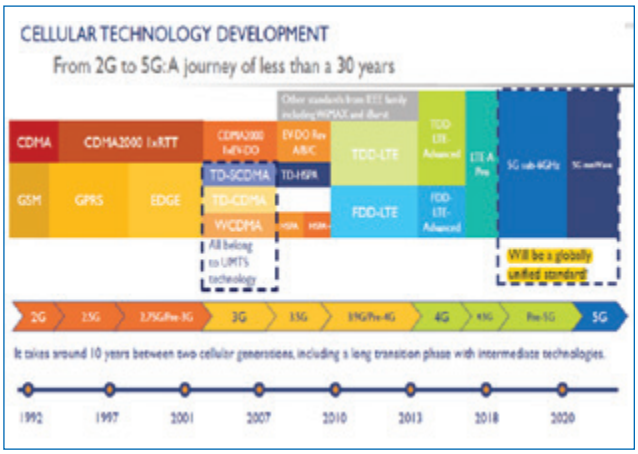

FIGURE 1. Cellular technology development timeline. (Source: Yole)

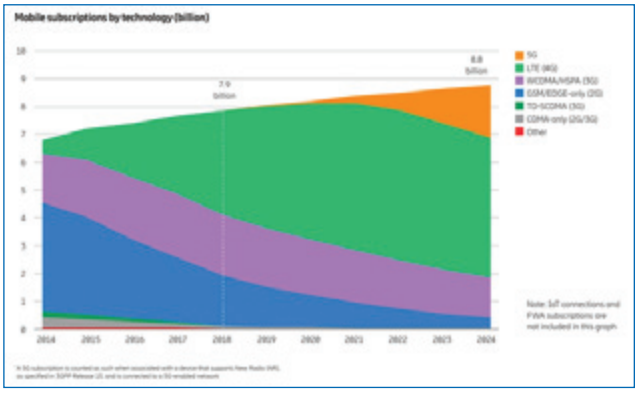

FIGURE 2. Mobile subscription forecast by technology. (Source: Ericsson Mobility Report 2019)

Solder Mask and LOW-STANDOFF COMPONENT CLEANING – A Connection?

Assessing the impact of six solder mask options on under-component cleanliness. by JIGAR PATEL and UMUT TOSUN

Why consider solder mask selection as a factor that can affect cleaning process effectiveness? The solder mask impacts the component standoff height. Of the three options – solder-mask defined (SMD), non-solder-mask defined (NSMD), or no solder mask (NoSM) – NoSM can increase the standoff height, which may enhance the cleaning process. Standoff height will vary depending on board design and component selection, so it is difficult to quantify standoff height for each solder mask selection and specific component. Reference **TABLE 1** for average standoff heights for specific component groups.[1]

By using NoSM, the component standoff height can be increased 10 to 40µm, depending on the component type, thereby increasing the potential of the cleaning agent to more effectively penetrate beneath low-standoff components.

Each solder mask type has its pros and cons for use. The purpose of this study is not to address the benefit of the various solder mask designs, but rather the impact, if any, each design has on cleaning process effectiveness.

The authors developed a design of experiments (DoE) to assess the impact of the three solder mask designs on defluxing effectiveness. For this study, standard substrates and inline cleaners were used. The substrates were populated with numerous low-standoff chip capacitors and soldered with no-clean tin-lead and lead-free solder pastes. Two aqueous-based cleaning agents were selected, and multiple wash temperatures and wash exposure times were evaluated.

Cleanliness assessment was conducted by visual inspection per IPC-TM-650. For each substrate, all components were mechanically sheared, enabling thorough under-component inspection. The under-component surface was rated as either clean or not clean. The effectiveness of the cleaning process was calculated by dividing the number of clean components by the total number of components on each substrate and detailed as a percentage. Cleanliness results were analyzed using main effects plots and factor analysis of mixed data (FAMD).

Percentage cleanliness (%) = No clean components / total number of components

In addition to visual inspection, the authors planned to conduct ion chromatography (IC) analysis on selected test vehicles for each solder mask option and solder paste. To verify the test methodology, IC test was conducted on uncleaned boards (NSMD) for each type of solder paste to verify if this method can be used for data analysis. However, because all tests yielded passing results for all the uncleaned boards, this method was deemed not useful for further data analysis and therefore abandoned.

It is important to note that this study was conducted as a comparative analysis to understand the impact of solder mask on test vehicle cleanliness assessment at specific wash temperature and conveyor speed. All other cleaning process parameters were maintained constant, and no attempt was made to optimize the cleaning process.

TABLE 1. Standoff Height (in microns)

Component Type	SMD and NSMD	NoSM	Additional Clearance with NoSM
Chip Caps	30 - 70	60 - 90	~30
BTCs	20 - 40	40 - 80	20 - 40
BGAs	80 - 120	90 - 130	10

TABLE 2. Process Conditions

Process Variables	Conditions
Solder Mask Option	SMD, NSMD & NoSM
Wash Temp (delta of 10°C)	144°F, 162°F, 180°F
Conveyor Speed	0.5 fpm (10.4 min), 1 fpm (5.2 min), 1.5 fpm (3.5 min)

Methodology

The purpose of this study is to assess the impact of solder mask selection on cleaning process efficacy with a given solder paste and selected process parameters. The goal was not to optimize the cleaning process, but rather to quantify the impact of the solder mask type for the given set of variables selected.

The study was limited to three variables: solder mask option, wash solution temperature, and conveyor speed. Three process conditions were identified for each variable (**TABLE 2**). Four solder pastes (**TABLE 3**) and two cleaning agents were selected (**TABLE 4**).

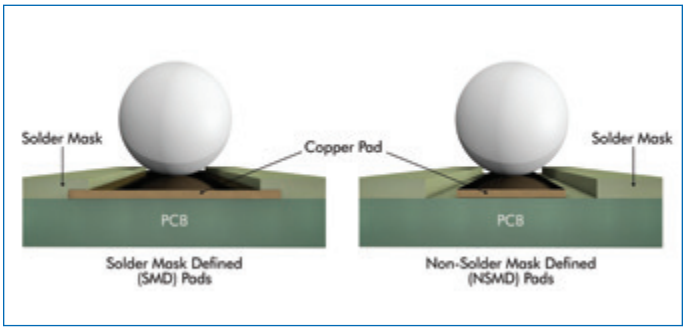

FIGURE 1. SMD and SDMD pads.

A standard test vehicle was selected and populated with 104 commonly used low-standoff capacitors (**FIGURE 3** and **TABLE 5**). In total, 18 trials were conducted, nine for each cleaning agent type (**TABLE 6**).

For each trial, four test vehicles were prepared, one for each paste type and solder mask option. In total, 216 test vehi-

TABLE 3. Solder Paste Selection

Solder Paste	Type
Solder paste A	No-clean SnPb
Solder paste B	No-clean SnPb
Solder paste C	No-clean Pb-free
Solder paste D	No-clean Pb-free

TABLE 4. Cleaning Agent Selection

Cleaning Agent	Type
Cleaning agent A	Surfactant-free alkaline uninhibited
Cleaning agent B	Surfactant-free pH-neutral inhibited

cles were required. Each was reflowed, cleaned and inspected for cleanliness on both surfaces, as well as underneath the component.

Standard tin-lead and lead-free reflow profiles were used (**FIGURES 4** and **5**). The selected equipment was a spray-in-air inline cleaner manufactured with high-temperature-resistant polymer material. Process operating parameters are detailed in **TABLE 7**. Other than conveyor speed and wash solution temperature, all parameters were held constant for all trials.

Results

All boards were inspected for surface cleanliness after being cleaned. Other than the MLF/BTC components, surfaces around all other components were found to be fully cleaned for all trials (**FIGURES 6** and **7**). **FIGURES 8** and **9** are representative of fully cleaned and partially cleaned surfaces of the MLF-68 component.

TABLE 8 shows representative pictures of rea under-components after cleaning at specific setting (Cleaning agent A @162°F wash temp, 1 fpm conveyor speed – Paste C).

Following surface inspection, all boards were visually inspected for under-component cleanliness in accordance with current IPC standards. To do so, all components were mechanically sheared from all boards, and the surface underneath the component was rated as either "fully cleaned" or "not cleaned." For each test vehicle, the ratio of cleaned components to total components was calculated and plotted.

The impact of solder mask, conveyor speed and wash temperature on under-component cleanliness results for all solder pastes are detailed in **FIGURES 10**, **11** and **12**, respectively.

For all test variables, regardless of solder paste and cleaning agent used, test vehicles with NoSM yielded best overall cleanliness results: 97.07% versus 78.4% (Figure 10). Cleaning results improved significantly at lower conveyor speed (0.5 fpm) compared to faster conveyor speed (1.5 fpm): 92.97% versus 77.52% (Figure 11). Cleaning results improved significantly at

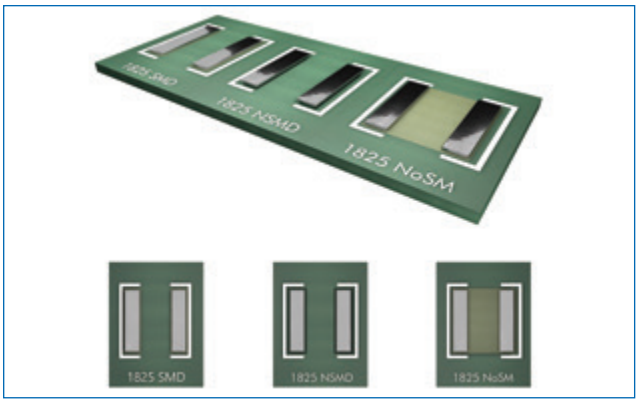

FIGURE 2. SMD, NSDM and NoSM pads.

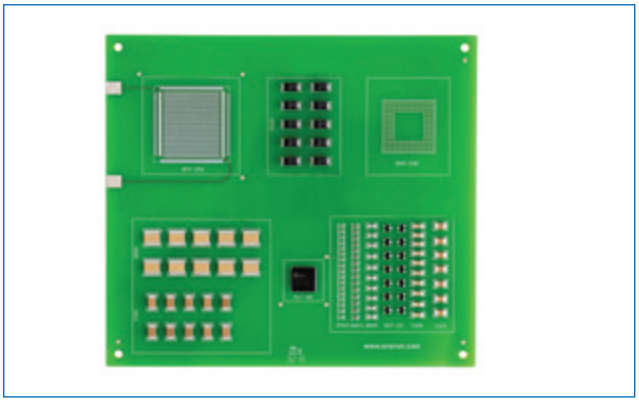

FIGURE 3. Test vehicle.

TABLE 5. Component Types

Component Type	No. of Components
6032	10
1825	10
1812	10
MLF-68	1
402	17
603	15
805	10
SOT-23	14
1206	10
1210	7
Total:	**104**

TABLE 6. Test Condition

Trial No.	Cleaning Agent	Wash Temp (°F)	Conveyor Speed (fpm)	Solder Mask Option
1	A	144	0.5	SMD, NSMD, NoSM
2	A	144	1	SMD, NSMD, NoSM
3	A	144	1.5	SMD, NSMD, NoSM
4	A	162	0.5	SMD, NSMD, NoSM
5	A	162	1	SMD, NSMD, NoSM
6	A	162	1.5	SMD, NSMD, NoSM
7	A	180	0.5	SMD, NSMD, NoSM
8	A	180	1	SMD, NSMD, NoSM
9	A	180	1.5	SMD, NSMD, NoSM
10	B	144	0.5	SMD, NSMD, NoSM
11	B	144	1	SMD, NSMD, NoSM
12	B	144	1.5	SMD, NSMD, NoSM
13	B	162	0.5	SMD, NSMD, NoSM
14	B	162	1	SMD, NSMD, NoSM
15	B	162	1.5	SMD, NSMD, NoSM
16	B	180	0.5	SMD, NSMD, NoSM
17	B	180	1	SMD, NSMD, NoSM
18	B	180	1.5	SMD, NSMD, NoSM

higher wash temperature (180°F) compared to lower wash temperature (144°F): 92.04% versus 75.67% (Figure 12).

FIGURES 13-15 were developed examining the relationship between each solder mask option and conveyor speed and wash temperature. If the NoSM option is used instead of SMD and NSMD, conveyor speed can be increased three times (i.e., to 1.5 fpm from 0.5 fpm), while keeping same wash temperature (Figure 13). If the NoSM option is used instead of SMD and NSMD, wash temperature can be lowered to 144°F from 180°F, while keeping same conveyor speed (Figure 14). The same under-component cleanliness results can be achieved with a combination of high wash temperature (180°F) and faster conveyor speed (1.2 fpm) compared to low wash temperature (144°F) and slower conveyor speed (0.4 fpm) (Figure 15).

The main effects graph (**FIGURE 16**) examines the relationship between all variables considered for under-component

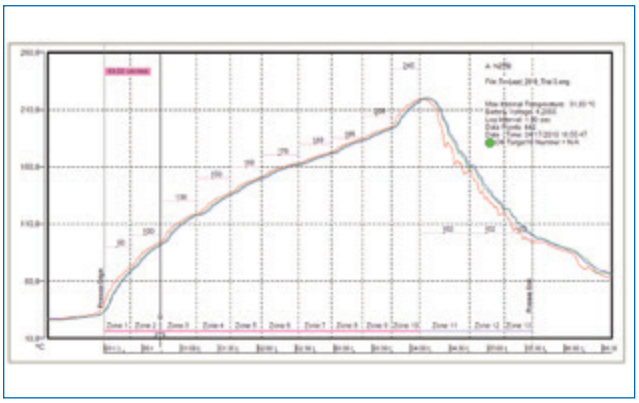

FIGURE 4. Standard tin-lead reflow profile.

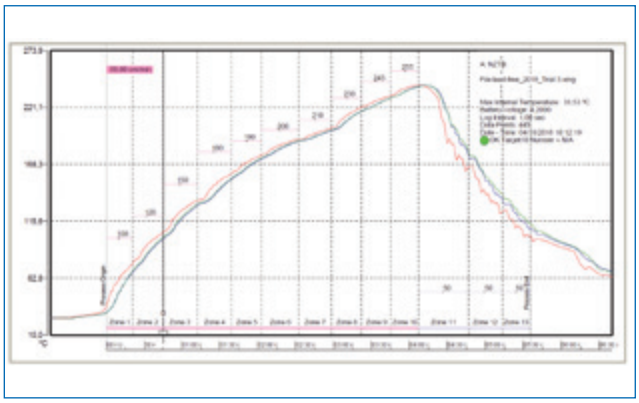

FIGURE 5. Standard lead-free reflow profile.

cleanliness level achieved. This plot examines the differences between level means for one or more factors. A horizontal line indicates no main effect. A non-horizontal line indicates a main effect. The greater the slope, the greater the magnitude of the effect.

With regard to under-component cleanliness, the main effects plot indicates:

- Minor effect due to cleaning agent selection: 83% vs. 85% for Cleaning Agents A and B, respectively.
- No effect using SMD and NSMD (78%), major effect using NoSM (97%).
- Major effect due to wash temperature: 75% at 144°F vs. 93% at 180°F.
- Major effect due to conveyor speed (wash time): 77% at 1.5 fpm vs. 94% at 0.5 fpm.
- Major effect using Pastes A and C versus Pastes B and D.

The interaction among all variables was also analyzed using factor analysis of mixed data (FAMD). This tool is useful when analyzing a data set containing both quantitative and qualitative variables. It makes it possible to analyze the similarity between individuals by considering mixed types of variables. Additionally, one can explore the association between all variables, both quantitative and qualitative.[2]

For this analysis, solder pastes, cleaning agents and solder mask options were treated as qualitative variables, while conveyor speed and wash temperature were treated as quantitative variables.

The quantitative plot (**FIGURE 17**) shows the relationship between conveyor speed and wash temperature on the cleanliness level achieved of each component type. The angle formed between any pair of arrows corresponds to the level of association. Angles between 0° and 90° correspond to positive association, and angles greater than 90° and up to 180° correspond to negative associations. Closeness to 0° indicates high level of positive association; closeness to 90° indicates no association; and closeness to 180° indicates high level of negative association. The axes (Dim1 and Dim2) have no physical meaning and are merely an analytical means of summarizing all the data and variables. The length of each arrow corresponds to the significance of the variable.

Observations from the FAMD quantitative analysis:

- The conveyor speed is in the opposite direction of 1210, 1812, 1825, and MLF-68 components, indicating that

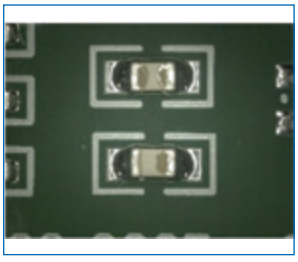

FIGURE 6. Component 0805 – before cleaning.

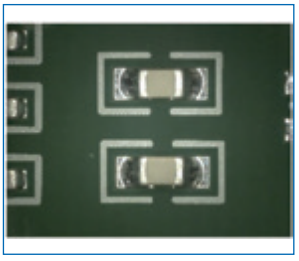

FIGURE 7. Component 0805 – after cleaning.

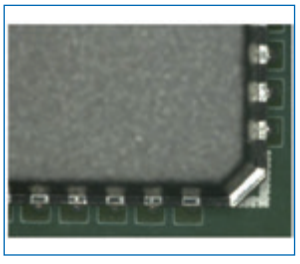

FIGURE 8. MLF-68 fully cleaned surface.

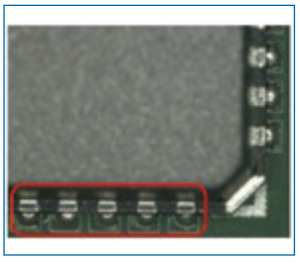

FIGURE 9. MLF-68 partially cleaned surface.

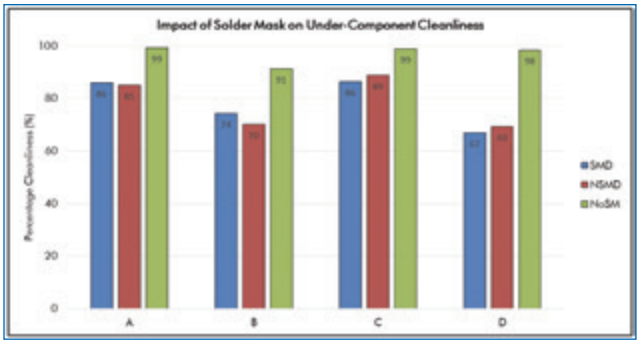

FIGURE 10. Under-component cleanliness: impact of solder mask option.

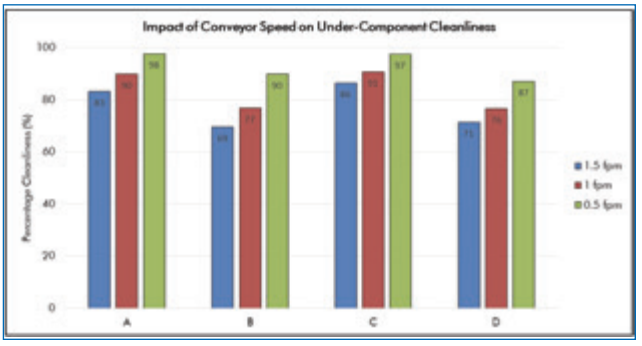

FIGURE 11. Under-component cleanliness: impact of conveyor speed.

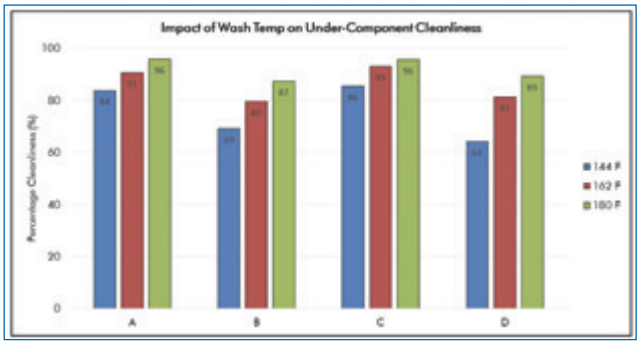

FIGURE 12. Under-component cleanliness: impact of wash temperature.

increasing the conveyor speed is associated with lower cleanliness for these component types.

- Conveyor speed forms an approximate 90° angle with 0402, 0603, 1206, 0805, and SOT-23 components, indicating conveyor speed has less impact on cleanliness for these component types.
- Wash temperature can be seen making a 30°-45° with most of the component types, indicating a soft positive association.

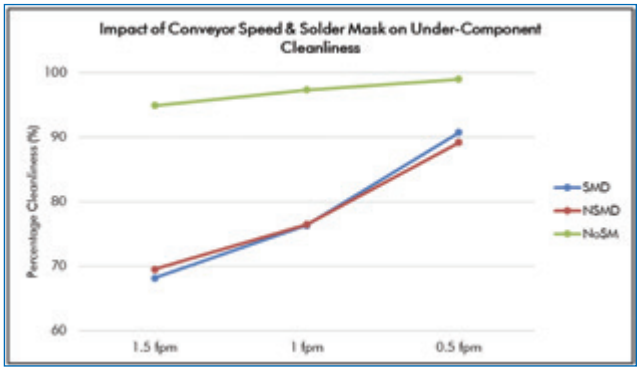

FIGURE 13. Under-component cleanliness: impact of conveyor speed and solder mask.

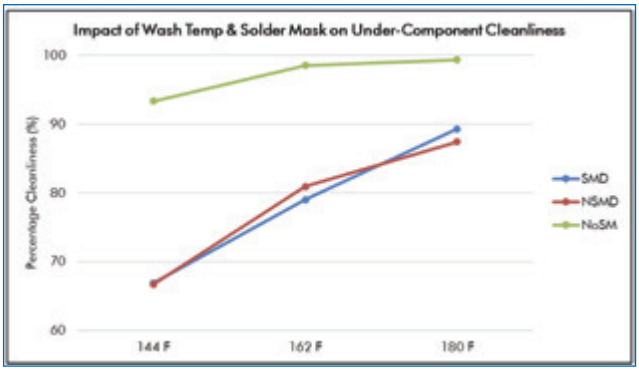

FIGURE 14. Under-component cleanliness: impact of wash temperature and solder mask.

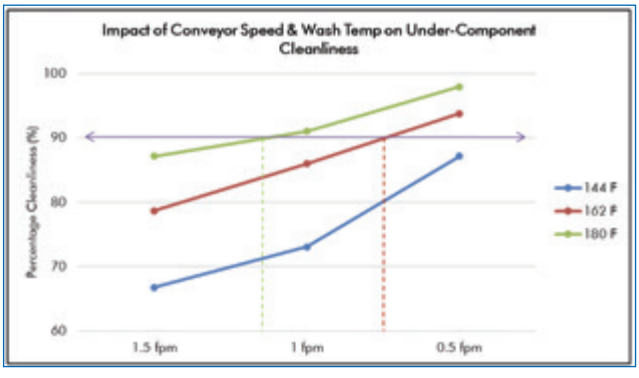

FIGURE 15. Under-component cleanliness: impact of conveyor speed and wash temperature.

- The arrows for both conveyor speed and wash temperature are shorter than the arrows for the component types. This indicates there is greater confidence in predicting the cleanliness results of one component type based on those of another than predicting cleanliness results directly using conveyor speed or wash temperature.

The qualitative plots show the relationship between the solder pastes, cleaning agents, and solder mask options on the average cleanliness level achieved for each substrate within the 216 trials (**FIGURES 18-20**).

Observations from the FAMD qualitative analysis (solder paste):

- The center of the ellipses corresponds to the average cleanliness results for each solder paste and the area of the ellipses corresponds to variability of those cleanliness results.
- This plot shows the distribution of all boards on the same axes without the quantitative variables. Instead, the boards are color-coded based on solder paste used.
- Most boards fall within the same region near the origin and in quadrants I, II, and IV. This indicates the cleaning results for most boards are similar and only a few boards such as those in quadrant III have results that are extremely dissimilar to the others.
- The center point of the Solder Paste A ellipse is close to the center point of the Solder Paste C ellipse. This signifies there is little difference in the cleaning results between these two solder pastes. Additionally, the ellipses of Solder Paste A and Solder Paste C are the smallest, which means they show the least variability in the cleaning results.
- The center point for the ellipse for Solder Paste D is dragged into quadrant III because of the outlier points. These outlier points show the greatest difference in cleaning results from the average board, which is located at the origin of the graph. These outlier points also contribute toward the ellipse for Solder Paste D having the largest size and therefore the largest variability.

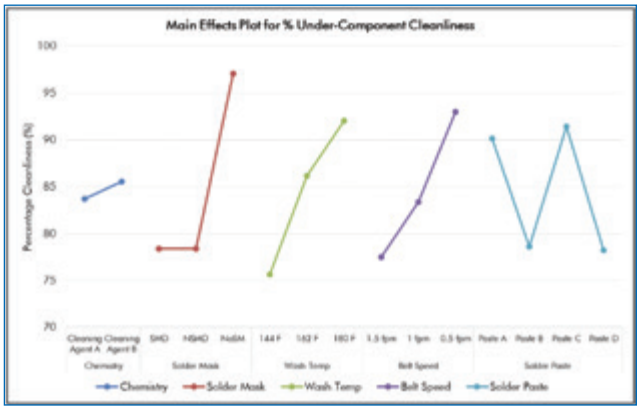

FIGURE 16. Under-component cleanliness vs. process variables.

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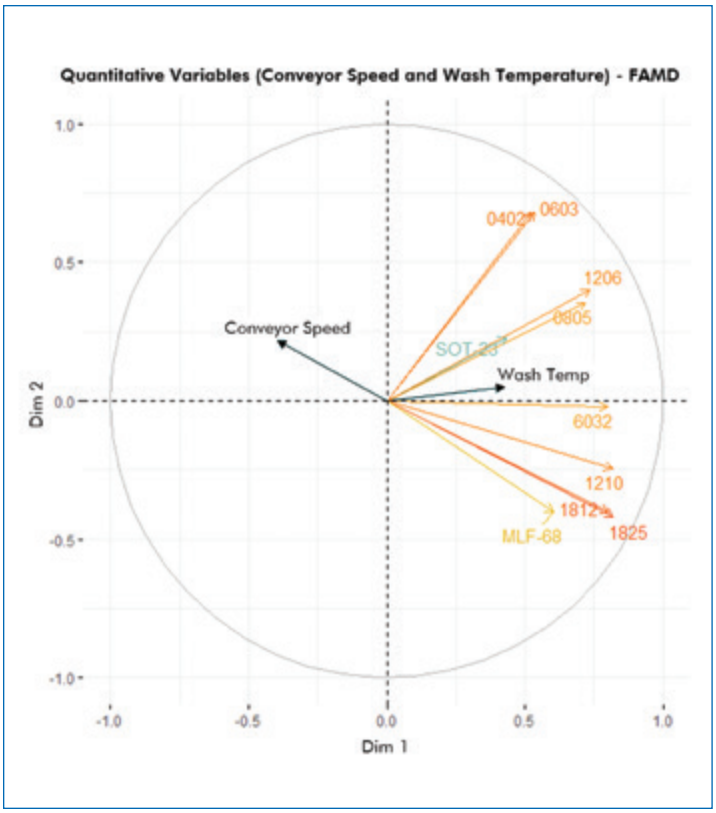


FIGURE 17. Quantitative plot.

Observations from the FAMD qualitative analysis (cleaning agent):

- This plot details the distribution of all boards on the same axes without the quantitative variables. Instead, the boards are color-coded based on the cleaning agent used.
- The ellipses for both Cleaning Agent A and Cleaning Agent B are similarly sized, indicating they show similar amounts of variability in the cleaning results.
- Both ellipses are close to the origin, which indicates the average cleanliness for either Cleaning Agent A or Cleaning Agent B is close to the average cleanliness for all the boards.

Observations from the FAMD qualitative analysis (solder mask):

- This plot shows the distribution of all boards on the same axes without the quantitative variables. Instead, the boards are color-coded based on the type of solder mask.
- The ellipses for NSMD and SMD are similar in both size and location, indicating similar levels of cleanliness and variability.
- The ellipse for NoSM is very small, indicating very little variability in the cleanliness results. The center point of the ellipses is slightly farther away from the origin, indicating the average cleanliness for NoSM is more different from the overall average than for NSMD and SMD.

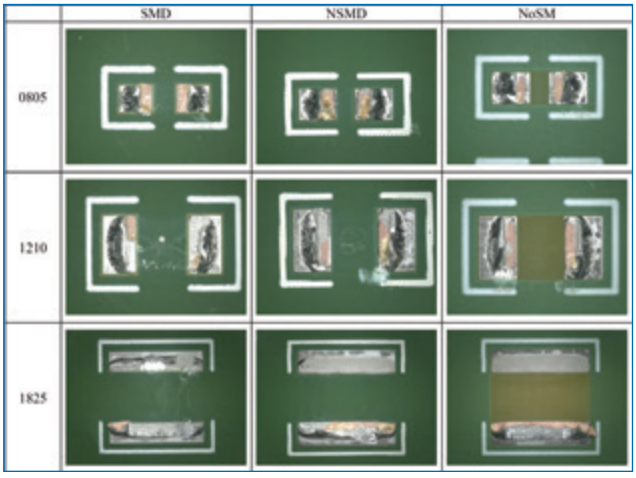
Finally, both localized IC and localized extraction electrical tests were conducted on four select components for each solder paste prior to cleaning. (NSMD option board was used.) The components selected were 1812, MLF-68, 0805 and 1210.

Localized IC was conducted using the localized extraction method.[3] All IC analysis and localized extraction tests were conducted at the company technical center. The company standards for passing IC results are based on an average used by certified industry labs. The standards used and IC data are detailed in the appendix (online).

TABLE 7. Process Operating Parameters

Cleaning Process	Inline
Equipment	Inline Spray-in-air
Concentration	15%
Conveyor Speed	1.5 fpm, 1 fpm, 0.5 fpm
Pre-Wash Pressure (Top/Bottom)	50 PSI / 30 PSI
Wash Pressure (Top/Bottom)	80 PSI / 60 PSI
Wash Solution Temperature	144°F, 162°F, 180°F
Chemical Isolation Pressure (Top/Bottom)	25 PSI / 25 PSI
Rinse	
Rinsing Agent	DI-water
Rinse Pressure (Top/Bottom)	80 PSI / 60 PSI
Rinsing Temperature	150°F
Final Rinse Pressure (Top/Bottom)	30 PSI / 30 PSI
Final Rinse Temperature	Room Temperature
Drying	
Drying Method	Hot Circulated Air
Drying Temperature (D1)	180°F
Drying Temperature (D2)	210°F
Drying Temperature (D3)	210°F

TABLE 8. Component Types



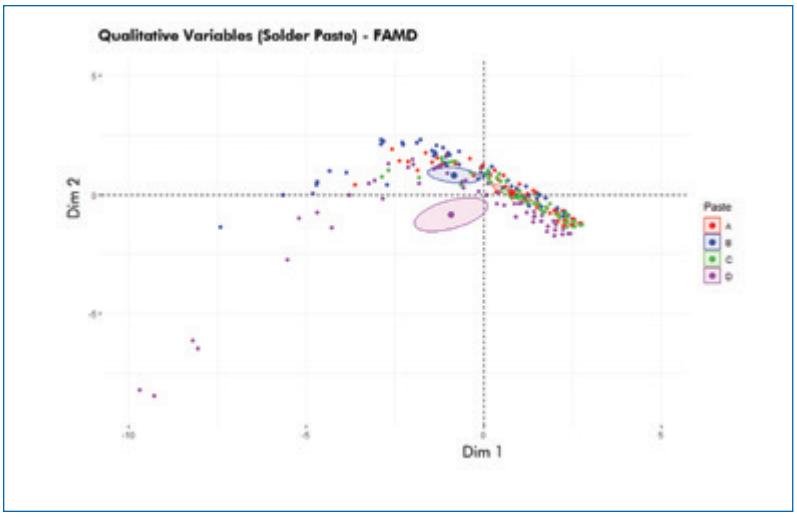


FIGURE 18. Qualitative plot (solder paste).

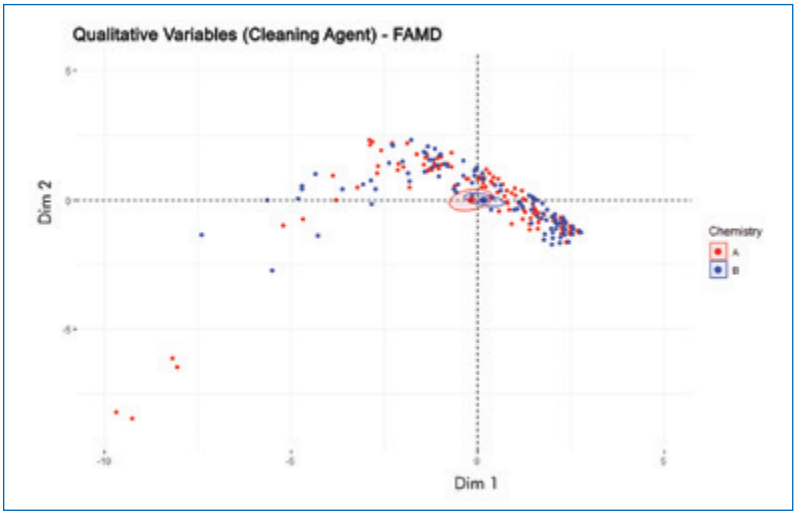


FIGURE 19. Qualitative plot (cleaning agent).

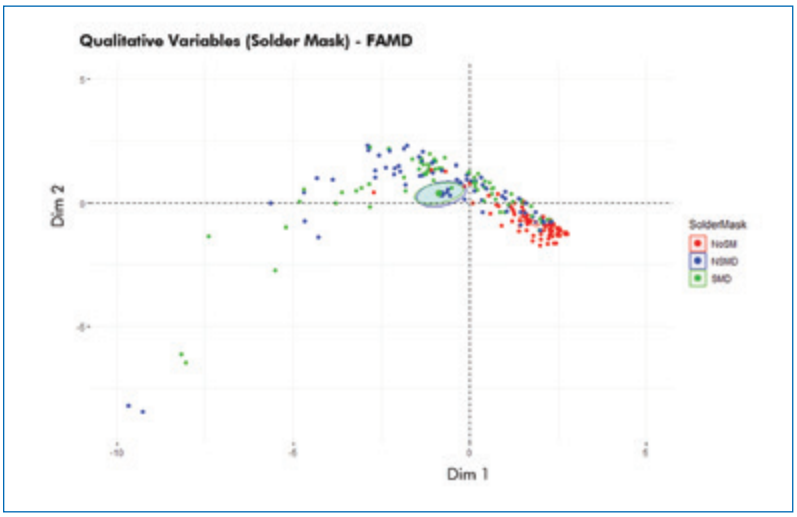


FIGURE 20. Qualitative plot (solder mask).

As part of the localized extraction analysis, an electrical test was conducted whereby a leakage current event can be identified based on a Class 2-3 setting established by the manufacturer of this specific equipment. In brief, using a sacrificial Y-pattern electrode immersed in the collected extraction solution, a 10V bias (+/-0.1V) is applied to the electrode, and an internal timer is started to measure the time it takes to achieve a leakage event. The system measures leakage current across the electrode generated by the extraction solution plus the residues extracted from the board surface. A threshold of 250µA was set to identify when a current leakage event occurs. If 250µA is achieved in less than 120 sec., this correlates to a corrosive surface and is identified as "dirty." In theory, the more corrosive/conductive the residue, the faster it will take to achieve this event. The less corrosive or conductive the residue, the longer it will take to achieve. Thus, timing events that take longer than 120 sec. have correlated to cleaner, less corrosive residues and are identified as "clean."[3]

For each solder paste and for all components tested, IC and localized extraction electrical test yielded passing results (**TABLES 9-12**, see Appendix). As this was the case, the authors chose not to conduct IC on the cleaned boards.

Conclusions

Surface inspection:

- For all trials, board surface was found to be clean, except minor residues around MLF/BTC components on a few boards.

Under-component inspection – impact of solder mask:

- Cleaning results improve significantly when using NoSM option compared to SMD and NSMD (i.e., 97.07% versus 78.4%).

Under-component inspection – impact of conveyor speed:

- Cleaning results improved significantly at lower conveyor speed (0.5 fpm) compared to faster conveyor speed (1.5 fpm) (i.e. 92.97% versus 77.52%).

Under-component inspection – impact of wash temperature:

- Cleaning results improved significantly at higher wash temperature (180°F) compared to lower wash temperature (144°F) (i.e., 92.04% versus 75.67%).

Under-component inspection – impact of conveyor speed and solder mask:

- If NoSM option is used instead of SMD and NSMD, conveyor speed can be increased three times faster (i.e., 1.5 fpm from 0.5 fpm), while keeping same wash temp.

Under-component inspection – impact of wash temperature and solder mask:

- If NoSM option is used instead of SMD and NSMD, wash temperature can be lowered from 180°F to 144°F, while keeping same conveyor speed.

Under-component inspection – impact of conveyor speed and wash temperature:

- The same under-component cleanliness results can be achieved with a combination of high wash temperature (180°F) and faster conveyor speed (1.2 fpm) compared to low wash temperature (144°F) and slower conveyor speed (0.4 fpm).

Localized extraction and ion chromatography results:

- Localized extraction and ion chromatography tests were conducted on unclean boards for each type of solder paste to verify if these methods can be used for data analysis. We had passing results (i.e., "clean") for all unclean boards, so this method was not used for data analysis.

Overall Conclusions

- Solder mask is the most critical factor impacting under-component cleanliness. NoSM option is significantly easier to clean compared to SMD and NSMD options.
- Wash temperature and wash exposure time are critical factors that also impact under-component cleanliness.
- By increasing wash temperature, we can also increase conveyor speed and achieve complete under-component cleanliness. ▫

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2. STHDA: FAMD – Factor Analysis of Mixed Data in R: Essentials.
3. S. Shoda and T. Munson, "Cleanliness Assessment Correlation to Electronic Hardware Reliability," IPC Apex Expo, March 2014.

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Appendix

TABLE 9. Ion Chromatography and Localized Extraction Electrical Test Results – Solder Paste A

		Acceptance Criteria	1812	MLF-68	805	1210
ANIONS	Fluoride (F^-)	3	0	0	0	0
	Acetate ($C_2H_3O^-_2$)	3	ND	ND	ND	ND
	Formate (CHO^-_2)	3	ND	0.412	0.794	0.406
	Chloride (Cl^-)	3	0	0	0	0
	Nitrite (NO_2^-)	3	0.016	ND	0.004	0.01
	Bromide (Br^-)	6	0	0	0	0
	Nitrate (NO_3^-)	3	2.032	0	0.208	1.624
	Phosphate (PO_4^{2-})	3	ND	ND	ND	ND
	Sulfate (SO_4^{2-})	3	0.594	0	1.158	0.492
	WOA (Weak Organic Acid)	25	2.662	ND	ND	ND
CATIONS	Lithium (Li^+)	3	0.002	0	0	0.002
	Sodium (Na^+)	3	0	0	0	0.008
	Ammonium (NH_4^+)	3	0	0	0	0
	Potassium (K^+)	3	0.858	0	0	0.744
	Magnesium (Mg^{2+})	n/a	0	0	0.212	0.036
	Calcium (Ca^{2+})	n/a	0	0	2.342	0.676
Localized Ion Chromatography Results			Pass	Pass	Pass	Pass
Localized Extraction Electrical Test Results		<250µA for 120s or more	Clean	Clean	Clean	Clean

TABLE 10. Ion Chromatography and Localized Extraction Electrical Test Results – Solder Paste B

		Acceptance Criteria	1812	MLF-68	805	1210
ANIONS	Fluoride (F^-)	3	0	0	0	0
	Acetate ($C_2H_3O^-_2$)	3	ND	ND	ND	ND
	Formate (CHO^-_2)	3	0.618	0.756	0.87	0.728
	Chloride (Cl^-)	3	0.06	0	0.792	0.808
	Nitrite (NO_2^-)	3	ND	ND	0.028	0.022
	Bromide (Br^-)	6	0.502	3.564	0.11	0.406
	Nitrate (NO_3^-)	3	0.134	0	0.426	0.352
	Phosphate (PO_4^{2-})	3	ND	ND	ND	ND
	Sulfate (SO_4^{2-})	3	2.134	0.728	0.142	0
	WOA (Weak Organic Acid)	25	ND	23.292	ND	ND
CATIONS	Lithium (Li^+)	3	0.002	0.002	0.002	0.002
	Sodium (Na^+)	3	0	0	0.24	0
	Ammonium (NH_4^+)	3	0	0	0	0.1
	Potassium (K^+)	3	0	0	0.366	0
	Magnesium (Mg^{2+})	n/a	0.09	0	0.132	0.222
	Calcium (Ca^{2+})	n/a	0.56	2.448	0	0.048
Localized Ion Chromatography Results			Pass	Pass	Pass	Pass
Localized Extraction Electrical Test Results		<250µA for 120s or more	Clean	Clean	Clean	Clean

TABLE 11. Ion Chromatography and Localized Extraction Electrical Test Results – Solder Paste C

		Acceptance Criteria	1812	MLF-68	805	1210
ANIONS	Fluoride (F^-)	3	0	0	0	0
	Acetate ($C_2H_3O^-_2$)	3	ND	ND	ND	ND
	Formate (CHO^-_2)	3	0.516	0.51	0.648	0.698
	Chloride (Cl^-)	3	0.152	0	0.458	0
	Nitrite (NO_2^-)	3	ND	0.03	ND	0.032
	Bromide (Br^-)	6	0.236	0	0.198	0.162
	Nitrate (NO_3^-)	3	0.476	0.7	0.442	0.306
	Phosphate (PO_4^{2-})	3	ND	ND	ND	ND
	Sulfate (SO_4^{2-})	3	1.562	0.258	2.328	0.61
	WOA (Weak Organic Acid)	25	ND	ND	ND	ND
CATIONS	Lithium (Li^+)	3	0.004	0	0.004	0
	Sodium (Na^+)	3	0	0	0	0
	Ammonium (NH_4^+)	3	0.008	0.018	0	0
	Potassium (K^+)	3	0	0.022	0.222	0
	Magnesium (Mg^{2+})	n/a	0.122	0.222	0.282	0.17
	Calcium (Ca^{2+})	n/a	1.258	0	0.914	1.63
Localized Ion Chromatography Results			Pass	Pass	Pass	Pass
Localized Extraction Electrical Test Results		<250µA for 120s or more	Clean	Clean	Clean	Clean

TABLE 12. Ion Chromatography and Localized Extraction Electrical Test Results – Solder Paste D

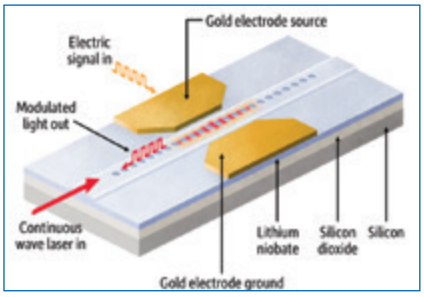
		Acceptance Criteria	1812	MLF-68	805	1210
ANIONS	Fluoride (F^-)	3	0	0	0	0
	Acetate ($C_2H_3O^-_2$)	3	ND	ND	ND	ND
	Formate (CHO^-_2)	3	0.622	0.51	0.814	0.886
	Chloride (Cl^-)	3	0.21	0	0	0.026
	Nitrite (NO_2^-)	3	0.024	0.034	0	0.04
	Bromide (Br^-)	6	0	0	0.056	0.096
	Nitrate (NO_3^-)	3	0.518	0.388	1.004	0.316
	Phosphate (PO_4^{2-})	3	ND	ND	ND	ND
	Sulfate (SO_4^{2-})	3	1.118	0	0.134	1.284
	WOA (Weak Organic Acid)	25	ND	ND	ND	ND
CATIONS	Lithium (Li^+)	3	0.002	0	0.002	0.002
	Sodium (Na^+)	3	0	0	0	0
	Ammonium (NH_4^+)	3	0.124	0	0.266	0.166
	Potassium (K^+)	3	0	0	0.314	0
	Magnesium (Mg^{2+})	n/a	0.12	0.236	0.078	0.202
	Calcium (Ca^{2+})	n/a	1.62	0	0	0.658
Localized Ion Chromatography Results			Pass	Pass	Pass	Pass
Localized Extraction Electrical Test Results		<250µA for 120s or more	Clean	Clean	Clean	Clean

State-of-the-Art Technology Flashes

Updates in silicon and electronics technology. by GARY MILLER

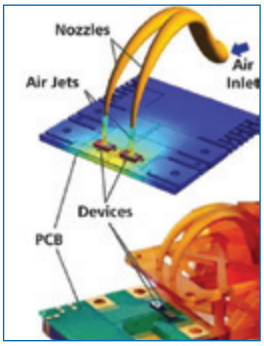
Ed.: This is a special feature courtesy of Binghamton University.

Smallest on-chip optical modulator has switching speed up to 11Gb/s. University of Rochester researchers have created the world's smallest modulator for photonic integrated circuits, augmenting communications, computing, and photonics research. The device consists of a thin film of lithium niobate (LN) bonded on a silicon dioxide layer to create a modulator that, besides being small, operates at high speed and is energy-efficient. The modulator occupies an electro-optical modal volume of 0.58μm^3 and has a modulation bandwidth of 17.5GHz, switching speeds of up to 11Gb/s and a tuning efficiency of up to 1.98GHz/V. Applications include communications, computing, and quantum photonic information processing. *(IEEC file #11886, Laser Focus World, 8/27/20)*



New memory device built using FTJ technology. University of Southern California researchers have developed a new memory technology based on ferroelectric tunneling junction (FTJ) technology using asymmetric metal and semi-metallic graphene materials. FTJ devices promise to increase data upload speed, extend smartphone battery life, and reduce data corruption. The unique ability of these materials to approach atomic-scale thickness can eventually lead to even faster and more energy-efficient FTJ memory down the line. These materials permit building devices that can potentially be scaled to atomic-scale thickness, which means the voltage required to read, write, and erase data can be drastically reduced, which in turn makes the memory electronics much more energy-efficient. *(IEEC file #11826, Electronics Weekly, 7/24/20)*

Electronics cooling using additive manufacturing. University of Illinois researchers have developed a new type of air jet cooler that overcomes previous barriers to jet cooling systems. Using additive manufacturing, they created an air-jet cooling system in a single component that can direct high-speed air onto multiple electronics hot spots. They manufactured the cooling system from strong polymer materials that can withstand the harsh conditions associated with high-speed air jets (200mph). The research focused on heat removal from high-power electronic devices. The thermal management problems of high-power electronic devices are in many applications, including electric vehicles, aircraft, automotive, and off-road vehicles. *(IEEC file #11904, NASA Tech Briefs, 9/1/20)*

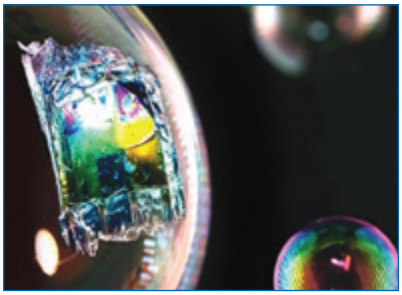


Artificial "neurotransistor" created. Researchers from TU Dresden and HZDR have successfully imitated the functioning of brain neurons using semiconductor materials. The approach is based on the brain, combining data processing with data storage in an artificial neuron. They simulated the properties of neurons using the principles of biosensors and modified a classical field-effect transistor to create an artificial "neurotransistor." The advantage of this new architecture lies in the simultaneous storage and processing of information in a single component. In conventional transistor technology, they are separated, which slows processing time and limits performance. *(IEEC file #11819, Science Daily, 7/14/20)*

Shrunken nanolasers enable on-chip optical connections. Moscow Institute researchers have solved the problems that had prevented the creation of electrically driven nanolasers for ICs. Their approach uses a coherent light source design on the

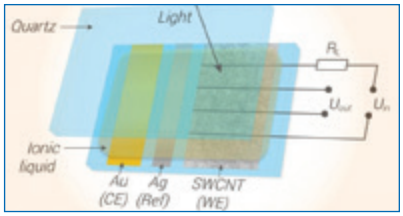
scale smaller than the wavelength of light emitted by the laser, which enables ultrafast optical data transfer in microprocessors. The electrical pumping is based on a double heterostructure with a tunneling Schottky contact that happens across the interface between the plasmonic metal and semiconductor. The plasmonic nanolaser is smaller than the wavelength of the light it emits. *(IEEC file #11901, Electronics Weekly, 9/17/20)*

Inkjet-printed thin-skinned solar panels. Solar cells can now be made so thin and flexible that they can rest on a soap bubble. These new cells, which efficiently capture energy from light, could offer an alternative way to power novel electronic devices, such as medical skin patches. Until now, ultrathin organic solar cells were typically made by spin-coating or thermal evaporation, which are not scalable and limit device geometry. To overcome these limitations King Abdullah University researchers applied inkjet printing, and printed a transparent, flexible, conductive polymer called PEDOT:PSS. The electrode layers sandwiched a light-capturing organic photovoltaic material. The solar cells achieved a power conversion efficiency (PCE) of 4.73%. The team also printed a cell onto an ultrathin flexible substrate with a PCE of 3.6%. *(IEEC file #11880, Printed Electronics World, 9/1/20)*



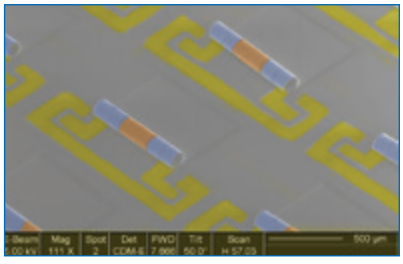
UCL breaks data transmission speed record. A team of UCL engineers achieved the world's fastest data transmission rate at an internet speed 20% faster than the previous record. The team achieved a data transmission rate of 178 terabits a second, a speed at which it would be possible to download the entire Netflix library in less than a second. The record, which is double the capacity of any system currently deployed in the world, was achieved by transmitting data through a much wider range of colors of light, or wavelengths, than is typically used in optical fiber. The benefit of the technique is it can be deployed on already existing infrastructure cost-effectively, by upgrading the amplifiers that are located on optical fiber routes at 40-100km intervals. *(IEEC file #11864, Electronics Weekly, 8/24/20)*

Researchers improve carbon nanotube transparent conductors. Aalto University researchers have discovered electrochemical doping with ionic liquid can significantly enhance the optical and electrical properties of transparent conductors made of single-walled carbon nanotube films. A single-walled carbon nanotube (SWCNT) is a seamless rolled sheet of graphene one atom thick. SWCNT films are highly conductive, flexible, stretchable and can be easily doped because all atoms in the nanotube are located on its surface. Moreover, the doping process leads to an increase in the transmittance of the films due to supersession of optical transitions. The applications for transparent conductors include medicine, green energy, etc. *(IEEC file #11860, Printed Electronics World, 8/5/20)*



Next-generation shielding may absorb electromagnetic interference rather than reflect it. Drexel University and KAIST researchers are developing shielding for RF-sensitive circuitry using material that absorbs RF energy rather than just reflecting it. They are researching a class of material called MXenes (titanium carbonitride) that can be processed in a way that lets it absorb electromagnetic radiation. MXenes are called 2-D compounds because they have a structure consisting of layers only a few atoms thick. The material itself consists of transition metal carbides or carbonitrides. It exhibits a high conductivity because of the metal content and is hydrophilic because the surfaces comprising it have hydroxyl or oxygen terminations. *(IEEC file #11861, R&D World, 7/30/20)*

Combining capacitors and inductors in a single component. University of Illinois researchers have devised a method of combining capacitors and inductors in a tiny, 3-D-rolled membrane. This will save space in the electronic filters found in phones and other wireless devices. The team used a specialized etching and lithography process to pattern 2-D circuits onto thin membranes. In the circuits, they join capacitors and inductors together with ground or signal lines, all in a single plane. The multilayer membrane was then rolled into a thin tube and placed on a chip. This electron microscope image below shows an array of new chip components that combine the inductors (blue) and capacitors (yellow) needed to make electronic signal filters in phones and other wireless devices. *(IEEC file #11865, Microwave & RF, 8/25/20)*



Photonics researchers report breakthrough in miniaturizing light-based chips. Photonic ICs that use light instead of electricity for computing and signal processing promise greater speed, increased bandwidth, and greater energy efficiency than circuits using electricity. But they are not yet small enough to compete in computing and other applications. University of Rochester engineers have taken a major step in addressing the problem. By using a thin film of lithium niobate (LN) bonded on a silicon dioxide layer, they created the smallest electro-

optical modulator yet. The modulator is a key component of a photonics-based chip, controlling how light moves through its circuits. This is a crucial foundation for realizing large-scale LN photonic ICs that are of immense importance for broad applications in data communication, microwave photonics, and quantum photonics. *(IEEC file #11867, Semiconductor Digest, 8/27/20)*

Parylene photonics enable future optical biointerfaces. Carnegie Mellon researchers have invented an optical platform called "Parylene photonics" that could likely become the new standard in optical biointerfaces. To create this new photonic material class, they designed ultracompact optical waveguides by fabricating silicone (PDMS) around a core of Parylene C. The contrast in refractive index permits the waveguide to pipe light effectively, while the materials themselves remain extremely pliant. The result is a platform that is flexible, can operate over a broad spectrum of light, and is just 10µm thick. The applications for Parylene photonics could one day replace current technologies in virtually every area of optical biointerfaces. Parylene photonic devices placed on the skin could be used to conform to difficult areas of the body and measure pulse rate, oxygen saturation, etc. *(IEEC file #11907, Science Daily, 9/22/20)*

Market Trends

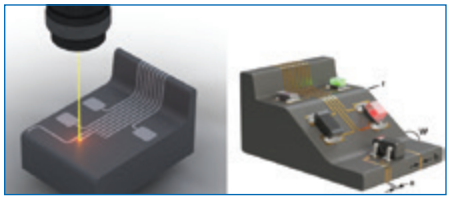
Sensors help predict when 3-D-printed parts will fail. 3-D-printed parts have a key advantage for the armed forces because they can be made quickly and easily at less cost onsite or in the field, providing a tactical advantage. 3-D-printed parts typically have structural imperfections that can negatively impact strength and performance in ways that traditionally machined parts do not. Determining when a part will fail could be the difference between successfully completing a mission and needing to be rescued. US Army researchers recently discovered a way to use sensors to monitor the performance and degradation of 3-D printed parts over time. With this data, they can predict when a part will need to be replaced. The goal of predictive maintenance is to get the most life out of a part before it breaks. *(IEEC file #11911, ASME, 9/15/20)*


Embedded sensors may enable better monitoring of wear. Photo: Army Research Laboratory

The electronic skin market to reach $16 billion by 2026. The electronic skin market is set to grow from its 2019 market value of $6 billion to $16 billion by 2026. The technology finds a wide range of use-cases on account of its self-healing characteristics and self-powering abilities. Electronic skin and patches can be used for patients with prosthetics to provide a sense of touch. Electronic skin patches form an essential component of microcurrent facemasks. Electro-active polymers, stretchable conductors, stretchable circuits, and photovoltaic systems are different components of an electric skin. Electro-active polymers are generally preferred over conventional electronic wearables, owing to benefits such as up to 10 times more battery life, noiseless operation, and ultra-low power consumption. *(IEEC file #11833, Semiconductor Digest, 7/15/20)*

Noise-cancelling smart window blocks street din. Nanyang Technological University researchers have created a noise-cancelling smart window. A sensor picks up a regularly repeating waveform, then electronics characterizes the wave, generates a mirror image, and emits that second "antiwave" from a speaker, causing the two waves' peaks to cancel out. Antinoise works best for frequencies above 300Hz and up to about 1000Hz. Antinoise also works best in limited spaces, where the wave and its antiwave are sure to meet up properly, as in the gap between a headphone and an ear. The researchers demonstrated an array of 24 small speakers placed in a window, together with a sensor strong enough to cut the room's noise by 10dB. *(IEEC file #11832, IEEE Spectrum, 7/15/20)*

Electronic assemblies without PCBs. Laser direct structuring (LDS) makes it possible to apply electronic conductor paths directly onto plastic parts during series production, hence enabling the production of electronic assemblies with flexible geometric shapes. This process enables electronic products (such as smartphones, sensors, or medical devices) to become even smaller and more powerful. Automated manufacturing processes also make this process more economically attractive. LDS enables further miniaturization and makes increasingly complex geometric designs possible. This is a stable and reliable process that has established itself in quality-critical sectors such as medical technology or safety-relevant components for the automotive industry. *(IEEC file #11900, EMS Now, 9/10/20)*



Recent Patents

Shape-memory alloy connector for plated through-hole (assignee: IBM Corp.), patent no. 16/351,695. Shape-memory alloy connectors and methods are provided for enhancing conductivity of a plated through-hole of a circuit board. A shape-memory alloy connector, including a shape-memory alloy material in deformed shape, is inserted into the plated through-hole of the circuit board. The shape-memory alloy connector is expanded within the plated through-hole by heating the shape-memory alloy material to, at least in part, transition the shape-memory alloy material toward a pre-deformed shape of the material. The transitioning of the shape-memory alloy material toward the pre-deformed shape expands the shape-memory alloy connector outward, at least

in part, against plating of the plated through-hole to enhance contact of the shape-memory alloy connector with the plating of the plated through-hole.

Package on active silicon semiconductor packages (assignee: Intel Corp.), pub. no. EP3688801. Systems and methods provide a low-profile stacked die semiconductor package in which a first semiconductor package is stacked with a second semiconductor package, and both semiconductor packages are conductively coupled to an active silicon substrate that communicably couples the first package to the second package. The first package may conductively couple to the active silicon substrate using a plurality of interconnects disposed in a first pattern having a first interconnect pitch. The second package may conductively couple to the active silicon substrate using interconnects disposed in a second interconnect pattern having a second pitch that is greater than the first pitch.

Semiconductor with integrated electrically conductive cooling channels (assignee: Ford Global Technologies), patent no.16/269702. A semiconductor assembly includes a power semiconductor, a housing containing the power semiconductor, and electrically conductive channels. The electrically conductive channels are arranged to direct coolant through the housing. Heat generated by the power semiconductor can therefore be absorbed by the coolant. The electrically conductive channels are also electrically connected with the power semiconductor to form terminals for the power semiconductor.

Semiconductor package having routable encapsulated conductive substrate (assignee: Amkor Technology), patent no.16/86105. A packaged semiconductor device includes a routable molded lead frame structure with a surface finish layer. In one embodiment, the routable molded lead frame structure includes a first laminated layer, including the surface finish layer, vias connected to the surface finish layer, and a first resin layer covering the vias leaving the top surface of the surface finish layer exposed. A second laminated layer includes second conductive patterns connected to the vias, bump pads connected to the second conductive patterns, and a second resin layer covering one side of the first resin layer, the second conductive patterns and the bump pads. □

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Product Development and the 7 Wastes

Striking the right balance between costs and cycle time.

DECISIONS MADE IN product design can impact assembly cost, defect opportunities and inventory cost. While design for manufacturability (DfM) analysis can eliminate many issues, less commonly analyzed decisions related to cost targets, scheduling and work team assignments can have unintended consequences that generate unacceptable levels of waste.

Lean manufacturing practitioners are aware of Taiichi Ohno's concept of the seven wastes (*muda*) in manufacturing as part of the Toyota Production System (TPS). To recap, those seven wastes are:

1. Waste of overproducing (no immediate need for product being produced).
2. Waste of waiting (idle time between operations).
3. Waste of transport (product moving more than necessary).
4. Waste of processing (doing more than what is necessary).
5. Waste of inventory (excess above what was required).
6. Waste of motion (any motion not necessary outside of production).
7. Waste of defects (producing defects requiring rework).

To better illustrate the impact of some of these less-analyzed choices, we will focus on some common scenarios and the wastes they drive.

The cost-reduction conundrum. Material typically constitutes 65 to 75% of product cost. Focusing on reducing bill of materials (BoM) cost seems like the best way to reduce product cost. But this can result in increases in the wastes of inventory, processing and defects. For example, in one redesign for cost reduction, an OEM doubled the number of components on the BoM. While the components represented a lower total BoM cost, the new design required more parts to do the same thing as fewer, albeit more expensive, components. Inventory increased, placements doubled, and the greater number of solder joints meant a higher number of defect opportunities. In this example, the OEM team was surprised assembly cost increased substantially. This type of situation can happen any time teams in procurement, design and manufacturing engineering work in silos. The better solution is a holistic approach that considers the impact of perceived material savings against increases in assembly cost or complexity.

The all-inclusive layout. Design cycle times are shrinking. One way to speed development of a new platform is to develop a high-level architecture that encompasses all features for multiple variants. Each variant is populated with the components needed for that product. The unintended consequence is that this "one size fits all" approach often breaks common DfM layout rules and adds complexity to the manufacturing process. Some common wastes it can drive include:

- The wastes of processing and transport when the all-inclusive printed circuit board assembly is double-sided SMT and an application-specific layout would require only single-sided SMT placement.
- Additional waste of processing on mixed-technology PCBs when bottom-side SMT components required by the all-inclusive layout require a masking pallet in wave solder.
- The waste of defects driven by tradeoffs in design rules to accommodate the layout required to cover all variants of the design.

The better choice is to transition the all-inclusive development layout to application-specific layouts to simplify assembly and test. This can lower assembly and tooling cost while eliminating defect opportunities.

Concurrent design and stackup surprises. When products are concurrently designed by multiple teams, and one or more of those teams push mechanical tolerances, the mechanical part stackup may not fit the packaging. Another error of this nature can occur when connectors and cables are left to the end of the design phase. This often leads to the waste of defects if the issue isn't addressed or the waste of processing if a workaround is added to correct the issue.

For example, a design had a cavity designed to fit a substrate mated with SMT headers. A late change to the design for leaded headers left inadequate space beneath the PCB to accommodate the solder fillet and device lead. With less than 1mm space available, the design team needed to adopt special header components and work with the manufacturing team to optimize the solder process due to a very shallow cavity. Ultimately, this workaround could result in field failures due to solder fillet fractures. Adequate space for leaded parts terminating the cable wasn't factored into initial design dimension considerations.

Performing DfM analysis on a 3-D model of the final product in packaging early enough to easily make adjustments can eliminate surprises that can otherwise occur in multi-team concurrent design efforts.

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X-ray Inspection of Low-Temperature Solder Joints

Results of experiments on PTH parts.

USE OF LOW-TEMPERATURE solders (LTS) is growing in popularity. LTS are predominantly composed of tin and bismuth, with a small quantity of a "special blend" of other elements to suit a given manufacturer's performance specifications. The opportunity, as the name suggests, is to create solder joints at far lower temperatures than those required for tin/silver/copper (SAC) alloys, and which are even lower than that needed for the (historic?) tin/lead eutectic solder. These LTS have a melting temperature of ~138°C. The benefits of using LTS mean no Pb is present in the joint, and lower processing temperatures can be used. Using lower temperatures means reduced energy consumption during manufacture, lower manufacturing costs and reduced greenhouse emissions. In addition, it offers the opportunity to use different, thinner and possibly cheaper PCB substrates and components compared with those used today. This obviates the "overengineering" required of today's boards and components to mitigate warpage, which due to LTS are operating close to the glass transition temperature of the board material. It also makes it possible to rework SAC area array package joints with low-temperature alloys.

Sadly, as ever, physics does not provide a free lunch. While LTS may be appropriate for selected products, and new LTS configurations are continually coming to market, it must be noted that LTS are less ductile than SAC alloys. This means the joints produced are more brittle and therefore potentially more prone to tearing, or cracking, following thermal or physical shock. Therefore, as with all solder joints, the need for inspection of LTS joints using both x-ray and optical techniques remains important for ensuring manufacturing quality.

For those considering LTS, then, from an x-ray inspection perspective, the first question to ask is can we see these solder joints in the x-ray equipment? The simple answer, as the QFN soldered with a low-temperature solder in **FIGURE 1** shows, is yes. This is because bismuth sits next to lead in the periodic table and, therefore, being as dense, absorbs x-rays passing through to create a well-contrasted image for analysis. This image looks in the x-ray to be no different from SAC alloy versions that readers have seen in some of my previous columns.

LTS and through-hole joints. As x-ray images of LTS joints look similar to their SAC cousins, the same analytical techniques I have suggested in previous columns remain true and, I hope, still offer better analysis for potential failures. However, as LTS joints are more brittle, the potential for more subtle tear, or crack, defects is possible, and these features, if present, are likely to be harder to see. To test for this, under both x-ray and optical inspection, I am grateful to Bob Willis and others noted at the end of this column for sharing results of a small experiment they conducted.

In the experiment, surface-mount components were assembled on four-layer, 1.6mm-thick PCB sample boards using a SAC alloy with the appropriate oven reflow temperature cycle. Afterward, a selective soldering system was used to assemble the through-hole components using a low-temperature solder. The finished boards were then subjected to thermal cycling between -55° and +125°C. The selective soldering process used a topside preheat temperature of 90° and 100°C and a solder bath set point temperature of 255°C. The LTS used was Sn64/Bi35/Ag1, which has a melting point of 138°C. The surface finish on the boards was nickel/gold. After the thermal cycling, optical and x-ray inspection was used to see if, how and where the LTS joints might have failed and potentially identify locations and features to check when using LTS in the future. As Bob notes, this was a small project, conducted during the lockdown caused by the Covid-19 pandemic. This restricted what could be done in terms of testing. Therefore, it was not possible

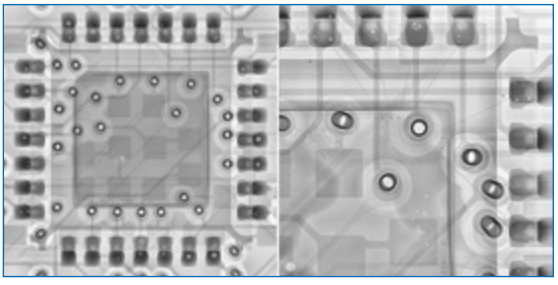

FIGURE 1. X-ray images of a QFN soldered onto a PCB using a low temperature solder (LTS).

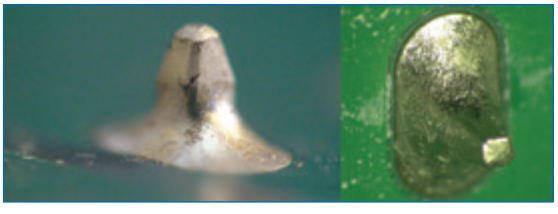

FIGURE 2. Optical images of satisfactory through-hole joints produced using selective soldering equipment with a low-temperature solder alloy and following 1,000 thermal cycles.

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to conduct x-ray inspection and microsectioning on some of the samples before subjecting them to temperature cycling.

Sample x-ray and optical images from these experimental boards are shown. **FIGURE 2** shows optical images of satisfactory through-hole joints using LTS. Optical inspection after 1,000 thermal cycles showed no apparent evidence of surface changes to the through-hole joints (Figure 2). After a further 1,000 thermal cycles, however, some joints did show evidence of cracks in the surface of the solder that were not seen before. In some of the joints these cracks were located at the joint surface directly above the barrel of the plated through-hole and at the solder fillet interface (**FIGURE 3**).

FIGURE 4 shows top-down and oblique angle x-ray images of the through-hole component joint seen in Figure 3. **FIGURE 5** is a magnified x-ray image that shows the extent of the cracking within the joint seen in Figure 3, which is not clear from the less-magnified views in Figure 4. Figure 5 shows the apparent separation of the solder from the barrel of the plated through-hole. This separation and the specific interface(s) at which the separation has occurred were established by microsectioning (**FIGURE 6**). The microsection shows cracking and separation in the bulk of the solder fillet and along the solder joint and plated through-hole interface.

X-ray inspection supports analysis for faulty joints that may occur with low-temperature solder. Observing the presence of cracks and/or tears within the joints may need the x-ray system to provide magnified and oblique angle views, as well as the ability to stretch the image contrast, so the subtle density difference between the crack, the bulk of the joint and the rest of the board has the best chance of being seen. Remember, the presence or absence of cracks on the surface when seen under optical inspection may not indicate what is happening within the joint. X-ray inspection will complement the analysis.

I am grateful to Richard Boyle of Henkel for thermal cycling and microsectioning the sample boards and to Peter Koch of Yxlon International for the x-ray images. I must again thank Bob Willis (bobwillis.co.uk) for directing the experiment, organizing the samples and taking and providing the optical images. Further information on the previous trials Bob has undertaken on LTS examples are available through his website. □

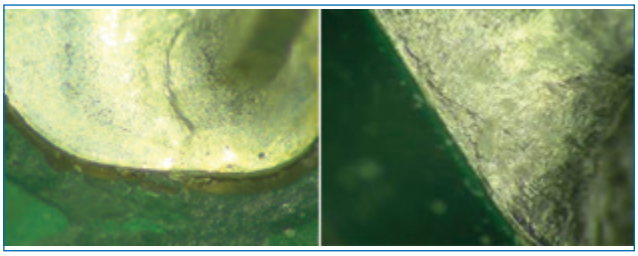

FIGURE 3. Optical images of cracks in the surface of low-temperature solder through-hole joints after thermal cycling. These cracks are located on the joint surface directly above the barrel of the plated through-hole at the solder fillet interface.

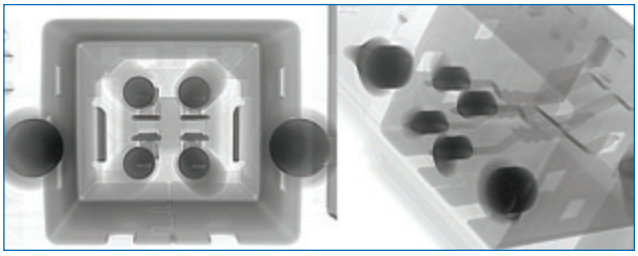

FIGURE 4. X-ray images of through-hole components selectively soldered with a low-temperature solder alloy after thermal cycling.

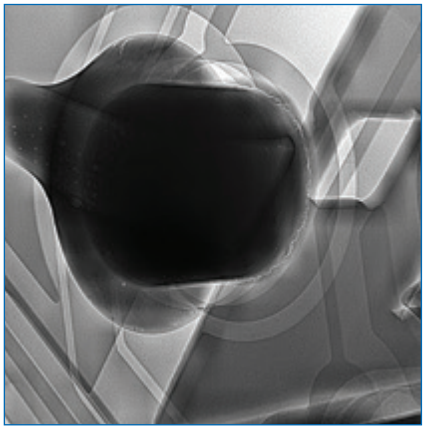

FIGURE 5. Magnified oblique angled x-ray image of low-temperature solder joint after 2,000 thermal cycles showing cracking all around the joint.

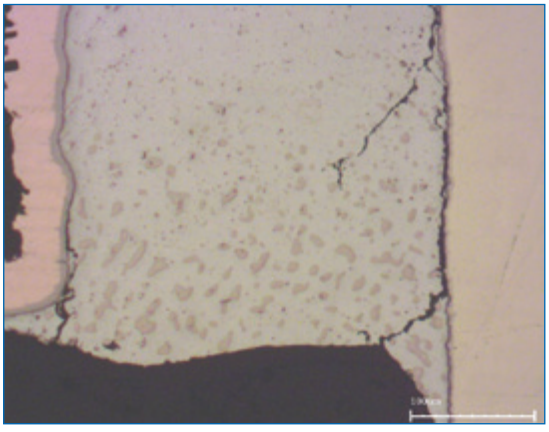

FIGURE 6. Microsection vertically through joint shown in Figure 5. Cracking and separation are seen in the bulk of the solder fillet and along the solder joint and plated through-hole interface.

Unsolicited Advice for the Morning Spammers

Sales pitches from Chinese board shops should come with arthritis medication.

DRAMATIS PERSONAE (in order of appearance):

1. Saleswomen from Chinese printed circuit board fabricators, all with curiously westernized first names.
2. Marketing types trying to sell me lists of attendees at nonexistent trade shows.
3. Serial killers.
4. Clowns (sometimes indistinguishable from #3). Generally speaking, disturbing.
5. SBA-approved loans. (I have one qualified offer right now from capitaldrip.com. I'm not making this up.)
6. Webinars about I-9 forms and Covid-19 mitigation and prevention.
7. Virtual trade shows (and the people lurking behind them).
8. SAM renewal.
9. Persons wanting me to sell our business.
10. Search engine optimization (SEO) companies, which often lead to:
11. Website developers from India named Mike.

To borrow a phrase, it's Morning in America. Somewhere sheep are bleating, and birds are chirping. Meanwhile, spam is accumulating.

My company tests printed circuit board assemblies. It also troubleshoots them when they fail those tests to identify the source of failure.

The Internet tests my patience. As each morning's caffeine jolt clears the head, bootup reveals 150 to 200 messages amassed during the preceding 24 hours. Five to 10% deserve a reply; the rest can be filed or deleted.

Time to collate one's thoughts for the day. See who needs assistance. Electronic products break daily, which is good for business. It is not unusual to open the laptop each morning and see one or two lifeboat appeals requesting immediate help. As in, that day. Time to assess the damage and formulate the daily game plan.

That is, after you hack your way through the weeds.

As in, candidates for obliteration like these:

Nice to know you here, this is Leo working for PCBs at Sunking Circuit in Shenzhen … which is a matured offshore PCB shop with wide ranges of production and various raw materials.

Matured? Old enough to drive?

Various raw materials? Like rubber, or maybe helium?

Long time quality guarantee after sales, fully automatic process.

Fast response, no matter is prompt Email reply, 2hrs quoting, 4hrs EQ advise, within 2wds for customer complain,24 hrs pcb also available, PCB assembly... etc.

Not unlike your guaranteed, fully automated spam emails infiltrating my inbox.

But see here: a two-working-day response for customer complaints. That's a clincher. Sign me up.

Also we have good control for the production, it allows us to offer the good lead time after we come back to work from the CNY holiday.

Unless, of course, you overindulged during the CNY holiday, in which case you will, ahem, exceed control limits, and good lead time becomes bad lead time.

If you don't mind, you can send me some inquiries to check our price first. It's my honor to serve you.

It's my honor to determine whether you are two one-hundredths cheaper in unit price to your nearest competitor. F.O.B. my side of the ocean. Nothing beats a race to the bottom of the barrel.

BTW, for me, I have more than 5 years engineering experience in CAM, so if you meet any engineering problems, please feel free to contact me. It's my pleasure to support you.

In attached the company presentation for reference more details. Kindly take some time to have a look. Thanks in advance. I am expecting to receive your letter soon.

Have a great day!

There you go, telling me what kind of day to have.

Then there's this uplifting pitch:

Dear friend,

This is Linda from wonderful PCB (HK) Limited.

Summer season will come soon, hope you and you family all the best .

with warm regards,

This is Linda from wonderful PCB Limited, we are professional PCB and PCBA manufacture in shenzhen china for 20 years.

Glad they're professional. Sure beats the alternative.

We …have quality assurance, may I know do you have any PCB or PCBA projects on pending? maybe you can give me a chance to let us service for you.

I've always said quality with high self-esteem is the key to good manufacturing.

Don't purchase just any PCB. Have a Wonderful PCB. All they're lacking is a Hallmark card in every shipment.

Or this:

Dear Manager,

Hope everything goes well.

ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.

Annis from Greatwall Circuit 15 years experience in PCBs manufacturing.

I can see their mission statement now: We stand athwart any PCB problems you may encounter, with all the resilience of a granite outhouse.

What we do?

Massacre English grammar, it appears.

Hi Sir

How are you these days? Hope you have a wonderful working and leisure time.

When you next consider your arrangements for PCB & PCBA products, i would welcome the opportunity to understand your requirements and situations.

We…more than 500 overseas companies choose us to expand their further business. Therefore, we growth up with our customers rapidly. And also enjoy the win-win results. Since we are the OEM of PCB, the price will be much more attractive. We strictly control the quality, you can have an amazing customer experience with me. And we have strong partners, such as global top 50 factories--SZ Suntak, SZ Fast Print and Shennan Circuit. The lead time will be also shorter than as usual. If plan A can not work, we have plans B-Z to satisfied you!

Kindly see our introduction

Give me a chance, you will find different paradise.

Paradise is at hand, for the price of a mere purchase order. Who knew?

Or this:

Hello dear manager,

Good day and hope you are well.

This is Cindy from Longteng Electronic Technology Co.,Ltd.

The picture below shows three PCBAs we have recently produced for our customers. If you have similar requirements,

Write me back or call me ,send me Gerber files& Bom list please, let's talk more in details.

I would be much gratitude if you could help forward to the purchasing manager, thanks.

Don't just have gratitude, up your game and ***be*** gratitude, dear manager.

The previous two companies should get together. The mind reels at the thought of the love child owing from the meeting of Wonderful and Gratitude.

That's just the fab shops. Then there's this appeal to making something out of nothing. Literally.

Hi,

I am following up to confirm if you are interested in acquiring the Visitors List.

Dallas Expo & Tech Forum

Date : 3/24/2020

Location : Plano, USA

Visitors : 6,500

Let me know if you are interested so that I can provide you additional details

We have Special Discount offer for this Month.

Looking forward to hearing from you.

Waiting for your response.

Have infinite patience because you will keep waiting.

Two observations: First, 6,500 attendees is a lot for a one-day tabletop show with about 75 exhibitors. The number would encompass friends, neighbors, families, and seven generations of each, draining Plano, Texas, of a sizable chunk of its population for one scintillating afternoon of face-to-face commerce. Two, and most concerning, the SMTA Dallas Expo and Tech Forum was not held on March 24, 2020. It was postponed due to the Covid outbreak.

Nice try.

Then there's this guy who defies categorization, but who reminds me and those of a certain age of an infamously patronizing and much-panned Wang Labs ad from the 1980s ("Shared a cab ride from Kennedy…"):

Hope you are well. Realized that you may not have a lot of context around the value Auth0 adds for growing companies like Datest. Thought I'd attach a picture showing how you can leverage our technology as a protocol translator sitting between your applications (native, SPA, etc) and the IdPs you want to connect to (SAML, G-Suite, U/P, etc). Trusted brands of all sizes lean on Auth0 to handle identity across their applications.

WTF?

If it's not too painful, could we set aside 15 minutes so I can get an understanding of the Datest authentication and authorization environment?

If it's not too painful, could you muster the effort to learn to write in clear declarative sentences, with a premise as well as a conclusion, supported by evidence, devoid of jargon?

Sister Mary Immaculata is warming up in the bullpen with the 12-foot long industrial-strength strand of rosary beads (the ones with the eight-inch baroque crucifix at the end), ready for a millennial smackdown. We're talking assault *and* battery. Not as creepy as a serial killer or disturbing as a clown, but effective just the same. Actions have consequences. The nun means business.

Beyond Chinese board fabricators, trade show list aggregators, and incomprehensible acronym-spewers, there's still more to crowd the morning spam section. Try SBA/PPP loan sharks or HR consultants who think our employees can't fill out I-9 forms or set up Covid prevention plans; or peddlers of bad virtual trade show software; or consultants who helpfully, and daily, remind us that our SAM (System for Award Management) registration is going to expire, one year before the deadline. Or consultants from the wheeling and dealing regions of our nation who are more than willing to assist selling family businesses. Or SEO specialists who have taken the time to analyze our website and pronounce it unfit for commercial consumption, but have a fourth cousin twice removed in Madras (named Mike) who will resolve the situation to the good. All for a modest fee. Payable in advance.

A commemorative postage stamp should exist honoring these scam artists. Without them, how would we spend our

continued on pg. 46

PCB Delamination Root Causes

Moisture is only one of the potential culprits.

BOB WILLIS
is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.

PCB DELAMINATION CAN be subtle or obvious. It is caused by expansion of moisture in the PCB laminate, but that may not be the root cause. Eliminating moisture often prevents the energy buildup that forces apart different layers, but this is not the complete story. Poor bonding during manufacturing of the multilayer board or some form of contamination may result in poor adhesion on innerlayers, permitting moisture to accumulate on these surfaces.

FIGURE 1 shows solder mask cracking around a through via. The PCB expanded during reflow, then contracted during cooling. This resulted in lifting and cracking of the solder mask, plus an intermittent electrical connection. **FIGURE 2** shows the innerlayer surface of the board after separation. The through vias are separated and there is no visible adhesion on this layer.

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at youtube.com/user/mrbobwillis. ▫

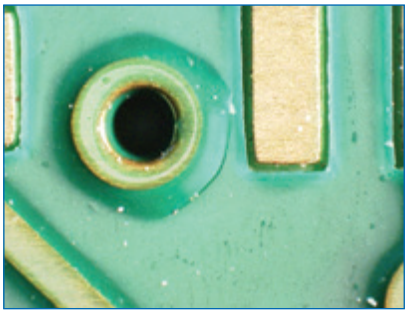

FIGURE 1. Solder mask cracking around a through via.

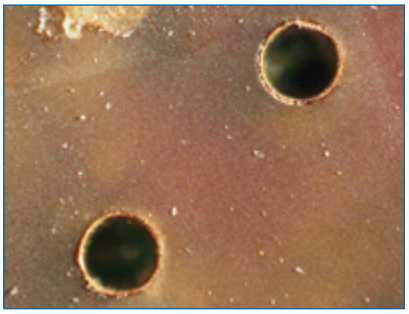

FIGURE 2. Post-separation, the innerlayer surface shows no visible adhesion.

Getting Lean, continued from pg. 41

Failure to schedule time for addressing first-article feedback. A key purpose of first-article builds is to prove out design assumptions and validate that specified assembly processes run as planned. Normally, lessons learned in that assembly process further improve manufacturability and overall processing efficiency. Incorporating those recommendations into the design typically takes less than a week if done immediately following first-article build. However, some project schedules send first articles off to agency approvals and other validations without leaving time for a quick re-spin of the design. This opens the door to the waste of waiting, since incorporating recommended changes can take many months to be reapproved through those processes. The waste of defects is also present if a decision is made to not incorporate those changes once the validation process is complete. It is much more efficient to plan for one quick optimization of the design following first-article build.

The final area with potential to generate all or some of the seven wastes is failure to adopt contract manufacturer DfX recommendations. When the seven wastes exist, both the OEM and contract manufacturer incur costs that are difficult to identify and usually aren't recoverable. A contract manufacturer's focus on the efficiencies and quality driven by Lean manufacturing is motivated by a desire to eliminate these difficult-to-identify, nonrecoverable costs. So, when a contract manufacturer recommends a change in overall design strategy, DfM or DfX, recognize that the overall benefit may result in savings far greater than the measurable cost benefit would indicate. ▫

Seeing is Believing, continued from pg. 45

mornings? That creeping arthritis from hitting the delete key 15,000 times over all these weeks and years would be just a memory.

Dear overnight email solicitation marketing genius,

What makes you think that inundating me with the same message, day after day, email after formulaic email, will sway me to place an order with you? Are you clear on the concept of alienation? Are you concerned that I'm not paying attention and, to remedy the situation, repeating the same email 467 times will close the deal?

The person who invents a device to send a countervailing electrical impulse back to the source of this AM verbal plague of yours will compete for a Nobel Prize.

Respectfully yours, etc.

If you find this article too reflective of your daily reality, and the last straw between you and spam overload, click "unsubscribe" here. ▫

In Case You Missed It

Harsh Environments

"Radiation-Hardened and Repairable Integrated Circuits Based on Carbon Nanotube Transistors with Ion Gel Gates"

Authors: Maguang Zhu, Hongshan Xiao, *et al.*

Abstract: Electronics devices that operate in outer space and nuclear reactors require radiation-hardened transistors. However, high-energy radiation can damage the channel, gate oxide and substrate of a field-effect transistor (FET), and redesigning all vulnerable parts to make them more resistant to total ionizing dose irradiation has proved challenging. Here, the authors report a radiation-hardened FET that uses semiconducting carbon nanotubes as the channel material, an ion gel as the gate, and polyimide as the substrate. The FETs exhibit a radiation tolerance of up to 15 Mrad at a dose rate of 66.7 rad s^{-1}, which is notably higher than the tolerance of silicon-based transistors (1 Mrad). The devices can also be used to make complementary metal-oxide-semiconductor (CMOS)-like inverters with similarly high tolerances. Further, the authors show that radiation-damaged FETs can be recovered by annealing at a moderate temperature of 100°C for 10 min. (*Nature Electronics,* Aug. 24, 2020, nature.com/articles/s41928-020-0465-1)

Printed Electronics

"Ambipolar Deep-Subthreshold Printed-Carbon-Nanotube Transistors for Ultralow-Voltage and Ultralow-Power Electronics"

Author: Luis Portilla, Jianwen Zhao, *et al.*

Abstract: The development of ultra-low-power and easy-to-fabricate electronics with potential for large-scale circuit integration (i.e., complementary or complementary-like) is an outstanding challenge for emerging off-the-grid applications; e.g., remote sensing, "place-and-forget," and the Internet of Things. The authors address this challenge through the development of ambipolar transistors relying on solution-processed polymer-sorted semiconducting carbon nanotube networks (sc-SWCNTNs) operating in the deep-subthreshold regime. Application of self-assembled monolayers at the active channel interface enables the fine-tuning of sc-SWCNTN transistors toward well-balanced ambipolar deep-subthreshold characteristics. The significance of these features is assessed by exploring the applicability of such transistors to complementary-like integrated circuits, with respect to which the impact of the subthreshold slope and flatband voltage on voltage and power requirements is studied experimentally and theoretically. As demonstrated with inverter and NAND gates, the ambipolar deep-subthreshold sc-SWCNTN approach enables digital circuits with complementary-like operation and characteristics including wide noise margins and ultralow operational voltages (≤0.5V), while exhibiting record-low power consumption (≤1pW/μ). Among thin-film transistor technologies with minimal material complexity, the approach achieves the lowest energy and power dissipation figures reported to date, which are compatible with and highly attractive for emerging off-the-grid applications. The approach paves the way for low-cost printed electronics that could be seamlessly embedded in everyday objects and environments. (*ASC Nano,* Oct. 13, 2020, https://pubs.acs.org/doi/10.1021/acsnano.0c06619)

Solder Materials

"Effect of Different Soldering Temperatures on the Solder Joints of Flip-Chip LED Chips"

Authors: Xinmeng Zhai, Chengyu Guan, *et al.*

Abstract: This paper investigates the effect of different soldering temperatures on the performance of the flip-chip light-emitting diode (FC-LED) filament during direct soldering. The changes in the intermetallic compound (IMC) interface, push-pull force and chip fracture surface of the chip solder joints under direct soldering temperatures of 220°, 260° and 320°C for the flip-chip LED filament were explored by scanning electron microscopy (SEM). Thereby, the optimal soldering temperature of direct joining in actual production is compared. The results show that when the soldering temperature is 260°C, Cu on the substrate begins to diffuse into the solder and react with the solder in the lower layer. The Sn content is relatively uniform, and the average push-pull force of the chip increases. The fracture occurs from inside the solder. With a soldering temperature of 260°C, it is observed that the interface shear stress of the flip-chip LED chip is the largest, and the mechanical stress and residual stress are the lowest. (*Journal of Electronic Materials,* Oct. 13, 2020, https://link.springer.com/article/10.1007/s11664-020-08517-9)

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

TIME MACHINE

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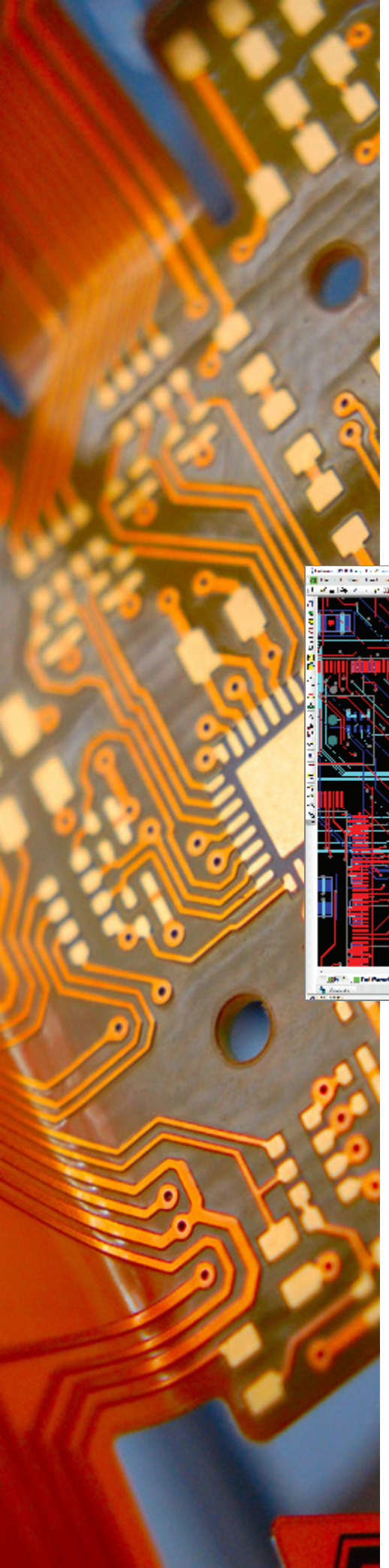
*under optimal conditions



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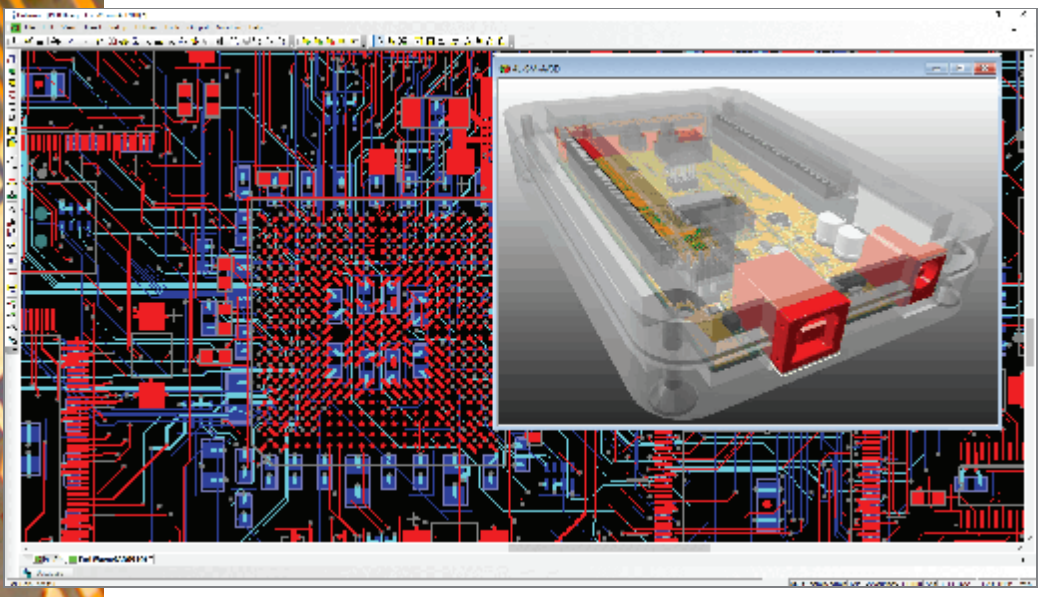

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