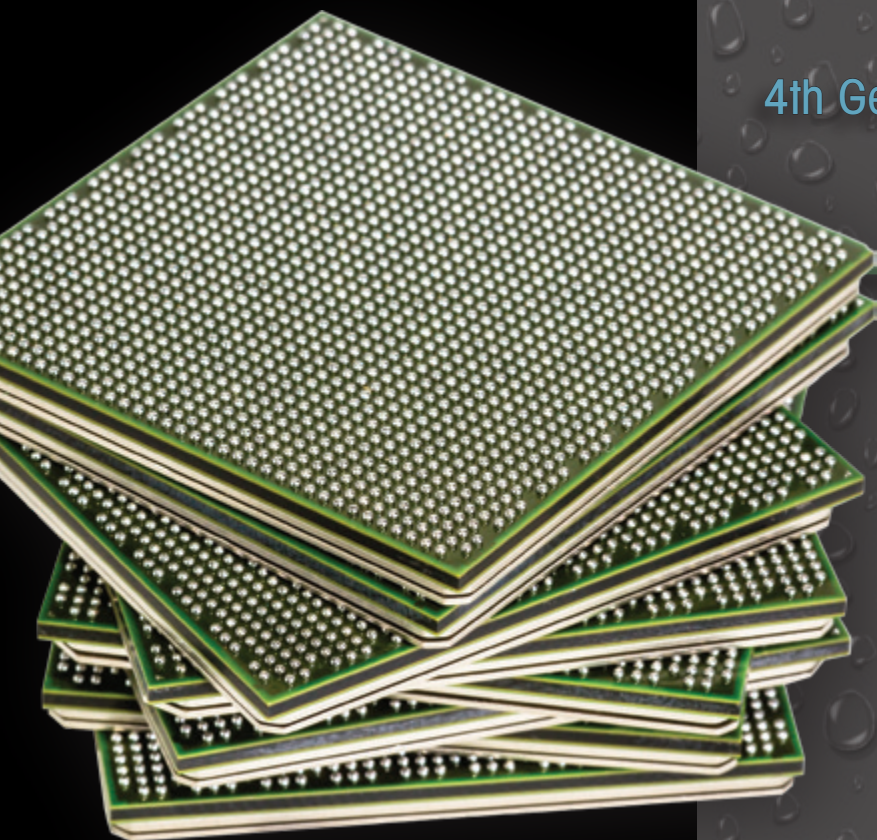


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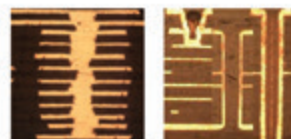


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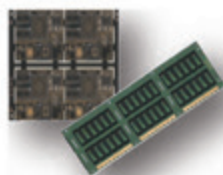
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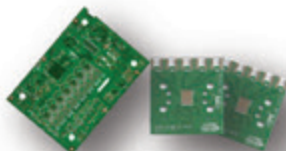
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by MORGANA RIBAS, PH.D., ANIL KUMAR, PRATHAP AUGUSTINE, PRITHA CHOUDHURY, PH.D., and SIULI SARKAR, PH.D.



## IN THE DIGITAL EDITION

## The Digital Route

Meet our leadership.

by KELLY DACK

## Retrospective

A look back at friends and colleagues who left us in 2020.

## ON PCB CHAT (pcbchat.com)

## The SMTA

with MARTIN ANSELM, PH.D.

## Electronics Data Transfer

with the IPC-2581 CONSORTIUM

## EMI Simulation Tools

with BRAD GRIFFIN

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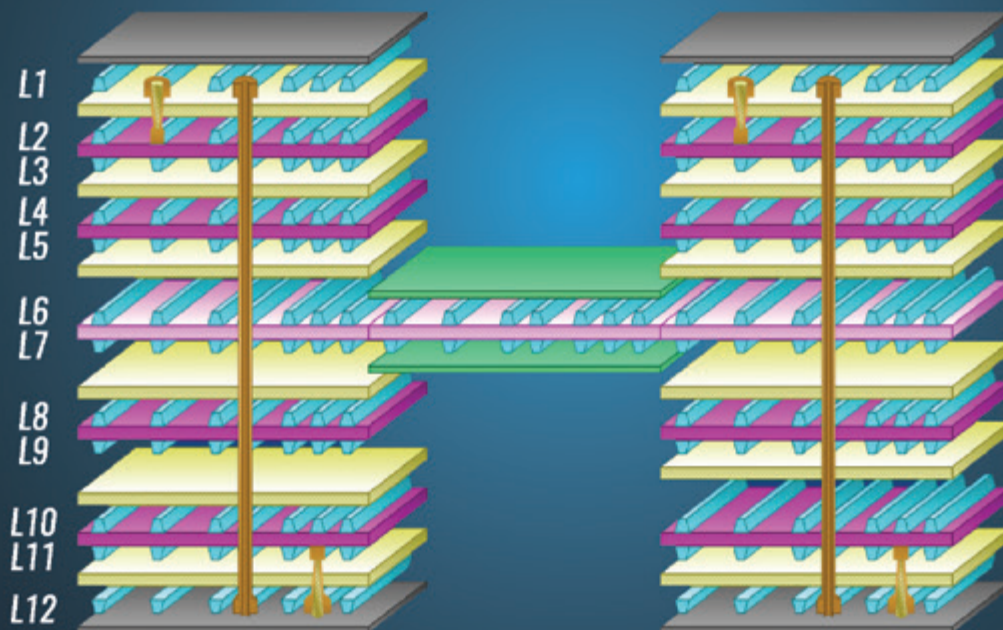


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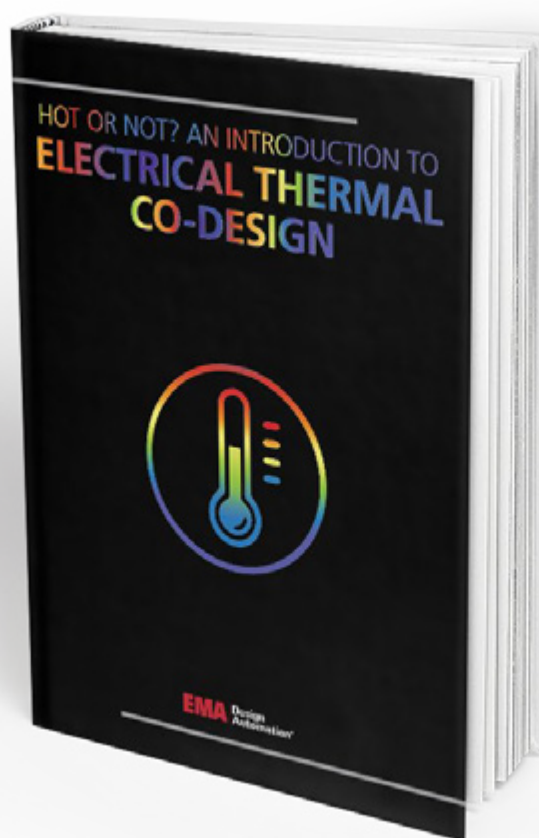
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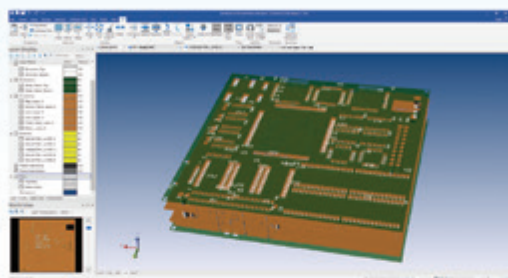
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# A New Fox in the EMS Henhouse?

**H**ON HAI, BETTER known as Foxconn, has been the largest EMS/ODM company in the world since 2005, when it catapulted Flextronics to gain the top spot. To be sure, Foxconn's revenues then and now are enhanced by ample non-electronics manufacturing segments, but the depth and breadth of the company is by any measure staggering. In calendar 2019, it reached roughly \$150 billion, a mark that is all the more impressive when you consider it doesn't include sales from some of its largest subsidiaries, such as Innolux, Sharp, and its connector and cable units. Its quarterly revenue alone would make it the largest EMS/ODM in the world. And its annual output not only eclipses all its customers' electronics sales, sans Apple, but also the next four largest competitors combined.

In pursuit of the almighty dollar, Foxconn is the almightiest. Nothing seems out of its reach. Its founder and erstwhile chairman ran for president of Taiwan. It also dabbled in American politics, putting a massive (if mostly empty) facility smack dab in the soy and corn fields of the district of the then-US House Speaker.

Never one to rest on its success, Foxconn is pushing further upstream into the semiconductor market. Having already snared Albit, three years ago it took a shot at the Toshiba memory business. And as we go to press, Foxconn is making a play for Silterra, the Malaysian maker of ICs, MEMs and sensors.

Hon Hai is on high. In mythical terms, toppling Foxconn would be like defeating Voldemort *and* Sauron. And then for good measure, maybe kicking the butt of that creepy emperor from *Star Wars*. Any company would be foolish to take that on, right?

And yet ... from China (where else?) comes an upstart that apparently doesn't believe the EMS/ODM pecking order is *set per lapis* (set in stone).

Luxshare had just been born when Foxconn ascended to the top of the EMS pyramid. It was founded in 2004, and its Xiexun Electronic manufacturing unit came along late the following year.

Like Foxconn, which got its first big break when Terry Gou convinced Michael Dell to start sourcing its plastic parts, Luxshare came about as a provider of cable assemblies and connectors. Its public offering on the Shanghai Exchange in 2010 produced nary a ripple. Yet a decade later, its annual run rate based on the past four completed quarters is nearly \$13 billion.

That's nothing to sneeze at, but why would Foxconn worry about an imitator it could gobble up in a strategic acquisition?

Two reasons. One, Luxshare has impressed the people it needs to impress. In January 2012, when Apple released its first public list of suppliers, a single

Luxshare facility was on it. Moving forward to 2007, however, Luxshare snagged a deal to build Apple's AirPods in Kunshan. Production of the wireless headphones quickly grew to account for nearly 80% of the plant's total output. As of last year, it had eight plants supplying Apple.

Luxshare's share of Apple's manufacturing is reportedly 5%, which equates to about 58% of its total revenue. That's going to rise, too. As we reported in July, Luxshare has signed a deal worth nearly \$475 million to acquire a pair of Wistron entities in China. Those plants make iPhones, giving Luxshare an added boost into the Apple supply chain.

Two, China Inc. can't be pleased that its biggest private-sector employer has been investing more readily of late in its native Taiwan, India and Vietnam. Moreover, after throwing his hat in the presidential ring, Gou publicly challenged the Communist government in China to recognize Taiwan as a sovereign country. That, coupled with Beijing's *Made in China 2025* strategic plan, could be more than enough to push the weight of the world's second-largest economy behind Luxshare.

Foxconn reportedly is concerned, enough so that, per Reuters, it convened a task force to study the upstart competitor, a move launched by none other than Gou himself. Among the questions: Is China's government supporting Luxshare?

Luxshare's growth has been fueled by acquiring suppliers to Apple. Is Foxconn about to be outfoxed? We are about to find out.

mbuetow@upmediagroup.com  
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P.S. As we come to the end of this most trying year, we thank our readers and customers for your ongoing support, and wish you all a healthy, prosperous 2021.





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## PCDF People



Dyconex promoted **Dr. Jonas Kottman** to vice president operations. He joined the fabricator last year as manager operational excellence.

The FED trade group awarded the PCB Design Award to **Thomas Blasko** (CiBoard Electronic), **Georg Scheuermann** (TQ-Systems) and **Michael Matthes** (Wittenstein Cyber Motor).



GoPro named **John Burkert Jr.** senior PCB layout engineer. He has more than 30 years' experience in PCB design with Velodyne, Google, Qualcomm and others.

Jacobs Technology named **Russ Pringle** printed circuit board designer.

L3Harris Technologies named **Cameron Stouder** ECAD tools and library team lead.



Lone Star Circuits promoted **Lance Riley** to chief operating officer. He has been with Lone Star since 2017, and previously held engineering and sales executive roles with TTM and

Unicircuit.

## PCDF Briefs

**Apple** is expected to accelerate the adoption of LCP (liquid crystal polymer)-based flexible PCBs for the antenna modules to be used by its future iPhone lineup supporting 5G mmWave technology, according to industry sources.

**Cicor** expanded production capacity at its Wangs, Switzerland, fabrication site.

**Exception PCB** purchased a **Ucamco** Ledia direct imager.

**Gerber Labs**, an Orange County-based engineering startup, is rolling out a platform that makes custom PCBs accessible to electrical engineering students, hobbyists and small businesses.

**Hitachi Chemical**, a longtime leader in the development of electronic materials, changed its name to **Showa Denko Materials**, reflecting the latter's acquisition of the venerable Japanese firm.

**ILFA** has acquired circuit board distributor **Skytech Europe** for an undisclosed sum.

**Insulectro** rolled out an online shopping center for conductive inks and pastes plus advanced substrates and films.

**Koh Young** joined the IPC-DPMX (IPC-2581) Consortium.

## California Startup Says It Has Answer to High-Density, Ultra-Thin Designs

**SAN FRANCISCO** – “Innovation starts at the bottom,” a San Francisco startup says, underpinning its belief printed circuit boards will drive the next big leap in innovation.

Thintronics, the new firm founded last year by chemist Dr. Stefan Pastine, wants to help companies make better products through “reconceptualizing PCB design.”

The materials company has ideas for lower layer count designs for devices that must be small or lightweight or both, such as mobile, IoT, wearables and autonomous systems for self-driving cars and LiDAR or drones.

Its hypothesis is companies capable of using the PCB to drive end-product innovation are few and far between, but superior materials will help design engineers shed design rule constraints, while manufacturers benefit from shorter processing cycle times.

Its solution? A novel thin, low dielectric constant, skew-free substrate. In this case, how thin is “thin?” The company defines it as a 1.0-mil thick dielectric for standard products and 0.5 mils for “ultra” thin.

According to Thintronics, the novel material can enable product designers to cut board thickness and layer counts in half without a loss in interconnect density, or reduce PCB thickness by 35% with no layer count penalty, while doubling interconnect density.

The company's claims are eye-opening: a 75% reduction in lamination cycle times and a 60% reduction in post-processing times, the latter because the Thintronics material cuts desmear times and requires no plasma. The dielectric constant range is 3.0-3.1, and the impedance tolerance is 5%. Moreover, Thintronics touts the “unlimited” prepreg shelf life. The dielectric spacing is 1 mil or 0.5 mils, and the material is CAF-resistant.

“Thintronics was created not by tweaking existing PCB materials, but by inventing new materials, starting from the molecular level. Our bottom-up molecular design approach creates products that, at their molecular core, are vastly different than any material in the world, much less the dielectrics used in the PCB market today,” the firm explains on its website.

Pastine comes to the PCB industry by way of Connora, a designer of thermoset plastics and composites that have the added feature of low-energy recyclability. Connora, which Pastine cofounded in 2011, was acquired by Aditya Birla Chemicals in 2019, freeing up Pastine to embark on his current pursuit.

As of November, longtime materials executive Tarun Amla has joined as president and chief operating officer. Amla was previously CTO at ITEQ and has held top technology jobs at Shengyi and Isola as well.

“We share the same view that it is sad that the USA has let its grip on dielectric technology slip away,” Pastine said in a LinkedIn post announcing Amla's arrival. “We both expect to reverse the trend *vis-à-vis* the coupling of advanced simulation with Thintronics' bottom-up, molecular-level design approach to inventing new dielectric materials.” (MB)

## Electronic Design Tool 'Morphs' Interactive Objects

We've come a long way since the first 3-D-printed item came to us by way of an eye wash cup, to now being able to rapidly fabricate things like car parts, musical instruments, and even biological tissues and organoids.

While much of these objects can be freely designed and quickly made, the addition of electronics to embed things like sensors, chips, and tags usually requires that you design both separately, making it difficult to create items where the added functions are easily integrated with the form.

Now, a 3-D design environment from MIT's Computer Science and Artificial





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**Meltex** is building a new fab plant in Japan and increasing production capacity in Thailand, according to reports.

The **Redfern Companies** will acquire **Automated Chemical Solutions**, a provider of specialty chemicals for PCBs.

**Soochow University** researchers have developed a new approach to printed electronics whereby ultra-low-power electronic devices could recharge from ambient light or radio frequency noise. The approach paves the way for low-cost printed electronics that could be seamlessly embedded in everyday objects and environments.

Smartphone OEMs are extending fully integrated modem-RF system designs to support 5G and LTE implementations over their flagship devices, a new teardown analysis from **System Plus Consulting** says.

**Unimicron Technology's** PCB fabrication plant in Taoyuan, Taipei, sustained a fire that sent at least 10 persons to the hospital.

A section of the US Senate's latest NDAA bill requires US companies to stop using PCBs made in China, Iran, North Korea and Russia by fiscal 2033.

## CA People

Circuit Works named **Luis Gallegos** manufacturing engineer manager.

Creative Electron named **Courtney Kalb** client specialist.



Electrolube appointed **Carolyn McAllister** European sales manager. She has a degree in chemistry from the University of Nottingham, and spent the past six years with the company's research and development team.

Nortech Systems named **Christopher D. Jones** chief financial officer and senior vice president of finance.

STI Electronics announced **Emery "Graham" Goff**, a student at Calhoun Community College, as recipient of the 2020/2021 Jim D. Raby Scholarship.



Z-Axis promoted **David Figler** to purchasing manager. He joined the purchasing team in 2019, and has more than 20 years' experience in electronics purchasing and commodity management with Caldwell Manufacturing Company, Alstom, ITT Gould Pumps and Pfaunder.

Zollner promoted **Erick Fabian** to supply chain designer.

Intelligence Laboratory (CSAIL) lets users iterate an object's shape and electronic function in one cohesive space, to add existing sensors to early-stage prototypes.

The team tested the system, called MorphSensor, by modeling an N95 mask with a humidity sensor, a temperature-sensing ring, and glasses that monitor light absorption to protect eye health.

MorphSensor automatically converts electronic designs into 3-D models, and then lets users iterate on the geometry and manipulate active sensing parts. This might look like a 2-D image of a pair of AirPods and a sensor template, where a person could edit the design until the sensor is embedded, printed, and taped onto the item.

To test the effectiveness of MorphSensor, the researchers created an evaluation based on standard industrial assembly and testing procedures. The data showed that MorphSensor could match the off-the-shelf sensor modules with small error margins for both the analog and digital sensors.

"MorphSensor fits into my long-term vision of something called 'rapid function prototyping,' with the objective to create interactive objects where the functions are directly integrated with the form and fabricated in one go, even for non-expert users," says CSAIL PhD student Junyi Zhu, lead author on a new paper about the project. "This offers the promise that, when prototyping, the object form could follow its designated function, and the function could adapt to its physical form."

**MorphSensor in action.** Imagine being able to have your own design lab where, instead of needing to buy new items, you could cost-effectively update your own items using a single system for both design and hardware.

For example, let's say you want to update your face mask to monitor surrounding air quality. Using MorphSensor, users would first design or import the 3D face mask model and sensor modules from either MorphSensor's database or online open-sourced files. The system would then generate a 3D model with individual electronic components (with airwires connected between them) and color-coding to highlight the active sensing components.

Designers can then drag and drop the electronic components directly onto the face mask, and rotate them based on design needs. As a final step, users draw physical wires onto the design where they want them to appear, using the system's guidance to connect the circuit.

Once satisfied with the design, the "morphed sensor" can be rapidly fabricated using an inkjet printer and conductive tape, so it can be adhered to the object. Users can also outsource the design to a professional fabrication house.

To test their system, the team iterated on EarPods for sleep tracking, which only took 45 minutes to design and fabricate. They also updated a "weather-aware" ring to provide weather advice, by integrating a temperature sensor with the ring geometry. In addition, they manipulated an N95 mask to monitor its substrate contamination, enabling it to alert its user when the mask needs to be replaced.

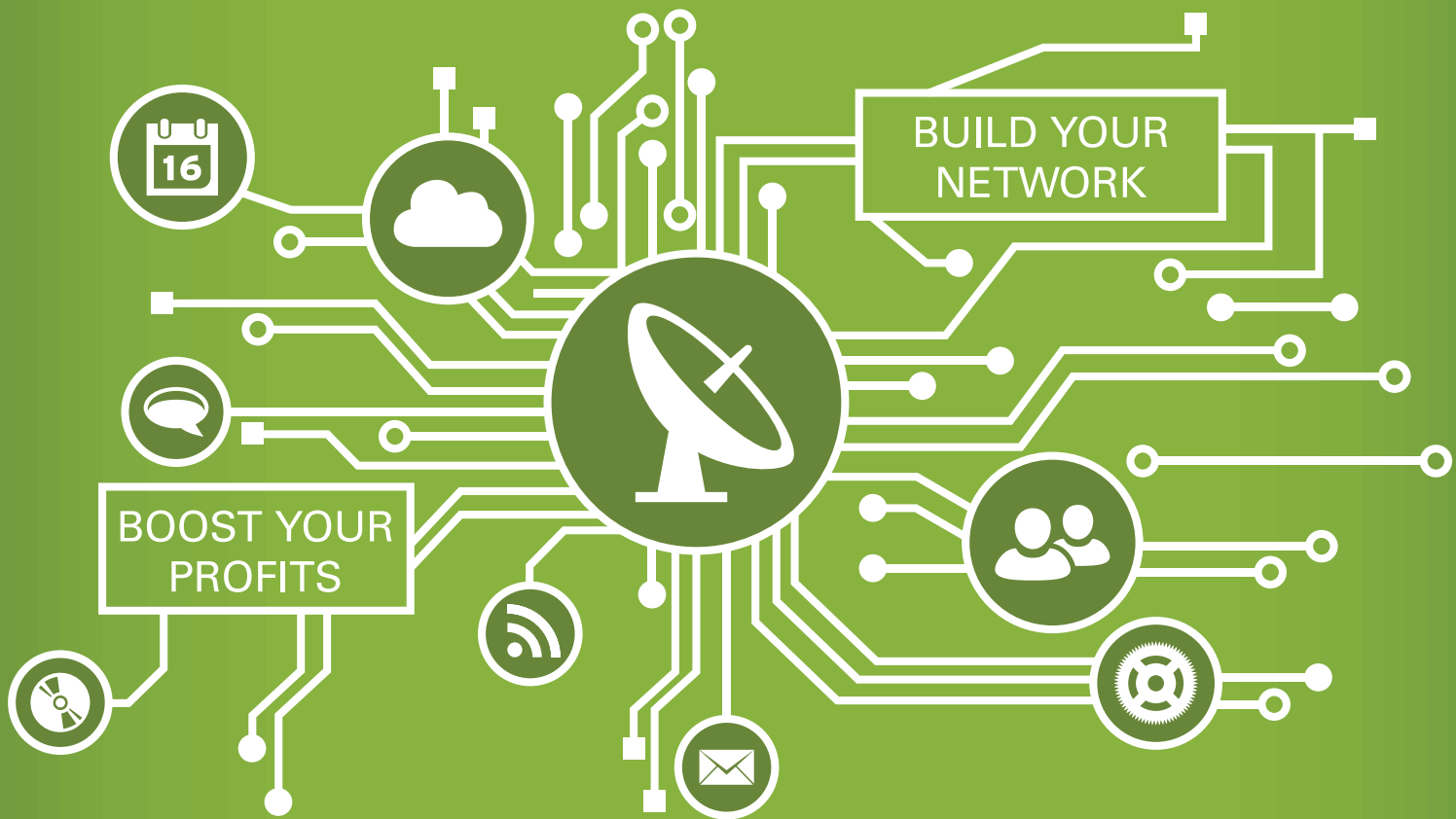
In its current form, MorphSensor helps designers maintain connectivity of the circuit at all times, by highlighting which components contribute to the actual sensing. However, the team notes it would be beneficial to expand this set of support tools



An MIT team used MorphSensor to design multiple applications, including a pair of glasses that monitor light absorption to protect eye health.



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## CA Briefs

**ABAJ Group** is setting up a TV and AC manufacturing facility near Mehsana, India.

**AIM Solder** opened a 12,000 sq. ft. ISO 9001-certified solder manufacturing facility in Malaysia.

**Aimtron** purchased an **Austin American Technology** X30 stencil cleaner, its second.

**Apple** has reportedly suspended new business with **Pegatron** after discovering labor violations at a student workers' program.

In the two months since **Huawei** lost access to American technology, Japanese makers of electronic parts have enjoyed a fresh wave of orders from other smartphone manufacturers seeking to claim market share now up for grabs.

**CalcuQuote** has partnered with **Rochester Electronics** to build a new integration that offers up-to-date information through the CalcuQuote platform.

**Cogiscan** named **AES** to handle sales and service throughout Vietnam.

**Compal Electronics** has been increasingly requested by its clients to diversify manufacturing bases beyond China, particularly for smart devices, according to a company executive.

**Compal Electronics** and **Cisco** have partnered to work in the 5G AIoT market and provide integrated network solutions.

**Computrol** installed a **Thermaltronics** TMT-R9800S solder robot.

**Creative Electron** has been awarded a US patent for AI-powered programming of x-ray inspection systems.

**East/West Manufacturing** will invest more than \$5 million toward a new electronics manufacturing facility in Round Rock, TX, with plans to be open by next August.

**Elisa Oyj** made a strategic investment to hold a majority stake in **CalcuQuote**.

**FoundPac Group** is considering spinning off its laser stencil unit, **Dynamic Stencil**, and is looking at IPO possibilities.

**Foxconn** dismissed media reports suggesting a souring relationship between the ODM and **Apple** as "nonsense" and vowed legal action. It reportedly formed a task force to fend off competition from **Luxshare**, which is targeting Apple as a key customer.

**Foxconn** chairman Liu Young-way said the company hopes to take 10% of global market share for electric vehicles between 2025-27, and that it has been in talks with multiple carmakers for future cooperation.

even further, where future versions could potentially merge electrical logic of multiple sensor modules together to eliminate redundant components and circuits and save space (or preserve the object form).

Zhu wrote the paper alongside MIT graduate student Yunyi Zhu; undergraduates Jiaming Cui, Leon Cheng, Jackson Snowden, and Mark Chounlakone; postdoc Michael Wessely; and Professor Stefanie Mueller.

This material is based upon work supported by the National Science Foundation. (By Rachel Gordon. This article was first published in MIT News and is republished here with permission of Rachel Gordon and MIT.)

## Victory Giant Technology Plans Second 'Smart' PCB Plant

**SHANGHAI** – Victory Giant Technology will begin work on a new smart manufacturing factory here in the first quarter 2021, the printed circuit fabricator's second such facility.

The new plant is expected to be operational by the second quarter 2022.

The plant is a larger version of VGT's high-volume Industry 4.0 factory, which opened last year. The site relies on AGVs and other automation, plus VGT developed intelligent ERP software and real-time product metrology to reduce labor and shorten production cycle time. (MB)

## Ticer to Buy Materion LAC Assets, Head Off Supply Break

**CHANDLER, AZ** – Ticer Technologies announced an agreement to acquire certain manufacturing assets from Materion's Large Area Coatings division, effective Jan. 1.

The deal will help Ticer avoid a potential supply disruption, the company said.

The companies did not disclose financial terms.

Ticer, which makes thin film embedded resistor foils, will acquire LAC's vacuum deposition/sputtering production equipment, which will remain at the firm's facility in Windsor, CT, as well as certain staff. Processes, equipment and raw materials will remain the same during the transition process, the companies said.

"This is a significant improvement in capacity and supply leadership long sought by Ticer," said David Burgess, president, Ticer. "We believe our global customers will benefit from the flexibility and supply chain control afforded by this change."

Ticer had previously announced a potential supply chain disruption due to the planned divestiture of Materion's LAC division. The acquisition will obviate that potential disruption and make product requalification unnecessary. (MB)

## BAE Breaks Ground on Massive Electronics Factory

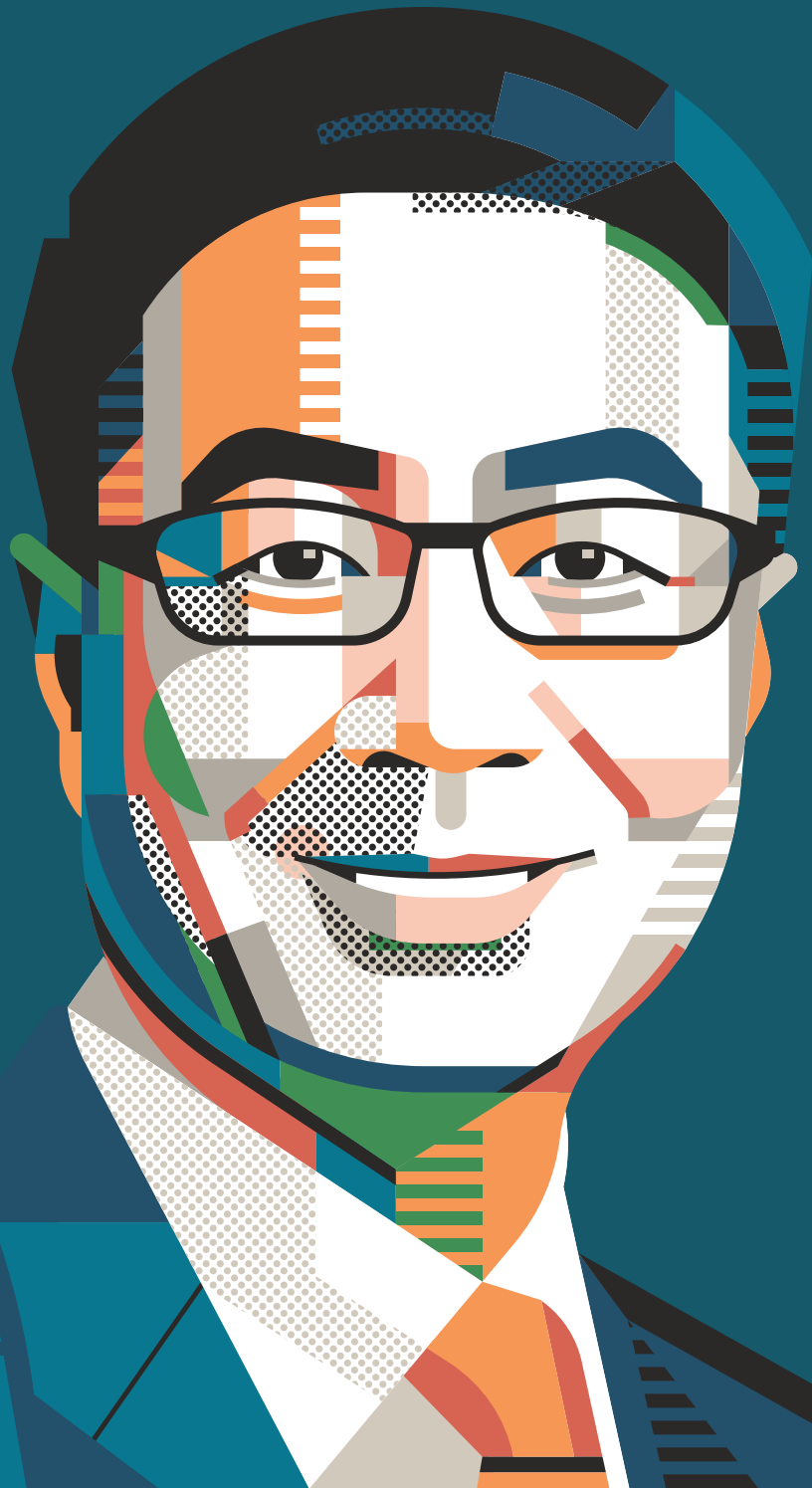
**CEDAR RAPIDS, IA** – BAE Systems is investing more than \$100 million to build a state-of-the-art manufacturing and R&D facility here. The center includes a 278,000 sq. ft. factory and research and development center located on a 32-acre site in Cedar Rapids.

Besides the large factory, the site will include several hundred offices, workstations, and flexible workspaces, and classified and unclassified labs. The building was designed for growth, with the ability to add 50,000 sq. ft. of additional space in the future.

The facility will support the company's newly acquired Navigation & Sensor Systems business, which makes mission-critical military GPS products. The new building will bring the company's local design and production employees from multiple locations into a single center of excellence with modern manufacturing, engineering, and office space.



Wenge Yang  
Vice President, Marketing  
Entegris



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**Foxconn** said its commitment to Wisconsin has not wavered, and it will continue to work with the local government to create new jobs and attract new investment to the state.

**Incap Electronics Estonia** opened a new SMT production line in its factory in Kuresaare.

**Indium** and **RENEX** have formed a strategic partnership for the service of PCB and engineered solder materials in Poland.

**Intellitronix** installed a **Europlacer** iineo+ pick-and-place machine.

**Kyzen** named **Solder Connection** to sell and support its cleaning products in Ireland.

**LeddarTech** announced a collaborative project agreement with **Flex** for the development of a LiDAR evaluation kit and related service.

**NASA** has selected **Nokia** to build the first cellular network on the moon.

**Niche Electronics** and **QCMS** have selected **MIRTEC's** MV-6 OMNI 3D AOI.

After being defunct for six years, a former **Nokia** factory in Sriperumbudur, India, came to life as electronics manufacturer **Salcomp** launched commercial operations from the plant.

**Nordson Dage** named **Murray Percival** representative of its Assure Series of x-ray component counters in the Midwest US.

**OnePlus** will allocate up to Rs 100 crores (\$14 million) in new phone and TV manufacturing sites and other expansion in India.

**Ryder Industries** is increasing its electronics manufacturing services capacity by investing in two new facilities in Taiwan.

**Square E** is shutting its EMS plant outside Louisville, closing the book on an operation that lasted more than 40 years.

**Syrma Technology** merged with **SGS Teknics** in a cash and stock deal of Indian EMS companies.

**University of Washington** engineers have created simple plastic devices without batteries or semiconductors that can wirelessly interact with smartphones and computers.

A **Wistron** subsidiary announced it will spend \$28.7 million to acquire a plant from **Western Digital** in Malaysia.

The facility will improve operational efficiency, optimize production, and enhance the company's ability to deliver high-quality military GPS products to the warfighter. Construction began in October and is expected to finish in 2022.

"Our world-class military GPS business is built on the rich talent pool in Greater Cedar Rapids," said John Watkins, vice president and general manager of Precision Strike & Sensing Solutions, BAE Systems. "This investment will provide our high-tech engineering and manufacturing experts with a world-class workspace and the tools to enhance operational excellence." (MB)



## New Study Lays Groundwork for US Semi Fab Resurgence

**WASHINGTON** – A new report finds the US government has a strategic opportunity to reverse the decades-long trajectory of declining chip manufacturing in America, strengthen national security, make domestic supply chains more resilient, and make the country one of the most attractive places in the world to produce semiconductors.

The report, issued in September by the Semiconductor Industry Association and the Boston Consulting Group, says the US share of the global semiconductor fabrication industry has dropped to 12%, from 37% in 1990. Moreover, just 6% of new capacity is earmarked for the US, the authors say. In contrast, China will add nearly 40% of new capacity, making it the largest semiconductor manufacturer in the world.

The US is slowed by the high cost of fabs, which is about 30% higher over a 10-year period than key sites in Southeast Asia, and 37% to 50% higher than China. Much of the difference – up to 70% – is due to government subsidies and incentives that gravitate manufacturers to the Pacific Rim.

Nonetheless, the US could grab back up to twice its current share through a series of targeted government incentives, the authors assert. Such a strategy would ensure supply for critical end-markets such as aerospace and defense and increase employment in the sector by 70,000, while providing a boost to political issues such as trade balances. The report says the right combination of incentives could generate 19 new fabs, each staffed with 3,000 to 6,000 workers.

Ironically, the study shows the US holds dominant positions in EDA software, core IP and manufacturing equipment. Its share of the materials and manufacturing sectors, however, is roughly 12% each, and it lacks the leading-edge capabilities of Taiwan (TSMC) and South Korea (Samsung). As fabless models have taken hold, the US now lags every major chip-producing market, including Japan and Europe. (Intel's plans to sell its manufacturing plants, announced after the report was released, will only accelerate this trend.)

The authors assert government investment of \$20 billion to \$50 billion would lead to the addition of 14 to 19 new fabs in the US, at the peak making it the top site for new plants outside China. Such a move would boost the US share of the world market to 14% by 2030, versus 10% if there were no changes to the status quo. (MB)

## METALS INDEX



## COMPUTERS BOOT UP

Trends in the US electronics equipment market (shipments only)	% CHANGE			
	JUL.	AUG.	SEP.	YTD%
Computers and electronics products	4.1	0.5	1.2	2.9
Computers	-2.8	-0.7	3.3	-10.1
Storage devices	2.9	-1.3	-7.4	34.5
Other peripheral equipment	23.7	3.0	-9.2	8.6
Nondefense communications equipment	9.2	1.7	2.8	9.4
Defense communications equipment	-3.8	6.2	-5.1	4.0
A/V equipment	10.7	-3.0	2.8	-9.3
Components <sup>1</sup>	4.5	0.7	-0.7	9.5
Nondefense search and navigation equipment	1.2	-0.8	-1.1	-5.9
Defense search and navigation equipment	1.7	-3.2	2.6	2.5
Medical, measurement and control	1.2	2.8	0.5	-1.9

<sup>1</sup>Revised. <sup>2</sup>Preliminary. <sup>3</sup>Includes semiconductors. Seasonally adjusted.  
Source: U.S. Department of Commerce Census Bureau, Nov. 3, 2020

## US MANUFACTURING INDICES

	JUN.	JUL.	AUG.	SEP.	OCT.
PMI	52.6	54.2	56.0	55.4	59.3
New orders	56.4	61.5	67.6	60.2	67.9
Production	57.3	62.1	63.3	61.0	63.0
Inventories	50.5	47.0	44.4	47.1	51.9
Customer inventories	44.6	41.6	38.1	37.9	36.7
Backlogs	45.3	51.8	54.6	55.2	55.7

Source: Institute for Supply Management, Nov. 1, 2020

## KEY COMPONENTS

	MAY	JUN.	JUL.	AUG.	SEP.
Semiconductor equipment billings <sup>1</sup>	13.5%	14.4%	26.7%	32.5% <sup>r</sup>	40.3% <sup>p</sup>
Semiconductors <sup>2</sup>	4.82%	4.9%	4.23%	4.94% <sup>r</sup>	5.79% <sup>p</sup>
PCBs <sup>3</sup> (North America)	1.10	1.12	1.00	0.94	0.93
Computers/electronic products <sup>4</sup>	5.44	5.44	5.28	5.22 <sup>r</sup>	5.18 <sup>p</sup>

Sources: <sup>1</sup>SEMI, <sup>2</sup>SIA (3-month moving average growth), <sup>3</sup>IPC, <sup>4</sup>Census Bureau, <sup>p</sup>preliminary, <sup>r</sup>revised

## Hot Takes

- Taiwan's PCB industry output in 2021 is expected to grow 2-3% to NT\$690 billion (US\$24 billion) because of 5G. (TPCA)
- Worldwide silicon wafer area shipments rose 6.9% year-over-year but were down 0.5% sequentially to 3,135 million sq. in. in the third quarter. (SEMI)
- Global tablet shipments rose 24.9% year-over-year to 47.6 million units in the third quarter. (IDC)
- Worldwide smartphone market shipments declined 1.3% year-over-year in the third quarter. (IDC)
- Global notebook shipments are forecast to rise at a CAGR of 0.9% from 2020 to 2025. (Digitimes Research)
- Singapore's factory output expanded 24.2% year-on-year in September on growth in semiconductor production. (Economic Development Board)
- Tin use contracted 5.4% in 2019 to 359,200 tonnes and is expected to decline a further 5.9% in 2020 because of the Covid-19 pandemic. (ITA)
- The AR headset market will grow to over \$20 billion by 2030. (IDTechEx)
- Global shipments of PCs (desktops, notebooks, and workstations) rose 14.6% year-over-year to 81.3 million units in the third quarter. (IDC)
- PC memory chip and device supplies are falling short of demand, with the tight supply unlikely to ease until the first quarter 2021. (DigiTimes)
- Companies are rushing to use AI, but few see a payoff, with only 11% reaping a "sizable" return on their investments. (Boston College)



# Preparing Your Company for Disaster

Businesses can't plan for everything, but with the right prep they can adapt.

**DECEMBER IS FINALLY** here. Mercy knows it seems to have taken forever to bring this most unusual year to a close. I keep pondering the question customers inevitably ask during a supplier audit: What contingencies are in place for “unforeseen and unthinkable” disasters and events? If anyone had asked me a couple years ago to come up with a plan to deal with a global pandemic I would have thought them to be crazy for asking. And yet, that was 2020!

The one takeaway from this crazy year is you can never plan for everything. Paradoxically, good planning makes it easier to deal with the unimaginable.

Business planning takes numerous forms. Most people think first of the financial budget planning, usually led by finance and account staffs. Visions of building a budget, whether bottom-up or top-down, as a tool to measure specific activities against comes to mind. This type of planning revolves around predicting core operating activities that are repeatable, predictable and highly measureable. While important, if not essential, for the operations folk to run the “business as usual,” that budget is only one aspect of planning.

Capital planning is the kissing cousin to financial budgeting. The one major difference is that planning for the acquisition of capital assets, facilities upgrades, or working capital needs more of a “what if?” in the equation. Multiple scenarios must be taken into consideration to hedge both the best- and worst-case scenarios. Such planning incorporates potential risks and focuses on what “could” occur, rather than what is “expected” to take place.

Contingency planning is a horse of a different color. While the event, situation, occurrence(s) and magnitude of the contingency being planned for may differ, the common trait is the events are major distractions, all unprecedented and usually quite unimaginable. One cannot do this type of planning alone, and this type of planning may seem a waste of time, as the contingency most likely will never occur.

For many, navigating and surviving the unimaginable (and most likely unplanned for) global pandemic was, in part, accomplished because the organization performed *some* kind of contingency planning and was able to leverage pieces of those plans to adapt to the situation at hand. Plans for any extreme disaster or crisis share several basic elements.

*Flexibility* is critical for everyone, especially the leadership team. An unprecedented event requires all involved to be flexible, adaptable and ready to shift gears on-the-fly to manage the crisis. Flexibility of one's mind, let alone an entire organization, doesn't

just happen. Leadership needs to plan for how it will adapt and enable a department, division or company to move in different directions if needed.

*Cross-trained staff* is one of the best ways to enable flexibility. Even those in very specialized roles or the most mundane jobs need to move around the organization periodically so they are exposed to other aspects of the process and see tasks they may be able to handle if and when necessary. A cross-trained staff does not happen organically. It takes planning and advanced training to have employees who can move in and out of different situations and tasks smoothly and effectively.

*Rapid deployment* is critical when dealing with a crisis. Leadership needs to quickly deploy people, ideas, contingency plans, and resources to deal with a given situation. Times like these have no set script. Management needs to utilize the best-available information from wherever it is offered to move decisively and rapidly. Waiting for perfect information, or analysis paralysis, is a surefire way to lose precious time, often the most precious resource.

*Communication* is the most important element, one that makes the difference between a successful attack plan and workers flailing unproductively. Communication is two-way. It is essential that all involved understand the strategy, deployment plan, risk, and basis of information used to make decisions. There is nothing wrong communicating that everyone is working in an unprecedented situation. Equally, it is imperative to listen and take what is reported by those in the line of action forward to the appropriate person(s), so *all* information is taken into consideration. A solid communication environment does not just happen: It is planned for and understood by all.

*Patience* is needed by all and, most important, must be exercised and demonstrated by everyone in the leadership team. While everyone reacts differently, plan on how those in charge will mutually support and demonstrate as much patience as possible while dealing with the challenge so employees don't panic.

Finally, have adequate financial reserves available to tap, if needed. All in charge should know if and when those resources are deployed, so they can be focused on the most critical areas of need.

No organization can plan for and be prepared for every possible event. Moreover, trying to plan for every permutation and combination is not the best utilization of resources. A management team and corporate culture that has the critical elements needed to prepare and respond may make the critical difference when an unimaginable event strikes. □

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# Opportunity Knocks at the Doors of Continuous Learners

Why you should consider a certification program.

**WHEN I LOOK** back on my career and consider the key ingredient to my success, I'd say whenever opportunity knocked, I had the right skill set to walk through the door. I was fortunate that my first electronics manufacturing services (EMS) employer had both a tuition refund program that paid for my master's degree in management and an internal management training program. That started me on a path of continuous learning that included multiple certification programs and other training programs. And, as advancement opportunities came up, I had the right qualifications and a results-focused track record.

Company-sponsored educational resources are more limited today. That said, technology has made it possible and convenient to engage in focused continuous learning opportunities. IPC's Certified Electronics Program Manager (CEPM) training and certification program is a good example. What once required multiple trips to training locations and a solid week of classroom time can now be done via computer either in live sessions or through reviews of class recordings. The program was redesigned to an online format in 2017 and now is a six-week program with two two-hour classes per week, providing overviews of program management, sales, cost accounting, materials management, contracts, production planning, quality and leadership. Students are assigned to teams that complete a case study each week related to the concepts presented. A variety of online exercises reinforce key concepts. The goal is to ensure participants are provided a common framework of knowledge and the opportunity to interact with peers to discuss best practices. Information on the program and upcoming dates is available here: <https://www.ipc.org/content-page.aspx?pageid=cepm>.

If you have a degree, why consider a certification program? The reality is many educational disciplines have only a peripheral relationship to the job functions performed. Employees learn on the job, and the result may be gaps in knowledge. A certification program lays out a formal framework of knowledge related to a specific discipline. It helps those who have learned on the job fill knowledge gaps. Another benefit of certification programs is students are usually working in their fields. The knowledge shared in class discussions tends to be hands-on and relevant to each student's current job. A byproduct is often better focus on skills improvement areas or stronger focus on incorporating best practices at work.

Most EMS salespeople and program managers don't have a degree that specifically relates to those

functions. Most have a technical/engineering or business background. In some cases, this may be the first manufacturing-related job an individual has held. The result is sales and program managers are often strong on either the technical or business side of the equation, but not both. IPC's CEPM program is designed to help participants develop balance in business and technical knowledge. There is strong emphasis on setting customer expectations, building a business case, understanding contracts and cost accounting. There is equal emphasis on materials management considerations, production planning and the production process. A leadership section focuses on team motivation and management skills.

CEPM's team aspect is also beneficial. The EMS environment can be stress-filled, which workers may believe is specific to their company. As teams work together on case studies, they typically find the challenges they encounter in their jobs are universal. They also learn there is often more than one "right" way to do things, enhancing the options available to resolve challenges or do their jobs better. Since the program is open to OEM and EMS participants, team activities and class discussion often build a better understanding on both sides about challenges inherent in the outsourcing process.

The focus on building a business case also has benefits. Often the reason a customer says no is because the reason for the request is not adequately explained. Inexperience in the industry or gaps in relevant knowledge are often the root cause of failure to build a business case. The CEPM training focuses on examples of typical business cases used to justify requests related to price changes, DfM recommendation implementation, inactive/obsolete inventory resolution and other common program issues. Combined with a better understanding of common cost drivers and how EMS processes interrelate, this makes it easier to discuss the business case for a change in customer behavior.

The CEPM program is not IPC's only online offering in the EMS management realm. This year they've rolled out a negotiation class, and other classes will follow. First quarter dates for CEPM and negotiation class should be added to the IPC website soon.

Regardless of the training opportunity, consider starting 2021 with a commitment to increase your skills base. Opportunity knocks regularly at the doors of continuous learners. □

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# Taming Electromagnetic Interference on a PCB

What's all this noise? Look beyond the wires and connectors to think inside the box.

**YOU CAN'T ALWAYS** hear it, feel it or see it, but every active electronic device radiates some kind of energy as it operates. For the most part, that's the point. We want to hear the music; we want to feel the air conditioning or see the light. Those are the good things.

Meanwhile, we don't want side effects: static on the radio, compressor noise from the AC or that annoying 60Hz hum from the light fixture bleeding over to my new bass amp. It's these things we try our best to design out of the products we build.

We can adjust the tuner on the radio, and we can install the central AC unit away from the windows. I ordered a noise suppressor and plugged it into a socket where there's no dimmer switches or high current motors plugged in. Then the amplifier and pedal board power cords were routed into the special apparatus, and I no longer get a wave of white noise when this MacBook Pro searches for a WiFi signal.

Even if the emissions cannot be perceived with our five senses, they can be detrimental to the performance of the circuit or spill out onto other nearby electronics. We use metal for the device housings for multiple reasons. Beyond its heat-shedding property, we want to keep the noise inside the box while preventing other noise from getting in. Those are the two central tenets of coexistence.

If you want to chain a bunch of gain-stages together, it helps to start with clean power and a common ground path. The fix for noise issues is almost always additive. The new schematic you get just before the prototype goes for FCC certification usually has a new ferrite bead, maybe a diode here and there and some retuned bypass capacitor values.

Generally speaking, a few factors cause signal degradation. One of the main factors is long traces. The farther a signal travels, the more likely it will end up near a bad neighbor. In this case, "bad" can mean noisy or susceptible to picking up noise. I'm tempted to open up that big, white plastic wall-wart for this laptop to see if it has any shielding.

Getting the dirt out of the wall juice is the first line of defense. At the PCB level, the second line of defense is to shield the most vulnerable victim traces from exposure to the outside world. EMI shielding is carried out around the

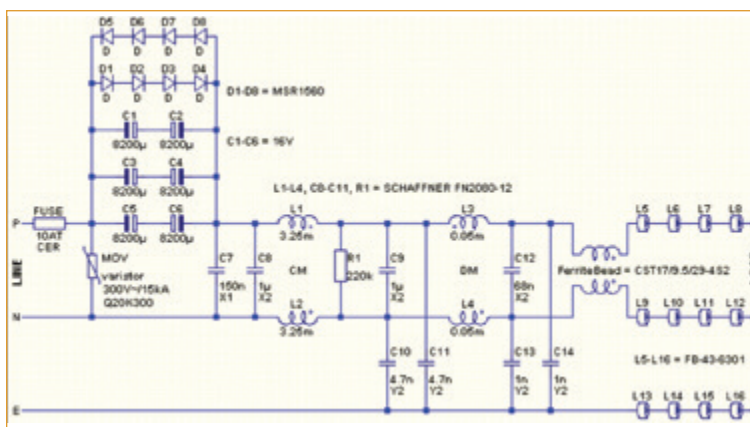
noise makers, as well as the sensitive signals (**FIGURE 2**). One of the best ways to reduce coupling between those two types of elements is simply adding space.

Placement and orientation of components and printed antennas go a long way toward mitigating noise issues. However, the luxury of a generous PCB is a rarity. No matter the amount of electronics, printed circuit boards cost money, so less is more. Doing more with less is our existential challenge. A lot of designs have an external oscillator, so let's take a look at that.

The crystal (**FIGURE 3**) is placed close to the IC, but we could achieve shorter traces by rotating the circuit 90° clockwise. Note the route keep-out that creates a moat that separates the outer layer ground plane from the pins of the crystal. Putting a ground via on the edge of the shape defeats the purpose. Ideally,



**FIGURE 1.** My Blackboard with a new surge protector that also filters EMI and RFI.



**FIGURE 2.** These components are the typical building blocks of a noise suppressor circuit. (Source: Audio Karma)

## JOHN BURKHERT JR.

is a career PCB designer experienced in military, telecom, consumer hardware and, lately, the automotive industry. Originally, he was an RF specialist but is compelled to flip the bit now and then to fill the need for high-speed digital design. He enjoys playing bass and racing bikes when he's not writing about or performing PCB layout. His column is produced by Cadence Design Systems and runs monthly.





# Understanding *High-Speed* Constraints

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*written by*  
**Charles  
Pfeil**

Charles Pfeil has spent over 50 years in the PCB industry as a designer, owner of a service bureau, and in engineering management and product definition roles at Racal-Redac, ASI, Cadence, PADS, VeriBest, Mentor Graphics, and Altium. He was the original product architect of Expedition PCB.

there are one or more XO return pins for a direct ground path back to the SOC.

A mechanical outline for a PCB typically comes from a mechanical engineer with little to no electrical training. They might give us one part of the board where tall components are allowed. Wouldn't you know it, the tall components include the crystal. All that thing does is sit there making noise, so something has to be done with the long link back to the mothership.

Internal routing is more effective than running an aggressor on the outer layers. That notion is predicated on the fact there will be an unbroken ground plane both above and below the trace. Taking it a step further, a dedicated shape on the signal layer that encloses the trace is a good policy.

In **FIGURE 4**, the ground net is highlighted in green. The cyan and magenta represent layers 3 and 5. The via labels indicate the span of the microvias. We want to tie the relevant ground planes together, but not necessarily any other ground layers. If we were to flood ground on the routing layers, the full plane would not engulf these guard-bands. You might have noticed several signal vias without an adjacent ground via. The signals on both layers see the ground plane on layer 4, so the ground via is a feel-good measure.

Note: I used a 2-4 microvia stack for layer three and a 4-6 microvia stack to shield the layer five routes. Finally, going beyond a single return via for the transition from layer three to layer five, there is a cluster of 2-6 vias around the 3-5 signal vias. The idea is to form a coaxial Faraday cage in the z-axis. In cases where there isn't this amount of space, do your best to isolate the noisy party.

We hear a lot about length-matching, phase tuning and taking care of the impedance of high-speed connections. We know vias are a discontinuity to avoid if possible. Routing over a split or void in the reference plane is a no-no. All these impedance and timing rules are also necessary to keep EMI to a minimum.

We are also drilled to keep inductive loops small when we place and route bypass caps. We are told to use multiple vias for power and ground planes. Alternating power and ground

planes transforms the PCB into a bunch of free capacitors. These signal integrity and power integrity rules are there for the circuit performance reasons listed above but also to quell emission of spurious radiation. Solid design practices help bust EMI and RFI problems.

Reducing crosstalk reduces power consumption. Making noise takes energy, so suppressing the noise saves power. I mentioned noise suppression is usually an additive process. Each of those resistive, capacitive and inductive elements has its own parasitic effects. It's like adding cream and sugar to make the coffee less bitter. At a certain point, we lose the flavor of the coffee and need a stronger brew.

An elegant layout that accounts for potential energy transfer does not require as much cream and sugar on top of the essential circuits. The ground net plays a huge role. It's the most interesting net on the board. Vias are the one element that prevents the ground net from taking on a charge from the other

nets.

Staking down the edges of the ground planes, including the voids, makes for a PCB that runs quieter and provides a substantial path for thermal dissipation. Once you've digested all the basic rules around EMI, you'll see PCBs in a different way. We can immediately spot it when an artist tries to draw imaginary circuits for a logo.

The average person sees the circles and lines and does not know the difference. A trained designer spots the flaws in a heartbeat. That goes beyond the artistic rendering and down into the nuances of memory routing or even chaining a bunch of guitar effects together to create a sound I hear inside my head. I'm looking beyond the wires and connectors to think inside the box. That's how a PCB designer sees the world. ▢



**FIGURE 3.** A crystal and its passive parts.



**FIGURE 4.** Guard bands around noisy traces. The surrounding low-speed signals benefit from the isolation.

# The 5G Rollout Should be Flying High – Literally

Affordable and accessible technologies are the key to global progress.

**MY SMARTPHONE DOES** everything so well I hardly use my tablet or laptop at all. It contains all the apps I need to use every day, is always with me and always connected, and the clarity of the screen makes it a pleasure to handle the majority of computing tasks on this device. I am convinced improvements in display technologies have helped the smartphone become the go-to device for a vast number of daily activities.

To support the best possible experiences in video, photography and gaming, new display technologies continue to emerge to provide seamless, immersive viewing. OLED displays are dominating the smartphone and flat-panel television markets, bringing attributes such as conformability and optical performance, including high contrast ratio with the ability to render true black, which conventional LCDs cannot manage.

But we humans are insatiable by nature. If the color is good, the viewing angle could be a little wider. If the angle is okay, the contrast could be higher. Now, another change is in progress with the arrival of mini-LED backlit LCDs. Containing many thousands of individual mini-LED emitters less than 0.2mm in size, the backlight has many dimmable zones and permits deep black levels, high contrast ratio and high luminance.

The prevalence of bright, high-resolution and colorful displays almost everywhere we look is another example of the way our technologies are constantly adapted to deliver better experiences and improve the quality of life for large numbers of people.

Technologies are usually expensive when launched, and often aimed at a relatively small and select market. They almost always evolve to become affordable and accessible for the masses. A combination of mature technologies and processes have been combined with new techniques to enable affordable mini-LED displays. We can expect further development of mini-LED displays to reduce the number of components and simplify control, improving both viewing performance and affordability. And we expect high-performing substrate materials with suitable dielectric and mechanical properties, as well as special optical microstructures, to be available for high-volume mini-LED production.

The optical microstructures also make these materials ideal substrates in horticultural lighting for applications such as indoor farming, also called vertical farming. As populations around the world continue to urbanize, growing fresh produce inside buildings such as multi-level warehouses can enhance efficiency in the food supply chain while saving costs and environmental burdens associated with food transportation. Spectrally tuned to the red and blue wavelengths

that maximize photosynthesis for faster growing, horticultural LED lighting earns vertical farms the nickname “pinkhouses.” Some indoor farmers believe the growth is as much as 20% faster with tuned LED lighting. Generating only photosynthetically useful photons also minimizes energy consumption. Other advanced technologies such as automation of crop care and harvesting are also being employed, helping indoor farming become cost-effective, profitable, and environmentally beneficial.

Our industry continues to come up with great ideas to improve our lives. I am intrigued by the Loon project, initially launched by Google, which promises to greatly democratize access to high-speed Internet by providing flexible 4G and 5G access. Loon – so called because the idea seemed crazy at first – puts 4G base stations in the sky, mounted on-board large balloons at stratospheric altitudes to avoid weather and commercial aviation. They have been successfully connected to commercial mobile networks, and agreements have been established to start services in various locations in South America and Africa. It’s an ideal solution for places beset with logistical and technical challenges and could help prevent large numbers of people becoming left behind as the digital and information revolutions gather pace in the developed world.

It’s not the only “flying infrastructure” concept out there. A fleet of drones has recently been proposed to provide 5G coverage for the UK. Apparently 60 units is enough to cover the entire country, each providing hundreds of steerable beams from a 3 m. antenna, at less than the cost to install conventional infrastructure. Their hydrogen-fueled motors eliminate emissions worries associated with keeping the drones airborne, and each drone will fly for several days at a time. Like the Loon balloons, they are designed to operate at stratospheric altitudes to avoid interfering with commercial aircraft.

I’ve mentioned in previous columns that 5G rollout to rural areas could take some time using conventional base stations. Using drones or balloons to provide access from the sky may offer a faster solution.

Another advantage of flying base stations like these is they can be set up quickly in disaster zones, provided the necessary supporting infrastructure is in place. The base stations can bypass access and power supply problems close to the affected area, enabling

*continued on pg. 31*

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# Etch Effects Explained

The impedance implications of the trapezoidal trace.

**UNTIL RECENTLY** I thought those who believed in rectangular traces were about as common as those who believe in square waves and a flat earth. Recently, though, I came to realize it's not as clear as I thought, not only for newbies but in general. Over the past 25 years, I've acquired a good number of books on PCB design and signal integrity, and you wouldn't know from reading most of the industry literature that traces were anything but rectangular. Interesting, right?

If you've read previous "Material Matters" columns, you may recognize the following cross-section from our Z-solver software. Among other things, it shows that the base of a trace, facing the core dielectric, is wider than the side of the trace that faces the prepreg. As such, the trace trapezoids face both up and down in a multilayer stackup. There's no relationship to the layer number or whether the trace is on the top or bottom half of the board. For this reason, some including me – but not everyone – avoid using terms like "top" or "bottom" with regard to trapezoidal traces.

In the dimensions shown in **FIGURE 1**, the  $w1$  value at the base of the trapezoid is the value hardware teams and fabricators exchange when talking about trace widths and spacing(s). It's important to know that actual fabricated boards won't have quite that much copper. As traces are etched from top to bottom, the etching chemical ("etchant") remains in contact with the prepreg side of the trace longer than the core side. This makes the prepreg side of the trace narrower than the core side and gives the trace a trapezoidal cross-section. In this column we'll discuss the reasons for this fabrication phenomenon and the implications for impedance.

**Innerlayer etching.** Etching innerlayers involves cleaning the copper on both sides of the laminate, applying a photoresist, exposing the photoresist to create the innerlayer pat-

tern, developing the resist, etching away the unwanted copper, and removing the etch resist. This process is automated in most shops, and the chemistry is automatically monitored. As a result, the accuracy and repeatability is quite good. Using this process, it is possible to etch innerlayer traces to an accuracy of  $\pm 0.5$  mils. This accuracy control helps keep impedance within the tolerances required for transmission lines.

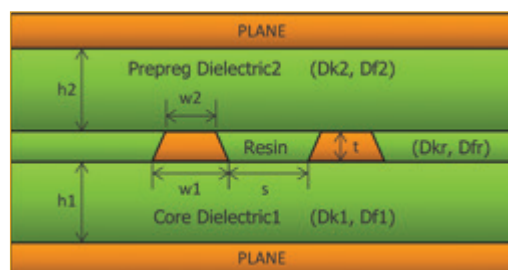
After cores are cleaned, **FIGURE 2** shows a blue light-sensitive film or photoimageable "resist" that is applied by heat and pressure to the metal surfaces of the core. The film is sensitive to ultraviolet light. If you ever tour a fab shop, the room where photoresist is handled uses "yellow light" to prevent inadvertent exposure of the resist. The filters remove the wavelength of light that would affect the resist coating.

The Gerber, IPC-2581 or ODB++ data for the part are used to plot film that depicts the traces and pads of the board design. The phototools or artwork include the copper features. This film is used to place an image on the resist.

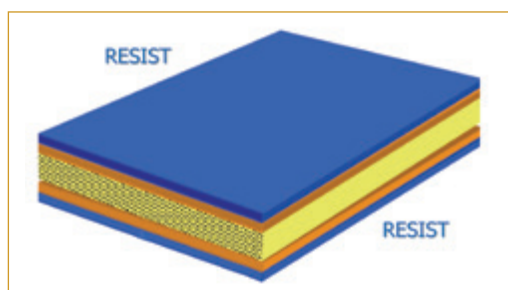
Innerlayer film is a "negative" image of the copper features, meaning the copper patterns left behind after processing the core correspond to the transparent areas on the film. Core panels are exposed to high-intensity UV light that serves to harden or "polymerize" the film resist, creating an image of the circuit pattern, similar to a slide-negative and a photograph.

The exposed core is then processed through a chemical "developer" that removes the resist from areas that were not hardened by the UV light. Next, the copper is chemically etched from the core in all areas not covered by the remaining blue dry-film resist. After etching, the developed dry-film resist is chemically removed from the panel, leaving just the copper features exposed on the panel.

It's even more nuanced than we've alluded to so



**FIGURE 1.** The trapezoidal shape of innerlayer traces, shown in a stripline cross-section, where  $w2$  is narrower than  $w1$ . (Image from Z-zero's Z-solver software)



**FIGURE 2.** Blue resist film is placed on both sides of an innerlayer core prior to imaging, UV exposure, and subsequent etching.

## BILL HARGIN

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far. As **FIGURE 3** shows, the actual sides of a trace are curved, and an etching “undercut” is below the blue resist. Remember  $w_1$  is the dimension hardware teams and fabricators use to describe trace widths.  $R$  is the width of the resist the fabricator uses. And the ledge under the resist is the undercut,  $u$ . Ideally,  $R$ ,  $w_2$  and  $w_1$  are equal. The closer a fabricator can get to this, the better, and good fabricators work hard to achieve this.

The gap between resist areas is removed evenly at first and then in a progressively cup-shaped fashion until the center area between traces is broken through to the exposed core dielectric, which opens progressively as the etchant goes to work in and under the resist as the side wall is gradually removed through increased exposure. The amount of time the copper is exposed to the etchant determines the final shape of the copper features, as illustrated in **FIGURE 4**.

A resist width ( $R$ ) equal to the base of the trapezoid ( $w_1$ ) is ideal etching. In Figure 4, this corresponds to the 140 sec. etching scenario. Note too that if  $R$  is less than  $w_1$ , as in the cases up to 125 sec., the copper features or traces are underetched. In the case where the copper is exposed to the etchant for 165 sec., the copper is overetched. The times here are for this specific example, where cupric chloride was used as an etchant, targeting 3.0-mil line and space patterns, using 1.0-mil resist on 1-oz (1.35-mil) copper foil.

**Etch factor.** From the parameters in Figure 3, there are two descriptive measures of the etching process: undercutting and etch factor. Undercutting is well-defined. It's the average overhang of resist after top width reduction. Hardware teams don't really need to worry about the width of the resist, but the “undercut” term and concept are useful. Obviously, the goal is to minimize the  $u$  parameter.

$$\text{Undercut (u)} = \frac{R - w_2}{2}$$

“Etch factor” is quite a bit murkier. Some define it as being proportional to copper thickness,  $t$ , and inversely related to the difference between  $w_1$  and  $w_2$ , the width difference in the trapezoid. But depending on whom you talk to, these relationships may be inverted or use different parameters.

I find the relationship shown in **FIGURE 5** intuitive. It

would be nice if we could agree on a definition like this, where  $x$  (“etchback”) is the difference between  $w_1$  and  $w_2$ , and “etch factor” is defined as the degree of etchback per thickness.

**Fabricator data.** Average suppliers typically maintain roughly 0.25 mils of etchback for 0.5-oz. copper and 0.5 mils of etchback for 1-oz. copper, respectively. Advanced PCB manufacturers can bring these numbers to 0.17 mils for 0.5-oz. copper and 0.45 mils for 1-oz. copper.

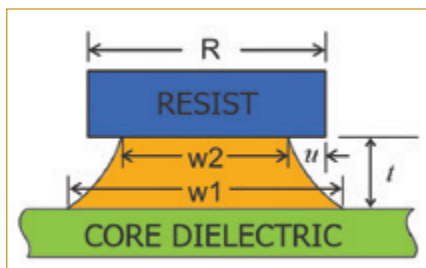
I could be talked into changing the practice, but to avoid getting the complications of conflicting definitions, I've worked in percentages, specifically the ratio between  $w_2$  and  $w_1$  (with the goal to get as close as possible to 1.0).

Using this approach, advanced PCB manufacturers might achieve  $w_2/w_1$  of 0.972, for example, for 0.5-oz. copper. Similarly, research shows advanced manufacturers can achieve  $w_2/w_1$  of 0.925. The limitation with this approach is that it presumes a specific value for  $w_1$ : in this case, 6 mils.

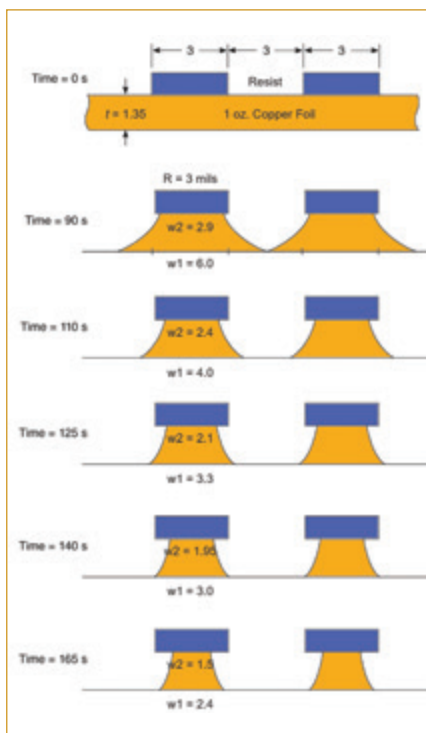
**Plated layers.** I hate to open another can of worms to discuss outer layers but will touch on the subject for completeness. In short, outer layers are even more complicated, particularly in the case of multiple plating steps and when copper reduction techniques are used to keep the surface copper thickness down. Sometimes, microstrip traces are anvil-shaped rather than trapezoidal-shaped, but more commonly they look more like a “mesa,” borrowing a term from geology, with the top-plated section almost vertical and the trapezoidal cross-section at the bottom; i.e., a rectangle on top of a trapezoid, with the rectangle representing the plated Cu. To model this, some use a 1-mil etchback for a plated microstrip. This seems to best represent “most” outer layers, although it is still incorrectly modeling the cross-section as a trapezoid.

Plated layers often have “other challenges,” including that there may be one, two, or even three plating passes. Some designs are plated 1x and end up exactly 1-mil thick, while other

boards have 1x plating and are considerably thicker.



**FIGURE 3.** The actual sides of a trace will be curved, and an etching “undercut” is below the blue resist.



**FIGURE 4.** Using a 3-mil resist, with a 3-mil target for  $w_1$ , these images show the amount of time the copper is exposed to the etchant determines the final shape and widths of the copper features.

*continued on pg. 31*



# What Is the Shortest Flex Length Between Rigid Areas?

The shorter the length, the stiffer the flex.

I HAVE AN application requiring two rigid PCBs mounted at 90° to each other. I would like to connect them with a flex zone and use rigid-flex construction. How close can rigid areas be to each other; i.e., what is the shortest flex length between rigid areas?

Most manufacturers can form 0.250" flex sections with no issues, and many can get down to less than half that. There are manufacturing and final-use implications of short flex sections between rigid areas on rigid-flex circuitry. The manufacturing issues affect cost, and the final-use issues could cause premature failure if the specified flex length is too small.

## Manufacturing Issues

**Alignment/misregistration.** How a flex area is created in a rigid-flex circuit is important to understand to grasp the challenges. You probably know that copper-clad polyimide substrates are present in both flex and rigid areas of a rigid-flex, not just in the flex areas. The way the manufacturer makes an area “flexible” is by *eliminating all rigid materials* in those areas. This is done many ways, depending on the manufacturer, but virtually all include a punching operation to form “windows” in the prepreg adhesive and FR-4 layers. These rigid layers then are aligned to the flex layers, so the future flexible areas are prepreg-free. The smaller these areas, the more critical alignment is. For example, consider an application where the distance between rigid areas is 0.1". If the top prepreg layer is skewed to the right by 0.015" and the bottom prepreg is skewed to the left 0.015", the flex zone is now 0.07", not 0.1". This is a 30% reduction in flex area, which could have a significant impact in the final application. However, if the flex zone is an inch wide or more, a 0.03" reduction is inconsequential. Very short distances between rigid areas can have a significant impact on yields and therefore cost.

## Final-Use Issues

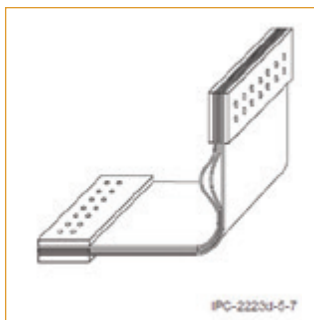
**Stiffness.** Short flex regions are stiffer and more difficult to bend. You want the circuit to bend 90°, and a shorter flex area will force the circuit to execute

that bend over a shorter distance – basically boxing the circuit into a very tight bend radius. The smaller the distance between rigid areas, the tighter the radius the circuit will have to bend. This issue becomes more critical as the flex layer count increases, due to the added thickness.

**Strain relief.** Many rigid-flex designs require a bead of semi-rigid epoxy for strain relief along each rigid-flex interface. This epoxy bead is typically applied by hand with a manual syringe or hand dispenser. The flow properties of the material and the epoxy applied by hand can lead to significant variation in the width of the strain relief bead. The typical range of bead width is 0.30" to 0.60". Keep in mind this will be on *both* sides of the flex and on both ends of the flex zone. In reality, the actual flex zone could easily be reduced 0.060" to 0.120", depending on bead width (**FIGURE 1**).



**FIGURE 1.** Adding strain relief can cause a much tighter bend radius on a short flex section.



**FIGURE 2.** Buckling will occur when an unbonded flex construction is bent. (Source: IPC-2223)

**“Loose leaf” or “unbonded” flex layers.** Loose leaf or unbonded construction makes the flex areas of a rigid-flex more flexible. This technique involves breaking up flex layers into multiple layers that are not bonded to each other; e.g., turning a six-layer fully bonded flex zone into three two-layer flexes that are not laminated to each other. When the distance between rigid areas is reasonably wide (~1" +), loose leaf construction can be an effective way to increase flexibility. When the circuit is formed, the flex outside the bend will perform as if it is the only flex layer. The remainder of the flex layers to the inside of the bend will now be “too long” when the circuit is formed and will buckle. Again, this is a good strategy when there is plenty of room to accommodate buckling. But when the distance between rigid sections shrinks, there is less room for the internal layers to

buckle without causing damage to the circuit (**FIGURE 2**).

Short flex regions on rigid-flex designs are more common as device sizes shrink and there is less room for everything, including the flex. It ends up a balancing act where cost, functionality and available space are all weighed to hopefully arrive at the best overall solution. □

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# A NEW INDUSTRY COMMUNITY

## Explodes Online During a Global Pandemic

A collaborative educational group formed in January and adapted virtually to bring the industry together. **by CHELSEY DRYSDALE**

A year ago, after IPC dissolved the Designers Council, its board members formed the Printed Circuit Engineering Association (PCEA) to continue their pursuit to collaborate, inspire, and educate the PCB design and engineering community.

The PCEA's mission is to promote the printed circuit engineering profession by encouraging and facilitating the exchange of information and the integration of new design concepts through communications, seminars, and workshops. Its efforts are buttressed by a network of regional chapters and the support of sponsors, including several CAD companies and other firms.

The PCEA has a growing membership of more than 1,000 members, with existing chapters in Phoenix, Orange County (CA), San Diego, Silicon Valley, Ontario (Canada), Minneapolis-St. Paul, Monterrey (Mexico), Nogales (Mexico), Research Triangle Park, and Seattle. Chapters planned for the near future include Columbus-Cincinnati-Dayton; Grand Rapids, MI; Illinois-Wisconsin; New Hampshire-Massachusetts; Albuquerque; Houston; Dallas; and Austin. The PCEA hopes to open another Canadian chapter soon.

The association established affiliations with SMTA and the European Institute of Printed Circuits (EIPC), and has gathered a significant number of members from Europe and Asia (**FIGURE 1**).

Because of the effects of Covid-19, chapter meetings are being held online. One of the rare positive side effects of the pandemic, the trade group leaders say, is Zoom has made it possible for regional chapters to share ideas outside their immediate surroundings. For instance, a dual chapter meeting is expected in

early December, led by the Orange County chapter, the largest PCEA chapter in the US, paired with the Seattle chapter.

PCD&F spoke in November with Stephen Chavez, CID+, chairman, Michael Creeden, CID+, vice chairman, and Gary Ferrari, CID+, chairman emeritus, to discuss current challenges and how the PCEA aims to help.

**PCD&F:** What are the leading issues for designers in today's world?

**Michael Creeden:** Technology is evolving. There are three fronts: how to solve a very dense packaging solution; high-speed and RF signal performance; and advanced manufacturing requirements. Everything is getting smaller. All three perspectives must be addressed at the same time (**FIGURE 2**). That is the definition of what we're trying to do. [We must] take a holistic approach with three competing perspectives, [and not] sacrifice one for the other two.

**Stephen Chavez:** You can't solve one without the other. The target goal is the first time you fire up that board, it works. If a respin is done, the circuitry is designed wrong. That's a board failure. It doesn't matter if it's RF, digital, high power, crazy gigahertz. What matters is you attack three perspectives. The essence of board design is the same no matter your background, language, location, or the tool you use. How you do that is up to you. You have to make that first design work. The triangle better be a tattoo on your arm.

**Creeden:** The profession is in an evolution



**FIGURE 1.** PCEA international activity.

right now. Education need is very strong. Who is filling the ranks? Historically, it was the designer. It was historically a mentor or apprenticeship profession. Designers served like one of the trades. You came in as a junior designer; then you were a designer, then a senior designer. But the fabricators and assemblers used to work for OEMs. Sometime in the '80s, manufacturing was no longer with the OEMs. They branched off on their own. Industry did not replenish the design staff. Designers got paid more money and eventually got gray hair. With the shortage, they conscripted electrical engineers coming out of college, but EEs had no PCB training in college.

**Chavez:** A lot of people don't know what they don't know. For engineers coming out of college now, guess what? It doesn't end here. If you don't like learning, this isn't the career for you. You have to constantly learn and evolve and be adaptable, whether you're getting it from a textbook or magazine article or webinar or speaker. The job is getting bigger and bigger. It's getting harder to find seasoned veterans. It's hard to find someone who truly knows how to design a printed circuit board. The designer makes the difference, not the tool.

**Gary Ferrari:** Designers are having the biggest problem with technologies changing rapidly. The tools are sophisticated. You have to have a good electrical background. Designers don't usually have that. Most are homegrown. We're seeing many companies forcing their engineers to do design. It creates a big problem. They can connect the dots and make that part work, but they don't know about manufacturability. Engineers are forced to do something they aren't trained for, and designers are going into technologies they weren't trained for.

**Creeden:** I've never met an engineer who says, "No, I can't do that." So, the engineer sits down and starts figuring it out. However, they would only pass the layout phase three to five times a year. One designer used to support five engineers. Engineers don't stay proficient at the tool, which is complicated, and they don't understand manufacturability. Layout is harder than doing schematic for the engineer. You either learn at school, self-study, or learn with the herd. All of them are valid directions to go in. You should always continue to go to school. You should always self-study. You should always have industry involvement.

One of PCEA's charters is to inspire (a neat new idea to build a better mousetrap) and educate (*how* to build a better mousetrap). PCEA is the central hub drawing people in to fulfill that ongoing mission. Every CID instructor is on our board.

**Ferrari:** All the instructors are master instructors. They are all known people in the industry from all over the place.

**PCD&F:** Speaking of the differences between designers of various experience, how do you ensure the PCEA remains relevant to both the older designers, many of whom are not engineers

by degree, and the newer generation, for which layout is often just a part of their larger job responsibilities?

**Creeden:** We're educators. We have a passion to fill this problem. We are like a wildfire spreading right now. People want to belong. Designers, fabricators, engineers, assemblers – we're all drawn into this. We are holding chapter meetings virtually, which draws a global reach. We reach out beyond our regional sphere of influence. There's a virtual time-zone draw now.

**Chavez:** The biggest thing is constantly bringing people together to collaborate. Not just designers and engineers but affiliates. Let's get talking in one big collective as one industry. That is the way we evolve. We feed off each other. Designers and engineers who are really good know what they don't know. They are not afraid to ask questions. "Don't give me a fish; show me how to fish and where to fish." That's what I see coming from the new younger generation out of college. They are hungry for knowledge and not afraid to say, "I don't know." The problem is we don't have

enough quality mentors around. The first thing we thought about with PCEA: choose to be a mentor or a mentee. Mentors share knowledge to change someone's life to expand success. There's a ripple effect. How do you improve other people's lives so they can look in the mirror and be happy with who's looking back at them? That's success.

**Creeden:** PCEA has a mentoring program geared to pair up those who want to share expertise and those who wanted to be mentored. It is truly meant to bring those two people together. That's how we hope to stay relevant. We'll be bringing content: education, webinars, etc.

I mentor three people in the industry currently. I have a relationship with [them]. They're soaking up [information] like a sponge. It's a two-way exchange. I learn from them as much as they learn from me.

**Chavez:** I mentor other designers and other engineers in general – one mechanical engineer. It's not so much mentoring PCB design but mentoring them in the life of an engineer and how to balance what they're up against and how to be a better professional and what's expected when they are climbing the ranks. One of the EEs I hired is my manager now. It's the perfect example of sharing knowledge and experience – the kind of education you don't get in school.

**Ferrari:** What are we doing for designers?

1. We are giving them any kind of technical assistance they need in their chapters: a home to grow. We want designers to talk to each other and exchange information.
2. Two chapters met together virtually with guest speakers (San Diego and Phoenix). When you bring in a group from another state, it opens the door. I hope this catches on.



3. We want to give them a Zoom seminar or technical activity every other month.

The bottom line is we want to give designers as much information to make them successful. [When someone asks,] “Listen, do you have anything on this technology that I just read about?” we want to be able to research that and have somebody come in to teach them. Chapters should share information.

**PCD&F:** How would you assess the current state of PCEA, and is it meeting your expectations?

**Chavez:** PCEA is a collective of all skillsets and all levels of experience. Put these people together to talk and communicate. Let humans be humans. Encourage each other. By sharing knowledge, you’re sharpening your own blade. You’re dusting off the cobwebs [of what] you’ve done automatically for 30 or 40 years. When you explain it, [you realize] there are ways you can improve and optimize. You share lessons learned so youth doesn’t make the same mistakes. A majority of engineers are willing to do that. We cling to those who are hungry and introduce them to people: “This is who you need to know.”

PCEA is more than just a collaboration of colleagues. It’s about human collaboration, inspiration, and education and making friendships, networking, and evolving. If I have a problem, I want to tap into my network. It’s much easier to talk to a friend than a stranger.

**Ferrari:** It’s the program and the people. If we can make a big dent and get designers to realize they have an organization [where] they can learn all new stuff, I consider it successful. It’s on its way. We’re trying to get linkage [between veterans and new people] within the chapters. We’re trying to get new folks into chapters to learn from senior people. The chapter basis is the best. A designer comes in and is struggling with something. They are not going to get an answer from one person. They’ll get answers from several people. Design isn’t black and white. [They] get to see different ways of doing things and why they were chosen. New folks learn from everyone talking shop. That is very valuable.

By the way, chapters aren’t only for designers. They are for anybody who has a vested interest in the printed wiring board industry: engineers, assembly people, purchasing people. That’s our target: to address the same thing to all these people.

**Chavez:** We share the latest industry content and understanding as designers: what you really want vs. what you call “noise.” [We share] what is truly the meat and potatoes of what you need to know. My job now is to share knowledge.

**Creeden:** Sponsors are leaning in, supporting chapters, bringing in technical know-how and educational content. Sierra Circuits is hosting. PCB Libraries. American Standard Circuits. [Other current sponsors include Insulectro, Mentor, a Siemens Business, and EMA Design Automation.]

**PCD&F:** What are the primary near-term goals for the organization?

**Chavez:** Our vision for 2021 is to contribute to growth. PCEA is gaining more and more momentum. It’s getting huge. We are all volunteers doing this part-time. I can easily see where we can no longer do this part-time. We may need a lot more than the core group we have. We’re always looking to add to the collective. You are eagerly welcome to belong. You’ll gain longevity in the industry. It amazes me how fast we’ve exploded. It exceeded my expectations.

**Creeden:** PCEA affiliates include UP Media Group, PCB007, SMTA, and EIPC. It’s our hope to have more. PCEA held a full educational track at SMTAI. It was well-attended. PCEA also facilitated PCB West tracks. The goal is to bring expertise to other portions of the industry.

**Chavez:** The silver lining of Covid-19 is we wouldn’t have the success we’ve had if we hadn’t been online. We are able to collaborate faster and instantly; we are adapting to virtual. I long for the days of face to face, but as our global footprint has shrunk, our virtual

footprint has expanded. We are collaborating with people we wouldn’t normally collaborate with.

Because of Covid-19, the majority of companies that can shrink their rental space can afford to pay you better and get additional team members they couldn’t afford before. PCEA is the collective hub. We will bring the IPC essence to the industry. It’s a win-win for everyone. “Where can I go to find out who’s hiring?” Tap your professional network at PCEA. “We’re thinking of trying this technology.” Tap that network.

**Creeden:** There’s excitement in the air.

Printed circuit industry professionals from any associated discipline are encouraged to join the PCEA. Membership is free. Visit [pce-a.org](http://pce-a.org) for more information. □

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**FIGURE 2.** The design triangle.

# PCEA and Women Industry Leaders

Some of our favorite subject-matter experts explain what motivates them.

**IN THIS MONTH'S** column I introduce a few of our inspiring women PCEA leaders. Next, PCEA chairman Stephen Chavez offers his take on the importance of diversity in a collective organization. As always, I include our list of professional development opportunities and events. Last, I tease some upcoming coverage on one of the PCEA's educational networking events.

## PCEA Updates

One of the most inspiring events I've had the opportunity to cover over the past decade was an early morning Women in Electronics at IPC Apex Expo. This event brings together women in the electronics industry to join their colleagues across the supply chain to network, share ideas, and discuss career experiences. It is an opportunity for women in the industry to learn from and inspire one another.

Recently, I've appreciated that within our PCEA meetings, we experience that same zeal with our executive staff every time we convene. It is not difficult to realize the impact of leadership by women in electronics in the PCEA. Many of our leaders – including women – reach out, team up, and work together to tackle many of the tough tasks that must be accomplished as the PCEA moves forward.

Tara Dunn, Susy Webb and Eriko Yamato are well-known in the electronics industry for service and leadership in their areas of expertise. They are subject-matter experts, and their experience spans high-tech electronic materials, flexible PCB manufacturing, emerging additive process technologies, and solid PCB design instruction. They are a few of the many women who dynamically serve their companies and customers each day and still find enough time and energy to contribute their leadership to the PCEA.

Here I share their backgrounds and hopes for the PCEA.

### Tara Dunn

Tara Dunn is a seasoned professional and columnist with more than 20 years in the electronics industry, exclusively focused on the PCB sector. Her experience spans roles from manufacturing to sales and marketing.

Tara is president of Omni PCB, a manufacturers' rep firm focused on the PCB market, offering sales and engineering support with technology ranging from standard technology to high-end HDI products. Spe-

cialties include flex, rigid-flex, RF microwave designs, and microelectronics. Her website ([pcbadvisor.com](http://pcbadvisor.com)) shares technical information related to all segments of the PCB industry.

Tara is also a founder of Geek-A-Palooza. This annual event provides all aspects of the local electronic industry with a unique networking experience focused on expanding resources and knowledge, building relationships, and bringing the industry together in a social atmosphere.

"My vision for the future of PCEA is to be all-inclusive, offering strong technical content, networking, and relationship building for designers, fabricators, and assemblers. My desire is for experienced PCB engineers to offer support to those new to the field, and those new to the field to bring energy and new ideas in return. With a strong network, what this industry can accomplish is limitless, and PCEA provides tools and community to inspire."



### Susy Webb

Susy Webb is a senior PCB designer with 40 years of experience. Her career includes experience in coastal and oceanographic oil exploration and monitoring equipment, point-to-point microwave network systems, and

CPCI and ATX computer motherboards. Webb is a regular speaker at PCB West, IPC events, and international design conferences, and she consults for individual companies and groups. Her presentations discuss the practical implementation of complex engineering concepts into board layout and methods to improve the overall design and flow of PCBs.

Susy is CID certified, a chapter writer for *The Printed Circuits Handbook*, and one of the judges for the annual TLA competition. She is also an active member of the PCEA Executive Board and education committees and is a member and past president of the Houston Chapter of the Designers Council.

While working a full-time PCB engineering job, Susy constantly seeks to learn more about the physics, electronics and DfM concepts that lead to better board design. She shares those concepts as a speaker/teacher at conferences and companies and strives to show others the reasoning behind why things are best done a certain way. Susy also maintains active involvement in the industry in the form of professional associations.

"The PCEA is an organization where engineering

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professionals can come together and discuss ideas and share experiences. There is an overwhelming amount of engineering information online. As a part of the education group, we seek to continually update the information on our web page about resources, articles, and books we have enjoyed, and which we find most accurate and beneficial, to be sure others know about them. In the coming year, we also hope to share some of our own articles and give presentations to local or web-based groups. We would also like to work up some training programs to help people who do not yet have a PCB background to design effective-and-correct-the-first-time boards.”



### Eriko Yamato

Eriko is originally from Kobe, Japan, and spent five years in San Francisco during her childhood. After getting a bachelor's in political science at Keio University in Tokyo, she worked at a TV station for five years, producing infotainment programs, sports news, and documentaries. In 2000, she

returned to California to pursue her passion for documentary film production at Stanford University, where she received her master's in communication and discovered her other passion: marketing.

Eriko has 15+ years of experience in technical marketing of EMC, SI, PI, and RF/wireless products and is currently marketing and QTA manager at Oak-Mitsui Technologies, headquartered in Frankfort, KY. She has been active with the IEEE EMC Society since 2012 as an officer and currently serves as the treasurer for the IEEE EMC Society Atlanta Chapter. Eriko is also the marketing representative for the IEEE EMC Young Professionals Group. In her spare time, she enjoys traveling, cooking, wine tasting, CrossFit, and hiking.

“I was truly honored when Steph Chavez and Mike Creeden asked me to help out PCEA as the events committee chair. I have been involved with the IEEE EMC Society for several years, and I enjoy giving back to the electronics industry. The PCEA is such a great organization where you can connect with other industry professionals, share information, and educate and support each other. This year has not been the easiest for all of us, to say the least, and I hope to organize an in-person event in 2021 where we can all reconnect and reenergize. Through events, I would like to showcase how resourceful PCEA is and encourage professionals to be part of this collaborative organization.”

### Message from the Chairman

by Stephen Chavez, MIT, CID+

Activity overload? Not for many, like those within the PCEA leadership team, who tend to shift it into a higher gear and thrive in this last quarter of the year, as they do year after year. There is no doubt PCEA activities continue with great success. As I review how the PCEA started, including where we are today and how we are coming along, it's awesome to see we are evolving beyond expectations.

At the core of this success is the engine that keeps PCEA

moving forward: the core leadership team comprised of talented, passionate, experienced, and selfless individuals. One of the many things I love about this team is it's a diverse group of special individuals and includes some awesome women who are vital parts of the PCEA leadership engine.

The PCEA strongly believes in and supports diversity. We see it, realize the strength in it and the importance of it, and encourage it. And when I refer to diversity within PCEA, I mean the women who are part of this PCEA engine. In no particular order, Susy Webb, Cherie Litson, Judy Warner, Tara Dunn, Terri Kleekamp, and Eriko Yamato are a force to be reckoned with. I am honored to work alongside each and every one of them. They are more than industry colleagues; they are close friends.

What these women do in their day jobs is great on its own, but what they do for and bring to our industry is where they truly shine. We are blessed to have such professional women of their caliber in our industry and the PCEA. Each of them leads the pack, and they are great examples of professional women for the younger generation to follow.

As always, refer to our column and the PCEA website to stay up to date with upcoming industry events. There are many webinars being offered, so take advantage of them. And if you have not yet joined the PCEA collective, I highly encourage you to do so by visiting our website at [pce-a.org](http://pce-a.org) to become a member.

I continue to wish everyone and their families health and safety.

### Next Month

By the time you read this, the San Diego and Arizona chapters of the PCEA will have co-hosted their first chapter meeting, which took place Oct. 28 and featured Insulectro speakers Mike Creeden and Chris Hunrath, who spoke on the following scintillating PCB materials topics:

- Design innovation
- Hybrid stackup models
- Material properties and considerations
- Effects of loss tangent
- Mixing laminates
- Embedded capacitance
- Advanced HDI structures

I'll check in with our chapter presidents and attendees for their thoughts on this event.

### Upcoming Events

- Mar. 6-11: IPC Apex Expo (San Diego, CA)
- Apr. 13-15: DesignCon (San Jose, CA)
- May 10-12: PCB East (Marlborough, MA)
- May 11-13: IPC High-Reliability Forum 2021 (Baltimore, MD)
- Jun. 7-10: Zuken Innovation World (Scottsdale, AZ)
- Aug. 31-Sept. 3: PCB West (Santa Clara, CA)
- Nov. 10: PCB Carolina (Raleigh, NC)

If you have a significant electronics industry event that you would like to announce, please send me the details at [kelly.dack@pcea@gmail.com](mailto:kelly.dack@pcea@gmail.com), and we will consider adding it to the list.



## Conclusion

There are many interesting printed circuit engineering folks out there whom we can learn from, and we will focus on the most interesting people in the PCEA from time to time. As a collective, we want to expand our diverse membership and foster healthy connections among people in printed circuit engineering. We believe this will be a fulcrum that will help our members become inspired to connect and collaborate, and it will open doors to educate and positively contribute to the wider electronics industry.

See you next month or sooner! ▢

# ACCURATE MICROSECTIONING for High-Volume Production

Processes and tools for accurate lab analysis and defect detection. by TIM WEBER, PH.D.

Electronic sample preparation is a complex process that goes beyond merely lopping a piece off a PCB for inspection. This process involves several, exacting preparation stages.

The process designs each step to specifically adapt to the inspected device's design, materials, and fabrication technology. Performing any of the preparation stages incorrectly can result in spurious features, artifacts and great potential for both Type I and Type II error.

The process starts with PCB manufacturers designing test coupon segments into each of their products. This function enables panel testing without wasting the actual production board. To confirm the lab has met product specifications, they separate the coupon from each panel.

When it comes to testing in this production setting, doing only a final inspection is insufficient. Continual monitoring of the process is vital, as otherwise-defective components may have been produced but not previously discovered. Uninspected parts might need to be recalled. Worse, components that fail in vital equipment and systems for medical, military, and aerospace end-products can cause fatalities. These boards must provide a continued performance or performance on-demand. There can be no equipment downtime, and the end-use environment may be exceptionally harsh.

Typically, the microsectioning process the article will discuss applies to PCBs that IPC categorizes as Class 3. Class 3/A boards call for stringent manufacturing criteria because the boards must remain operational in critical conditions such as in space or munitions. The IPC-6012 Class 3/A is a relatively new class that includes space and military avionics and is the highest class for printed circuits. These boards are expensive to manufacture relative to consumer-grade class products since they need to be close to perfection. Consider the environments in which these components function: aerospace, military airborne systems, and missile systems. All depend on reliable performance.

Aerospace has the AS9100

specification. For military applications, MIL-PRF-31032 establishes that PCBs must meet demanding environment requirements. The US Defense Department requires that a company certified to the specification produces every single PCB for the equipment and systems it uses.

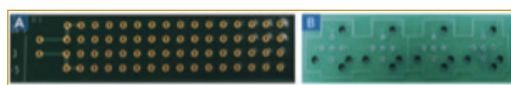
Early detection of deviations from required manufacturing standards avoids additional processing steps to remedy defective product and reduces time in the lab (and the subsequent hit to profits). Producing test coupons enables the production test lab to accurately discover and address problems "at the moment." By isolating problems, the test lab can reduce the scrap rate and increase productivity, and the operation becomes more cost-effective. In these quality control tests, the lab extracts coupons from manufactured boards. The boards are mounted and ground/polished to the plane of interest, so the lab can target areas of potential defects.

Labs have been performing microsectioning since circuit boards were invented, and along with covering the process, this article will look at recent improvements.

## Microsectioning PCBs

Microsectioning is destructive testing, though it is only performed on a test coupon, and therefore the functional portion of the PCB remains functional. A destructive technique for evaluating PCB quality, microsectioning exposes a cross-sectional view of microstructure at a selective plane. This plane usually is the center of copper-plated through-holes or vias within +/-10% tolerance of plated material thickness accuracy. This approach's beauty is that clipping these coupons is a destructive analysis of a sample piece off the board, while the working portion of the component remains intact (**FIGURE**

**1**). To set the industry standard for test coupons, IPC has developed a specific coupon design that PCB manufacturers include in each panel to experience the same manufacturing process and represent the remaining board. Moreover,



**FIGURE 1.** Examples of PCBs (a) without reference holes and (b) routed and drilled, ready for use.

# PCB Chat

## Recent Chats:



**The SMTA**  
with  
Martin Anselm, Ph.D.



**Electronics Data  
Transfer**  
with the IPC-2581  
Consortium



**EMI Simulation  
Tools**  
with Brad Griffin

[upmg.podbean.com](http://upmg.podbean.com)

# The PCB Podcast



the production lab can remove the coupon for cross-sectioning at any stage of production (**FIGURE 2**). In many cases, it is possible to manufacture coupons into the board design and a test coupon to “press out” of the board, permitting the quickest yield of test coupons. In the event the test coupon must be cut from the board, it is vital the cutting method should not introduce any defects in the sample.

Avoid aggressive methods such as the use of bandsaws or punches if possible, as they inflict excessive damage in the sample. Routing or cutting with a diamond wafering blade and coolant are the best methods for cutting the sample.

If a sample from a populated board or production piece is required, cut it with a silicon carbide (SiC) abrasive cutting wheel on a high-speed rotary tool. Ensure cutting is performed away from the specific area of interest at all times.

Tabletop saws that make these precision cuts are combining higher speeds with intuitive control. The higher speeds mean faster production, while minimizing the sample surface's deformation, which reduces time later in the preparation process.

Improved machine and vise designs enable quick and simple setup. Precision laser guidance, tool-less adjusting, and three-axis blade movement available on these newer saws align the board's target area quickly.

System programmability enables technicians to train quickly and save routines to perform consistent cuts, depending on the board design. The precision saw retains the most important and frequently used features to call up with one touch.

## Preparing Vias and PTHs on Test Coupons

When preparing vias and plated through-holes on test coupons, take care to ensure the following:

1. The final polishing quality should represent the true structure of the sample.
2. There should be no scratches or edge rounding to create errors in measurement.
3. During potting of the sample, avoid any sample orientation error. Attention to this detail ensures the mounted sample coupon does not have any tilt.
4. Hit the center of the target to avoid errors in dimensional measurement (**FIGURE 3**).

Exceptional control of the grinding and polishing steps is necessary for each step to remove deformation from the previ-

ous step completely. True microstructure with an absence of edge rounding should be shown by the final polishing step, which should also find the target feature with accuracy and good alignment.

## The Conventional Mounting Method

The conventional mounting method involves several different mount shapes, sizes and materials, depending on the application. Preparation is consequently inconsistent, and the quality of the result tends to vary. Performing this procedure improperly puts the quality of the PCBs in doubt.

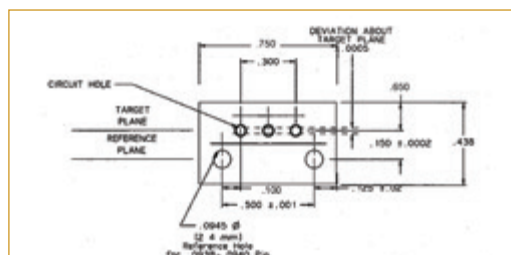
Many PCB manufacturing labs use numerous SiC abrasive papers to manually grind from coarse to fine grit size on a rotating table with water. To perform a final polish the technician typically places a water-based alumina suspension on a napped cloth. The process involves regular stops to visually inspect the sample to confirm the current location through the sample. A significant risk is that the desired point is ground through, leading to a complete loss of that production sample.

Assuming no operator errors, each sample can take 17 to 25 min. or more to complete. Grinding and polishing on a rotating plate using the manual speed setting often takes place in these cases.

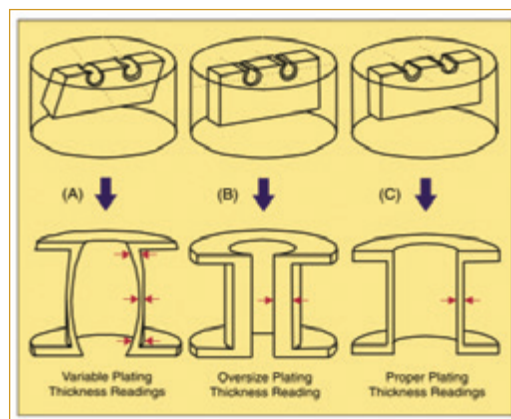
Some applications use a sequence of polishing papers, and others involve three to four, spaced through the range. Technicians use each paper for around one minute.

This approach has the following limitations:

1. Sample throughput is low.
2. The inconvenience of switching different grit sizes of SiC papers during the grinding process.
3. Quality is inconsistent due to operator variability.
4. Cleaning can cause cross-contamination if not appropriately handled.
5. Smearing can result in an uncontrolled load, which can hide crucial features like micro-cracks, delamination or voids.
6. Uncontrolled times can cause polishing relief, making both focused and accurate plating thickness measurement difficult.
7. Inspecting the sample during processing can require frequent, time-consuming stops, though necessary to ensure accurate targeting.
8. The operator needs a high level of skill to maintain the plane of grind.



**FIGURE 2.** An example of possible mounted sample deformation due to tilt error (a). Results of planar error – plating thickness is exaggerated (b). A properly prepared section (c).



**FIGURE 3.** Hit the center of the target to avoid errors in dimensional measurement.

Production delays can occur by running one sample at a time with poor preparation. This workflow may also lead to a flawed interpretation of results and too few statistical data for analysis, and ultimately costs will be higher.

## The Next Phase of Coupon Test Sample Prep

Accessory kits for semiautomatic grinder-polisher equipment overcome the conventional method's problems (FIGURE 4). These kits are well-suited for users who have a high volume of samples and can accommodate as many as 36 coupons (at 0.125" thickness). The kit components can target the center of features accurately, down to 0.008" (200µm).

Here's how it works. The technician can place as many as six coupons in each sample position. Two indexing pins with a 0.094" diameter hold the samples in place. All these samples are simultaneously ground and polished to target.

This is another option for users seeing smaller target feature sizes, given the electronics industry trend toward miniaturization. The center of features can be accurately targeted, down to 0.004" (100µm). As many as 18 coupons can be accommodated at once, up to a thickness of 0.125". Such kits enable producing accurate microsectioning of coupons within the target requirement. The kit also enables true microstructure at the area of interest. These accessories also benefit from excellent reproducibility, as the result is not dependent on an operator. Every sample maintains the correct orientation and reaches the target area.

## Operation Procedure

**Set dial to zero position.** Set the total grinding distance from the feature of interest to a reference pin on which the sample is mounted. In the standard setup, the distance is set to 0.150". By grinding to diamond stops in the fixture, the perfect target is reached.

Set the diamond stops as accurately as possible to ensure accurate targeting, as verified by a dial gauge. When a calibrated reference pin sets the dial gauge to zero, the target plane is set at the holes' center.

A reference pin of 0.1972" diameter is required for a standard distance of 0.150". Different reference pins can be used for other distances. The calculations for these pins are as follows: distance from reference holes to target holes + 0.047" (half the value of 0.094" diameter index pin).



FIGURE 4. Accessory kits for semiautomatic grinder-polisher equipment.



FIGURE 5. Setting the position of diamond long stop (left) and diamond short stop.



FIGURE 6. Coupons are loaded onto the pins using the pin locator.

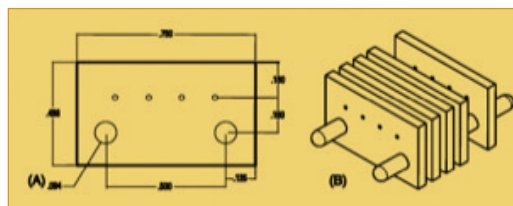


FIGURE 7. A typical coupon design for high-volume specimen preparation (a) and the pinned coupon concept (b).

**Diamond stops setting.** There are six diamond stops on the sample holders in the accessory kits: three "short" and three "long" diamond stops. The long diamond stop aims to set the first grinding step's position, while the short diamond stop sets the second grinding step's position.

The long stop's recommended settings are 0.007" (177.8µm), and the short stop's recommended settings are 0.003" (76.2µm) (FIGURE 5). Adjusting the sample holder fixture's position relative to the dial gauge can set these distances. This adjustment ensures the grinding surface plane will not pass beyond the center and remains above the target plane.

**Coupon pinning.** Mounting these coupons on the pins with a positioning tool holds them firmly in place in the sample holder (FIGURES 6 and 7). The pin loading tool maintains regular spacing. Keep space between each coupon to ensure the mounting media's best penetration.

**Mounting.** The specimen is embedded in a resin mold to enable handling for the operations coming up next. Doing this step right means creating a flat surface on the mold, providing good edge retention, and preventing further damage during grinding. This part of the process could, but should not, physically damage or chemically damage the sample.

Most technicians regard this step of specimen preparation as too routine. However, specimen preparation's effectiveness depends on the mounting components without gaps or air bubbles that could leave critical areas unsupported and unprotected from the mechanical forces of abrasive material removal.

The resins labs use traditionally, like polyesters, can be health hazards on top of the possibility

of producing inferior preparation results. The epoxies take an extremely long time to cure. As a result, recently developed resins offer a quick cure time of under 10 min. and brilliant wetting characteristics.

Before mounting, each coupon is dipped into the liquid part to improve the acrylic material's surface coverage inside the holes by evacuating trapped air from the sample. This procedure is especially important when using smaller hole sizes.

Fill each cavity to the top edge of the coupons with the resin. Cavities should be at an equal height without overfilling, as surplus mounting media may increase grinding times, without any benefit. To ensure an even level of support around the sample holder, the mounting media should fill any empty cavities.

Once cured, remove the mounting plate. The sample holder is then separated, ready for both grinding and polishing (**FIGURE 8**).

Solder joints and plated through-holes have become smaller features that require care to ensure true microstructure is shown and no artifacts are induced during preparation. Proper potting of samples, along with the consumable and equipment choice, can reveal the true microstructure of boards, solder joints, BGAs and plated through-holes.

Labs may use epoxy for critical applications where adhesion to the board surface and filling of fine voids is of great import. Cast mounting can minimize problems to the sample to preserve specimen integrity by avoiding thermal stress. For mounting with epoxy, recently introduced programmable vacuum systems optimize both pore impregnation and edge retention, enabling the resin to penetrate all the specimen's recesses.

System programmability allows technicians to set the number of cycles, vacuum level and time under vacuum. As epoxy mounting involves longer cure times, features and a large sample tray in a large chamber reduce processing time (**FIGURE 9**).

**Grinding/polishing.** Using semiautomatic preparation and multi-sample target grinding equipment can significantly reduce the time spent on this function. An example of the time savings to grind and polish for 18 boards can drop to less than one minute from roughly 20 min. This time savings represents a significant benefit to any high-volume laboratory that processes multiple samples.

The design of the newer grinding and polishing systems enables fast setup, program-

mability and reproducible results. A rinse-and-spin function removes the excess water used to flush debris to prevent cross-contamination.

An accessory enables dispensing diamond and polishing abrasives for different stages in the grinding/polishing process for additional versatility and ease of setup. This accessory can dispense suspension at fixed intervals and configurable rates.

Grinding/polishing for test samples involves:

**Step 1: Coarse grinding.** Using silicon carbide paper, it is possible to grind through polymer-based PCB coupons quickly. The opening step begins with 240-320 grit SiC paper and running water until the long diamond stop is reached.

Change the SiC paper every two minutes and continue grinding until all the diamond stops contact the surface.

Along with testing equipment, the industry has been making improvements in abrasive papers. The newer versions are resistant to water, folding, and tearing; they have improved flexibility and feature a superior surface finish for improved material removal rates.

**Step 2: Fine grinding.** Using 600 grit SiC paper and water, grind until reaching all short diamond stops. Rinse the specimens and holder thoroughly with water.

Backout all three of the short diamond stops by half a turn. There should be a 7 mil or less reading on the dial gauge after step 1, and 3 mils or less following step 2.

**Step 3: Coarse polishing.** Use 3 $\mu$ m diamond suspension paste for a repeatable finish. Evenly apply the paste to a woven, pressed cloth and spray enough lubricant, enabling reapplication of the paste every five to 10 uses. Polish for three minutes, then clean the sample and holder with water. Spray with ethanol and then dry with warm air.

Inspect the prepared surface to confirm the complete removal of SiC scratches during this process.

**Step 4: Fine polishing.** In the final polishing step, apply 0.05 $\mu$ m alumina suspension to a medium napped polishing cloth. Polish for 90 sec. Rinse with running water during the final 15 sec. of the polishing cycle to clean the polished surface and the polishing cloth. Do not over-polish during this step.

Running this step for extra time will cause rounding at the sample's edges, particularly on soft material such as tin-lead coating, which can interfere with accurate measurements.

Upon completion of these steps the sample is ready for inspection.



**FIGURE 8.** Coupons mounted into holder before pouring the resin (a), cured mounts in the mounting assembly (b), and the grinding fixture with the molding plate removed (c).



**FIGURE 9.** Vacuum system loading reduces processing time.



## Conclusion

Semiautomatic preparation, and multi-sample target grinding equipment, can reduce the per-sample processing time. Clearly, for any high-volume laboratory processing multiple samples, these advances represent an enormous benefit.

The upgrades in systems and consumables can result in reproducible targeting of features, reduction of rework, consistency in the finish, and repeatability over time and between operators. In addition, the capability to process multiple sample types with fewer consumables improves quality control while requiring fewer samples to test.

In all cases, an inspection process that yields more accurate results aids in root-cause statistical analysis. Over time, labs can build a profile of detected defects, enabling them to isolate problems on the assembly line to reduce scrap and increase throughput. □

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### Material Gains, continued from pg. 20

responders to restore telephone and Internet services within hours or days, rather than weeks or months. This could save many lives and help reestablish security and well-being more quickly than otherwise possible.

Our technologies have the power to transform lives all

around the world. We need inventors to direct their creativity toward making the benefits available to everyone. It's what will bring us together as a species and help us understand each other and cooperate productively. Connecting people is the way we will find peace and sustainability. □

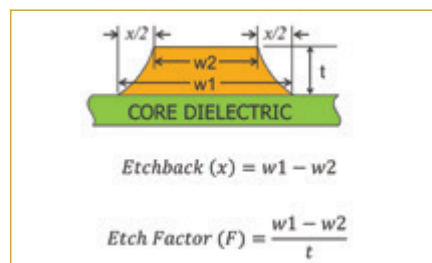
### Material Matters, continued from pg. 22

**Impedance implications.** Let's consider an "average" PCB fabricator, where a 1-oz. stripline layer has 0.5 mils of etchback, and compare the impedance results against a trace where etchback is ignored. In **FIGURE 6**, the left image with the blue border assumes a rectangular trace cross-section. The image on the right includes the 0.5 mils of etchback for a single-ended transmission line targeting 50Ω and a differential pair targeting 100Ω. As you can see, the single-ended impedance difference is 1.25Ω and the differential-impedance difference is about 2.5Ω. Could your design live with such a difference? It depends on a lot of factors, some that you control and some random. You don't directly control Dk variation or copper-thickness variation from nominal, for example, but you can specify impedance at +/-10%. The difference we're show-

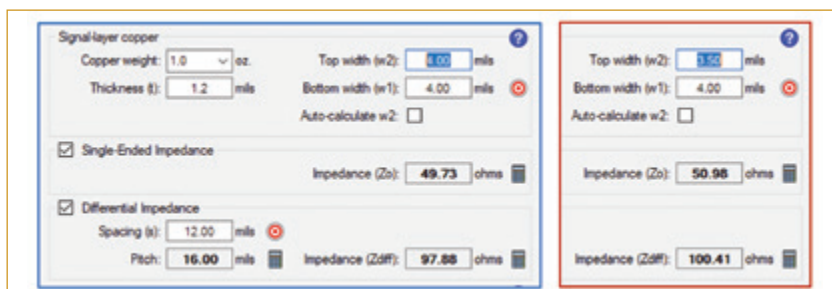
ing here would be stacked on top of Dk variation, copper-thickness variation, and any other variation in fabrication. In short, you're giving up ohms right out of the gate, which is not good design practice. □

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3. Lee Ritchey, *Right the First Time*, vol. 1, 2003.



**FIGURE 5.** Proposed definitions for "etchback" and "etch factor," where x (etchback) is the difference between w1 and w2, and etch factor is defined as the degree of etchback per thickness.



**FIGURE 6.** The left image with the blue border assumes a rectangular trace cross-section. The right image includes 0.5 mils of etchback for a single-ended transmission line targeting 50Ω and a differential pair targeting 100Ω. (Simulated with Z-zero Z-solver, using Mentor's HyperLynx field solver)

# COURAGE in the Face of Covid

As a pandemic crashed the industry, EMS companies responded with vigor and speed. **by MIKE BUETOW**

2020 will be remembered as the year of Covid-19. It hit China first, spurring a national response that included the shutdown of all industrial activities, including manufacturing.

That's no small matter. China produces some 90% of all electronics worldwide. In anticipation of the Chinese New Year, most companies outside China had increased their inventories of raw materials, so the impact on the supply chain wasn't immediately felt. As buffer stocks dwindled, producers in the US and Europe were socked with virus-related shutdowns. Meanwhile, China came back online. So, while materials weren't always where manufacturers needed them, even critical components generally were accessible in relatively short order.

Throughout much of the West, demand for most end-products ground to a halt. Aerospace, especially for commercial jets, and industrial electronics were hit hardest, offset for some by spikes in demand for PCs, tablets and related networking gear as telecommuting for work and school became an overnight worldwide phenomenon.

On the other hand, medical became the top priority for scores of OEMs and supply-chain companies that heretofore had not dipped a toe in that market. As hospital capacities surged with sick in-patients, OEMs scrambled to find designs for much-needed ventilators and other critical medical devices. In turn, EMS companies rose to meet the challenge.

Celestica, for instance, engaged with Valencia's Polytechnic University (UPV) to develop of a new mechanical ventilator that consists of a controlled electrical-mechanical device that maintains the respiratory cycle of critical patients, and tripled production of a portable ultrasound device doctors use to quickly perform lung scans of patients exhibiting symptoms of Covid-19. It also ramped production of printed circuit board assemblies and subassemblies for blood analyzer devices used

in the testing process for Covid-19.

Jabil's Healthcare unit started building everything from Covid-19 test kits to surgical generators and sterilization devices. Likewise, Jabil and Benchmark are producing millions of cartridges for DnaNudge's lab-free CovidNudge test, which delivers results in just over an hour.

Integrated Micro-Electronics Inc. received certification from the Food and Drug Administration (FDA) for its UCL Ventura Flow Generator, a non-invasive ventilatory support in the management of Covid-19 patients.

Benchmark's array of medtech products includes ventilators, portable x-ray units, chest scanning devices, nitric oxide treatment systems, diagnostic equipment, and infusion pumps for temporary hospitals. Additionally, Benchmark manufactured two rapid testing products, one for Covid-19 and one for sepsis, a common condition in infected patients.

Plexus built thousands of critical medical products being used by front-line healthcare workers, ranging from infusion pumps, portable ultrasounds, hospital bed electronics, portable patient monitors, ventilators, mobile x-ray electronics and diagnostic test systems.

NOTE joined forces with Breas Medical, a Swedish developer of ventilators for hospitals and home care.

Key Tronic CEO Craig Gates took to Twitter to tell everyone from Elon Musk to New York Governor Andrew Cuomo to Medtronic that the company was ready and able to make ventilators.

Even Foxconn got in the act. The world's largest ODM joined forces with Medtronic to build ventilators at its controversial new plant in Wisconsin, which has often been maligned in the media because of generous tax breaks the state granted the company.



**FIGURE 1.** DnaNudge's rapid Covid test cartridge, being built by Jabil and Benchmark.

The flurry of medtech activity wasn't restricted to larger players, however. Indeed, some of the largest contributions came from Tier 3 and 4 EMS providers.

Lightspeed Manufacturing retrofitted snorkeling masks with a custom-designed adapter that plugs in a medical-grade anesthesia filter. The company has shipped over 20,000 masks to more than 5,000 medical institutions, all donated at no cost to hospitals and emergency workers.

National Circuit Assembly ramped production for AutoMedx to produce a small, portable ventilator for use

by doctors and laypersons. The spike raised production from 1,000 units a year to 20,000 in just a few months.

This is just a small list of the many, many companies big and small that pitched in. And we would be remiss if we failed to note the hundreds of thousands of workers who overcame any angst over getting infected to show up to work each day to churn out the lifesaving devices. But for them, the global death toll would certainly be much uglier.

Furthermore, although concerns over materials availability were rampant, all in all the supply chain held. The entire industry deserves commendation for its efforts.

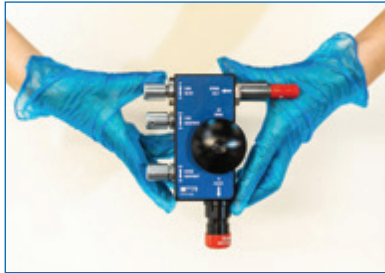
As we head into 2021, we have yet to lick Covid-19, but the responsiveness of the electronics manufacturing services industry to the latest pandemic puts us at relative ease, or at least relaxes some of the anxiety over the sector's disaster management preparedness.

For its creativity and courage in facing down a potentially deadly illness, the EMS Industry is the CIRCUITS ASSEMBLY EMS Company of the Year. □

MIKE BUETOW is editor in chief of PCD&F/ CIRCUITS ASSEMBLY; mbuetow@upmediagroup.com.



**FIGURE 2.** Lightspeed Manufacturing has converted thousands of snorkels into life-saving masks.



**FIGURE 3.** The ULC Ventura was reverse-engineered by academics from a more conventional CPAP device in hours, then quickly licensed and brought to market by IMI.

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# High-Reliability, Fourth-Generation LOW-TEMPERATURE SOLDER Alloys

Results of melting behavior, solder joint formation, tensile strength and high-temperature creep tests.

by MORGANA RIBAS, PH.D., ANIL KUMAR, PRATHAP AUGUSTINE, PRITHA CHOUDHURY, PH.D., AND SIULI SARKAR, PH.D.

There has always been a latent interest in low-temperature solders, as they can 1) potentially reduce material cost by enabling use of cheaper PCBs and components due to the lower processing temperature, 2) promote long-term reliability by reducing exposure to thermal excursion, 3) reduce labor cost, 4) reduce energy cost, and 5) reduce dynamic warpage in sensitive components.

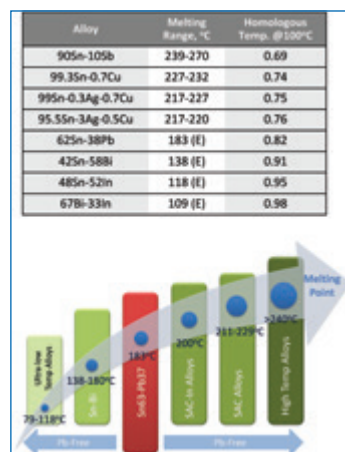
SnPb alloys have been historically used for making joints. In the case of electronics, eutectic 63/37 SnPb was a very good choice, as solder joints could be soldered at relatively low temperatures, considering its melting point at 183°C. Eutectic SnPb also produced solder joints with very good mechanical reliability. The transition to lead-free was mostly a matter of regulatory compliance, and in the early 2000s various lead-free alloys were considered substitutes for eutectic SnPb, including the eutectic 42Sn58Bi alloy.

The 42Sn58Bi alloy was attractive from the point of view of its melting point at 138°C. Almost all the other choices were Sn-based alloys, such as SAC 305, and required higher soldering temperatures. Unlike SAC solders, eutectic SnBi reflows at temperatures lower than eutectic SnPb, so it does not require more expensive materials for PCBs and packages. Concerns

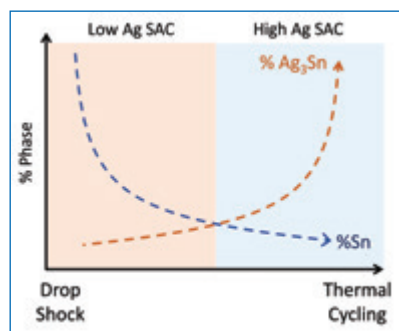
remained over compatibility with packages using SnPb, however, as the residual Pb in combination with the BiSn solder could form 51.5Bi33Pb15.5Sn alloy that melts at 95°C.<sup>1,2</sup> There were also concerns about other drawbacks such as poor drop shock<sup>3,4</sup> and limited thermal cycling performance.<sup>5-7</sup>

Alloys with lower melting points enable lower soldering temperatures, of course. However, soldering at lower temperatures needs to be balanced with thermal and mechanical reliability requirements for a specific application. As packaging and assembly requirements evolve, higher thermal and mechanical reliability have been a strong driver for new solder alloy designs. **FIGURE 1** shows the melting range, or melting point in the case of eutectic alloys, and the homologous temperature at 100°C of various solders. Metals with homologous temperatures above the 0.4-0.6 range creep and will eventually fail due to creep. Among the examples shown here, 90Sn10Sb has the highest liquidus temperature, yet its homologous temperature is within the range expected to fail due to creep. Thus, creep properties need to be considered for selecting the right solder for each electronics assembly application.

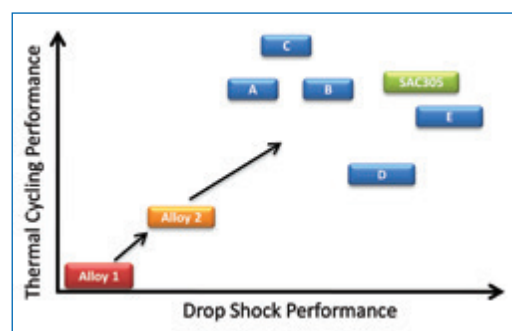
Relative to each other, alloys with lower Ag content have higher drop shock and lower thermal cycling performance than high Ag solders such as SAC 305 and SAC 405.<sup>8-10</sup> In SAC alloys such thermal and mechanical performance is



**FIGURE 1.** Melting range (or melting point in the case of eutectic alloys) and homologous temperature at 100°C of various solders.



**FIGURE 2.** (a) Relative thermal cycling and drop-shock performance of SAC alloys can be predicted based on their silver content,<sup>12-13</sup> while b) LTS performance depends on the individual and combined effect of its multi-additives.





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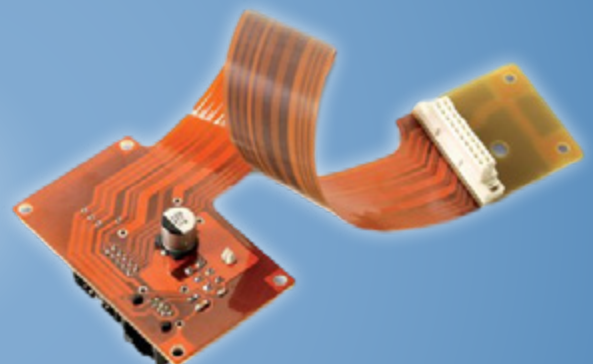
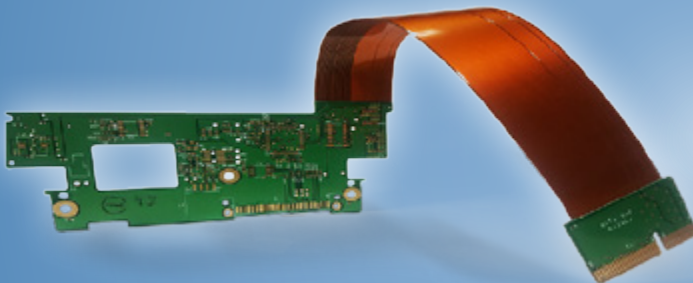
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associated with the amount of  $\text{Ag}_3\text{Sn}$  IMC<sup>10-13</sup>, as shown schematically in **FIGURE 2A**. It is difficult to make a similar type of model for low-temperature alloys, considering the variety of additives and varying bismuth content of the available solders (**FIGURE 2B**). However, it is reasonable to conclude that low-temperature solder performance depends on both the individual and combined effect of its multi-additives.

Dynamic warpage of ultra-thin electronic packages is a serious concern for PoP bottom and PoP memory packages, as they can cause serious soldering defects such as non-wet opens, solder bridging, head on pillow, and non-contact opens.<sup>14-15</sup> Leading semiconductor companies have done extensive research to identify such phenomena and found that the dynamic warpage of such packages can be drastically reduced by limiting the reflow peak temperature to 200°C or lower.<sup>15-20</sup> Reducing dynamic warpage has become the latest and strongest driver for low-temperature soldering, and various investigations have been initiated by materials suppliers and industry consortia, such as iNEMI.<sup>21-29</sup>

This work addresses four alloys representing what can be categorized as low-temperature solders first to fourth generation.

- Alloy 1 is the eutectic 42Sn58Bi.
- Alloy 2 is the eutectic 42Sn58Bi + additives X.
- Alloy 3 is a non-eutectic alloy with 49-51 wt.% Bi plus about 2 wt.% additives.
- Alloy 4 is a near eutectic alloy, having 56-58 wt.% Bi plus about 2 wt.% additives.

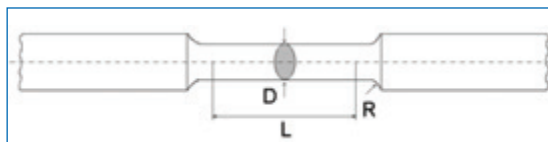
The bulk properties of these alloys are compared with SAC 305 in terms of melting behavior, tensile and creep properties. Their use in heterogeneous solder joints using SAC 305 spheres, and how this can affect solder joint mechanical and thermal properties, is also discussed.

### From First-Gen to Third-Gen LTS

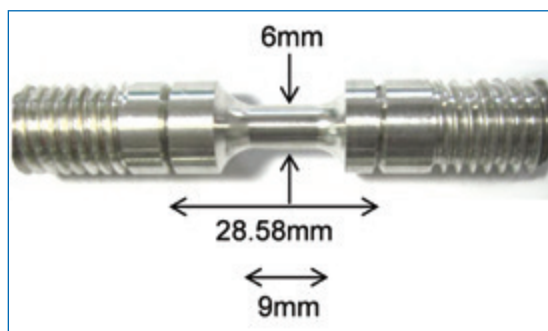
Despite the drawbacks of 42Sn58Bi as a solder, this alloy system is quite interesting, as Bi is one of the few elements forming a solid solution in Sn. It is a binary alloy with one single eutectic composition that melts at 138°C. Moving into the hypoeutectic zone of the SnBi phase diagram, the liquidus temperature increases as the bismuth content decreases. Second-generation LTS alloys include many variations of the eutectic alloy with minor alloying additions. For example, Ag was shown to improve ductility and thermal cycling.<sup>30-31</sup> Lowering the Bi content increases its ductility, and very small additions of Cu were shown to have a further improvement of its elongation.<sup>32</sup>

From the second-generation LTS onward, alloying additions

are used for improving the properties of SnBi alloys to the point where the industry stands now, in which there is a concrete interest to explore these alloys for a variety of applications. Plastic deformation is a top consideration for improving solder joint thermomechanical fatigue resistance. It is caused by the movement of dislocations, which are present in most crystalline materials and could be generically called defects in the atomic structure. Impeding the movement of dislocations can reduce plastic deformation. Known mechanisms are responsible for doing that,



**FIGURE 3.** Specimen geometry used for the tensile tests.



**FIGURE 4.** Specimen used for creep test.

such as solid solution strengthening, in which local stress fields interact with the dislocation, and precipitate hardening, in which precipitates create obstacles to the dislocation movement. Also, grain refinement results in strengthening as the dislocation movement is interrupted by the shorter distance within grain boundaries. Diffusion modifiers can directly or indirectly affect bulk and interfacial intermetallic compound morphology and size. The choice of which alloying element or elements to add depends on their relationship with the alloy system and its resulting properties. Reducing only the Bi content of 42Sn58Bi cannot overcome all its drawbacks. Most common, new solder alloys need to combine multiple

physical metallurgy strategies to overcome this limitation.

These strategies are at the core of the design and development of Alloys 2, 3 and 4, which are discussed here. Alloy 2 has better tensile properties than the 42Sn-58Bi and other second-generation LTS having small additions of Ag.<sup>4</sup> In fact, Alloy 2 also shows a significant improvement of drop-shock performance compared to the 42Sn58Bi and 42Sn57.6Bi0.4Ag.<sup>26</sup>

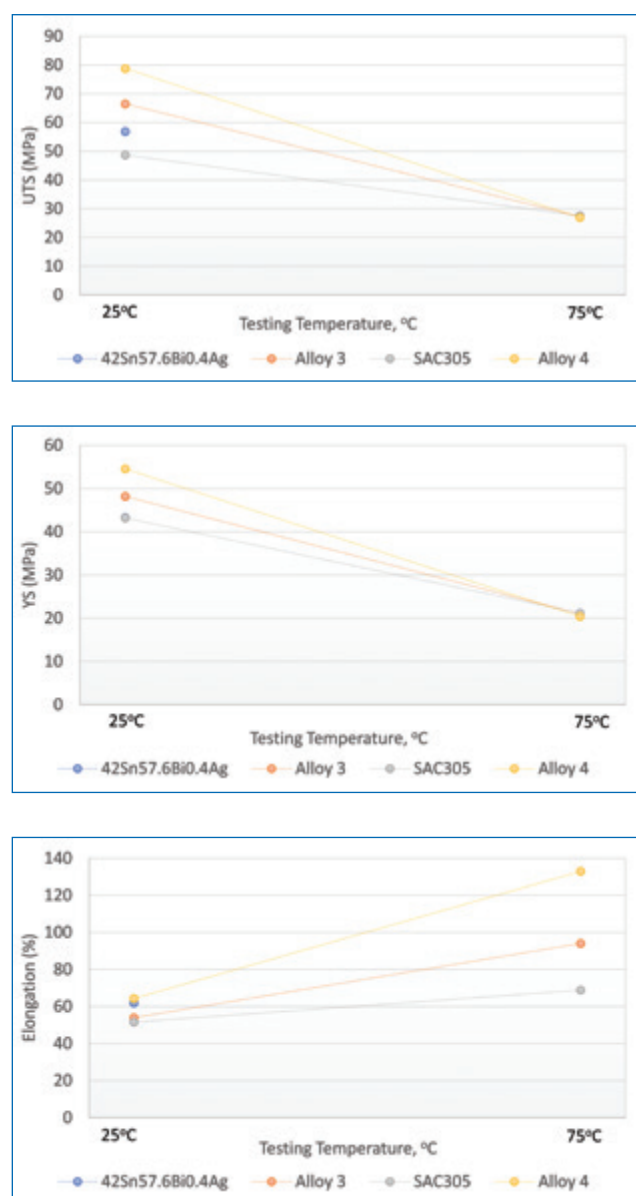
Alloy 3 (third-generation LTS) was developed with more recent requirements of solders in mind that combine lower temperature processing and high mechanical reliability performance. In this case, the alloy design strategy was to increase the concentration of additives above 1 wt.% and reduce the bismuth content. Reducing the bismuth content can increase the elongation under tensile stress, but as seen in the SnBi phase diagram, it also increases its liquidus temperature. If we consider that SMT assemblies are generally reflowed at 25°-30°C above the solder melting point, a SnBi alloy with 35 wt.% Bi would need a reflow profile reaching around 211°C, whereas decreasing the Bi content to 40 wt.% would require a peak reflow temperature around 200°C.<sup>25-26</sup> Although alloys with lower % Bi have higher ductility, this alone is not enough to improve their drop-shock performance to the same level of SAC 305.<sup>4, 25-26</sup>

Increasing the Ag addition from 0.4 to 1 wt.% in the eutectic SnBi results in higher strength, but somehow lower elongation. Further addition of 1 wt.% In on the same alloy has minimal effect on its mechanical properties.<sup>25</sup> Alloy 3 has lower tensile



and yield strength than the other alloys shown, but its yield strength and elongation are similar to SAC 305.<sup>25, 28</sup> The drop-shock characteristic life of Alloy 3/SAC 305 heterogeneous solder joints (i.e., SAC 305 spheres and Alloy 3 solder paste) is around 80% of the SAC 305 in the CTBGA84 solder joints, while the characteristic life of the Alloy 3 homogeneous solder joints matches that of SAC 305.<sup>26-27</sup> Thermal cycling test of the CTBGA84 heterogeneous solder joints shows that after 2,000 cycles, from -40°C (10 min.) to 125°C (10 min.), Alloy 3 has considerably fewer failures than Alloy 1 and is at the same level of SAC 305.<sup>28-29</sup> Cross-sectioning and SEM analysis of these BGAs confirmed these results. For the chip resistors, the SEM images were even more striking, as no cracks were observed in Alloy 3, while many cracks are seen in Alloy 1 and in SAC 305.<sup>28-29</sup>

## Experimental Methodology



**FIGURE 5.** Tensile properties (25° and 75°C) of SAC 305, 42Sn57.6Bi0.4Ag, Alloy 3, and Alloy 4.

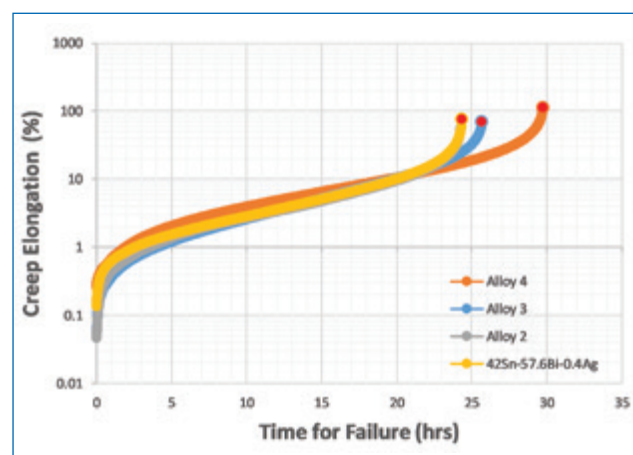
Alloys were prepared using pure metals and/or pre-alloys. Although a detailed composition is not presented here, the presence and quantification of micro-additives is analyzed using ICP-OES, so the comparisons made here refer to the actual intended alloy compositions. The melting behavior was evaluated through differential scanning calorimeter (DSC) per the ASTM E794 standard, using a heating rate of 10°C/ min. Coefficient of thermal expansion (CTE) was measured using a thermal mechanical analyzer according to the RT-500C standard.

Tensile tests were performed using a universal testing machine (UTM). Samples were machined to the shape and dimensions shown in **FIGURE 3**, having 16mm gage length (L), 4.01 mm gage diameter (D), and 3mm shoulder radius (R), per the ASTM E8 standard. Five specimens were tested at each temperature (25 and 75°C) using 10-3mm/s crosshead displacement speed.

Creep tests were performed using round-threaded samples having 9mm gage length and 6mm diameter (per ASTM E8) as shown in **FIGURE 4**. Samples were cleaned with IPA and heat treated for 48 hr. before testing to ensure a uniform microstructure and eliminate any residual strain due to sample machining. Creep tests were performed under constant load (150 N) and temperature (80°C).

The reflow simulator experiments use an IR heater that can simulate the same profiles used in a regular reflow oven. A high-speed camera captures and records video images in real time. Real-time images of solder joints using Alloy 3 solder paste were obtained using time above liquidus (TAL) 60 seconds, and peak temperature was 185°-190°C. Real-time images of solder joints using Alloy 4 solder paste were obtained using the same temperature profile, but the peak temperature was 175°C. SAC 305 was reflowed using a 245°C peak temperature. In all examples shown here, the solder pastes use type 4 solder powder.

Cross-sectioning and microstructural analysis were performed using a scanning electron microscope (SEM), and the elemental composition was semi-qualitatively identified using energy dispersive x-ray spectroscopy (EDS). Solder joint samples shown here use a CTBGA84 component with 12 mil SAC 305 balls assembled on a test vehicle with OSP surface finish.



**FIGURE 6.** Creep curves for 42Sn-57.6Bi-0.4Ag, Alloy 2, Alloy 3, and Alloy 4. Note: Data collected at 80°C and 150N load.

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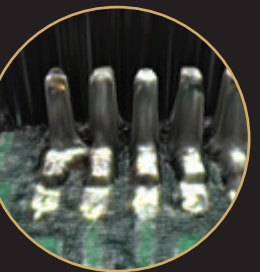
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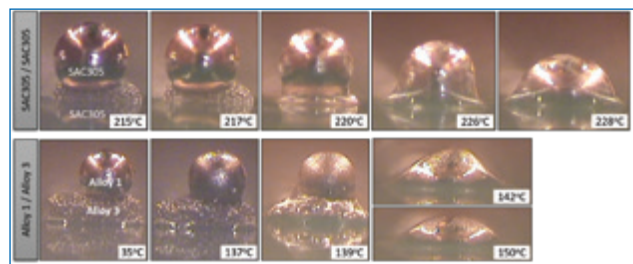
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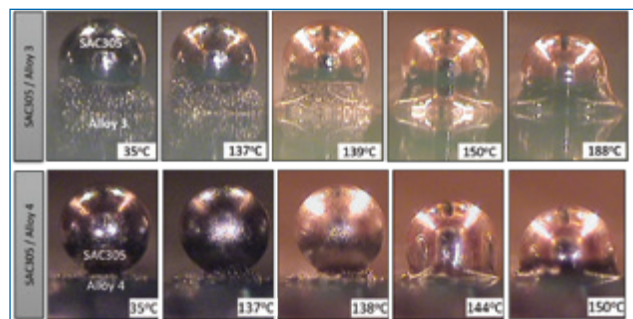
## Results and Discussion

As low-temperature solders evolved from their first to third generation, they used a variety of additives and varying bismuth content. An alloy may have higher drop shock and lower thermal cycling, while another alloy may have higher thermal cycling and lower drop-shock performance. Thus, it seems clear LTS aiming to match or coming as close as possible to the SAC 305 thermal and mechanical performance will be multicomponent. That is the case of Alloy 3, as well as Alloy 4.

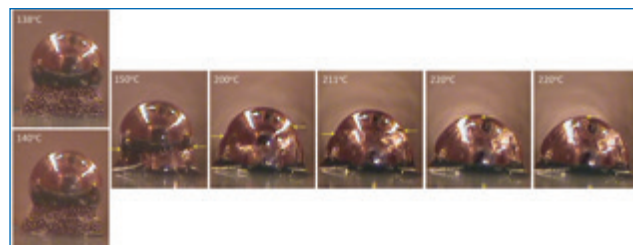
**Mechanical properties.** The results of the tensile tests at 25 and 75°C for the SAC 305, 42Sn57.6Bi0.4Ag, Alloy 3, and Alloy 4 are shown in Figure 5. Room-temperature ultimate tensile stress (UTS) of all three SnBi alloys is higher than SAC 305, as shown in **FIGURE 5A**. This is mostly a contribution from their increased Bi content. Alloy 4 has the highest tensile strength, followed by Alloy 3, 42Sn-57.6Bi-0.4Ag and SAC



**FIGURE 7.** Homogeneous SAC 305 and homogeneous LTS solder joint formation.



**FIGURE 8.** Heterogeneous (or hybrid) solder joints of SAC 305/Alloy 3 and SAC 305/Alloy 4 are formed below SAC 305 liquidus temperature.



**FIGURE 9.** Heterogeneous SAC 305/Alloy 4 solder joints reflowed at 245°C peak temperature, showing ball collapse at 150°C and SAC 305 melting at 220°C (indicated by the yellow arrows as it progresses).

305. At 75°C the 42Sn57.6Bi0.4Ag samples were deformed by the grips during testing due to their low melting temperature and poor mechanical properties and consequently could not be tested. There were no issues testing Alloy 3 and Alloy 4, and their ultimate tensile strength at 75°C was found to be identical to SAC 305. The values of yield stress (YS) follow a similar trend, as shown in **FIGURE 5B**. Similarly, Alloy 3, Alloy 4 and SAC 305 have the same yield strength at 75°C. Although the elongation of LTS alloys is generally similar or slightly higher than SAC 305, at 75°C Alloy 3 and Alloy 4 have a considerably higher elongation, as shown in **FIGURE 5C**. Alloy 4, in particular, shows very good results and at 75°C has the same tensile strength as SAC 305 and twice its elongation.

Electronics devices generally endure longer periods in service at temperatures that are significant fractions of the Sn-based solder melting temperatures. In other words, solder alloys have higher homologous temperatures while in service, ultimately resulting in deformation due to creep. In previous works, it was shown high-reliability solder alloys with superior high-temperature creep properties also have improved thermal cycling performance.<sup>33-35</sup> High-temperature creep tests provide relevant information about how long it takes for each alloy to fail under certain thermal and mechanical stresses. In this way, it can also provide insights on the solder joint thermal cycling performance.

A typical creep curve can be divided into three portions, generally called primary, secondary, and tertiary creep. After an initial instantaneous deformation (mostly elastic), the strain rate decreases (primary creep) until it reaches a steady state (secondary creep), before it starts rapidly increasing again until the sample rupture (tertiary creep). The graph shown in **FIGURE 6** compares the creep curves of 42Sn57.6Bi0.4Ag, Alloy 2, Alloy 3, and Alloy 4, under the same thermal (80°C) and mechanical (150N) loads. The two second-generation LTS alloys have similar creep properties, while Alloy 3 samples take more time to fail (i.e., higher creep strength). Alloy 4 has the best creep properties among these alloys, as it results in longer time to failure and higher creep elongation.

**Thermal properties.** **TABLE 1** presents the solidus temperature ( $T_s$ ), liquidus temperature ( $T_L$ ), and coefficient of thermal expansion (CTE) of first- to fourth-generation LTS alloys. The additives used in any of Alloys 2, 3 and 4 do not affect the solidus temperature, while the liquidus temperature is highly dependent on the Bi content of each alloy. The liquidus temperature of Alloy 2 is basically the same as Alloy 1, as both are eutectic

**TABLE 1.** Solidus Temperature ( $T_s$ ), Liquidus Temperature ( $T_L$ ), and CTE

Alloy	$T_s$ , °C	$T_L$ , °C	CTE, ppm/°C
1	138	140	18
2	138	141	18
3	138	151	19.5
4	138	146	19
SAC 305	217	220	22.5



alloys. It is also important to note these are not ultra-pure alloys but actual solders that have some degree of impurities allowed by industry standards. In this way, although Alloy 1 has a eutectic composition, there is a small difference between its solidus and liquidus temperatures. The liquidus temperature of Alloy 3 is 10°-11°C higher than the eutectic Alloys 1 and 2, and about 5°-6°C higher than Alloy 4.

The materials forming the solder joint – the package, solder, interfacial intermetallic layer, and substrate – have different coefficients of thermal expansion. For example, the CTE of copper, FR-4 and the alumina substrate of a typical chip resistor are 18, 14, and 7 ppm/°C, respectively.<sup>36</sup> As the assembled parts are cycled between cold and hot zones, these materials expand and contract at different rates, generating shear stresses at the interfaces and potentially leading to thermal-mechanical fatigue.<sup>37</sup> This phenomenon is generally called CTE mismatch, and it is generally accepted solder alloys should try to minimize it. The column on the right shows the CTE of Alloys 1 to 4 and compares it with SAC 305. The low-temperature solders have CTE between 18 and 19.5 ppm/°C, which is a little lower than SAC 305 and well within what is expected for a solder alloy.

**Homogeneous and heterogeneous solder joints.** Before moving from the bulk alloy properties to solder joint properties, it is important to understand how the melting behavior of the LTS alloys affects the formation of homogeneous and heterogeneous solder joints. Usually, the liquidus temperature of the alloy is used to define the soldering temperature or other reflow parameters (e.g., TAL). However, further investigation was needed in the case of heterogeneous solder joints.

**FIGURE 7** shows two examples of homogeneous solder joints. The sequence on top shows a SAC 305 ball with SAC 305 paste, reflowed using a typical SAC 305 profile with peak temperature at 245°C. As expected, the paste starts melting at 217°C and is completely molten at 220°C. There is a partial ball collapse around 226°C, when the ball has had a certain amount of melting, and the final ball collapses at 228°C. The final shape of the solder joint will depend on the size of the ball and amount of paste, but from these images one can understand that a certain time is required at temperatures above the liquidus for a proper solder joint formation. The second sequence (at the bottom) has Alloy 1 as the sphere and

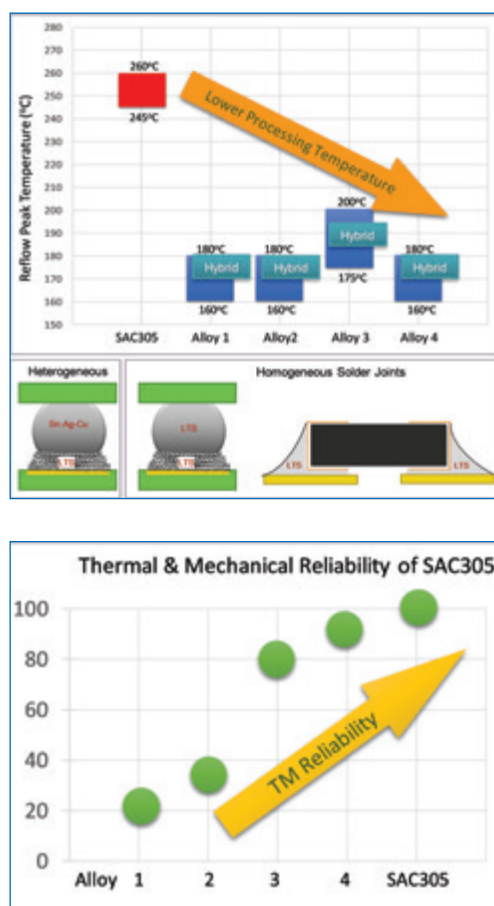
Alloy 3 as the solder paste. The melting of the solder paste starts above the solidus temperature, but it is mostly concluded at a temperature lower than the liquidus of the ball. In this case, the full collapse of the ball happens once it reaches the liquidus temperature of Alloy 3.

**FIGURE 8** shows two examples of heterogeneous solder joints. The sequence on top shows the joint formed using SAC 305 ball and Alloy 3 solder paste. Alloy 3 solder paste starts melting at 139°C and is fully molten at 150°C. This reflow profile had a peak temperature of 190°C, which is much below the SAC 305 melting range. However, there is a localized melt at the Alloy 3 and SAC 305 interface, which results in a partial ball collapse between 185 and 190°C. Also, in Figure 8, the example at the bottom shows the formation of a joint using SAC 305 ball and Alloy 4 solder paste. Melting of the solder paste starts at 138°C and is completed at 144°C. In these images, it is easier to see how the SAC 305 ball reaches its final collapse at 150°C. In both cases the solder joints are formed below the SAC 305 liquidus temperature.

**FIGURE 9** shows the heterogeneous solder joint formed from SAC 305 ball and Alloy 4 solder paste, but this time reflowed at 245°C peak temperature, i.e., the reflow profile used for SAC 305. This sequence of images shows the progressive melting of the SAC 305/Alloy 4 solder, in which the melting of the SAC 305 solder ball is indicated by the yellow arrows. The ball collapses at 150°C, as shown in Figure 8, and SAC 305 is completely molten at 220°C.

From the examples shown above, it is also clear that heterogeneous and homogeneous solder joints have different reflow temperature requirements. **FIGURE 10A** shows the recommended reflow temperature processing window for Alloys 1 to 4 homogeneous and heterogeneous solder joints. The SnBi

alloys shown here (Alloy 1 to Alloy 4) can be reflowed at temperatures below 200°C and as low as 160°C, which is significantly lower than the SAC 305 usual 245°C peak. However, the SAC 305 ball collapse in heterogeneous solder joints requires temperatures on the higher side of this range. Besides lower processing temperature, new LTS solders need to be as close as possible to the thermal and mechanical reliability of SAC 305. As shown schematically in **FIGURE 10B**, four generations of SnBi solder evolution resulted in achieving lower processing temperature and further enhancements in thermal and mechanical reliability.



**FIGURE 10.** (a) Reflow temperature processing window for heterogeneous (or hybrid) and homogeneous solder joints, and (b) thermal and mechanical reliability of Alloys 1-4 with respect to SAC 305.

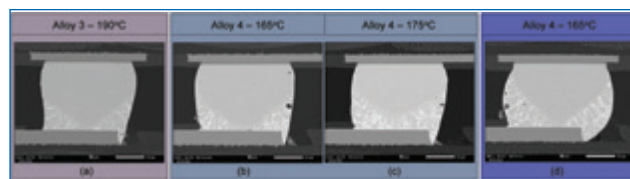
The progressive melting from the bottom to the top of the solder joint, as shown in Figures 8 and 9, can also be visualized through their cross-sections. One such example is presented in **FIGURE 11**. As the SnBi phase melts, it generates a localized change of melting behavior at the interface with the SAC 305. Another thing to consider when optimizing the reflow profile of these solder joints is the level of what is called bismuth mixing.<sup>18</sup> This can vary, depending on the LTS alloy, its Bi content, melting behavior, and perhaps on how easily it is for the LTS alloy to diffuse into the SAC 305. For example, **FIGURE 11B** and **C** show the effect of the reflow peak temperature on the degree of mixing, i.e., how much the Bi (indicated by the light grey microstructure) moves toward the package. From the discussion above, size of the spheres and the amount of solder paste deposit also need to be considered when defining processing temperature and reflow parameters.

## Conclusions and Future Work

A fourth-generation SnBi solder alloy was introduced, and its performance was compared with previous SnBi solders and SAC 305. Key findings are:

- Alloy 4 shows improved tensile and creep properties. At 75°C, Alloy 4 matches SAC 305 ultimate tensile strength and has twice its elongation. Among the LTS alloys evaluated (generation 1 to 3) at 80°C, Alloy 4 has the highest creep strength and elongation.
- Alloy 4 has good solder joint formation at lower reflow peak temperatures. For example, heterogeneous SAC 305/Alloy 4 solder joints can be reflowed as low as 165°C.
- Multicomponent SnBi solder alloys, as in the examples shown, facilitate achieving lower processing temperature, while maintaining thermal and mechanical performance.

Future work will include the effect of reflow character-



**FIGURE 11.** Examples of solder joints processed under various conditions.

istics, viz., time above liquidus (TAL) and peak temperature, on the drop-shock performance of heterogeneous SAC 305/Alloy 4 LTS solder joints. Using these optimized conditions, a comprehensive evaluation of Alloy 4 solder joints, including performance during drop shock, thermal cycling, and thermal shock tests, shear strength measurements and microscopic analysis will also be presented. □

## Acknowledgments

We thank our colleagues Harish Shet, Divya Kosuri, Raghu Raj Rangaraju, Vikas Patil, V. Ramakrishna, and Paul Salerno for their help and support. Special thanks to Harish Siddappa for his help running the reflow simulator experiments.

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# In MEMORIAM

A look back at friends and colleagues who left us in 2020.

**Frances “Fran” Allen**, 88, computing pioneer, first female IBM Fellow, Turing Award winner.

**Preston Averette**, 71, founder and owner of Photo Chemical Systems.

**Danny Carr**, 65, CAM software engineer and founder of Everything PCB.

**Chen Sheng-wei (陳昇偉)**, 44, Taiwan Artificial Intelligence Academy CEO who helped bring AI to PCB CAD.

**Arvelee Church**, 84, Martin-Marietta Aerospace soldering instructor.

**Julian Coates**, 62, marketing executive with Valor.

**Karl Dietz, Ph.D.**, PCB materials expert at DuPont and prolific author.

Undisclosed Foxconn worker.

**Patty A. Houston**, 64, circuit board department worker, General Electric Medical Systems.

**Steve Hughes**, 60, Stone Mountain Tool manager and SMTA chapter president.

**George Floyd Klaus**, 89, manufacturing engineer at IBM, Pemstar, Brady Manufacturing, and Benchmark Electronics.

**Ronald Scott Laugherty**, 51, ex computer programmer, Jabil.

**Lee Kun-Hee**, 78, Samsung chairman for more than 20 years.

**John Lynch**, 77, former CEO of Pye Irl, the radio electronics manufacturer.

**Mary Jo Mai**, 75, circuit board inspector, B.E.I.

**Virginia “Jenny” Day McClure**, 82, ex circuit board engineer, General Motors.

**James D. Meindl, Ph.D.**, 87, founding director of Stanford’s Integrated Circuits Laboratory, where he developed low-power ICs and sensors.

**Eugene U. Merkel**, 70, spent 40 years at Kimball Electronics as a test engineer.

**Ruth W. Nafis**, 78, ex printed circuit tester, RCA Corp.

**Warren Lloyd Pepper**, 69, ex production supervisor, Benchmark Electronics.

**Allen F. Rosenthal**, 77, worked at Bureau of Engraving for 41 years.

**Irene Elizabeth Schindler**, 90, ex circuit board assembly operator, Collins Radio.

**Ron E. Sinclair**, 90, ex Control Data and Chippewa Falls Laboratories engineer, held patents for printed circuit board design.

**George Michael Sousa**, 87, founder of Circuit Service, a printed circuit fabricator.

**Steve Stiller**, 65, owner, Midwest Production Specialists and SMTA chapter president.

**Yoshio Tateishi**, 80, ex-president of Omron.

**Wayne A. Weinsheimer**, 78, electronics engineer who owned Professional Assembly & Mfg. Co., an electronics assembly business in Ocala, FL.

**Evelyn Carson White**, 91, ex printed circuit technician, Packard Electric.



COMPUTER MAVEN  
Allen



METALLIZATION MAN  
Dietz



AI GENIUS  
Sheng-wei



OMRON VISIONARY  
Tateishi



SAMSUNG LEADER  
Kun-Hee



IC MASTER  
Meindl



# Evaluating the Risk and Reward of Statistical Analysis

Questions to ask before action is taken.

**MOST WHO PERFORM** statistical analyses that guide organizations to solve problems do not have advanced degrees in statistics. We've attended classes at university, engaged in varying levels of Six Sigma training, or conducted self-study.

But I think it is safe to say we all have learned that statistically evaluating a set of data is complicated and rife with uncertainty. We choose among many possible statistical tools, and numbers "pop" out telling us if our hypothesis is correct. From those data, we proceed to either take an action or not take an action, depending on the statistical results.

Yet how many finish an analysis and wonder what if it is wrong? Did I have enough data? Did I choose the proper statistical tool? Do I even know the proper statistical tool? Arghh! (I suspect doctors of statistical science also have "arghh" moments.)

Most of us in decision-making roles that require analysis of data to determine choices are cautious and risk-averse. But we had our training. My Anova said part A is better than part B, so why ask more questions?

I suggest that after any statistical analysis and before taking an action based on that analysis, we ask two more questions:

- What is my confidence I am right?
- What is my risk of being wrong?

And I don't mean the statistical definitions of "risk" and "confidence." I mean sit back and take a broad overview of the data, where they came from, and how you evaluated them. How strongly do you feel the results are true? Then ask yourself, What is the impact on the customer if my analysis is wrong?

Then you can decide what to do. But how?

I came up with a simple chart to guide the action to take (**FIGURE 1**). I don't know whether this is original, but here you go.

Let's look at each box in a little more detail.

**1. Confidence of being right is HIGH, risk of being wrong is LOW (green quadrant).** You've done your analyses. You've used multiple tools, did your "Practical/Graphical/Analytical" analysis and feel very

good you've found something significant and the benefits are measurable. You find the cost to implement is acceptable, and after some thought and study you realize if you are wrong, the implications to the customer are minimal. You recommend doing it.

**2. Confidence of being right is HIGH, risk of being wrong is HIGH (blue quadrant).** You've done your analyses. You've used multiple tools, did your "Practical/Graphical/Analytical" analysis, and you feel very good you've found something significant and the benefits are measurable. You find the cost to implement is very high, however, or the effect on the customer if you are wrong is high.

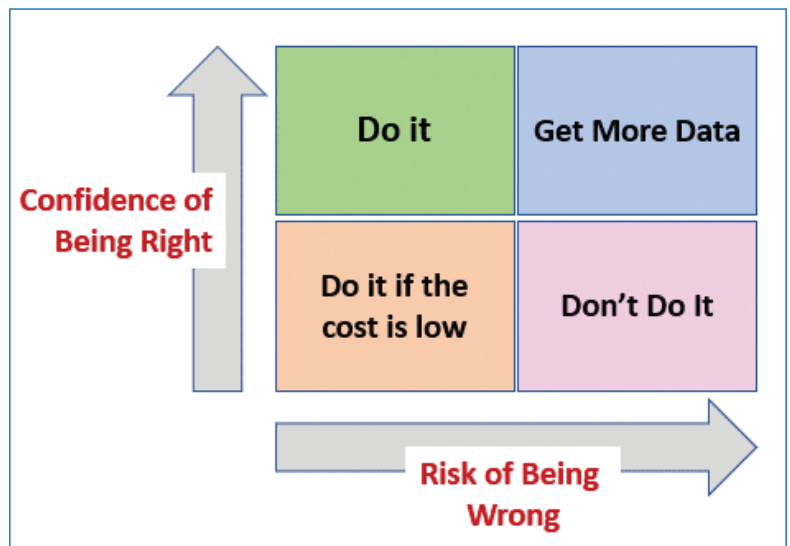
Maybe wait and collect more data. Even if you are fairly certain about your results, more data might help convince management, your customer (and you).

**3. Confidence of being right is LOW, risk of being wrong is LOW (tan quadrant).** You've done your analyses. You've used multiple tools, and did your "Practical/Graphical/Analytical" analysis. But you are still not certain if you've found something significant, and you are not certain the benefits are measurable. However, you find the cost to implement is acceptable, and after some thought and study you realize that even if you are wrong, the implications to the customer are minimal but the benefits could be positive.

So, you can decide to make the change. After all, the risk of being wrong is low and cost to implement

*continued on pg. 42*

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# Successful Printing, Even When the Walls Close In

For 01005 parts, some apertures are better than others.

**CONTINUOUS REDUCTION IN** component size has been at the forefront of electronics product innovation, assembly process development and the industry conversation for years. Readers will no doubt recall the papers presented, tools developed, and processes modified to accommodate the “coming soon” metric 03015 and 0201 components. That preparation is essential. In my opinion, however, it is more likely than not that widespread use of these ultra-small chips is far in the future; it will come, but probably not in the next generation.

Another reality presents, perhaps, a more immediate challenge: increasing component density beyond current norms. Realistically, for next-generation mobile phones and wearables, the primary consumers of the most miniaturized components, board designs will continue to incorporate the 01005 chip (metric 0402). There are a gracious plenty of reasons for this, not the least of which are cost and component availability. The challenge for product designers is how to get the most function from chips that may be larger than they would prefer. What’s the solution? Squeeze the 01005s closer together, of course!

High component density is already demanding. Today, the prevailing dimension for the component to component gap (from the edge of one component to the edge of the adjacent component) is 130 $\mu$ m to 150 $\mu$ m. Assuming a 130 $\mu$ m gap in total, each of the 01005s has a keep-out envelope of 65 $\mu$ m. To prevent bridging defects, that envelope must remain intact through printing, placement and reflow. Paste on pad must be precise during stencil printing. Placement force control is essential to avoid material being pushed out beyond the dimensional envelope. The reflow process cannot result in material hot slump. With tight control, current processes are meeting these conditions in high volume. However, the component

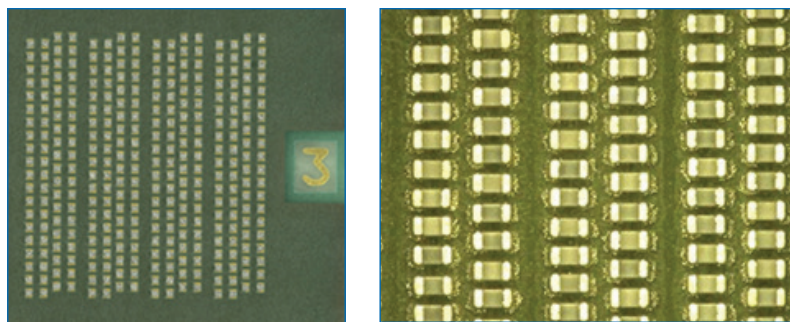
envelope is shrinking as handheld designs move to increase function while maintaining use of 01005s, meaning more 01005s on the PCB.

According to technology roadmaps, the component gap will soon reduce to at least 100 $\mu$ m, with a longer-term goal of 50 $\mu$ m. With the surrounding 01005 envelope effectively decreased to 100 $\mu$ m in the near term, and soon approaching 75 $\mu$ m, any deviation in the printing, placement or reflow process that crosses a dimension smaller than a human hair may result in a bridge. Frightening as this may sound, the reality is that printing with 75 $\mu$ m gaps has been achieved with other processes, so we know it’s possible. Printing, though, is not the end of the story; other processes within the assembly operation can violate this barrier if not in extreme control. To accommodate for placement and reflow tolerances, the logical assumption is to reduce solder paste material volume during printing, which would lessen the likelihood of potential issues downstream. With the appropriate stencil thickness and aperture dimension, print volume can be reduced, but this must be done holistically with process balance in mind so we don’t create more problems than we solve.

Our company has studied approaches to maintaining printing area ratio rules, while successfully reducing paste volume on 01005 pads with component gaps of 75 $\mu$ m – or 37.5 $\mu$ m envelopes per component. Using a 0.60 area ratio rule, which is considered acceptable for fine-feature printing, with a 60 $\mu$ m-thick stencil, the aim was to reduce the aperture size to optimize the paste volume and protect against potential defects downstream. Of course, reducing aperture size may not be enough on its own. As discussed in previous columns, the shape of the aperture also plays a role in volume and, potentially, in paste release efficiency. What our analysis revealed was two aperture archi-

tectures are delivering success in maintaining area ratio rules while producing sufficient material volume. Using an ASM test board with 01005s and a 75 $\mu$ m component gap (**FIGURE 1**), the home plate and obround (**FIGURE 2**) aperture shapes both resulted in a 2.0 Cpk print process. Placement and reflow evaluation, though still ongoing, have shown equally good results.

While the 01005 compo-



**FIGURE 1.** Wide and closeup views of ASM 01005 test board, component gaps of 75 $\mu$ m.

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nent has been part of technology designs for some time, and successfully manufactured in high volume, the ever-shrinking gap between these small chips is a new hurdle. Yes, my friends, the walls do indeed feel like they are closing in. As with most challenges in our exceptionally dynamic industry, however, we are already designing solutions to ensure continued high-yield results. □



FIGURE 2. Obround aperture design.

*Getting Lean, continued from pg. 40*

is also low. In parallel, you might decide to find someone more experienced than you to check your work and see if they agree or if they can suggest other ways to analyze the data. Of course, doing nothing, collecting more data, or doing more research are also options.

**4. Confidence of being right is LOW, risk of being wrong is HIGH (red quadrant).** You've done your analyses. You've used multiple tools, did your "Practical/Graphical/Analytical" analysis. But you are still not certain if you've found something significant. Maybe there's uncertainty that the tools you used apply to this data set. Maybe you are uncertain the data were collected properly. Or maybe you don't know if you have enough data. You also see the cost to implement is very high, or the effect on the customer if you are wrong is high.

You don't do it. You might return to this sometime if more data are collected or if something changes, or you might decide to find someone more experienced than you to check your work and see if they have suggestions on how to become more confident. □

## DEFECT OF THE MONTH

### Component Pin Float Issues

When through-hole connectors move during soldering, damage to the nozzle ensues.

**THIS MONTH WE** look at through-hole connectors and component pin float. All connector pins should be held in place by the body molding and not move during soldering. The connector should not be used outside of its specification. Suppliers typically define the temperature and time the pins and body of the part are exposed to a specific peak temperature. It is the designer's job to ensure the correct parts are defined for the process. It is the purchasing department's job to ensure the correct parts are ordered.

In the images shown, the pins in the connector have floated down. This happens easily during soldering or rework. In an automated process, if the pins drop down 1 to 2mm below the board in selective or wave soldering, they can cause damage. Pins can contact the solder nozzle or wave former, which will jam the machine. Using low-temperature solder with a lower specification connector will work fine, but consider the rework temperatures if parts must be removed.

We have presented live process defect clinics at exhibitions all over the world. Many of our Defect of the Month videos are available online at [youtube.com/user/mrbobwillis](https://www.youtube.com/user/mrbobwillis). □

#### BOB WILLIS

is a process engineering consultant; bob@bobwillis.co.uk. His column appears monthly.



FIGURE 1. Connector pins that "float down" too far can damage soldering equipment.



# Recognition for INNOVATION

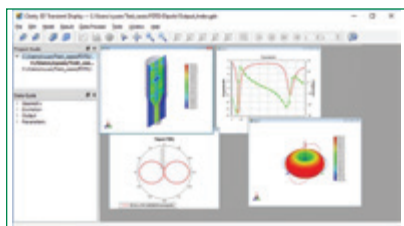
A glowing lightbulb is held by a white-gloved hand on a silver tray. The lightbulb is illuminated from within, casting a warm glow. The background is a neutral, light gray.

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PRINTED CIRCUIT  
DESIGN & FAB **CIRCUITS  
ASSEMBLY**

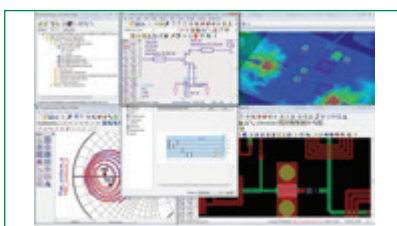


## CADENCE CLARITY 3D TRANSIENT SOLVER

Clarity 3D Transient Solver system-level simulation solves EMI system design issues up to 10x faster than legacy 3-D field solvers. Parallel matrix solver technology reportedly handles workload levels that previously required anechoic test chambers to test prototypes for EMC compliance. Performs large-scale simulations when designing interconnects for PCBs, IC packages, and SoC designs within mechanical enclosure.

Cadence

[cadence.com](http://cadence.com)



## KEYSIGHT PATHWAVE 2021

PathWave advanced design system software 2021 now comes with design cloud simulation services. Reduces simulation time, increases simulation test coverage and provides access to scalable hardware resources in the cloud. Can perform compute-intensive electromagnetic simulations with on-premise clusters or scalable cloud hardware and tackle large electromagnetic simulations. Runs signal acquisition and measurement in parallel, rather than in series.

Keysight Technologies

[keysight.com](http://keysight.com)



## MACDERMID ALPHA MACUSPEC VF-TH 300

MacuSpec VF-TH 300 VF-TH series electroplating is for processes used in mSAP HDI manufacturing. Is a single-step pattern plating process for simultaneous copper filling of blind microvias and PTHs, while providing controlled trace profiles in mSAP applications. Electrolytic copper layer is naturally resistant to V-pitting.

MacDermid Alpha

[MacDermidAlpha.com](http://MacDermidAlpha.com)

## OTHERS OF NOTE

### TELEDYNE LECROY DDR5 DEBUG TOOLKIT

DDR5 Debug Toolkit is for SDA 8 Zi-B and LabMaster 10Zi-A oscilloscopes. Now supports DDR5/LPDDR5 for test, analysis and debug of DDR design cycle. DDR/LPDDR5 JEDEC specifications JESD79-5 and JESD209-5A feature faster rates of up to 6400 Mb/s. Supported design cycle includes automatic read/write burst separation; burst data jitter analysis; eye diagram mask tests; DDR-specific measurement parameters; and integration with HDA-125 high-speed digital analyzer for command bus analysis.

Teledyne LeCroy

[teledynelcroy.com/ddr/](http://teledynelcroy.com/ddr/)

### CORELIS SCANEXPRESS V. 9.8.0

ScanExpress v.9.8.0 boundary scan software includes optional memory test diagnostics with automated analysis. Processor-controlled functional test results are diagnosed down to the net-and-pin level, even on BGAs where physical debug and test access is limited. Processor-specific memory tests include multiple memory standards, including DDR and GDDR.

Corelis

[corelis.com](http://corelis.com)

### VENTEC TEC-SPEED 20.0 VT-870 H348

Tec-Speed 20.0 VT-870 H348 TCR laminate is available in 1/2-oz- and 1oz-thick foil with resistivity values of 25, 50 and 100Ω/sq. Tec-Speed 20.0 glass-reinforced hydrocarbon and ceramic laminate with thin-film resistor material is now available with Ticer TCR NiCr thin-film resistor foil as a service option. For use in aerospace and defense, radar, control circuits, sensor technologies, wireless communications, MEMS microphones/sensors/motors and medical diagnostic applications.

Ventec

[ventecclimates.com](http://ventecclimates.com)

### NIPPON MEKTRON MPI FPC

Modified-PI FPC is for high-speed transmission applications in mass production, in addition to liquid crystal polymer base flex circuits. Transmission properties are similar to LCP FPC, with higher resistance to bending and heat. Complies with serial transmission standards like USB4.0 or PCI Express.

Nippon Mektron

[mektron.co.jp](http://mektron.co.jp)

### HIROSE IX60G CAT.6A

IX60G series horizontal mount PCB connector supports space-constrained applications that require Cat.6a Ethernet cabling. Has reduced mounting requirements. Is compliant to IEC PAS 61076-3-124. Offers low-inductance, high EMC resistance and superior EMI shielding to deliver data transmission. Vibration-resistant connector. Comes in upright right angle, horizontal right angle, and vertical mount options.

Hirose

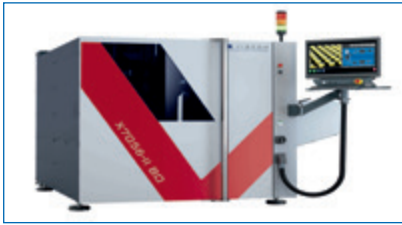
[hirose.com](http://hirose.com)

### UCAMCO IAMCAM

Iamcam is a web-based client/server software for automated PCB frontend workflows. Can be integrated with third-party systems. Compatible with incumbent CAM system.

Ucamco

[ucamco.com](http://ucamco.com)



## VISCOM X7056-II BO

X7056-II BO inline x-ray optically and radiographically inspects bond wires, including enclosed ones, and concealed solder joints beneath chips. Inspects tapes and wires, and soldering quality of dies. Detects opens, concealed connection points, and surface soldering voids. Library contains inspection patterns for die bonds, ball-wedge, wedge-wedge and security bonds.

Viscom

[viscom.com](http://viscom.com)


## INOVAXE SR100E

SR100E parts replenishment rack operates on the production line next to pick-and-place machines to facilitate efficient feeder replenishment. Handles 7", 10", 13", and 15" reels of various widths, along with a work surface for various tasks like tape splicing and feeder loading. Can store splicing tools and materials and install splicing fixtures.

Inovaxe

[inovaxe.com](http://inovaxe.com)


## VITROX V310I

V310i 3-D SPI has warpage compensation, auto pads and component learning. Handles boards weighing up to 7kg and 510mm x 510mm in size in single-lane mode or 460mm x 325mm in dual lane.

ViTrox Technologies

[vitrox.com](http://vitrox.com)

## OTHERS OF NOTE

### HENKEL BERGQUIST GAP PAD TGP 12000ULM

Bergquist Gap Pad TGP 12000ULM thermal interface material is for high-power-density designs such as hyperscale and cloud-scale data centers and 5G telecom infrastructures. Combines thermal conductivity of 12.0W/m-K with soft, conforming properties to ensure wet-out at interface for optimized thermal transfer and low assembly stress. Conforms to rough or irregular surfaces. Stores at room temp.

Henkel Adhesive Technologies

[henkel.com/brands-and-businesses/adhesive-technologies](http://henkel.com/brands-and-businesses/adhesive-technologies)

### EMIL OTTO GSP 2633/RX, GSP 2933/RX

GSP 2633/RX and GSP 2933/RX alcohol-based no-clean fluxes have 12-month shelf life. GSP-2633/RX, GSP-2633/RX/OVAO, GSP-2933/RX and GSP-2933/RX/OVAP can be used in selective soldering. For wave soldering, dip soldering and strand tinning. RX series can be applied using both spray and foam flux methods.

Emil Otto

[emilotto.de](http://emilotto.de)

### MASTER BOND EP21ARLV

EP21ARLV two-part epoxy may be used as adhesive, sealant, coating or encapsulant. Withstands prolonged exposure to 70% sulfuric acid, 10% hydrochloric acid, 10% nitric acid and butyl acetate. Parts A and B have viscosity of 3,000-6,000cps and 4,000-6,000cps, respectively. Cures at room temp. Volume resistivity greater than 10<sup>14</sup> ohm-cm at 75°F and dielectric strength of 440V/mil at 75°F for a 1/8" test sample.

Master Bond

[masterbond.com](http://masterbond.com)

### CALCUQUOTE SHOPCQ

ShopCQ supply chain management software now includes ordering API integrations for faster, simpler purchasing when placing online orders with several leading component distributors, including Arrow, Avnet, Digi-Key and Mouser. Provides access to supplier ordering APIs, simplifying purchasing and moving products through the supply chain faster. Shows real-time pricing information and allows electronic orders.

CalcuQuote

[calcuquote.com/products-shopcq.html](http://calcuquote.com/products-shopcq.html)

### AQUEOUS TECHNOLOGIES ECO-CYCLER

Eco-Cycler third-generation rinse water recycler permits low-discharge cleaning systems to operate in a zero-discharge configuration. Receives, re-dionizes and replenishes rinse water, creating a zero-discharge cleaning system, reportedly alleviating requirement for a drain. Rolled stainless steel frame and panel construction.

Aqueous Technologies

[aqueoustech.com](http://aqueoustech.com)

### HIOKI IM9202

IM9202 test fixture makes high-frequency measurements of surface-mount and leaded components. Handles SMDs of irregular shape, including axial- and radial-leaded components, film capacitors and RFID and NFC tags. Tests SMDs from 1.6mm to 23mm long and radial components with lead spacings up to 26mm. Applications include components for high-power, high-frequency PCBs, and components and antennas for RFID and NFC circuits.

Hioki

[hioki.com](http://hioki.com)





## ASM SIPLACE SX

Siplace SX pick-and-place machine has new placement head versions, a more powerful vision system, open interfaces for special feeders and new software functions. SpeedStar CP20 head raises placement performance to up to 43,250 components per hr. Siplace MultiStar and Siplace TwinStar heads handle larger and more complex components and place them with force of up to 100N.

ASM Assembly Systems

asm-smt.com

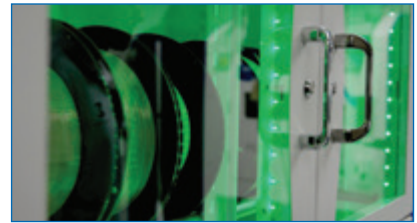


## PALOMAR 8100

8100 automated, thermosonic high-speed ball-and-stitch wire bonder is capable of ball bumping and customized looping profiles. Is for applications with tight spaces, fragile surfaces, flip-chip, deep access cavities. Pattern referencing software for vision processing. Bond parameters traceability.

Palomar Technologies

palomartechnologies.com



## ESSENTIUM DRYBOX

DryBox cabinet stores and protects 3-D printing filaments in a humidity-controlled environment. Is built on ECD SmartDRY storage technology, modified to align with requirements of 3-D material storage. Intelligent, automated system has humidity recovery time of less than 5 min. and can maintain RH values under 1% (dew point under -40°C).

Essentium

essentium.com

ECD

ecd.com

## OTHERS OF NOTE

### INDIUM WS-829

WS-829 ball-attach flux for printing and pin transfer applications, including LED die-attach, can be used for ball-attach on substrate in a standard BGA process, especially for sphere applications <0.25mm, as well as wafer/panel-level packaging. Water-soluble and halogen-free. Cleans with DI water; cleans contamination or pad oxidation from processes before ball mount. Has high tackiness. Ensures consistent flux definition over long periods of time with minimal slump.

Indium Corp.

indium.com

### CREATIVE MATERIALS 813-76

813-76 is a two-component room-temp.-curing thermally conductive and electrically insulating adhesive. Is for assembling heat-sensitive components on PCBs. Provides high-impact bonds that improve heat transfer while maintaining electrical insulation. Bonds to variety of surfaces; has a low CTE; provides resistance to mismatched substrates. Is chemical-resistant; shows low shrinkage; passes NASA outgassing requirement (ASTM-E-595).

Creative Materials

creativematerials.com

### KOKI TF-M881R

TF-M881R tack flux is for BGA/CSP component applications. Has 9 mo. shelf life. Categorized as halogen-free per JEITA ET-7304A and ROL0 by IPC J-STD-004B. Has more than 72 hr. of tack time, in addition to heat resistivity and meltability. Reportedly exhibits stable and consistent dispensing after 5,000 dispensing shots. Retains high electrical reliability and ensures good melting properties. High surface insulation resistance is suitable for fine-pitch applications.

Koki

ko-ki.co.jp

### SHENZHEN JAGUAR R10-N

R10-N lead-free forced convection reflow oven comes with nitrogen. Center rail support prevents warpage to PCB board panel. Fully enclosed oven efficiently maintains oxygen levels at 500-1000ppm. Nitrogen consumption of 16m³/h based on 500-1000ppm. Three cooling zones with chillers. Conveyor chain built with single pin-plate design. Siemens PLC+Industrial PC with precise controlling unit and stabilized performance.

Shenzhen Jaguar Automation Equipment

jaguar-ele.com

### EMIL OTTO EO-MC-001

EO-MC-001 liquid flux can be mixed with water or alcohol and can be used for tinning process in electronics industry and mechanical engineering. Can be used in electronics production, as well as in strip tinning and cooler construction. Mixing with alcohol achieves rapid evaporation. Ensures good wetting and allows effective temp. range of approx. 130°-300°C.

Emil Otto

emilotto.de

### THERMO FISHER AXIA CHEMISEM

Axia ChemiSEM scanning electron microscope includes always-on EDS analysis. Next-generation auto-alignment and auto-focus technology lowers need for training. Chamber and stage design aids in investigation of samples of all shapes and sizes, including samples up to 10kg. Offers instant quantitative elemental information without additional setup or switching between user interfaces.

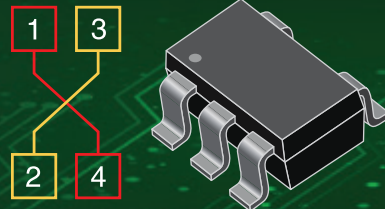
Thermo Fisher Scientific

thermofisher.com



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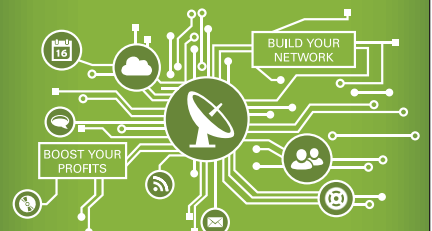
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# In Case You Missed It

## Component Technology

“N-Polar GaN-on-Sapphire Deep Recess HEMTs With High W-Band Power Density”

**Authors:** Brian Romanczyk, Weiyi Li, Matthew Guidry, Nipuram Hatui, Athith Krishna, Christian Wurm, Stacia Keller, and Umesh K. Mishra.

**Abstract:** This work presents recent progress in the W-band (94GHz) power performance of N-polar GaN deep recess HEMTs grown on sapphire substrates. While SiC has been the substrate of choice to achieve the highest level of performance, sapphire substrates are a lower cost alternative. The authors show that N-polar GaN deep recess HEMTs grown on sapphire match the power performance of a device on SiC up to 14V with 5.1W/mm of output power density. At 16V the device on sapphire starts to suffer from thermal effects but still demonstrated 5.5W/mm with an associated 20.6% power-added efficiency. This work also examines the impact of encapsulating the device in a low dielectric constant film often used for the implementation of an RF wiring environment. Such a device could be critical to efficiently pushing 6G's terahertz-frequency signals out of the antennas of future smartphones and other connected devices. (*IEEE Electron Device Letters*, vol. 41, no. 11, November 2020, <https://ieeexplore.ieee.org/document/9187650>)

## IC Packaging Materials

“Sintered Nanocopper Paste for High-Performance 3D Heterogeneous Package Integration”

**Author:** Yiteng Wang, Atom O. Watanabe, *et al.*

**Abstract:** 5G communications have been driving major package innovations to enable low-loss interconnects between ICs and other system components such as antenna arrays. Antenna-in-package with three-dimensional or double-side components is widely pursued as the front-up architecture to realize this vision. The interconnect height and losses are critical parameters in these 3-D package structures. Copper sintering paste is emerging as an ideal candidate to replace solders for both off-chip and on-package interconnects because of the resulting higher electrical conductivity and relatively simple manufacturability with additive processes. This article focuses on computational modeling, optimization of sintering conditions, and electrical conductivity measurements of highly conductive copper paste to verify the proposed model. The model is based on two-particle sintering theory, which describes the neck growth evolution of copper paste at the initial stage of sintering. The neck-growth model shows good consistency with the measured neck size of copper, and hence can be used to

provide guidelines for the sintering conditions of copper paste. The electrical conductivity measurements suggest the copper paste sintered at 260°C for 30 min. shows an electrical conductivity of  $1.4 \times 10^7$  S/m, which is 82% higher than that of solder. In addition, this article investigates the potential of copper paste interconnect technology in high-frequency applications such as in 5G millimeter-wave communications. The transmission lines patterned with the copper paste show good correlation with simulated results in the millimeter-wave frequency band. The high-frequency characterization also indicates the copper paste enables simple circuit patterning, offering equivalent signal losses with plated copper. The detailed analyses suggest the eligibility for multi-applications of copper sintering paste in IC packaging. (*Journal of Electronic Materials*, Sept. 10, 2020; <https://link.springer.com/article/10.1007/s11664-020-08399-x>)

## Inkjet Printing

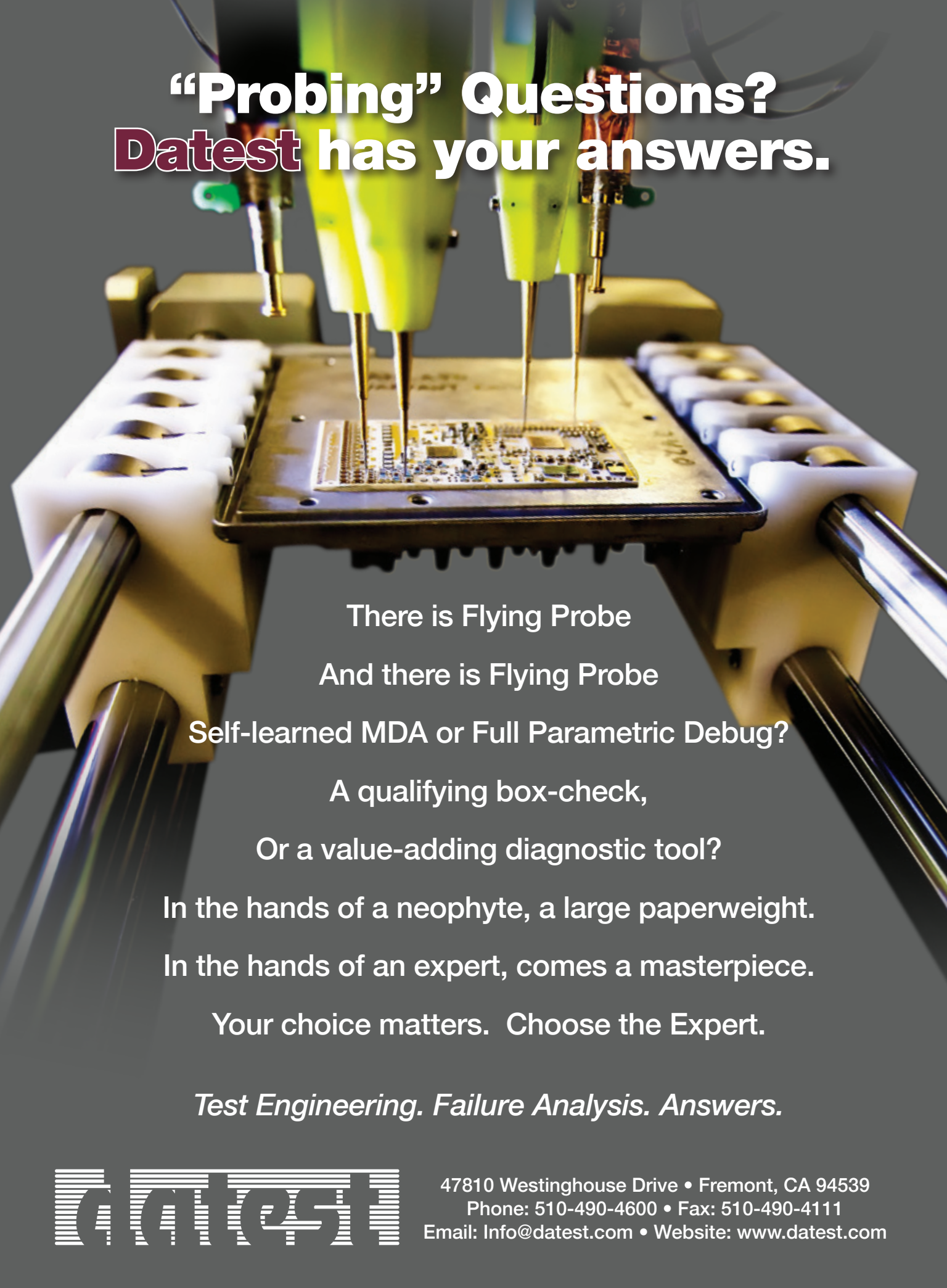
“Drop Impact Printing”

**Authors:** Chandantaru Dey Modak, Arvind Kumar, Abinash Tripathy and Prosenjit Sen.

**Abstract:** Hydrodynamic collapse of a central air-cavity during the recoil phase of droplet impact on a superhydrophobic sieve leads to satellite-free generation of a single droplet through the sieve. Two modes of cavity formation and droplet ejection are observed and explained. The volume of the generated droplet scales with the pore size. Based on this phenomenon, the authors propose a drop-on-demand printing technique. Despite significant advancements in inkjet technology, enhancement in mass-loading and particle-size have been limited due to clogging of the printhead nozzle. By replacing the nozzle with a sieve, the authors demonstrate printing of nanoparticle suspension with 71% mass-loading. Comparatively large particles of 20µm diameter are dispensed in droplets of ~80µm diameter. Printing is performed for surface tension as low as 32mNm<sup>-1</sup> and viscosity as high as 33mPa·s. In comparison to existing techniques, this way of printing is widely accessible as it is significantly simple and economical. (*Nature Communications*, vol. 11, Aug. 28, 2020, [www.nature.com/articles/s41467-020-18103-6](http://www.nature.com/articles/s41467-020-18103-6))

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.





# **“Probing” Questions?** **Datest** has your answers.

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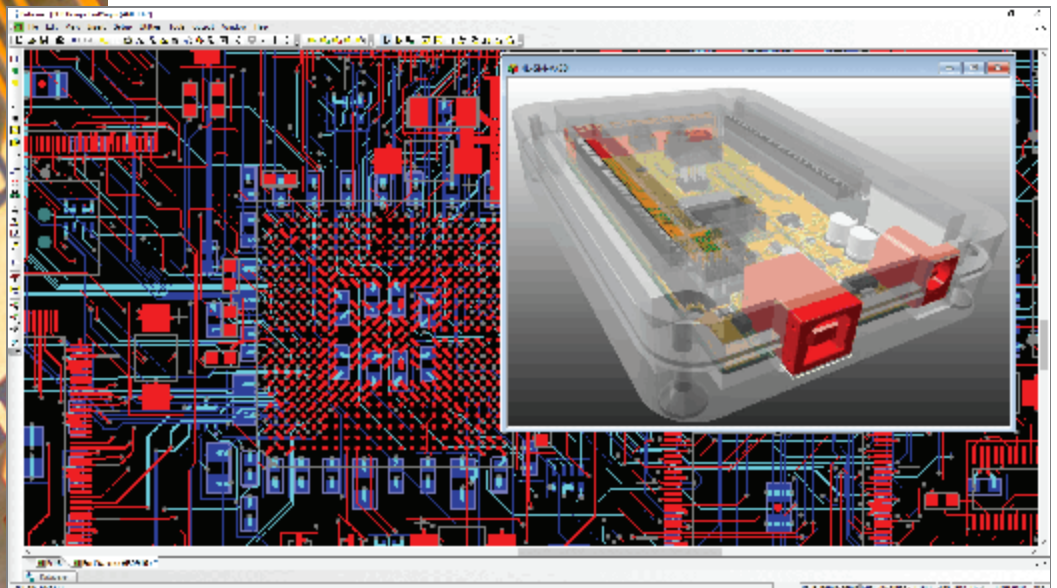
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