PCEA PRINTED CIRCUIT ENGINEERING ASSOCIATION

The Flexperts: Get Bent

PRINTED CIRCUIT DESIGN & FAB CIRCUITS ASSEMBLY

pcdandf.com
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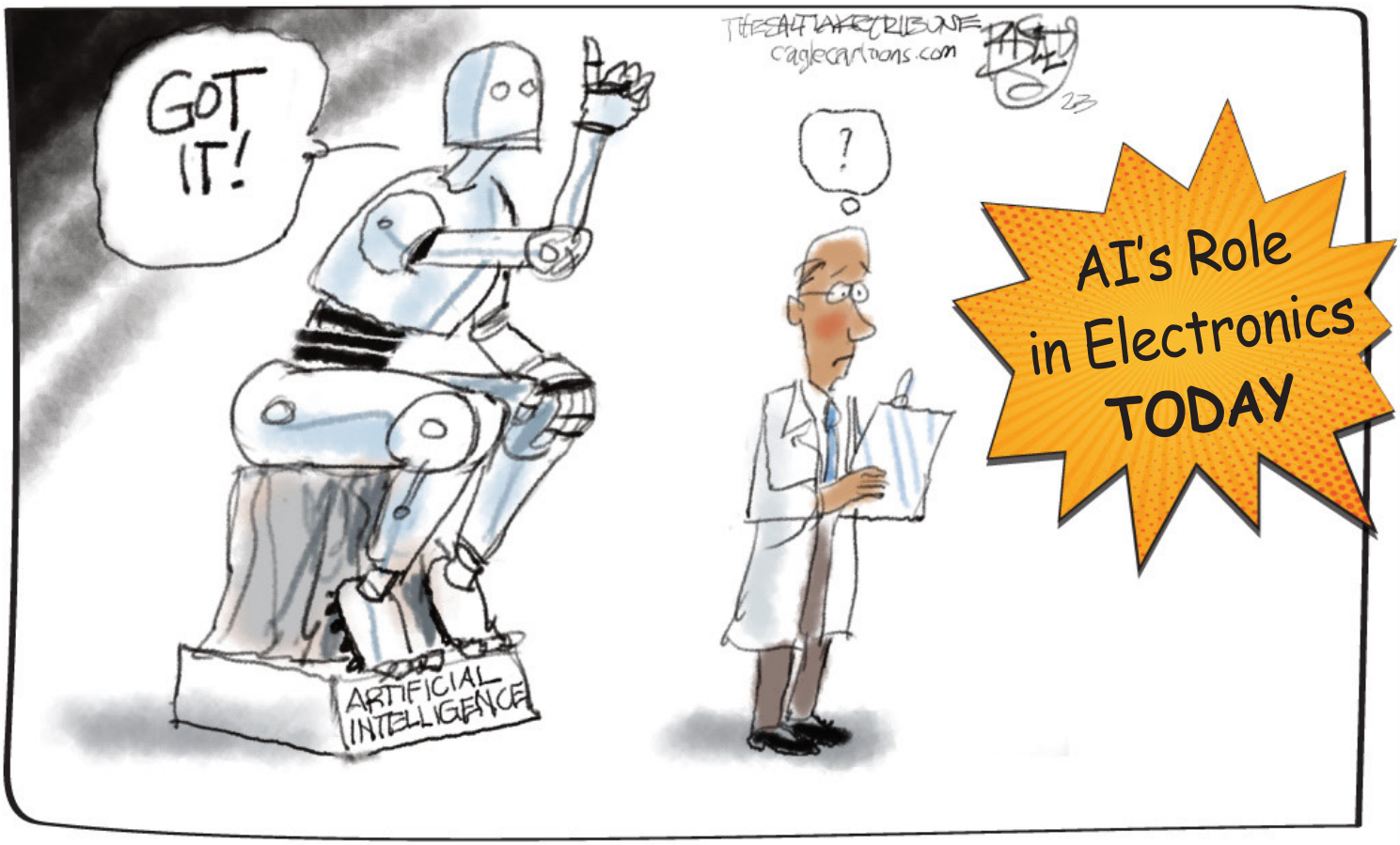
June 2025

WIRED FOR INTELLIGENCE



MEANWHILE, IN OTHER NEWS...

- ✔ 6 Steps for **Bluetooth** Design
- ✔ PCB **Stack-ups**
- ✔ Avoiding **Solder Balls**
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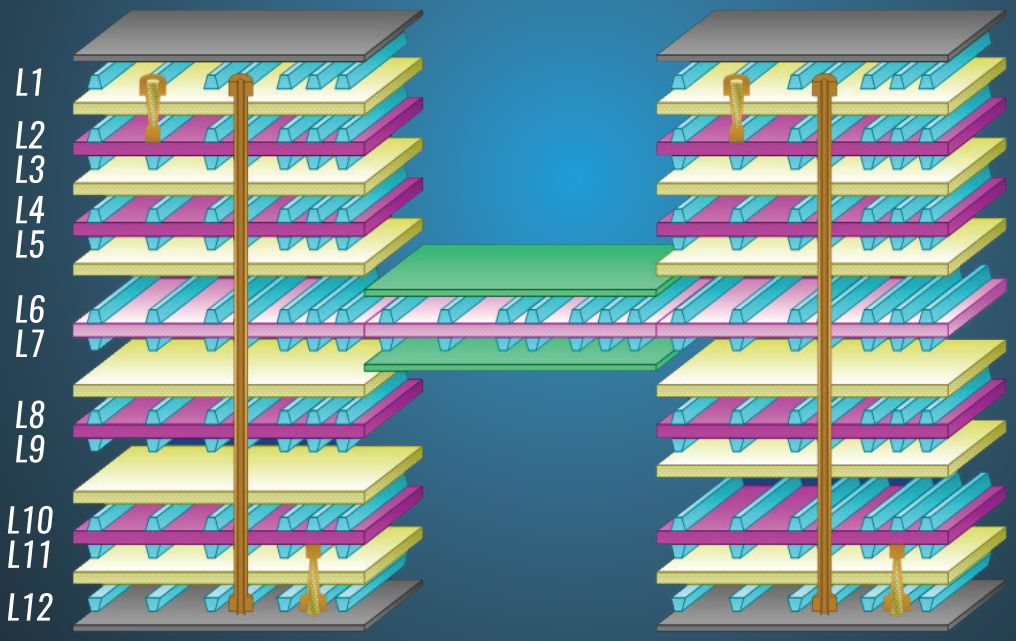

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Support For Flex, Rigid Flex and Embedded Component Designs Now Available.

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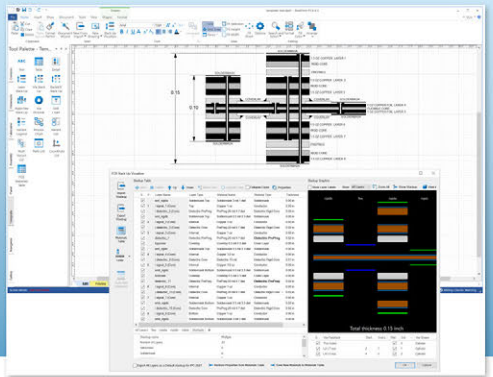
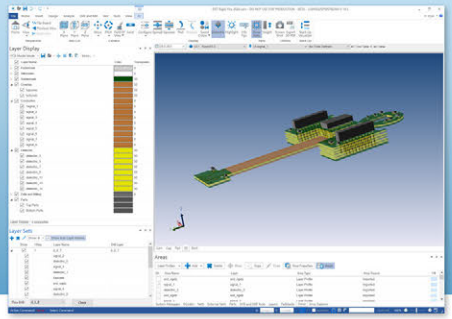
DownStream's CAM350 and BluePrint-PCB support importation and visualization of PCB designs containing Flex, Rigid Flex or Embedded components. Visualize designs in both 2D and 3D, and easily document complex Flex or Rigid- Flex Stack-Ups for submission to PCB Fabricators.

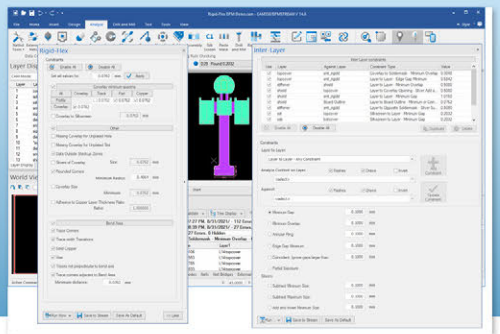
- **Import and Visualize Flex, Rigid-Flex and Embedded Component Designs**
- **3D Visualization to Validate PCB Construction and Component Assembly**
- **Manage Variable Stackup Zones for Rigid-Flex Designs**
- **Easily Create Custom Flex or Rigid-Flex Fabrication and Assembly Documentation**
- **Use DFM analysis to analyze a flex or rigid-flex design for potential fabrication or bend related defects**



Use Stack Up Visualizer and Blueprint's Rigid-Flex Stackup template to easily manage and document rigid-flex stackups.



A rigid-flex design in 3D. Shown with layers spread to improve visualization of the layer stackup.



Use Rigid-Flex and Inter-layer DFM analysis to analyze flex and rigid-flex designs.

DownStream Technologies

For more information visit downstreamtech.com or call (508) 970-0670

JUNE 2025 • VOL. 42 • NO. 6

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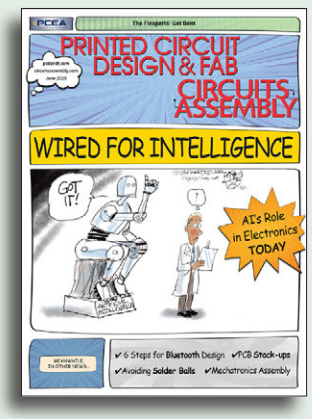
MONEY MATTERS

TECH TALK

DEPARTMENTS



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Can DoE Program Energize PCB Technology?

AMONG THE MANY surprises at PCB East this spring was the appearance of a pair of scientists from a semi-obscure (to we laypeople) government contractor called, obliquely, JLab.

JLab is shorthand for Jefferson Lab, or its official name, the Thomas Jefferson National Accelerator Facility (TJNAF). The facility is operated on behalf of the US Department of Energy, which has a budget larger than Jabil or Flex, and oversees, among other things, the US nuclear arsenal.

Now, in the event you haven't been paying attention, the US government has been in the media kind of often of late, for reasons too numerous for this page to detail. But one big newsworthy item has been the administration's efforts to change the federal government's budget priorities.

Certainly, most readers are familiar by now with the Chips Act, the overarching legislation passed in fall 2022 that authorized more than $50 billion in direct spending and tax incentives to rally North American semiconductor production. It was perhaps the most significant government-led mandate since the European Union ratified the Restriction of Hazardous Substances Directive (RoHS).

And most are also aware of a similar, albeit smaller, bill to bolster domestic printed circuit board and IC substrate production that has been proposed in Congress but has yet to make it out of committee. (The latest version, called the Protecting Circuit Boards and Substrate Act, was introduced in late May.)

Far beyond the headlines, the team representing Jefferson Lab is working on an AI solution for the manufacturing side of the PCB industry. Which is how we came to find team members Dr. Thomas Britton and Dr. Nataliia Matsiuk walking the show floor at PCB East, talking with PCB manufacturers as part of a DoE academic program that aims to get scientists out of the labs to learn what problems the industry faces.

As Britton explains on a recent podcast we did, he and Matsiuk are technologists and problem-solvers out to provide tailored solutions applicable to the industry at large. What they need in return is for manufacturers to explain what their problems are.

"A lot of value is sitting above the manufacturing process," Britton says, referring both to inaccessible collected data and missed opportunities to collect other useful data. "Can we make something adaptive and reactive utilizing that data coming from the manufacturing line?"

"There's a lot of data being produced," he elaborates. "It's very complicated, lots of steps." The DoE program seeks to take the data from those steps, aggregate it and use it to better assess the manufacturing process holistically, he says, getting in front of potential variances as opposed to, " 'Oh, what, there's a problem here?' "

Clearly there is (or was) government momentum to support critical industries. While the Chips Act and Boards Bill are still trying to execute on their lofty goals, the DoE has been honing its craft for years.

The subtle gem of the DoE is it is already taxpayer funded. The crucial lever, then, isn't money – but communication.

"We're doing things to help our science. And we're funded from taxpayer dollars through the DoE to do the work we do," he says.

One program, for instance, was for machine vision, which sought to replace shift workers with AI solutions.

"We're looking at deep learning and those kinds of solutions," says Britton. "One thing that I've heard of that's a roadblock for a lot of factories, at least in the US, to develop this smart factory, is to be able to communicate with the AI systems. [Manufacturers] don't have equipment that's capable of reporting and communicating this [data].

"What we've found is Asia is very well-instrumented. Around [the US], legacy machinery maybe isn't collecting the data. They didn't know it would be valuable. We see PCB as a beachhead to prove out the technology because you have similar challenges, especially with substrate-like manufacturing techniques that are coming up."

As part of their commercialization strategy, the DoE is considering an open AI model in which its researchers partner with a private manufacturer, and the improvements in the line outputs make up the proof of concept.

"I think it's going to take a lot of partnerships between the lab, the researchers and industry partners to really dig into the data that is held so close to the chest for a variety of reasons.

"You take the knowledge you gain at one company and to go to the next one. And you are transferring that knowledge – just like an employee working at one firm and then moving to a different firm – without exposing the secrets of any party involved to enhance the manufacturing across the line," Britton says.

"I think, right now, our top hypothesis is that you would do it through embedding with viable partners willing to give you the data, work with you, devote the time and then hopefully it would be made commercially available."

Fabricators have often privately groused that the US government can be a roadblock to success. Will they take the opportunity to clear that path now that they know it's available?

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@mikebuetow

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

NCAB GROUP

PCB Design Guidelines

Get it right from the start with our PCB Design Guidelines

Nothing impacts the cost and quality of a printed circuit board (PCB) as significantly as the initial PCB layout and design. In today's world, electronic products are expected to deliver increasingly advanced features while becoming smaller in size. This places greater demands on the PCB layout and design, making it more crucial than ever to make informed choices during the design stage. To ensure a successful start, we have compiled our PCB design guidelines, which serve as a comprehensive checklist.

Design guidelines for **Multilayer** PCB, **HDI** PCB, **Ultra HDI** PCB, **Flex / Rigid-Flex** PCBs, **Semi-Flex** PCB, **Copper coin** and **Stackups and Impedances** are available for download.

Download our design guidelines here

Or visit **www.ncabgroup.com** to learn more.

AMD to Sell ZT Systems Manufacturing Business to Sanmina for $3B

SANTA CLARA, CA – AMD has entered into a definitive agreement to divest ZT Systems' US-based data center infrastructure manufacturing business to Sanmina for $3 billion in cash and stock, including a potential $450 million contingent payment.

As part of the agreement, Sanmina becomes AMD's preferred new product introduction (NPI) manufacturing partner for rack-scale and cluster-scale AI infrastructure. AMD will retain ZT Systems' design and customer enablement teams to continue supporting rapid deployment and high-quality AI solutions for cloud providers.

The transaction, expected to close by the end of the year pending regulatory approval, fulfills AMD's stated intent from its 2024 ZT Systems acquisition to partner out the manufacturing portion of the business.

Siemens to Acquire Wevolver

MUNICH – Siemens Digital Industries Software announced its intent to acquire Wevolver, a move that will enhance its previous acquisition of Supplyframe platform by extending its global reach, adding to its content capabilities and strengthening digital marketing and campaign execution. Terms of the acquisition were not disclosed.

Supplyframe, acquired by Siemens in 2021, delivers real-time insights into design intent, demand, supply, and risk factors for the electronics industry. The addition of Wevolver brings a broader audience of hardware and software engineers to the platform, fostering a deeper connection with professionals involved in early-stage product research and innovation.

"The future of product development starts with smarter design decisions – and that means meeting engineers where innovation begins," said Steve Flagg, CEO and founder, Supplyframe. "By joining forces with Wevolver, we're not just expanding our reach; we're accelerating a new era of design-to-source intelligence that's collaborative, data-driven and built for the speed of tomorrow's manufacturing."

Wevolver's content platform reaches millions of engineers monthly across web and social media, offering technical resources on semiconductors, robotics, AI and manufacturing processes. The combination with Supplyframe is expected to provide manufacturers and distributors greater visibility for emerging technologies at the crucial stage of research.

"Supplyframe and Wevolver both support engineering professionals throughout their research, development, and

supply chain journey," said Bram Geenen, CEO, Wevolver. "Together we bring an even stronger value proposition to the global technology ecosystem and will be the home for the global engineering community."

Syrma to Add Bare Board Manufacturing

MUMBAI – Syrma SGS Technology in May approved the incorporation of two wholly owned subsidiaries to manufacture electronic components, bare printed circuit boards, component assembly and manufacturing interface cards and other electronic components.

The measure marks an expansion of the company's traditional EMS focus.

Syrma's revenue for the fiscal year ended March 31 was 2.3 million rupees ($269 million), up 23% year-over-year.

MKS Breaks Ground on $40M Thailand Facility

ANDOVER, MA – MKS Instruments has begun construction on a $40 million chemical manufacturing facility and technical center near Bangkok.

The new site aims to support Southeast Asia's PCB and advanced packaging sectors.

The 27,000 sq. m site will offer chemical production, plating technologies, labs and regional service, with operations expected in 2027

Lacroix to Exit North American Market by End of Year

SAINT-HERBLAIN, FRANCE – Lacroix announced plans to fully exit its North American electronics operations by the end of the year as part of a shift toward higher-potential activities in Europe and environmental solutions.

The company will explore options for its North American operations, including sale, shutdown or liquidation. It will also seek to pare its dependence on the automotive sector.

The exit follows sustained losses and worsening conditions at Lacroix Electronics, which operates in Juarez, Mexico and Grand Rapids, MI.

The division reported an EBITDA loss of approximately $14.5 million on annual revenue of roughly $151.7 million in 2024. Multiple contract losses and geopolitical uncertainty, including the risk of new US import duties, contributed to the decision.

For the first quarter, Lacroix's electronics revenue fell 15.9% year-over-year to $125.1 million.

Cofactr Acquires Hardware Sourcing Provider Cogbase

NEW YORK – Cofactr has acquired Cogbase, a hardware sourcing platform with a network of over 450,000 suppliers, to strengthen and scale supplier options for US manufacturers. Terms were not disclosed.

The acquisition will permit Cofactr to automate sourcing for complex parts while reducing the average time spent on vetting suppliers.

Cofactr will integrate Cogbase's automated sourcing capabilities, including 2-D/3-D drawing uploads, specification matching and supplier outreach.

"Going through multiple rounds of searches for new suppliers has often become the norm for hardware procurement teams," said Phillip Gulley, CSO and cofounder, Cofactr. "With Cogbase, we're expanding our ability to solve this challenge."

Cogbase CEO Doug Platz will now serve as Cofactr's head of supplier network. The deal follows Cofactr's February acquisition of Factor.io.

Celanese to Divest Electronics Business

DALLAS – Celanese is preparing to sell its Micromax electronic inks and paste unit as part of a broader push to cut debt and raise cash. The business, housed within its engineered materials division, is expected to bring in over $300 million in revenue this year.

The company aims to generate $1 billion from divestitures over the next 30 months, with Micromax positioned as the first in a series of sales.

The company was developed by DuPont and acquired by Celanese during its $11 billion buyout of DuPont's mobility and materials segment in 2022.

CEO Scott Richardson emphasized the high level of interest in the unit and said that going public with the sale was a strategic move. Additional divestitures may come from both the engineered materials and acetyl chain businesses as Celanese looks to streamline around its core operations and prioritize deleveraging.

TechSearch Warns of Substrate Shortage by

2029

AUSTIN, TX – A supply shortage of build-up substrates is looming, starting in 2029, with tight conditions emerging as early as 2028, according to a new report from tech research firm TechSearch International.

In its latest Advanced Packaging Update, TechSearch says a surge in artificial intelligence hardware, particularly for training and inference workloads, is accelerating demand for high-bandwidth memory stacks and pushing substrate body sizes larger across server CPUs and high-end network switches.

The report, which includes a detailed capacity and demand analysis, emphasizes how this trend will affect the global supply chain for advanced packaging.

Despite sluggish long-term growth in consumer electronics, 2024 saw 5.2% revenue growth for the top 20 OSATs from the previous year, driven by a rebound in smartphone and PC shipments. TechSearch projects limited future growth in PC, smartphone and consumer markets, however, which may constrain unit volumes for ball grid array (BGA) and chip scale packages (CSPs).

Epec Acquires Roca Printed Circuits

DALLAS – Epec Engineered Technologies' NetVia Group division has acquired Roca Printed Circuits, a move aimed at enhancing both companies' printed circuit board offerings.

Barry Finberg, president of Dallas-based Roca, said the partnership comes in response to global economic shifts and supply chain pressures: "Epec was the clear choice to uphold the standards of quality, pricing and delivery that Roca customers have come to expect."

Epec has expanded its manufacturing facilities across the US, UK and Asia. Since acquiring NetVia in 2020, the company has doubled production capacity and now adds Roca's operations to its Dallas-based footprint.

The acquisition is part of Epec's broader strategy to strengthen domestic manufacturing.

Kaynes Technology Acquires August Electronics

CALGARY, AB – Kaynes Technology India Limited has announced the acquisition of Canada-based August Electronics through its subsidiary, Kaynes Canada Ltd. The transaction was expected to close by the end of May, pending regulatory approvals.

August will continue to operate under its existing structure, with CEO Tanya Korenda remaining in her role, while

Co-Founders Jack Francis and Peter Wilson will step away.

“There is a tremendous alignment between August and Kaynes in terms of culture, capabilities and customer focus,” said Korenda.

Kaynes managing director Ramesh Kannan called the move “a strategic alternative to China-based sourcing” and said it strengthens the company’s reach in North America.

PCD&F

AGS Devices will license and cobrand the **Celus** Design Platform.

Duro announced its technology partner program and initial members.

DuPont filed an initial Form 10 with the **SEC** to separate its Electronics business into a standalone company, temporarily named **Novus SpinCo1**.

The **FCC** in May unanimously approved rules banning Chinese labs considered national security risks from certifying electronic devices for use in the US.

Laird Thermal Systems has rebranded to **Tark Thermal Solutions.**

Logitech announced a collaboration with **Elephantech** to integrate SustainaCircuits, a low-carbon PCB technology, into its manufacturing process.

Nano Dimension completed its acquisition of **Markforged Holding.**

Technical University of Munich researchers have developed a neuromorphic AI chip, AI Pro, that processes data locally without requiring cloud access. The chip, modeled after the human brain, uses hyperdimensional computing to identify patterns with significantly less energy.

University of Chicago scientists have developed ProtoPCB, a tool that scans old circuit boards for reuse in new projects.

CA

3C Tae Yang, a South Korean electronics and semiconductor firm, is eyeing Kalaburagi as a site for setting up its first manufacturing unit in India.

4Front Solutions has installed a second **Seica** Pilot V8 Next flying probe tester.

APE is expanding into contract assembly and repair services.

BEST Inc. now offers full-service electronic component salvaging, including BGA reballing and reconditioning.

Canadian Circuits introduced a prototype PCB assembly service.

Creation Technologies expanded its Denver Product Realization Center, increasing the facility's footprint 40% to 45,000 sq. ft.

Dixon Technologies' wholly owned subsidiary, **Padget Electronics,** has signed a contract manufacturing agreement with **NxtCell India** to produce smartphones for the **Alcatel** brand under the Make in India initiative.

ECIA has formed a tariff-focused working group to support members with strategy, compliance and policy shifts.

Enim has partnered with the Royal Canadian Mint to test metals extracted from printed circuit boards for coin production.

Essemtec has opened a larger demo lab and relocated its US office to Burlington, MA.

IEEE released **IEEE 3119**, the first internationally accepted, consensus-based standard that focuses on the procurement of AI tools and offers operational guidance for responsibly purchasing high-risk AI systems that serve the public interest.

Frank Elektronik has upgraded with a new SMT line, featuring **ASYS** and **EKRA** machines.

Integra Technologies installed a **Hentec/RPS** Photon steam aging system.

Inventec is expanding manufacturing operations in Texas and Thailand to address rising AI server demand and mitigate geopolitical supply chain risks.

Libra Industries upgraded its Dallas facility with new **Juki** LX-8 placement machines, **Omron** inspection systems, and a nitrogen-capable reflow oven.

LG Electronics will invest an additional $100 million to expand its Clarksville, TN operations, adding 80 jobs and a 560,000 sq. ft. warehouse.

Medco West Electronics installed an **Aqua Klean** Typhoon T9 aqueous cleaner.

Mycronic renamed its High Flex division PCB Assembly Solutions.

Nivelco installed two **Fuji** Aimex IIIc placement machines.

Novair USA appointed **Horizon Sales** regional representative for the Midwest US.

Pegatron unveiled its new manufacturing facility on Indonesia's Batam Island, featuring a dedicated 5G private network spanning the entire plant.

Pride Industries added a **Kurtz Ersa** Powerflow wave soldering system.

Schaeffler is accelerating product deployment for automakers in China, following the acquisition of **Vitesco Technologies.**

Semi-Kinetics purchased four **Hanwha Semitech Americas** ESE US-2000 screen printers.

SisTech Manufacturing installed an **LPKF** CuttingMaster 2127 ultraviolet laser depaneling system and **Koh Young** aSPIre 3 and inline SPI.

Taiwanese EMS firms are increasingly shifting operations to Indonesia, prioritizing labor stability over supply chain completeness amid rising tariff concerns.

Test Connection named as representatives **Microwave Component Sources** in the Southeastern US and **USM Reps** in Mexico.

US lawmakers in May introduced a bipartisan bill requiring AI chipmakers to verify chip locations before export to curb smuggling into China.

ViTrox has updated its demo center in Hutto, TX.

Wistron in May approved an additional investment of $455 million in its new US subsidiary, bringing the total planned investment to $500 million.


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PCDF

Kent Alder

The Ranger Group named **Paul Brionez** senior electrical engineer.

TTM Technologies announced the retirement of founder and board member **Kent Alder**.

Flexium elevated **Chen Chin-Yuan** to president.

CA

Bryce Timms

Curt Anderson

Eric Ting

Federal Electronics' Business Development Team

Daniel Enríquez Gómez

Michael Buseman

James Wertin

Shane Nunes

Aligned Solutions appointed **Bryce Timms** regional sales representative for Ohio, Kentucky and Western Pennsylvania.

Altus Group promoted **Steve Leake** to sales engineer.

Ana Wold Garcia launched AW Manufacturing Solutions, an EMS rep firm.

Avalon Technologies named **Curt Anderson** director of business development.

Axxon-Mycronic promoted **Eric Ting** to sales director, Southeast Asia.

Cofactr named **Mike Giardinelli** supplier development manager and **Matthew LeVan** principal engineer.

Federal Electronics added **Andrew Davis**, **Joel Robbins** and **Will Oliver** to its business development team.

Inovaxe welcomes **Daniel Enríquez Gómez** as regional sales manager for Northern Mexico.

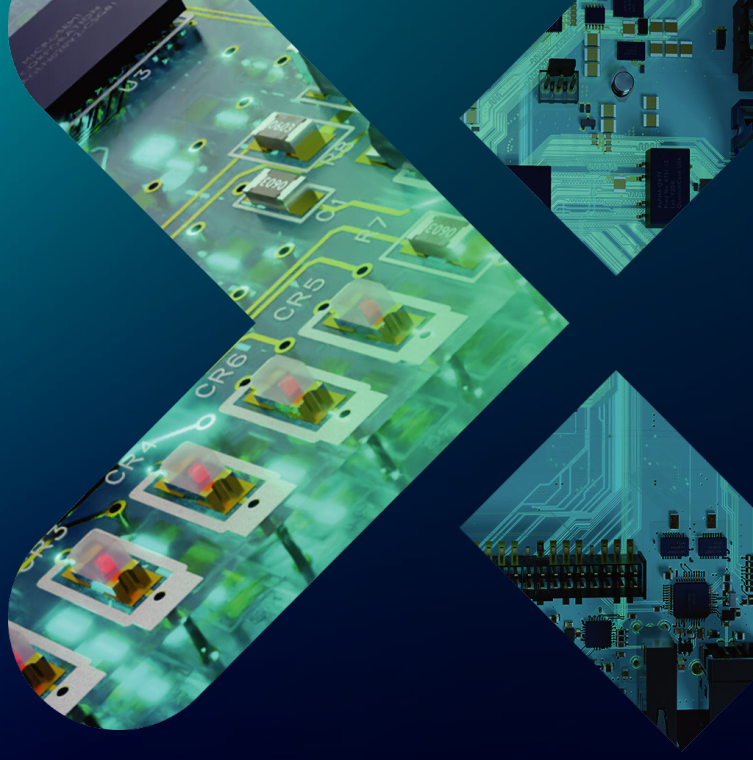
SMTC appointed **Mike Buseman** president and CEO.

Stannol welcomes **James Wertin** as director of technical sales and solutions.

Universal Instruments appointed **Shane Nunes** chief operating officer.

USI named **Rodrigo Sierra Avila** site engineering director.

SIEMENS



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FROM INDIVIDUALS TO ENTERPRISES

PCB West Technical Conference Announced

PEACHTREE CITY, GA – The Printed Circuit Engineering Association announced the technical program for PCB West 2025, featuring more than 125 hours of in-depth electronics engineering training spread over more than 50 sessions. The program includes 30 classes new to PCB West, PCEA added.

Among the industry experts scheduled to speak this year are Rick Hartley, Susy Webb, Stephen Chavez, Chuck Corley, Karen Burnham, Tomas Chester and Charlene McCauley. The conference will be held Sept. 30 to Oct. 3 at the Santa Clara (CA) Convention Center and features classes for every level of experience, from novice to expert.

The scope of classes ranges from designing all types of printed circuit boards to complex signal and power integrity and power delivery systems design. Foundational topics such as circuit grounding, signal integrity and PCB stackups are interspersed with advanced tutorials on switch mode power supplies, EMC, DDR5, thermal management, RF and mixed-signal design and more.

New courses this year include high-power PCB design, designing using preexisting schematics, supply chain resilience, application of IPC-6012F to the factory, signal integrity analysis, designing in 3-D, bypass capacitor placement and more.

“PCB West is the best place for designers, design engineers and their manufacturers to connect,” said Mike Buetow, conference director, PCB West. “It’s the only place you’ll learn from all the industry’s leading experts and meet legions of new peers and colleagues.”

Registration will open shortly at pcbwest.com. Conference registrants who sign up by Sept. 2 can take advantage of the Early Bird Special discounts for the conference.

An exhibition featuring more than 100 leading suppliers to the electronics design and manufacturing industry will be held Oct. 1.

This year’s show will also introduce the PCB West Management Program, a special one-day symposium featuring experts on the use of artificial intelligence (AI), new product introduction, global manufacturing and new facility engineering expansion, among other topics.

PCD&F/CIRCUITS ASSEMBLY is media partner for the event.

PCB East 2025 Basks in Higher Attendance, Conference Plaudits

PEACHTREE CITY, GA – Attendance for the PCB East 2025 exhibits rose nearly 4% year-over-year, the Printed Circuit Engineering Association announced. Attendance among the exhibits-only category was up 15% from a year ago.

The annual trade show was held Apr. 29 through May 2 at the Boxboro Regency Hotel and Conference Center in Boxborough, MA. In all, more than 65 leading suppliers of electronics design tools, manufacturers of bare boards and assemblies, suppliers of fabrication and assembly equipment and materials, and related industry companies exhibited at the show.

PCB East exhibitors were pleased with the traffic through the door.

"We were very pleased at the turnout for PCB East this year, especially given the economic uncertainty in the industry," said Mike Buetow, conference director and president, PCEA. "Exhibitors were roundly supportive of the show floor activity, and conference registrants were particularly pleased with the additional networking events."

"What a great conference!" exclaimed veteran engineering manager Mike Boutin. "The speakers were of the highest caliber and the topics varied greatly. They were not all focused on PCB design but on the efforts related to hardware design more broadly."

"We had a fantastic few days connecting with engineers, OEMs and industry partners from across the country," said Jeff De Serrano, president of PCB Technologies, US Operations.

“Another ‘old home week’ for me at PCB East,” said Manny Marcano, president of EMA Design Automation, Inc. “It is very rewarding to be a part of this event and see customers, prospects, new technologies and especially old friends in our industry. It was a great day!”

Design Certification Classes Announced

PEACHTREE CITY, GA – The next series of live Certified Professional Circuit Designer (CPCD) training and certification classes is starting this month. The class meets once a week between June 23 and July 21.

The career development sessions are for printed circuit engineers, layout professionals, and other individuals currently serving in the design engineering industry or seeking to get into it. The instructor-led classes cover the gamut of printed circuit design engineering, from layout, place and route to specifications and materials to manufacturing methods. Schematic capture, signal integrity and EMI/EMC are also part of the comprehensive program.

Subsequent sessions begin in August, September and November. Classes will be held once a week over five weeks. Each class is 40 hours long and includes a copy of *Printed Circuit Engineering Professional,* a 400-page handbook on circuit board design, and the optional certification exam recognized by PCEA.

There are no prerequisites to enroll. Upcoming classes will be held online. All courses are led by experienced instructors.

The course handbook, *Printed Circuit Engineering Professional,* was authored by Michael Creeden, Stephen Chavez, Rick Hartley, Susy Webb and Gary Ferrari, industry veterans who combined have more than 200 years’ experience designing and building PCBs for all types of applications.

For information or to register, visit pceatraining.net/registration.

Abstracts Sought for PCB East 2026

PEACHTREE CITY, GA – Abstracts for next year’s PCB East technical conference are due Sept. 5. The conference, the largest of its kind in New England, takes place next spring in the Boston suburbs, and focuses on training and best practices for printed circuit board design engineers, electronics design engineers, fabricators and assemblers.

Papers and presentations of the following durations are sought for the technical conference: one-hour lectures and presentations; two-hour workshops; and half-day (3.5-hour) and full-day seminars. Preference is given to presentations of two hours in length or more, and no presentations of less than one hour will be considered.

Abstracts of 100-500 words and speaker biographies should be submitted to PCEA. Papers and presentations must be noncommercial in nature and should focus on technology, techniques or methodologies related to printed circuit board design, fabrication, assembly, test, components or packaging, and additive manufacturing.

Submit abstracts at https://pcbeast.com/abstract-submission-guidelines by Sept. 5. No emailed abstracts will be accepted. Submitters will be notified in November if their abstract has been accepted. Presentations are due Apr. 10, 2026.

Presenters of accepted abstract(s) for the 2026 program receive complimentary access to the online proceedings and a complimentary pass to the technical conference.

For more information about PCB East, visit pcbeast.com or contact conference director Mike Buetow at pcea@pcea.net.

PCEA CURRENT EVENTS

ASSOCIATION NEWS

Networking. The PCEA Discord server brings together engineers and designers from around the world on a private channel to discuss technical questions and career opportunities. To join, contact PCEA.

CHAPTER NEWS

Orange County. The next chapter meeting is July 22 at the Siemens Costa Mesa facility (located within The MET at 535 Anton Blvd, Costa Mesa, CA). Stephen Chavez of Siemens will speak on Optimizing Engineering to Manufacturing Efficiencies. Contact Armando Saldana for more information.

Portland, OR. Our June 26 meeting starts at 12 p.m. Pacific and features renowned SI expert Don Telian. Thank you to our May presenter, Daniel Lindmark of Allspice.io, who shared higher-level details on design for manufacturing challenges and solutions. Contact Stephan Schmidt for details.

San Diego. Still finalizing plans for an in-person meeting this summer.

Silicon Valley. The Silicon Valley Chapter will hold a lunch-n-learn meeting in Fremont on June 19 from 11:30 a.m. to 1:30 p.m. Pacific. The topic is Demystifying Manufacturing Validation from a PCB Designer's Point-of-View, presented by Jayson Harames, application engineer consultant with Siemens. To reserve a seat, email Bob McCreight.

Richmond, VA. Our kickoff meeting is on June 11 at 12 p.m. EST and features a presentation from Dan Beeker of NXP Semiconductor. Contact membership@pcea.net for the Zoom meeting link.

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MARKET **WATCH**

Taiwan's PCB Industry to Grow 6% to $40B in 2025

TAIPEI – Taiwan's PCB industry is projected to reach $39.9 billion this year, growing 5.8% year-over-year, according to a joint report released in May by the Taiwan Printed Circuit Association (TPCA) and ITRI's Industrial Economics and Knowledge Center. Last year, the industry recorded $37.7 billion, an 8.1% rise fueled by strong demand for AI server applications.

The materials segment saw a significant boost, growing 13.4% to $10.7 billion last year compared to the year prior. Rigid board materials accounted for more than half of this, with high-end copper-clad laminates (CCL) and low-loss materials leading demand for use in 800G switches and AI/HPC servers.

Flexible PCB materials are gaining traction in emerging technologies like smart glasses, which are expected to grow this year. Taiwan is developing low-loss substrates and transparent PI to support this shift. The flexible materials market is projected to grow 8.5% this year compared to last year, reaching $11.6 billion.

On the equipment side, Taiwan's output hit $1.84 billion last year, with expected growth to $2 billion this year. Growth is supported by high-density manufacturing equipment for AI-related PCB processes and advanced packaging technologies. Taiwanese equipment makers are moving into backend semiconductor sectors such as CoWoS and fan-out packaging amid competition in the mid-range PCB equipment space.

Geopolitical uncertainties and US-China tensions have pushed companies to expand production in Southeast Asia. Major investments in Thailand, Vietnam and Malaysia include new CCL and substrate factories and equipment facilities. Companies like TUC, Elite Material and ITEQ are actively increasing overseas capacity.

Military Chatter

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	JAN.	FEB.[r]	MAR.[p]	YTD
Computers and electronics products	0.8	1.7	0.2	4.0
Computers	4.5	5.7	1.7	16.8
Storage devices	13.2	-6.3	-2.5	4.5
Other peripheral equipment	0.2	-2.5	-2.8	5.3
Nondefense communications equipment	-0.4	2.5	2.3	6.5
Defense communications equipment	18.9	1.1	13.1	0.9
A/V equipment	0.0	-2.7	0.0	-5.4
Components[1]	-0.3	3.5	0.7	2.6
Nondefense search and navigation equipment	4.7	-1.2	-1.7	6.4
Defense search and navigation equipment	2.5	3.8	-0.6	2.5
Electromedical, measurement and control	-0.1	1.0	-0.3	4.6

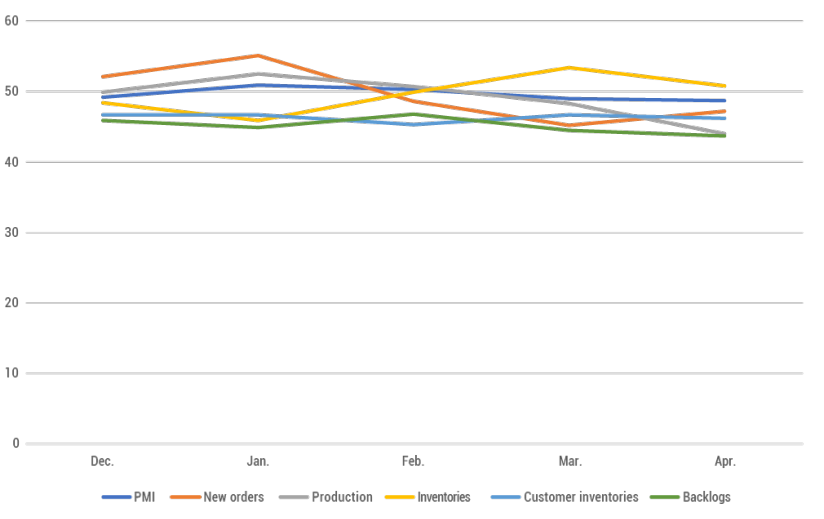
[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, May 2, 2025

Key Components

	DEC.	JAN.	FEB.	MAR.	APR.
EMS book-to-bill[1,3]	1.24	1.27	1.33	1.36	1.41
Semiconductors[2,3]	17.1%	17.9%	17.1%	1.8%	TBA
PCB book-to-bill[1,3]	1.18	1.24	1.33	1.23	1.21
Component sales sentiment[4]	115.2%	108.5%	113.0%	112.5%	94.7%

Sources: [1]IPC (N. America), [2]SIA, [3]3-month moving average, [4]ECIA

US Manufacturing Indices



Source: Institute for Supply Management, May 5, 2025

Hot Takes

Taiwan reported record-high export orders for April, up 19.8% year-over-year, driven by strong global demand for artificial intelligence applications. The **electronics sector** grew 35% to $23.1 billion. (Ministry of Economic

Affairs)

Semiconductor sales reached $167.7 billion in the first quarter, up 18.8% from the previous year, but down 2.8% from the previous quarter. March sales were up 1.8% month-over-month. (SIA)

While first-quarter electronics sales dipped 16% quarter-over-quarter and remained flat year-over-year, **IC sales** posted a 23% annual increase, fueled by AI and data center demand, and capital expenditures rose 27% year-over-year. (SEMI)

North American printed circuit board shipments fell 6.8% year-over-year in April but rose 11.5% sequentially. Year-to-date shipments are up rose 4.6%. Bookings surged 23.5% year-over-year and 26.9% from March. (IPC)

The **memory market** is seeing a sharp surge, fueled by rising contract prices since the second quarter and Samsung Electronics' move to phase out DDR4 modules. (DigiTimes)

China's manufacturing activity fell to a PMI of 49 in April, dropping below the growth threshold as steep US tariffs took effect. (China National Bureau of Statistics)

Global semiconductor materials revenue increased 3.8% to $67.5 billion in 2024. (SEMI)

Industrial printer shipments declined 1% in 2024, as shipments in the fourth quarter were 5% lower than the previous year. (IDC)

Weakening demand in the automotive and industrial sectors slowed **shipment growth for SiC substrates** in 2024, with global revenue for N-type SiC substrates falling 9% $1.04 billion. (TrendForce)

North American **EMS shipments** rose 0.2% in April compared to the same month in 2024 and dipped 1.4% from March. Year-to-date shipments are down 0.2%. Bookings dropped 10% year-over-year and declined 7.7% sequentially. (IPC)

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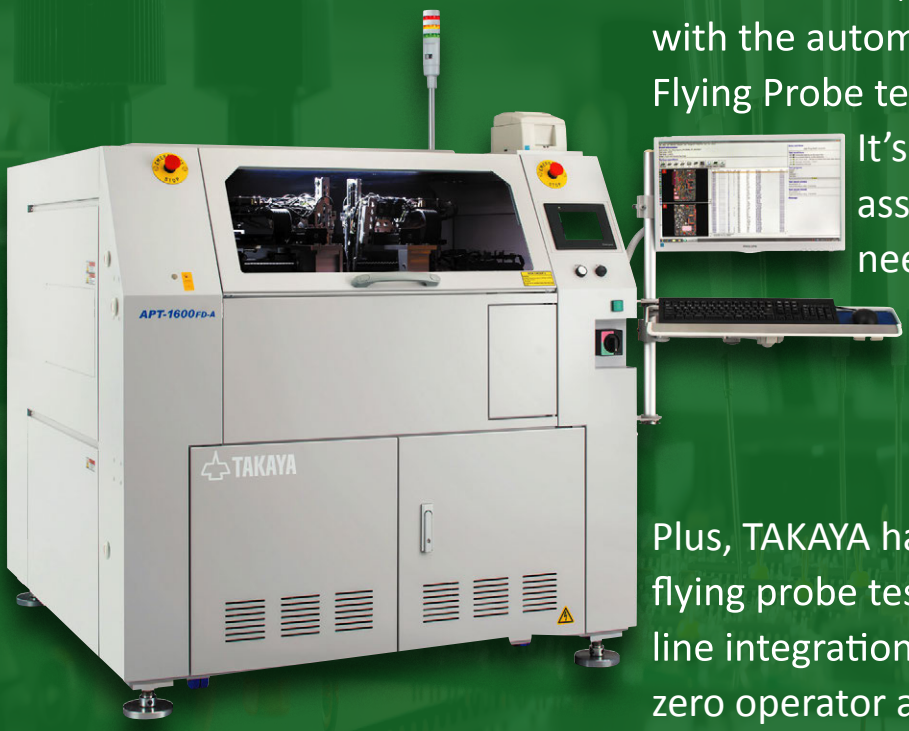

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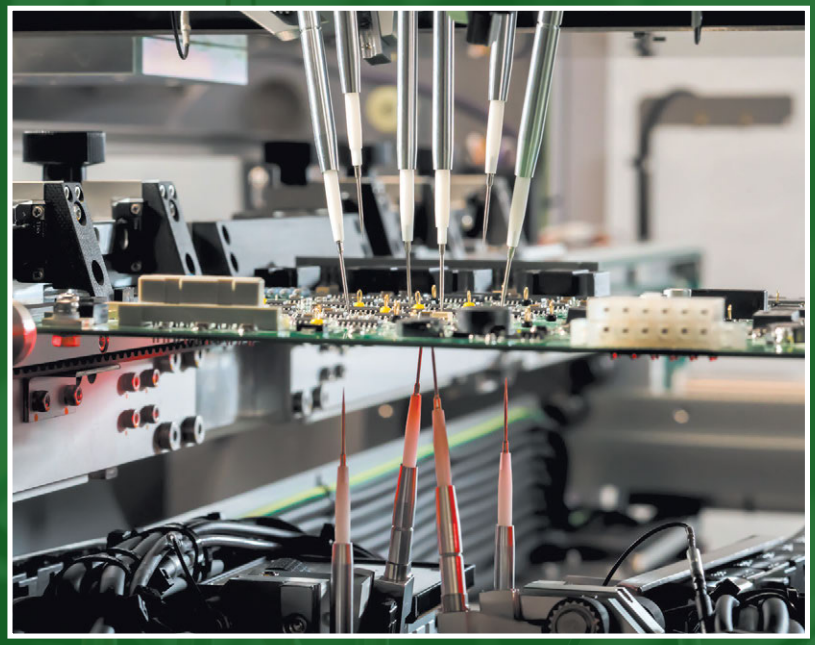

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ROI

A Taxing Moment in History

Tariffs always have an effect. It's usually not the intended one.

TELL ME IT isn't so. Tell me we are not going back, excuse me, that's backwards, to when I began my career in the 1970s! As you age, you remember the way things were, for better or worse. And in my case, add being a student of history, albeit a casual one, as well as a selective packrat of industry periodicals. Together, looking at the current state of the global world of technology, the trajectory certainly appears less forward and more backward.

In the 1970s, America was an epicenter of manufacturing, including electronics and technology. Then Japan and Taiwan began to outperform the US in terms of quality and value. At that time, South Korea, Vietnam, Thailand and even China were not yet mainstream economic engines. The time-to-market for new technology stretched years. While innovation flourished, double-digit inflation hindered any single company or nation from profitably funding significant technological advancements.

Business executives are resourceful, however. Western countries, led by the US, began to study how Japan was transforming its economy into one that produced cost-effective and high-quality products. One of the most notable observations was how Japanese companies began to source components and sub-systems from lower-cost countries. Even more importantly, Japanese companies invested in building manufacturing facilities in lower-cost countries and taught the local workforce how to produce the quality products the Japanese required. By observing and copying the successes that Japan and Taiwan enjoyed, the modern global supply chain came to life.

Since the 1970s, companies around the world have developed global supply chains for virtually all products. These supply chains offer several advantages, including the ability to collaborate across different parts of the world, which creates a 24/7 workforce. This collaboration has significantly reduced time-to-market to months from years. Additionally, when product development teams are international, they account for the tastes, needs and unique preferences of consumers worldwide, resulting in products that truly appeal to a global audience. These two examples have dramatically reduced cost-to-market, while enhancing global product demand to enable scalable manufacturing, resulting in much lower unit costs. In short, a win-win-win for consumers, companies and countries!

Even in successful endeavors, however, imbalances can occur. Currently, certain specific technologies and industries need a better mix of imports versus domestic production. When we identify such imbalances, focusing on them has proven successful in the past. The CHIPS and Science Act, enacted by Congress in 2022, serves as an example of this approach to rebalancing critical needs. By implementing legislation similar to the Chips Act, rebalancing can take place without destroying the long-evolved and highly efficient global economy.

But now, these highly efficient supply chains that support global economies face threats from tariffs that one leader believes will revitalize its manufacturing industries. Regrettably, bulk, across-the-board tariffs have never worked. Worse, the taxing country loses more than the nation it taxes. The Smoot-Hartley Tariff Act, which the US Congress enacted in 1930, led to the collapse of international trade, prolonged the Great Depression and served as a catalyst for World War II.

Over the years, selective tariffs have worked, but only when implemented with the precision of a surgeon, not a lumberjack. Even then, free-trade biases have discouraged tariffs. Two decades ago, the June 2004 *IPC Review* recapped the IPC Capitol Hill Day, where Rep. Donald Manzullo (R-IL), chairman of the Committee on Small Business, stated, "Tariffs don't work." He discussed how tariffs raise costs and reduce supply of impacted materials. The results of 1930 and 2004 are harbingers of what could come.

Yet one government's worldview may regrettably take everyone on a long, torturous journey back to the 1970s. Like a bumpy rollercoaster ride, markets will reel, shortages of critical items will develop and many common consumer products will disappear from store shelves. Costs for everyone will rise and time to market will equally suffer.

If the global industry has patience and sets a positive example by encouraging collaboration, we may be able to mitigate the disruptions that history suggests are likely to occur. Hopefully, we will wake up from a bad dream and resume thriving as part of a highly efficient global economy in 2025, not the 1970s!

PETER BIGELOW has more than 30 years' experience as a PCB executive, most recently as president of FTG Circuits Haverhill; peterbigelow@msn.com.

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BOARD BUYING

Thailand PCB Manufacturing Progresses but Needs Time to Mature

An in-person visit reveals unrealized potential.

IT'S BEEN ALMOST two years since the authors' first visit to Thailand, which occurred just after Covid travel restrictions were lifted. We first reported on our impressions of Thailand's PCB manufacturing environment in August 2023.

On our first visit, ground was just being broken on several large facilities funded mostly by Chinese parent companies. These new plants are located a few hours outside Bangkok in large industrial parks with wide roads and plenty of land between neighboring factories.

On what was cleared land just two years ago, newly constructed modern facilities now stand, with room for an additional building or two. These new factories have large floor plans for each of the major processes involved in making a printed circuit board.

Some of these factories are designed with environmental sustainability in mind by collecting the abundant rainwater that seasonally falls on the facility roofs for eventual use in the PCB manufacturing process.

The equipment in these facilities is the latest and greatest. The plating lines are long, brand-spanking new and do not have the usual obnoxious odors wafting about. Back in the day, the plating lines (also known as "wet process") often were accompanied by wet floors. But these new Thai facilities are dry and immaculate.

Autonomous guided vehicles (AGVs) are readily available to take manufacturing panels from one department to another **(Figure 1)**. These AGVs even have their own special mini elevator system to take them from floor to floor.

Figure 1. AGVs are commonplace at new Thailand PCB factories.

Many facilities have all this great equipment, but do not possess enough of it. They are in the first phase of gradually increasing production volumes, expected for now to produce about 40,000-50,000 sq. m per month, using about 300 employees each.

Rooms set up to house eight laser drill machines have only two installed. A room that holds a plating line, be it for the inner- or outer layer process, has capacity for two more. Each department – automatic optical inspection, drilling, routing, press – has plenty of space for more equipment to add as demand increases.

Yes, they are operational and actively building quality product, but they are not at capacity, even with the limited amount of equipment installed. Many of the AGVs were standing idle when we visited because of the lack of work on hand.

While Thailand has been mostly known for low-mix, low-to-medium technology PCB manufacture, these new facilities are gearing up to take on higher-mix and higher-technology boards that are more conducive for sales to the US market.

With over 20 large PCB facilities currently manufacturing or about to begin operations in Thailand, machine operators, engineers and chemists – *who are experienced in PCB manufacture* – are in high demand.

High demand means short supply, and many of the established domestic factories have had technicians and engineers hired away by other manufacturing newcomers. And the available personnel have little or no proof of actual IPC

training or certification.

It was interesting to note during our visit that English was the common language spoken between Chinese management and the local Thai workers. Language is still the greatest barrier, meaning it will take more time for a factory to become a cohesive operation. Some in management at these facilities estimate that could be as much as a year.

While Thai labor is much cheaper than that of China, the cost for electricity is 25% greater. Many of the chemicals and laminates required for board manufacture still come from China, which adds to the cost.

While Thailand does manufacture raw materials, it is not enough to support the burgeoning industry. A major Chinese laminate supplier intends to open a new facility by year's end to hopefully ease the burden.

All that said, pricing for PCBs manufactured in Thailand is 15-20% higher than in China.

For now, the 25% US-imposed Section 301 tariffs for all PCBs manufactured in China do not apply to PCBs manufactured in Thailand. That is good news for US buyers, but the average time to receive a quote and for an order to ship is much longer, averaging six to eight weeks.

In comparison, China will quote a PCB in a day and will ship most product in three to four weeks or less.

And don't forget, a 10% reciprocal tariff exists between the US and Thailand. As of the time of this writing, higher tariffs imposed on Chinese goods are on hold, and it's unclear whether they will continue.

In our estimation, a total cost of ownership difference of only 10-15% will give pause to many buyers wanting to move work from a known supplier in China, where they likely have buying leverage, to an up-and-coming factory in Thailand.

The next 12-18 months will determine how successful Thailand will become as a PCB manufacturing player. It is not from the lack of investment, as there seems to be no shortage of monies pouring in. Instead, the politics, tariffs, struggles with labor and shoring up of the internal supply chain will determine the outcome.

GREG PAPANDREW and **CLEMENT YUAN** are cofounders of DirectPCB (directpcb.com) and can be reached at greg@directpcb.com.

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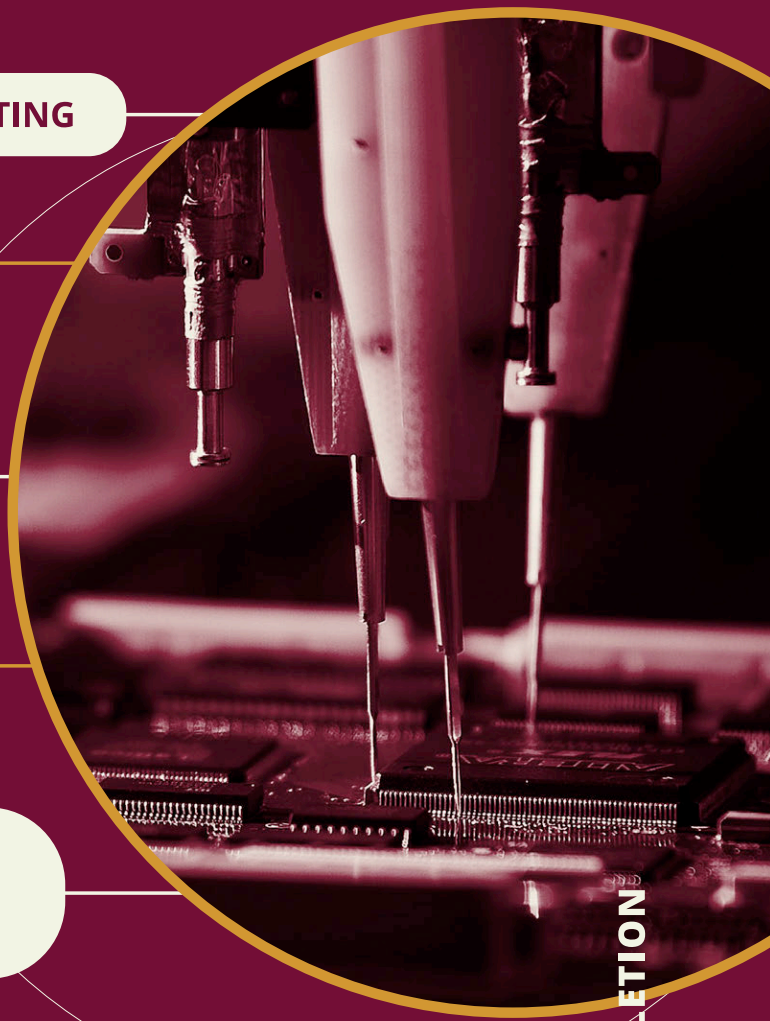

CONCEPT TO COMPLETION

Navigating Paradigm Shifts

2025 is going to have a lot of surprises.

THE POLITICAL WINDS of change present challenges and opportunities for electronics manufacturing services (EMS) companies this year. This shift creates many challenges for EMS program managers. My April column discussed how to address customer tariff concerns. Here I will focus on the dynamics of market uncertainty.

IPC's April market trend data provide valuable insight into changing dynamics in the manufacturing sector. According to the US Federal Reserve, domestic factory output was up 0.7% year-on-year in February, predominantly driven by an 8.5% surge in motor vehicle production. US output showed renewed weakness in April, however, with the Purchasing Manager's Index (PMI) declining to 48.7 from a year to date high of 50.9 in January. IPC's EMS book-to-bill ratio data show shipments rose 0.2% in March compared to the previous year, while bookings climbed 12.7%. April orders pushed the EMS book-to-bill ratio to 1.37, its highest level since November 2022.

So, what do these contradictory data mean for program managers? The short answer is that customers are reacting to market uncertainty. Tariff concerns have incentivized material pull-ins to get ahead of tariff cut-ins. Since tariff rates have become a matter of negotiation rather than fixed policy decisions, this situation adds another layer of uncertainty to the market, complicating the program management role. Nevertheless, one rule of program management never changes: you can't control what happens, but you can control how you respond.

First, let's look at the impact of uncertainty on customer orders. Tariffs drive the need to understand price elasticity of demand. Some products are inelastic, meaning that the product is so necessary that consumers will continue to buy it at similar levels regardless of price increases or decreases. Other products are elastic, meaning that demand decreases or increases when prices rise or fall. Consequently, program managers should review their programs to determine under which category the products are likely to fall. Programs with inelastic demand such as defense, industrial infrastructure and medical products will likely perform to forecast. Natural disasters such as those experienced last year and this spring may drive ordering spikes in some industrial infrastructure. Comparatively, programs involving products consumers buy with discretionary income are likely to be pushed out, because these products are elastic and demand will drop as prices increase. Material availability may also fluctuate. There is already a spike in demand for components from countries with the lowest tariff rates. Reduced demand for products bought with discretionary income may partially offset this.

Do your homework. Program managers should work with their purchasing teams to better understand changing availability trends and options, particularly for programs with inelastic demand because these steady runners are going to be critical to achieving near-forecasted revenue levels. When dealing with programs that involve products

with likely elastic demand, review the material related to orders, on-hand inventory, forecasts and contract terms. Discuss market conditions with customers and determine if there is demand softness that could lead to changes in agreed-upon forecasts. If a customer needs to push out the schedule, have an internal discussion on any contractual customer obligations (such as buying excess or inactive inventory) and decide if negotiation is necessary.

On the opportunities side, OEMs are going to be shopping to price out supply chain realignment scenarios. But much of this activity is likely to be "what if" scenarios rather than a sincere effort to select new suppliers until tariff policies stabilize and become predictable. Southeast Asia and Mexico will likely emerge as winners in this realignment, and if India opens its markets, it may also benefit. US manufacturing is set to see a reshoring of projects that never suited offshore settings. If tax policy changes to further benefit Made in USA manufacturing, this opportunity could expand.

Sales teams should do their homework on potential customers to determine how serious these prospects are on changing supplier location versus simply developing a pricing model. This diligence will help avoid wasting resources on quoting exercises or prioritizing quotes that cannot win over those that can. That said, increased shopping translates to increased opportunities to get on the radar screen of companies that may be serious prospects longer term. If there is a potential fit, it's worth building a relationship and staying in touch even if the initial interaction is a pricing exercise.

In short, 2025 is going to have a lot of surprises. Program management and sales teams who carefully watch trends and strategize the best responses are going to have better outcomes than teams who simply react as their customers react.

SUSAN MUCHA is president of Powell-Mucha Consulting Inc. (powell-muchaconsulting.com), a consulting firm providing strategic planning, training and market positioning support to EMS companies and author of *Find It. Book It. Grow It. A Robust Process for Account Acquisition in Electronics Manufacturing Services.* She can be reached at smucha@powell-muchaconsulting.com.

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Designing for High-Pin Count Devices

Overcoming "anywhere but here."

AS THE DEVICES shrink in pitch and increase in pin count, current density becomes a concern. The outer rows of devices typically have lots of signal pins, while center pins focus on power and ground. This situation means that designers must reserve the first few layers of the board specifically for fan-out **(Figure 1)**.

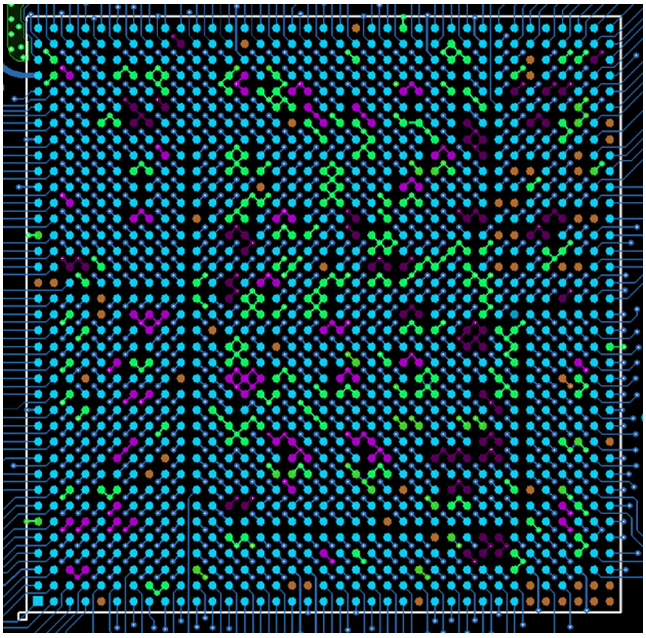

Figure 1. Just your average 1,369 pin FPGA using a 1.27mm (0.05") pitch. In terms of colors, green indicates the primary ground domain. Deep purple represents where heavy metal is desired for high current. The lighter magenta is a lower wattage, more spacey kind of metal (like Pink Floyd). Orange marks the no-connect pins.

One of the worst mistakes when dealing with a BGA of 1,000 pins is to drop a via deep into the board for pins on the device's edge. Be ready to use every lane of the first three layers, and route layer 2 through the air gaps between the other two.

The point is to get away from the device until the trace gets a chance to join the normal flow of the routing channels. You have two distinct areas: the fan-out zone and everything else, where routing up, down, left and right makes sense **(Figure 2)**.

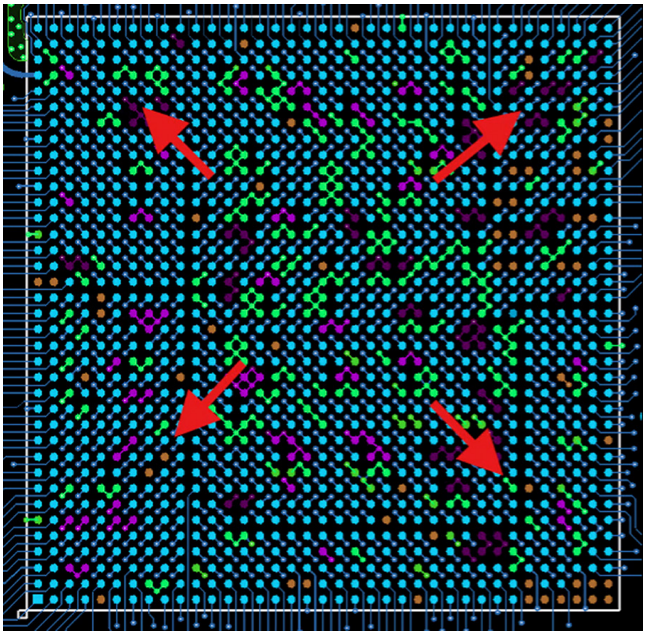

Figure 2. The first thing is to address the outer ring(s) where the top layer is used to escape to a via for the internal routing layer or to a nearby component that is placed there for that reason. The arrows indicate the fan-out flow, always away from the core. For the sake of rework (and room for the fan-out), a component-free area around the device will make it easier to desolder if it needs to be replaced. Otherwise, the tech has to remove the nearby components first.

Find your beach and drop a via that takes you to a level where the current is going your way. Until the vast majority of connections are handled that way, routing between component clusters makes no sense. Fan-out is early in the timeline and updates to the schematic are probably on the table. It's much easier to move or edit a group while isolated from the rest of the board.

Route the outer ring of pins to "anywhere but here" using the outer layer of the board. If space permits routing between the pins, then the second ring of pins should also escape on the outer layer. If there is no room for that, like with a 0.4mm pitch, then the next layer down is the best option, even if it's the traditional ground layer.

Conventional wisdom suggest routing orthogonal to traces on the adjacent layers. In reality, that's a nonstarter on the edges of a pin field. The right routing direction radiates far enough away from the center of the device to connect to components placed around it or to a via where we can start adhering to regular routing according to each layer's purposes.

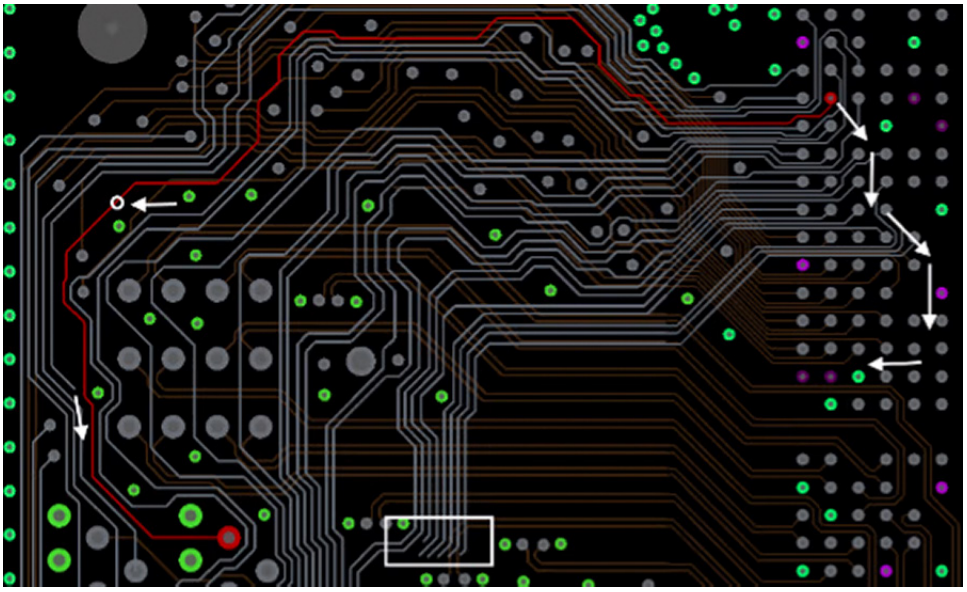

Figure 3. This trace in red is eating too many vertical routing channels. One option is to drop a via in the upper left corner and wrap around the differential pairs on the horizontal routing layer. The other option is to use the same brown layer all the way and follow the arrows on the right, routing under the FPGA to the point where only two traces pass through the fan-out vias. From there, routing goes all the way around the high-speed lanes. The first option seems like less work.

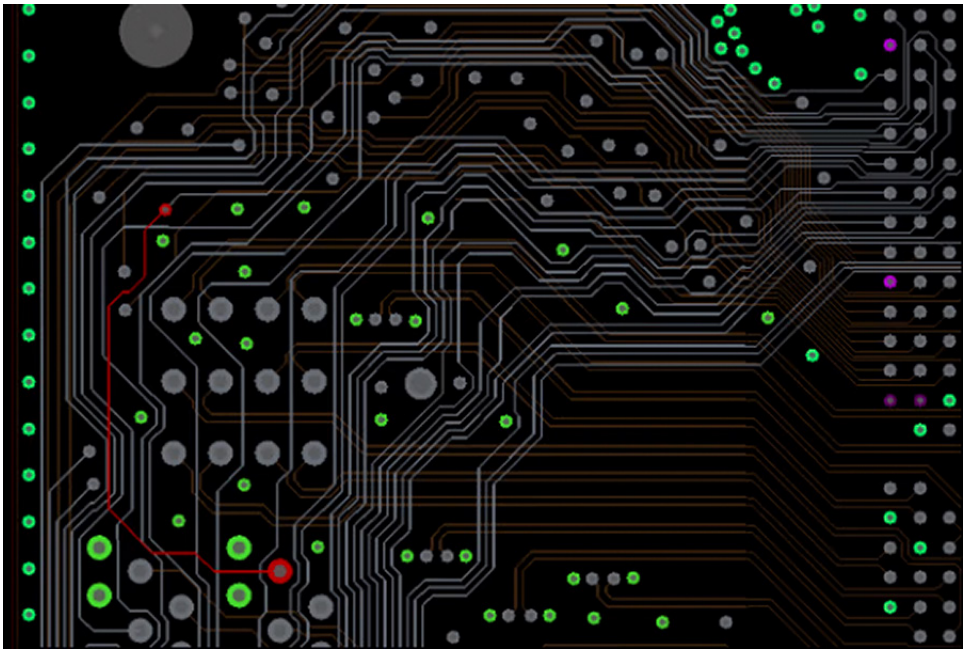

Figure 4. The strategy around horizontal and vertical routing layers is knowing when to break away from the trend. The little box full of dangling lines has enough lanes to proceed with a minor revision to the trace. Obstacles such as shields, slots and board edges can be a place to route counter to the prevailing directions as a matter of necessity.

If a PMIC device has external oscillator pins, they are likely buried deep inside the BGA pin field rather than on the perimeter where we like them. Are you going to have headroom for a crystal on the far side of the board? Some internal routing might be involved in getting to the crystal.

In that case, I recommend using a guard band around those traces. Like almost every other component, placing the PMIC near the SoC makes sense. This practice minimizes signal degradation, similar to how engineers position a single regulator near the pins that use the power supplied to any chip. In the case of a PMIC, such concerns are numerous.

With the power domains and essential routing behind us, we can finally close the schematic and play connect the dots using the two innerlayers for vertical and horizontal routing lanes. The unrouted segments have no remaining length or width requirements. My guess is the average person would think this is the nature of most, if not all, routing solutions. This belief has become less common as the percentage of constrained nets has grown over time.

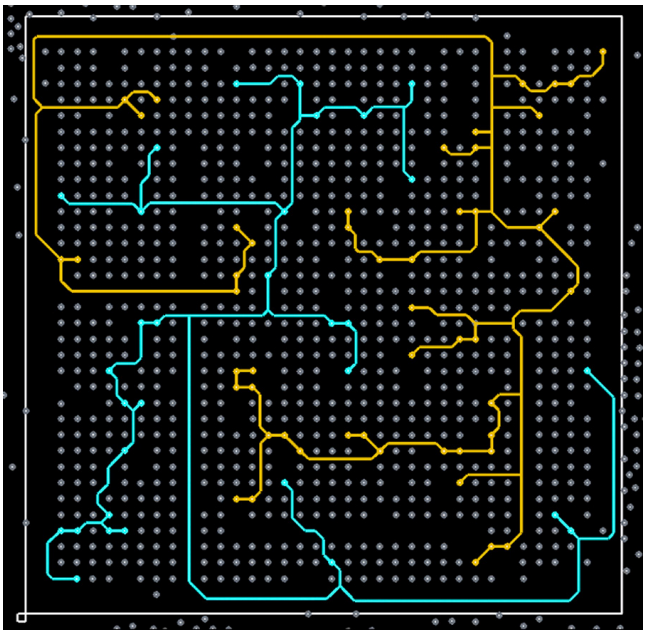

Figure 5. Both power domains can be connected without overlap. If it weren't obvious before, it's now clear we can supply the two main power domains with shapes on this layer based on the routing study. The shapes will fill in to distribute the voltages with minimal neck-down. (As we would most likely be using dynamic copper for the power planes, the traces would remain as a backbone. Although they are not close to sufficient in terms of width, they will prevent a future trace from splitting the plane entirely, in case additional routing ends up on this layer.)

Closing those last traces can be a chore as all the good routing channels seem taken. Sometimes, the routing goal becomes "anywhere but here." You might start at both ends and route a meander as far as it goes in any direction. Along the way, you might have to be "impolite" with the existing work. If the two ends can cross each other at some point, then the routing solution is only a via away. On a 95%-routed board, that still may be a problem. I remember

spending 20 minutes clearing out space to add one ground via. Such is life under an NFC chip of a phone.

The fan-out is a chance to make minor adjustments to the placement. This effort continues throughout the fan-out and routing steps. There's always some guesswork as we go about making design decisions. We're not always right, but we're always ready to make it right when new information comes to light.

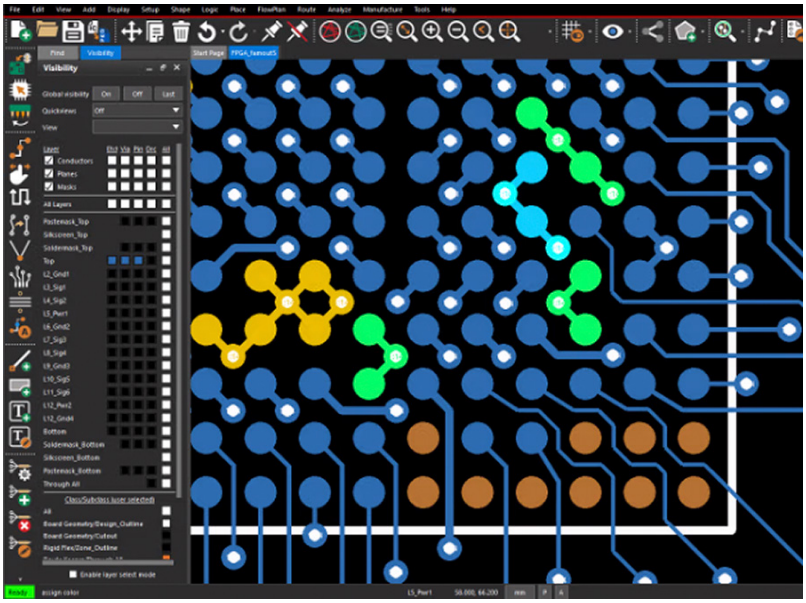

Figure 6. Re-examining this unused MIPI corner getting two more vias out of the grid. If only one trace may be routed between pins/vias, ensure you do just that. Get a trace through every gap. We can depressurize inner layers in the same way. This applies to pin grid connectors as well as BGA devices. Maximizing each layer's number of connections is how layer count is reduced to something more feasible.

Preliminary routing. Cross-probing and selectively displaying or colorizing nets provide insight into what's to come. Although we've checked off on the placement gate, it's a good idea to maintain elasticity for as long as possible. Modularity proves useful when the inevitable update makes it necessary to relocate or rotate a device and its constituent parts.

That said, we must begin connecting the various devices at some point. The heaviest hitting device on the board is a good place to start. It could be key because it uses the most power or has the most interconnects. It may also be the main amplifier or whatever motivates the product. Every board has a device at its heart, so that's where risk management begins. We must start somewhere.

Step one is the highest priority net on the highest priority chip. It will all be downhill from there; working toward the least significant connections. Operationally, I might not even place pull-up resistors until I complete the pin-escape from the device. Once the trace is fanned out and routed to a clear spot for the via, land the low priority part can land. The same can be said for test points. Get away from the dense area and find a home for the test point.

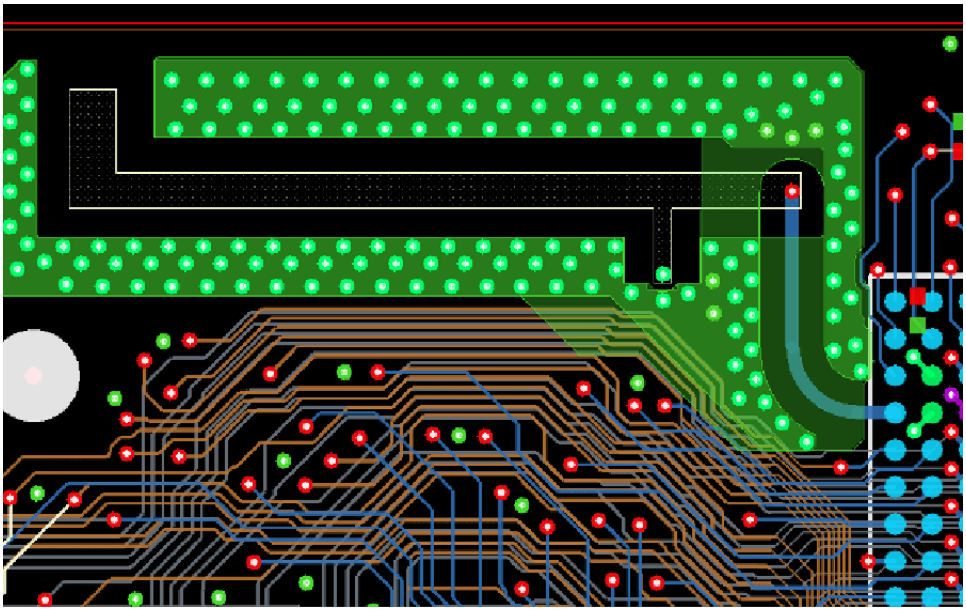

Figure 7. At times, everything else must step aside and clear all layers for a printed antenna. I use a net short property to tie the antenna shape and the ground via so that the two can coexist at DC and the antenna's frequency. Like most of these slides, this is made entirely from scratch. The takeaway: Ground vias are always in demand around features like this one.

Like going back to the good old days, we're using the organic, free-range kind of intelligence that comes straight from our brains. Sometimes it helps to flip the bit. Mirror the board's image. Soften the color palette. Make it easy on yourself. I hope many of you remain blessed with the option to work from home.

Either way, consider via stubs when doing the fan-out. If the chip is on layer one, then you should use the higher layer numbers for diff-pairs and similar routing. If the route is on layer 3, a stub will run from 3 to the bottom. Avoid back-drilling whenever possible, as it can become a signal integrity thing as layer count increases.

JOHN BURKHERT, JR. is a principle PCB designer in retirement. For the past several years, he has been sharing what he has learned for the sake of helping fresh and ambitious PCB designers. The knowledge is passed along through stories and lessons learned from three decades of design, including the most basic one-layer board up to the high-reliability rigid-flex HDI designs for aerospace and military applications. His well-earned free time is spent on a bike, or with a mic doing a karaoke jam.

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Lateral Thinking and Simplicity Can Power Our Quest for Decarbonization

Can today's sustainability drive turn on a solution from the past?

AS GLOBAL TRADING and economic power dominate the news, it's essential to consider the significance of the world's electric vehicle markets in these developments. Western and Japanese car manufacturers are realizing that China has a huge lead in electric vehicle technology and a large, receptive domestic market that fuels the success of its local brands.

Brands that historically relied on strong exports to China may never recover the ground lost against these emerging domestic players, which offer cutting-edge products at lower prices. Chinese industry data calculate that battery EVs already represent about 25% of the country's new car market and that China has been the world's top producer in the new energy vehicles category for the past 10 years consecutively.

EV technology has rapidly advanced, with key targets focused on increasing driving range and reducing charging time. Range anxiety remains a significant barrier to widespread EV adoption and has resulted in vehicles equipped with large and heavy batteries. Their weight and bulk can compromise drivability and cause technical and environmental problems. Moving the vehicle demands a large quantity of energy, even though the powertrain may achieve extremely high energy-conversion efficiency.

Additionally, tire stress and wear increase, and producing the batteries demands large quantities of strategically important minerals like lithium. As the first wave of large-scale EV adoption reaches the end of life for many batteries, we will face urgent challenges with battery disposal and reclamation of valuable materials.

An abundance of hydrogen. If larger batteries are not a good long-term solution, hydrogen may offer an alternative power source. It's much lighter in weight and has acceptable energy density. As the most common element in the universe, there is none of the scarcity challenges associated with lithium or fossil fuels. On the other hand, how clean hydrogen is depends on how it's made. One method, electrolysis, splits water using electricity from renewable or nuclear sources – this is considered cleaner. Another method, called methane reforming, is more common today but produces a lot of CO_2, which harms the environment. These production methods are the reason hydrogen is labeled by color: green and pink hydrogen come from cleaner sources, while gray hydrogen comes from reforming and is less environmentally friendly.

Perhaps electric road systems (ERS) could offer a solution. Leveraging inductive charging, ERS lets electric vehicles go further with smaller batteries. Researchers in Sweden have built short stretches of experimental roadways and run

simulations that suggest a combination of home and dynamic charging could shrink car battery sizes up to 70%. Clearly, ERS will be expensive to install and maybe viable only in urban areas, although the Swedish team reckons the system could be viable if only 25% of the road network is converted.

There's a cool piece of lateral thinking at the heart of this idea. Since the beginning of the automobile age, the vehicles we drive have carried their energy source. Semantically, it's a defining principle, but ERS flips the concept on its head by taking the energy source off the vehicle. This enables lighter and more affordable EVs with extra range, something that traditional methods have struggled to achieve so far.

Historical precedents. Like many of the technologies currently being explored and developed to support a sustainable future, there are historical precedents. The San Francisco cable car system provides an example that dates from the 1870s. Cables running in trenches are driven continuously at 9.5 miles per hour, each powered by a DC electric motor, while the cars are simple and unpowered. An operator on board manually clamps the vehicle to the cable when it is time to move. Through the 20th century, people began to phase out the system until they acknowledged its cultural significance and preserved the remaining routes. The three surviving lines are still operating today, carrying passengers and sightseers to their destinations.

You may have noticed I've moved the goalposts, as the cable car system is an example of mass transit and not personal transport. Its simplicity is admirable, however, and this enabled the engineers to deliver a service of great value to the community using the limited capabilities of the time.

Similarly simple, functional and extremely environmentally friendly, are water-powered railways. Several are operating in different locations worldwide, including Braga in Portugal, Fribourg in Switzerland and the Lynton and Lynmouth Cliff Railways in the UK. Designed to carry passengers to the top of the steep coastal cliff, the Lynton and Lynmouth system comprises two carriages linked by a cable and consumes no power at all. Each carriage has a large tank filled at the top station using water from the nearby West Lyn River as ballast. The intricately engineered brakes are used to control the system as the heavy top car descends, which raises the lower car. At the end of the descent, the water is released and the other car is filled, permitting the process to repeat continuously.

Although the cliff railway has an extremely low carbon footprint, there would have been no such environmental imperative at the time it was built. A lack of funding is quite likely to have driven the unpowered design. Although ingenious, it was not widely copied. Today, under pressure to decarbonize, we should let ourselves be inspired by engineering like this as we seek to create solutions that are functional, affordable and fossil-fuel-free.

ALUN MORGAN is technology ambassador at Ventec International Group (venteclaminates.com); alun.morgan@ventec-europe.com. His column runs monthly.


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Beyond the Bend: Practical Guidelines for Flex and Rigid-Flex Design

A bend radius lower than the recommended minimum needs a closer look at the details.

IT SEEMS SELF-EVIDENT that designers create a flex or rigid flex because the part must bend. That does not tell the whole story, however. We need more information to ensure the design works in the application as intended.

For starters, are we talking "Use A" (flex to install), or "Use B" (dynamic flex)? I estimate that 95% or more of the flex designs are Use A; truly dynamic uses are rare. Let's talk first about flex to install.

For flex to install, rules of thumb are well-defined. IPC design guidelines establish that for 1- and 2-copper layer circuits, the bend radius should be at least 10 times the thickness of the flex. For circuits with three or more bonded flex layers, the rule of thumb is 20 times the thickness. The key for parts with multiple unbonded flex layers is to select the thickest set of bonded flexes for the radius assessment. For example, if the part is five flex layers but is unbonded between the second and third flex layers, making a 2- and 3-layer section, do your assessment on the thickness of the 3-layer portion, not all five layers.

The guidelines ensure the copper in the stackup does not experience significant plastic deformation during the bend process. In many cases, a small amount of deformation may be acceptable, especially if the application is truly "bend to install" and does not move again. If you expect some type of movement for servicing, it's better to use more conservative values.

Keep in mind, these guidelines are intentionally conservative because they consider all possibilities, including bend angle: 45°, 90°, 180°, etc. Material selection and artwork patterns on each layer can also impact performance. If the bend radius ends up lower than the recommended minimum, take a closer look at the details.

Bend angles less than 90° are more or less a non-concern. I don't recall ever seeing failure on a part bent less than 90°. For 90° to 180° bends, use a fixture to control the bend process to ensure a repeatable process with a controlled radius.

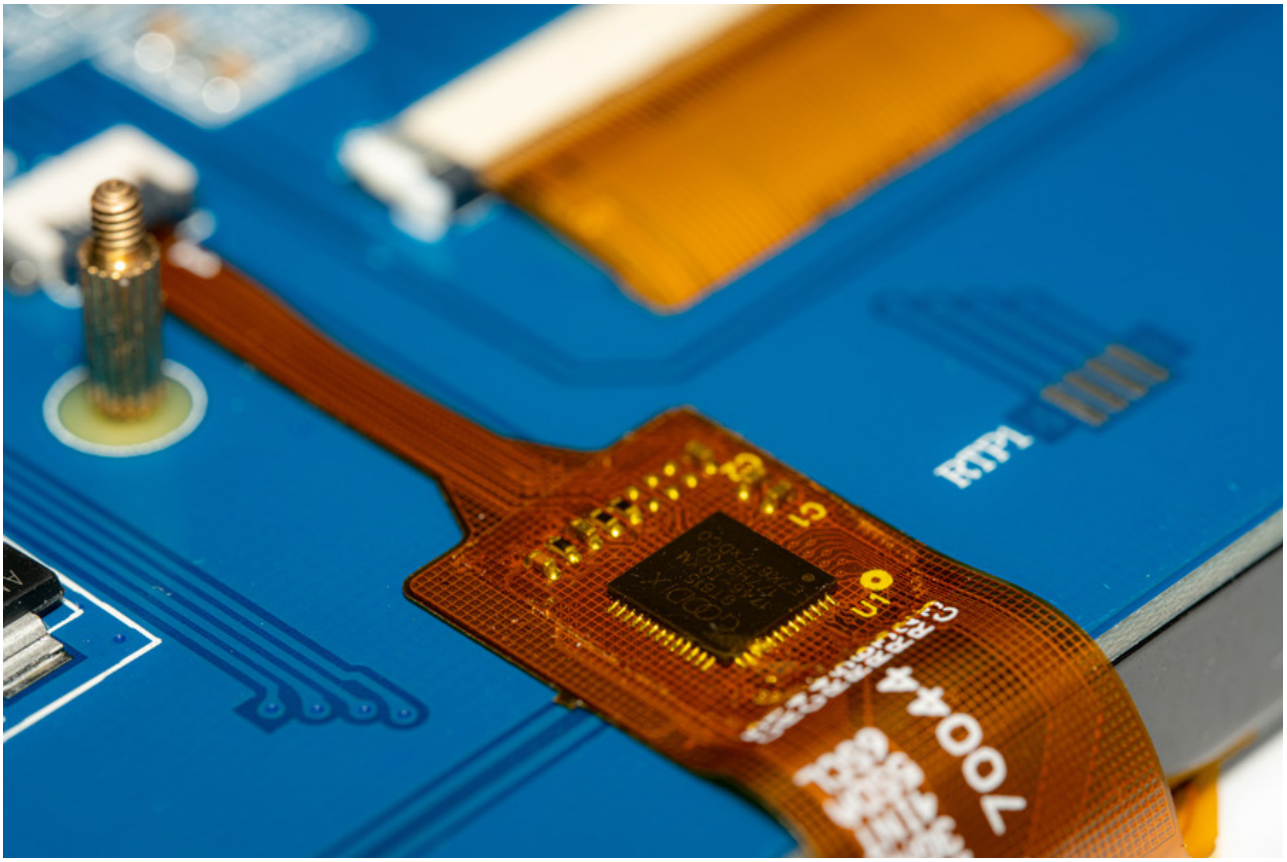

Figure 1. Bend angles less than 90° are typically a non-concern.

Generally, we want the layer with the narrowest traces to be in the middle of the stackup along the neutral axis of the bend. The neutral bend axis defines the point in the cross-section where no compression or tension exists. If signal traces can go there, the radius can get quite tight without risking foil deformation. This is unlikely, however. On a two-layer flex, the center core dielectric usually acts as the neutral bend axis, while the two foil layers experience tension and compression, respectively.

For the two-layer flex, we recommend putting the layer with the thinnest traces on the inside radius of the bend. Experience tells us that traces are more likely to crack under tension than compression. Also, plane layers are unlikely to crack unless severely creased.

In all cases, wider traces perform better. Wider traces withstand tighter bend radii and more bend cycles because any fatigue failures take longer to initiate and propagate on wider conductors. The wider trace can overcome certain grain boundary imperfections.

When working with multilayer flex, the same idea applies, and it is more common to see the signal layers sandwiched between plane layers for EMI and impedance purposes. This comes with a few advantages. First, the signal layer sits closer to the centerline of the stack and neutral strain. Second, the planes above and below protect the signal layer from torsion stresses on the outermost conductors. Put simply, you need to break or severely damage the plane layer before you can break the internal signal traces.

Some construction options can help reduce thickness. For example, using foils of 12µm and 18µm thicknesses allows

thinner coverlay materials, shaving a few mils off the stack, which is a big deal when working with 10X and 20X multipliers. Using unbonded flex pairs increases flexibility and lets you define the radius based on two-layer construction and 10X rather than 20X.

We have observed that cases with very aggressive bends can be quite successful; however, doing your homework beforehand is crucial. This research can include microsectioning to evaluate the distortion in the radius, confirming that the end-result meets performance needs. Depending on the severity of distortion, you may need to implement some method to anchor the part in place after bending to avoid work hardening the foil.

Dynamic bending presents a different story. The 10X and 20X rules of thumb do not apply. Bend radii must be much larger to avoid work hardening of the copper foil. For dynamic applications, you are usually limited to one or two flex layers unless the bend radius is very large and the range of travel is very limited. There are many permutations of dynamic bending, but here are some examples:

- Coiling and uncoiling a spooled flex
- Opening and closing an S or U bend
- A unidirectional bend (0° to 90° and back to 0°) repeating
- A bidirectional bend (0° to 90°, back to 0° and then to -90°) repeating
- Other custom dynamic moves such as one end of a board staying stationary and the other moving slightly up and down.

All these are impacted by the number of expected cycles as well as the frequency and speed of the bends.

Dynamic bend designs clearly need the copper as close to neutral as possible and use the thinnest, most flexible construction practical. These are almost always validated with an endurance test. While a couple standards exist in the test methods, custom test systems often emerge to emulate the real bend mechanism. Generally, the ability for the part to meet the bend requirement is almost entirely design related. Manufacturing process variations are rarely a factor. So, it is very important to mind all the details when optimizing for a tight bend or dynamically moving flex. As always, if you have a good relationship with your fabricator, lean on them to help make the best possible choices.

NICK KOOP is director of flex technology at TTM Technologies (ttm.com), vice chairman of the IPC Flexible Circuits Committee and co-chair of the IPC-6013 Qualification and Performance Specification for Flexible Printed Boards Subcommittee; nick.koop@ttmtech.com. He and co-"Flexpert" **MARK FINSTAD** (mark.finstad@flexiblecircuit.com) welcome your suggestions. They will speak at PCB West in September.

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RF DESIGN

Bluetooth Circuit Board Design Guidelines

Six steps for limiting interference and data loss.

by ANDREW GONZALES and JASON METZNER

Printed circuit boards (PCBs) utilizing Bluetooth technology can encounter issues like interference, lost data and poor signal integrity if certain precautions aren't taken. This guide outlines essential rules and guidelines for selecting Bluetooth technology for various applications and, more specifically, for integrating it into circuit boards.

A variety of applications utilize Bluetooth, including:

- Beacons used in shopping malls
- Eddystone frames for industrial sensing applications
- Headsets and audio/stereo products
- Remote peripheral devices such as video game controllers or computer mice/keyboards
- Home automation systems
- Wireless consumer electronics applications, including cameras, printers and phones.

Each application incorporates the same common Bluetooth technology but adapts it based on connection types. Design engineers must apply fundamental principles to optimize signal integrity and enhance overall device effectiveness.

While Bluetooth is not as fast a wireless choice compared to Wi-Fi, it is getting faster. Its performance declines when obstructed by walls or nearby objects, and range is limited.

Despite these challenges, Bluetooth remains a strong choice. The latest version, 5.0, shows significant improvements over 4.2. Overall, Bluetooth provides a low-power, reliable and secure solution that integrates easily into a range of small peripherals.

Bluetooth has been around for more than 20 years and is still evolving, and although it's improved in speed, power, range, security and other attributes over the years, some of the issues seen at its conception in the mid-90s remain, including its susceptibility to signal interference.

So, what can be done from a PCB design standpoint to optimize signal integrity, minimize interference and lost data packets?

Here are a few Bluetooth circuit design considerations and general rules of thumb:

1. **Use certified modules.** When incorporating Bluetooth into a product with limited resources, consider a pre-certified, fully contained module to accelerate development and reduce time-to-market. While this choice may slightly increase costs, it often prevents headaches related to antenna placement, design issues and EMI susceptibility. Many reasonably priced certified modules are available today, typically featuring a small ARM processor such as the RN4020 or RN4870 from Microchip or the BT121 or BGM113 from Silicon Labs. The on-board processor provides greater flexibility and power, allowing control of simple peripherals through GPIO, SPI, I2C, PWM and more, in addition to managing the Bluetooth stack.

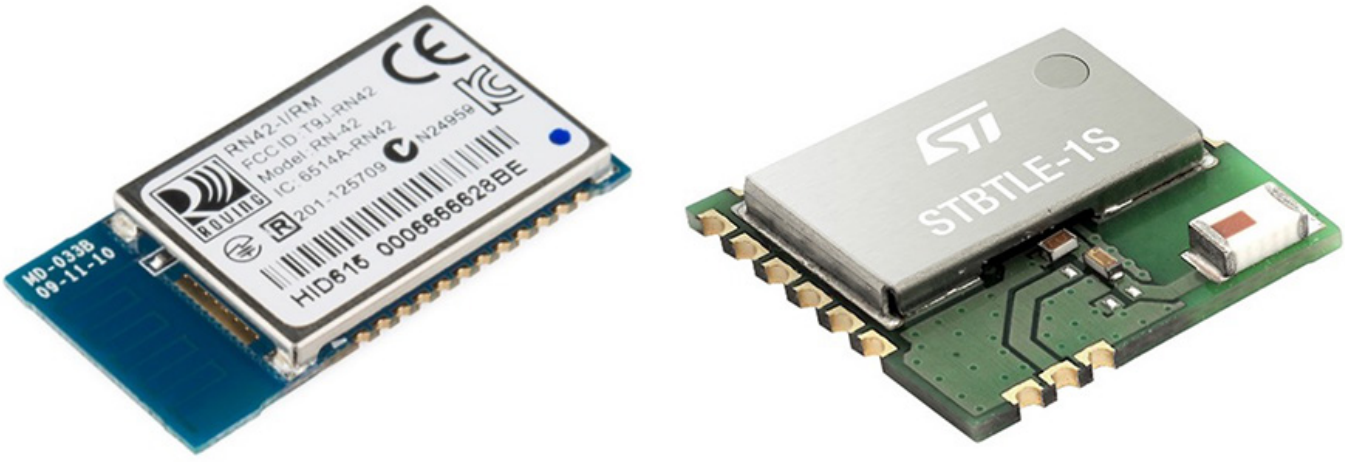

Figure 1. Sample Bluetooth boards.

2. **Check the Bluetooth device selection.** Ensure an appropriate Bluetooth device is chosen for the application and the antenna is appropriately sized and tuned.

   For a simple beacon application requiring short bursts of location or data advertising, opt for a low-power device using Bluetooth Low Energy (BLE). This cost-effective solution minimizes features and peripherals, helping to save on-board space and reduce overall costs **(Figure 2)**.

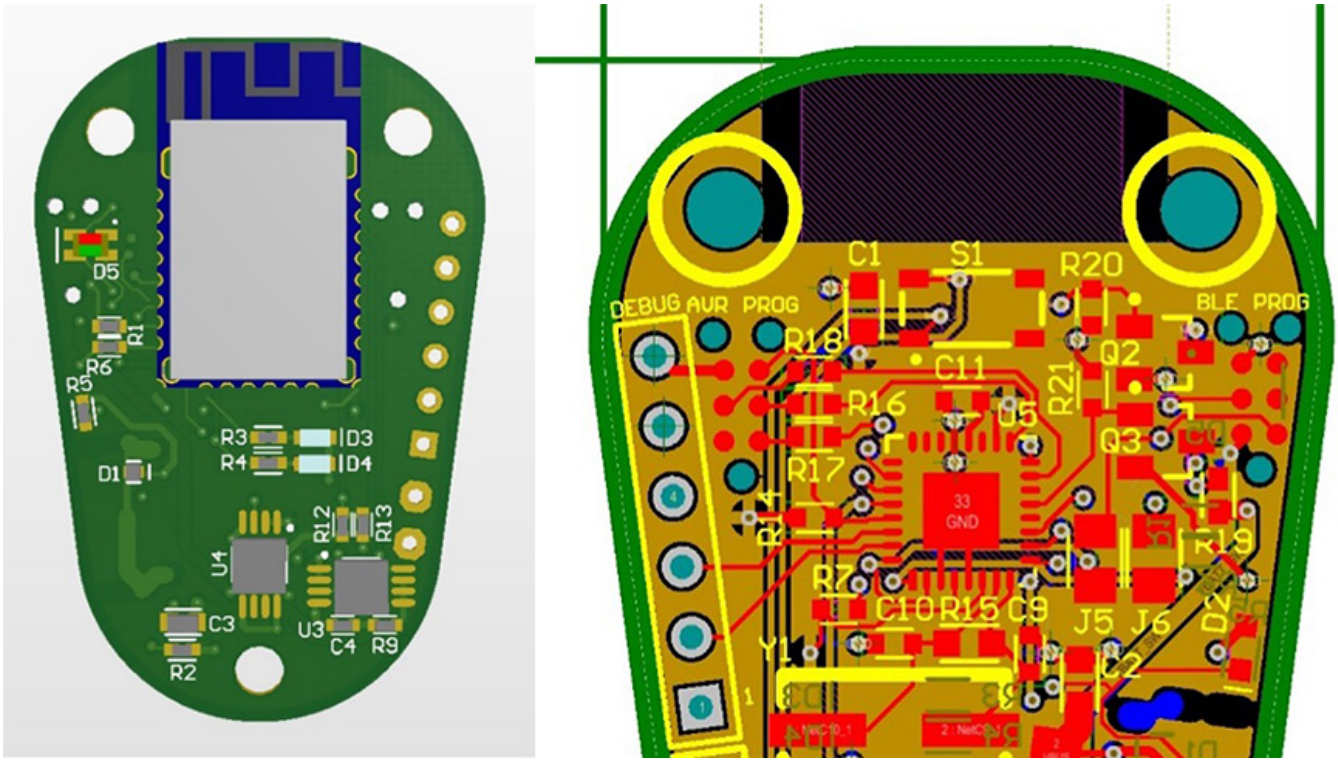

Figure 2. For simple beacon applications, a low-power BLE is a cost-effective solution and can save board real estate.

If a higher throughput, audio-streaming or data-exchanging Bluetooth application is needed, select a device with increased transmit (Tx) power, higher receiver (Rx) sensitivity and a faster data-rate (although slowing the data rate can typically help with minimizing dropped packets).

Need an all-in-one chip? Consider chipsets containing powerful or secondary processors with available UART, SPI, I2C, PWM, ADC, DAC and GPIO pins. If the project relies heavily on received signal strength indicator (RSSI) readings, ensure the device provides adequate decibel (dB) resolution on its RSSI monitor.

3. **Separate or remove copper signals and high-energy components.** When designing in a Bluetooth chipset or module, keep the antenna completely free from nearby copper signals or components carrying significant amounts of energy (especially switched power paths, such as boost or buck converters).

   This includes keeping the area (and board layers) free of planes and polygon pours. Most Bluetooth chipset manufacturers will provide layout guidelines to follow closely during PCB design. When manually laying out the antenna area, use a ground plane as appropriate to keep a good bandwidth at the input and make sure to build in room for tuning elements (a ground plane is required for printed and ceramic antennas).

   Ground stitching vias prevent unwanted radiation from the PCB edge which could otherwise penetrate nearby Bluetooth signals. When possible, optimize the board shape to the Bluetooth device's antenna location, keeping it on the edge and far away from nearby components and signals. If using analog-based signals such as audio, separate analog and digital ground planes.

   And it's always a good idea to shield the electronics (not the antenna, of course) to prevent cross-coupling and

minimize picked up noise.

4. **Consult power supply notes.** Ensure the rail supplying power to the Bluetooth module or chip is clean. Use bypass capacitors (1.0µF) and decoupling capacitors (0.1µF and 10nF) where needed. Additionally, incorporate ferrite beads on the power rail entering the Bluetooth area of the board to effectively reject high-frequency noise.
5. **Tools and analysis.** If designing the antenna area, make sure have the proper equipment (such as a network analyzer) is available to analyze and tune the matching network, or consider sending the design to a third-party RF test lab.
6. **Consider real-world obstructions.** A wide variety of things can cause obstruction or de-tuning during a Bluetooth connection, including nearby water (humans too … we're made mostly of water), metallized objects, smartphones/tablets, computers, devices operating on the same ISM band (such as microwave ovens or WLAN technologies), power sources, wireless RF video, office lighting and home phones.

   The device is highly susceptible to signal loss, even at distances of just 1-2 meters. If there is a higher risk of these kinds of things impacting signal quality, choose a higher power device and operate at a slower speed to minimize packet drop. When electronics are housed in an enclosure, ensure that metallized materials are minimized and positioned far away from the BLE module. The relationship between Bluetooth signal strength and distance is nonlinear and somewhat unpredictable based on the surrounding environment, though it generally follows the pattern shown in **Figure 3**.

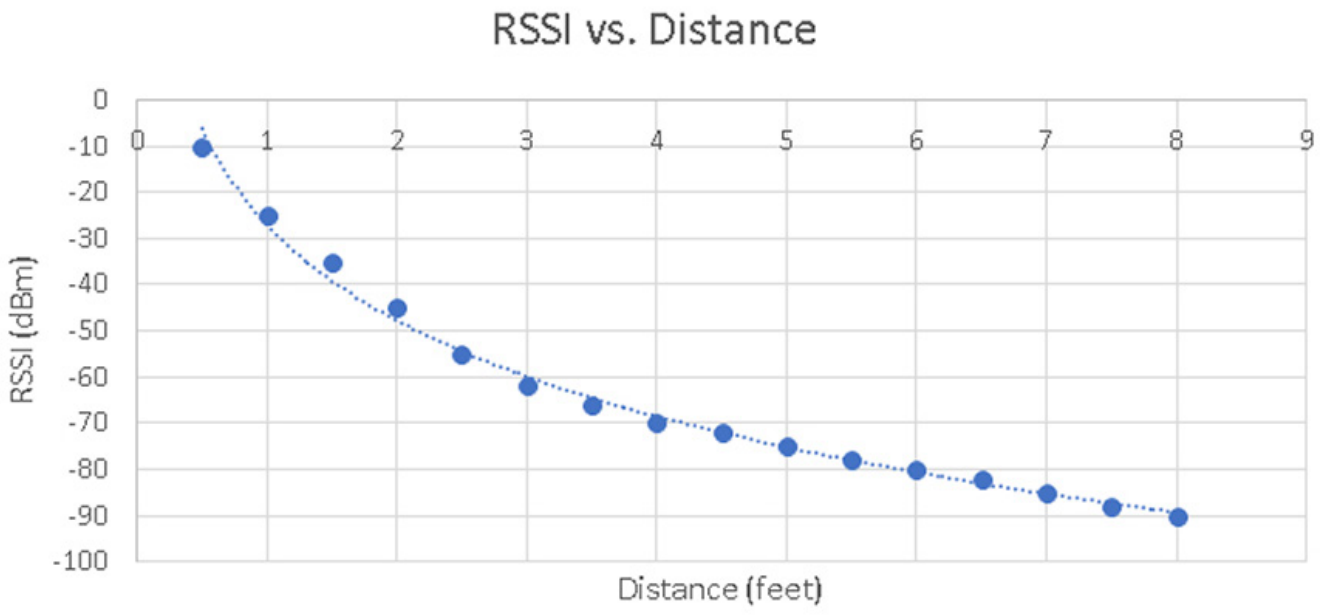

Figure 3. A graph showing the relationship between Bluetooth signal strength and distance.

Whether designing a small, simple Beacon module or a data-streaming, power-hungry Bluetooth hub, following these considerations could save tons of headaches during the test/implementation stage of design.

With the expansion of Bluetooth PCB assembly, it's an exciting time to incorporate wireless communication and control into products, and the future will only bring smaller, faster, cheaper and stronger Bluetooth components.

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CONTROLLING **IMPEDANCE**

Fundamentals of PCB Stack-up and Signal Integrity

A summary of how to order layers to achieve target impedance values.

by AKBER ROY

Printed circuit boards are becoming highly dense, hosting all kinds of high-speed interfaces. The bandwidth of the clock frequencies reaches hundreds of GHz, leading to complex issues related to EMI interference, crosstalk, reflections, jitter and losses.

These new challenges impact all processes involved in design, analysis, manufacturing and testing. Manufacturers employ advanced and complex technologies and methods to accommodate the higher density of functionalities packed into smaller components. To manage losses and achieve desired functionality at higher speeds, research into new materials is leading and revolutionizing this industry. The PCB is at the center of issues related to signal integrity, power integrity, electromagnetic interference, crosstalk, mechanical, thermal and more. It also plays an integral role in solutions for each of these challenges.

These issues begin at PCB stack-up design, since a well-designed stack-up forms the foundation of a strong and stable PCB. It acts as the fundamental backbone of the PCB design structure that impacts signal integrity, power distribution and signal impedance. A sound and properly designed stack-up minimizes the circuit's vulnerability to external noise and helps improve the electromagnetic compatibility of the product **(Figure 1)**.

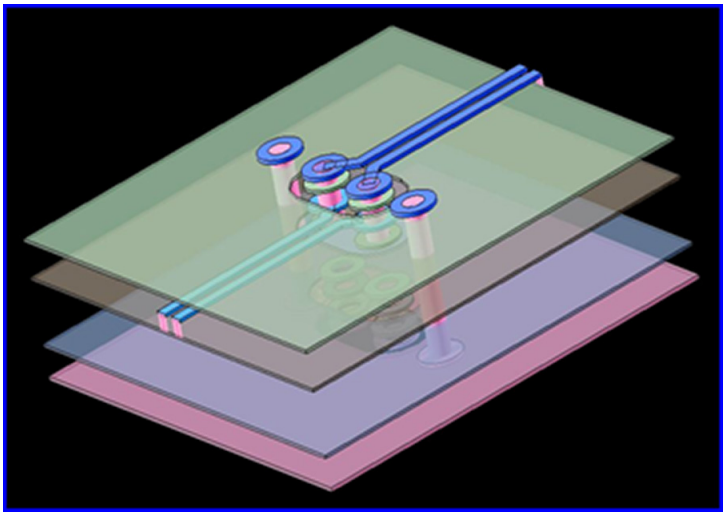

Figure 1. The PCB is the center of a host of electrical, mechanical and thermal issues.

What follows is a summary of some key SI-related points in simple terms, without delving into deep mathematical calculations and complex theories. The stack-up is the arrangement of conductive and insulating layers within a PCB. The total number of layers in a stack-up is determined by the higher pin count ball grid array (BGA) components, complexity of the circuit, its placement and performance requirements. The order of these layers is very important and should be finalized carefully, taking into consideration manufacturability requirements and signal integrity **(Figure 2)**.

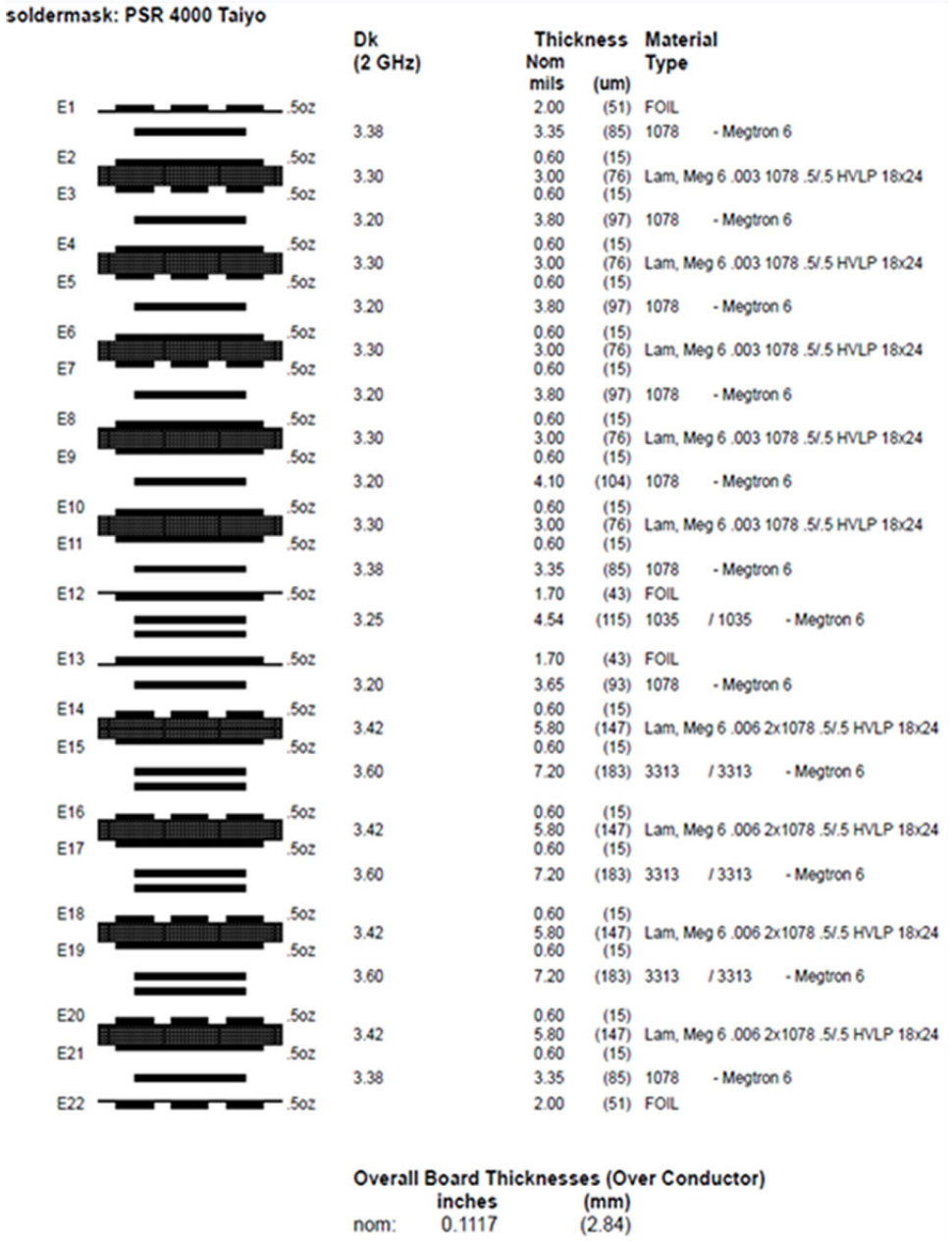

Figure 2. Sample PCB stack-up configuration.

Regarding insulating layers, pay special attention to the properties of the dielectric material and its width. The type of material and its thickness significantly impact signal speed, impedance and losses. These materials play an important role in managing the mechanical and thermal stresses in the PCB, while the width of the dielectric material also contributes to the overall PCB width. Some conductive layers serve as power or ground planes (power/GND), while others function as dedicated signal layers. Designers use plane layers to establish power delivery networks (PDN) and

carry high power signals from the power supply to their respective loads. In contrast, signal layers connect all manner of critical high-speed and other general inter-IC connections. Critical signals, which include high-speed signals on a PCB, require special attention and are highlighted in IC vendor datasheets.

Designers cannot route these signals on just any layer; they must meet specific timing and impedance-based requirements for the product to function correctly. For example, consider memory, the bread and butter of every design. DDR3 memory, for instance, operates as a high-speed interface that contains all types of signals, including data, strobes, address, command, control, status and clock signals. This interface can feature over 100 signals, each with specific timing and impedance requirements **(Figures 3** and **4)**. The strobe and clock signals are differential in nature, while the remainder are single-ended, with different impedance requirements.

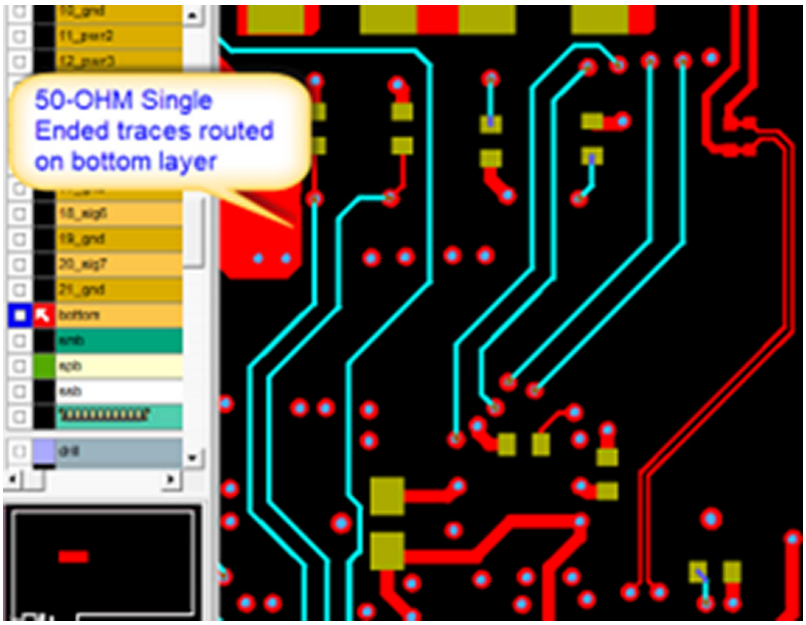

Figure 3. 50Ω single-ended signal routing in DDR3 interfaces.

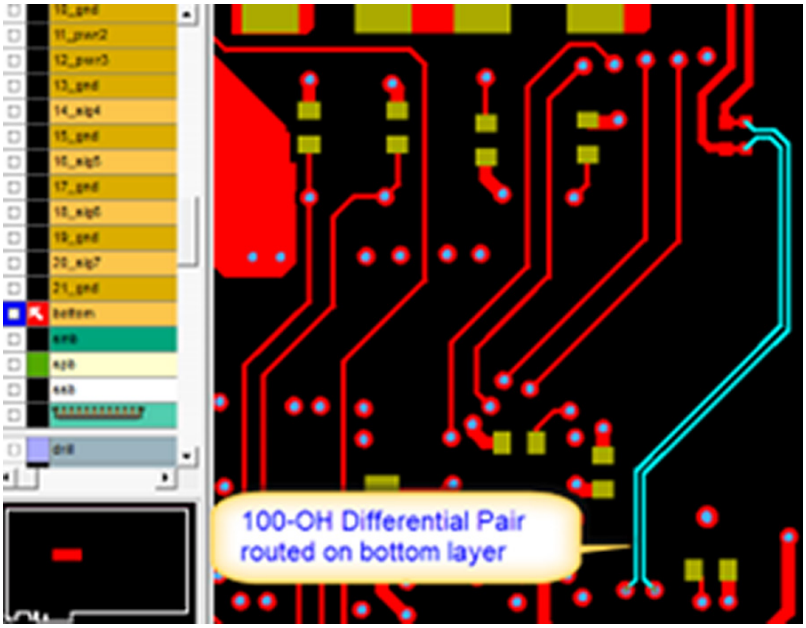

Figure 4. 100Ω differential pair routing for DDR3 clock and strobe signals.

Regarding timing-related constraints, at a high level, data bits exist as bytes/lanes and each lane has its own differential strobe. In each lane, every data bit must maintain a timing relationship with its strobe and match the length of the strobes within a certain tolerance as provided in the datasheet. Additionally, all these data lanes must maintain a specific timing among themselves. All strobes in all lanes must maintain their timing with respect to the clock. The clock requires all address/command/control signals to match its length as well **(Figure 5)**.

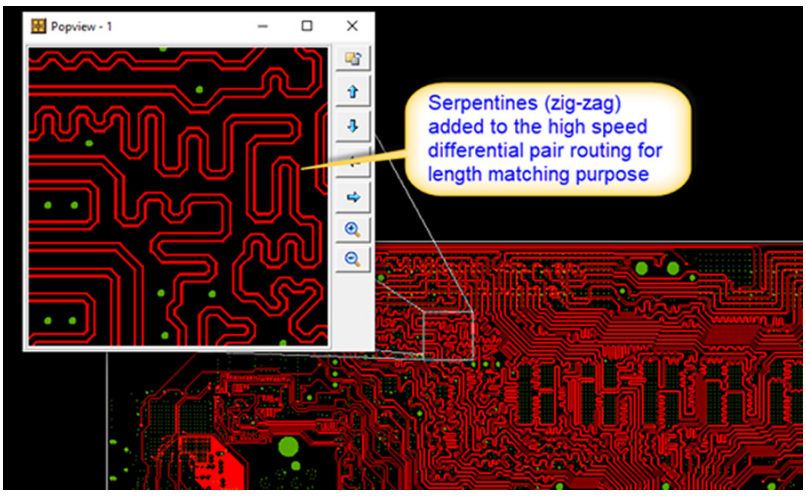

Figure 5. Serpentine routing for length-matching of DDR3 data, strobe and clock signals.

Design engineers mention these delay requirements in terms of time units, such as picoseconds or nanoseconds, while PCB layout designers prefer length-based constraints such as millimeters or mils. Converting time into distance depends on the signal's speed on that particular layer, which relies on the properties of the dielectric material around the signal trace. These material properties also impact the trace impedance. All these factors are a part of PCB stack-up design, linking both speed and impedance closely to this design process. Let's explore how this connection works.

Stack-up design → Signal speeds

When electrical signals travel on the PCB traces, they generate waves of electromagnetic fields around them that travel along with the signals. These electromagnetic (EM) waves travel through the materials surrounding the PCB trace. In free space, EM waves propagate at the speed of light, which is 3×10^8m/s. In a PCB, however, there is no free space; instead, dielectric materials surround the signal traces. The speed of the EM fields in a PCB is affected by the effective relative permittivity (Er) value of the insulating material and is therefore equal to the speed of light in a vacuum, divided by the square root of the effective Er value of the insulating materials surrounding the transmission line; i.e.,

v = c / sqrt(Er)

In PCBs, FR-4 is the common dielectric material used, and its dielectric constant has a range of values from 3.9 to 4.7. To make it simple, take Er = 4 and put it in the above equation, which then reduces to

v = c / sqrt (4) = c / 2 = 1.5 x 10^8m/s = 150mm/ns ~ 6in/ns

In a PCB, the signal trace exists on an external layer (TOP/BOTTOM) or on an internal layer. When the signal trace resides on an internal layer, with a reference plane above and below it, as shown in **Figure 6,** the configuration is called a stripline configuration.

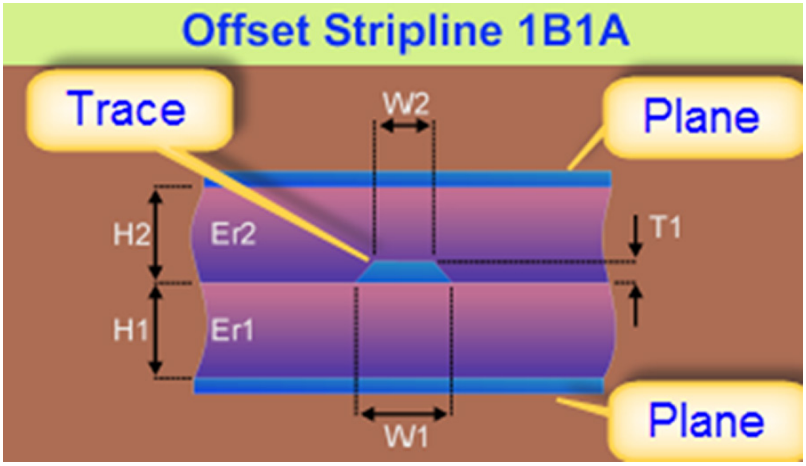

Figure 6. Offset stripline 1B1A configuration with signal trace between two reference planes.

In this configuration, the trace is completely surrounded by the dielectric material. Thus, the effective dielectric constant for this trace is equal to the Er value of the insulating material. For an Er value of 4, the speed of the signal on the internal layer will be approximately 6in/ns. The configuration in which a Cu trace is present on an external layer with a reference plane under it is called microstrip line configuration **(Figure 7)**. In this configuration, the trace has dielectric material below it while air and solder mask typically sit above it. The Er value of the air/solder mask is less than that of FR-4. As a result, the effective Er value for the microstrip line drops below 4, leadings to higher signal speeds on external layers, meaning v > 6 in/ns. Signals always travel faster on external layers. Therefore, a

signal routed on an external layer with a certain length experiences less delay compared to the same length of signal routed on the internal layer. Traces of the same length routed on different layers may have different delay times depending on the effective Er value for each respective layer.

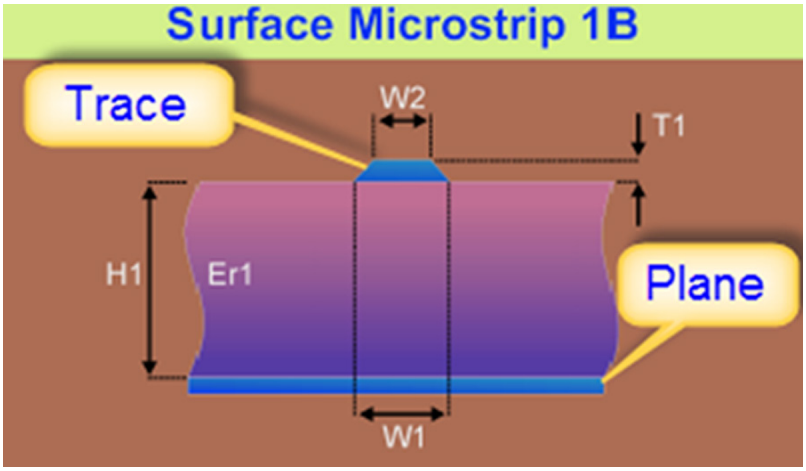

Figure 7. Surface microstrip 1B configuration with a copper trace on the external layer.

From the SI timing point of view, this point is crucial when routing signals in an interface that needs to be length-matched. Route signals belonging to the same group on the same layer to control and easily match the delays. This practice explains why all signals of a DDR3 byte lane are routed on the same layer: it ensures they all maintain the same speed and, consequently, the same delay. Modern day layout tools have this capability built in. If the PCB stack-up is defined properly and all details of material properties and their widths provided, the tool calculates the signal speeds on every layer and can convert the delays into lengths **(Figure 8)**.

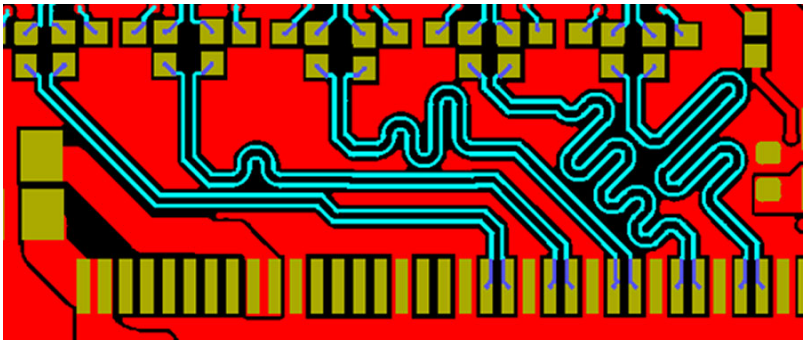

Figure 8. Routing byte lane signals on the same layer.

Stack-up design → Trace impedance, Zo

Now it is time to discuss the relation of characteristic impedance, Zo, with the stack-up design. Closely review the Cu trace in the PCB: it makes a parallel plate capacitor with the reference plane below **(Figures 9** and **10)**.

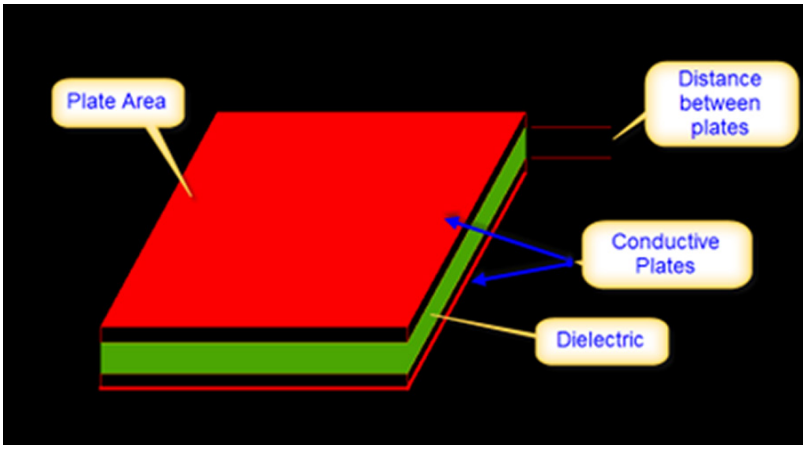

Figure 9. Copper trace and reference plane form a parallel plate capacitor.

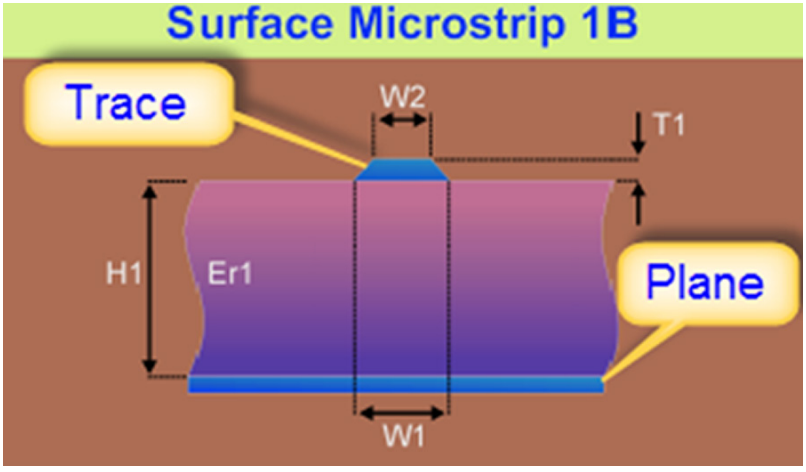

Figure 10. Surface microstrip configuration (1B) affects impedance and signal integrity.

In a parallel plate capacitor, the two plates are separated from one another by air or by a dielectric material in the same way the trace is separated from the plane by an insulating material.

The capacitance of the capacitor is linked to the overlapping area of the plates (A), the distance between the two plates (d) and dielectric constant (Er) of the insulating material between the plates, through this formula

$$\text{Capacitance} = (A \times Er) / d$$

For the capacitance of the PCB trace, the above formula can be written as

$$C = (w \times Er) / h$$

The trace impedance, Zo, and its capacitance are related by the formula

$$Zo = \text{sqrt}\ (L/C)$$

It is evident and can be easily concluded that the trace impedance, Zo, is inversely related to its capacitance, C; i.e.,

$$Zo \Leftarrow \Rightarrow 1/C$$

This means that the factors that will increase the trace capacitance will in turn decrease its impedance, and vice versa. Keeping in view the formula C = (w x Er)/h, it can be concluded that:

- Increasing trace width, w, will increase trace capacitance but will decrease the trace impedance, Zo, and vice versa.
- Using insulating material with higher dielectric constant value (Er) will increase the trace capacitance, but will decrease its Zo and vice versa.
- Increasing dielectric material thickness (h) will decrease the trace capacitance, but will increase its impedance, Zo, and vice versa.

So, in a nutshell:

Trace capacitance (C)	$\Leftarrow \Rightarrow$	Trace impedance (Zo)
$C \rightarrow w$	$\Leftarrow \Rightarrow$	$Zo \rightarrow 1/w$
$C \rightarrow Er$	$\Leftarrow \Rightarrow$	$Zo \rightarrow 1/Er$
$C \rightarrow 1/h$	$\Leftarrow \Rightarrow$	$Zo \rightarrow h$

The trace impedance inversely relates to its width (w) and the dielectric constant value (Er) of the dielectric material, while it directly relates to the thickness of the dielectric material. These factors directly connect to the PCB stack-up. These parameters are tweaked to find suitable trace widths that achieve different target impedance values for all SE and diff-pairs. While making these calculations, ensure that the specified trace widths and spacing values are manufacturable and that selected materials are economical. Additionally, ensure impedance targets are met while keeping the thickness of the dielectric materials so that the overall PCB thickness is within allowable specs.

The stack-up design directly impacts signal speeds and trace impedances through the selected material properties in PCB layer construction. Engineers calculate and control parameters that affect multiple things at once. For example, changing the value of Er impacts both the trace impedance Zo and the signal speed. Sometimes, engineers alter material properties simply to achieve target impedance values, ignoring their impact on signal speeds. The result can be timing issues – product failure.

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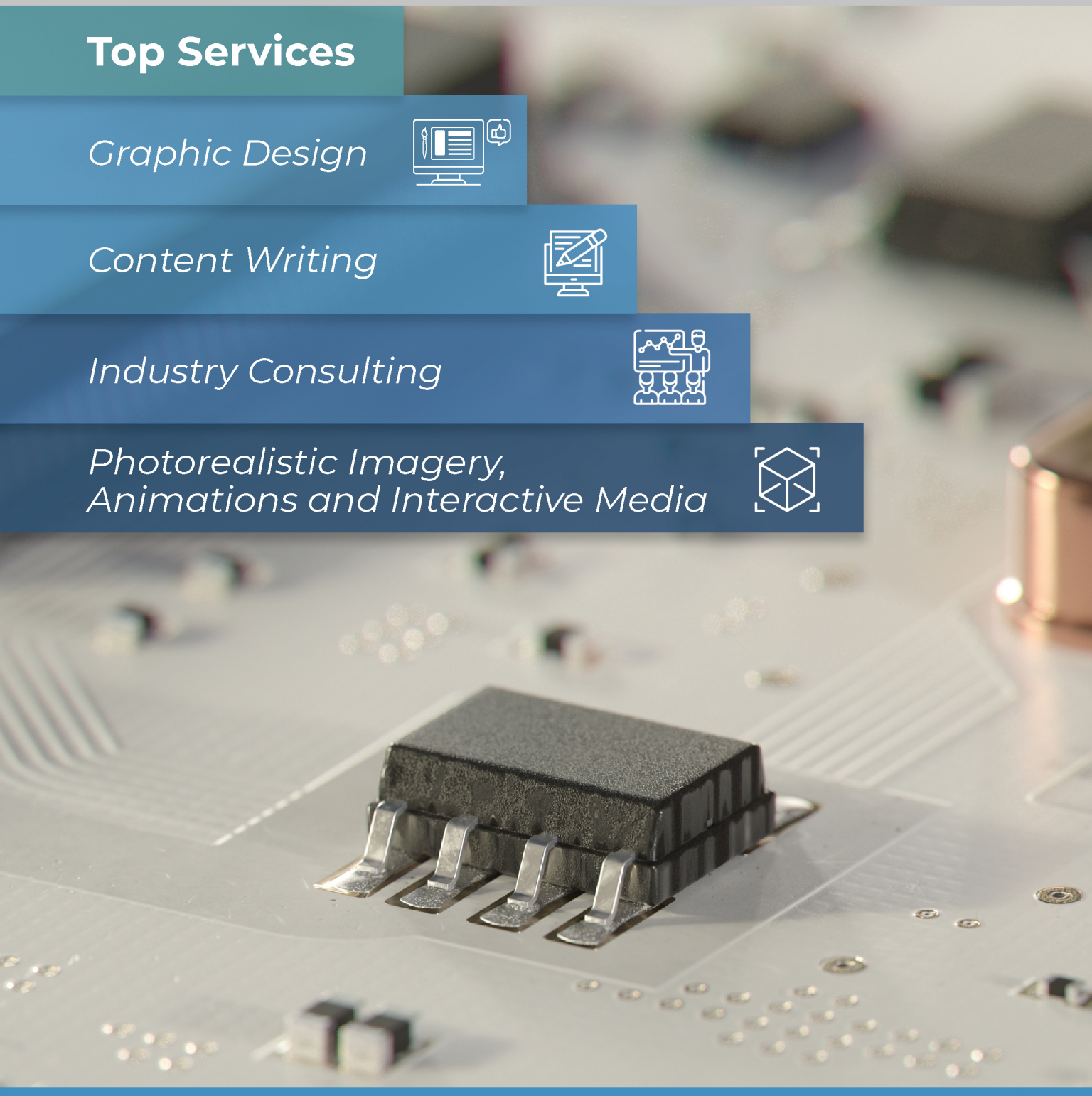

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FUTURE TECH

AI in Electronics Manufacturing: What's Working Now, What's Not (But Should Be)

Artificial intelligence is superb at corralling volumes of data but still lacks the flexibility needed for many engineering tasks.

by RYANN HOWARD

AI is transforming electronics design and manufacturing, making significant strides in everything from procurement to PCB design, and even defect detection. But while there's a lot AI can do today, there's still a whole lot it can't (yet). Here's what's really happening on the ground according to experts in the field.

The easy consensus among those we spoke with is that AI automates the repetitive stuff. At Celus, André Reggiani, AI product manager, highlights that AI is really shining when it comes to "retrieving tons of information from datasheets" and helping engineers "find the right components for their circuits." No more scouring datasheets, crossing fingers that you're not missing something important. It's like having an incredibly efficient assistant, but with fewer coffee breaks.

Celus' André Reggiani says AI shines at retrieving datasheet information.

Zachary Feuerstein of Breadboard promotes AI's cleanup capabilities.

Similarly, Zachary Feuerstein from Breadboard points to AI's prowess in automating data extraction – think BoMs, RFQs, POs and supplier communications. "It can clean up unstructured data, extract part numbers and even handle back-and-forth emails with suppliers," he says. This doesn't just save time; it slashes the annoying admin work that no one signed up for in the first place.

Timon Ruban, cofounder and managing director of Luminovo adds that AI is currently best used for "turning unstructured into structured data." He explains: "Think 'extracting a BoM from a PDF,' 'extracting the PCB specification from a PDF' or 'extracting technical parameters from a datasheet.' AI is taking that chaotic, scattered information and turning it into something engineers can actually use." This is a time-saver for engineers buried under mountains of unstructured data.

AI can add structure to scattered information, Luminovo's Timon Ruban says.

Problem Predictor

Forget waiting for things to break, AI's got a crystal ball. According to Arch Systems cofounder and CEO Andrew Scheuermann, AI's predictive powers are a game-changer. From anticipating when materials will run out to flagging potential downtime-causing machines, AI's shifting the focus from reactive to proactive. This not only keeps things running smoothly, but it also keeps engineers ahead of the game, sparing them from panic mode.

It's all about staying ahead of the curve. "AI's now able to surface real-time, actionable guidance," says Scheuermann. So, no more endlessly scrolling through dashboards. AI serves up the next best action, whether it's pinpointing the nozzle causing scrap or identifying early signs of quality issues based on historical patterns.

AI's Role in PLM – Streamlining Complexity

Duro's Michael Corr believes AI's strength is assessing bespoke datasets.

When I sat down with Michael Corr from Duro, we dove into why AI is such a strong fit for product lifecycle management (PLM). As he put it, "AI is great at handling bespoke datasets and making sense of them," which is a step up from older machine learning tools that required everything to be perfectly formatted. This flexibility is why AI excels in the PLM space, where a mix of CAD content, manufacturing instructions, test data and more all come together. Instead of forcing all that info into a single format, AI can work with it as-is and still deliver meaningful insights.

Corr also highlighted how AI can cut down on redundancy across teams. "It's easy for an engineer to recreate a part because they couldn't find the original," leading to duplicates and inefficiencies. AI can spot these issues by flagging identical or nearly identical parts, suggesting they be merged or removed. This streamlining of data helps strengthen the digital thread, making the entire process more accessible and collaborative. While we're not there yet, Corr is

excited about AI's potential to not just organize data but also analyze changes over time and flag potential future issues before they arise.

Breaking barriers – literally. AI's ability to break down language and cultural barriers is another unexpected perk. Scheuermann points out that AI tools are bridging global divides by translating across languages and dialects, allowing teams in different plants to communicate seamlessly. This means that once a solution is discovered in one factory, it can be applied to another without the hassle of language barriers. Talk about team spirit!

Alek Tyszka from Instrumental agrees, adding that AI can detect defects in real-time using computer vision. This means no more waiting to catch issues during the testing phase – AI spots them as they happen. But what's next? Full integration from CAD to automated assembly and testing. The holy grail? A fully automated digital thread. But that's still a few steps down the line.

The Current AI Struggle: Fully Autonomous Procurement

Now, let's talk about the stuff AI still can't do, no matter how many improvements we see. First up, Breadboard's Feuerstein points to AI's inability to act as a fully autonomous trading agent in electronics procurement. "AI still can't dynamically buy components in real-time," he explains. While it can forecast stock availability and help with price predictions, it's not yet ready to pull the trigger on purchasing decisions without a human steering the ship.

Sergiy Nesterenko from Quilter.ai also offers a sobering view of AI's current limitations in PCB design. While AI is, to a degree, fantastic for automating routing and placement, getting a board ready in hours instead of days, he points out that the real challenge comes in designing something as complex as a motherboard. When it comes to "balancing signal integrity, power integrity, routing density and thermal relief," AI isn't quite at the stage where it can manage those trade-offs like an experienced human engineer. It's like a juggler trying to keep too many balls in the air – something's bound to fall.

Sergiy Nesterenko of Quilter.ai says AI falls short at managing design tradeoffs.

Rui Calsaverini of Celus awaits AI's improved interaction with engineers.

Rui Calsaverini, VP of R&D at Celus, echoes that sentiment: "Probabilistic systems like AI cannot generate an exact design on their own (yet)," he says. "The evolution in AI becomes more about how well it interacts with the engineer and the engineer's intent."

David Wiens of Siemens reinforces this design-focused view, noting that while AI excels in specific areas today, the leap to full design autonomy remains a major hurdle. “We’ve leveraged AI for things like natural language processing using large models, predictive analytics across the supply chain and rapid component selection based on datasheet information,” he explains.

David Wiens says Siemens is focused on improving engineers’ productivity, not replacing them.

These tools already help engineers identify part availability, streamline BoM creation and even predict optimal signal configurations much faster than traditional simulation. However, Wiens is realistic about what AI can’t yet do: generate high-complexity schematics and layouts. “Most of the tools you see today focus on simpler designs,” he notes, due to the lack of high-quality training data and the sheer complexity of real-world boards. “We’re exploring these technologies, but we’re focused on improving engineers’ productivity, not replacing them.”

Celus cofounder André Alcade adds engineers must still intercede.

André Alcade, Celus cofounder, adds: “These tools are producing higher-quality output over time, but even as the quality gets better, you can’t turn them into something for public use without an engineer’s guiding hand.”

From Design to Production – A Bridge Still Missing

At Celus, there’s a similar gripe about AI’s failure to bridge the gap between design and production in real-time. Alcade explains that while AI is excellent at interpreting block diagrams and datasheets, it still struggles to provide actionable insights that cut across both design and production. Imagine AI suggesting a design tweak based on real-world production data. Sounds like a dream, right? But we’re not there yet.

Scheuermann from Arch Systems agrees, emphasizing that unlocking real-time end-to-end intelligence is the big frontier for AI in electronics. “Once AI can bridge that gap, like surfacing how a layout decision impacts yield, we’ll see a massive leap forward,” he says. Right now, design and production still live in their own silos. AI can’t yet connect the dots in a way that can predict or fix issues on the fly.

Zuken's Kyle Miller has laid out a compelling case for how AI is reshaping PCB design in ways that traditional rule-based automation never could. "It doesn't do it like I would do it," he wrote, citing a common frustration among engineers who feel that rigid automation systems don't mirror their judgment or design style. His point is that past automation tools failed because they were brittle – too inflexible, too difficult to set up and too unaware of when breaking the rules was actually the best decision. AI, by contrast, "offers a fundamentally different approach, providing adaptive intelligence rather than rigid rule-following."

Zuken's Kyle Miller asserts AI can reshape PCB design.

Miller explains that modern AI systems can balance competing design priorities, customize to individual preferences and reuse design intelligence from past projects. He outlines key areas where AI is already helping – from intelligent constraint management during setup to adapting layouts based on previous successful designs. "By allowing the designer to interact with the PCB at a much higher level," Miller argues, "it speeds up time to market but still keeps overall control with the designer." Zuken's own tools, he notes, already leverage AI for routing and decap placement, with more adaptive features planned for future releases.

The Road Ahead

While AI is undoubtedly making waves in electronics manufacturing, it's clear that it's not ready to take the reins. From making predictions before things go wrong to automating tedious tasks, it offers some serious time savings.

But there's still a long road ahead, whether it's perfecting procurement, mastering design trade-offs or integrating the entire design-to-production process, AI's journey is only just beginning. As Nesterenko of Quilter.ai puts it, "AI's real challenge is learning to make the same kind of tradeoffs as an experienced engineer."

Stay tuned for more updates on how AI continues to shape the world of electronics. Who knows what it'll do next?

RYANN HOWARD is managing editor of PCD&F/Circuits Assembly; ryann@pcea.net. Prior to joining PCEA, she helped train the AI for a major US-based company.

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PROCESS CONTROL

Factors Contributing to Solder Ball Formation: A Guide

Improper paste viscosity and incorrect reflow ramp profiles are just a few of the root causes.

by MD. IMTIAZ UDDIN

Solder balls are small, spherical metallic balls that can form on circuit boards, typically around the leads or pads of surface mount components. Ranging from just a few micrometers to a couple of hundred micrometers in diameter, these balls form from issues in the soldering process.

If solder balls appear, they can affect the overall functionality of the circuit board. Small solder balls are unsightly and can move components slightly off mark. In the worst cases, bigger solder balls can fall off the surface and deplete the quality of the component joints. Worse, balls can roll onto other board parts, leading to shorts and burns.

Typically, solder balls are located on the side of chip components **(Figure 1)**. Solder balls, which are typically between 0.2mm and 0.4mm in diameter, can occasionally be observed surrounding the pins of ICs and connectors.

- 0.5mm solder balls or larger are typically unacceptable due to the risk of bridging and shorts.
- Even when smaller than 0.2mm, solder balls may not cause immediate issues. They may indicate problems with solder application and can lead to reliability concerns.
- Regardless of size, solder balls are typically not permitted close to high-density areas or important components.

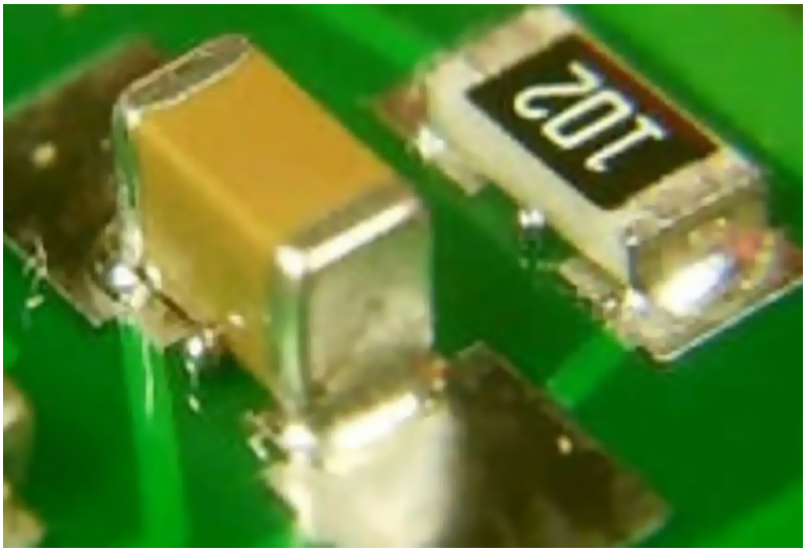

Figure 1. Solder balls formed on the periphery of a passive component.

Always check the specific requirements provided by manufacturers or clients, as they may have stricter criteria based on their applications.

Factors and Solutions

Several factors contribute to solder ball formation.

Moisture. Excess moisture in solder pastes or the bare PCB can lead to the formation of solder balls during reflow. Moisture contributes to this issue in multiple ways:

- Solder paste is hygroscopic, meaning it can absorb moisture from the environment. Improperly stored paste can take on moisture, leading to problems during soldering.
- During reflow, heat causes absorbed moisture to vaporize rapidly, creating steam. This steam can create bubbles in the solder paste. The rapid expansion of steam can disrupt the solder paste, causing the solder to bead up and form solder balls instead of flowing smoothly to create solid joints.

An improper metal-to-flux ratio or poor solder paste quality can lead to solder being expelled and forming solder balls during the soldering process. If the flux content is too low relative to the solder metal, it may not effectively reduce surface tension and facilitate proper flow, leading to solder balls instead of smooth joints. Conversely, too much flux can create an unstable mixture that causes solder to clump and form balls during reflow. Poor quality paste may have inconsistent viscosity, which can result in uneven application and excess solder in certain areas, increasing the likelihood of solder balls.

Extreme temperature variations can alter the viscosity of solder paste, affecting its application and performance. Higher temperatures can make the paste too runny, while lower temperatures can make it too thick. Temperature changes can cause the metal and flux components in solder paste to separate, resulting in an inconsistent mixture that may not perform well during soldering.

Viscosity. Low viscosity solder paste can lead to slumping and the formation of solder balls during the soldering process.

Low viscosity solder paste lacks the necessary thickness to maintain its shape during the reflow process. This can cause excessive flow, leading to solder slumping away from pads and forming unintended shapes. When solder paste slumps, it may lose the defined areas needed for proper solder joints, increasing the likelihood of solder balls forming instead of smooth, cohesive connections. Low viscosity also can disrupt the balance of surface tension, causing solder to bead up instead of spreading evenly across the pads.

Oxidized solder paste. Expired or oxidized solder paste can create solder balls and contribute to leaching effects during the soldering process.

Inconsistent flux activity. Expired solder paste may have degraded flux, resulting in poor wetting and inadequate solder flow. This causes solders to clump and form solder balls instead of creating smooth joints.

Low viscosity. Oxidized solder paste can lose its intended viscosity, leading to excessive solder application and the formation of balls during reflow.

Inadequate adhesion. Degraded paste may not adhere properly to the PCB or component pads, permitting solder to pool and create balls.

Among the mitigation strategies are the following:

- **Choose appropriate paste.** Select solder paste with the correct composition per product and design requirement for the specific application and printing process.
- **Proper mixing.** Ensure the solder paste is well-mixed before use to achieve the desired viscosity and consistency.
- **Temperature control.** Maintain proper temperature and humidity conditions during storage and application to prevent changes in viscosity and oxidation.

Reflow Process

Insufficient preheat temperature can significantly affect the soldering process by causing the flux to evaporate too quickly, which can lead to solder expulsion and the formation of solder balls. With insufficient flux activity, solder may not adhere properly to the pads or components. This leads to solder being expelled from the joint during the reflow, causing it to form balls.

A reflow profile with a high ramp-up rate or a too-rapid temperature increase can lead to solder splattering and formation of solder balls. If the temperature increases too quickly, the flux may not have enough time to activate properly, which is essential for good wetting and adhesion. This results in poor solder flow and ball formation.

Vibrations during the reflow process can dislodge solder paste from its intended position, causing components to move and leading to solder balls forming either on the PCB surface or between solder joints.

Stencil and Printing

Improper stencil aperture design, especially excessive volume or poor gasket seal, can lead to solder ball formation during the reflow process, as the solder paste can creep under the stencil and form beads. If the aperture area is too large for the pad size or if the stencil is not properly gasketed, excess solder paste may be deposited, resulting in the formation of solder balls under the component or on pads.

Guidelines for avoiding solder balls due to printer errors include the following:

- **Follow the datasheet.** Develop a stencil per component data sheet guidelines.
- **Reduce aperture volume.** Design apertures slightly smaller than the pads to ensure a good gasket seal and prevent excess paste deposition.
- **Optimize aperture shape.** Consider using "home plate" or "radiused inverted home plate" (RIHP) apertures to reduce the possibility of "mid-chip" solder balls.
- **Ensure proper stencil-to-PCB contact.** Ensure a tight seal between the stencil and PCB to prevent paste from creeping under the stencil.
- **Use appropriate squeegee pressure.** Proper squeegee pressure is crucial to ensure complete paste transfer and prevent paste from being trapped in the apertures.
- **Choose the right stencil foil thickness.** Thicker foils can be used for larger components or those prone to warpage or coplanarity problems, while thinner foils are better for smaller components with finer pitch I/Os (input/outputs).

Stencil cleaning. Improper stencil cleaning can lead to solder paste residue accumulating, which negatively impacts solder paste application, potentially causing solder balls and other defects during reflow. Regular cleaning of the stencil, or cleaning after a certain number of prints, is essential for ensuring consistent solder paste application and preventing solder ball formation. Adhere to the guidelines in IPC-7526 for cleaning stencils and misprinted boards.

Stencil alignment with PCB. When the stencil and PCB are not properly aligned, the solder paste is printed in the wrong location, potentially depositing paste on areas other than the intended pads. It is important to ensure proper stencil alignment during initial setup only.

Wiped PCB. A misprinted and wiped board can contribute to solder ball formation during reflow. Wiping a misprinted board with alcohol or other solvents can leave residual moisture or solvents that interact with the solder paste during reflow, causing it to splatter and form solder balls. Additionally, the act of wiping can push solder paste into vias or other areas, exacerbating the problem. Instead of wiping, use an automatic cleaning process, like an air spray or ultrasonic cleaner, to remove misprinted solder paste. These methods are more effective at removing paste

without pushing it into unintended areas.

PCB and Component Issues

Trapped moisture in a PCB or component can lead to solder balls during the reflow process. When heated, this moisture outgasses and creates steam, which can displace solder and result in the formation of solder balls. It is advisable to store PCBs and components in a dry environment. Bake PCBs before assembly to remove any trapped moisture.

Poorly executed hot air solder leveling (HASL) with nonuniform PCB pad flatness can contribute to solder ball formation, Uneven or warped pads can lead to inconsistent solder deposition. Higher areas may not receive adequate solder, while lower areas may accumulate excess solder.

Control the HASL process to achieve consistent solder coverage, ensuring pads are properly leveled.

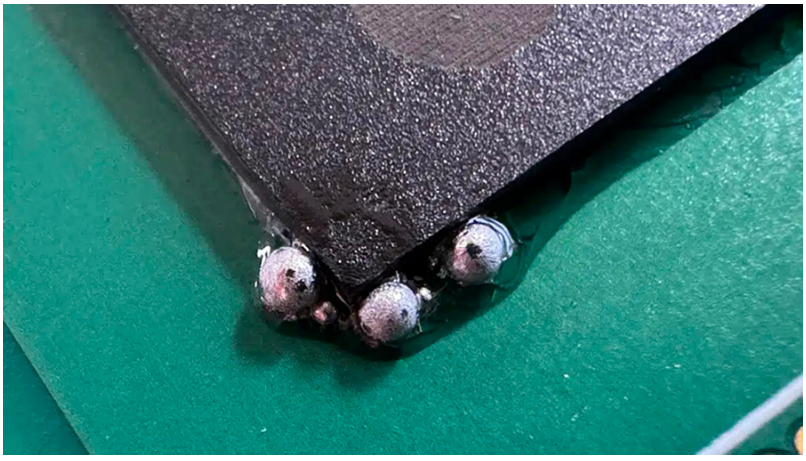

Figure 2. Multiple solder balls formed on the edge of an array package.

High pressure during placement. An often-overlooked factor contributing to solder balls is excessive mounting stress. Applying too much pressure when placing components can compress solder paste beyond its intended limits, resulting in paste being pushed off the pads. This can lead to solder being displaced and forming balls. If the mounting stress is excessive, the solder paste may be forced out of the pad, which can transform into solder balls after the reflow soldering process. To avoid this problem, minimize mounting stress so that components can be accurately positioned on the printed solder paste and pressed down appropriately.

Conclusion

Solder ball formation is a critical issue that can significantly impact the functionality and reliability of circuit boards. Factors contributing to the formation of solder balls include issues with solder paste, reflow process, stencil and printing as well as PCB and component issues. Moisture, paste composition, storage conditions and oxidized solder paste are key contributors to solder ball formation during the soldering process.

Mitigation strategies such as choosing appropriate solder paste, ensuring proper mixing, temperature control and preheat temperature during the reflow process are essential in preventing solder ball formation. Proper stencil design, cleaning, alignment and PCB moisture management are crucial in avoiding solder ball formation during the printing and assembly process.

By understanding and addressing these contributing factors, manufacturers and designers can effectively mitigate the risk of solder ball formation and ensure the quality and reliability of circuit board assemblies.

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COLLABORATIVE **ROBOTS**

Mechatronics Assembly Techniques You Should Be Using in 2025

Ten techniques to ensure a smooth end-to-end process.

by NEIL SHARP

From medical devices to monitoring systems, products are becoming smaller, smarter and more complex to manufacture, making mechatronics assembly the bedrock of innovation for forward-thinking OEMs. Modern mechatronics manufacturing no longer focuses solely on mechanical integration; it now fuses electronics, sensors, software and control systems in ways that demand tighter tolerances, smarter testing and leaner processes. Although core techniques remain relevant, recent developments in mechatronics assembly – such as the integration of Industry 4.0 technologies, automation and AI – means more modern techniques are emerging.

To meet the high level of skill, precision, accuracy and consistency that today's mechatronic assemblies demand, here are 10 advanced mechatronic assembly techniques that ensure a smooth end-to-end process.

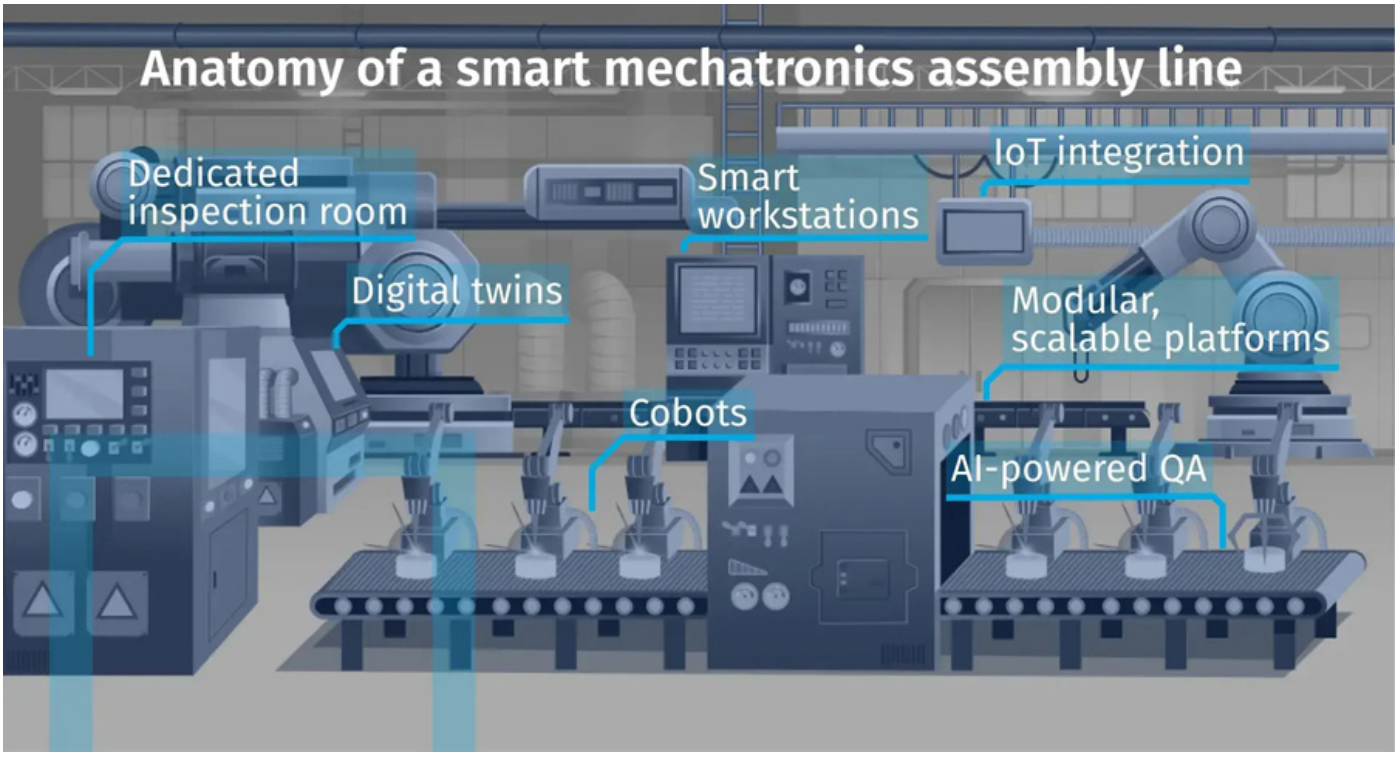

Figure 1. Anatomy of a smart mechatronics line.

1. Organize purchasing teams into clear commodity groups. Because mechatronic assemblies tend to feature

bespoke metalwork, you must build a broad and robust supply chain that delivers high-quality parts as needed. A well-structured procurement team is the first line of defense against supply chain disruptions, component shortages, quality issues and pricing volatility. By organizing experts into commodity groups – mechanical, electronic, plastic, PCB, etc. – each buyer can focus their skills and efforts on one specific area. For example, one person may purchase sheet metal while another is responsible for all the machined parts. This approach encourages excellence, as each specialist can develop deep supplier relationships and sourcing strategies for each category. This leads to better negotiation power, supply-chain resilience and effective design feedback loops.

2. Set up an inspection room. A dedicated inspection room ensures that each part of a mechatronic assembly – especially safety-critical components – looks and functions as specified, with consistent visual, dimensional and functional checks at every stage of the process.

Often, builders won't find issues until the physical build takes place as, individually, the parts produced will pass initial quality checks. But problems such as wrong dimensions, missing cut-outs in metalwork, incorrect paint or anodizing finishes, scratches to front panels, etc. can and should be picked up beforehand.

The inspection room should include calibrated equipment like height and surface measuring instruments, digital calipers, mechanical micrometers and high-magnification microscopes. Any issues found either at material level or during build should be fed back to the purchasing and engineering teams to implement corrective actions.

3. Invest in 3-D CAD modeling packages. It is well worth investing in a 3-D computer-aided design (CAD) modelling package to support collaboration among design, manufacturing and quality teams. This software reduces the time it takes to design a product and improves quality and delivery during the build process. Many software packages available today simulate real-world scenarios, which bring a design to life. This process helps to identify potential tolerance issues during the mechatronics build, enabling prevention before work starts.

4. Implement a robust test strategy. Testing ought to be at the heart of everything an OEM does. After all, if the product doesn't work properly, the entire manufacturing process is rendered useless. A good test plan reduces field failures, accelerates compliance approvals and feeds back into design improvements. Testing is especially important in mechatronics manufacturing because the addition of moving parts requires them to operate at high and low tolerances while interacting with stationary parts, adding complexity. Therefore, a robust test strategy ensures the product is functionally tested to meet the end-user's requirements.

5. Adopt digital twin technology. Digital twin technology creates a virtual replica of the product and the production process, permitting simulation, monitoring and optimization of mechatronic assemblies before they hit the physical production line. In mechatronic assembly, this means virtually assembling components to test tolerances, thermal performance and interdependencies between mechanical and electronic systems before committing physical resources. This helps proactively identify and mitigate issues during the design or prototyping stages, avoiding costly revisions in later production phases.

6. Set up smart workstations with IoT integration. Smart workstations combine digital guidance, torque-controlled tooling, barcode scanning and connected sensors to create a closed-loop manufacturing environment. Each

assembly step is validated in real time, and deviations are flagged instantly, improving traceability and reducing operator error.

IoT integration, a hallmark of Industry 4.0 technology, takes it a step further by connecting machines, materials and personnel into a real-time data network. For example, when a part is assembled outside of its specification at any point, it's instantly logged and reported, supporting real-time corrective action and data-driven process refinement.

7. Use modular, scalable assembly platforms. A modular platform strategy transforms rigid manufacturing setups into reconfigurable, future-ready assembly environments. Workstations are designed to be retooled or repurposed quickly, making it easier to switch between products or scale production based on demand without sacrificing throughput. This is ideal for OEMs that need to pilot new products, support multiple variants or respond to fluctuating order volumes. With this approach, a new product can ramp up in weeks, not months, while maintaining the highest quality and traceability standards.

8. Deploy advanced cobots with vision systems. Modern robotic systems, particularly collaborative robots (cobots), execute high-precision tasks in environments that demand both flexibility and repeatability. For example, they can selectively solder, pick and place components, automatically fasten screws and even dynamically inspect products. Paired with machine vision systems, cobots check, measure and manipulate components with micrometer-level accuracy. This is especially useful in mechatronic assemblies where tolerances are tight and product configurations vary frequently.

9. Use AI-powered quality assurance tools. AI-driven visual inspection tools can now outperform the human eye in inspection speed, consistency and defect detection. Machine learning models trained on thousands of images can instantly spot anomalies like microcracks, missing components or solder bridges and even under varying lighting or orientation.

Integrating AI across several inspection points can help close the loop among design, process and quality faster, thus improving first-pass yield rates and accelerating root-cause analysis and regulatory documentation.

10. Adopt a closed-loop feedback system. A closed-loop feedback system, powered by Six Sigma and lean manufacturing principles, captures data from manufacturing and test stations, links it back to design and process teams and triggers updates in real-time. This creates a living manufacturing environment where issues are resolved before they escalate, and lessons learned are instantly embedded into future iterations.

For example, if the system identifies recurring failures in a specific connector, engineering can evaluate the root cause and adjust design tolerances or sourcing decisions accordingly. This shortens development cycles, reduces product revisions and makes for a more agile supply chain.

Conclusion

Whether developing a next-gen surgical device or a smart industrial controller, mechatronics assembly is a complicated process; the combination of moving parts and bespoke metalwork means that there is a lot to take into

account. It's vital to adopt modern techniques to ensure a successful mechatronics assembly process, from concept to full-scale production.

Ed.: This article was first published in the Escatec *EMS Review* and is republished with the author's permission.

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PCD&F

AMPHENOL RF EXTENDS SMA CONNECTORS LINE

Amphenol RF SMA connectors are now compatible with 0.81mm and 1.32mm cable, engineered for secure, routable RF performance in harsh environments.

Features threaded coupling mechanism and support for up to 9GHz. Meets demands of Wi-Fi 7 and other high-frequency applications. Tested for 500 mating cycles and built with gold-plated brass and stainless-steel components. Suited for antennas, telecom and aerospace systems. Preconfigured and custom cable assemblies available.

Amphenol RF

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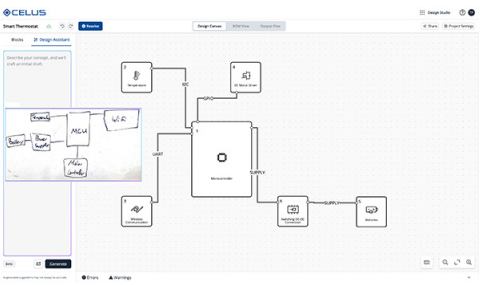
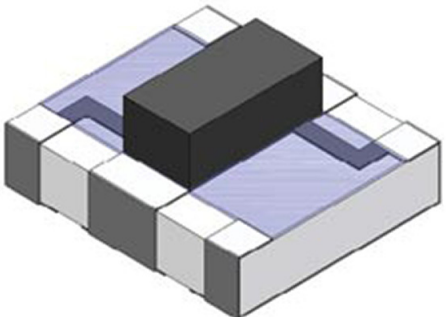


CELUS UPGRADES CELUS DESIGN PLATFORM

Celus Design Platform now includes Design Assistant, an AI-driven feature that creates full projects from a simple image or text command. Simplifies design workflows and reduces component selection errors. Identifies compatible

components based on preferred vendor and creates complete schematic of the design. Offers access to thousands of cataloged parts.

Celus
celus.io



IMS 20GHZ ATTENUATORS

IMS AV-0607-C temperature variable attenuators for RF power amplifiers, broadcast equipment and multiband communication systems feature low-noise, thin-film construction. Reduce attenuation with increasing temperature, helping offset PA or LNA gain loss at higher frequencies. Offer TCA from 10MHz to 20GHz, for simulating impacts on signal attenuation and gain. Attenuation ranges from 2-9dB and power ratings of 160-200mW, the 50Ω SMT TVAs fit compact 0607 packages. Operates between -55° to +125°C, and maintain ±1.0dB attenuation accuracy from DC to 15GHz and ±1.8dB or better to 20GHz. For use in aerospace and defense applications, including radars and satcom systems.

IMS
ims-resistors.com

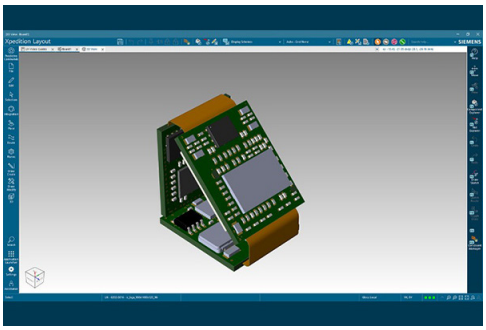
JIVA MATERIALS RPCB PCB LAMINATE

Jiva Materials RPCB printed circuit laminate has a 67% smaller carbon footprint compared to FR-4. Is said to be fully compatible with low-temperature soldering and standard PCB assembly. Comes in standard thickness, single and

double-sided configurations, and various copper weights. Fabrication turnaround is 10 to 15 working days, depending on board complexity.

Jiva Materials

jivamaterials.com

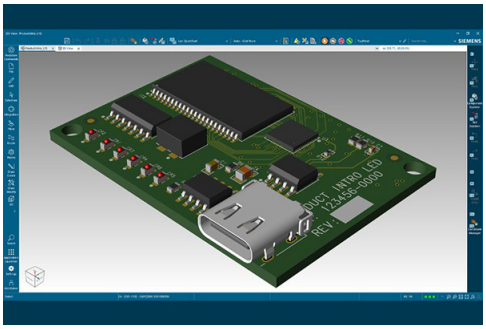


SIEMENS XPEDITION STANDARD PCB DESIGN TOOL

Siemens Xpedition Standard AI-enhanced PCB design platform combines cloud collaboration, AI automation and professional-grade toolsets tailored for small and mid-sized electronics teams. Adds design reuse, variant management, advanced routing automation, native 3-D layout and deeper collaboration across mechanical, manufacturing and supply-chain stakeholders. Token-based options provide on-demand access to more advanced capabilities such as fully integrated pre- and post-layout signal integrity analysis powered by Hyperlynx software for PCB analysis and rigid-flex design without requiring a full tier upgrade.

Siemens Digital Industries

siemens.com



SIEMENS LAUNCHES PADS PRO ESSENTIALS PCB CAD

Siemens Pads Pro Essentials incorporates features of its higher-end Xpedition technology in a streamlined, cloud-connected design environment.

Introduces integrated, co-branded front-end powered by Celus, for designs using intelligent functional blocks with AI-

assisted schematic and BoM generation. Tailored for independent engineers and startups, it includes schematic capture and place and route capabilities.

Siemens Digital Industries

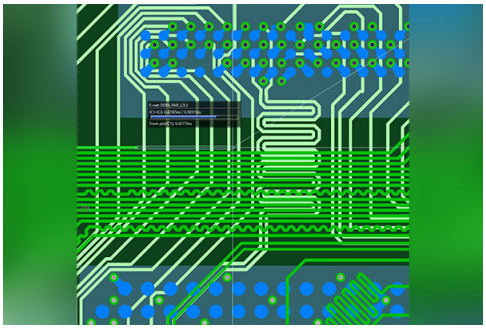
siemens.com

TTM TECHNOLOGIES RF COMPONENTS

TTM Technologies high-performance RF components, including XMB0465Z1-50100G and XMB0220K1-50100G, are for telecom, test and mil-aero applications. Includes ultra-small broadband transformers for RF SoCs and converters, low-profile hybrid couplers for VHF and C-Band and RF terminations for 5G, LTE, ISM and mil-aero bands.

TTM Technologies

ttm.com



ZUKEN CR-8000 2025 PCB DESIGN SOFTWARE

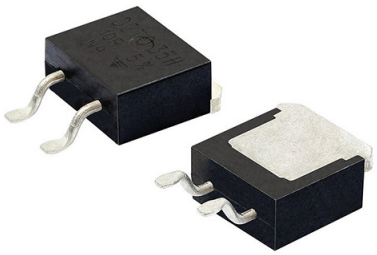
Zuken CR-8000 2025 printed circuit board design software features updates to Design Gateway and Design Force, including intelligent schematic auto-generation, delay-aware routing and reliability validation tools.

Enhances early-stage design with auto-generated connectors and standardized circuits like ESD protection and filters. Uses rule-based logic and simulation feedback. Updates to Circuit Adviser enable analysis of component lifespan, thermal limits and voltage margins.

Includes AI-assisted bus routing and decoupling capacitor placement, as well as timing-aware features for interfaces like DDR4 and PCIe.

Zuken

zuken.com



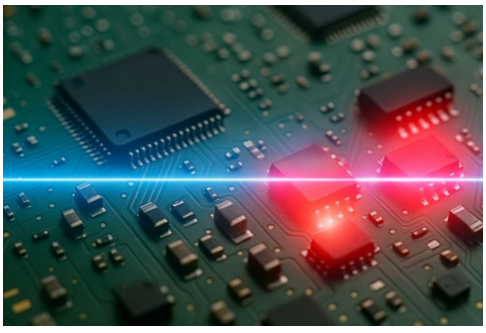
VISHAY D2TO35 SERIES SMT RESISTORS

Vishay D2TO35 series surface-mount thick-film power resistors are AEC-Q200 qualified and deliver pulse absorption up to 15J/0.1s and offer power dissipation of 35W at a +25°C case temperature. Come in TO-263 (D²PAK) automotive grade package. Unique design provides 30% higher energy absorption than standard D2TO35 resistor for enhanced protection against short transient pulses. Temperature operation to +175°C, and resistance values from 1Ω to 14kΩ, with tolerances down to ± 2%; and thermal resistance of 4.28°C/W. Serves as active discharge, discharge or precharge resistor for controls, 48V board nets, BMS, fuel cells, and onboard chargers for HEVs, EVs and low-speed electric vehicles; energy monitoring and metering systems; agricultural vehicles and farm equipment; industrial motor drives, welding equipment, and power tools; and military weapons guidance systems. RoHS-compliant resistor and comes in noninductive design. Solder reflow secure at 270°C/10s.

Vishay Intertechnology

vishay.com

CA



CYBORD SHIELDSCAN VISUAL-AI PCBA INSPECTION TOOL

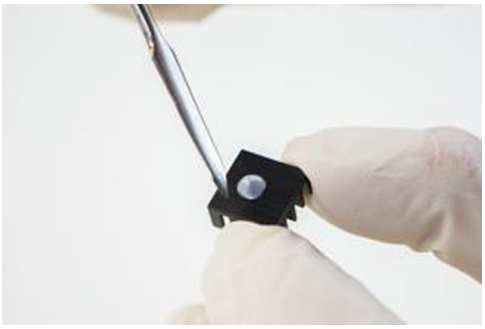
Cybord ShieldScan visual-AI printed circuit board assembly (PCBA) inspection software automates full PCBA mapping, detects anomalies in real time, and is said to ensure 100% board integrity, protecting manufacturers from supply chain tampering and security threats.

Is said to detect malicious hardware implants to prevent rogue chips from compromising security; detect missing components; detect unauthorized replacements; verify component origins to meet strict regulations, including US

country-of-origin bans; and perform 100% visual verification of every component. Does not rely on BoM lists or CAD files. AI-driven optical character recognition (OCR) and natural language processing (NLP) ensure accuracy in analyzing manufacturer markings, lot codes, datecodes and compliance data.

Cybord

cybord.ai



MASTER BOND EP3HTSDA-2MED EPOXY

Master Bond EP3HTSDA-2Med one-part silver filled epoxy is for high-speed medical device manufacturing. Offers high electrical conductivity and thermal performance. Meets ISO 10993-5 cytotoxicity standards.

Material cures at elevated temperatures and supports automated dispensing with a long working life at room temperature. Fine filler particles enable thin bond lines and low thermal resistance. Resists common sterilization methods like EtO and gamma radiation. Comes in syringe and jar formats.

Master Bond

masterbond.com

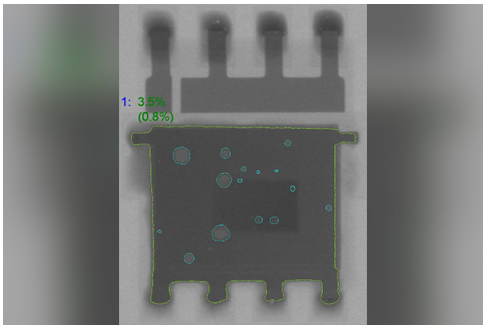
SEICA VALID LR MULTIFUNCTIONAL TESTER

Seica Valid LR performs supports a range of tests including in-circuit, functional, dynamic digital and boundary-scan. Configurable with a range of additional resources such as LED test. Is said to preserve original fault coverage and test program compatibility. Supports legacy replacement on three levels: mechanical, electrical and software.

Cableless architecture supports up to 5888 channels with a 1:8 digital multiplexer. Offers up to 24 programmable power supplies for flexible management of power-on tests. UI uses PLC system with OPC-UA communication for integration into modern test environments. Includes up to 64 general-purpose I/O channels per unit under test (UUT) and features four independent vacuum paths and two compressed air paths for efficient fixture operation. Has 16 OBP channels, compatible with Seica and third-party technologies. Front panel connectivity options include USB 3.0 ports, Ethernet, digital sync interfaces for debugging, and compressed air connections.

Seica SpA

seica.com



SHENMAO PF606-PW220 SOLDER PASTE

Shenmao PF606-PW220 lead-free water-soluble solder paste is for high-reliability PCB assembly applications. Ensures compliance with RoHS, RoHS 2.0 and REACH regulations. Delivers print consistency with ease of cleaning, with residue removed using 60°C hot water.

Is for surface mount and ground pad soldering in industries such as telecommunications, automotive electronics, industrial controls and medical devices. Produces solder joints with low ionic residue.

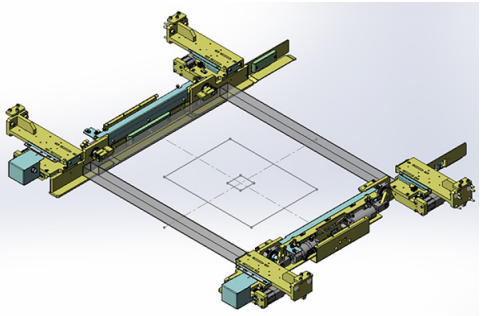
Shenmao

shenmao.com

VIE TECHNOLOGIES VISIONXPERT XC-100 SERIES

ViE Technologies VisionXpert XC-100 Series Smart Camera is compact and delivers real-time detection and high-speed image processing. Features 180° rotatable connector, wide-angle lens and AI-powered deep learning tools that simplify deployment. Includes OCR, code recognition, measurement, counting and detection functions. Offers flexible integration with platforms like V-ONE Mars and Automated Mobile Robots. Supports smart manufacturing and Industry 4.0 transformations.

ViE Technologies



YAMAHA YRP10E SCREEN PRINTER

Yamaha YRP10e entry-level screen printer has a three-stage conveyor for efficient loading and removal of boards from the print process. Core cycle time is 6 sec. Chassis is designed to prevent vibrations or deflections due to movement of the printing mechanisms. Features include stopperless board transport – eliminating settling time and positional errors that can occur with conventional mechanical stoppers, and position adjustment for flexibility to accommodate complex PCB outlines and different sizes. Overprinting feature prepares stencil apertures properly by cleaning to enhance aperture filling in the next few print cycles. Optional universal stencil holder allows one-touch automated adjustment for any standard-sized stencil.

In Case You Missed It

Antenna Design

"Flexible Metasurface Loaded Felt Substrate Built Wearable Antenna with Tri-band and High Gain Features for WBAN Applications"

Authors: Dheeray Nagar, Prashant Ranjan and Atanu Chowdhury

Abstract: A low-profile tri-band wearable antenna is presented. The unique features of the proposed antenna design are as follows: 1) With the assistance of dual U-formed printed lines, the proposed wearable antenna works in three different frequency bands; i.e., 2.4GHz, 3.5 GHz and 5.5 GHz; and 2) the single metasurface placed on the backside of the antenna reduces specific absorption rate (SAR) by more than 90% and improves antenna gain (4.55dBi) in all three operating bands. The designed aerial and metasurface have total size of $46.12 \times 51.8 \times 1.3mm^3$ and $90 \times 90 \times 1.3mm^3$, respectively. Experimental results confirm that the designed aerial operates at 2.4-2.59GHz, 3.15-3.76GHz and 5.1-5.9GHz. Furthermore, the radius of curvature was shown to have no effect on the functioning of the developed antenna, which makes it ideal for on-body measurements. Additional studies on low-cost felt substrate-based antennas for wireless body area network (WBAN) applications may be motivated by this concept. *(Journal of Electronic Materials,* April 12, 2025, https://doi.org/10.1007/s11664-025-11910-x)

Conductive Materials

"A Novel Modeling and Analysis of Mechanical Properties of Single-Component Thermal Conductive Silica Gel"

Authors: Yuezhen Wang, *et al.*

Abstract: Single-component thermal conductive silica gel (S-TCSG) is a new type of thermal conductive material for packaging electronic components in high-performance printed circuit boards. Its mechanical properties can lead to excessive deformation of PCBs or even solder joint fracture during screw fastening or falling. The paper details an experimental program developed to study mechanical properties of S-TCSG, such as cushioning property, creep and stress relaxation. The relationship model is established between cushioning coefficient, compression stress and compression strain based on the compression stress-strain test. In addition, the time-varying laws of the compression creep and stress relaxation of S-TCSG were studied experimentally. The elastic modulus, relaxation modulus and creep compliance can be obtained based on the experimental data. A nonlinear finite element model (FEM) of S-

TCSG is established. Further, the influence of gel thickness on stress distribution is analyzed in screw tightening. A mathematical model is proposed to characterize the relationship between gel thickness, compressive stress and displacement load. This study is of great practical significance to the rationality of coating thickness of S-TCSG and the performance improvement of PCBs. *(Scientific Reports,* April 30, 2025, https://doi.org/10.1038/s41598-025-99953-2)

Plating

"Electroplating Behavior of a Phosphorous-Based Cyanide-Free Silver Electrolyte in an Acidic Environment"

Authors: Soojin Lee, *et al.*

Abstract: This study entailed the development of a novel acidic silver-plating solution using phosphorus-based compounds. A systematic investigation was conducted to optimize the effects of the complexing agents tris(hydroxypropyl)phosphine (THPP), pyrophosphoric acid (PPA) and phosphoric acid (PA) electrolytes on silver reduction and solution stability. Linear sweep voltammetry demonstrated the stabilizing effect of THPP on Ag ions, revealing cathodic polarization of the Ag reduction potential at $[Ag^+]$:[THPP] ratios ranging from 1:1 to 1:5. Notably, the 1:4 ratio exhibited the lowest reduction potential, indicating that the $[Ag(THPP)_4]^+$ complex formed under these conditions was the most stable, a conclusion supported by density functional theory (DFT) calculations. Further, the optimal concentration of the plating solution was determined by analyzing current density variations concerning the concentrations of PPA and PA. The Scharifker–Hills model, energy level analysis using DfT, and cyclic voltammetry elucidated the impact of electrolyte–proton interactions in influencing hydrogen evolution, thereby revealing distinct nucleation mechanisms for Ag reduction in each electrolyte. This study establishes a THPP-based acidic plating solution capable of achieving stable Ag deposition under acidic conditions by optimizing the conditions for complexing agents and electrolytes. These findings suggest the possibility of substituting cyanide-based plating solutions in applications requiring silver plating in acidic environments, potentially enhancing precise plating processes such as pattern plating. *(Electrochimica Acta,* vol. 523, April 2025, https://doi.org/10.1016/j.electacta.2025.145902)

Semiconductors

"Three-Dimensional Transistors with Two-Dimensional Semiconductors for Future CMOS Scaling"

Authors: Arnab Pal, *et al.*

Abstract: Atomically thin two-dimensional (2-D) semiconductors – particularly transition metal dichalcogenides – are potential channel materials for post-silicon complementary metal-oxide-semiconductor (CMOS) field-effect transistors. Their application in CMOS technology, however, will require implementation in three-dimensional (3-D)

transistors. The authors report a framework for designing scaled 3-D transistors using 2-D semiconductors. The approach is based on non-equilibrium Green's function quantum transport simulations that incorporate the effects of non-ideal Schottky contacts and inclusive capacitance calculations, with material inputs derived from density functional theory simulations. A comparative performance analysis of different 3-D transistors (2-D and silicon-based) and channel thicknesses is carried out for both low-standby-power and high-performance applications. This suggests that trilayer tungsten disulfide is the most promising material, offering an improvement in energy-delay product of over 55% compared with silicon counterparts, potentially extending CMOS scaling down to a few nanometers. The authors also show that 2-D semiconductors could be uniquely engineered to create 2-D nanoplate field-effect transistors that offer nearly tenfold improvement in integration density and drive current over both 2-D- and silicon-based 3-D field-effect transistors with similar footprints. *(Nature Electronics,* December 2024; nature.com/articles/s41928-024-01289-8)