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CIRCUITS ASSEMBLY

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Designing the **PCB Stackup**

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The Electronics Industry's East Coast Conference and Exhibition

PCB EAST 2026

Conference & Exhibition

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Exhibition: **Wednesday, April 29**

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PCB EAST 2026

Conference & Exhibition

Exhibition: **Wednesday, April 29**

Conference: **April 28 – May 1**

DCU Convention Center
Worcester, MA

WHO'S EXHIBITING (to date)

Accurate Circuit Engineering
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All Flex Solutions, Inc.
AMD
American Computer Development, Inc. (ACDi)
ASC Sunstone Circuits
BittWare
Blue Pearl Solutions, Inc.
Breadboard
Cofactr
DirectPCB
Efinix
Electronic Interconnect
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ESPEC North America Inc
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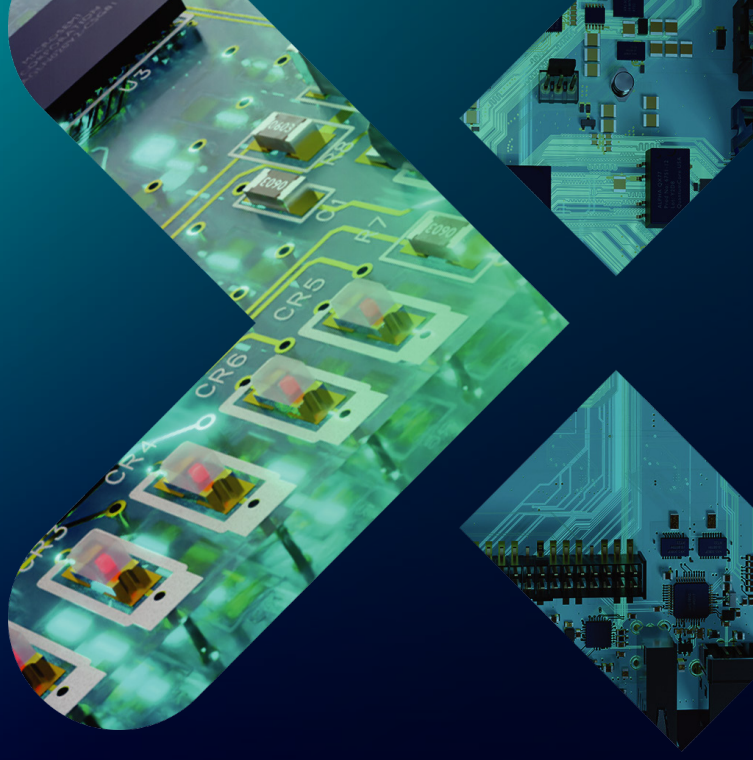

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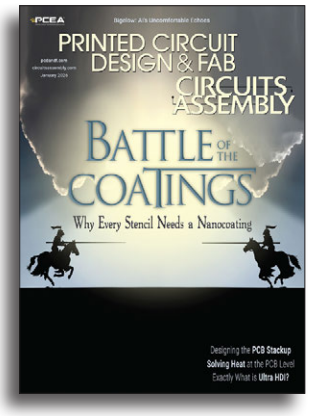
MONEY MATTERS

TECH TALK

DEPARTMENTS

FEATURES



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PCB Chat

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MANAGEMENT

PRESIDENT
Mike Buetow 617-327-4702 | mike@pcea.net

VICE PRESIDENT, SALES & MARKETING
Frances Stewart 770-361-7826 | frances@pcea.net

PCD&F/CIRCUITS ASSEMBLY EDITORIAL

MANAGING EDITOR
Ryann Howard 912-803-9780 | ryann@pcea.net

COLUMNISTS AND ADVISORS

Jeffrey Beauchamp, Peter Bigelow, Robert Boguski, John Burkhert, Jr., Stephen Chavez, Mark Finstad, Geoffrey Hazelett, Nick Koop, Jake Kulp, Alun Morgan, Susan Mucha, Greg Papandrew, Chrys Shea, Jan Vardaman, Gene Weiner

PRODUCTION

ART DIRECTOR & PRODUCTION
blueprint4MARKETING, Inc. | production@pcea.net
Nathan Hoeller | nathan@pcea.net

SALES

VICE PRESIDENT, SALES & MARKETING
Frances Stewart 770-361-7826 | frances@pcea.net

SENIOR SALES EXECUTIVE
Will Bruwer 404-313-1539 | will@pcea.net

REPRINTS

sales@pcea.net

EVENTS/TRADE SHOWS

EXHIBIT SALES
Frances Stewart 770-361-7826 | frances@pcea.net

TECHNICAL CONFERENCE
Mike Buetow 617-327-4702 | mike@pcea.net

SUBSCRIPTIONS

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When the Robots Stop: From San Francisco, a Cautionary Tale

MANY YEARS AGO, in *The Dark Knight*, Batman's nemesis the Joker famously observed that nobody panics when things go "according to plan – even if the plan is horrifying." It's when the unexpected happens that chaos erupts.

San Francisco got a taste of that chaos in late December when a power outage brought the city's fleet of Waymo autonomous vehicles to a standstill. For hours, the self-driving cars sat motionless at darkened intersections, hazard lights blinking, blocking traffic and stranding frustrated drivers. Social media lit up with videos of the gridlock. Tow trucks worked overtime. And the ride-hailing service that had been touting its superior safety record was forced offline.

Let's be clear: Waymo's safety statistics are impressive. According to the company, its autonomous vehicles have 90% fewer serious injury crashes, 82% fewer airbag deployments and 81% fewer injury-causing incidents compared to human drivers over the same distance. Dr. Jonathan Slotkin, a Pennsylvania neurosurgeon and trauma specialist who analyzed Waymo's data, suggests that if just 30% of cars were fully automated, we might prevent 40% of crashes. That's a compelling case for autonomous vehicles.

Except when the power goes out.

The malfunctions are especially puzzling because these vehicles are specifically designed to handle lost connectivity and dead traffic signals. Poor weather on occasion knocks out traffic lights in San Francisco without causing problems. The cars run on onboard batteries and are engineered to operate in areas where wireless signals drop.

Yet they did. Or at least, they relied on something that failed when the grid went dark.

Waymo explained that while its vehicles treat nonfunctional signals as four-way stops, "the sheer scale of the outage led to instances where vehicles remained stationary longer than usual to confirm the state of the affected intersections." Translation: the system got overwhelmed and froze.

The irony is, remote facilitation may be more critical to safe operation than we know. Some autonomous vehicle companies employ remote technicians who help these cars navigate situations they can't solve independently. To wit, Tesla's Robotaxis, which have onboard remote assistance monitored by humans, reportedly operated without problems during the same outage. That's worth noting.

In the electronics industry, we understand redundancy, fault tolerance and graceful degradation. We design systems

expecting failures. But public infrastructure – and that's what these vehicles have become – requires the highest standard. When you're transporting people, blocking intersections and potentially impeding emergency services, "system bugs and failures" aren't acceptable.

No injuries or accidents resulted from the Waymo outages, which is fortunate. But the company has previously issued recalls after software malfunctions caused vehicles to collide with a pickup truck and a telephone pole in Phoenix. The pattern suggests that edge cases and unexpected scenarios remain significant challenges.

If you are thinking it's unusual for electronics and public health to intersect so dramatically, you are not alone. The fundamental question remains: Are these systems truly ready for widespread deployment?

Dr. Slotkin's assessment is that it's in the public's best interests to make the transition to autonomous vehicles, because even with the potential for mistakes the robots are less error-prone than humans.

But December's power outage revealed something important: when systems fail – which eventually they all do – autonomous vehicles can create new problems even as they solve old ones. The technology may be 90% safer in normal conditions, but what happens in abnormal conditions matters too. It's up to all of us to decide just how much.

By the next afternoon, San Francisco streets returned to normal, aside from the conspicuous absence of Waymos. When service resumed, users were still greeted with: "Our service is currently paused. We're sorry for the inconvenience – please check back again soon."

The inconvenience passed. The questions remain.

The Joker was right about one thing: it's the unexpected that causes panic. If autonomous vehicles are going to share our streets, they need to be ready to handle the chaos. And so must we.

mike@pcea.net
@mikebuetow

P.S. Registration for PCB East opens later this month. Be sure to check out the full slate of offerings this year: technical conferences for design and fabrication, plus three dedicated assembly tracks, including an all-day hand soldering workshop! Plus, the PCB Management Forum and the FPGA Horizons conference. All of this wraps around the one-day exhibition on April 29, featuring more than 80 companies, including AMD, Microchip, Samtec and the leading PCB EDA software vendors. Hope to see you there.

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

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Quilter AI Tool Lays Out Complete Computer Design in Less than Week, Company Says

LOS ANGELES – Quilter in December announced the creation of a printed circuit board design for a computer using artificial intelligence tools in under a week.

The startup company, founded in 2019 by former SpaceX engineer Sergiy Nesterenko, said a single engineer completed the layout taking a schematic to manufacturing-ready files in less than a week, a process that traditionally takes an entire engineering team months and requires multiple rounds of redesign. This initiative, called Project Speedrun, represents a major milestone for the hardware industry, demonstrating an ability to compress quarter-long hardware R&D cycles into rapid weekly experiments.

Project Speedrun based its computer design around the widely used NXP i.MX 8M Mini processor, the same embedded computing hardware commonly used in automotive infotainment, safety and machine-vision systems. The system was fully functional upon first boot, capable of handling the demands of video calls, video games and more – a rare outcome in printed circuit board design, where projects typically build in as many as 3-5 respins when scoping.

Professional PCB designers quoted 428 hours of manual labor to create the same two-board system that Project Speedrun would produce; 238 hours for the baseboard and 190 hours for the system-on-module (SOM). With Quilter, 98% of the placement, routing and physics validation was completed autonomously in 27 hours. A single engineer required 12 hours to clean up the baseboard and 26.5 hours to clean up the SOM, which represents an 11x acceleration overall and a peak of 20x improvement on the baseboard.

Quilter works by using physics-driven reinforcement learning to explore manufacturable board layouts. Instead of placing hundreds of components and routing thousands of traces manually, engineers simply submit a schematic and let the AI generate multiple physics-tested designs to choose from.

“We see this as the compiler moment for hardware,” said Nesterenko. “What used to take a team months now happens in days, which means you reach market months, if not a year, ahead of competitors. That’s how hardware will be built from now on.”

Tony Fadell, an investor in Quilter, founder of Nest and a codeveloper of the iPod and iPhone, commented, “Everyone in hardware knows that the best PCBs are still designed by humans, track by track, over weeks of painstaking work. Quilter blows that bottleneck apart. It’s a complete paradigm shift. When you iterate faster, you can out-innovate your competitors.”

Quilter integrates with Altium, Cadence and Siemens Xpedition, and runs natively on private cloud and GovCloud.

Guangzhou Guanghe Technology Files for Hong Kong IPO

HONG KONG, CHINA – Guangzhou Guanghe Technology has submitted its prospectus to the Hong Kong Stock Exchange, seeking a main-board listing with CITIC Securities and HSBC acting as joint sponsors.

According to its prospectus and third-party data from Frost & Sullivan, Guanghe ranked third globally and first among China-headquartered manufacturers by cumulative revenue from computing server PCBs between 2022 and 2024. Server-related products now account for more than 70% of total revenue, reflecting strong demand tied to AI workloads, data center expansion and high-performance computing.

The company operates major manufacturing bases in Guangdong and Hubei provinces and supplies both OEM customers and electronics manufacturing services providers through a direct sales model.

US-China Economic & Security Review Commission Highlights Need for American-Made PCBs

WASHINGTON – The US-China Economic and Security Review Commission has released its 2025 Report to Congress, warning that decades of offshoring PCB manufacturing have sharply eroded domestic capacity. According to the report, US PCB production in output value has fallen from roughly 30% of global supply in 2000 to just 4% today.

The Commission emphasized that semiconductors used in national defense, critical infrastructure and commercial systems all rely on PCBs as their foundational platform. It flagged US dependence on foreign suppliers, particularly China, which now accounts for approximately 60% of global PCB production, as a strategic vulnerability.

While current US defense needs are still supported by domestic manufacturers, the report noted that defense demand alone is insufficient to sustain a modern PCB industrial base. As a result, the United States lacks the capacity to scale production rapidly in response to national or economic security needs.

“We agree with the Commission’s finding that Congress should create or expand industrial policy tools, including grants, loans, loan guarantees, advanced manufacturing tax credits and a dedicated industrial finance entity, to rebuild domestic capacity, modernize equipment, and support the US workforce,” said David Schild, executive director of the Printed Circuit Board Association of America.

Schild added that the association is backing H.R. 3597, the Protecting Circuit Boards and Substrates (PCBS) Act, which aligns closely with the Commission’s recommendations. “We encourage members of Congress to co-sponsor this important legislation, which would help revitalize the US PCB industry and reduce risks to national and economic security,” he said.

Looming Substrate and Materials Shortages for Advanced Packaging, TechSearch Warns

AUSTIN, TX – Rapid growth in AI servers and data center hardware will push substrate demand beyond available capacity by 2028, forcing manufacturers to expand production within the next three years, according to a recent report from TechSearch International.

Advanced Packaging Update highlights rising pressure on substrate materials – especially glass fiber used in core constructions – and evaluates potential alternatives as supply tightens.

The analysis also compares projected high-bandwidth memory (HBM) demand against planned capacity, noting widening gaps as AI accelerators scale. A dedicated section examines hybrid bonding adoption, equipment requirements, and competing fine-pitch interconnect approaches now entering development.

Foxconn to Invest $170M to Build Electronics Manufacturing Plant in Louisville

LOUSIVILLE, KY – Foxconn in December confirmed plans to establish a US production hub in Louisville, announcing a $170 million investment that will bring 180 new jobs to the region. The project is being supported by Kentucky Economic Development Finance Authority incentives for the company.

The company expects production to begin in the third quarter of next year.

Foxconn plans a new $170 million electronics manufacturing plant in Louisville.

Executives from Foxconn Technology USA joined Louisville Mayor Craig Greenberg to unveil the plan, noting that

the facility will produce a well-known consumer product for a well-known brand, though further details were not disclosed. During the announcement, a global operations map labeled the Louisville site as "Kentucky Assembly – TV/Display," hinting at potential product categories.

Local officials said the project signals renewed momentum for US-based electronics manufacturing.

Foxconn has a long history of announcing major investment programs in the US, only to back away, however. Over the past decade, new plants in Wisconsin, Pennsylvania and other states have been announced, only to fail to materialize as planned – or at all.

Incap Buys Lacon in $54M Deal, Expands Defense and Design Services

HELSINKI – Incap has signed an agreement to acquire 100% of Germany's Lacon Group in a transaction valued at $54.2 million, marking an expansion of the Finnish EMS provider's presence in Europe and growing its position in fast-growing defense and industrial markets.

Lacon Group operates EMS and ODM facilities in Germany and Romania totaling roughly 21,300m^2. Its offering includes PCB assembly, cable harnessing, box build, system integration and design and testing services, which are capabilities that expand Incap's scope beyond manufacturing and into full product-development support. For the first 10 months of 2025, Lacon reported unaudited revenue of $61.8 million.

The purchase price will be paid in cash and funded through Incap's own reserves and a bank loan of about $32.5 million. An additional earn-out of up to $5.4 million may be paid in 2027 based on Lacon's 2026 financial performance. Closing is expected in the first quarter of 2026 pending foreign-investment approvals in Germany and Romania.

Incap expects the acquisition to increase revenue in 2026 and have a slightly positive effect on operating profit after accounting for integration and purchase-price allocation costs. The deal also gives Incap a larger foothold in the DACH region and adds more than 600 employees, bringing the combined organization to over 3,000 employees across Europe, Asia and North America.

Micro-Precision Technologies Acquires Stellar Manufacturing

SALEM, NH – Micro-Precision Technologies has acquired Stellar Manufacturing, adding PCB assembly capabilities to its US microelectronics platform. The deal, which closed in early October, builds on MPT's partnership with Great River Capital Partners and supports its expansion across defense, aerospace, medical and commercial markets.

Stellar's Salem, NH, operation will continue serving customers. MPT said the acquisition combines Stellar's PCBA expertise with its own hybrid, multichip module and thick-film technologies.

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AGY will invest $12 million to expand specialty glass fiber production at its Aiken County, SC, facility, adding 80 jobs and increasing capacity for materials used in semiconductor packaging and high-performance printed circuit boards. Operations are expected to begin in early 2026.

Calumet Electronics installed a **Schmid** Infinity H+ developer.

Celus announced electronic component supplier **AGS Devices** has officially gone "live" with the Celus Design Platform, an AI-assisted electronics design platform.

Doosan Electro-Materials is reportedly positioned to become the sole CCL supplier for **Nvidia's** upcoming Rubin AI platform.

Ecarx has partnered with **Victory Giant Technology** to scale production of high-performance automotive computing platforms.

KKR has reportedly become the main contender for the acquisition of assets of **Taiyo Holdings,** with the intent to privatize the Japanese chemical company.

Mobius Materials has closed a $3 million seed round to expand its authenticated semiconductor spot market.

Syrma SGS has started building a PCB facility in Andhra Pradesh, India, to expand domestic production capacity.

Wipro Electronics plans to begin operations at its new, $60 million PCB facility in Doddaballapura, Bengaluru North within the next nine months.

CA

AIM Solder appointed **RMG Vietnam** authorized distributor in Southeast Asia.

Amber Enterprises India has completed the acquisition of a majority stake in Pune-based **Shogini Technoarts**.

Coherix opened a new vision center in Sinsheim, Germany.

Critical Manufacturing partnered with **Canonical** to expand cloud-native MES deployment options across cloud, hybrid and on-premises manufacturing environments.

Foxconn and **Luxshare** plan to expand Vietnam's game console manufacturing capacity by several million units per year as both firms seek permits for large production increases across Northern Vietnam.

Foxconn is set to invest NT$15.9 billion ($510 million) to develop a new headquarters complex in Kaohsiung, Taiwan. Construction is scheduled to begin in 2027 and completion targeted for 2033.

Giga Computing is partnering with **Syrma SGS** for a production hub in Tamil Nadu, India.

Golden Technology broke ground on its second mobile phone manufacturing facility in Kurdistan.

GPV and **East/West Manufacturing** have entered into a strategic partnership whereby the two EMS companies will support each other's production to serve customers in regions affected by trade and domestic manufacturing compliance issues.

Kitron secured an $18.5 million contract to produce advanced electronic components for combat vehicle systems, with deliveries beginning in late 2026, and signed an $8.3 million agreement with a new customer to produce electronics for autonomous systems across air, land and sea domains for the defense industry.

Kitron in December received approval from Swedish competition authorities and the Swedish authority **ISP** to proceed with the acquisition of **Deltanordic,** a deal that was announced on Nov. 19.

Merck Electronics is entering qualification on its $581 million Kaohsiung materials plant.

NanoFlowX named **Bentec** representative in Europe and India.

Nidec Advance Technology and **Gantu Technology** are codeveloping AI-driven inspection and test solutions for PCBs and advanced semiconductor packaging.

Safari Circuits has acquired **Lacroix Electronics'** Grand Rapids, MI, manufacturing plant, preserving 116 PCB assembly jobs.

Samson has begun electronics manufacturing at its new Offenbach facility, completing the transition from Frankfurt.

Scanfil in December finalized its previously announced acquisition of US-based electronics manufacturer **Adco Circuits.**

Solutions Manufacturing installed a **Universal** Fuzion pick-and-place machine.

SynQor, which designs and manufactures power electronics, will relocate its 250 employees in Massachusetts to Salem, NH.

Tata Electronics and **Intel** signed an agreement to explore chip manufacturing, packaging, and AI PC development in India.

Wistron's board approved a new, $135 million investment plan to expand AI server and networking production at its campus in Hsinchu, Vietnam.

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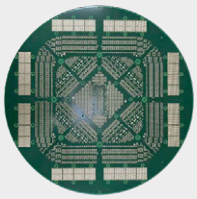

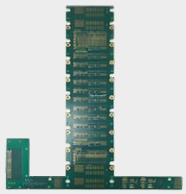

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Max. Panel Size: 620*710mm (24.4*28'')
Max. Board Thickness: 6mm
HDI: 3+N+3, Anylayer
Back Drilling
Max. Through Hole Aspect Ratio: 32:1
Max. Laser Via Aspect Ratio: 1:1
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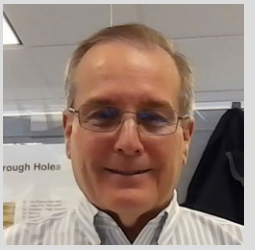
Denis Boulanger


Nancy Smith


Kelly Dack


Jay Gorajia


Steve Robinson


Paul Cooke

AdvancedPCB named **Lisa Holmes** director of global marketing.

AT&S appointed **Gerrit Steen** chief financial officer.

Blue Origin named **Chris Sadler** senior PCB designer.

Dan Beeker has retired from NXP and has assumed the role of president and CTO at System Solution Specialists.

Draper named **Denis Boulanger** principal engineer DFM PCB/CCA.

Equinox Power Innovations hired **Nancy Smith** as senior printed circuit board designer.

Kelly Dack joined Pioneer Circuits as senior applications engineer.

Siemens Digital Industries Software promoted **Jay Gorajia** to vice president – professional services and customer support – Lifecycle Management Solutions.

Steve Robinson, former president and CEO of APCT, Data Circuit and executive VP at Merix, passed away in December.

Summit Interconnect named **Paul Cooke** director of engineering.

CA


Billy Aldridge


Keith Howell


Tim Filteau


Sascha Brüning


Andrew Regrut

Helios Technologies promoted **Billy Aldridge** to president, electronics segment.

Keith Howell, technical director at Nihon Superior USA, passed away in December.

Naprotek appointed **Tim Filteau** chief executive officer.

Neways named **Sascha Brüning** vice president defense.

Kimball Electronics promoted **Andrew Regrut**, the company's treasurer and investor relations officer, to lead strategic development efforts.

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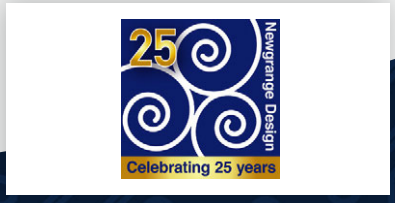

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PCB West Booth Space Now Open to Any Exhibitor

PEACHTREE CITY, GA – The exhibition floor for PCB West 2026 is now open to any prospective exhibitor. The exhibit floor is expected to sell out, as it has in 11 of the past 12 years.

PCB West will be held Sept. 29 to Oct. 2, 2026, at the Santa Clara (CA) Convention Center. The event includes a one-day exhibition on Sept. 30.

Booth sales opened in early November to returning exhibitors, and the exhibit floor is currently over 60% sold out.

"PCB West has sold out 11 of the past 12 years, and we fully expect it to do so again," said Frances Stewart, vice president of sales and marketing, PCEA. "Attendance at the show was up 3.5% year-over-year in 2025, and attendees have noted the access to vendors and each other as the primary reasons why they come to PCB West."

Companies interested in exhibiting should contact Stewart at frances@pcea.net for details.

PCB East More than 70% Sold Out

PEACHTREE CITY, GA – The exhibition floor space for PCB East 2026 is more than 70% booked and is expected to sell out. The one-day exhibition will be held Apr. 29 at the DCU Center in Worcester, MA, with a four-day conference taking place Apr. 28 – May 1.

"Since its return in 2021, PCB East has sold out each year, and we fully expect it to do so again," said Frances Stewart, vice president of sales and marketing, PCEA. "Attendance at the show was up 15% in 2025, and attendees have noted the access to vendors and each other as the primary reasons why they come to PCB East.

"With the exhibit floor selling out quickly for PCB East, we look forward to another outstanding event for the printed circuit engineering community in 2026."

“Moving PCB East is a major step for the electronics industry’s East Coast exhibition and conference,” said Mike Buetow, president, PCEA. “The DCU Center is a top-tier venue, and Worcester offers big-city advantages at a more affordable cost to attendees. This change reflects the event’s growth and the industry’s expanding needs.”

Companies interested in exhibiting should contact Frances Stewart at frances@pcea.net for details.

Registration for PCB East Conference to Open this Month

PEACHTREE CITY, GA – Registration for the PCB East 2026 conference and exhibition will open this month. PCB East will feature more than 65 hours of design and manufacturing classes, plus another 18 hours of assembly courses during the four days starting in late April.

In addition, this year’s event will offer a two-day, two-track conference on FPGA, produced by FPGA Horizons.

The 2026 conference takes place Apr. 28 – May 1 at the DCU Center in suburban Boston.

Among the 33 printed circuit design classes are 20 new to PCB East, including talks on designing high-thermal PCBs, design-time estimation, DfM for UHDI, design for test, and the fundamentals of EMC. Speakers include Rick Hartley, Susy Webb, Stephen Chavez, Tomas Chester and Karen Burnham, among others.

The three-track assembly conference, chaired by Chrys Shea, includes an all-day hands-on soldering class, plus two half-day sessions on circuit assembly. An all-day session on management and supply chain, with a special focus on security, robustness, equipment evaluation and workforce development, rounds out the program.

Leading off the week is a one-day management session, Strategic Leadership in the Age of AI, New Technology Adoption, and Talent Scarcity: Executive Strategies for AI Adoption, Meeting Workforce Challenges, and New PCB Process Selection For Advanced Electronics Packaging, chaired by Gene Weiner and Peter Bigelow and featuring talks on technology implementation, workforce skills training, market conditions and legislative updates will take place on Apr. 28.

More details are forthcoming at pcbeast.com.

Spring PCB Design Training Classes Scheduled

PEACHTREE CITY, GA – Registration is open for the next PCEA Training Certified Professional Circuit Designer (CPCD) training and certification classes.

Upcoming sessions are

- Feb. 6, 13, 20, 27, and Mar. 6. Registration closes Jan. 9.
- May 15, 22, 29, Jun. 5 and 12. Registration closes Apr. 16.

The 40-hour instructor-led course is designed for printed circuit engineers, layout professionals and other individuals currently serving in the design engineering industry or seeking to get into it.

The classes cover the gamut of printed circuit design engineering, from layout, place and route to specifications and materials to manufacturing methods. Schematic capture, signal integrity and EMI/EMC are also part of the comprehensive program.

Each class includes a copy of *Printed Circuit Engineering Professional,* a 400-page handbook on circuit board design, and the optional certification exam recognized by PCEA.

There are no prerequisites to enroll. Classes are held online and led by experienced instructors.

To enroll, visit pceatraining.net/registration.

PCEA CURRENT EVENTS

ASSOCIATION NEWS

Certification. The following recently passed the PCEA Certified Printed Circuit Designer exam:

- John Andorf
- Joshua Cruz
- Michael Dauphinai
- Javier Feliciano
- Sean Welch

Conferences. PCB Detroit will return to the campus of Wayne State University on Jun. 15-16, 2026. More details will be forthcoming at pcea.net/events.

Networking. The PCEA Discord server brings together engineers and designers from around the world on a private channel to discuss technical questions and career opportunities. To join, contact PCEA.

Recent conversations covered the implementation of copper pours, design reviews and low-voltage differential signals.

CHAPTER NEWS

Richmond, VA. Our next in-person meeting is being planned for January, possibly with a presentation on manufacturing tests. Contact Michael Burns for details.

Portland, OR. Our next chapter meeting will be held online on Jan. 22. The tentative topic is thermal issues and thermal management. Contact Stephan Schmidt for details.

The Electronics Industry's East Coast Conference and Exhibition

PCB EAST 2026

Conference & Exhibition

SAVE THE *Date*

Conference: **April 28 – May 1**

Exhibition: **Wednesday, April 29**

DCU Convention Center, Worcester, MA

colocated with FPGA HORIZONS BEYOND GATE ARRAYS

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The Electronics Industry's East Coast Conference and Exhibition

PCB EAST 2026

Conference & Exhibition

Exhibition: **Wednesday, April 29**

Conference: **April 28 – May 1**

DCU Convention Center
Worcester, MA

WHO'S EXHIBITING (to date)

Accurate Circuit Engineering
Adiuvo Engineering
All Flex Solutions, Inc.
AMD
American Computer Development, Inc. (ACDi)
ASC Sunstone Circuits
BittWare
Blue Pearl Solutions, Inc.
Breadboard
Cofactr
DirectPCB
Efinix
Electronic Interconnect
Eleprint S.R.L.
EMA Design Automation
EMX US Inc.
ESPEC North America Inc
Fineline Global
Flexible Circuit Technologies
Freedom CAD Services, Inc.
Glory Faith Electronics Co., Ltd.
GS Swiss PCB
InstaDeep
JBC Tools USA Inc.
JS Circuit
K2 Engineering Services
Lattice Semiconductor
Microchip Technology Inc.
Millenium Circuits Limited
NCAB Group
Newgrange Design
OKI Circuit Technology Co., Ltd.
PalPilot International Corp.
PCB Technologies USA, Inc.
PCBWay
Photonics Systems USA Inc.
Polar Instruments, Inc.
Polyonics Inc.
Precision Circuit Technologies
Printed Circuit Engineering Assoc. (PCEA)
Quantic Ohmega-Ticer
RBB
Samtec
Screaming Circuits
Sierra Circuits
Suntech Circuits
Trylene Inc.
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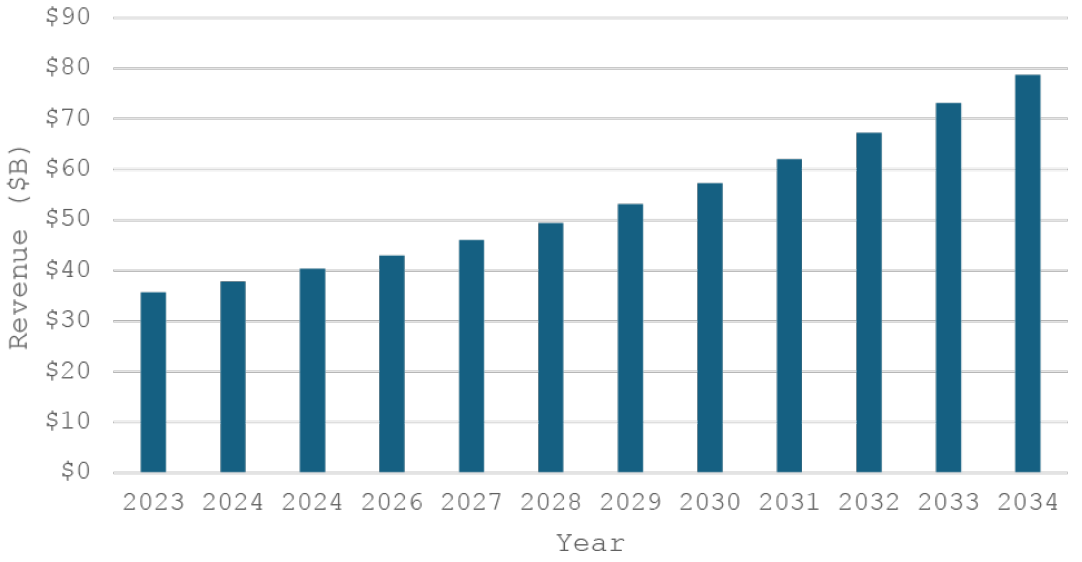
MARKET **WATCH**

Advanced Packaging Market Set to Double by 2034

OTTAWA – The advanced packaging market is poised for explosive growth over the next five years, driven by AI, high-performance computing and the insatiable demand for smaller, faster electronics, a new report asserts.

According to new research from Towards Packaging, the global advanced packaging sector will climb to $78.8 billion by 2034 from $40.3 billion in 2025 – a compound annual growth rate of 7.6%.



Change in advanced packaging revenue, 2023-34. (Source: Towards Packaging)

And with the growth will come a fundamental shift in how semiconductors are assembled and interconnected, the firm says.

The growth drivers are familiar to anyone tracking the industry: AI accelerators need enormous bandwidth and power efficiency. Data centers are proliferating. Automotive electronics keep getting more complex. And consumer devices? They're demanding performance that can only be delivered through advanced heterogeneous integration.

Fan-out wafer-level packaging is leading the charge, offering superior thermal performance and smaller footprints critical for mobile and wearable applications. But it's the chiplet revolution that's really changing the game. By disaggregating monolithic designs into smaller, specialized dies, manufacturers can mix and match components, boost yields and dramatically reduce costs.

2.5D and 3D packaging technologies continue to mature, with through-silicon vias (TSVs) and interposers enabling the high-bandwidth, low-latency connections that AI and HPC applications require. Meanwhile, system-in-package (SiP) solutions are carving out territory in IoT, wearables and 5G infrastructure by integrating multiple functions into compact modules.

Use of panel-level packaging (PLP), which involves larger panel substrates instead of individual wafers, is rising, which can lower per-unit cost and improve throughput.

North America remains the dominant region, thanks in large part to its strong semiconductor ecosystem, rapid adoption of AI and 5G technologies, and continuous R&D investments.

Computers Adding Up

Trends in the US electronics equipment market (shipments only)

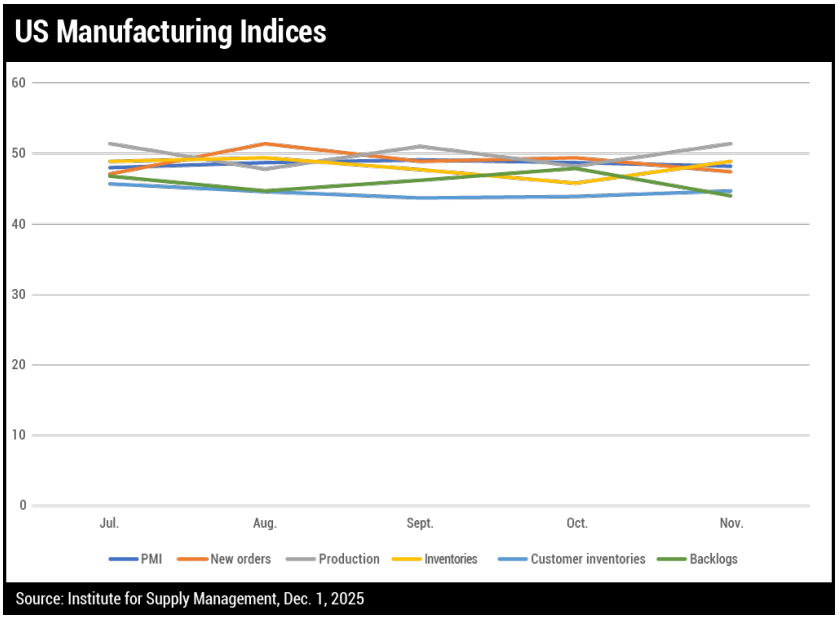
	% CHANGE			
	JUL.	AUG.[r]	SEPT.[p]	YTD
Computers and electronics products	0.2	-0.2	-0.1	4.9
Computers	1.8	-1.0	1.5	14.4
Storage devices	6.9	-0.2	-5.2	9.7
Other peripheral equipment	7.3	-7.6	-8.4	11.5
Nondefense communications equipment	-0.2	2.5	1.9	7.6
Defense communications equipment	-6.9	-1.9	-2.4	-1.0
A/V equipment	6.1	-4.5	-2.4	-3.1
Components[1]	-0.2	-0.1	-0.7	4.6
Nondefense search and navigation equipment	0.1	-2.5	0.4	3.8
Defense search and navigation equipment	-0.7	-0.6	1.1	2.3
Electromedical, measurement and control	-0.7	0.6	0.1	4.3

[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, Dec. 4, 2025

Key Components

	JUL.	AUG.	SEPT.	OCT.	NOV.
EMS book-to-bill[1,3]	1.23	1.26	1.31	1.26	
Semiconductors[2,3]	20.6%	21.7%	15.3%	27.2%	
PCB book-to-bill[1,3]	1.00	0.98	0.92	1.00	
Component sales sentiment[4]	121.6%	113.2%	121.6%	122.2%	120.1%

Sources: [1]IPC (N. America), [2]SIA, [3]3-month moving average, [4]ECIA



Hot Takes

Taiwan's **sales of rigid printed circuit boards** rose 16% year-over-year in November. (TPCA)

The US Pentagon has launched a $1 billion program to build an industrial base for **attack drones.** (US government)

Worldwide **foldable smartphone shipments** are forecast to grow 10% year-over-year in 2025 to 20.6 million units. (IDC)

Global **smartphone shipments** are expected to decline 2.1% in 2026 as rising chip costs are likely to impact demand. (Counterpoint)

Taiwan's PCB industry is on track to generate $29 billion in output in 2025, representing 11.1% year-over-year growth. Combined domestic and overseas PCB production was up 11% to $21.2 billion during the first three quarters. (TPCA)

Global **chipmaking equipment sales** will rise 9% to $126 billion in 2026, and past $150 billion for the first time in 2027. (SEMI)

China's November factory PMI contracted for an eighth month, falling to 49.2, underscoring continued weakness in electronics and PCB manufacturing despite a recent US-China tariff truce.

Worldwide **server market revenue** reached a record $112 billion during the third quarter, a year-over-year increase of 61% in vendor revenue. (IDC)

Vietnam's electronics exports hit nearly $143 billion year-to-date through November, with computer, components and device shipments surging 48%. (Vietnam Customs)

US retail sales in November and December will grow between 3.7% and 4.2% versus 2024, for total spending between $1.01 trillion and $1.02 trillion. (National Retail Federation)

ROI

AI Demand Echoes the Late-'90s Tech Surge

Memory chip shortages and PCB order spikes signal strength, but history suggests caution amid the hype.

IT APPEARS THAT possibly, as baseball legend Yogi Berra would have said, it's déjà vu all over again.

Reuters reports that the AI (artificial intelligence) frenzy is creating a major shortage of memory chips, used in everything from consumer electronics and industrial equipment to computers and even the most advanced military systems. Concurrently, the Global Electronics Association (IPC) reported that printed circuit board bookings and shipments surged during October. While both announcements suggest that the electronics industry is alive and well, could they also be a forewarning that we are heading toward the same euphoric economic environment that occurred in the late 1990s?

For the electronics industry, the late 1990s was the best of times, until they weren't. PC power was growing by leaps and bounds, creating constant demand for the latest iteration. The internet was in its infancy, creating an insatiable demand for servers and all the infrastructure required to harness emerging technology and enable users to take full advantage of the nascent web. The dot-com frenzy was upon us. Add to that the fear that Y2K, the millennial bug, would render older computers and analog technologies inoperable, which prompted further demand for new, compliant equipment. Demand for all things electronic, and the printed circuit boards and assemblies that the new technology was built on, was skyrocketing, and company revenues and profits were soaring.

Regrettably, the euphoric '90s came to a stunning halt in 2001. Companies with year-long order books had the rude awakening first that demand was flattening, and then decreasing. Inventories spiked. As a white-hot industry cooled, overcommitted companies began to cancel orders. For the electronics industry, especially the circuit board industry, the bottom fell out and many, many businesses foundered. The best of times became the worst of times.

Many will say, that was then, but this time is different. True, we do not have to contend with the uncertainty of a new millennium; we are now a quarter of the way through it. What is similar – if not identical – however, is the economic frenzy an emerging technology is creating, coupled with the resultant demand for electronics. As with the dot-com environment of the late '90s, euphoria over AI now drives the electronics industry. Every business "must" either make or use AI – even if they are not sure how. Consumers are equally enchanted with the likes of ChatGPT or Google AI Overview, which are being played with and deployed for a host of trivial and major activities.

As with many exciting new technologies, a mixture of science, wishful thinking and a lot of hype have swirled together in the story. Since the dot-com era, other "must-have" technologies have been championed. Electric vehicles

are a recent example that has proven exciting and technologically successful, but perhaps disappointing when it comes to worldwide demand. And while EVs are here to stay, many auto companies are scaling back sales projections, production, new product development and, most importantly, are writing off huge investments that will not meet prior forecasts.

The question is, will demand for all things AI come to the same abrupt demise as the dot-com bubble, or just fizzle, as is occurring with EVs? More importantly, will today's electronics companies take what was learned back then and apply those lessons to avoid potential future calamity?

Short term, the future of AI may serve our industry well in creating demand, filling plants and providing the profits to continue investing in our businesses. Clearly, serious money is being invested at all levels of the AI supply chain. And with any new technology, the goal should be to participate at some level and to take advantage of the opportunity at hand. The challenge is not losing objectivity amid all the hype.

When dealing with anything new, a jaundiced eye can be helpful. Upward projections of demand are fine. Unrealistic or euphoric projections should be questioned and challenged, however. When planning capacity utilization or considering expanding capacity, also consider the business response if projections do not materialize. What if the exit ramp is straight down? Possibly most importantly, diversify your customer base, so all your business eggs are not in a single end-market basket.

AI is the next exciting technology. Just be aware that our industry has been there before many times and, in the past, when there has been excessive hype, the end game has not necessarily gone well. As we all navigate the excitement, use lessons from the past to reduce some of the inevitable risk.

PETER BIGELOW has more than 30 years' experience as a PCB executive, most recently as president of FTG Circuits Haverhill; peterbigelow@msn.com. He is vice chair of the PCEA PCB Management Symposium, taking place April 28 at PCB East.

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September 29 - October 2
EXHIBITION:
Wednesday, September 30

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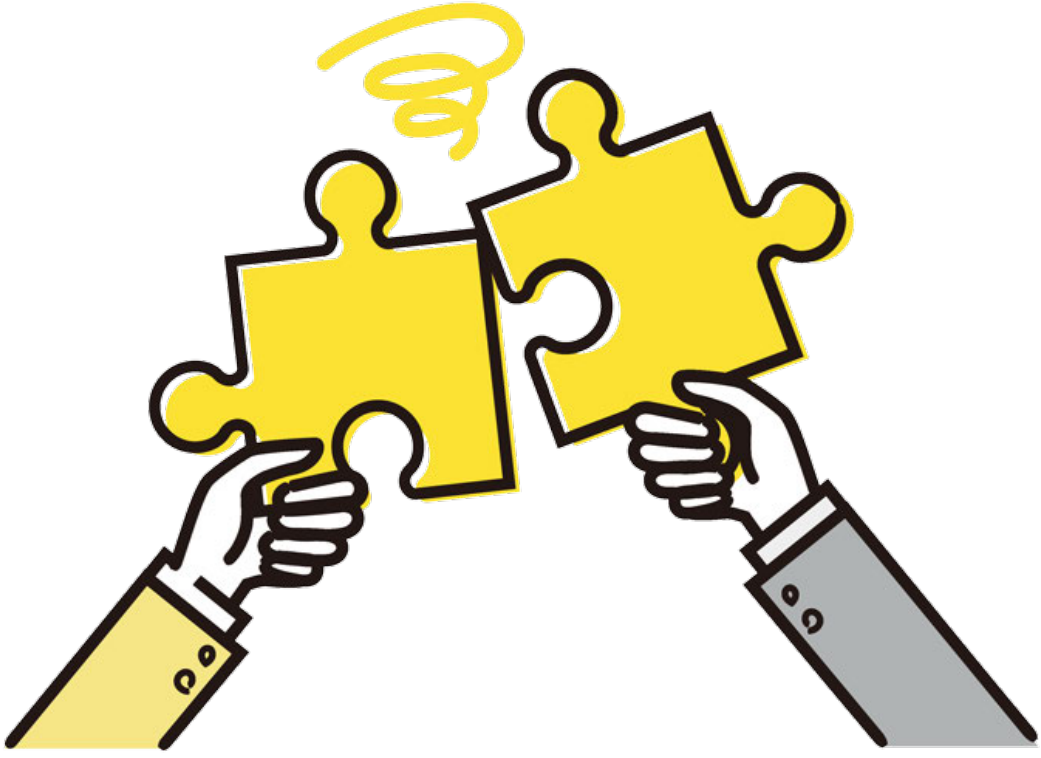
FOCUS ON BUSINESS

Lessons From My Worst Sales Hires

You're going to make some mistakes!

HAVING LED DIFFERENT-SIZED sales forces over the years, I've made some massive hiring mistakes. This isn't a "how to avoid all hiring mistakes" piece; everyone will make hiring errors over a long and active career. It is how you respond to those mistakes that can make a big difference in your company.



Some of my mistakes:

- A top East Coast sales manager had an impeccable resume and a history of accomplishments. All his references checked out, and he passed my multiple-stage interviews with his peers and me. Every response was spot-on, demonstrating an uncanny knowledge of our business, and he seemed perfect. At my board meeting, as I was preparing an offer, I advised the board of my concerns that he seems "too good" to be true, but we would know in 90 days. Without too much detail, we began to see issues in the 60-day period, and when 90 days were almost up, I was preparing a termination. He resigned on day 89, having accomplished nothing we jointly set out as a plan for him.

- A gentleman on the West Coast had an impeccable history, accomplishments, solid paper and a depth of understanding of the EMS industry. He was also my worst-ever hire. When I finally understood the mistake I had made and began a corrective program, he quit as well. The lies and falsehoods he made about our company capabilities and myself caused damage across the region to our brand, his teammates (backdoor gossip), and my leadership. On an exit interview he told HR he was afraid I would resort to violence once he left. I had to personally own the corrective actions across the territory, repairing the lies, and it became a massive time-suck to get back to ground zero with potential customers, manufacturer reps and some existing customers. (This pattern repeated in his subsequent career moves, or so I heard from hiring managers who were embarrassed that they, too, had hired him.)
- A young woman whose first three months were as strong as any new hire I ever made, bringing new opportunities and working with me on a massive deal I had started before she came aboard. We lost that deal (no fault of hers), and in the following three months every potential deal she brought to us fizzled, almost all before a quote stage. Then, communications stopped. Every call or "I am coming to travel with you" action was driven by me. We agreed on corrective actions, but none of the milestones was hit. Expenses ceased, new opportunities dried up, reports and CRM entries stopped. When I confronted her, she mentioned that she had "some issues" that were never disclosed to me or our HR department, and she couldn't work for us. After termination, it was rumored she may have held a concurrent job with a competitor.

Keep in mind I always lived and worked hundreds or thousands of miles away from my team, so we didn't meet face-to-face in the office every week. We had reporting (CRM) requirements, however, as well as many calls during the week. I also traveled with my team as often as possible, helping move deals forward or assisting with closing deals. Metrics were fudged, details of their activities were fabricated and when I made time to travel with them there seemed to be health or family reasons many of those planned trips had to be postponed. The 30, 60, 90, 180 and 360-day sales goals that were mutually agreed upon onboarding with each new hire, and their subsequent progress reports, mostly turned out to be inaccurate.

For many years, I ran remote sales forces ranging from three to 100 strong. But my propensity to believe my team over what the metrics were indicating led me to suboptimize my role to some degree with these three individuals. Some of these folks also came through professional EMS recruiters, who also could have been able to spot issues before presenting a candidate to me.

The takeaways:

1. When managing a team over a long period of time, you'll make hiring mistakes.
2. Good paper (résumés), prescreening by a recruiter, multiple "touch points" in an interview process with multiple cross-functional senior leaders, excellent knowledge of our business and solid references don't always guarantee a good hire.
3. In the highly competitive EMS sales world, with our extremely long sales cycles, it will probably take more than a few months to discover you have made a bad hire.
4. Personality tests don't guarantee a good fit.

5. Using a professional EMS recruiter is no guarantee. (Note to all my EMS recruiter friends: you are an excellent resource, just not foolproof.)
6. Setting 30, 60, 90, 180 and 360-day sales plans/goals during the first week of employment (onboarding), detailing jointly agreed-upon accomplishments/milestones, are a good indicator of future success, but not a 100% guarantee.
7. You cannot run a salesforce from a dashboard (CRM) alone. You must be in the field selling with them. That said, tracking progress in a CRM is an indicator to pay attention to.
8. A good passive way to view remote sales progress is expenses, which is counterintuitive to a fiscally conservative company. If they aren't spending on lunches, as one example, something's up.
9. Speaking with and visiting potential new prospects the new hire is engaging is smart practice, but no guarantee of success.
10. A detailed job description is important to avoid any misunderstanding early in an interview process.

I treated recruiting as a 24/7 sort of side job I had to do. I was always on the look-out for talent and performance. I used all these takeaways in the hiring process, and in managing them once they were hired. And while most of my recruiting was successful, I made some huge mistakes. How I responded when it became clear I made an error were some of my most memorable accomplishments.

Want to be a dynamic growth engine sales leader? Get over yourself. We all make mistakes. Failing to admit them, refusing to try to correct them, and finally having to make a hard termination call if you cannot turn the person around, is what can kill your small-to-medium-sized business. I was often asked if terminating an employee was hard. Yes! If it becomes easy to fire someone, it is time to punch out; you've lost your heart.

Use your best demonstrated practices recruiting and making hiring decisions, try not to make a quick hiring decision no matter how good the person seems, stay true to your recruitment process, and while you'll probably be successful most of the time, you will have some catastrophic failures. Identify them as fast as possible, invest time to correct those errors and terminate quickly when you are sure this was a hiring mistake.

JAKE KULP is founder of JHK Technical Solutions, where he assists OEMs and EMS companies with optimizing demand creation offerings and deciding when and where to outsource manufacturing. He previously spent nearly 40 years in executive roles in sales and business development at MC Assembly, Suntron, FlexTek, EMS, and AMP Inc. He can be reached at jkulp@cox.net.

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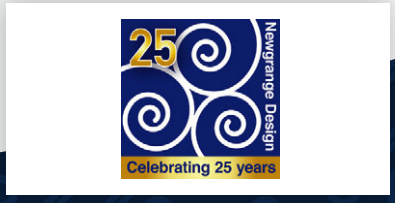

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DESIGNER'S **NOTEBOOK**

Reviewing the PCB Design Review Process

A structured design review process ensures alignment across teams.

ONE THING IS certain about printed circuit board design: change is inevitable. The vernacular surrounding the art and science of PCB design gives credence to this statement. Upfront, it's a schematic editor that leads to a layout editor. If you get far enough downstream, you're working with a Gerber editor. Across the board, the notion of making changes is distilled into the process.

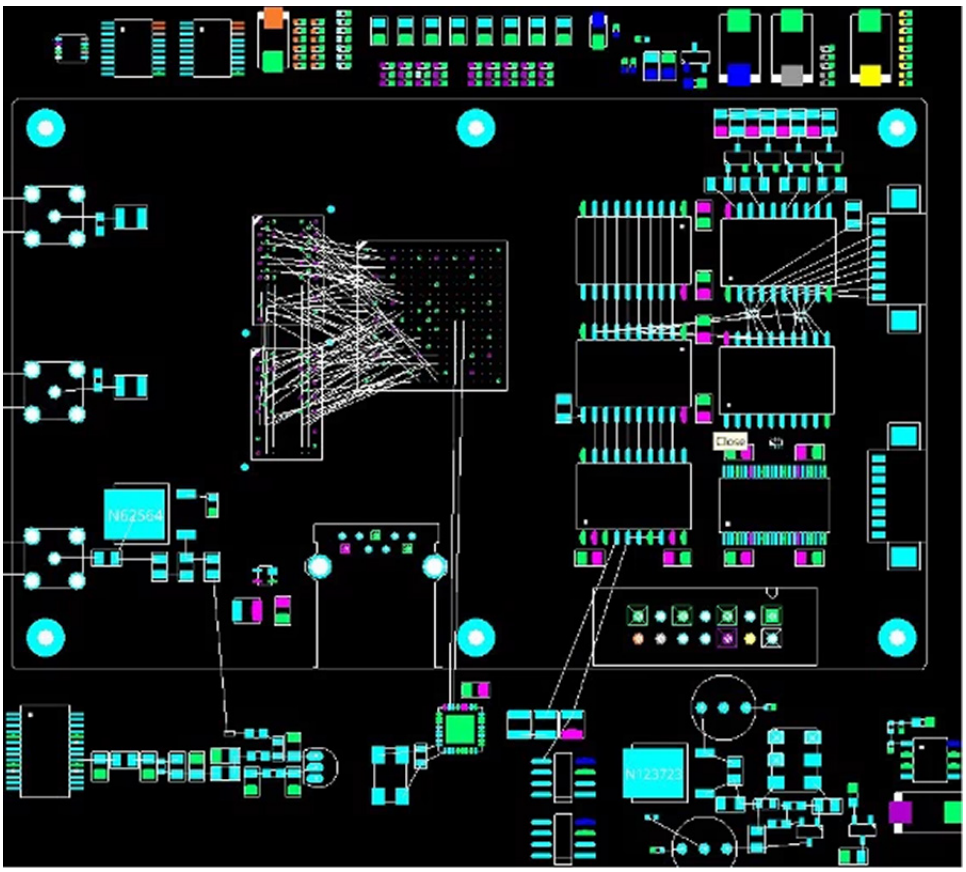

Figure 1. Colorizing power and ground domains helps floorplan the design. The passive components arrayed across the top of the board are mostly bypass capacitors intended for the secondary side. The components below are pre-placed to provide greater visibility into the extent of these subcircuits. (Credit: Author)

Another axiom in effect is: "If it works, don't break it." This sentiment is especially strong where a circuit must be qualified through a regulatory body. If a radio meets the requirements, it's as if it were written in stone rather than copper. Change is for the better unless it adds unreasonable risk or lengthens the schedule.

It's important to maintain that continuity while making improvements as needed. A second pair of eyes is always helpful and, in fact, the more the merrier, up to a point. The mechanical engineering of PCB layout is the foundation of the circuit board, while embedded electronics are the vessel for the software. Testing the circuit lies somewhere between these two camps. Herding all these cats requires finesse from the PCB designer.

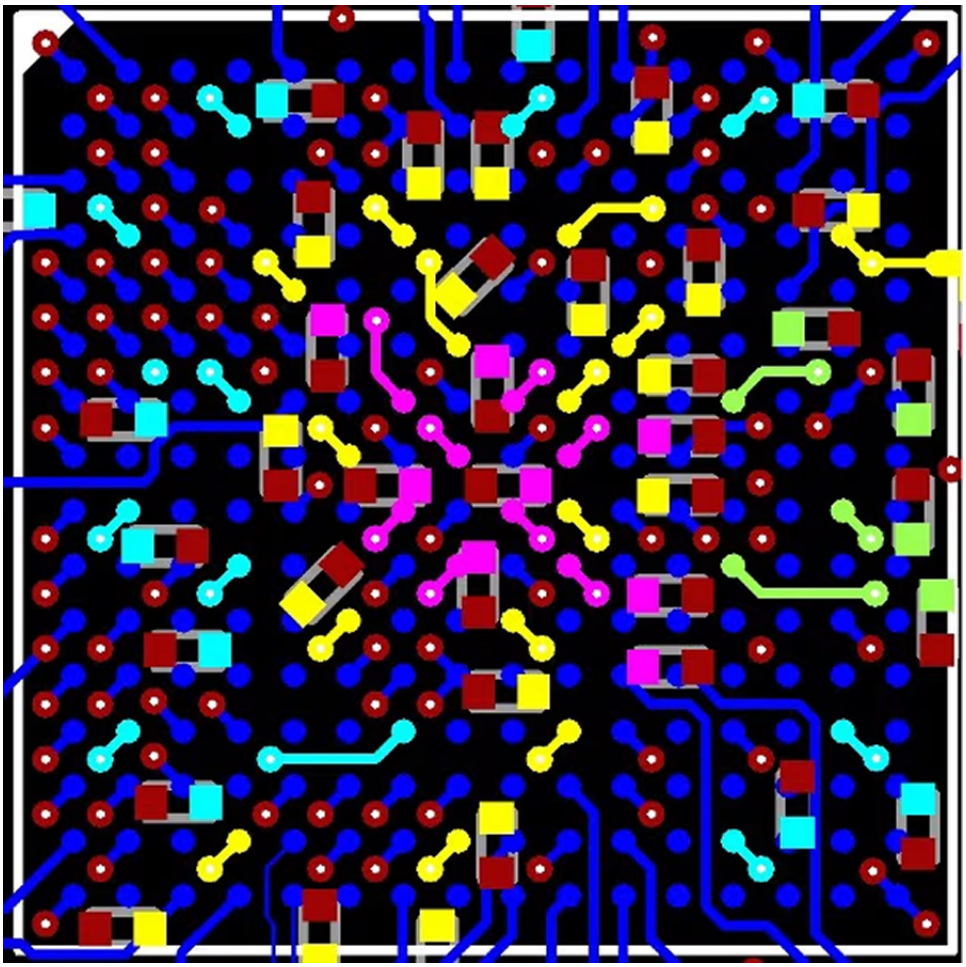

Figure 2. Capacitors on the bottom (red) respond to a 1.2V patch of pins (magenta) in the middle of the processor. Surrounding them is a ring of 2.5V (yellow). Finally, the outer voltage domain is for 1.8V (cyan) with a side of 3.3V (green). Completing this PDN is a top priority. (Credit: Author)

Getting the lay of the land. Kicking off a layout usually starts with the mechanical information. Design reuse of the mechanicals is a common theme. The trick is that later upgrades rarely come in the form of a reduction to the bill of materials. We fix electrical problems with more electronics, perhaps a new filter or a shield. Sometimes, it's another mounting hole, and it could be all those things at once.

We compete in the market with new features to enhance the product. Even with the same feature set, we're compelled toward faster, smaller and more efficient designs. You could say that revision 1 is just messing around, while revision 2 is after you find out what was overlooked in the rush to market.

With all of this going on, we can't go it alone. Tight schedules push us into a corner. Backtracking is a waste of that precious time and money. The goal is always to do it right the first time. All this is just to say that we need clear communication on every aspect of ongoing improvements.

Arbitrary and capricious “changes” can backfire. Don’t go at it alone. Schedule a design review at each stage of the design cycle. Day one of the schedule is a good time for setting milestones. Once you have an outline and a stackup, you have enough data for a budgetary quote from your vendor(s). “Vendor” should always be plural for the bare board as well as the components.

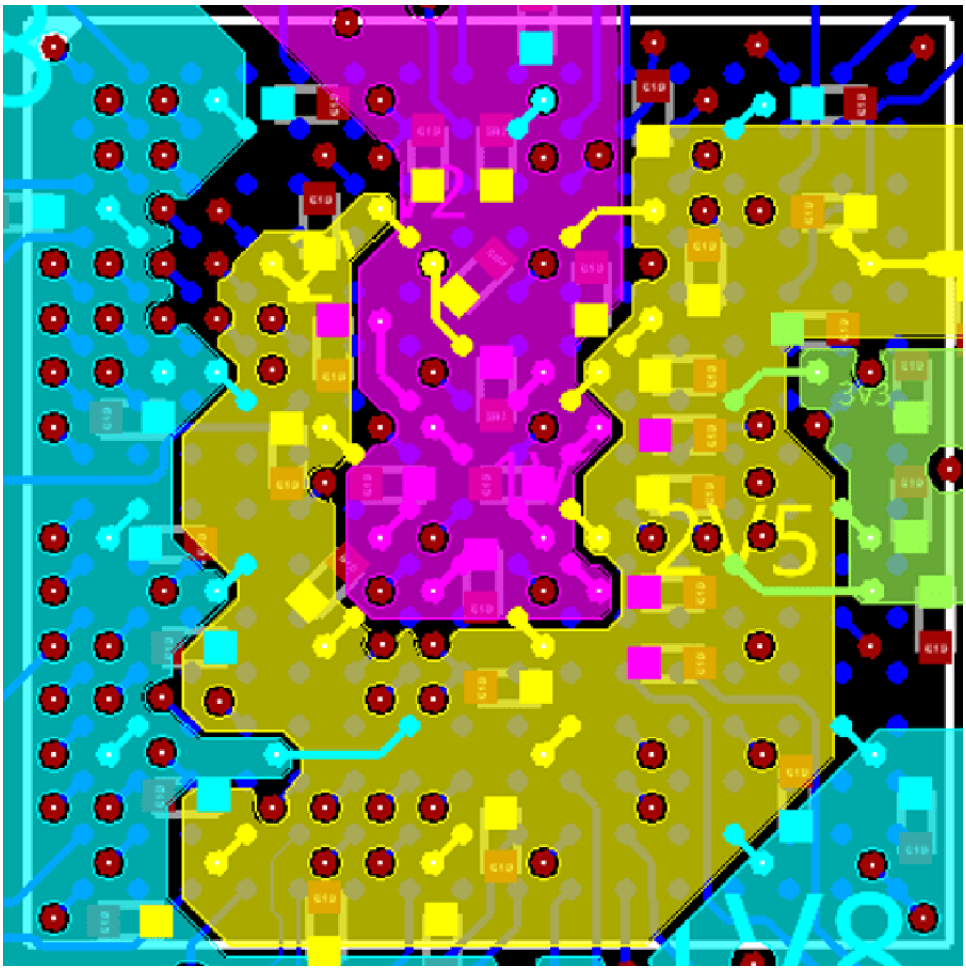

Figure 3. Fan-out optimized for bypass cap placement and avoiding choke points in the power planes. (Credit: Author)

Being prepared to kick off placement. The mechanical outline and stackup should account for all packages involved, as well as the routing and placement keep-out regions. If you don’t want routing below a component type, the footprint should include a route keep-out. I built a route keep-out into every inductor since no one wants routing under there. Some sensors require more clearance than a standard part. That extra space should be incorporated into the virtual part.

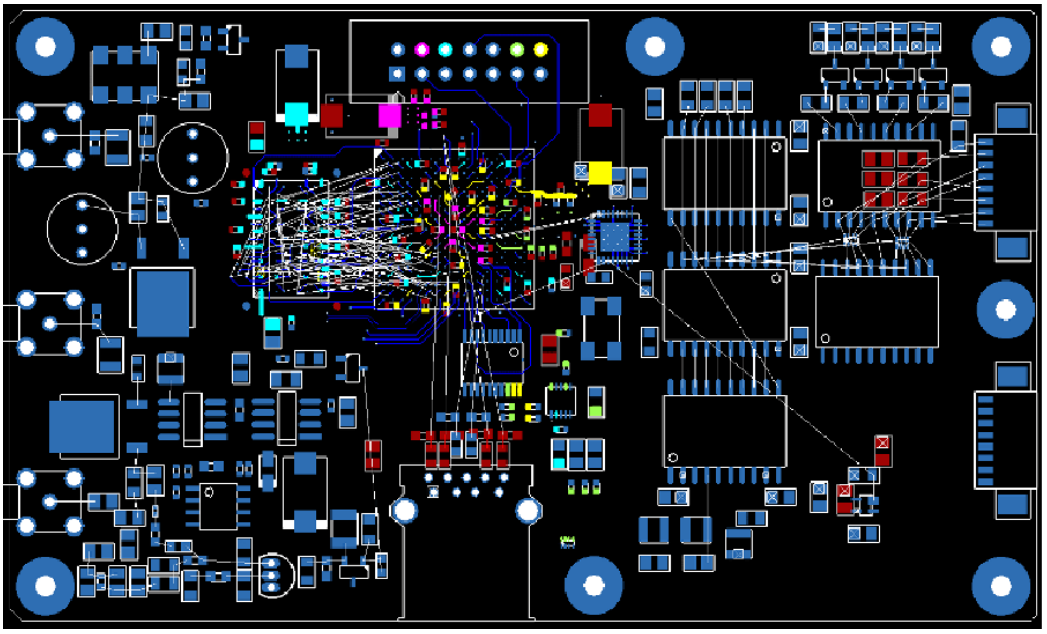

Figure 4. When all was said and done, the board grew horizontally while the technology moved from plated-through-hole to HDI in order to place the DDR memory belly-to-belly. (Credit: Author)

The more absolute rules you can encapsulate, the better. This serves two purposes. It reduces your workload and shows reviewers that you're aware of the constraint and have acted. Keep-ins, keep-outs, headroom limits and other restrictions can be a hassle, but the payoff is a compliant PCBA that fits where it belongs and works as intended.

The design review. Design reviews will be boring for someone with no stake in that part of the process, so the attendee list should reflect that. The mechanical engineer is required to verify that the board outline and all non-electrical features were imported correctly. That's square one. There's no point in inviting the test engineer to that review. Loop them in when you're fairly certain that the test points have optimal coverage. By that point, the ME is out of the picture. Their return could be disruptive.

Certain milestones deserve a design review.

1. Mechanical outline review, including all components, holes and other features covered by the outline drawing. An outline drawing might not yet be available. At a minimum, we compare the layout to the 3-D model to see if everything makes sense. This should involve you and mechanical engineering. After this review, it makes sense to spool up the fabricator so they can provide trace geometry and any other input related to the proposed stackup.
2. Library completion with all components randomly placed outside the board outline. This is you, the EE and maybe copy the project manager. If you're lucky enough to have a dedicated librarian, loop them in.
3. Critical placement with RF chains routed and major ICs in their proposed locations. You, the EE and signal integrity, and at least one of your peers, if possible.
4. Detailed but rough placement with your best effort at fleshing out the power delivery network (PDN). This is a good time to organize your reference designators for the first time. Doing so will make the final push a little

more bearable. You, the EE and power integrity.

5. After fanout of the most complex integrated circuits. You the EE and, again, copy the project manager. The assembly team, whether in-house or contracted, should be included for a placement evaluation. They can advise you on the assembly subpanel and any test coupons, as required. Markup every document shared as **Preliminary**!
6. When memory or other high-speed signals have been connected and length-matched as required. Bring back signal integrity and call on test engineering. The EE should be in the loop daily at this point anyway.
7. Routing of the miscellaneous unnamed traces. You, the EE, your manager and a friend to balance out the power dynamic. After this, your main objective is punching in gratuitous vias for thermal and signal integrity compliance.
8. Full documentation package with all design rule errors squared away. Make a print of every layer and each drawing so there's something to mark up. Invite mechanical engineering, electrical engineering, project management, your manager and the SI/PI team. CC everyone else who contributed to the design effort.

Depending on the design's complexity and nature, some of these may be combined, but it still pays to break the job down into milestones so you can tell whether the project is on track to meet the tape-out date. Waiting until tape-out day to say that the board isn't done could be seen as a failure on your part, particularly if you've been on "radio silence." Keeping on top of the schedule is a part of managing expectations.

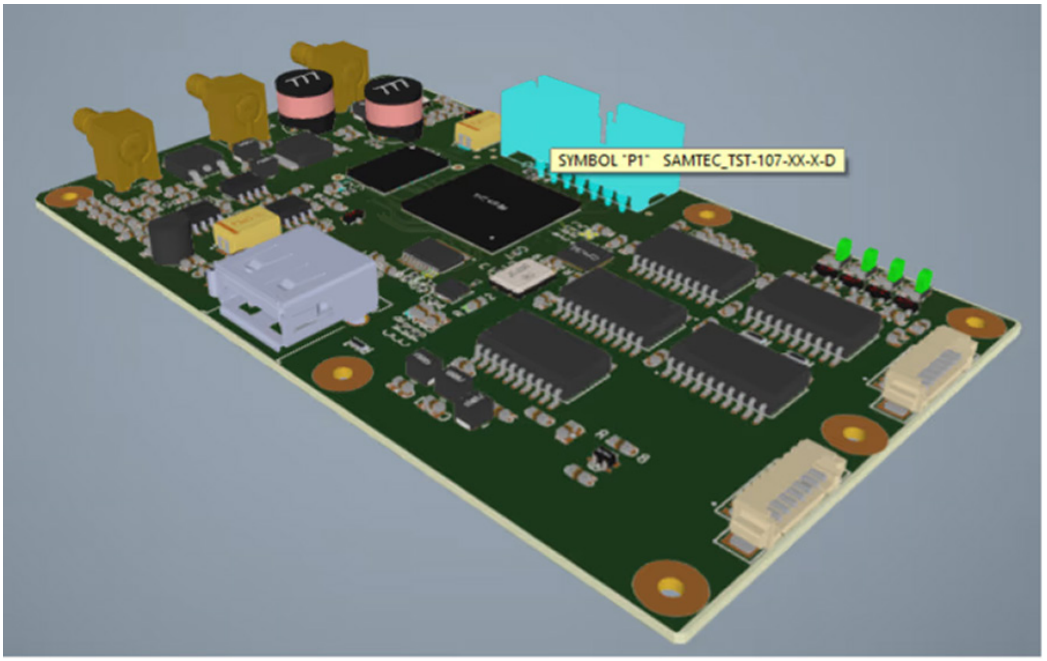

Figure 5. A sanity check after moving the JTAG connector. I will also revisit the inductor between the SMB connectors in the upper corner. (Credit: Author)

The number of touchpoints will vary with each design. Some folks will need a special reminder to make it to the meeting. I remember a signal integrity guy hiding from everyone while using the design review to catch up on his emails. It cuts both ways. Modern times have spread out the workforce, so there are likely to be people phoning it in. Make sure they have a chance to speak and that no one in the room talks over them.

Schedule design reviews as soon as practical. Everyone's calendar fills up by the time they get to work that day. Scheduling these reviews at the start of the layout gives you flexibility to include the people you need, when you need them. This can be done while the schematic is in progress, with the schematic-complete milestone penciled in somewhere along the way. Let's be honest here. The schematic will not be done on the day you start the layout.

When things outside of your control happen, it's the only time you can be forgiven for proposing a whole new set of dates for the follow-on milestones. Product managers are under pressure too. They do not want you to pad the schedule for unforeseen circumstances. We act like everything will fall into place at the right moment, but it doesn't happen often.

Hope for the best while preparing for the inevitable. While Sun Tzu often gets credit for it, Helmuth von Moltke said, "No plan survives contact with the enemy." To be clear, your coworkers are not the enemy, but they do tend to disrupt the best laid plans. As we work with those around us, we learn who is most likely to surface with a last-minute request.

We manage those people the same way we manage an overwhelming concentration of "rats" coming out of an SoC. Ping them early and often. Ask how confident they are in the input provided at any stage. Some people will hold back on giving new information until they are certain that it is the best way forward. They keep their cards close to the vest until they are compelled to share. At the same time, the vendor can't answer questions that weren't asked.

I remember at Qualcomm when we onboarded an engineer on a work visa. She was from Australia and informed us that she received the very last visa issued for that year. I remarked that she was going to fit right in and added that, "If it wasn't for the last minute, nothing would get done around here." It isn't just Qualcomm. It's human nature. It's incumbent upon us to herd those cats to get the job done by the 11th hour, when it all comes together.

JOHN BURKHERT, JR. is a principle PCB designer in retirement. For the past several years, he has been sharing what he has learned for the sake of helping fresh and ambitious PCB designers. The knowledge is passed along through stories and lessons learned from three decades of design, including the most basic one-layer board up to the high-reliability rigid-flex HDI designs for aerospace and military applications. His well-earned free time is spent on a bike, or with a mic doing a karaoke jam.

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The AI Boom is Driving Technological Change at Every Level, Reshaping Supply Chains and Business Strategies

AI investment shows no signs of slowing, prompting concern about what happens when it eventually does.

VICTOR HUANG HAS described ChatGPT's arrival as AI's "iPhone moment," when the technology's potential to change the way we live became clear to all. Indeed, the publication of large language models (LLMs) is arguably the most powerful innovation we have seen so far, enabling widespread user engagement spanning personal and professional purposes. Resulting from this, acceptance has snowballed and more and more of us have come to trust and rely on AI assistants. In turn, mainstream use has driven further improvements, as successive updates have delivered more humanlike interactions and additional capabilities.

Within a short space of time, it seems, an AI-based solution has become available for almost everything. In some of the most contentious examples, AI is giving us original novels, including new works in the style of our favorite authors, and virtual film stars. At the same time, the Albanian government has even put an AI – complete with a traditionally dressed avatar – in charge of its national procurement department. On a more day-to-day level, many of us are discovering how much we need the skills AI can bring to our lives, for finding information on the Internet, organizing our digital content, taking better selfies and fulfilling job responsibilities.

On the one hand, edge AI and tiny machine-learning (ML) applications, while on the other, cloud data centers are where we find the heavy lifting for social media, business applications, and intensive analytics. The AI data center server market has become a huge opportunity for equipment vendors as operators upgrade their data centers to meet the explosion in end-user demand. Already worth almost $300 billion, currently representing 17% of the total server market by value, it's predicted to grow another 20% in 2026.

The effects permeate the entire hardware supply chain, extending to materials needed for chip-packaging substrates and PCBs for high-performance accelerator cards and motherboards. This is advanced, high-end materials technology, including low-CTE quartz glass and ultra-low-profile copper foils needed for high-layer-count boards. The boards are made using advanced techniques such as semiadditive process (SAP) and modified SAP (mSAP) for precise control over circuit dimensions, allowing designers to achieve feature sizes as small as 30μm and traces of 15μm width. Some advanced mSAP and full SAP can achieve even finer features, down to 5-10μm. The opportunities for AI data center equipment present a powerful lure for materials suppliers and fabricators to focus more sharply on high-end products or even realign their businesses away from PCB fabrication and into IC packaging. As AI processors and high-

bandwidth memory drive demand for high-performance substrates, this is a $20 billion slice of the action in a global semiconductor market poised to reach $1 trillion in revenues by 2030.

Attracted by the prospect of greater margins, some suppliers are moving higher up the value chain and out of their traditional markets for conventional standard materials. While not all are following this trend, shortages and price increases are likely for these products as the supply chain adjusts and other companies in different geographic areas take over.

As consumer excitement over AI rises to ever-higher levels, however, signs of dissent are appearing. Doubters question whether the current boom is a bubble that's about to burst. While arguments rage on either side of that debate, we must consider at least one spectacular precedent: the telecom industry of the early 2000s. Some of the industry's biggest and most successful hardware suppliers, which built for what they thought was limitless demand, suddenly found themselves holding vast unsold inventories and were forced to revise their forecasts. Multi-billion-dollar write-downs followed, and key players suffered enormous pain in the stock markets. While some are even now just regaining their pre-boom market valuation, others went bust in the debacle, along with many overhyped dotcoms. We are certainly experiencing a hardware boom today, as data centers invest in new AI servers. In the historical telecom example, spending stopped suddenly due to the dotcom bust as operators stopped spending on hardware and reverted to their normal investment cycle of about 5-10 years, which is the typical lifetime of carrier-grade switches.

Today's top computing companies estimate the lifetime of an AI server at 3-6 years. Investment could slow, although the timing is very difficult to predict accurately. After the telecom bust, a major materials supplier asked me to carry out an analysis to learn whether similar issues in the future could be anticipated and avoided. Notionally, of course, it's easy to predict a fall happening sometime because demand cannot continue rising forever. In reality, dynamic high-tech markets that are constantly creating new services and capabilities have many variables as well as many unknowns. With so many interrelated and abstract factors in play, accurately pinpointing the timing and extent of any downturn is practically impossible.

This time, will we learn the lessons history teaches us? Few can resist the excitement of a boom, and shareholders will always expect executives to follow the money. Right now, data centers are still investing in hardware, and the market is expected to continue growing strongly. Sooner or later, however, every bubble bursts and all will be affected in some way. The industry needs to combine dynamism to make the most of the market highs with the resilience to handle the inevitable lows.

ALUN MORGAN is technology ambassador at Ventec International Group (venteclaminates.com); alun.morgan@ventec-europe.com. His column runs monthly.

"An investment in knowledge pays the best interest."

-Benjamin Franklin

noted entrepreneur,
yep, rich too...
hippie hair. hmm--

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BOARD **TALK**

Metal-Core PCBs and Thermal Management

Catch heat at the board before it turns into a full-time job.

HEAT SNEAKS UP fast in today's electronics. Higher power density, smaller form factors and long-life reliability expectations all collide, requiring better thermal design. The teams that come out on top with this challenge are the ones who solve heat at the PCB level rather than trying to fix it later with a bigger heat sink or more airflow.

PCB products designed for this level of thermal management generally fall into two categories. The first is metal-base, often called IMS or insulated metal substrate. The second is metal-core. In both variations, the technology turns the familiar idea of a printed circuit board into an active part of the thermal system, rather than expecting FR-4 to carry the load. FR-4 is an excellent structural and electrical material, but it is not a thermal material.

IMS and metal-core types are often referred to interchangeably, and while they share many common traits, there are a few distinct differences worth understanding before choosing one over the other. With MC PCBs, for instance, the heat has a direct path into a metal substrate, such as aluminum or copper. This puts the thermal solution right beneath the components that generate the temperature rise. By permitting the PCB to act as a direct heat distributor, designs become more compact, more predictable, and often lower cost overall. It also buys a lot of reliability margin, especially in LED lighting, power electronics and automotive systems, where junction temperature directly translates to product life.

The fundamental advantage of a metal-base PCB comes down to thermal conductivity. FR-4 stays around 0.3 – 0.5W/m·K, which is enough for structural integrity and electrical insulation, but not for heat. Aluminum substrates typically offer 1 – 4W/m·K, while copper can reach anywhere from 3 to around 14W/m·K, depending on the grade and the dielectrics paired with it **(Figure 1)**.

Material	W/mK	Comment	Thermal conductivity	Availability	Price
Standard FR4	0.2-0.6	Benchmark - Epoxy resin woven glass system	LOW MEDIUM HIGH	LOW MEDIUM HIGH	LOW MEDIUM HIGH
Shengyi ST110G	1.0	Epoxy resin woven glass system – Suitable for multilayer, thick copper, high voltage applications. Not common.	LOW MEDIUM HIGH	LOW MEDIUM HIGH	LOW MEDIUM HIGH
Shengyi ST115G	1.6	High CTI, Tg170°C, suitable for power, automobile and LED product, can be used for HDI and high layer count. **Recommended.**	LOW MEDIUM HIGH	LOW MEDIUM HIGH	LOW MEDIUM HIGH
~~Rogers 92ML~~	2.0 (average)	Epoxy resin woven glass system – Suitable for Power and Industrial control applications. Multilayer use. It is out of market since March 8, 2023.	LOW MEDIUM HIGH	LOW MEDIUM HIGH	LOW MEDIUM HIGH
Ventec VT-5A2	2.2	Ceramic filled epoxy resin woven glass – Suitable for Power and Industrial control applications. Multilayer use.	LOW MEDIUM HIGH	LOW MEDIUM HIGH	LOW MEDIUM HIGH
Rogers TC350 series	0.72 – 1.24	Ceramic filled PTFE-based woven glass reinforced - RF application, Antenna, Power amplifier, Passive device.	LOW MEDIUM HIGH	LOW MEDIUM HIGH	LOW MEDIUM HIGH
Rogers TC600	1.1	Ceramic filled PTFE-based woven glass reinforced - RF application, Antenna, Power amplifier, Passive device.	LOW MEDIUM HIGH	LOW MEDIUM HIGH	LOW MEDIUM HIGH
Rogers Curamik	24 / 90 / 170	Aluminium Oxide / Silicon Nitride / Aluminium Nitride ceramic substrates. Very high current (wind/power/rail). 1-2L. Rogers currently supply to selected customers only	LOW MEDIUM HIGH	LOW MEDIUM HIGH	LOW MEDIUM HIGH

Figure 1. Thermal characteristics of some printed circuit materials.

When a copper circuitry layer is bonded to a thermally conductive dielectric over a metal-base, heat flows vertically, not just laterally **(Figure 2)**. It travels from component pads into copper and then directly into the plate of the metal that can be bolted to a chassis. The improvements are noticeable: lower junction temperatures, increased stability under load and the ability to maintain performance in harsh environments. There is a reason LED manufacturers embraced aluminum-base PCBs early: without them, failures due to thermal stress would be a major issue.

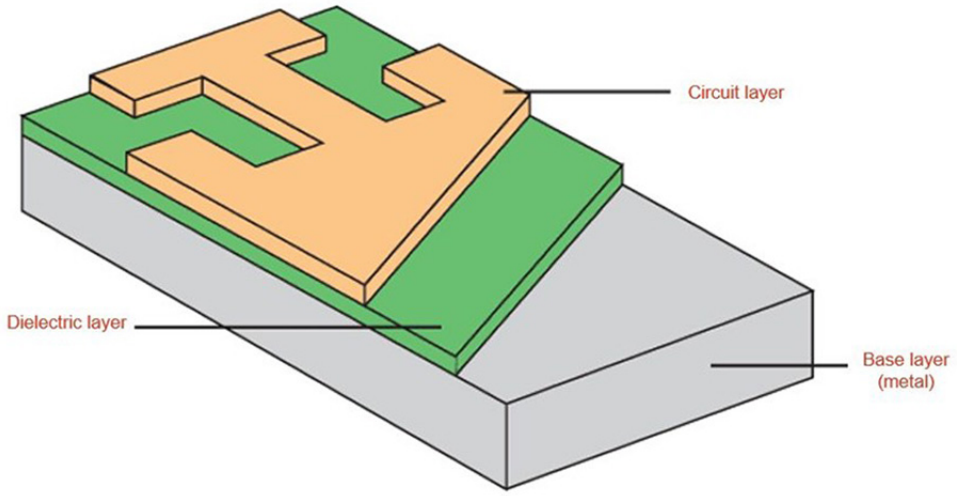

Figure 2. Representation of a metal-base PCB construction.

Aluminum is the most common choice because it is affordable, lightweight and of sufficient quality for the majority of moderate-power applications. Copper is used when designs push into demanding current density, tight packaging, or high shock and vibration. The big differentiator between the two is not just thermal conductivity but manufacturability. Copper can survive drill and plating operations, which means it supports plated through-holes and even multilayer routing. Aluminum simply can't handle the thermal stress of plated through-hole (PTH) fabrication without compromising reliability. Therefore, when a metal-base PCB with more than one routing layer or interconnects passing through the structure is needed, copper is where the design usually ends up.

The simplest and most cost-effective metal-base designs are single-sided **(Figure 3)**. All components sit on one surface

directly above the metal plate, and heat flows straight downward with almost nothing to get in the way. You still have copper planes to help spread heat laterally, but the real value comes from the short, direct conduction path to the base.

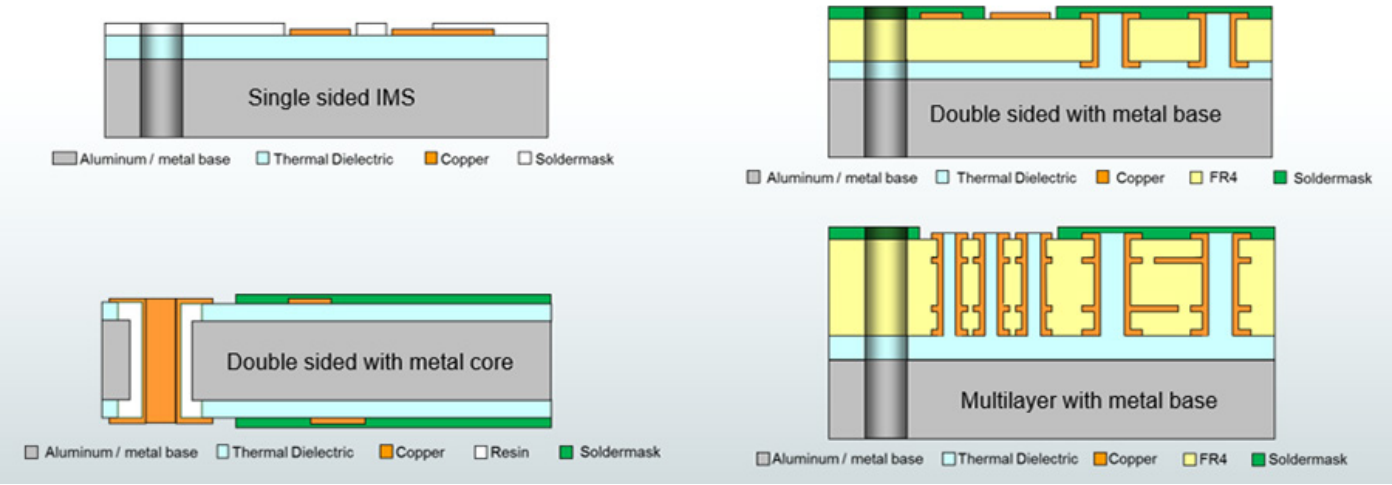

Figure 3. Examples of IMS builds.

There are plenty of situations, however, where that routing simplicity isn't enough. Power conversion is a great example. You may have to bring signals around the board or support more elaborate circuitry. In those cases, the construction changes from aluminum-based designs to copper-core builds.

Once a copper core is introduced, plated through holes become a reliable option. Those vias can be intentionally tied into the metal-core when the goal is to spread heat more broadly, or they can be electrically isolated from the core when the design requires the interconnect to remain independent. This flexibility permits metal-base solutions to stretch into multilayer territory without giving up their thermal advantage.

As power devices shrink and technologies like GaN and SiC push current density through the roof, thermal engineering must evolve with them. Many modern designs are incorporating high-density interconnect (HDI) features into metal-base structures, such as laser-drilled microvias and thinner dielectrics that place heat-conduction paths closer to the active junction.

Another technique that is becoming standard in demanding power modules is the use of copper pedestals **(Figure 4)**. A solid slug of copper is positioned directly beneath a hotspot, almost acting as a direct bridge to the metal foundation. The result is a dramatic reduction in thermal resistance for devices like IGBTs, Mosfets and high-power LEDs. This is the approach taken when even a small increase in junction temperature would cause performance degradation or shorten service life.

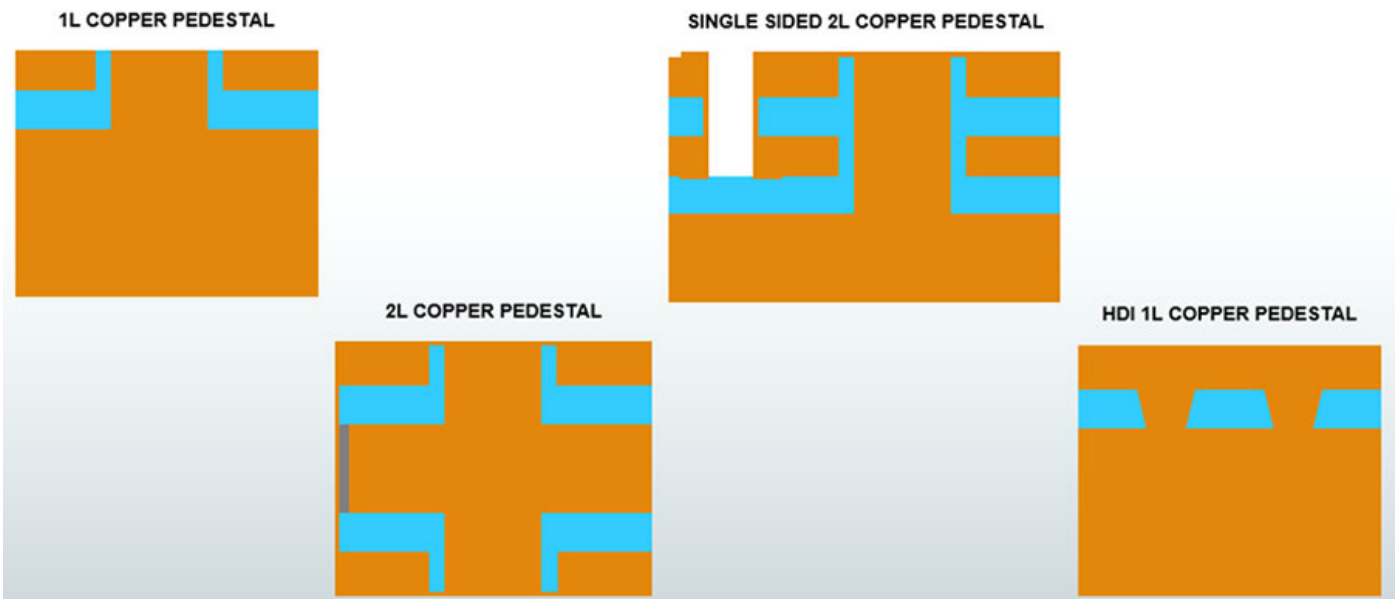

Figure 4. Copper pedestals involve a solid slug of copper positioned directly beneath a hotspot to reduce thermal resistance.

A misconception is that metal-base PCBs automatically represent a premium cost solution. In many cases, the opposite is true. When the PCB takes responsibility for heat spreading, other thermal hardware becomes unnecessary or can be reduced. Instead of installing oversized heatsinks or stacking up thermal interface materials, the heat goes directly into the chassis, with fewer components in the way. That cuts assembly cost and weight. These factors matter more than ever today.

Copper-core multilayers still sit at the higher end of the price spectrum, and aluminum-base single-sided designs are typically an affordable step above FR-4. The key is evaluating them not in isolation but against the total system cost. In many applications, the ROI isn't just measurable, it's immediate.

Metal-base PCBs are a powerful tool for power and thermal engineers when heat must be managed at the source. They keep designs smaller, improve reliability and solve thermal problems early and efficiently. They also give mechanical teams more freedom because less bulky cooling hardware means more room to innovate and more confidence that temperature won't be the weak link.

They don't eliminate the need for fans, heatsinks or proper airflow design. But they make each of those strategies more effective because the PCB is no longer simply a structural element. It becomes one of the primary heat-handling features of the entire assembly.

When the stakes are thermal, and they always are, starting the solution on the board is often the smartest move you can make.

JEFFREY BEAUCHAMP is director of technology & engineering at NCAB Group USA (ncabgroup.com); jeffreybeauchamp@ncabgroup.com. He started his career in the PCB industry in 2003 at PD Circuit, now part of NCAB Group, and works with PCB customers to provide optimal solutions. His column runs quarterly.

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The PCB Podcast

DATA TRANSFER

Bidirectional Design Data Exchange and Technical Query Management with IPC-2581

How the industry standard revolutionizes PCB collaboration.

LAST MONTH'S COLUMN talked about a simpler way to exchange stackups with manufacturing partners. This month, continuing the theme of migrating from handoffs to bidirectional design data exchange, we will talk about electronic exchange of technical queries with design/manufacturing partners through IPC-2581's DfX module. The module may be included within the design data or exist independently, such as a stackup exchange module that can be shared separately.

In the AI age, why does anyone need this? There is a smarter, better way to exchange technical queries – by using IPC-2581 DFM exchange module. Adopting IPC-2581's DFx module transforms the way PCB designers and manufacturing engineers collaborate, replacing manual, error-prone processes with streamlined, electronic communication. This approach accelerates new product introduction, reduces mistakes and enables both sides to track and learn from every exchange. By making technical queries (TQs) and DfM feedback easy to send, review and act on, IPC-2581 creates a win-win environment for design and manufacturing teams.

Let's examine how technical query data is shared between designers and manufacturers. Then we will review how the same process of exchanging TQs will work with IPC-2581.

Current Design Data Handoff and TQ Exchange

Traditional handoff packages are fundamentally one-way exchanges. Instead of true bidirectional communication, design data are simply handed over, then reverse-engineered by manufacturing partners: Gerber files require full reverse engineering **(Figure 1)**, while ODB++ files are partially reconstructed. After this laborious process, the data undergo DfM analysis, which almost always uncovers issues:

- Mismatches between Gerber and fabrication drawings
- Manufacturing data inconsistencies
- Outright DfM errors.

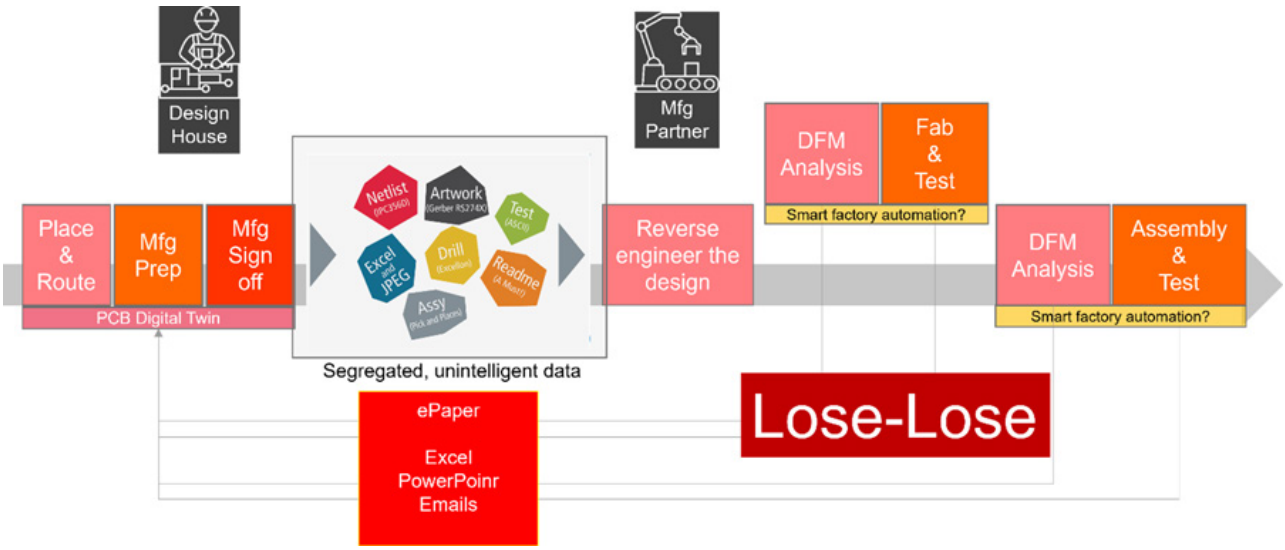


Figure 1. Traditional handoffs and ePaper-based communication are a lose-lose scenario for the designer and manufacturing partners.

These findings are then relayed back to the designer using ePaper methods – emails, Word documents, PowerPoint slides – tracked manually in spreadsheets. Each ePaper document references specific design structures, coordinates and embedded images to help layout and manufacturing engineers understand the context. This manual correlation is not only tedious; it is entirely unnecessary in today's AI-driven era. Why can't tools talk to each other? Why do tools require layout designers to perform nonproductive correlation work that can be completely avoided? PCB designers must be free to perform real layout work.

Manufacturing partners often ask for variance of some rules, chamfering of pads, etc. to improve yields. These variance requests are also sent through ePaper. The approval/disapproval process is through ePaper, and the designer and their manufacturing partners must track these exchanges through emails, spreadsheets, etc. The layout designer manually matches the request's context, and the pre-CAM process engineer must also ensure the responses correspond appropriately. Any mistake made by either party is costly to both in terms of time lost and wasted materials. Why follow a process that was invented in the 1960s?

IPC-2581 stands out as the only true bidirectional standard, sidestepping the drawbacks of traditional one-way handoffs. IPC-2581 revision C introduced the DfX module, which permits electronic exchange of DfM data and TQs. This module can either accompany the complete set of design data or be distributed on its own, in a manner similar to stackup information.

The latest IPC-2581 release (version 4.0) enhances the DfX module capabilities, thanks to feedback from IPC2581 Consortium and IPC 2-16 committee members. By adopting the DfX Module, designers and manufacturers can finally eliminate ePaper – no more emails, Word docs or PowerPoint slides – saving time and reducing errors **(Figure 2)**. Better, the contextual data exchanged can be analyzed by AI agents to recommend process improvements and minimize unnecessary iterations. Design teams can compare changes across sources, while manufacturers can pinpoint which customers consume the most time, and incent better collaboration. This streamlined process accelerates new product introduction and creates a genuine win-win for everyone involved.

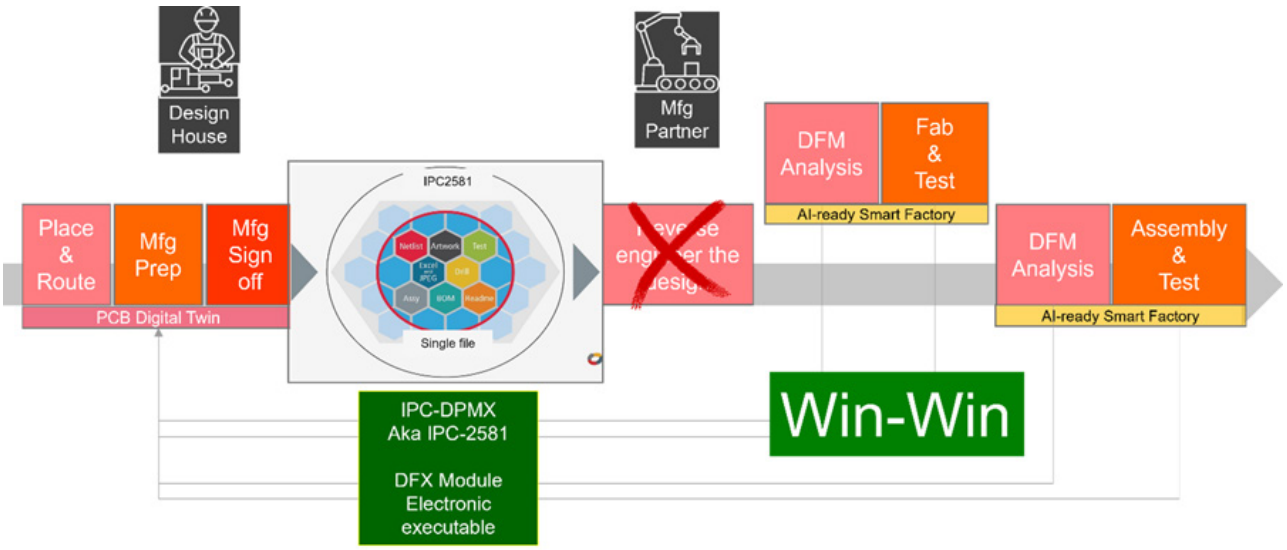


Figure 2. IPC-2581 DfX module queries are sent electronically, understood by the tools on both sides, eliminating manual error-prone ePaper-based communication to accelerate NPI.

What the DfX Module Contains

The module enables seamless, bidirectional communication of technical queries and error reports in an intelligent electronic format, easily interpreted by both design and manufacturing tools. This modern approach replaces the outdated, error-prone ePaper methods of the past.

Within a single DfX module, multiple queries can be included for a given board, ranging from requests for clarification to DfM errors to variance requests on specific design elements. These queries can address a wide spectrum of topics, such as components, assembly, fabrication, stackup, testing, quality, mechanical aspects, materials or footprints. Each query provides detailed information, permitting tools to precisely identify the referenced element. For DfM violations, the module can specify the measurement criteria used in DfX analysis and list any measurements that fall outside the defined standards.

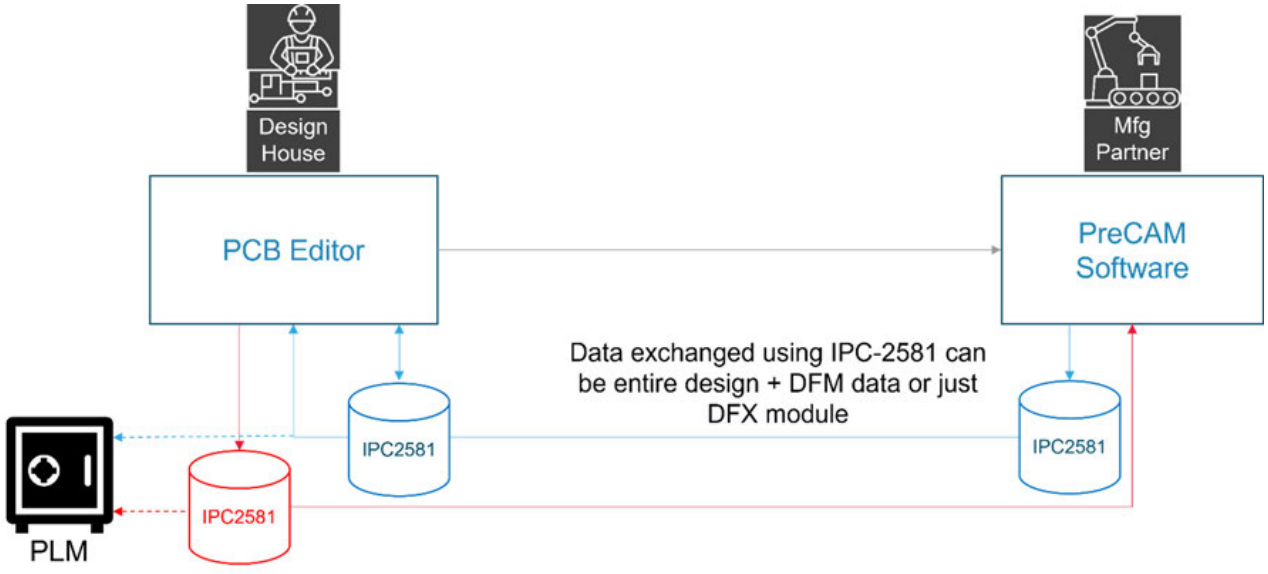


Figure 3. Data flow using IPC-2581 DfX module.

The DfX module also supports communication about conflicts, such as discrepancies between fabrication spec notes attached to elements in the design and reference specifications, or mismatches in drill counts. Each query is linked directly to the design data, enabling tools to cross-reference, zoom in and highlight the relevant elements. External references, such as URLs or files, can be included, and additional items like images, documents, firmware or executables can be embedded in a base64 format.

The DfX Module allows both sides to go back and forth with comments, approvals and rejections.

- Manufacturer (fabricator, assembler) and designer can use their specific viewing formats while sending the information in a neutral format
- Fabricators can eliminate customer-specific TQ formats
- Product engineers can standardize on a common GUI
- Approved DfM can be electronically stored within the IPC-2581 file rather than on an engineer's disk drive or other database. These data can be stored in the company's PLM system for streamlined management.

Examples of TQs through DfX Module

Below are some examples of technical queries between design and manufacturing.

Example 1: Query on silkscreen on opening area.

- "Per data file, some silkscreen overlapped onto opening area. We would like to move legend aside if room is available, otherwise we can clip them away from opening."
    - Image attached
- Response
    - "Do not move silkscreen. Clip all silkscreen over solderable surfaces and over holes."

Example 2: Request – add dummy pad.

- Recommended thieving-1
- Unbalanced copper
- Measurement point – layer reference, location x, y
- Marker location and dimension
- Description
    - "We can add thieving on internal layers except area of 14a. Thieving pad 50 mil squares spaced on

80 mil centers and keep 130 mil clearance from pattern on adjacent signal layer, no effect for impedance control."

- Response
    - Approved / rejected

Example 3: (from assembler) – Component height analysis.

- Bottom side wave spacing-1
- Location
    - Layer reference
    - X, y
- BoM reference
    - C138, C140, C187, C186, C29, C171
- Description
    - "Current heights are 228-531mil, DFM spec is 200mil max in bottom side for wave solder fixture design. Please check and move them to top side."
- Response
    - Rejected
    - Comment: "This board will be processed as paste in hole."

Benefits of Bidirectional Data Exchange with IPC-2581 DfX Module

The module accelerates NPI, creating a win-win for both design teams and manufacturing partners.

For the design team:

- Saves review time for technical questions or DfM errors.
- Returns DfM errors electronically. No more ePaper (PowerPoint, spreadsheets, etc.).
- Direct links from errors to specific design elements make troubleshooting fast and accurate.

- Tracks every feedback and decision, so it is apparent exactly what was done, by whom and why.
- Eliminates manual data entry or interpretation from emails or documents.

For the manufacturer:

- Sends errors and feedback electronically, eliminating need for generating reports in different formats for different customers.
- Easily tracks which errors are fixed, waived or ignored for each design.
- Know who approved, rejected a request and why.
- Metrics are simple to follow over time, whether by customer or by design type.

For both sides:

- Shared metrics over time reveal insights that are hard to see with manual processes.

Conclusion

Embracing the IPC-2581 DFX module revolutionizes collaboration between PCB designers and manufacturing engineers by shifting from manual, error-prone workflows to efficient, electronic communication. This streamlined process speeds up the new product introduction, minimizes errors and allows both teams to monitor and learn from every interaction. By simplifying the exchange, review and resolution of technical queries and DfM feedback, IPC-2581 fosters a mutually beneficial environment for the design and manufacturing teams.

HEMANT SHAH is an EDA veteran and chair of the IPC-2581 Consortium (ipc2581.com). Shah led the effort to create an industry-wide consortium of design and supply chain companies to get IPC-2581 – the standard for transferring PCB design data to manufacturing – adopted.

He spent 20 years at Cadence as product manager for various PCB design products. Shah also led the industry adoption of the IBIS-AMI algorithmic modeling standard. Prior to joining Cadence, Shah worked at Xynetix and Intergraph. He is passionate about developing and marketing leading-edge software products for PCB design.

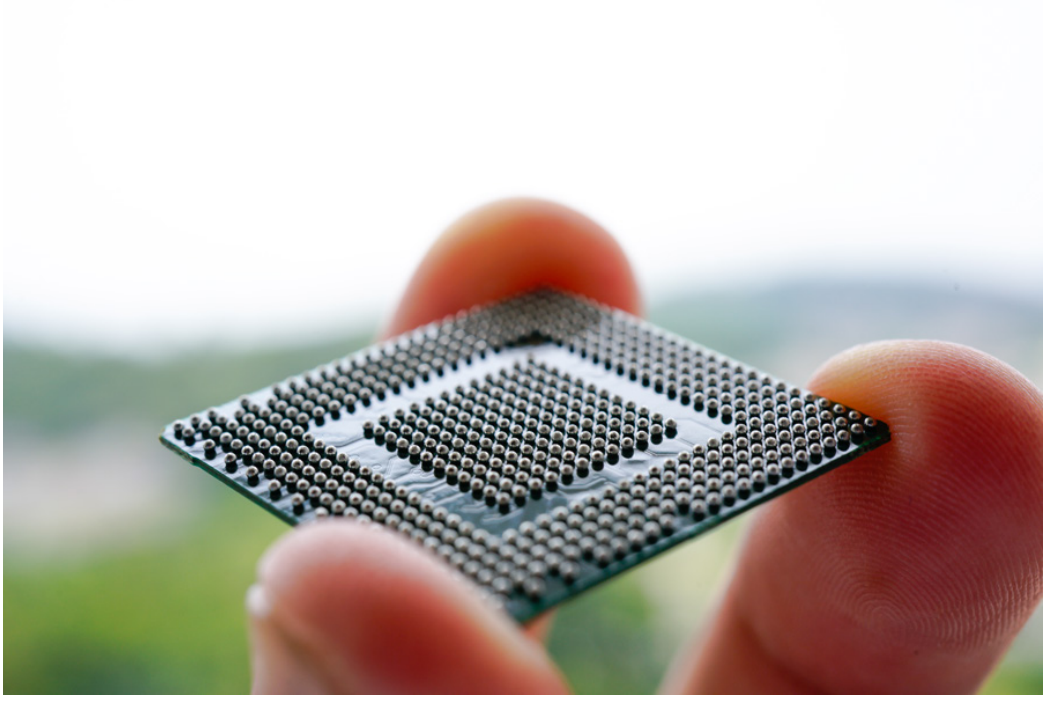
UHDI **FOUNDATIONS**

Ultra HDI: What is It and How is It Different than HDI?

With ultra-high-density interconnect design, small features come with big decisions.

by ANAYA VARDYA

Ultra HDI (UHDI) has become a prominent part of the PCB design conversation, often presented as "the next frontier" in density and miniaturization. But before we move on to advanced routing strategies and design techniques, let's establish a solid practical foundation. What is the difference between UHDI and the HDI processes, which so many designers have already learned to rely on? Why does the shift in the underlying process matter, and when does it become worth incorporating into mainstream design work? We will address those questions here.



What Ultra HDI Actually Means

Most designers are well-acquainted with traditional HDI: laser-drilled microvias, 3–4 mil line/space and the lamination cycles required to build stacked or staggered microvia structures. For many years, this combination carried us comfortably through 0.8mm and 0.65mm pitch devices, meeting the rising expectations of high-speed digital architectures.

UHDI pushes those boundaries further: not only with smaller geometries, but with fundamentally different processes

to manufacture this technology. While definitions vary slightly among fabricators, UHDI HDI generally refers to:

- Line/space below 65µm.
- Very small capture pad and land sizes suitable for next-generation device pitches
- Tighter copper thickness control, which makes for more predictable electrical behavior
- Imaging methods that can continuously maintain such features in a semi-additive way.

In other words, UHDI is not simply "smaller HDI" but rather a different approach to manufacturing the copper structures themselves. The difference becomes particularly important when a design involves very fine-pitch BGAs, dense routing channels, or demanding RF and high-speed nets.

Why the Manufacturing Process Matters More Than It Used To

Conventional HDI is based on subtractive-etch processing. The process starts with copper foil laminated to the dielectric. Resist protects areas that are intended to become traces or pads, and exposed copper is chemically etched away. This works extremely well, up to a point. As trace widths shrink, several issues become more pronounced:

- Undercut becomes harder to control; traces may narrow beyond what is wanted.
- Sidewalls taper, forming a trapezoidal cross-section.
- The final copper geometry may vary more from panel to panel than designers would like, especially for critical impedance nets.

These limitations begin to compete directly with electrical performance requirements as feature sizes fall below 75µm.

Semi-additive processes (SAP) approach the problem from the opposite direction. Rather than removing copper, they add to build it up. That process is as follows:

- Use a very thin seed layer or ultra-thin copper foils rather than full-thickness foil.
- Image the areas in which copper should be deposited.
- Plate copper onto the defined regions.
- The remaining seed layer or ultra-thin copper foil is removed in a controlled flash etch.

These traces have more vertical sidewalls and a more consistent geometry, which directly translates into tighter impedance control, reduced loss, and more predictable routing density. In UHDI features, geometry is not just a manufacturing outcome; it becomes a key enabling characteristic.

This is why UHDI requires designers and fabricators to work even more closely together. The imaging method influences what line/space can be reliably achieved, which in turn affects routing strategies, stackup planning, and the overall architecture of the board.

When to Consider UHDI

Not every design requires UHDI. Using it in situations where it is not required might add unnecessary cost. A number of design conditions start to indicate that it may be the correct choice, however.

1. **Device pitch and breakout constraints.** BGA pitch often becomes the first clear indicator. Traditional HDI is good at 0.8mm and 0.65mm and can often achieve 0.5mm with careful routing strategies. However, as devices move closer to the threshold of 0.5mm, and especially below, fanout becomes increasingly constrained. Via escape patterns and routing channels rapidly consume available space, and layer count begins to rise. Subassembly strategy for complex microvia and buried/blind microvias is often used, driving cost and lead times higher.
2. **Size, weight and power (SWaP) requirements.** Miniaturization pressure is playing an increasing role across the board, from wearables and medical devices to aerospace and advanced industrial electronics. UHDI enables routing density to make meaningful reductions in layer count and board area feasible.

   Examples include reducing a 10-layer design to six or eight layers by opening additional routing channels, lowering overall thickness while maintaining electrical performance and improving component placement options through cleaner breakout geometry. This is where the SWaP benefits become tangible: the value of UHDI is not just about small traces but also architectural decisions that can be made with this technology to reduce size and complexity in the complete assembly.

3. **RF integrity and high-speed signaling.** In RF or high-speed designs, the geometry of copper directly impacts insertion loss, impedance stability and signal isolation. The smooth, consistent copper features afforded by semi-additive processes can help minimize the variability in nets operating within narrow margins and UHDI geometries have provided the required discipline for maintaining consistent electrical performance across production lots. This benefit applies to traces greater than 75µm as well as to hold linewidths to very tight limits.
4. **Balancing cost and reliability.** Moving to UHDI may affect the cost structure: more sophisticated imaging methods and tighter controls generally raise the cost per panel. The broader cost picture is more complex.

   Total cost often balances out with UHDI because designs can use fewer layers, smaller board sizes, more efficient assembly through simplified breakout, greater flexibility in component placement and more stable impedance performance without relying on exotic or high-cost materials.

   Reliability considerations can be mitigated with UHDI: denser via structures and smaller capture pads require careful attention to aspect ratios, thermal management, and the use of stacking strategies that minimize stacking.

   Semi-additive geometries have improved consistency compared to traditional HDI, which reduces some of the variability.

Early collaboration with an experienced fabricator does make a difference. The process window for UHDI is different, and knowing where that window is most robust will guide better design decisions.

Key Design Implications

Once UHDI rules are in place, several design areas deserve early focus.

1. **Line/space usage.** UHDI does not mean applying minimums throughout the design. The most successful designs use fine features in selected, strategic areas such as the BGA fanout region and other crowded areas, and relax the rules in open spaces where it is possible. This approach is much better to maximize yield and contain cost without sacrificing routing efficiency. Keeping the finest lines on specific layers helps cost by allowing for the mix of technologies. Subtractive etch may be used on power/ground layers and signal layers of 75µm or greater.
2. **Stackup planning.** Layer reduction thus becomes a practical possibility, and the stackup often differs from traditional HDI designs. In many designs, Ultra HDI will permit more efficient routing channels, more flexibility in placing planes, and better control over impedance structures.
3. **Impedance accuracy.** Because the copper thickness and geometry in semi-additive traces are more predictable, impedance calculations become more reliable, especially for designs with very small structures or pushing the limits of high-speed performance. Use of actual fabricator process data within modeling tools is critical; this ensures simulations reflect real manufacturing outcomes.
4. **Data packaging clarity.** Fabricators may want to understand in more detail which features are needed and where the design rules can be relaxed. Clearly identifying the critical nets, functional regions and constraints aids in helping the fabricator optimize yield and manufacturability without sacrificing performance.

Where This Leads

Ultra HDI is much more than a set of smaller numbers on a capability chart. It introduces a process that supports tighter geometry, higher routing efficiency and improved electrical performance, provided that the design, stackup and manufacturing assumptions are aligned from the start.

The bottom line: the value of UHDI comes from making smart, informed decisions upfront. When process capabilities, routing strategy and electrical performance are all in concert with one another, designers have options, not limitations.

With the next article, we can move from foundational concepts to practice, looking at design for manufacturing considerations.

ANAYA VARDYA is chief executive of American Standard Circuits/Sunstone (asc-i.com); anaya@asc-i.com.

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STACKUP **ESSENTIALS**

The Critical Nature of PCB Stackup, and How to Build an Efficient One

Like a building foundation, the stackup supports every layer above it.

by AKBER ROY

The way the printed circuit board layers shown in **Figure 1** are arranged is called a stackup. It's one of the most important constructs in a PCB design. In many ways, it's configured just like the foundation of a building. If the stackup is weak or poorly planned, for example, everything built on it will suffer from instability, no matter how good the circuit design is.

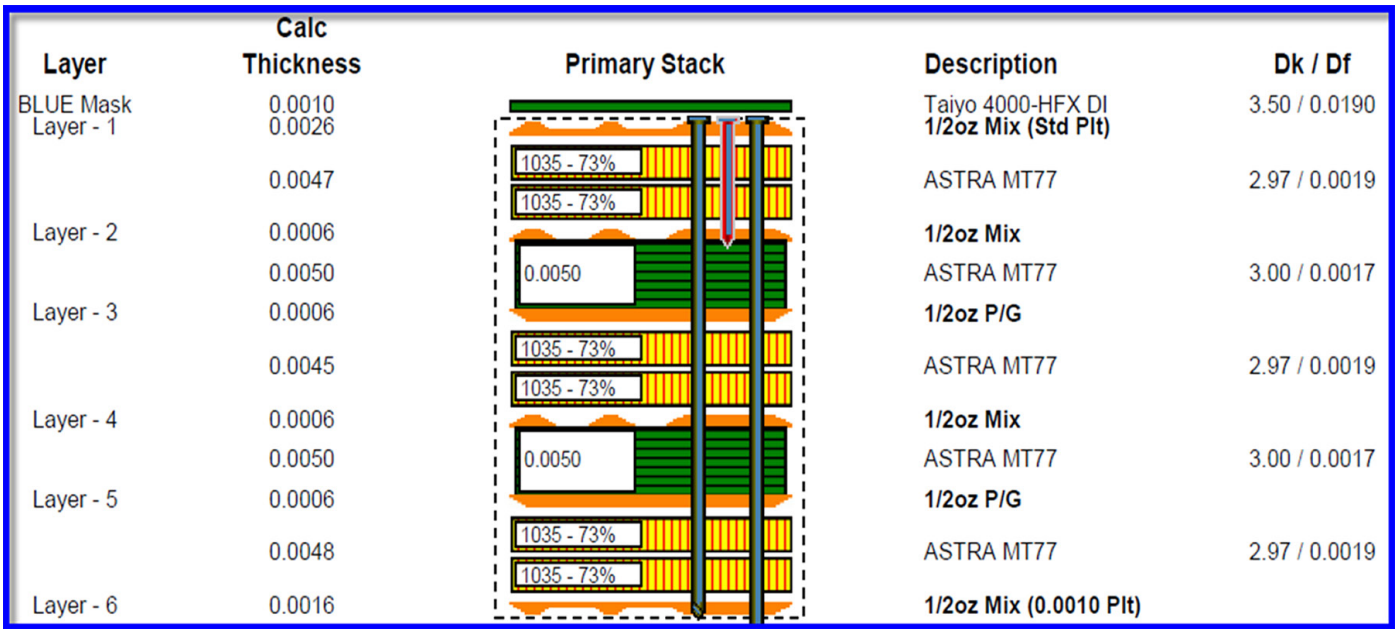

Figure 1. Example of a PCB stackup.

Why the PCB Stackup Matters

As noted, proper circuit design can be undone by a poorly planned stackup. Here are some ways to think of how the board is constructed and the effects of a thoughtful approach.

Signal integrity (SI). Imagine shouting in a tunnel; your voice echoes and distorts. Poor stackup has the same effect on high-speed signals. A good stackup makes signals travel smoothly, with controlled "lanes" (impedance) and solid "walls" (ground planes) to keep them clean.

Electromagnetic compatibility (EMC). Have you ever held your phone next to a speaker and heard a buzzing sound? The source of that is known as interference. A proper stackup reduces unwanted "noise radiation" by keeping signal return paths close to ground planes.

Thermal and mechanical reliability. Think of a sandwich where one slice of bread is thick, and the other is paper-thin – it bends easily. A PCB works the same way. Symmetrical and balanced stackups prevent warping and help distribute heat evenly.

Prototype perspective. When you build the first prototype, the stackup is like your test recipe. You are evaluating several things:

- Can the fabricator achieve the planned impedance values?
- Do thin dielectrics really work for your signals?
- Does the board survive lamination without warping?

If the stackup isn't right in the prototype, production will only multiply the problems.

Fine-pitch parts. Modern chips often come in BGA packages with very small pin pitch and edge-to-edge spaces (as small as 0.4mm (about 0.02″) between pads). Escaping traces from these packages is like parking cars in a narrow alley. You need slim lanes (fine traces), smaller drills and sometimes "underground tunnels" (blind or buried vias). The stackup determines whether that's even possible.

DfM (design for manufacturability). Think of DfM as designing not just for your idea, but also for the factory. Even if your design works on paper, can it be built repeatedly, reliably and at a reasonable cost? For example, if you choose exotic materials not available locally, your project may get delayed. If you stack too many microvias, yields may drop, and costs could skyrocket. A DfM-friendly stackup balances performance with manufacturability.

Steps to Build an Efficient Stackup File

To build an efficient stackup file, follow this process:

Step 1: Define the requirements. The first step is to define what the circuit actually needs. High-speed interfaces such as USB 3.0 or DDR require controlled impedance, while power-dense components call for thicker copper to carry higher current. If the design includes fine-pitch BGAs, thin dielectrics become necessary to enable proper breakout. For example, a board using DDR4 memory typically requires planning for 50Ω single-ended traces and 100Ω differential pairs within the stack-up.

Step 2: Select the materials. Different dielectrics behave much like different types of road surfaces: some offer smooth, low-loss "highways," while others resemble rough, high-loss dirt roads. The choice depends on how fast the signals need to travel. Standard FR-4 is suitable for many designs, but for 5G, RF or other high-frequency applications, low-loss materials are often required.

Step 3: Plan layer arrangement. Planning a stackup is a lot like planning a city. Signals should travel alongside solid "ground highways" to ensure clean return paths. Power and ground layers belong close together, much like stacking the meat and cheese in a sandwich, to support stable power delivery. And keeping the structure symmetrical helps prevent bending as the board is manufactured.

Example of an 8-layer structure:

- L1: Signal
- L2: Ground
- L3: Signal
- L4: Power
- L5: Power
- L6: Signal
- L7: Ground
- L8: Signal

Step 4: Set dielectric thickness and copper weight. Dielectric thickness acts like the distance between traffic lanes; too wide, you lose control over impedance; too narrow, the board becomes difficult to manufacture. Copper weight works the same way: it's essentially the width of the lane. Thicker copper can carry more current, but it also makes fine routing significantly harder. That's why, in a BGA breakout, designers often choose 0.5oz. copper with 3-mil traces rather than 2oz. copper, which is simply too thick for that level of detail.

Step 5: Run impedance calculations. This is like checking lane width before painting road lines. Tools or fab calculators will tell you what trace width/spacing gives 50Ω or 100Ω. For example, if your fabricator says "with 3 mil dielectric, 4 mil trace = 50Ω", that defines your PCB rules.

Step 6: Verify with fabricator (DfM check). Once the draft stackup is complete, confirm with the fabricator whether the "recipe" is actually manufacturable. They'll determine whether the planned via sizes can be drilled reliably, whether the stack can be pressed without bow or warp, and whether the specified materials are available and supported in their process.

Step 7: Finalize and document. Once everything is validated, create a clear table that lists each layer's name and function, the dielectric thickness and type (including Dk/Df), copper thickness, target impedances and any special notes such as "VIPPO for BGA pads." This table becomes the blueprint that guides both your design team and the fabricator through the build.

Lyr	Layer	Image	Foil Wt	Cu Thk	Thk	Dk	Description
SMT					0.70		
L1	Sig		1/2oz	1.9			Foil 0.5 oz
					3.86	3.12	PREPREG Megtron7(N) 1078 74% 18.25Gx24.25 (IN)
L2	Mix		1/2oz	1			Foil 0.5 oz
					4.01	3.12	PREPREG Megtron7(N) 1078 74% 18.25Gx24.25 (IN)
L3	Mix		1/2oz	1			Foil 0.5 oz
					3.76	3.12	PREPREG Megtron7(N) 1078 74% 18.25Gx24.25 (IN)
L4	Mix		1/2oz	1			Foil 0.5 oz
					4.01	3.12	PREPREG Megtron7(N) 1078 74% 18.25Gx24.25 (IN)
L5	Mix		1/2oz	1.2			Foil 0.5 oz
					5.17	3.11	PREPREG Megtron7(N) 1035 75% 18.25Gx24.25 (IN)
						3.11	PREPREG Megtron7(N) 1035 75% 18.25Gx24.25 (IN)
L6	Mix		1/2oz	0.6	2.00	3.21	LAM Megtron7(N) 0.0020 1035 .5/.5 HVLP 18Gx24(IN)
L7	PIn		1/2oz	0.6			
					3.40	3.17	PREPREG Megtron7(N) 1078 70% 18.25Gx24.25 (IN)
					3.41	3.17	PREPREG Megtron7(N) 1078 70% 18.25Gx24.25 (IN)
L8	PIn		1/2oz	0.6	2.00	3.21	LAM Megtron7(N) 0.0020 1035 .5/.5 HVLP 18Gx24(IN)
L9	Mix		1/2oz	0.6			
					5.13	3.11	PREPREG Megtron7(N) 1035 75% 18.25Gx24.25 (IN)
						3.11	PREPREG Megtron7(N) 1035 75% 18.25Gx24.25 (IN)
L10	Mix		1/2oz	1.2			Foil 0.5 oz
					4.03	3.12	PREPREG Megtron7(N) 1078 74% 18.25Gx24.25 (IN)
L11	Mix		1/2oz	1			Foil 0.5 oz
					3.76	3.12	PREPREG Megtron7(N) 1078 74% 18.25Gx24.25 (IN)
L12	Mix		1/2oz	1			Foil 0.5 oz
					4.04	3.12	PREPREG Megtron7(N) 1078 74% 18.25Gx24.25 (IN)
L13	Mix		1/2oz	1			Foil 0.5 oz
					3.92	3.12	PREPREG Megtron7(N) 1078 74% 18.25Gx24.25 (IN)
L14	Sig		1/2oz	1.9			Foil 0.5 oz
SMB					0.70		

Figure 2. A detailed PCB stackup table showing layer functions, copper weights, dielectric thicknesses and material specifications.

single-ended impedance

Layer	Customer's Design			Reference Layer
	Line Width	Impedance	Cal impedance	
1	6	40+/-10%	40.4	2
1	4.8	45+/-10%	45.2	2
1	4.5	46+/-10%	46.1	2
1	3.8	50+/-10%	50.3	2
3	4	40+/-10%	39.9	2&4
3	3.1	46+/-10%	46	2&4
3	2.8	50+/-10%	50	2&4
5	4	40+/-10%	39.9	4&6
5	3.1	46+/-10%	46	4&6
5	2.8	50+/-10%	50	4&6
7	4	40+/-10%	39.9	6&8
7	3.1	46+/-10%	46	6&8
7	2.8	50+/-10%	50	6&8
12	4	40+/-10%	39.9	11&13
12	2.8	50+/-10%	50	11&13
14	6	40+/-10%	40.4	13
14	4.8	45+/-10%	45.2	13

Figure 3. Single-ended impedance table comparing the customer's intended trace widths and target impedances with the fabricator's calculated values.

Tips for Signal Integrity

Keep signals adjacent to a ground plane whenever possible and avoid letting high-speed traces cross plane splits. Doing so is essentially the electrical equivalent of removing the bridge beneath a moving car.

Fast signals belong on innerlayers where they can be naturally shielded, and fine-pitch BGAs require early planning for microvias to ensure breakout is possible.

Throughout the design, maintain copper balance from left to right like a seesaw to prevent mechanical stress and warping.

Think of the PCB stackup as the DNA of your design; responsible for how signals behave, how heat moves and how reliably the board can be produced. A well-built stackup keeps signals clean without unwanted reflections or noise, helps the design pass EMC testing, supports fine-pitch components and can be manufactured repeatedly at scale without unexpected issues.

When teaching stackup design, I always say: "If schematic is your brain, then stackup is your backbone. Without a strong backbone, nothing else stands straight."

AKBER ROY is CEO and founder of RUSH PCB Inc. an electronics manufacturing company specializing in PCB design, fabrication, and assembly services; roy@rushpcb.com (rushpcb.com).

MARKETPLACE **MECHANICS**

The Marketplace for Untapped Inventory

Where excess inventory stops being clutter and starts being currency.

by RYANN HOWARD

For years, companies have treated excess electronic components like an embarrassing secret. They get over-purchased, boxed up and quietly written off – destined for the trash, the gray market or whatever corner of the warehouse no one wants to inventory.

And according to startup founder Margaret Upshur, the bill for that silence is massive.

“We’re talking about $15 billion of chips across the whole industry getting thrown away annually,” she says. “That is the size of many very robust, full industries, just the amount that’s being thrown away.”

Figure 1. Margaret Upshur is the founder of Mobius Materials.

Upshur is CEO and founder of Mobius Materials, a woman-led Virginia-based startup building the first authenticated secondary marketplace for electronic components. Mobius already serves OEMs, EMS providers, defense manufacturers and component traders across North America, Europe and Asia.

The Semiconductor Industry Loves Efficiency – Until It Hits Surplus

Electronics companies can forecast their demand to the decimal place, but the moment a product is delayed, redesigned, canceled or simply not sold fast enough, the inventory chain breaks. Those components – often still sealed, sometimes worth millions – are treated as a sunk cost.

Upshur, who ran operations at IoT infrastructure company Particle for four years, saw the pattern firsthand.

"If you over-forecast, you're stuck with a ton of chips you can't offload and you take huge losses," she says. "If you under-forecast, you're scrambling for short-lead-time chips and diving into the gray market."

The result? Perfectly good parts die in storage while companies on the other side of the world pay inflated panic pricing for the same thing.

'The Drawer of Shame'

Individuals keep a junk drawer. Electronics manufacturers keep … pallets.

"Everybody's got the drawer of shame," Upshur says. "But if you're a manufacturer and you've got the mini pallets worth of shame … maybe you should come talk to me."

Those pallets represent carbon waste, supply chain volatility and avoidable financial loss. Yet culturally, the industry is trained to focus forward, on what needs to be produced, rather than backward, on what was over-bought.

It isn't malicious. It's structural. The losses show up quietly, trickling through E&O (excess and obsolescence) lines that barely get noticed.

"On a financial statement, the E&O line doesn't really appear," she says. "A lot of companies don't realize how much it's costing them to carry this excess."

Figure 2. Margaret Upshur and the group behind a platform that is reshaping how manufacturers resell surplus electronic components.

Fixing a Broken Market, Not Selling to One

Upshur's solution – a liquid, anonymous marketplace for components – is built with modern tools, real price transparency and post-Covid awareness that shortages and gluts are two sides of the same coin.

She didn't set out to build a marketplace because it was trendy. She built it because the pain was personal.

And as a founder in a sector dominated by procurement veterans, semiconductor execs and manufacturing lifers, her perspective stands out: the supply chain doesn't need motivational speeches or sustainability slogans.

It needs infrastructure.

Mobius facilitates real spot-market price discovery by analyzing supply and demand signals across distributors, OEM listings and marketplace activity. The platform identifies a clearing price at which parts can move – giving both buyers and sellers transparent, data-driven pricing. On the supply side, they look at the volumes on the market at authorized distributors and the spot market. On the demand side, they study trends around individual categories and offers for an exact part they have in their system. Then they match those two to create a price at which parts can be bought and sold.

Privacy prevails. Buyers and sellers cannot see the party on the other end of the transaction. All transactions run through a secure escrow model, so funds aren't released until authentication and inspection are complete, protecting both sides without adding friction.

Mobius, which has inspection hubs in Virginia and Hong Kong, performs quality tests on the parts prior to shipment to the buyer. Mobius performs risk-based authentication, including visual inspection, X-ray analysis and electrical testing where applicable. Its machine-learning models help flag potential anomalies earlier in the process (if needed). It also developed its own machine learning-based quality inspection. Buyers receive a comprehensive test report.

"Different types of parts require different types of testing. We're checking for primarily storage type issues; moisture, oxidation. And we can detect them extremely well."

Customers have 14 days to inspect parts themselves and can return failed devices to Mobius.

Export compliance is another strength. "A lot of people don't know the amount of regulation around who you can sell each part to. You can't sell certain chips to some military customers, obviously. But there are kind of second-tier, third-tier level restrictions on what and who you can sell to and what forms you need to fill out to do those sales," Upshur says.

That's important, she asserts, because manufacturers are in the business of buying parts to build product. Their expertise is not in selling parts. Mobius handles that compliance work through managing the export-control requirements for secondary-market component sales, from screening restricted parties to ensuring proper documentation and jurisdiction checks, so manufacturers don't need in-house expertise to safely resell inventory.

Sustainability that Works Like a Balance Sheet

On average, manufacturers recover significantly more value through resale compared to write-downs or scrapping, and they avoid the carbon and material waste associated with disposal.

Upshur is blunt about her philosophy: sustainability only succeeds when it's profitable.

"Most of the things that are sustainable are actually about resource conservation, which is about saving money," she says. "We can be sustainable while saving money."

In other words, companies shouldn't recycle parts because it's good PR. They should recycle them because throwing away inventory is a terrible use of capital.

That shift – from moral good to financial logic – is what she believes will unlock change. Not pressure. Economics.

A Founder Who Went Home to Win

Having lived around the world for her previous jobs, when Upshur launched the business, she returned to her home

state of Virginia. It made good business sense: It's a state with a massive defense footprint and the country's largest chip fab.

"Virginia is a great place," she says. "It's home of Micron, a lot of aerospace and military, pro-business regulation, and lower cost."

Upshur named the company after the Mobius strip: a two-sided shape that is, mathematically, one continuous surface.

A loop without waste. A circle with no end.

The Bigger Picture

Whether Mobius wins the market or sparks a wave of similar efforts, the idea feels overdue. The semiconductor industry has mastered precision at the front of the supply chain; Upshur is trying to bring the same rigor to the back end.

If she's right, sustainability won't come from regulations or corporate messaging. It will come from the same force that drives every supply chain decision:

Profit.

And perhaps from one founder who looked at billions of dollars sitting in warehouses and thought:

What if waste didn't have to be wasted?

RYANN HOWARD is managing editor of PCD&F/Circuits Assembly; ryann@pcea.net.

To listen to the PCB Chat interview with Upshur, click here.

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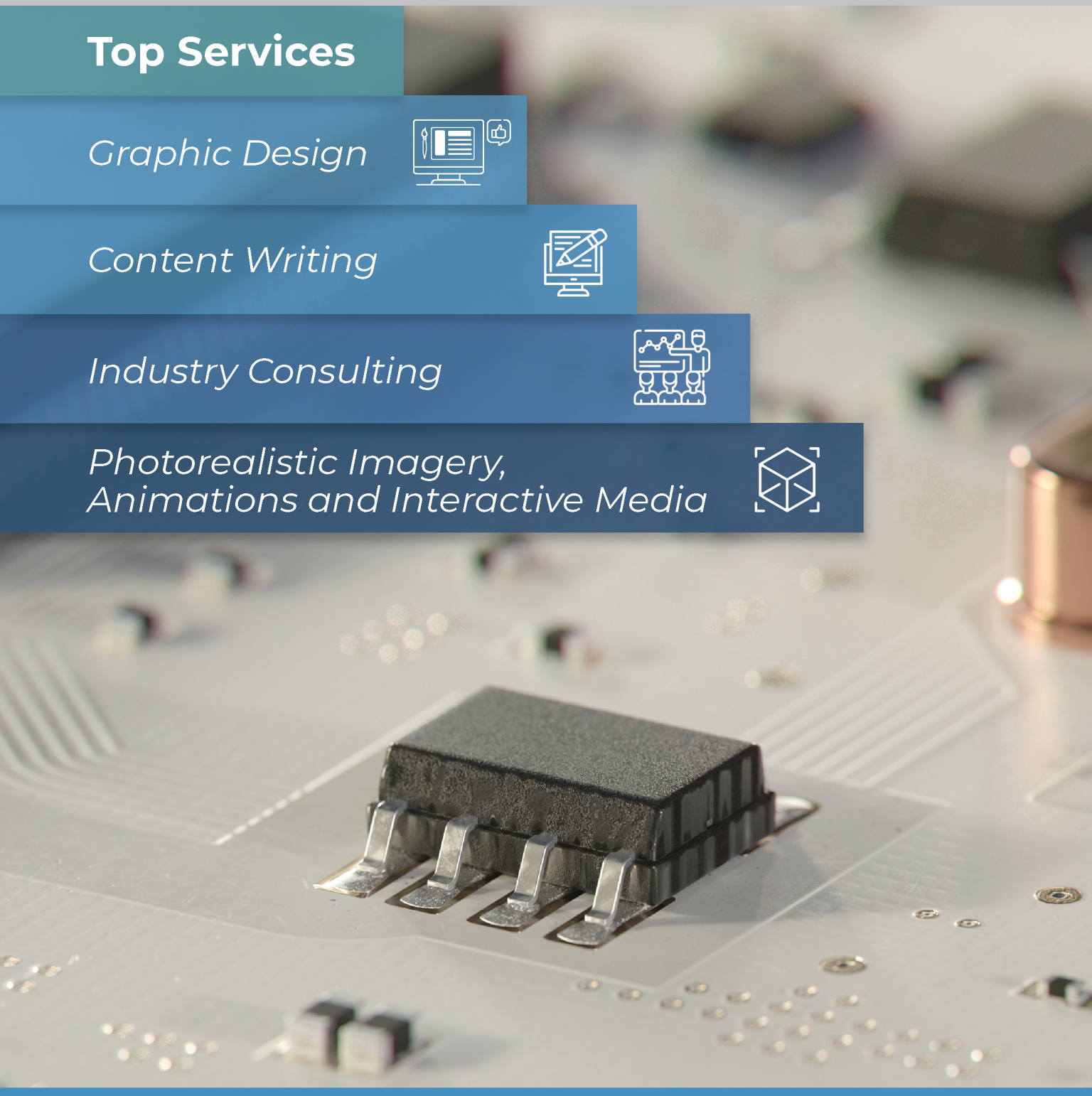

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STENCIL **PERFORMANCE**

A Comparison of Stencil Capabilities

How do modern stencil materials and coatings influence transfer efficiency and volume repeatability as SMT features continue to shrink?

by CHRYS SHEA, ANTONIO TORRES and MICHAEL BUTLER

The key indicators of SMT stencil performance are transfer efficiency and volume repeatability. Transfer efficiency (TE) refers to the percentage of solder paste released from the stencil when compared to the stencil's aperture volumes and is expressed as a percentage. Typical values range from 60% to 120%.

While maximizing TE is important, minimizing variation is imperative. Variation in solder paste prints leads to rework, a non-value-added expense that risks the assembly's functionality and reliability. Volume repeatability is expressed in terms of statistical variation. The coefficient of variation (CV or CoV) is calculated by dividing the standard deviation of print volumes by their average. It is also expressed as a percentage. Acceptable values are 10% or less. Borderline values are 10-15%. CVs over 15% are unacceptable.

Background

The relationship between stencil design and print quality is often characterized using the following terms:

- Area ratio (AR) is calculated as the area of the aperture's PCB-side opening divided by the area of the aperture walls **(Figure 1)**. It is an indicator of the relative adhesive forces on the solder paste deposit during separation from the stencil. As area ratios decrease, the typical percentage of paste transferred also decreases. The minimum acceptable area ratio is often considered to be 0.60 for typical SMT purposes that print with Type 4 solder paste and 0.66 when using the larger particles in Type 3 solder paste.

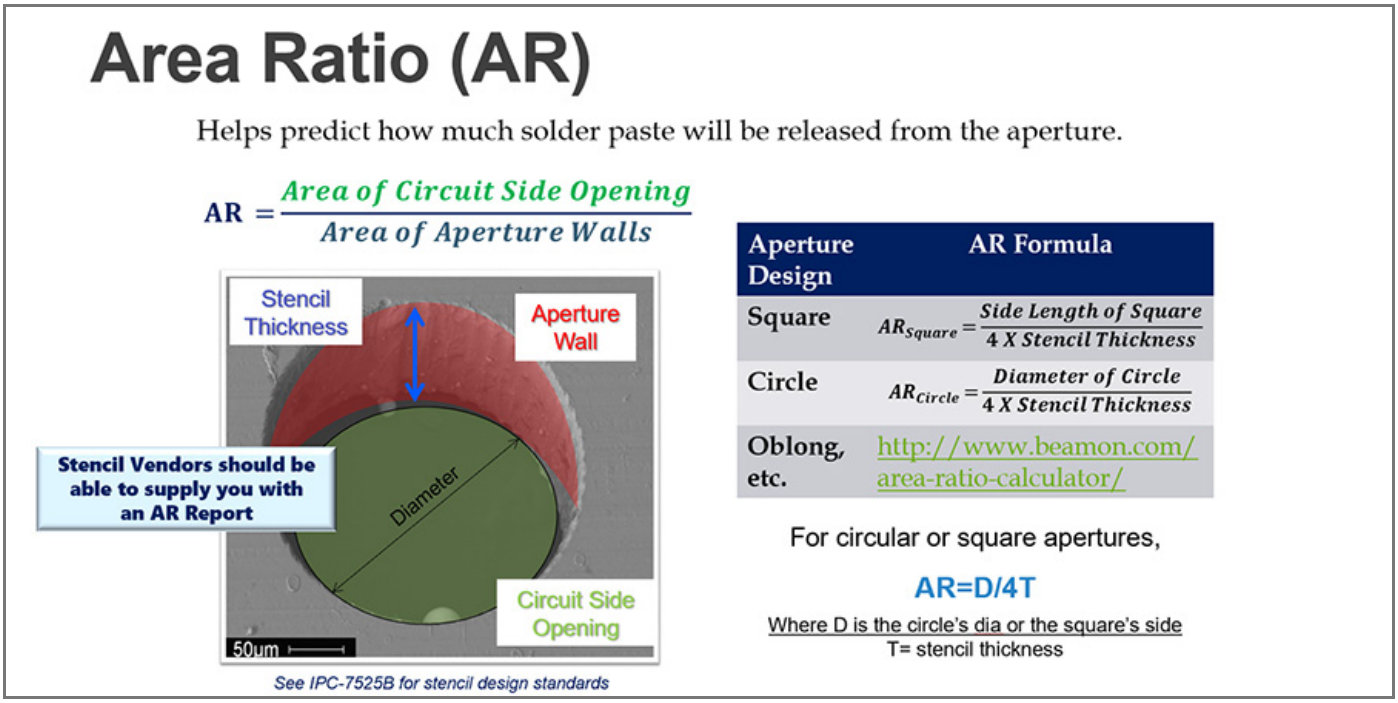

Figure 1. Area ratio calculation.

- Transfer efficiency (TE) is the percentage of paste that is actually transferred out of the stencil aperture onto the PCB, as opposed to what was left sticking inside the aperture walls or on the bottom of the stencil **(Figure 2)**. It is calculated as the average paste deposit volume divided by the aperture's volume and expressed as a percentage. A common benchmark is 80% TE.

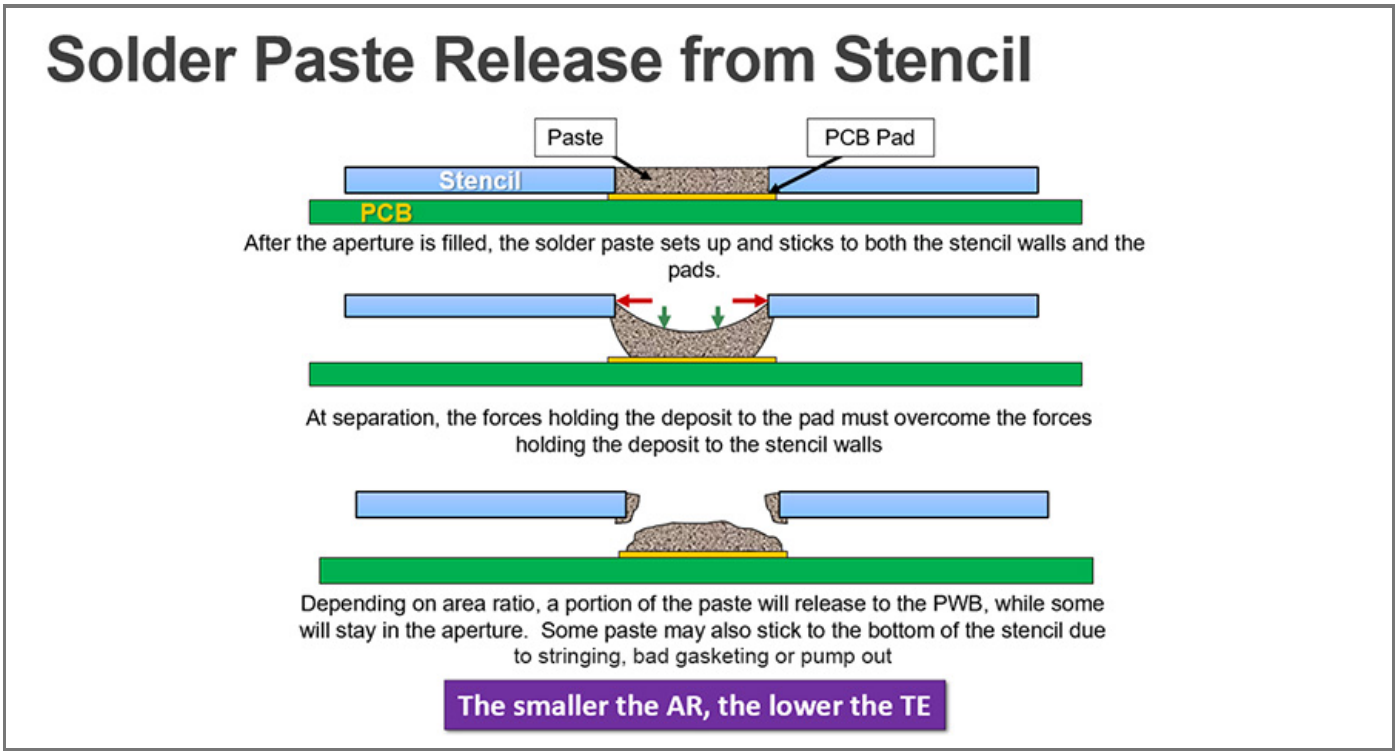

Figure 2. Opposing forces in solder paste release from stencil aperture.

TE is often plotted as a function of AR to characterize stencil release. **Figure 3** shows a typical TE plot for different

stencil types, and **Figure 4** shows actual photographs of release for different Ars.

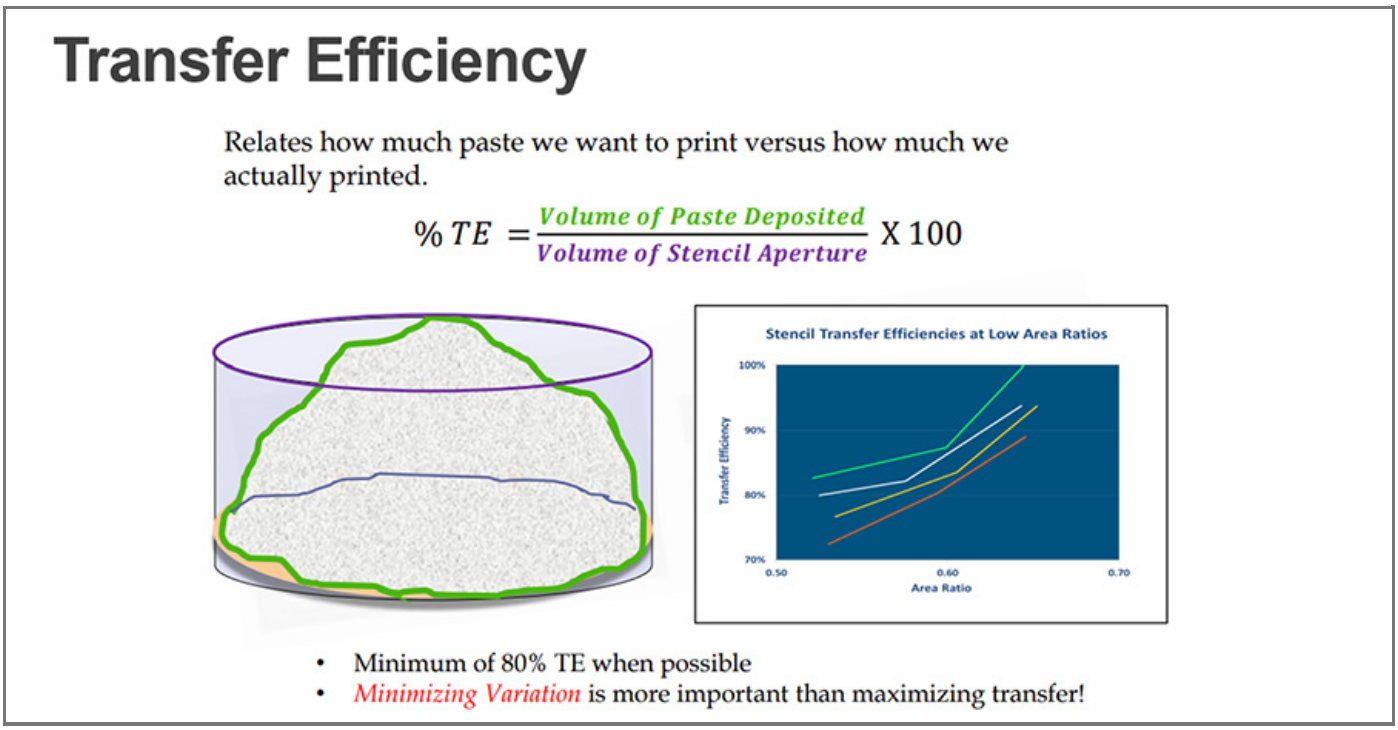

Figure 3. Typical TEs of different stencil types.

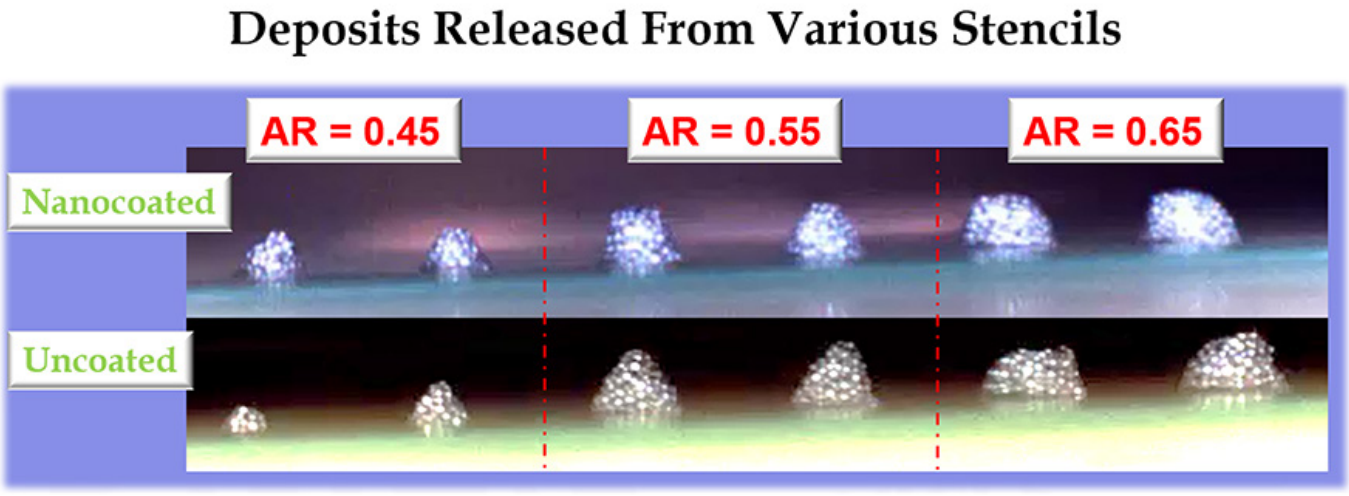

Figure 4. Side-view photos of paste deposits at different ARs.

ARs and TEs may be either theoretical or actual. Theoretical ARs and TEs are calculated from the stencil specification, whereas actual ARs and TEs are based on actual measurements. The TEs reported by solder paste inspection (SPI) machines are theoretical, based on the apertures' CAD dimensions and thickness.

Variation. Minimizing variation is critical in fine feature printing. Print volume variation can lead to opens, shorts, head-in-pillow and tilted component defects. High variation indicates an out-of-control process that may be creating both obvious and hidden defects.

Cpk, or the process capability index, is a popular and common metric for indicating manufacturing variation. It is usually calculated using a target or goal of 100% volume and upper and lower control limits of +/-50%. In cases involving solder paste volumes, where average TEs are often below 100%, standard Cpk calculations can skew the metric unfavorably.

Example: If the average solder paste deposit is 200 cubic mils and the standard deviation is 20 cubic mils. CV = 20/20 0 × 100 = 10%

If the average deposit is smaller – say 50 cubic mils – but the standard deviation is still 20 cubic mils.

CV = 20/50 × 100 = 40%

Both cases have the same absolute spread, but the smaller deposit is much less consistent relative to its size. This is why CV is more meaningful than standard deviation alone.

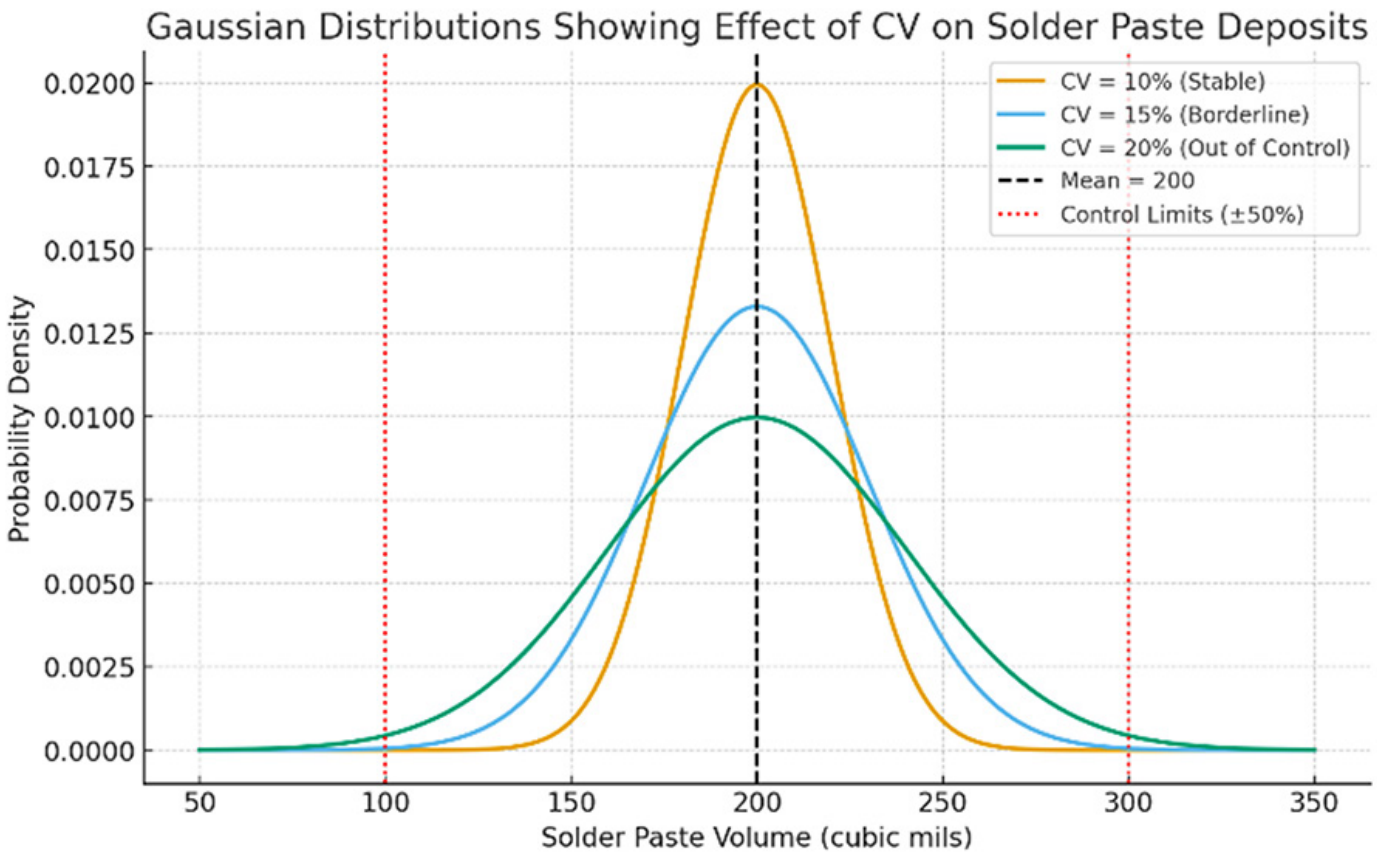

Figure 5. Modeled Gaussian curves show the impact of CV on solder paste volume consistency.

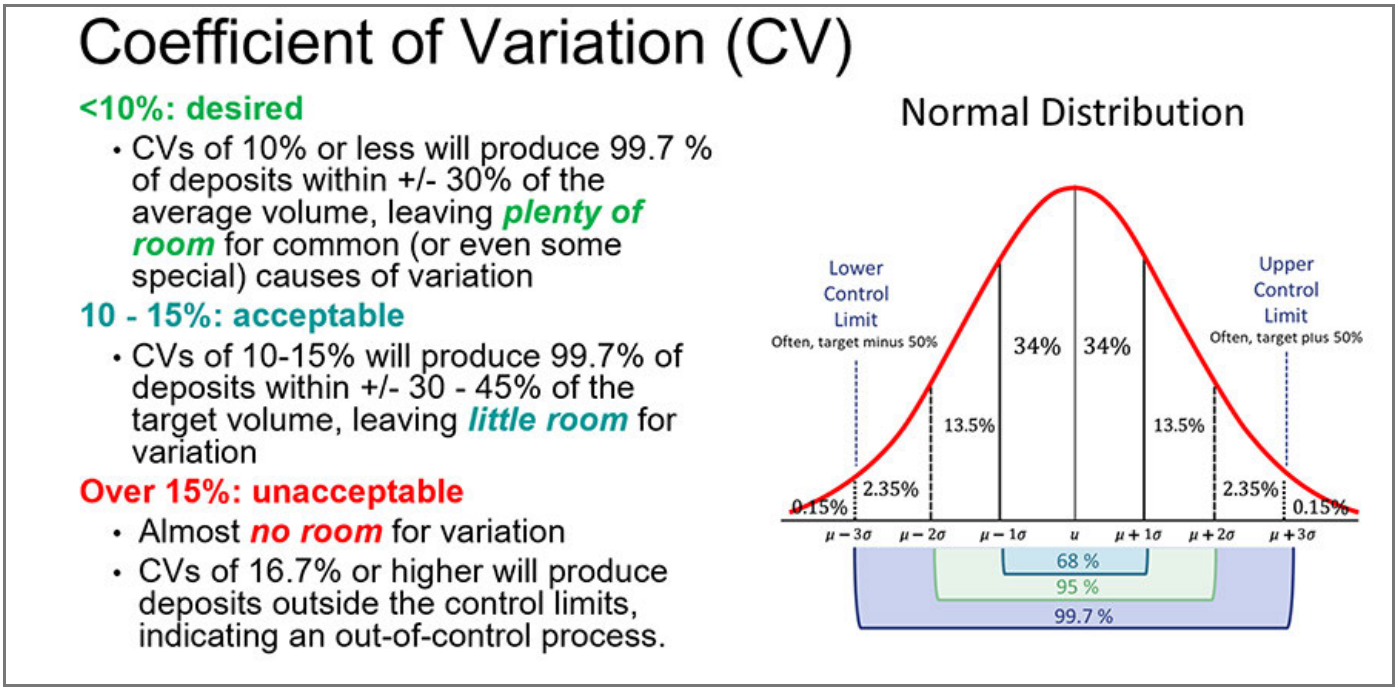

Figure 6. Relationship between CV and control limits.

Interpreting CV in Solder Paste Printing

- CV <10% stable and desirable: A CV below 10% indicates a very stable process. Statistically, 99.7% of solder deposits will fall within ±30% of the average volume. For example, if the average deposit is 200 cubic mils, nearly all deposits will land between 140 and 260 cubic mils. This is well inside the typical process control limits of ±50%.
- CV ≈ 15% borderline / at risk: At around 15%, the variation grows. Here, 99.7% of deposits fall within ±45% of the mean. For a 200 cubic mil target, that means deposits ranging from 110 and 290 cubic mils. While still technically within process limits, the margin is tight. Any drift in stencil condition, paste rheology, or printer setup could push the process out of control.
- CV > 16.7% out of control: A CV above 16.7% signals excessive variation and an unstable process. Too many deposits will exceed the ±50% control window, leading directly to defects such as opens, insufficiencies, bridging or head-in-pillow failures.

The CV measures the repeatability of solder paste deposits relative to their mean size, providing insight into process stability. While high TE confirms that sufficient solder paste is being deposited, low CV demonstrates that the deposits are applied consistently across the board. Together, TE and CV form the foundation of a reliable solder paste printing process, ensuring consistent joint formation and long-term assembly reliability.

Experimental Methods

Print tests. The top side of the SMTA miniaturization test vehicle is shown in **Figure 7**. The top side was printed. Clean, new boards were used for the tests.

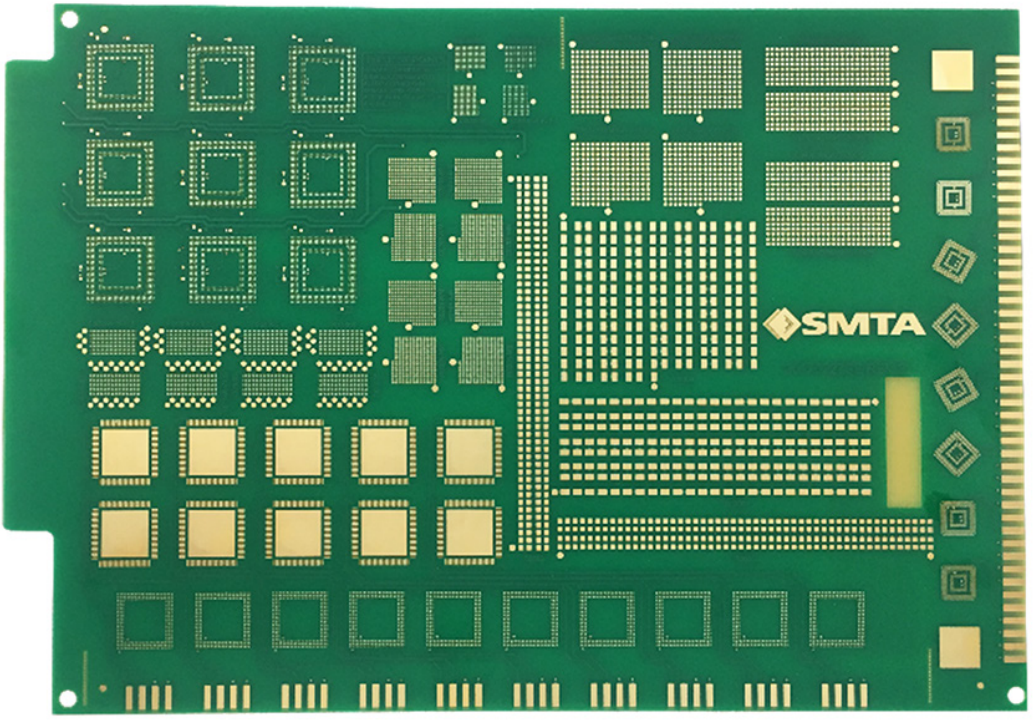

Figure 7. A SMTA miniaturization test vehicle.

All stencils were print–tested simultaneously on the same run, using the same setup, paste and SPI machine **(Figure 8)**.

Figure 8. A printer and SPI machine in the laboratory.

The typical 10-print test was used for all stencils. The 10-print test consists of two knead strokes, a dry underwipe and 10 consecutive prints with a dry wipe between each print. The first print is always back-to-front to visually ensure the paste is rolling properly.

Printed boards were then automatically passed via conveyor to the SPI. Print tests took place at the Parmi demonstration laboratory in Hopkinton, MA, using the following equipment and materials:

- Printer: ITW MPM Momentum
- SPI: Parmi Sigma X certified by CeTaQ[3]
- ScanCAD stencil inspection equipment
- Paste: Indium 8.9 HF Type 4
- Squeegees: 60-degree Surgical SS with backing plate
- Six stencils from three different suppliers; one uncoated and five with nanocoating
- Standard underwipe textile, no solvent used

To aid in debugging print results, stencil measurement software was used to scan the stencils and compare the aperture openings to their theoretical sizes. The system uses a high-resolution scanner to capture the stencil image and software to overlay CAD designs and compare actual aperture sizes with their designed dimensions.[4]

Data Analysis Methods

Datasets for the 0201, 05BGA, 04BGA and 01005s are exported to a comma-delimited file. Each dataset contains the

- Measured volume (mils)
- Theoretical transfer efficiency, TE (%)
- Actual area measured at the 20µm threshold
- Theoretical area % at 20µm threshold
- X offset* (mils)
- Y offset* (mils)
- Panel index**
- Time stamp.**

* Offsets are not used in calculations for these tests but are always exported to help in diagnosing seemingly anomalous data, such as excessive volumes due to aperture-pad misalignment.

** Panel ID and time stamps are recorded for purposes of clarification when reviewing data.

The datasets are then imported into an Excel spreadsheet. Several different analysis methods are applied. Pivot tables are used to calculate the average and standard deviation of the measured solder paste volumes. The CV is then calculated and analyzed. Data with CVs indicate the edge of the process window, where slight input differences can have considerable effects on process outputs.

Experimental Results

Initial results showed similar TEs for most stencils, but one stencil showed far superior performance – so superior that it was suspicious **(Figure 9)**. An investigation subsequently revealed that the wrong stencil design was used. The data were excluded from the analysis; however, the investigative methods and results are reviewed.

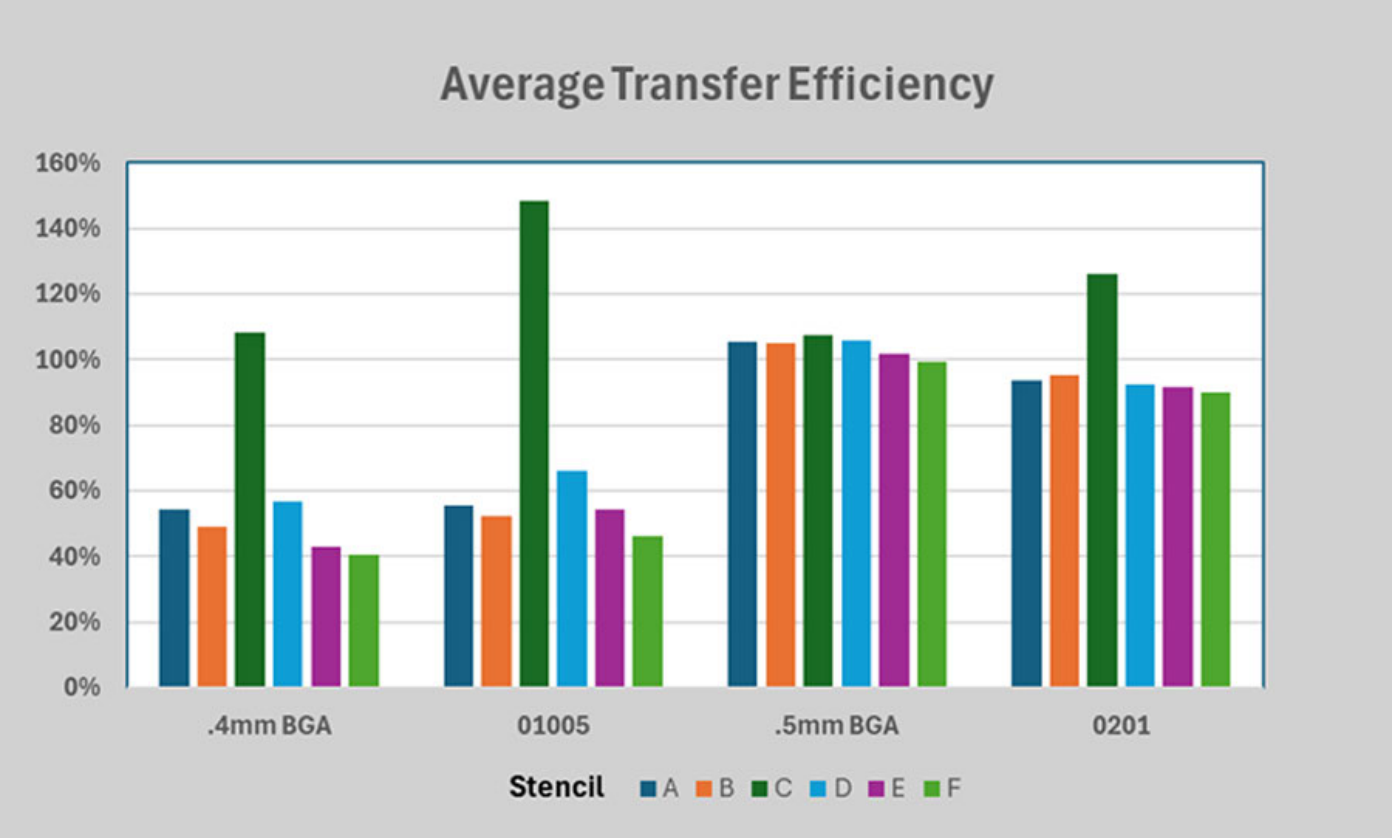

Figure 9. SPI TE results.

Table 1 shows TE and CV results for the remaining five stencils. The 0.5mm BGA (05BGA) exhibited an interesting range of CVs in or near the 10-15% range. Therefore, the solder paste volume and release data for the 05BGAs are the focus of the analysis.

Table 1. Chart on TE Results

Component	Stencil	Transfer Efficiency	CV of TE
0.4mm BGA	A	55%	57%
	B	49%	68%
	D	57%	51%
	E	43%	75%
	F	41%	76%
1005	A	56%	48%
	B	52%	51%
	D	66%	32%
	E	54%	51%
	F	46%	59%
0.5mm BGA	A	106%	10%
	B	105%	9%
	D	106%	9%
	E	102%	13%
	F	99%	12%
0201	A	94%	7%
	B	95%	6%
	D	92%	6%
	E	92%	7%
	F	90%	7%

Print data from the 10-print test may be analyzed in multiple ways. First is a simple run chart showing the volume of each print **(Figure 10)**. The average volume shift between prints indicates uniformity across back-to-front and front-to-back strokes and the "leading edge" effect. In this experiment, average volumes ranged from approximately 360 to 420 cubic mils across stroke directions, with greater variability in earlier print strokes than in later ones. The stroke-to-stroke variation may be partially attributable to machine calibration and partially to the leading-edge effect of the PCB design.

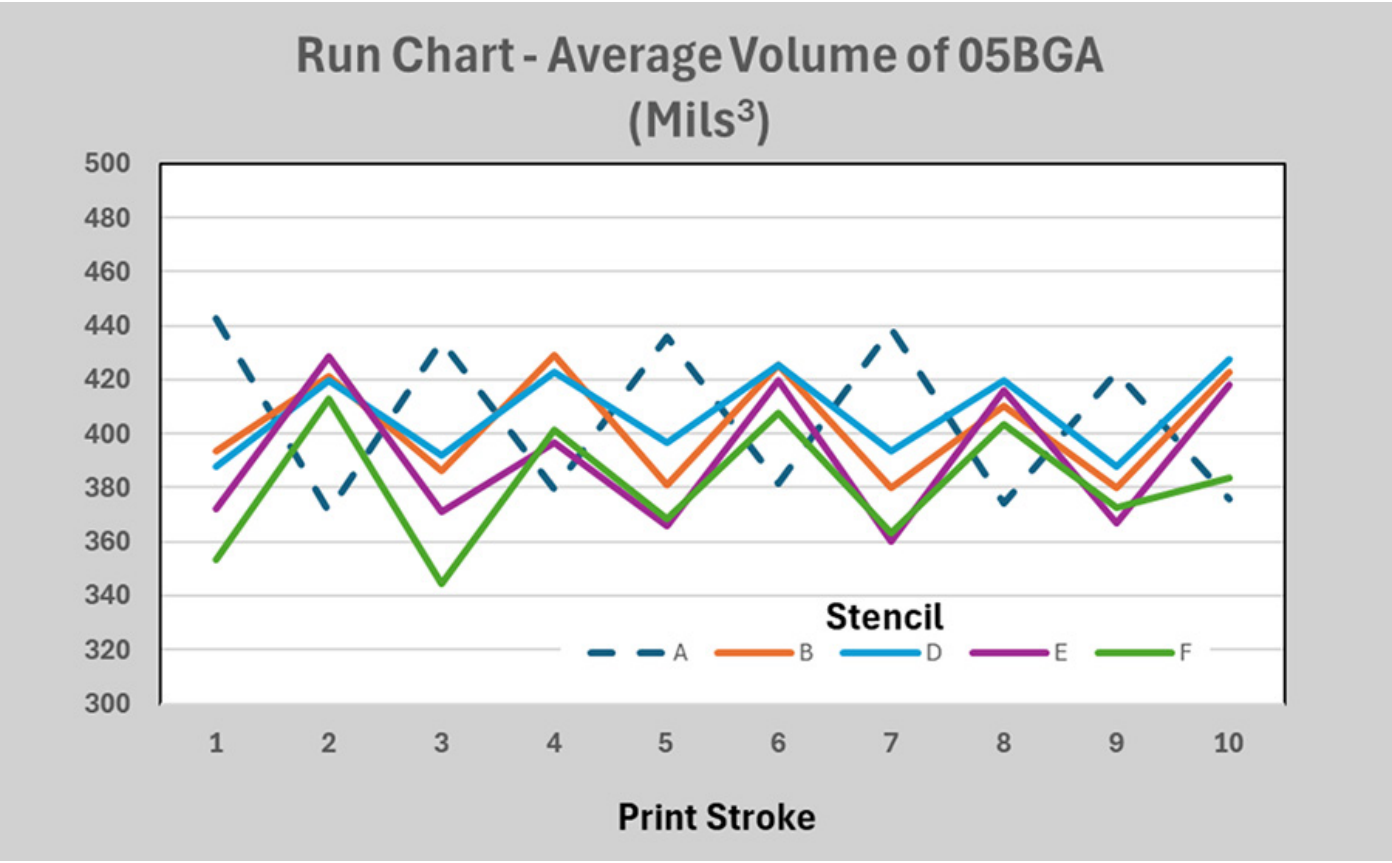

Figure 10. Average volumes of 05BGAs for prints 1-10.

Of particular interest is Stencil A, which was obviously run in opposite squeegee directions from the rest of the stencils tested.

Run charts often show that paste volume increases and variation decreases in the first few prints as the paste reaches its working viscosity from rolling on the stencil. Note that two knead strokes were applied before the first print to begin shearing the paste down to lower its viscosity.

The histograms in **Figure 11** show the distribution of the data. Taller, narrower bell curves are preferred over shorter, wider bell curves, because they show a tighter distribution. Their tighter distribution indicates better process control, less obvious defects and rework, and less latent joint failures in service.

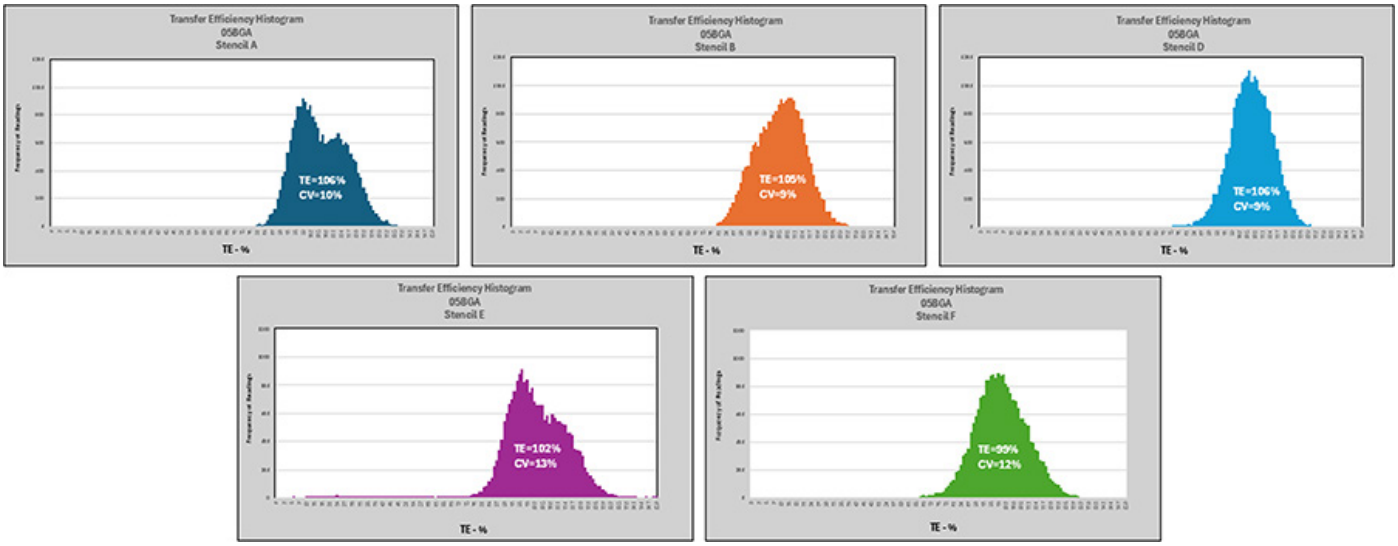

Figure 11. Histograms showing the distribution of data.

Review of the histograms: notice that the means are not 100%, indicating the use of CV over Cpk as a metric of paste volume repeatability. A Cpk metric would be skewed by calculating Cpk based on 100%, +/-50%, because the process would not be considered centered in the window. Also, notice that Stencil E has a relatively large CV due to its many insufficient solder deposits. Based on histogram analysis, Stencil D provided the tightest distribution of print volumes.

Box and whisker plots also show the average volume and spread of the data, but offer more interesting insights. In a boxplot, the data set is divided into quartiles **(Figure 12)**. The box represents the middle two quartiles (Q2 and Q3) of the data. The average or mean – represented by the X – may or may not be in the middle of the box. The whiskers represent the outer two quartiles (Q1 and Q4), indicating the overall spread of the data. Outliers are calculated statistically.

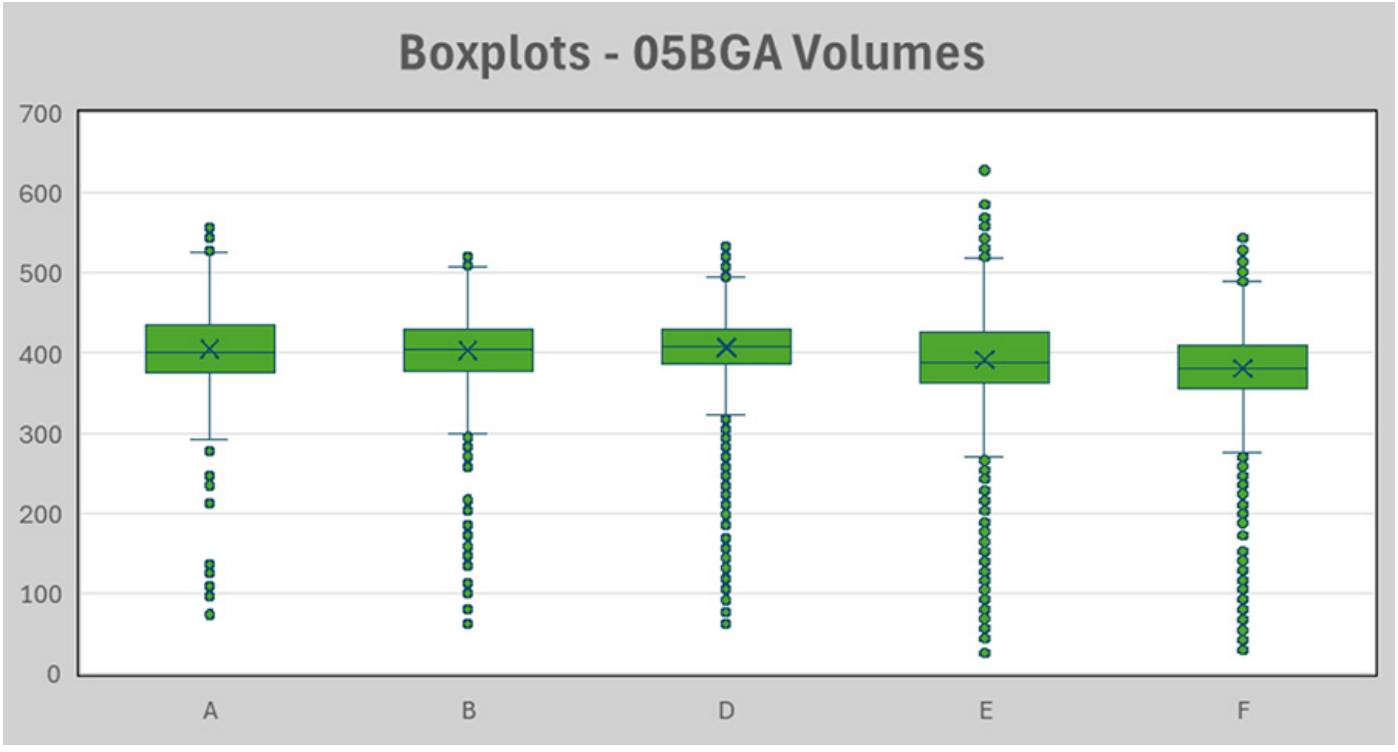

Figure 12. Boxplots of 05BGA volumes from different stencils.

Outliers are important in reviewing SPI data. Outliers above the upper whisker indicate excessive volumes, which are often due to gasketing issues, and are less worrisome than insufficient volumes. Outliers below the lower whisker are more prevalent on fine feature prints and can result in fragile solder joints. The frequency of insufficients and zero volume reading are more visible in box and whisker plots than histograms or CV calculations.

Review of the b and whisker plots shows that Stencil D has the tightest distribution, but Stencil A has fewer outliers, particularly on the more dangerous lower end of the spectrum.

Zero volume readings in SPI. On fine-feature prints, the SPI may read and report zero volume, despite visible paste on the pad. SPI machines read solder paste deposit volumes at a height threshold off the board; typically, that Z-height is 40µm above the board surface. The algorithm precisely measures the solder paste volume above the threshold and calculates the volume under the threshold by multiplying the area at the threshold by its Z-height. Solder paste that does not cross the threshold does not get included in the measurement or calculation. In this test, the threshold was set to 20µm.

Discussion of Results

All five stencils performed respectably. One stencil was not coated; the others were coated with very thin nanocoatings. These coatings lower surface energy to enable better release, but they do not always compensate for aperture wall roughness **(Figure 13)**.

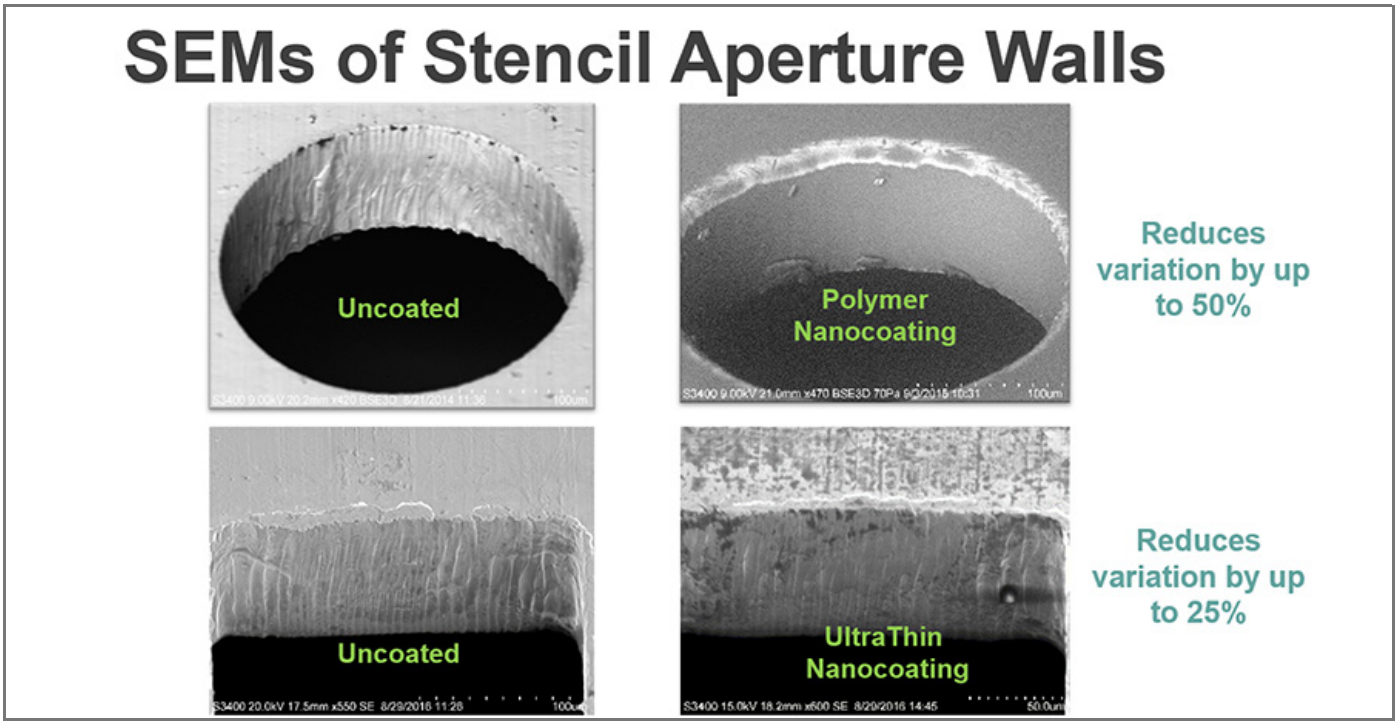

Figure 13. High magnification views of stencil aperture walls.[5]

Previous studies have indicated that thinner fluxophobic coatings reduce variation by approximately 25%, whereas the thicker, spray-coated and cured coatings reduce variation by as much as 50%.

It has been hypothesized that the reason the thicker coatings provide lower variation is that they fill in the small fissures in the aperture walls created by the laser-cutting process. The reduction in wall roughness essentially lowers the surface area of the aperture, positively affecting its actual AR and improving the boundary condition of the paste-aperture interface by leaving fewer places for solder particles to bind when flowing through the stencil.

Thicker polymer coatings have also demonstrated quantifiable TE benefits at ARs as low as 0.50. But because of the coatings' physical thickness, they may become self-limiting in the future as aperture sizes continue to shrink. Thinner coatings will ultimately be needed to extract the benefits of nanocoating in future miniaturized electronic assembly processes.

All the stencils tested showed good process capability for 0.5mm BGAs with ARs of 0.63, but poorer capability for 01005s with ARs of 0.50. These results are typical for Type 4 solder paste with 4 mil stencil thickness and ultrathin nanocoatings.

Stencil Discrepancy Investigation

Several avenues were pursued to understand why Stencil C printed so differently from the other five.

The first step when investigating high solder paste volumes is to review the X and Y offsets. Poor gasketing is often the root cause of excessive solder volumes. As shown in **Table 2**, most X and Y offsets were less than 1 mil, thereby excluding them as possible root causes of excessive deposit volumes.

Table 2. Average Print Offsets

Component	Stencil	Avg Offset X	Avg Offset Y
0.4mm BGA	A	0.82	-0.64
	B	0.90	-0.56
	C	1.51	-0.73
	D	0.53	-0.18
	E	1.27	-0.28
	F	1.36	-0.63
1005	A	0.24	-0.10
	B	0.37	-0.06
	C	1.26	-0.47
	D	0.41	0.20
	E	0.50	-0.04
	F	0.60	-0.12
0.5mm BGA	A	0.48	0.05
	B	0.61	0.20
	C	0.69	0.30
	D	1.27	0.78
	E	1.05	0.43
	F	0.96	0.31
0201	A	-0.03	-0.12
	B	0.08	-0.27
	C	-0.02	0.06
	D	-0.09	0.07
	E	0.26	-0.14
	F	0.38	-0.27

The next step was to review areas with excessive pressure, indicating possible “pump out” or “squeeze out” from high pressure that disrupts gasketing or stringing due to release issues.

Table 3 shows the average area % readings for each stencil. The disproportionately large areas of Stencil C on three of the four device types supported the hypothesis that something was different in C’s dataset.

Table 3. Average Print Areas

Component	Stencil	Area %
0.4mm BGA	A	38
	B	35
	C	67
	D	40
	E	32
	F	32
1005	A	37
	B	36
	C	81
	D	42
	E	37
	F	34
0.5mm BGA	A	97
	B	92
	C	98
	D	98
	E	93
	F	91
0201	A	136
	B	136
	C	164
	D	133
	E	132
	F	133

The third avenue was to examine the potential for experimental execution errors. The original data was re-exported and re-analyzed. The numbers were identical, eliminating data transfer as a root cause.

The stencil was then reprinted using the same solder paste. The data correlated with the first test's results, indicating no errors in setup or execution.

The stencil was then visually reviewed, but no discrepancies in the apertures in question were noticed.

The stencils were sent out for scanning to measure the apertures. The scanned and compared images revealed the differences. In the close-up view of the scanning results **(Figure 14)**, the actual aperture is round, whereas the aperture design is a squircle – a square with rounded corners.

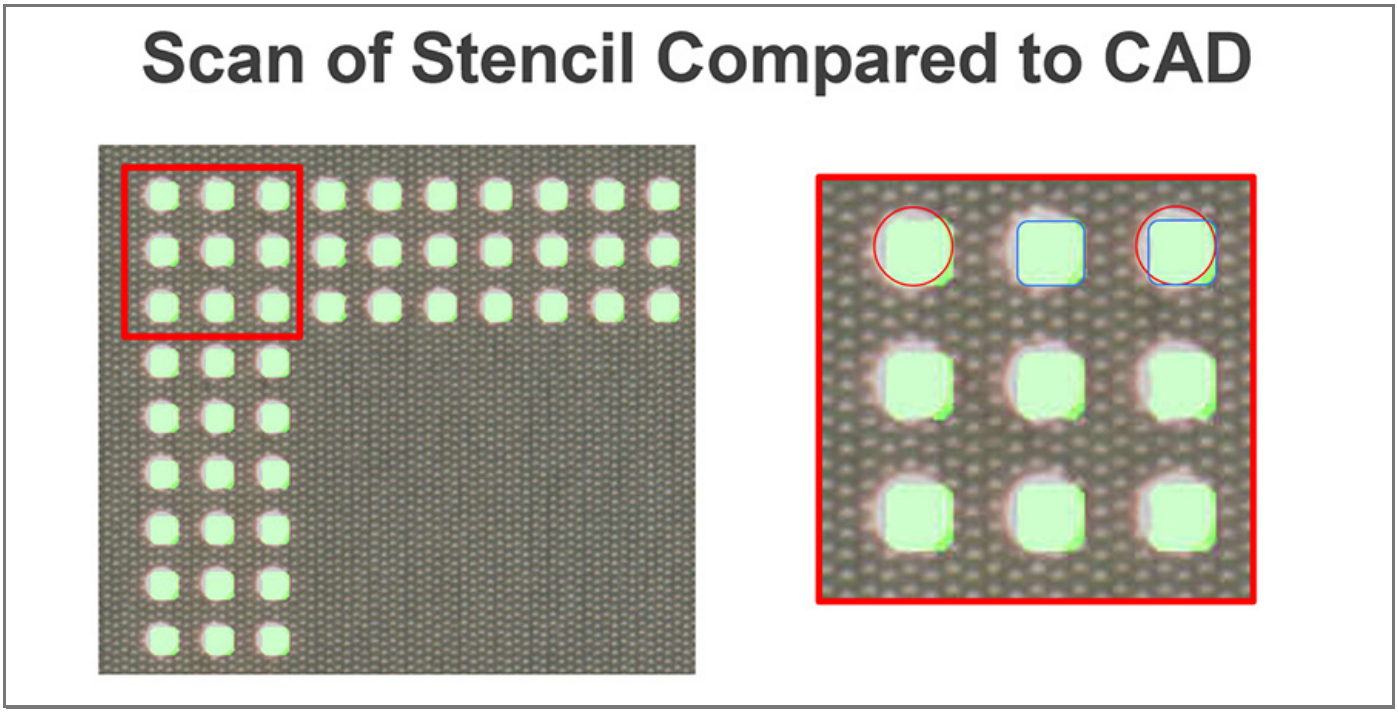

Figure 14. ScanCAD image of actual stencil vs. Gerber data.

The shape of the apertures was not exactly the same as the CAD, but they were not very different, and therefore, not easy to discern. Other apertures on the stencil overlay were recognized from a previous experiment, and the Gerber files were still available for comparison.

In the test stencil design, the 04 BGAs and discretes had smaller apertures than the ones on stencil C. The default stencil design for the 04BGAs is a 7.5 mil squircle; Stencil C had an 8.5 mil circle. **Figure 15** shows the overlay of the two and the impact on area ratio.

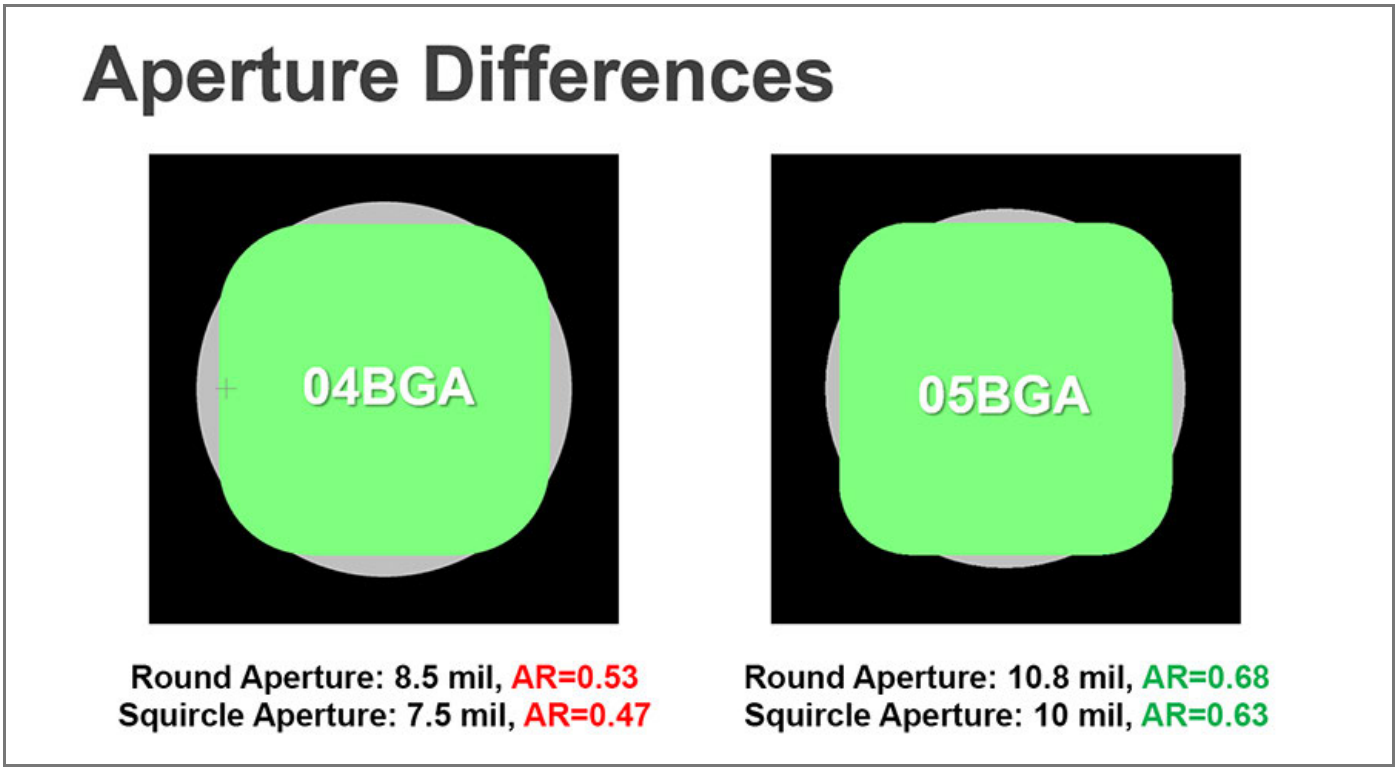

Figure 15. Shape, size and AR differences in CAD.

The default stencil design for the 05BGA device is a 10 mil squircle; Stencil C had a 10.8 mil circle. Of the four aperture designs studied, the 05BGAs were the most similar in geometry. Referring back to Figure 8 and Table 3, these apertures produced the closest volumes to the default stencil design. Because the designs were not exact, and Stencil C had an AR advantage, the data remained excluded from the analysis.

Conclusion and Discussion

Solder paste print processes with CVs below 10% are considered very stable. Print processes with CVs greater than 17% are considered unstable and out of control by standard criteria. Processes with CVs in the 10-15% range offer excellent opportunities to understand the edges of the process window.

In this study, the 0.5mm BGAs produced CVs within the typical range for the test process used. Therefore, the dataset for the 05BGAs was selected for further analysis.

The five stencils with the same aperture designs performed as anticipated. Stencils A through D and F were coated with different coatings; stencil E was uncoated. It had the largest CV, the widest distribution, and the most insufficient deposits. All coatings outperformed the uncoated stencil.

A key takeaway is that all four coatings outperformed no coating. While some combinations of metals, laser-cutting technologies, and nanocoatings may exhibit performance advantages over others, one fact remains consistent: nanocoating is better than no coating, every time.

Multiple methods of evaluating stencil and printer performance were introduced and reviewed, including:

- **Run charts** help illustrate the differences between front and rear print strokes, as well as the number of strokes for the paste to reach its working viscosity.
- **Histograms** show the spread of the data. In the context of solder paste transfer, they are rarely centered at 100%.
- **Boxplots** also show the spread of the data but make outliers more visible than histograms.
- **Pivot tables** enable fast and easy data manipulation, including basic statistics on volumes, TEs, areas and offsets for analysis.

Statistical analysis software can yield more sophisticated insights into the main effects and interactions of input factors than spreadsheet-based analysis, particularly when additional factors are introduced. Spreadsheet analysis is fast, easy and accessible, and pivot tables provide excellent opportunities to run "what if" scenarios and identify trends, however.

Lessons Learned

In addition to the planned results from this study, three valuable learnings were also realized:

1. If data looks anomalous, do not ignore them. Investigating spurious data may lead to new discoveries or, in this case, cleaner data. Had this dataset been part of a multivariable DoE analyzed without human review, the aperture discrepancy would have grossly skewed the main effects and interactions results – and perhaps the conclusions and subsequent critical decisions.
2. Always use SPI to verify a stencil before a run. Using the two-print test shown in **Figure 16** would have immediately indicated the differences in Stencil C.
3. Cut test coupons similar to those shown in Figure 16 in the corners of the stencil for ease of measurement. This practice has been recommended since 2014, but was not followed in this experiment. It will be reintegrated into the next revision of the SMTA Miniaturization Test Vehicle (MTV) stencil artwork.

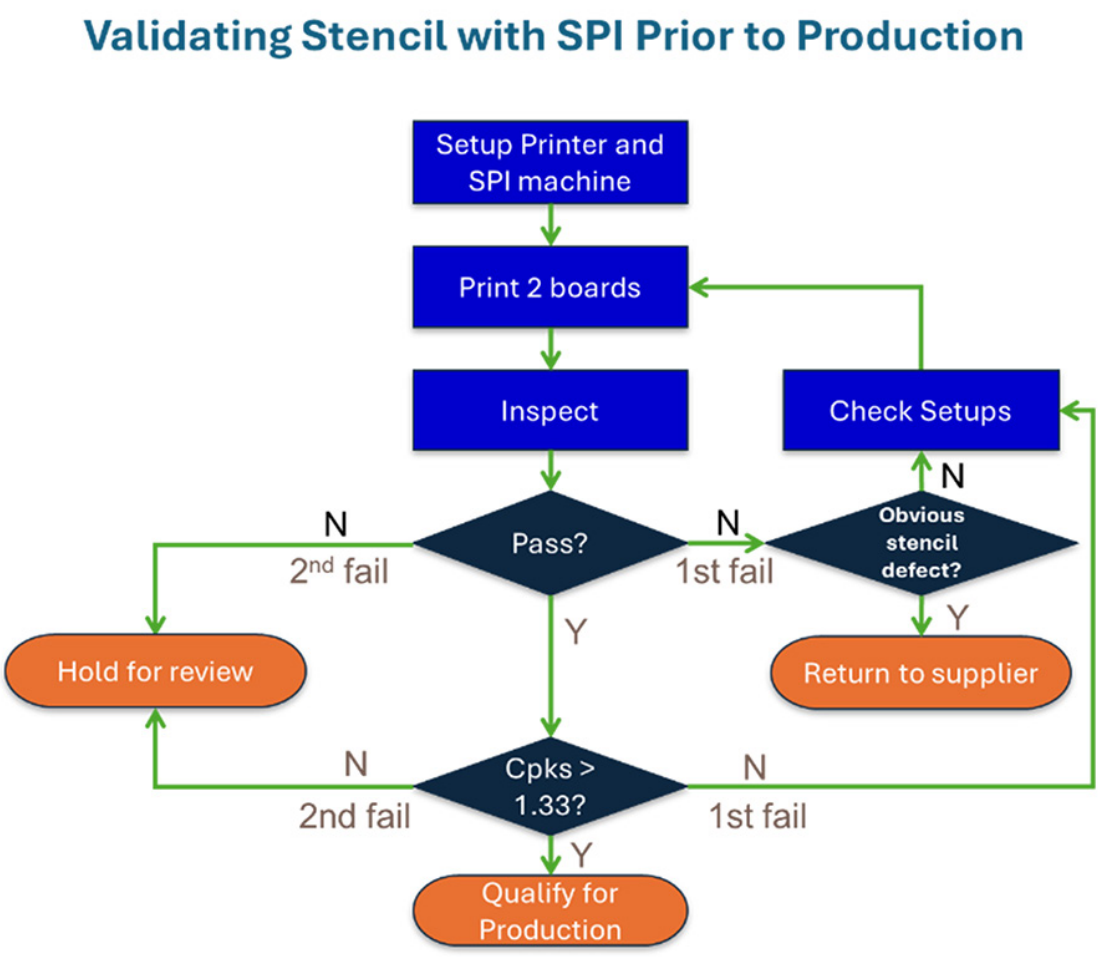

Figure 16. SPI stencil verification flow chart.

Recommendations and Future Work

The quest for electronics miniaturization will never end. Manufacturing processes will continue to develop in order to support the ongoing trends.

As feature sizes shrink with the advent of ultra high-density interconnect (UHDI) technology, the solder paste deposition process will address new challenges with more evolution:

- More accurate and repeatable deposition hardware
- Thinner, stronger stencil foils
- Types 5 and 6 solder pastes
- More advanced test vehicles.

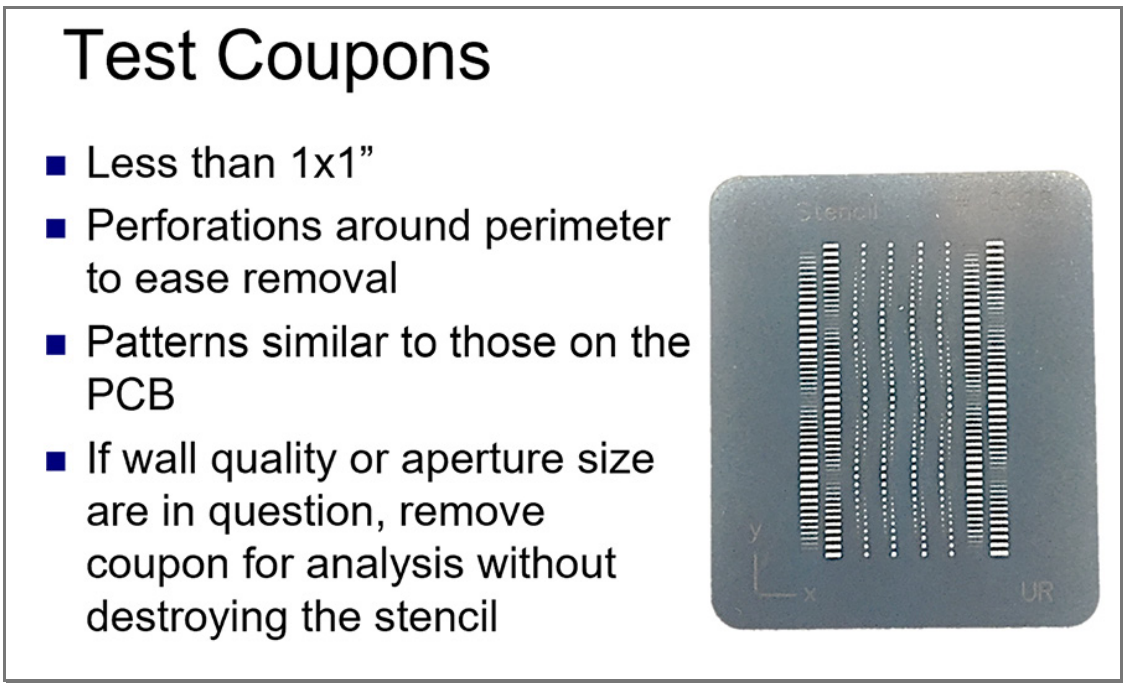

Figure 17. Test coupons for measuring stencil apertures.

The “original” SMTA test vehicle, designed in 2017, was used for this test because it has a long history and a very large database, which can be used to compare print performance. Even this MTV test board faces impending obsolescence as it gets phased out in favor of a more contemporary, 2025 version referred to as the UHDI board **(Figure 17)**.

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CHRYS SHEA is owner at Shea Engineering Services LLC (sheaengineering.com), and a four-time recipient of the SMTA International “Best of Conference” award. ANTONIO TORRES is application engineer and MICHAEL BUTLER is application manager at Parmi (parmi.com); atorres@parmiusa.com.

Evolving Quality Control into Quality Assurance

An automation shift shows how smarter processes reduce inspection and boost value-added work.

ADVANCES IN TECHNOLOGY offer many ways to improve efficiency and reduce costs without impacting quality through automated inspection tools. The full potential of these tools cannot be fully leveraged without rethinking organization and processes, however. This month, we look at ways SigmaTron International's facility in Chihuahua, Mexico, is evolving its inspection approach after validating the effectiveness of the automation it has been investing in over the past three years.

The facility serves customers in a variety of industries with projects ranging from low-volume, complex box-builds under 100 per day to printed circuit board assemblies in volumes of 40,000 per day. The bulk of production is in the thousands-per-day range. Consequently, there is a mix of dedicated production lines run continuously and shared production lines with multiple changeovers per day.

Over the past three years, barcode scanning capability has been added to manual inspection, automated optical inspection, in-circuit test, programming, functional test and final inspection, enabling the manufacturing execution system (MES) to implement enforced routing and automate quality data collection and trends analysis. As automation improved quality, the inspector base was reduced to 20 inspectors from 30.

The current state model had 20 inspectors/process auditors in two shifts engaged in a variety of activities, including doing process audits on SMT, automated inspections and final assembly, as well as testing PCBAs per AQL tables and documenting release model changes. They also audited material stored at the point of use in secondary assembly lines. Trend analysis suggested further realignment was necessary, however.

Analysis of the past two years of quality data showed zero defects in finished goods audits. There has been no wrong-component defect in the past three years. Auditing activity has also changed. Previously, process audits had included verifying setups. The majority of the SMT lines had been upgraded to smart feeder setups, where the feeders automatically validated that the correct reel was loaded. Auditors may still do audits on release parts for new product introduction or feeder carts loaded offline when there is a need for fast changeovers. However, 100% verification has been eliminated from SMT lines using smart feeders.

The future state model reduced the number of inspectors to 10 positions and redeployed the other 10 into other needed positions. Finished goods inspectors have been eliminated as a job position. The data highlight that automation and its associated tighter process control reduce the need for manual quality control activities, while

highlighting the benefits of preventative quality assurance activities associated with new product introduction (NPI) validation, customer-driven engineering changes and processes with fewer automated controls.

In this example, quality trend data drove the realignment strategy by demonstrating where automation eliminated the need for manual inspection. The electronics manufacturing services (EMS) environment has inherent quality challenges, driven by the number of customers and the variety of projects each facility must manage. Enforced routing and automated inspection technologies ensure consistent controls that are not impacted by changes in product mix are in place.

There has long been debate on quality assurance versus quality control. Because quality assurance focuses on preventing defect opportunities, Lean philosophy treats it as a value-added activity. Quality control, which uses inspection to prevent defects from escaping the factory, is considered a necessary, but non-value-added, activity. Both are necessary in today's manufacturing environments because smaller product footprints, narrow process windows, and high-mix production environments pose higher risks of defects. Investing in automation that eliminates the need for headcount associated with non-value-added inspection activities enables personnel to focus on the value-added side of quality activities while systems focus on identifying any defects that do slip through. It reduces the cost of quality over time and improves efficiency and throughput.

ALVARO GRADO is general manager at SigmaTron International's (Chihuahua, Mexico) facility (sigmatronintl.com).

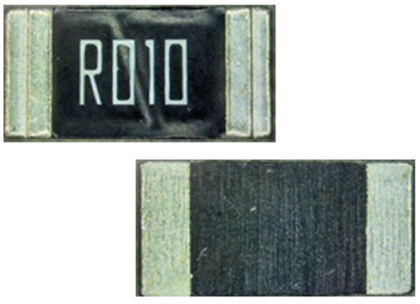
PCD&F

SCHMOLL RELEASES XRA³ X-RAY

Schmoll XRA³ series x-ray machines come with 70kV microfocus x-ray source and high-resolution CMOS detector, detects PCBs and enables precise referencing and processing by integrated drilling units. Are for multilayer and innerlayer PCBs. Patented flex-table mounting plate is said to ensure PCB registration due to full-surface vacuum system. Linear motor technology in all axes for system availability and minimal maintenance costs. Comes as manual or fully automatic. XRA³ handles panels up to 710 x 762mm; XRA³ XXL handles 813 x 1219mm.

Schmoll

schmoll-maschinen.de

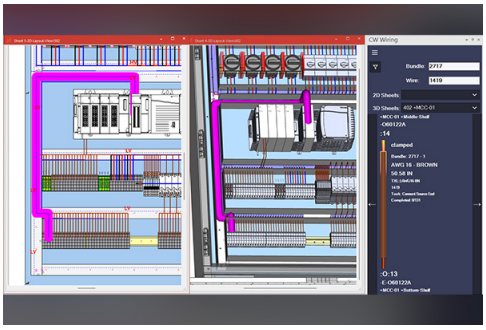


STACKPOLE CSSU2512 RESISTOR

CSSU2512 has a 5W power rating in standard 2512 footprint, using an all-metal element and thermally conductive structure to minimize resistance heat-rise. Delivers 5W performance comparable to lower-rated 3W chips, with resistance options from 1–10mΩ, 1% tolerance and 50ppm TCR.

Stackpole Electronics

seielect.com



ZUKEN PANEL BUILDER 2026 FOR E3.SERIES

Panel Builder 2026 is the newest update to the E3.series manufacturing module, adding expanded controls for wiring preparation, assembly coordination and multi-build management. Supports tracking of repeat panel builds under a single project record and aligns wire-processing outputs with Wiring Task Manager data. Includes Skip Attribute filtering for variant-specific exclusions and pin-level wire sorting for refined instruction sequencing. Technicians can toggle between 2-D and 3-D sheets during wiring tasks, with enhanced task filtering and progress indicators for complex assemblies. Assembly workflows permit loading updated .e3s data without clearing existing tasks.

Zuken

zuken.com

CA

A.P.E. INTRUDER BGA REWORK STATION

Intruder is a complete hot air BGA rework station with split vision placement/removal capability. Comes with own separate computer (control) station. Features integral split vision placement and removal capability.

APE

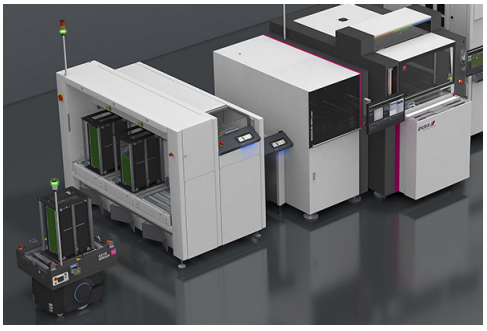
ape.com

ASMPT SIPLACE V PLACEMENT PLATFORM

Siplace V placement platform has a new machine frame and efficient linear drives and measuring systems with increased resolution. Placement heads can now be changed during operation via a central head interface. CP20 placement head places up to 52,500cph with a precision of 25µm @ 3σ). Switches between collect-and-place, pick-and-place and mixed modes via software. Twin VHF placement head handles parts up to 200x150x28mm with up to 100N. Handles components down to 016008M. Come in single or dual gantry versions and can be configured with single or dual conveyors.

ASMPT

asmpt.com



ASYS VEGO GENS HANDLER

VEGO GenS handler has modular design and up to 20% faster cycle time than previous models. Transport speed is up to 50% faster and speed range 10x greater. Stores 5x more program memory and 15x more data. Uses up to 100% less compressed air and reduces energy consumption 20% due to use of fewer pneumatic components. Software scales and upgrades on demand. Is self-learning and intuitive.

Asys

asys-group.com

CENCORP 1500 OF EVO 2 ODD-FORM PLACEMENT

1500 OF EVO 2 odd-form placement machine features large feeder bench capable of handling up to 24 different components in all sizes. Average placement speed is 1.9cps with a 400mm pick-and-place cycle using radial components. Robust gantry enables semi-press fit capability with assembly forces up to 600N with full force monitoring during placement process. Exchangeable feeders available for axial, radial and tube feeders. All existing PMJ or Cencorp feeders are compatible. Equipped with software for online CAD import, MES connectivity and traceability.

Cencorp

cencorpautomation.com

INDIUM SIPASTE C312HF SOLDER PASTE

SiPaste C312HF halogen-free, cleanable solder paste is for fine-feature printing. Designed with Type 7 powder for aperture sizes down to 60µm, it enables fine-feature printing in advanced system-in-package applications. Is said to offer class stencil print transfer efficiency and stencil life with consistent printing, response-to-pause, and reflow performance. Post-reflow flux residue can be cleaned with a standard cleaning process using semiaqueous chemistries or a saponifier, or it can be used as a standard no-clean paste in processes where post-reflow cleaning is not required. Offers slump resistance, low voiding across all components, minimal stencil cleaning during printing, a wide reflow profile window, and wets to various metallization. Is specifically designed for fine-feature printing with fine powders ranging from Type 5 to Type 8.

Indium Corp.

indium.com

JUKI RS-2 COMPONENT MOUNTER

RS-2 offers high-speed placement up to 50,000cph, aided by laser sensor closer to the board and reduces travel time from pick-up to placement. Height of laser sensor on 8-nozzle Takumi head automatically adjusts based on height of each component being placed, Component height can be selected from six levels: 1, 3, 6, 12, 20, and 25mm. Handles various component shapes, including BGA, SoP and QFP, ranging from 03015 to sizes up to 74mm square or 50mmx150mm, with placement heights accommodating up to 25mm. RF feeder supports up to 112 feeder units (front and rear combined). Is for multi-product, small-lot production with minimized setup times. Coplanarity sensor detects floating and BGA ball deformation to prevent placement of defective components.

Juki Automation

juki.co.jp

KEIRON LIFT PRINTER

LiFT printer offers stencil-free paste application for component assembly. Unlike a traditional stencil of a jet or ink printer, uses a fully digital, contactless process, for precision, repeatable results down to the nanoliter level. Built-in solder paste volume metrology (SVPM) reduces need for additional inspection. Can handle deposits down to 01005.

Keiron Technologies

keirontechnologies.com

MIRTEC TAL 3D SCAN

TAL 3D Scan inspection module attaches to MV-6 Omni 3-D AOI, performing pre-inspection while main 3-D AOI operates. From a system-wide perspective, this is equivalent to inspecting two PCBs simultaneously. Consistently operates faster than the MV-6 Omni, effectively converges inspection time to zero within overall manufacturing process. Inspects components higher than 5mm, which typically takes longer to inspect beforehand, significantly reducing total inspection time.

Mirtec

mirtec.com

MYCRONIC BA 01 SMALL DOT EJECTOR

BA 01 small dot ejector for MY700 jet printer accommodates solder paste deposits from 180 to 330µm in diameter with a volume ranging from 1 to 4nl. Reportedly reduces risk of overprinting, solder bridging and solder balls. Supports pitch sizes down to 0.35mm. Offers software-controlled variability, delivering multiple dot and volume size using only one applicator.

Mycronic

mycronic.com

MYCRONIC MYPRO A41DX, A41SX PLACEMENT MACHINES

MYPro A41DX and A41SX placement machines handle boards up to 1,000mm x 609mm in size, 12.5mm thick and up to 10kg using new T1000 conveyor. MX7 head places a significantly larger range of components of any size with perfect precision on a large substrate. Full backward compatibility with existing feeders and magazines. A41DX-17 has a rated speed of 49,000cph and includes standard electrical verification of components for quality assurance.

Mycronic
mycronic.com

MYCRONIC GENI 3-D METROLOGY INSPECTION

GenI offers true 3-D metrology inspection and full measurement traceability. Is said to complete automatic AOI program generation setup in 10 min. or less with CAD data from Mycronic pick-and-place, permitting inline AOI without production stoppage during new product introduction. AI-powered, library-free inspection eliminates need for inspection libraries, ensuring consistent results regardless of programmer expertise. Inspection program based on first assembled board; no need for golden or perfect board.

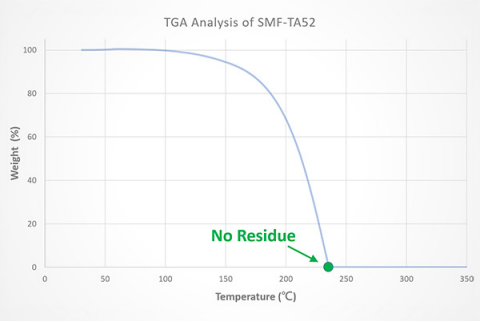
Mycronic
mycronic.com

NORDSON SQ5000PRO MULTI-FUNCTION INSPECTION

SQ5000Pro combines AOI, SPI and CMM-grade metrology in a single inline system. Platform captures dimensional, positional and volumetric data in seconds. Two new 500-series multi-reflection suppression (MRS) sensors – HR and HS variants – are said to deliver distortion-free imaging on reflective and complex surfaces. Unified architecture is suited for applications including fine-pitch SMT, advanced packaging, 0201 metric components, sockets and connectors and precision geometry measurement. Coordinate measurement software suite enables CMM-level accuracy at production throughput, while the updated AutoProgram tool leverages AI to reduce setup time and identify features and inspection regions.

Nordson

nordson.com

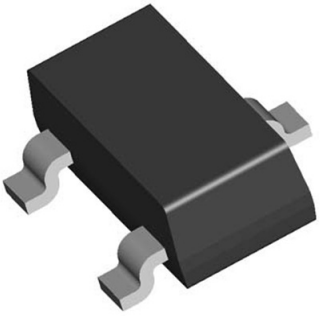


SHENMAO SMF-TA52 TRANSIENT ADHESIVE

SMF-TA52 zero-residue transient adhesive is for assemblies using formic acid reflow. Holds solder preforms, dies and wafers in place during heating and reportedly breaks down fully at peak reflow, eliminating post-process cleaning. Supports dispensing and jetting and is compatible with formic acid reflow, vacuum reflow and silver sintering. Is SVHC-free, halogen-free and no-clean, meeting requirements common in semiconductor packaging and power-module production.

Shenmao Technology

shenmao.com



TOPLINE ZERO OHM JUMPERS AND DUMMY COMPONENTS

Zero Ohm jumpers and dummy components come in multiple body sizes and pitches for routing changes. SnPb and lead-free versions ship from stock for training applications and design modifications. Components support post-production changes, replacement of obsolete parts and routing adjustments on single-sided layouts. SOT23 Zero Ohm jumper package enables board-level routing changes without generating a new layout file.

TopLine Corp.

topline.tv

VISION ENGINEERING PROTEQ VISO 3-D DIGITAL STEREO MICROSCOPE

ProteQ VISO 3-D digital stereo microscope has integrated autostereo display for eyepiece-free viewing for inspection and design workflows. Twin cameras and eye-tracking generate true 3-D images on a flat screen, supporting precision tasks in electronics, medical devices, micromolding and aerospace components. Includes upright viewing angle, adjustable display and a 10:1 zoom range, with option to switch between 3-D and 2-D modes for individual or group evaluation. Digital tools include image and video capture, picture-in-picture, overlays, annotation and measurement, with integration options for external software and connected platforms.

Vision Engineering
visioneng.us

PCB WEST 2026

Conference & Exhibition

SAVE THE *Date*

CONFERENCE:
September 29 - October 2
EXHIBITION:
Wednesday, September 30

Santa Clara Convention Center

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