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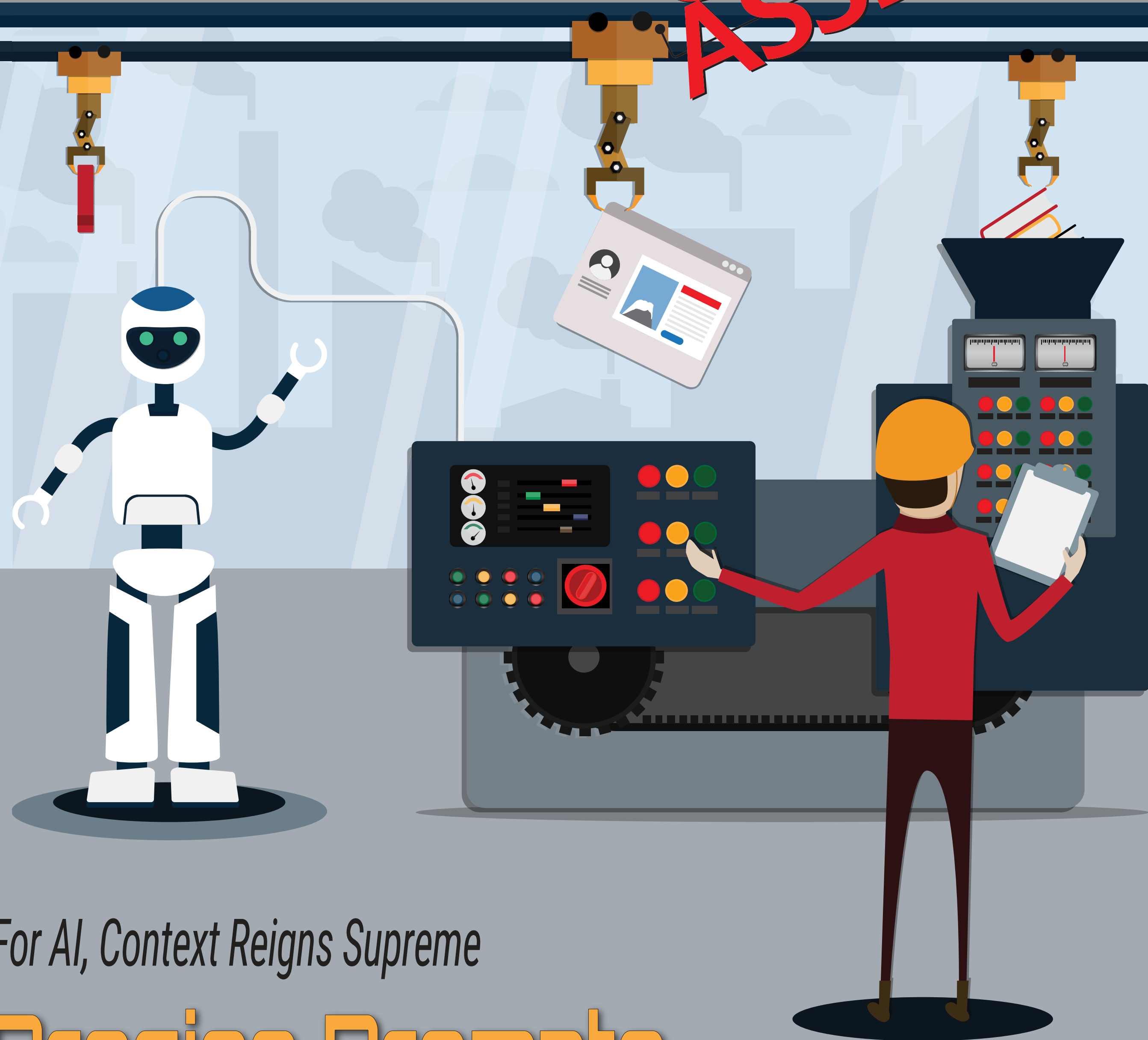

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FEBRUARY 2026 • VOL. 43 • NO. 2

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PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is published monthly by Printed Circuit Engineering Association, Inc., PO Box 237, Portsmouth, NH 03802. ISSN 1939-5442. GST 124513185/ Agreement #1419617.

THE **ROUTE**

The Hidden Cost of AI: When Data Centers Devour Your Supply Chain

ANALYSIS OF ARTIFICIAL intelligence's place in the world is as ubiquitous (and occasionally, insufferable) as those chatbots cluttering up many businesses' websites. Not unironically, then, am I adding to the din.

More than 5,400 data centers operate in the US alone today, including more than 50% of the world's hyperscale AI facilities. Last year alone, global spending on data centers reached an estimated $580 billion and is expected to continue to grow at a 28% clip per year through 2030, with AI investments alone reaching $200 billion by 2030. Assuming much of that investment is financed, interest charges from that capex could exceed $1.5 trillion.

Much of the impact – realized or projected – has focused on energy consumption and location, and for good reason. While local folks might want access to AI so they can make quick work of otherwise time-intensive projects, they tend not to want to see their energy bills spike to underwrite the data center across town.

The average data center holds 2,000 to 5,000 servers, with smaller ones ranging from 500 to 2,000. According to the International Energy Agency, worldwide electricity consumption for data centers is projected to double by 2030 to around 945TWh, which translates to about 3% of total global electricity consumption. Given how much developed economies rely on computing power, that doesn't seem too bad.

However … during that span, data center electricity consumption is expected to grow around 15% per year, which is more than four times faster than the growth of total electricity consumption from all other sectors. And in areas with high numbers of these server farms, consumer pushback is already being felt.

Then there's the comparisons to the dot-com bubble, when high demand for the nascent Internet industry spurred mass overbuying of – that's right – servers, culminating in Cisco, then (and now) the largest network infrastructure OEM, taking a $2.25 billion inventory write-down in a single quarter. (In layman's terms, that meant Cisco determined the market value of the finished goods it had on hand was over $2 billion less than what they originally paid. Ouch.)

Amid the hue and cry, less recognized are the downstream material shortages threatening to jack up prices on all kinds of products. And for those of us who recall the material shortages of the 1990s, forgive us if we think the potential financial reckoning might already be at hand.

AI datacenters will use some 70% of all high-end DRAM production in 2026. Component suppliers are changing up their processes, cutting lower-margin product to free capacity to feed AI demand. DDR4 memory is falling victim, as major component makers sunset those parts. Memory prices shot up about 50% in the fourth quarter, and TrendForce sees prices rising by another 70% in 2026 due to persisting shortages.

Hope you bought that new computer ahead of the Windows 11 switch, because it is probably about to become a whole lot more expensive. "Memory shortages are affecting the entire industry, and the impact will likely reshape market dynamics over the next two years," said Jitesh Ubrani, research manager, IDC, in the research firm's quarterly PC industry forecast.

The surge has laminate vendors and their suppliers on edge, too. Supplies of BT resin and T-glass, used in materials for much of the AI chip substrates and boards, are already strained. Nittobo, the Japanese company that holds most of the patents and manufacturing expertise for T-glass, and Mitsubishi Gas Chemical, the largest supplier of BT substrate raw materials, are both warning of sold-out conditions into the second half of 2027.

The knock-on effect is not just that PCB designers must adjust their component BoMs, but fabricators need to consider different glass fabric styles. A lot of conversations need to take place, in short order.

As AI effects are throughout the supply chain, whether humanity is unlocking the doors to its own replacement might be the least of our concerns.

mike@pcea.net
@mikebuetow

P.S. A warm welcome back to Andy Shaughnessy, our former editor who is returning to become our first content architect! Be sure to say hi to him at PCB East this year. The annual conference (registration is open) and exhibition takes place April 28-May 1, at the DCU Center in Worcester, MA. Sign up now!

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

Siemens Acquires Aster Technologies to Expand PCB Test Engineering Capabilities

PLANO, TX – Siemens has acquired Aster Technologies, a provider of printed circuit board assembly test verification and engineering software, expanding its capabilities in design for test and manufacturing readiness for complex electronic systems. Financial terms of the transaction were not disclosed.

The acquisition brings Aster's shift-left DfT and test coverage analysis into Siemens' Xpedition and Valor software portfolios, part of the Siemens Xcelerator platform. The integration is intended to help electronics manufacturers identify test coverage gaps earlier in the PCB design process.

By combining Aster's test engineering tools with Siemens' existing design for manufacturing capabilities in Valor and PCB design workflows in Xpedition, Siemens aims to strengthen the digital connection between PCB design, assembly and test.

Siemens said the move addresses increasing test challenges driven by higher electronics complexity, including advanced automotive systems, 5G integration and denser PCB assemblies.

Unitech PCB Establishes First Thailand Manufacturing Base in Thailand

BANGKOK – Unitech PCB has opened its first manufacturing facility in Thailand, establishing a new production base at the S Ang Thong Industrial Estate.

The facility spans approximately 8.4 hectares and will support production of HDI printed circuit boards for export markets. The site is intended to serve as a regional manufacturing hub as Thailand continues to expand its role in the global PCB supply chain.

Unitech PCB's new manufacturing facility in Thailand.

Thailand is currently the largest PCB manufacturing base in ASEAN and ranks fifth globally, supported by established electronics infrastructure, an experienced workforce, and export-oriented industrial policies. The addition of Unitech's facility increases regional capacity for advanced PCB fabrication as manufacturers continue to diversify production across Southeast Asia.

Defu Abandons Circuit Foil Luxembourg Deal

WILTZ, LUXEMBOURG – Chinese copper-foil manufacturer Jiujiang Defu Technology has abandoned its planned acquisition of Circuit Foil Luxembourg after Luxembourg authorities imposed conditions that would have prevented Defu from obtaining operational control of the company.

The transaction, announced in July and valued at approximately $190 million, was subject to foreign investment screening due to Circuit Foil Luxembourg's strategic role in Europe's electronics supply chain. Defu said regulators would only approve a minority ownership structure, with limited voting rights and no authority over management decisions.

According to Defu, the imposed conditions also restricted influence over corporate governance, intellectual property, trade secrets, and other sensitive operational areas, fundamentally altering the scope of the deal. As a result, the company opted to terminate the agreement.

The acquisition was reviewed under Luxembourg and European Union foreign investment regulations. Luxembourg's Ministry of the Economy confirmed that it issued a conditional authorization on Jan. 8, but declined to disclose further details, citing confidentiality requirements related to critical industries.

Following the termination, Defu said it plans to refocus its expansion efforts within China. The company announced its intention to pursue a 51% stake in Huiru Technology, a domestic producer of electrolytic copper foil with annual capacity of approximately 20,000 tons. Transaction pricing will be determined following completion of due diligence.

Zhen Ding Technology to Launch Thailand JV, Add to PCB Fab Capacity

BANGKOK – Zhen Ding Technology plans to expand its printed circuit board manufacturing presence in Thailand through a joint venture with Saha Pattana Interholding following government approval of more than $2 billion in new PCB fabrication investments.

According to Thai authorities, the approved projects will add PCB fabrication capacity tied to Zhen Ding's existing Thailand campus, which began operations last fall. The new investment is expected to support large-scale production expansion as global PCB manufacturers continue to diversify manufacturing footprints in Southeast Asia.

Zhen Ding Technology is partnering with Saha Pattana Interholding, a publicly traded Thai investor and industrial park developer, on the project. The specific location of the new facilities was not disclosed.

The Thai government said the investment is expected to create approximately 5,600 jobs.

Hanza to Acquire EMS Provider BMK Group

GERMANY – Hanza in January completed its previously announced acquisition of BMK Group in a share-for-share transaction, expanding its European EMS footprint and adding scale in complex, high-reliability electronics manufacturing.

The transaction values BMK at approximately $193 million, based on Hanza's share price at signing. Under the agreement, BMK's three founders are expected to own about 27% of the combined company following completion.

The joint company has annual revenues of about SEK 10 billion ($1.05 billion) and 5,000 employees.

BMK is a European electronics manufacturing services provider focused on high-reliability and complex electronics, with operations in Germany, Israel, the Czech Republic, and China. The company was expected to generate revenue of approximately SEK 3.3 billion ($350 million) in 2025, with an operating margin of about 7.3%. Its services include engineering, prototyping, industrialization, manufacturing, testing and lifecycle support for industrial, medical and defense customers.

The acquisition significantly increases Hanza's presence in Germany, which is expected to become the group's largest operating cluster.

Voltatron Acquires Komitec

FÜRTH, GERMANY – Voltatron AG has acquired 100% of Komitec Electronics, expanding its electronics manufacturing services capabilities and adding capacity as part of its acquisition-led growth strategy. The transaction closed on Jan. 1.

The merged company will have 2026 revenue in the range of €47 million to €51 million ($55 million to $60 million) and an adjusted EBITDA margin between 7% and 10%.

Voltatron said the acquisition extends its value chain by adding electronics research and development capabilities alongside medium- and large-scale production capacity for electronic assemblies, devices, and systems. The deal also broadens the company's customer base and more than doubles available production space, increasing operational flexibility and redundancy.

The transaction includes a cash component as well as the issuance of new shares through a capital increase against contribution in kind. As part of the agreement, Komitec managing director Jochen Schmitt-Ruenhorst will remain in his role and become a long-term shareholder in Voltatron to support continuity and integration.

Foxconn Acquires Belkin and Subsidiary Brands for $866M

TAIPEI – Foxconn Interconnect Technology Limited (FIT), an affiliate of Foxconn, has agreed to acquire Belkin International for $866 million. The deal brings Belkin and its subsidiary brands, Linksys, Wemo and Phyn, under FIT's ownership.

The acquisition represents the first major move by FIT into operating established consumer brands, following a history focused on manufacturing and interconnect solutions. While the agreement has been signed, the transaction remains subject to approval by the US Committee on Foreign Investment, a process that has drawn heightened scrutiny following the US government's prior intervention in high-profile semiconductor and technology mergers.

Belkin founder and CEO Chet Pipkin will continue to lead the company, which will operate as a subsidiary of FIT following the transaction. "This move will accelerate our vision of delivering technology that makes the lives of people around the world better, more convenient and more fulfilling," Pipkin said. He added that the transaction provides access to additional manufacturing resources and capital to support operational efficiency and future investment.

Inventec Commits $136M to Expand Thailand Footprint

TAIPEI – Inventec plans to invest approximately $136 million to expand production capacity at its Thailand operations, reflecting accelerating demand from US customers shifting notebook manufacturing from China.

The investment will fund a combination of plant renovations, equipment upgrades, and the construction of a new factory and supporting infrastructure. Roughly $54 million is allocated for facility improvements and equipment, while about $82 million will be used to build the new production site.

The Thailand expansion is designed to support both notebook and server manufacturing. Demand from US clients has increasingly driven notebook production outside China, prompting higher utilization at both leased and company-owned facilities in Thailand.

While China remains the largest manufacturing base, Thailand now represents a low double-digit share of total notebook shipments, signaling a growing role in the company's global supply chain diversification strategy.

In the artificial intelligence server segment, most production continues to be based in Taiwan. A US manufacturing facility in Texas is scheduled to begin operations by the end of the first quarter, with mass production expected in the second quarter, positioning the company closer to North American customers.

Mycronic Acquires German PCB Test Probe Supplier ETZ

STOCKHOLM – Mycronic's Global Technologies division has acquired ETZ, a German manufacturer of test probes used in electrical testing of bare printed circuit boards.

ETZ supplies the majority of test probes used by the PCB test business line within Global Technologies, making probe development and production a core strategic capability. The company employs 34 staff and operates its manufacturing facility in Seesen, Germany.

In 2025, ETZ reported net sales of about $4.3 million, with roughly 85% of revenue generated from sales to Mycronic. Prior to the transaction, Mycronic held a 15% ownership stake in ETZ.

Following the acquisition, ETZ will be fully integrated into the PCB test business line within Global Technologies.

PCD&F

American Standard Circuits and **Sunstone Circuits** unified under the **ASC** brand family, introducing a refreshed corporate identity. The fabrication also added a high-precision via fill machine to its Oregon facility.

Amazon entered a partnership with **Rio Tinto** to source copper for data center components.

Dynamic Electronics said it will double its investment in its Thailand PCB manufacturing plant.

Pinnacle Technology Group rebranded as **PTG Electronics**, introducing a new name and visual identity.

Schweizer Electronic completed the sale of a 15% stake in its Jiangsu subsidiary to **Wus Printed Circuit**.

Taiyo Nippon Sanso plans to build an Advanced Electronics Materials Development Building, scheduled for completion in March 2027.

TSMC is accelerating its Arizona expansion, with 3nm mass production now expected to begin as early as 2027.

Wus Printed Circuit said it will invest $300 million to develop and mass-produce high-density optoelectronic integrated circuit boards for AI computing and autonomous driving.

CA

Absolute EMS formed a strategic partnership with **SIIX USA** to provide production support within SIIX's global manufacturing network.

Amber Enterprises India completed the acquisition of a majority stake in Pune-based **Shogini Technoarts**.

Axos Designs acquired a 30,000-sq. ft. manufacturing facility in Long Island City, NY.

Distron became the first US electronics manufacturer to deploy **Keiron's** HF2 LIFT-based precision solder paste printing technology.

EDAC registered with **PEZA** to establish an export-oriented electronics manufacturing hub in New Clark City, Philippines.

Mozambique broke ground on its first dedicated electronics assembly factory.

Rohde & Schwarz opened a larger Osaki office to expand automotive test, calibration, and local engineering support in Japan.

SRC Technologies Group secured a $1 million grant from **Missouri State University's** Jordan Valley Innovation Center to build a low-volume, high-mix electronics assembly line.

VDL Groep acquired **Sintecs** to strengthen its electronics manufacturing capabilities.

Yamaha Robotics integrated its German liaison office into **Yamaha Motor Europe's** robotics business.

PCDF


Don Cantow


Panos Angelopoulos


Sarmad Khemmoro

Altium appointed **Don Cantow** general manager.

Anduril named **Steve Mueller** printed circuit board designer.

Optical Gaging Products appointed **Panos Angelopoulos** president of global sales.

EIPC elected **Rico Schlüter** president and elected as vice presidents **Emma Hudson** of EHTC and **Thomas Michels** of Ilfa.

Siemens promoted **Sarmad Khemmoro** to senior director of product strategy for Electronics & Semiconductor.

CA


Angel Lopez


Ray Whittier


Josh Hollin


Jan Janick


Jonathan Molina


Casey Cooper


Tony Jepson


Greg Rowell


Barbara Koczera

AIM Solder appointed **Angel Lopez** technical support engineer for North America.

BAE Systems promoted **Ray Whittier** to operations affordability lead.

Benchmark named **Josh Hollin** senior vice president and chief technology officer.

Benchmark Electronics chief technology officer **Jan Janick** retired in January.

Jabil named **Jonathan Molina** engineering manager.

Koda Technologies named **Casey Cooper** director of digital engineering.

Libra Industries appointed **Tony Jepson** general manager of its Dallas, TX, electronics manufacturing facility.

Libra Industries named **Greg Rowell** global director of continuous improvement.

Microboard promoted **David Kleffman** to vice president, Engineering Solutions & Technology.

Texmac-Takaya Group named **Barb Koczera** Western regional sales manager.

Z-Axis promoted **Danielle Sklepik** to design engineering manager at its Phelps, NY, facility.


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Conference Registration Opens for PCB East 2026

PEACHTREE CITY, GA – PCEA has opened registration for the technical program for PCB East 2026, featuring more than 80 hours of in-depth electronics engineering training on circuit board design and assembly.

Rick Hartley, Susy Webb, Stephen Chavez, Karen Burnham and Tomas Chester are among the headliners of this year's conference. It will be held Apr. 28 to May 1 at the DCU Center in Worcester, MA. It features classes for every level of experience, from novice to expert.

The scope of classes ranges from the basics of design engineering, libraries and circuit grounding to more advanced fare such as power distribution, EMC, stackups, thermal management and DDR memory routing.

More than two-thirds of the presentations are new to the conference, including ones on DfM for ultra high-density interconnects (UHDI), designing in 3-D, advanced dielectrics for thermal PCBs, AI and time budgets for new projects.

New this year are two days of assembly tracks, offering in-depth circuit assembly basics and advanced assembly, including an all-day hand soldering workshop, plus a full day of supply chain and business management sessions.

The all-day Executive Management Forum on Apr. 28 will cover executive strategies for AI adoption, meeting workforce challenges and new PCB process selection for advanced electronics packaging.

"PCB East is the largest technical conference and exhibition for the electronics design, fabrication and assembly industry on the East Coast," said Mike Buetow, conference director, PCB East. "This year's event offers an array of experts in printed circuit design engineering and manufacturing, and a new emphasis on assembly."

Registration for both the technical conference and the exhibition takes place at pcbeast.com. Those who sign up by Mar. 27 can take advantage of the early bird special discounts for the conference.

PCEA Names Andy Shaughnessy Content Architect

PEACHTREE CITY, GA – PCEA in January named Andy Shaughnessy its first content architect. Shaughnessy, a veteran industry journalist and media personality, will be responsible for creating and overseeing PCEA's technical publications and media communications, including podcasts and video.

Andy Shaughnessy

Shaughnessy has been a writer, editor and journalist for 30 years. He has been covering PCB design and the EDA market since 1999, serving as associate editor and editor-in-chief of PCD&F Magazine from 1999-2007, prior to its acquisition by PCEA.

From 2007-2025, he was editor of I-Connect007's Design007 Magazine and the Design Newsletter, as well as an on-camera interviewer for the *Real Time* video program.

"Once we realized Andy was available, a reunion was obvious," said Mike Buetow, president, PCEA. "Our vice president of sales and marketing, Frances Stewart, and I worked with Andy years ago and have always been impressed with his passion, knowledge, and ability to connect with people of all backgrounds and responsibilities. We are thrilled to have him as a colleague again."

"I'm excited to be back working with Mike and Frances," Shaughnessy said. "Although some of the team is different, I know everyone in the company. How often do you get to start a new job at a company where you've known everyone for decades?"

Spring PCB Design Training Classes Scheduled

PEACHTREE CITY, GA – Registration is open for the PCEA Training Certified Professional Circuit Designer (CPCD) training and certification classes this spring.

Class dates are May 15, 22, 29, Jun. 5 and 12. Registration closes Apr. 16.

The 40-hour instructor-led course is designed for printed circuit engineers, layout professionals and other individuals currently serving in the design engineering industry or seeking to get into it.

The classes cover the gamut of printed circuit design engineering, from layout, place and route to specifications and materials to manufacturing methods. Schematic capture, signal integrity and EMI/EMC are also part of the comprehensive program.

Each class includes a copy of *Printed Circuit Engineering Professional,* a 400-page handbook on circuit board design, and the optional certification exam recognized by PCEA.

There are no prerequisites to enroll. Classes are held online and led by experienced instructors.

To enroll, visit pceatraining.net/registration.

PCB East Show Floor 95% Sold Out

PEACHTREE CITY, GA – The exhibition hall floor space for PCB East 2026 is more than 95% sold out.

The annual one-day exhibition will be held April 29, 2026, at the DCU Center in Worcester, MA. The exhibition is part of the PCB East conference, which takes place April 28 – May 1.

"We have seen tremendous interest this year, owing in part to our past history of turnout coupled with the move to the DCU Center, which is a high-end facility and offers big-city advantages at a more affordable cost to attendees," said Frances Stewart, vice president of sales and marketing at PCEA.

"Several major semiconductor companies such as AMD, Lattice Semiconductor, Microchip and Samtec are joining our traditional group of leading software developers and manufacturers as we build on our industry-leading events for electronics design and manufacturing," she added.

Companies interested in exhibiting should contact Frances Stewart at frances@pcea.net for details.

For more information about PCB East, visit pcbeast.com

PCEA CURRENT EVENTS

ASSOCIATION NEWS

Certification. The following recently passed the PCEA Certified Printed Circuit Designer exam:

- Dr. Amar Basu
- Ernesto Esparza

New Corporate Members

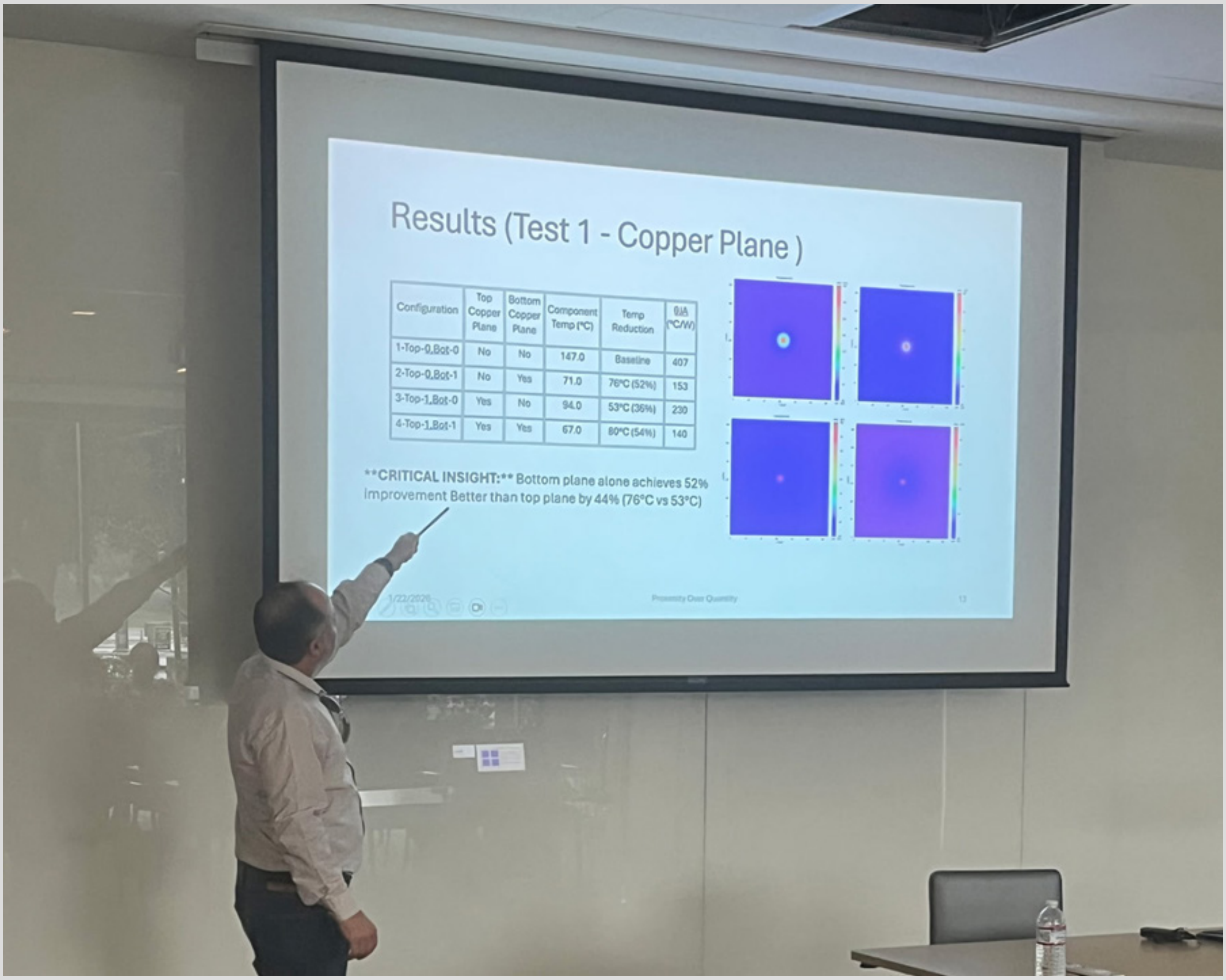
- Polyonics

Conferences. PCB Detroit will return to the campus of Wayne State University on Jun. 15-16, 2026. More details will be forthcoming at pcea.net/events.

Networking. The PCEA Discord server brings together engineers and designers from around the world on a private channel to discuss technical questions and career opportunities. To join, contact PCEA. Recent conversations covered high voltage boards, reflowing through-hole components, and differential signals.

CHAPTER NEWS

Orange County. Our January meeting featured design guru Ulisses Castro on the topic "Proximity Over Quantity: How Copper Plane Placement Outperforms Thermal Via Count in QFN Package Thermal Management." Thanks to Siemens for hosting.



Ulisses Castro describes copper plane test results at the Orange County chapter meeting.

Portland, OR. Our January meeting featured Anaya Vardya, president and CEO of American Standard Circuits, presenting on Thermal Management of PCBs, offering a unique perspective from a leading PCB fabricator. This session was the latest in our ongoing discussions about thermal management, providing valuable insights into real-world fabrication challenges and solutions that can enhance your designs. Our next meeting is Feb. 19 at 12 p.m. Pacific.

Richmond, VA. Our Feb. 12 meeting will be a Community Hardware Night, focused on connection, conversation, and real-world projects. Guests are welcome to bring a circuit board or hardware project they've worked on, or any other examples of the design or production of electronics. This informal gathering is designed to connect people who are involved in, or curious about, circuit board design and production. That includes designers, manufacturers, distributors, students, educators, and individuals or organizations interested in exploring how electronics design fits into their work or future plans. The time is 6-8 p.m. and the location is 1717 E. Cary St., Richmond. Come with a friend, classmate or coworker who may be interested.

Pizza will be provided by Mobius Materials; RSVP on LinkedIn or email Mike Burns.

PCB Design Software Sales Up 3.4% YoY in Q3, ESD Alliance Says

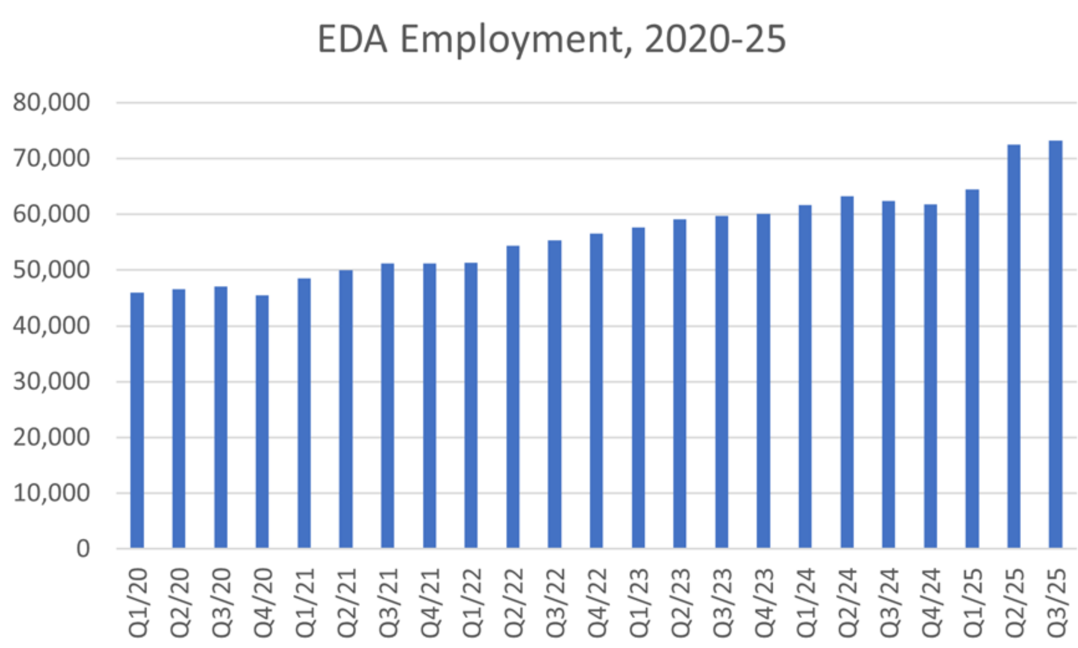
MILPITAS, CA – Printed circuit board (PCB) and multichip module (MCM) design software revenue rose 3.4% in the September quarter, reaching $466 million, the ESD Alliance announced today.

The four-quarter moving average, which compares the most recent four quarters to the prior four, rose 8.1%.

Electronic system design (ESD) industry revenue increased 8.8% to $5.6 billion in the third quarter, from $5.1 billion in 2024. The four-quarter moving average rose 10.4%.

“The electronic design automation (EDA) industry continues to report strong year-over-year revenue growth in Q3 2025,” said Walden C. Rhines, spokesperson for the ESD Alliance. “All product categories reported increases, with semiconductor IP and services showing double-digit gains. Geographic regions, including Americas, EMEA and APAC reported growth in Q3, with a double-digit increase in APAC.”

The companies tracked in the report employed 73,185 people globally in Q3, up 17.3% over 2024 and up 0.9% sequentially. It brings the sector’s total employment growth to 60% since Q1 2020 **(Figure 1)**.



EDA industry employment has grown 60% in fewer than six years.

Computer-aided engineering (CAE) revenue increased 9.1% to $2.1 billion. The four-quarter CAE moving average increased 11.6%. IC physical design and verification revenue increased 1.3% to $865 million. The four-quarter moving average for the category decreased 1.2%.

Semiconductor intellectual property (SIP) revenue increased 13.6% to $1.92 billion. The four-quarter SIP moving average rose 14.8%.

Services revenue increased 10.2% to $221.4 million. The four-quarter moving average rose 13.7%.

The Americas, the largest reporting region by revenue, procured $2.4 billion of electronic system design products and services in Q3 2025, a 3.4% increase. The four-quarter moving average for the Americas rose 10.3%. Europe, Middle East and Africa (EMEA) procured $675 million of electronic system design products and services, a 4.6% increase. The four-quarter moving average for EMEA grew 7.6%.

Japan's revenues decreased 11.5% to $264 million in Q3. The four-quarter moving average for Japan increased 2.4%. Asia Pacific (APAC) procured $2.2 billion, up 20.5%. The four-quarter moving average for APAC grew 12.8%.

Computers Adding Up

Trends in the US electronics equipment market (shipments only)

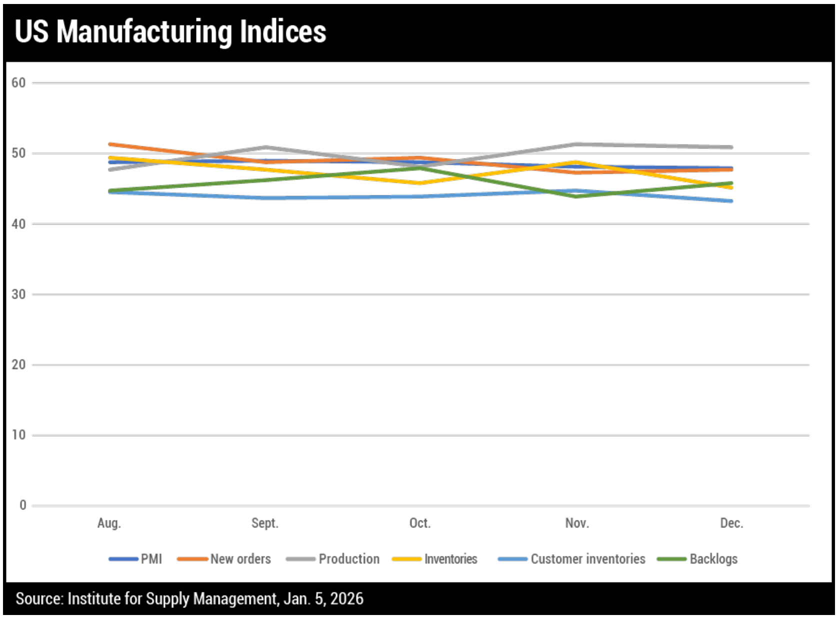
	% CHANGE			
	AUG.	SEPT.[r]	OCT.[p]	YTD
Computers and electronics products	-0.2	-0.1	0.5	4.8
Computers	-1.0	0.7	1.7	14.8
Storage devices	-0.2	-5.4	2.4	9.2
Other peripheral equipment	-7.6	-8.2	3.0	11.7
Nondefense communications equipment	2.5	1.7	-1.9	7.6
Defense communications equipment	-1.9	-2.4	2.4	-1.1
A/V equipment	-4.5	-3.9	-3.3	-4.0
Components[1]	-0.1	-0.2	0.1	4.7
Nondefense search and navigation equipment	-0.6	1.1	0.0	2.2
Defense search and navigation equipment	0.6	0.3	0.8	4.2
Electromedical, measurement and control	0.1	0.5	0.0	4.3

[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, Jan. 4, 2026

Key Components

	AUG.	SEPT.	OCT.	NOV.	DEC.
EMS book-to-bill[1,3]	1.26	1.31	1.26	1.17	TBA
Semiconductors[2,3]	21.7%	15.3%	27,2%	15.3%	TBA
PCB book-to-bill[1,3]	0.98	0.92	1.00	1.12	TBA
Component sales sentiment[4]	113.2%	121.6%	122.2%	120.1%	134.0%

Sources: [1]IPC (N. America), [2]SIA, [3]3-month moving average, [4]ECIA



Hot Takes

Worldwide **shipments of desktops, notebooks and workstations** reached 279.5 million units in 2025, up 9.2% year-over-year, supported by replacement demand and a stronger second half. Q4 shipments totaled 75 million units, up 10% compared to 2024. Tightening memory and storage supply is expected to weigh on growth this year. (Omdia)

Several major memory makers are **preparing to exit DDR4 in 2026**, with Samsung reportedly standing firm on its end-of-life schedule. (TrendForce)

Global **semiconductor sales** climbed 29.8% year-over-year to a record $75.3 billion in November, with month-to-month growth of 3.5%. (SIA)

A **shortage of high-quality glass cloth** used in BT substrates is threatening supply stability for advanced chips. (Nikkei)

North American EMS shipments declined 0.7% year-over-year in November and fell 3.6% compared with October. Year-to-date shipments were down 0.9%. Bookings dropped 4.1% year-over-year and 9.7% sequentially. Year-to-date bookings were 0.5%. (GEA)

The **global DRAM market** is experiencing a rare price spike. Tight supply, rapid AI expansion, and expectation-driven buying have pushed memory prices higher since the second half of 2025. (DigiTimes)

Global **PC shipments** grew 9.6% year-over-year in the fourth quarter, reaching 76.4 million units. Average selling prices (ASPs) are expected to rise in 2026 as vendors prioritize midrange and premium systems to offset higher component costs, especially memory. (IDC)

India approved $4.6 billion in subsidized electronic component manufacturing projects across eight states, aiming to boost local supply chains, generate $28.6 billion in output and employ about 34,000 workers. (India IT Ministry)

Taiwan's combined onshore and offshore PCB manufacturing output reached NT$244 billion ($7.73 billion) in the third quarter, a year-on-year increase of 7.2%. Cumulative output for the first three quarters totaled NT$667 billion ($21.1 billion), up 11.3% year-over-year. (TPCA)

Total **North American PCB shipments** increased 21.1% year-over-year in November, though volumes declined 4% sequentially. Year-to-date shipments were up 12.6% compared with the same period a year earlier. Bookings rose 23.3% from the previous year and slipped 0.7% sequentially, with year-to-date bookings increasing 16.6%. (GEA)

India is targeting PCB self-reliance with $2.4 billion in investment, aiming to attract 10 to 12 major producers, cut import reliance from 88%, and support a threefold industry expansion. (Elcina)

Delays and cancellations tied to Europe's Chips Act are casting doubt on the EU's goal of reaching 20% of global semiconductor production by value by 2030, exposing gaps in its industrial strategy. (EUToday)

China has mandated that **chipmakers source at least 50% of equipment** domestically for new capacity. (Reuters)

Global **smartphone shipments** increased 2.3% year-over-year to 336.3 million units in the fourth quarter, raising the total number of smartphones shipped in 2025 to 1.26 billion units. (IDC)

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The Next Great Technology Challenge: Designing without Rare Earths

As demand for AI and advanced electronics grows, the industry faces mounting pressure to reduce its reliance on scarce rare earth materials.

MUCH HAS BEEN written and said in all areas of the world and in all walks of life about the challenges facing the world of technology. Whether it is developing and harnessing AI (artificial intelligence), utilizing electric vehicles, reducing pollution to leave a smaller carbon footprint, or training the next generation of employees to fill the multitude of jobs required to manufacture the advanced technologies that all the above will require, the number and magnitude of all these challenges is staggering. It is nothing, however, compared to the granddaddy of them all: creating the next generations of technology without depleting rare earth minerals.

Rare earths are front-page news today, but regrettably the focus is more toward geopolitical wrangling among countries that have them and those that do not. But all the saber-rattling among competitors fails to address the root challenge: how can new technologies be developed that perform the functions we want while using far less – or no – rare earths?

First, what are rare earth minerals? They include minerals that most people have heard of, such as cobalt, lithium, manganese, graphite, and silicon derived from quartz. There are far more than those, however, most with names that are hardly household: neodymium, praseodymium, dysprosium, terbium and samarium, to name a few, are among the ones used to form industrial-quality magnets, sometimes for high-heat applications. These can be found in the battery of just about any hybrid or electric vehicle.

And then there are rare earth elements, such as yttrium, europium, cerium, lanthanum and gadolinium among them, each used in different applications ranging from LED television and smartphone screens to MRI displays. Besides these rare earth minerals/elements, there is ever-increasing demand for other critical metals such as copper, silver, gold, indium and nickel.

By leveraging the above, advanced technologies have been developed and refined into highly manufacturable devices. As the name indicates, however, "rare" earth minerals, elements and metals are limited in supply and require a disproportional effort to extract and refine. When "rare" is combined with "disproportional effort," and then "geopolitics" is added, the mix is a problematic combination that at some point will warrant a full-court press to meet the challenge of developing new technologies that do not deplete rare earths, are easier to extract, and reduce geopolitical saber-rattling for all concerned.

While replacing rare earth minerals in electronics and technology is an increasing challenge, it by no means will be a quick or easy process, especially if Big Tech is less concerned than it should be. This challenge, to me, is eerily similar to the late 1990s when the European Union (EU), via edict, banned lead in most electronics. Industry screamed it could not be done, but then the R&D commenced, and within a decade, lead was virtually eliminated from electronics. The only difference between then and now is that there is no entity like the EU to decree it shall be done.

Another similarity to the lead-free electronics initiative is the number of end-applications and industries – from critical high-reliability aerospace and military systems to consumer-oriented fare – competing for rare earths. Back in the 1990s, aircraft and autos were beginning to become electronics-rich. The demand for personal computers and cellphones was exploding, and telecommunications and server growth were exponential. Today, electronic vehicles of all types and sizes, home and garden tools powered by batteries, and server farms to support AI are all growing leaps and bounds, growth that looks to continue in the foreseeable future. All of this puts more demand for rare earths.

Possibly, the current geopolitical environment will result in a gauntlet being thrown down. Too often in contemporary politics, it is “ready, shoot, aim,” and if that approach results in rare earths being accessible to only a few countries, technologies that do not require them will then need to be developed. With hope, it will not come to that, and entrepreneurial technologists will see benefits that warrant the herculean effort to design out rare earth minerals.

However, as we all think about the challenges we have and the resulting opportunities they may create, replacing rare earth minerals in electronics and technology in general should be high on the list. High on the list of challenges and needs, but equally, it should be high on the list of opportunities that will create future profitability and the well-being of the planet.

PETER BIGELOW has more than 30 years’ experience as a PCB executive, most recently as president of FTG Circuits Haverhill; peterbigelow@msn.com. He is vice chair of the PCEA PCB Management Symposium, taking place April 28 at PCB East.

Do You Have a 2026 PCB Buying Strategy?

A PCB buying strategy shifts focus from unit price to total cost, design discipline and supplier governance.

THIS IS *NOT* the year for buyers to accept PCB price increases blindly. This is the year to buy PCBs like a professional who understands the job isn't just about placing orders; it's about controlling total cost of ownership while protecting delivery, quality and continuity.

Here's how I believe board buyers should approach 2026, including what to change in your quoting process, how to structure your supplier base and how to use logistics and design to reduce costs. These are concrete buyer moves you can implement immediately.

Stop comparing PCB quotes and start comparing total cost of ownership. Most buyers still shop boards like it's 2019; i.e., comparing unit prices, choosing a vendor and putting off dealing with shipping and tariffs until later. In 2026, that approach will have your company bleeding money.

Assuming the quality and delivery are the same with every vendor, the total cost of ownership (TCO) for PCBs is

Board price + Freight to deliver + Tariff impact = TCO

Then buyers should require every PCB quote to clearly spell out three things: board price, logistics and tariff assumptions.

Board pricing should be quoted Ex-Works or FOB origin and include unit pricing at the requested volume, two to three realistic volume breaks, and separate line items for NRE and electrical test.

Logistics should be quoted across multiple scenarios – standard air (three to five days), air cargo (five to 10 days) and, where timing allows, sea freight (five to eight weeks).

Finally, tariff and duty assumptions must be explicit, including the country of origin and the value basis being used to calculate any applicable tariffs.

Why should you insist on this? Because some board suppliers will get creative as they may try to win a quote by shifting money between a low unit price that has a high freight cost, a lesser tooling charge with an inflated production price or tariff costs applied to the wrong incoterm, costing you more unnecessarily. This detailed comparison among your vendors will make pricing fair and transparent.

Your biggest cost lever in 2026 is design discipline, not negotiation. You can negotiate a few percentage points off PCB pricing, but a design change can remove 10–25% from the right boards, especially when metal and laminate prices are climbing.

I'm not advocating mass redesigns. I'm telling you to create a targeted, buyer-led cost-takedown program with engineering on the small set of part numbers that drive most of your annual spend.

How? Build a "top 10 cost takedown" list. Start by identifying your top 10 PCB part numbers by annual spend or margin sensitivity, then run a structured review with engineering and your primary fabricator. The sooner this happens, the more leverage you have.

Copper is usually the first place to look. Too many designs carry extra copper simply because they always have. Challenge whether heavier copper is required everywhere, or whether localized thermal performance can be achieved through stitching vias or layout changes. It's also worth revisiting hole wall copper requirements; many are legacy specs that haven't been questioned in years.

Surface finish is another quiet cost driver. ENIG should not be the default. In many cases, OSP or HASL will meet assembly requirements just fine, and hard gold fingers often get specified out of habit rather than necessity. Buying premium finishes because "that's what we've always done" is one of the most expensive mistakes buyers make, especially when gold prices move, as they inevitably do.

Layer count deserves equal scrutiny. If you have repeatable six-layer designs that could realistically be engineered into four-layer versions, 2026 is the year to explore it. Reducing layer count lowers laminate and copper usage and can improve yields. Not every design will qualify, but even one or two high-volume parts can produce meaningful savings.

Quotes should also include the panel drawing and utilization percentage. Excessive rail width, inefficient panelization, or a fabricator that doesn't volunteer a better layout can quietly inflate cost. In those cases, you're paying for air and scrap rather than boards.

Finally, be deliberate about where X-outs are acceptable. For certain products, permitting controlled X-outs can unlock price relief during yield-challenged periods. This must be governed by part number and policy, not chaos, but it's a real lever when used correctly.

These are the distinctions between routine board buying and professional procurement. Experienced buyers don't just negotiate price; they use design discipline and acceptance policy to control cost.

Figure 1. Effective PCB procurement in 2026 depends on total cost visibility, supplier discipline and structured buying strategy.

Build a vendor bench and use it, even if you don't want to switch. Let me be blunt: if you only quote your incumbents, you are training them to raise prices with confidence. (Buyers: repeat this line again to yourself out loud.)

In 2026, every serious PCB buyer needs to maintain two qualified production sources for each core technology bucket that accounts for 60% of your business, and two quote-ready challengers to keep warm with the 40% balance of your spend.

Quoting is not betrayal. Quoting is governance.

Quoting "for fun" is a 2026 survival tactic. Even if you're happy with your vendor, quote competitors. Why?

- It validates your current pricing (best case).
- It forces your incumbent to stay sharp (most common).
- And sometimes you discover a better fit – price, lead time, service – without even trying.

Visit key suppliers and make sure they know you're watching. Supplier visits aren't just about relationship building. They are more about operational oversight. The greater the annual spend with a vendor, the more likely you are to see them, *even if* they are halfway around the world.

The worst thing a buyer can say is "I didn't know you could build that." Knowing what a vendor can and cannot do will save you money, along with the associated headaches that come with supplier ignorance.

This is how you go into 2026 with a plan instead of a prayer. By carrying out these steps, 2026 becomes an opportunity, a year when disciplined PCB buyers separate themselves from mere order placers. And your company will be one of those with a real buying strategy, protecting your margins while everyone else complains about price increases.

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as the founder of a leading distributor. He is cofounder of DirectPCB (directpcb.com); greg@directpcb.com.

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Dashboards and Controlled Chaos

In an EMS environment built on controlled chaos, dashboards help program managers catch problems early and keep accounts on track.

THE ELECTRONICS MANUFACTURING services (EMS) industry is controlled chaos by design. The basic EMS value proposition is that outsourcing relieves original equipment manufacturers (OEMs) of manufacturing challenges. The EMS provider covers fixed costs during manufacturing and carries the associated inventory costs on its balance sheet. Market slowing down? Revise your EMS provider's forecast. Market improving? Tell your EMS provider to pull some production in. Engineering challenges? Send your EMS provider a set of engineering change orders (ECOs) as the team determines what needs to change. The OEM side of the equation has the chaos part of the business model down. Even when things are running smoothly, the number of unplanned emails and calls in keeping projects on track is a significant part of the program management team's daily activities. When more of the day gets consumed than planned, activities designed to control the chaos may not get done.

This underscores the importance of having a control system that makes sense for managing that chaos. Walk a production floor, and you'll see control limits established for critical processes such as solder paste deposition and reflow. If a process exceeds those limits, either the monitoring software in that equipment or the inspection equipment immediately following that process tells the operator a problem has developed so that the operator can identify the root cause and bring it back within control limits before significant amounts of defective products are built. Program managers need to create control systems that provide that intelligence as well. A dashboard is an effective way to highlight developing issues when they are small.

The basics of a good dashboard include:

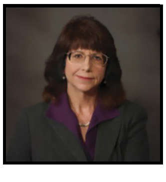
- **It educates.** You can't expect customers to change behavior if you can't show them why that behavior is costing them unnecessary money. Dashboards need to be data-driven, and those data need to be able to support the program manager's business case.
- **It needs to highlight exceptions.** We have the power to automate more real-time data than we can comprehend, especially in a chaotic environment. Consequently, the dashboard's control system must prioritize data requiring immediate attention.
- **It provides automated snapshots of critical account metrics.** The right dashboard template may vary by business size or even by business type, but typically it includes quality and on-time delivery metrics, contribution margin or some other form of profitability measurement, sales to forecast, inventory trends, PPV trends and accounts receivable status. For accounts involving dedicated lines, utilization metrics may also be

included.

- **It is graphical, so trends are easy to see.** We have become a very visual society, and program management time is at a premium. A bar graph is far more meaningful than a report in showing trends. Consequently, dashboards should be visual enough that metrics can be evaluated almost immediately.

That said, a dashboard is just part of a program manager's toolkit. EMS providers don't build superior quality products by just inspecting quality in. They develop efficient processes, define inspection points within those processes where issues may be likely to occur, and adjust the process if defect opportunities or inefficiencies are developing. Program managers should envision account strategy before the dashboard and underlying control system is designed, and over time, existing dashboards should be evaluated for relevancy. What common problems are occurring in accounts? What customer behaviors are creating unnecessary costs? What issues tend to slip under the radar until they create big problems? What goals are being set for the account by either the customer or the EMS provider? How will dashboard metrics be used in changing that dynamic? How frequently do those metrics need to be measured? Which timeline view is most effective for understanding trends in each metric? In short, design the tool with the end-users in mind. Automate the data collection process so it occurs at an appropriate frequency and then use the data to drive actions within the account.

As we begin a new year, take the time to evaluate whether the dashboard currently used or the lack of a dashboard is making it difficult to control chaos. Technology improves daily. AI adds significant options for fast trends analysis and exception reporting. Most importantly, consider whether account control activities are based on an issues-driven, reactive approach or on a clear strategy to help the customer understand the elements of an optimal relationship. The time invested in developing a partnership strategy for each account, along with the tools needed to track when the relationship is trending out of control, pays for itself in less chaos.



SUSAN MUCHA is president of Powell-Mucha Consulting Inc. (powell-muchaconsulting.com), a consulting firm providing strategic planning, training and market positioning support to EMS companies and author of *Find It. Book It. Grow It. A Robust Process for Account Acquisition in Electronics Manufacturing Services.* She can be reached at smucha@powell-muchaconsulting.com.

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Rebuilding America's Electronics Backbone, One Member at a Time

The PCBAA is on a mission to ensure domestic security via a revitalized American manufacturing base.

ACROSS THE UNITED States, a quiet but urgent realization has been taking shape – one that echoes through defense briefings, aerospace reviews, medical device evaluations and critical infrastructure planning sessions. The nation that once led the world in electronics manufacturing now faces a stark truth: the ability to design and manufacture advanced electronics on domestic soil has diminished to dangerous levels.

This isn't speculation. It's not a theory. It's a matter of national security.

Again and again, leaders across government and industry have expressed the same concern:
A country that cannot build its own electronics cannot secure its own future.

That fundamental truth fueled the creation and mission of the Printed Circuit Board Association of America (PCBAA) in 2021. The organization exists because the stakes are no longer academic – they are strategic, economic and deeply tied to national security and resilience.

How America Lost Its Electronics Backbone

Time was, North America's electronics factories hummed with activity. Printed circuit boards flowed off production lines. Assemblers placed components with precision. Engineers developed new materials, architectures and processes. The region was a global leader in capability, innovation and capacity.

Over several decades, however, production gradually migrated offshore. First small projects, then major programs, then entire product lines. Lower costs dictated decisions, and lower-wage regions absorbed capability at an accelerating speed. The shift was slow enough to ignore in the moment, and large enough to reshape the entire global landscape.

Today, the numbers tell the story clearly:

- The US once produced over 30% of the value of the world's PCBs.
- Now it produces approximately 4%.

- Advanced substrates and packaging – key to defense and high-performance electronics – are almost entirely absent domestically.

This erosion has left critical sectors dependent on foreign sources for the technologies that power missiles, fighter jets, space systems, medical devices, energy grids, telecommunications networks and more.

In a world where electronics are the nervous system and backbone of every modern system, losing domestic capability means losing control over reliability, quality, lead time, security and strategic independence.

The Strategic Risk of Outsourcing Electronics

Consider what it means when a nation no longer manufactures the vital circuitry behind:

- Missile guidance
- Radar systems
- Secure communications
- Power management for spacecraft
- Implantable medical equipment
- Transportation safety systems
- Intelligence platforms
- Energy grid monitoring.

These aren't consumer gadgets. They are the pillars of national power, public safety and economic stability.

Relying on overseas production introduces unacceptable risks:

- Supply chain disruption
- Intellectual property theft
- Counterfeit component infiltration
- Geopolitical leverage
- Production delays during global crises
- Loss of technical expertise
- Reduced innovation capacity.

National security is not just tanks and aircraft. It is the ability to manufacture the electronics that makes those systems function. Without secure, domestic technology manufacturing, even the most advanced military platform is compromised before it leaves the ground.

This reality is what drives the mission of PCBAA.

Why PCBAA Emerged and Why it Matters

PCBAA was created at a time when the consequences of decades of offshoring had become undeniable. The nation needed a unified voice that could:

- Advocate for restoring domestic electronics manufacturing
- Educate policymakers about supply chain vulnerabilities
- Elevate the importance of PCBs and PCB assemblies
- Strengthen the infrastructure required for advanced technology production
- Support investment in US-based capability
- Connect industry leaders in a shared movement to rebuild.

The organization was not formed to maintain the status quo. It was built to change it.

PCBAA represents designers, PCB fabricators, assemblers, materials companies and equipment and testing suppliers – every essential link in the electronics manufacturing ecosystem. Its mission is to create a coordinated front capable of influencing policy, shaping national priorities, and driving real industrial resurgence.

Membership is Momentum

In most associations, membership benefits the individual company. With PCBAA, membership strengthens the entire sector.

- Each member adds weight to national advocacy efforts.
- Each member amplifies the case for investment and reshoring.
- Each member contributes to a unified message to Congress, defense agencies and OEMs.
- North America is committed to rebuilding its electronics manufacturing capability.

This collective voice is how industries change course. It is how legislation gets written, how incentives get created, how reshoring gains traction and how new capacity becomes commercially viable.

The message becomes stronger with every company that joins.

Membership directly fuels:

1. **National security advocacy.** Educating policymakers on the risks of foreign dependence for critical electronics and pushing for incentive structures that rebuild US capability.
2. **Industry visibility and influence.** Increasing awareness among defense and commercial OEMs about the importance of choosing domestic partners.
3. **Reshoring initiatives.** Driving policies and funding that encourage manufacturers to expand U.S.-based operations.
4. **A unified industry platform.** Creating a collaborative space where manufacturers, designers, suppliers and assemblers can align on shared national priorities.

These are not abstract goals; they are foundational to America's technological future.

That is how America's electronics backbone is restored, and I encourage you to engage with the PCBAA team to learn more about how to become a member today and be part of the mission. For more info, visit pcbaa.org.

DAN BEAULIEU is a longtime management consultant to the printed circuit industry and a member of the PCBAA; danbbeaulieu@aol.com.

Inspecting Printed Circuit Boards and Assemblies

How do inspection discipline and sampling plans decide whether a shipment ships or gets torn apart?

BEFORE GOING INTO PCB design, my employer was in the telecom business. I started out putting PCBs into antistatic bags, then into individual boxes with appropriate labels. A group of eight distinct boards was placed in a larger box to form a die group. The big box labeling reflected the part-dash number and revision for each board. This was called "final prep" and was the last step prior to shipping.

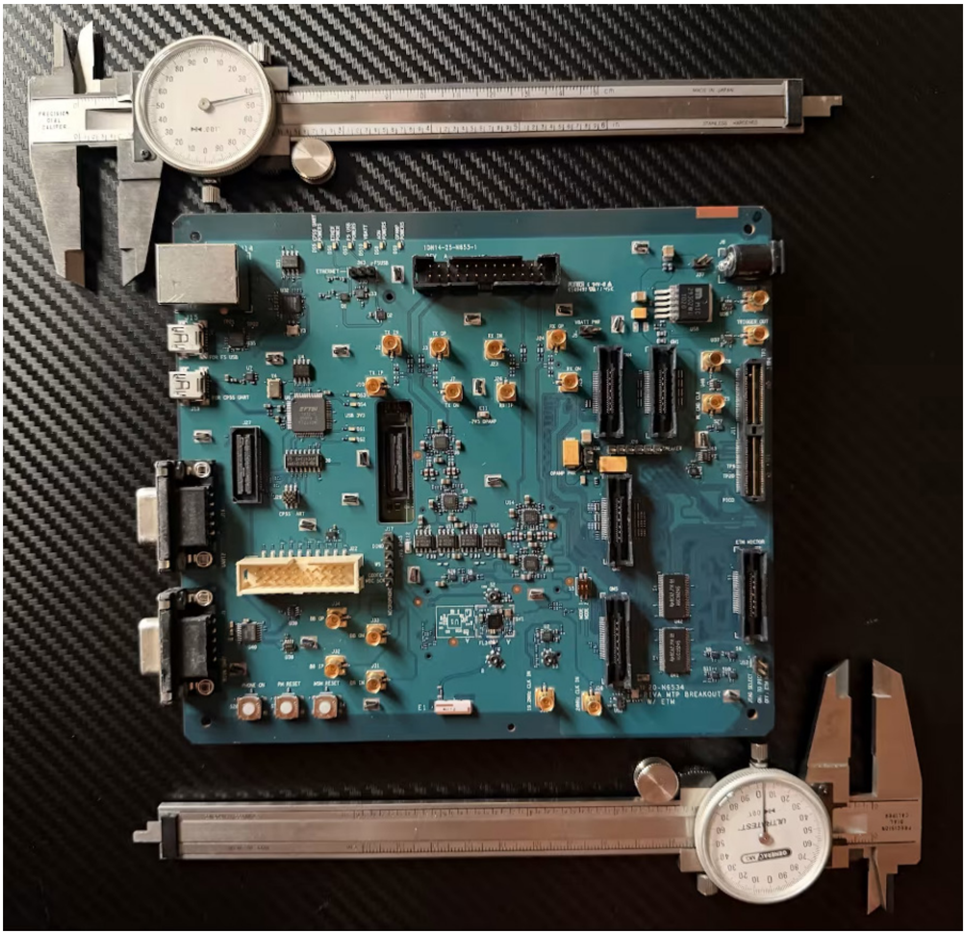

Figure 1. Dial calipers are essential for accurately measuring features on a PCB. Measuring outer or inner edges including hole sizes is possible using one end of the jaws or the other. Depth measurements use the other end of the calipers. (Source: Author)

A few selected to represent the whole shipment. Someone would audit the shipping boxes, looking for incorrect information on the labels and any other obvious defects. If they found a problem with the ones sampled, the entire lot would be re-examined by final prep. A missing antistatic awareness label could jeopardize the whole shipment. It could happen, especially toward the end of the quarter when we were sprinting to make our quotas.

The QC inspector and QA auditor were the last line of defense before submitting the die group to AT&T or one of the Baby Bells that came out of the antitrust settlement of 1984 that broke the phone company into several regional companies. After a few months, I transitioned to assembling card shelves and heat shields for telecom equipment racks.

Inspectors would check the card guides for burrs. They looked at everything from correct labeling to bent pins and even fingerprints. Each assembler had their own rubber stamp with their unique number. Mine was "ASSY68," surrounded by a square in black ink. Traceability matters.

It wasn't long before I moved to the Rack Wire and Test group, which assembled entire equipment racks. You've probably seen IT racks where the wiring looks like a plate of spaghetti and others that look so clean and orderly. I strove for cleanliness.

Eventually, I returned to a seated job assembling fuse/alarm panels installed at the top of the racks. The fuse panels had a 46-point wiring harness (23 wires) that wrapped around the inside of the two RU (rack-unit) enclosures. The wires were for signals, while busbars strapped all the fuses to power and ground.

I had my own way of dressing the wires into an S-turn so that the service loops to the fuses didn't overlap. When they made me the lead assembler, I wanted all nine (plus temps) of us to take the time to form the 18-gauge wires just like mine so that it was easier to spot a mis-wire. Aside from the ASSY-number, there was no way to tell who built the fuse panel.

One day, my manager asked me if we were on "tightened inspection" – where the sample size was much higher than normal inspection. I stated that if the lot submitted to the AT&T source inspector passes, we would be eligible for reduced inspection. He shook his head and said, "You're the only one" in the TransMUX department that is not on tightened inspection.

A sampling plan is derived from MIL-STD-105E. The document has several tables that specify how many units out of a lot or batch must be inspected based on the AQL (acceptable quality level) and the total number of units in the lot. A track record of rejects leads to greater scrutiny. A control chart would be the basis for monitoring a specific failure point if it becomes an issue.

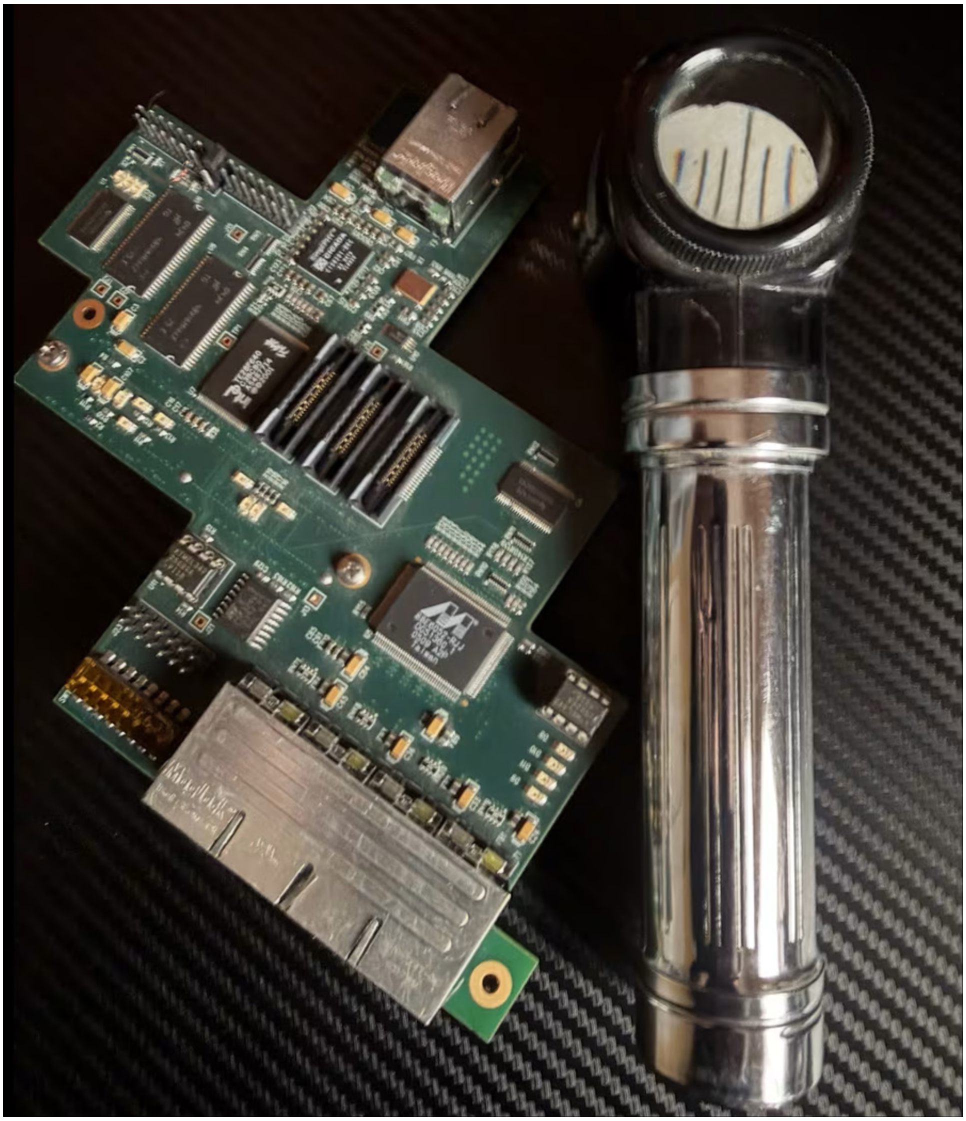

Figure 2. A loupe with a built-in light enables inspection of smaller objects. Note the graduations shown in the eyepiece. There is an open square with different hash marks for alternate units of measure. (Source: Author)

One day, a job opening came up in the Radio division. Point-to-multipoint radios were like a precursor to cellular networks that we know today. One of the use cases was offshore oil rigs where the land-based managers stayed in touch with the array of drilling platforms at sea. This job was an in-process inspection. I sat at the end of a row of fine-fingered ladies who stuffed the boards and put them through the drag solder machine before soaking them in freon to clean off the flux.

To reject or not to reject? If I couldn't find anything wrong with a PCBA, I pressed my triangular QA23 stamp into a red ink pad and applied it to the board. If placement or workmanship was off, I stuck little red arrows to the board, with a red tag to describe the defect. One thing the ladies didn't want was a red tag on their work.

There was an issue with letting them fix a noncompliant solder joint without first rejecting the board. I found that out the hard way when I asked for a touch-up on a borderline solder joint. Ruth, my manager, said that "if it's good, accept it and if it's not, then reject it. It's on you to decide what is acceptable."

To be fair, the company needs that information so that it knows where to focus its process improvement efforts. The better course of action was to get in touch with Henry, the QA inspector, for his opinion. He would audit the lot, choosing a random selection of units for visual and electrical qualification. The source inspector would do the same with their chosen samples.

Analog circuits can be an unusual case. I found the meniscus of a mica cap jammed down to the surface of the board unacceptable. There was no room for a top-side solder fillet. Although that was a clear violation of the workmanship standards, these were analog boards, and any length of wire acts as an antenna. As a practical matter, we accepted the defect on the radio boards, where we wouldn't have it on the digital boards.

One day, Ruth invited us four inspectors to move from in-process inspection over to receiving inspection. The only requirement was that we enroll in two concurrent Quality Assurance classes at a local junior college. My hand shot up immediately. One of the things that lifted my hand was a reluctance to put a red arrow on a PCBA with assemblers sitting right there. Rejecting something from a vendor seemed much less personal.

Studying the works of Dr. Edwards Deming (the godfather of statistical process control) and Dr. Joseph Juran (the architect of quality and author of the Pareto Principle) was indeed a life-shaping experience. We learned the theory about the standard deviation of a Poisson distribution along with practical aspects of quality assurance.

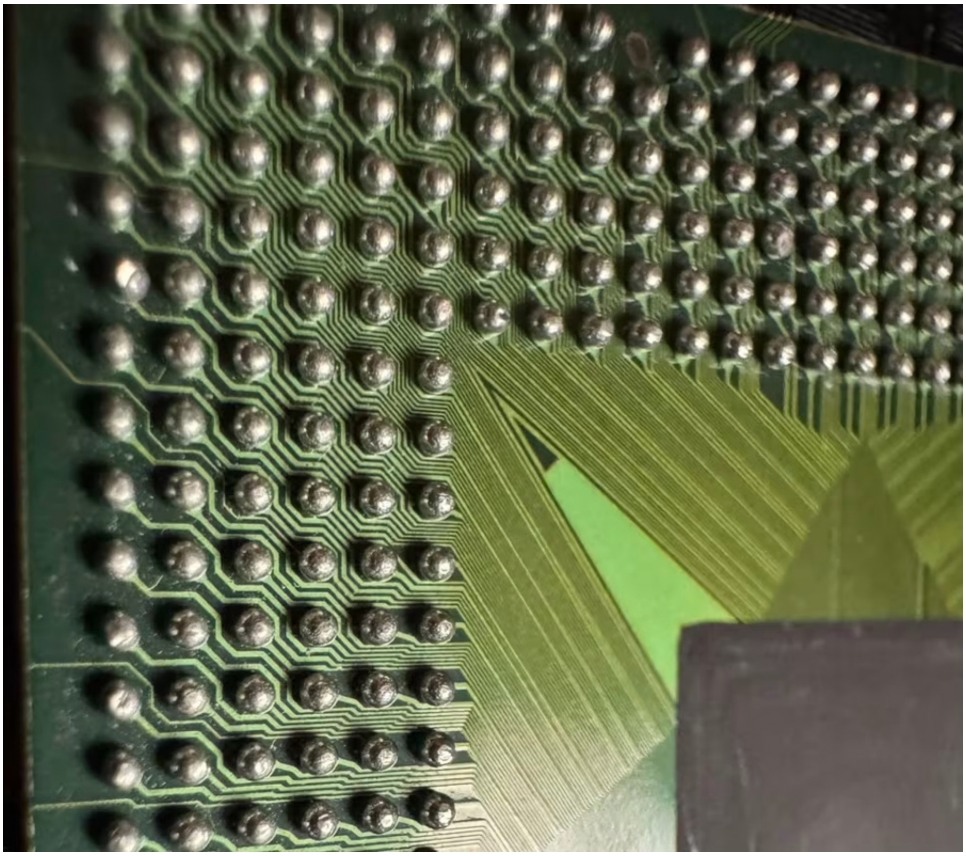

Figure 3. Today's PCBs begin to resemble substrates while substrates incorporate silicon in 2.5D construction borrowed from chip technology. We can expect this tech-drift to continue. (Source: Author)

Receiving inspection: the first line of defense. Running the Receiving Inspection lab meant checking bare boards before they went into the stock room. Of course, all the components also had to be compared to the source control drawings. Looking for absolute perfection wasn't the thing. What mattered is that the PCBs and their components "met the requirements." Our field guide in these matters is IPC-TM-650, "Test Methods Manual."

When a new part number came into the RI lab, it underwent first-article inspection. That meant that every dimension or feature was thoroughly examined. For example, if soft gold is specified on the fab drawing, we use a nondestructive method to verify its hardness by applying a specially cut diamond tip to an indenter. A fixture holds the board or a cross-section, and the indentor drops down, making a tiny indent in the metal. A bigger indent registers a lower number on the Knoop scale of hardness.

Pure gold is the softest and rates between 50 and 90; graded as ASTM B488 Code A. The next level of hardness is medium gold, which tests between 91 and 126 on the Knoop scale; classified as Code B. Hard gold is rated between 130 and 200, which would fall under ASTM Code C. For reference, diamonds are rated at the high end of the Knoop scale at 7000.

The receiving inspection lab also included a machine for checking the copper thickness in the via barrel. Another one measured the thickness of gold on the edge fingers. An optical comparator could measure tiny objects projected onto a backlit glass with graduation marks. The shadow of the part was projected at 10X actual size to facilitate the math. We also had a binocular microscope to find cracks in the PTH barrels.

A set of Mitutoyo pins was calibrated to check board warpage and hole sizes. We used plain old Scotch tape to see if any ink, mask or copper could be peeled from the boards in accordance with IPC-TM-650.

These days, we add automated optical inspection (AOI), x-ray and other technologies to look deeper into the PCBs. A reliability lab performs destructive testing, whereas all the other inspections are nondestructive. Weeding out the defects is one thing. Improving the process so that there are fewer defects is the ultimate goal of the inspection team. This is the inspector's value-add that goes beyond a rubber stamp.

JOHN BURKHERT, JR. is a principle PCB designer in retirement. For the past several years, he has been sharing what he has learned for the sake of helping fresh and ambitious PCB designers. The knowledge is passed along through stories and lessons learned from three decades of design, including the most basic one-layer board up to the high-reliability rigid-flex HDI designs for aerospace and military applications. His well-earned free time is spent on a bike, or with a mic doing a karaoke jam.

DESIGN **BEST PRACTICES**

Mastering Signal Integrity: From Fundamentals to AI-Powered Analysis

Signal integrity underpins reliable electronic design, and emerging AI tools are reshaping how engineers optimize it across all system speeds.

EVER WONDER WHAT makes our modern electronic devices so incredibly reliable, whether they're processing gigabits of data or simply ensuring a sensor reads accurately? While many factors contribute, one unsung hero often working behind the scenes is signal integrity (SI). Think of it as the invisible guardian of your electrical signals, ensuring they travel cleanly and efficiently from point A to point B. Ignoring it can lead to headaches, delays and even product failures, regardless of your operating speed. But embracing it? That's where the magic happens.

In today's electronic systems, from the fastest data centers to the most sensitive medical devices, a deep understanding of how signals propagate and how to mitigate issues that degrade signal quality has become critical. It's not just about "high-speed" anymore; it's about any signal path where clean, reliable transmission is paramount. Let's dive into why understanding and prioritizing signal integrity is crucial for every designer across all design spectrums.

Getting SI Right from the Start

Imagine building a skyscraper without a proper blueprint or a solid foundation. It wouldn't stand a chance, right? The same applies to your electronic designs. The very first steps you take in your PCB layout can make or break your signal integrity.

At its core, signal propagation, even at seemingly lower frequencies, involves transmission lines. These aren't just simple wires; they are sophisticated structures that guide electromagnetic energy, modeled by per-unit-length inductance (L), capacitance (C), resistance (R), and conductance (G). While their effects become more pronounced at higher frequencies, any trace whose length is a significant fraction of the signal's rise-time wavelength behaves as a transmission line. Their characteristic impedance is a crucial parameter, determined by the trace geometry and the PCB material properties.

Don't make fundamental mistakes (routing, parts placement, stackup). This is where we lay the groundwork. Simple errors in how you route traces, place components or design your PCB stackup can introduce noise, reflections and crosstalk that degrade signal quality. This isn't just for fast signals; even a slow digital signal can suffer from ringing, or a sensitive analog signal can pick up unwanted noise. It's much easier (and cheaper!) to correct these issues during the design phase than after prototypes are built.

Component placement dictates board performance. Where you put your components isn't just about fitting everything on the board. Strategic placement minimizes trace lengths, reduces parasitic effects and optimizes signal paths, directly impacting your board's overall performance by managing impedance and reducing potential discontinuities. This is vital for minimizing noise pickup in analog circuits and ensuring reliable switching in digital ones.

Route signals adjacent to their reference planes. This is a golden rule for all designs. Keeping signals close to their ground or power planes provides a clear, low-inductance return path for the current, minimizing loop inductance and significantly reducing electromagnetic interference (EMI) – both radiated and susceptibility. This helps maintain a consistent characteristic impedance for your transmission lines and reduces noise.

Tightly coupled power and ground planes. A well-designed power delivery network (PDN) with tightly coupled power and ground planes acts like a stable reservoir for your components, providing low impedance and filtering out noise. This keeps components powered reliably and prevents power rail noise from coupling into signals, which can be detrimental to both digital and analog performance.

Understanding the Challenges: Impedance, Reflections and Crosstalk

Even with a great foundation, signals face inherent challenges that can compromise their integrity, regardless of their speed.

Impedance discontinuities and reflections. When a signal encounters a sudden change in its electrical environment – a change in characteristic impedance – a portion of its energy doesn't continue forward. Instead, it reflects toward the source. This phenomenon is quantified by the reflection coefficient (which depends on the impedance before (Z_1) and after (Z_2) the discontinuity. These reflections cause signal degradation like overshoot, undershoot and ringing. While more severe at higher speeds, ringing can still lead to false triggering in slower digital circuits or introduce significant errors in sensitive analog measurements.

Termination techniques. To minimize these detrimental reflections, various strategies are employed:

- **Series termination:** A resistor placed at the source end, matching the combined driver and resistor impedance to the line's characteristic impedance. This absorbs reflections at the source.
- **Parallel termination:** A resistor (or network) at the receiving end, absorbing the signal energy to prevent reflections from bouncing back. This includes variations like DC, AC and Thevenin termination, each suited for different power and signal characteristics.
- **Multi-load scenarios:** These require careful layout and often utilize parallel termination at the bus end with very short stubs to each load to minimize reflections.

Crosstalk. This is the unwanted coupling of energy between adjacent signal traces, primarily due to capacitive and inductive coupling. It manifests as near-end crosstalk (NEXT), which is coupled noise measured at the aggressor's source end, and far-end crosstalk (FEXT), measured at the aggressor's load end. Crosstalk isn't just a high-speed problem; it can introduce noise into sensitive analog signals or cause logic errors in digital circuits if the coupled noise is large enough to cross logic thresholds. Mitigation involves increasing spacing between traces, decreasing coupling length, using ground planes as shields, and optimizing trace geometry.

Low-Hanging Fruit and Advanced Analysis

Sometimes, we're tempted to push through a design, hoping for the best. But when it comes to SI, a little analysis goes a long way and can save a lot of grief down the line, no matter the application.

You don't have to be an SI guru to benefit from good practices. Partnering with dedicated signal integrity and power integrity (SI/PI) engineers is invaluable. They bring specialized knowledge and tools, helping identify potential issues early and guide you toward robust solutions for any design.

Many SI issues are low-hanging fruit that can be resolved with basic checks and adherence to best practices. Addressing these early frees SI/PI engineers to tackle the truly complex challenges and help set overarching standards and limits for your designs. It's a win-win for everyone.

To effectively address these challenges, both simple and complex, advanced analysis tools are essential for validating and diagnosing SI issues:

Software. Modern electronic design automation (EDA) simulation and analysis tools are indispensable for pre-layout and post-layout simulation and analysis. They allow engineers to predict signal behavior and identify potential problems before fabrication, whether it's a high-speed bus or a low-frequency, noise-sensitive sensor line.

Hardware. For real-world validation and debugging:

- **High-performance oscilloscopes:** Used for time-domain measurements, allowing engineers to visualize signal waveforms, measure rise/fall times (edge rates) and generate eye diagrams – a powerful visual representation of signal quality, jitter and noise margins, particularly useful for digital signals of all speeds.
- **Vector network analyzers (VNAs):** Crucial for frequency-domain analysis, providing S-parameters (scattering parameters) that offer a "health report" of how signals perform at different frequencies. This reveals losses, resonances and impedance variations that can severely impact data, from RF to high-speed digital.
- **Time domain reflectometry (TDR):** A powerful technique that sends a fast edge down a transmission line and analyzes the reflections to precisely locate and identify impedance discontinuities along the trace. It's like an x-ray for PCB traces, invaluable for debugging any signal path.

AI as an Enabler

The future of design is here, and artificial intelligence (AI) is rapidly becoming a powerful ally in the world of signal integrity. AI isn't just about doing more with less; it's about doing things smarter, faster, and more accessible across all design types.

AI opens up the possibility to do more with less, enabling mentorship and training to be taken further, faster and more easily.

Imagine a new user interface (UI) that leverages AI to guide PCB designers through general SI analyses with ease. This could mean automated checks for common pitfalls, suggestions aligned with industry best practices, or flagging potential issues before they become major problems. It empowers designers to tackle the "low-hanging fruit" effectively, ensuring a solid foundation without needing deep SI expertise, whether they're designing a simple microcontroller board or a complex server.

For those who want to deepen their understanding or are working with limited resources, AI unveils incredible new options. Through design space exploration (DSE), AI can rapidly evaluate numerous design variations to optimize performance, cost, and manufacturability. This allows PCB designers to explore complex tradeoffs, uncover innovative solutions and achieve optimal signal integrity, even in the most-challenging scenarios. It's like having a highly intelligent assistant that can recommend an optimized topology using simulation in the blink of an eye, regardless of design complexity.

Conclusion

I'll end with this: signal integrity is not just a buzzword for high-speed systems; it is a fundamental pillar of PCB performance for any electronic design. Mastering these concepts, from understanding transmission lines and mitigating reflections to leveraging advanced simulation and measurement tools, is crucial for creating robust and reliable systems as technology continues to push boundaries in speed, edge rates, complexity and sensitivity. Let's build our electronic future on a solid foundation of excellent signal integrity, no matter the application.

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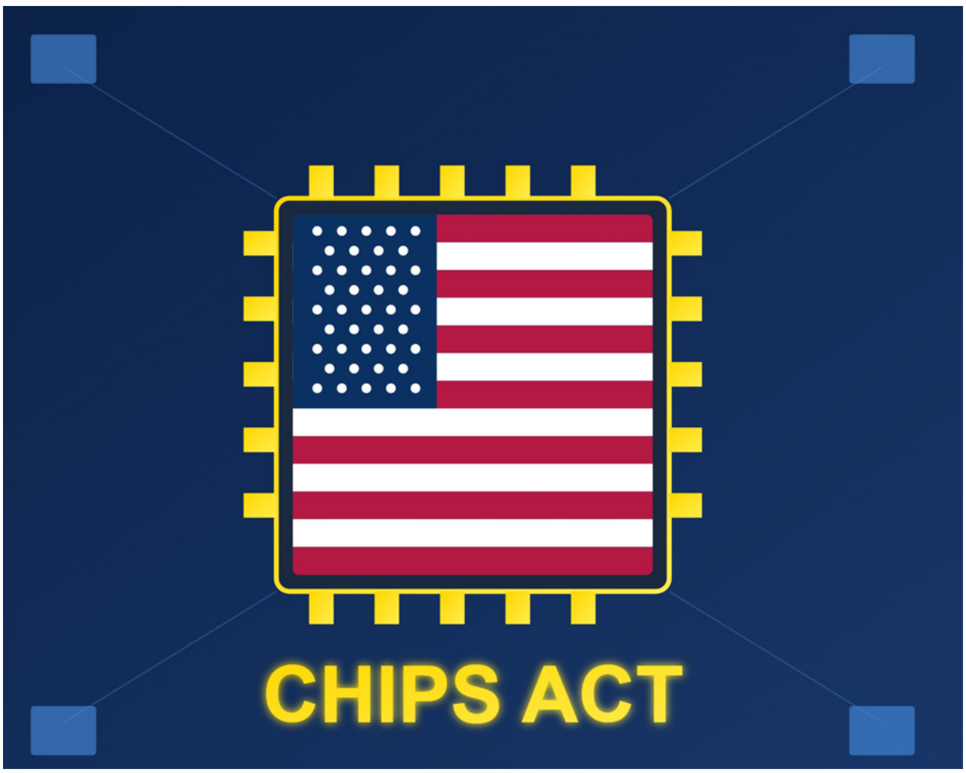
MATERIAL **GAINS**

Value Chain Reshaping is the Latest Maturing Stage of the Global Electronics Industry

Under Foundry 2.0, the semiconductor value chain is moving back into strategic focus.

WHEN JONI MITCHELL recorded *Big Yellow Taxi*, singing "You don't know what you've got till it's gone," she was reiterating the proverbial warning that we often appreciate things properly only after losing them. It's an observation that transcends context and can be applied even in today's electronics industry. For decades, Western companies have outsourced significant parts of their value chain to achieve cost-down and to focus on core competencies in pursuit of efficiency. Today's geopolitical tensions are drawing attention to the loss of sovereignty that results from exporting control of critical processes like packaging and testing as part of the semiconductor value chain.

While repatriation initiatives like the US Chips Act have focused on silicon, it's becoming clear to all involved – politicians included – who depend on experts from the industry to provide technical and practical insights, that achieving any meaningful future shift in the balance of economic power is a much broader task than setting up wafer fabs alone. Although establishing those fabs is a huge undertaking that demands massive investment, the Act has not ascribed comparable value to activities like packaging and testing.



At the same time, packaging has undergone significant technical changes. While traditional lead frame-type packages, including small-outline lead frame packages, account for more than 60% of the market, emerging AI and high-performance computing demands are driving powerful new trends in advanced packaging. As chip makers combine processors and memory dies in 2.5D/3D structures and chiplets to increase compute performance and efficiency, the emphasis is shifting from wafer-level packaging to panel-level technologies that package multiple dies together. This convergence aligns well with vertical technology integration and brings additional advantages such as greater overall yield and efficiency, as silicon manufacturers can easily identify and select good dies and perform system-level testing.

Hence, panel-level packaging has disruptive potential by creating a strong case for chip fabricators to handle testing and packaging under the same roof. It's recognized as a trend, now described as Foundry 2.0, and the largest companies, including TSMC and GlobalFoundries, are already committing multi-billion-dollar investments to expand their advanced packaging capabilities. There are major implications, not only for the outsourced semiconductor assembly and test (OSAT) sector but also for the future of Western semiconductor manufacturing, as the model is based on companies extending sovereignty over their value chain. The window of opportunity for Western chipmakers is slim, however, as they must move quickly or be left behind by the big foundries. Given the narrow focus of the Chips Act and similar European government initiatives, and the Trump administration's reframing of Chips funding, private equity appears to be the most practicable source of timely and sufficient financing.

Adding to the complexity of the situation, leading PCB fabricators are also investing heavily to migrate their businesses into the advanced packaging market. However, the processes are not easy or cheap to set up. Such is the investment needed that making the change to advanced packaging is an option only for the largest companies here.

With the silicon fabs and large board shops eyeing a slice of the advanced packaging cake, the changes present opportunities for OSAT businesses as well as vertically integrated manufacturers that bring chip fabrication, assembly and test together under one roof. Private equity is flowing into companies of all types, which is unsurprising given the strong growth in demand for electronic hardware across markets such as automotive, consumer, industrial, medical and defense. It's a favorable risk-versus-reward equation for investors.

Foundry 2.0 embodies the values of vertical integration in combining competencies to create a whole greater than the sum of its parts. In the past, as each constituent process became more developed, it made sense for individual specialists to make it their core competence, effectively globalizing the industry. Now that high-tech is recognized as a hugely powerful economic engine, with semiconductor innovation taking such a central role in driving progress, it has become extremely important politically. In this context, the lack of control over critical packaging and testing processes is a problem. Fixing it will not be easy because few, if any, companies in the West now have the required competencies, as they have been so extensively exported.

As the pendulum swings back, things will not simply return to the way they were. The industry has become more mature and professional, processes are more complex, quality standards are higher, and so, too, are market expectations. The large investment needed to enter and compete presents a barrier to smaller companies.

Although time is of the essence for Western economies, there is evidence of action in the US to restore lost competencies, including through acquisitions and organic growth. Perhaps we can all learn the importance of bigpicture planning and mapping in advance the long-term consequences of business decisions. It's true that outsourcing to reduce costs has been critical to the survival of businesses in the West. On the other hand, the tradeoffs are now clearly visible, including the loss of indigenous suppliers and, more importantly, the loss of up-to-date knowledge by effectively handing the baton of progress offshore.

Clearly, today's globalized electronics industry is set to change. In Foundry 2.0, however, we are seeing the birth of a new approach, and not a return to the old. It's the next stage in the maturing of a value chain that is always innovative, intriguing and exciting.

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Managing Moisture and Heat in Flex and Rigid-Flex Assembly

Successful flex and rigid-flex assembly depends on controlling moisture.

QUESTIONS ABOUT BAKING and assembly come up at least monthly, if not more often. Several factors can impact successful assembly with flex and rigid-flex.

Environment. As a rule, delamination is usually due to retained moisture. The rapid rise in temperature during reflow causes moisture to change from liquid to expanding vapor or steam. This expansion can result in delamination.

Storage and factory conditions can certainly impact assembly success. Baking times and temperatures are definitely humidity-dependent. Most guidelines are not defined based on a specific condition. I would treat them as a baseline, and if humidity is high or if parts were exposed to a long liquid cleaning, I would increase bake times.

Some assemblers use vacuum ovens for drying. The advantage is that this can be done at lower temperatures because the boiling point of water drops as the vacuum is applied. The vacuum also provides mechanical encouragement to draw the moisture out. It's just another technique that can be employed.

It is important to process immediately after baking. If you can't process these circuits right away, store them in a desiccant chamber to keep them dry. A desiccant chamber cannot dry parts, but it can keep them dry for long periods.

Soldering thermal profile. Regardless of the PCB design, the assembly solder type will drive your solder profile – lead-free solders will mean higher temperatures. Often, there is a tendency to jump to a 260°C profile. However, before going there, consider lower temperatures. Many lead-free solders will reflow at lower temperatures. Data tell us that as the reflow temperature rises, the increase in the amount of stress on all the materials and plated through-holes is not linear. These stresses rise much faster than the temperature increase. Often temperatures of 245°C or even as low as 235°C can be successfully employed. This can result in a dramatic reduction of stress on the board and assembly. As a result, the odds of delamination will be reduced.

Material selection. Certainly, every material has a different moisture absorption rate as well as a rate of drying. Some materials absorb moisture slowly. However, they also release it slowly, so it is still important to bake these materials if they have been exposed to moisture for a long time. In some cases, you may need to extend bakes to account for hygroscopic materials or long exposures.

For rigid materials, epoxy-based laminates do not absorb moisture as much as polyimides. Fluorocarbon materials do not really absorb moisture as they lack polar groups, which are receptors to moisture. Liquid crystal polymers (LCP) are also known for low moisture absorption.

Flex materials, specifically acrylic adhesive and polyimide film, are known to absorb moisture. Flex materials can absorb ambient moisture within 30 min. Making sure these are dry during reflow is very important.

Generally, moisture absorption is an issue only during reflow processes, due to high temperatures and rapid temperature rises. For most PCBs, the most stressful condition they will ever see is solder reflow. In most applications, they are unlikely to see anything close to this in actual operation.

Stackup. Additionally, the overall PCB construction and artwork pattern are variables to consider. Thermal mass and heat absorption rate come into play. Polyimide film is very sensitive to infrared energy and will absorb IR energy very rapidly. It is important to avoid placing IR systems on flex circuits.

One- and two-layer flexes are very low in mass and will reach reflow temperatures quickly. In addition, it is easy to bake out moisture. Both baking and reflow profiles can be managed accordingly. Baking can be successful in just a couple hours.

As we add layers, thermal mass increases. A part with many layers or very thick has a lot of mass to dry, and it can take a long time for moisture to exit. Bake times need to increase to ensure the parts are dry. Bake times may increase to 6-12 hr.

Rigid-flex PCBs bring other complications. The number of flexible vs. rigid layers will impact moisture capacity. In the rigid sections, the flex is sandwiched inside the rigid material. If there is moisture retained in the flex layers of the rigid, it can be trapped and difficult to remove.

The rigid sections are also much thicker than flex regions. As a result, flex regions get up to reflow temperature and stay there much longer than rigid sections. This puts more stress on the flex region. Some assemblers will apply "shields" over flex regions to reduce heat absorption. This can be as simple as a rigid laminate.

From the artwork perspective, plane layers will impact moisture absorption and expulsion. It may be harder to get the moisture in because the plane blocks it. Conversely, it also traps it since the moisture can't exit through the plane. It needs to exit horizontally from the side of the part. It can take much longer to remove moisture under planes. Essentially, think of this as a plumbing challenge. What is the path out, and how do you encourage it?

So, in summary, accommodate your design by using prebake times sufficient to drive out as much moisture as possible. An extra few hours of oven time is a small price to pay. Once dry, keep 'em dry until soldering. Finally, keep your cool – if a lower reflow temperature is used, delamination is a rare occurrence.

NICK KOOP is director of flex technology at TTM Technologies (ttm.com), vice chairman of the IPC Flexible Circuits Committee and co-chair of the IPC-6013 Qualification and Performance Specification for Flexible Printed Boards Subcommittee; nick.koop@ttmtech.com. He and co-"Flexpert" **MARK FINSTAD** (mark.finstad@flexiblecircuit.com) welcome your suggestions.

ULTRA **HDI FUNDAMENTALS**

Designing for Manufacturability in Ultra HDI: New Rules, New Realities

Ultra HDI changes the design for manufacturability equation.

by ANAYA VARDYA

As more teams begin to explore ultra HDI, one of the early surprises is just how different the design for manufacturability (DfM) conversation becomes. HDI gave us a playbook to follow, and many designers could recite those spacing and registration rules from memory. UHDI shifts that comfort zone. This technology opens remarkable routing opportunities, but it also requires us to revisit assumptions we have relied on for years.

Before diving into advanced routing techniques or material selection, it helps to step back and examine how manufacturability changes when features are built differently. Ultra HDI is not "just HDI but smaller." Guidelines change because the underlying process changes, and that affects every DfM decision we make.

A Different Starting Point

With traditional HDI, most of us learned to design around the behavior of traditional subtractive etch processes. We understood the limits of undercut, the shape of a trapezoidal trace and how copper thickness drifted across a panel. That experience still matters, but Ultra HDI introduces a new manufacturing baseline.

Semi-additive processes build copper traces with very precise control. The sidewalls are more vertical, the geometry is more consistent and small variations are easier to hold. The tradeoff: these geometries also introduce sensitivities in other processes. Imaging accuracy, seed-layer uniformity and plating distribution now play a much bigger role in overall yield.

This is where DfM becomes critical. At these feature sizes, even tiny mismatches between *design intent* and *process capability* can cascade into larger problems. A design that technically "meets the rules" might still suffer yield loss if spacing, pad shapes, or stackup choices don't match how the semi-additive process behaves.

Good DfM is no longer a polishing step at the end of layout. For ultra HDI, DfM is one of the enabling steps that keeps the entire build stable.

Let's take a practical look at the areas where UHDI requires us to rethink our approach.

Spacing: Precision with a Purpose

If there is one thing UHDI designers learn quickly, it is that spacing rules deserve more attention than ever. In subtractive etching, spacing was primarily used to compensate for undercut. UHDI changes that dynamic. Since copper is plated up instead of etched away, spacing becomes less about etch bias and more about how well the imaging system defines the boundaries.

The temptation is to use the smallest spacing everywhere, simply because it is available. In reality, the most robust UHDI designs do the opposite. They tighten spacing only in the areas that truly need it, usually underneath or immediately around fine-pitch BGAs. Everywhere else, spacing is relaxed to give the process a more comfortable margin.

Consistent spacing within a region also helps with plating uniformity. Abrupt shifts from very fine spacing to larger geometries within the same area can create subtle thickness variations. In most cases, they are harmless, but at UHDI dimensions, they can have more influence than you might expect. A little restraint goes a long way.

Pad Geometry and Capture Constraints

As pitch narrows, pads inevitably shrink. Smaller pads are wonderful for breakout channels, but they reduce the margin for registration and solder mask alignment. Semi-additive copper gives cleaner pad edges and more predictable land shapes, but the pads are still small enough that the registration budget becomes one of the first constraints to watch.

A few practical recommendations to help maintain stability:

- Use consistent pad sizes across the same feature group.
- Avoid pushing capture ring tolerances to the absolute limit unless no other option is available. Work closely with the fabricator on minimum annular ring when the pad sits on a UHDI layer. The acceptable ring in a subtractive layer may not translate directly.
- Be mindful of via size and aspect ratio.
- Keep communication clear in the data package when an area is especially sensitive.

These decisions are not about being conservative. They are about recognizing how small geometries amplify normal manufacturing variations. When the pad size is already near the floor, every micron counts.

The Growing Value of Hybrid Stackups

For many designs, the most effective and cost-conscious approach is a blend of UHDI and traditional subtractive layers. You gain the routing density where it is needed, without committing every layer to the tighter controls that UHDI requires.

A hybrid stackup might place one or two UHDI layers strategically around the BGA breakout, then rely on more traditional layers for power distribution, high-current paths or broader routing. This gives the design team:

- Freedom to route dense areas efficiently
- More predictable thermal and mechanical behavior
- Lower total cost
- Flexibility with impedance on layers that do not require UHDI features.

The key is to align the stackup with the fabricator's process sequence. Every manufacturer with UHDI capability has preferred pairings of dielectric, seed-layer thickness, and lamination order. These preferences often result from years of development. When the stackup works with the shop's process window, yields improve dramatically.

At the end of the day, stackup planning is one of the best opportunities to avoid rework later.

Tolerances: What "Tight" Really Looks Like Now

Those who have been designing HDI for a while know how important tolerances are. Ultra HDI sharpens that importance. Copper thickness, line-width variation, and dielectric thickness all affect impedance more intently at small geometries.

The best practice is to rely on your fabricator's input when modeling impedance. Even simulation tools that perform well at larger geometries can mispredict performance at UHDI scales if the inputs do not match actual manufacturing conditions.

Similarly, solder mask registration deserves more attention. As pads shrink, the percentage of pad area covered by mask tolerance increases. Mask-defined lands should be approached thoughtfully, and your fabricator can often offer guidance on where mask alignment is most challenging.

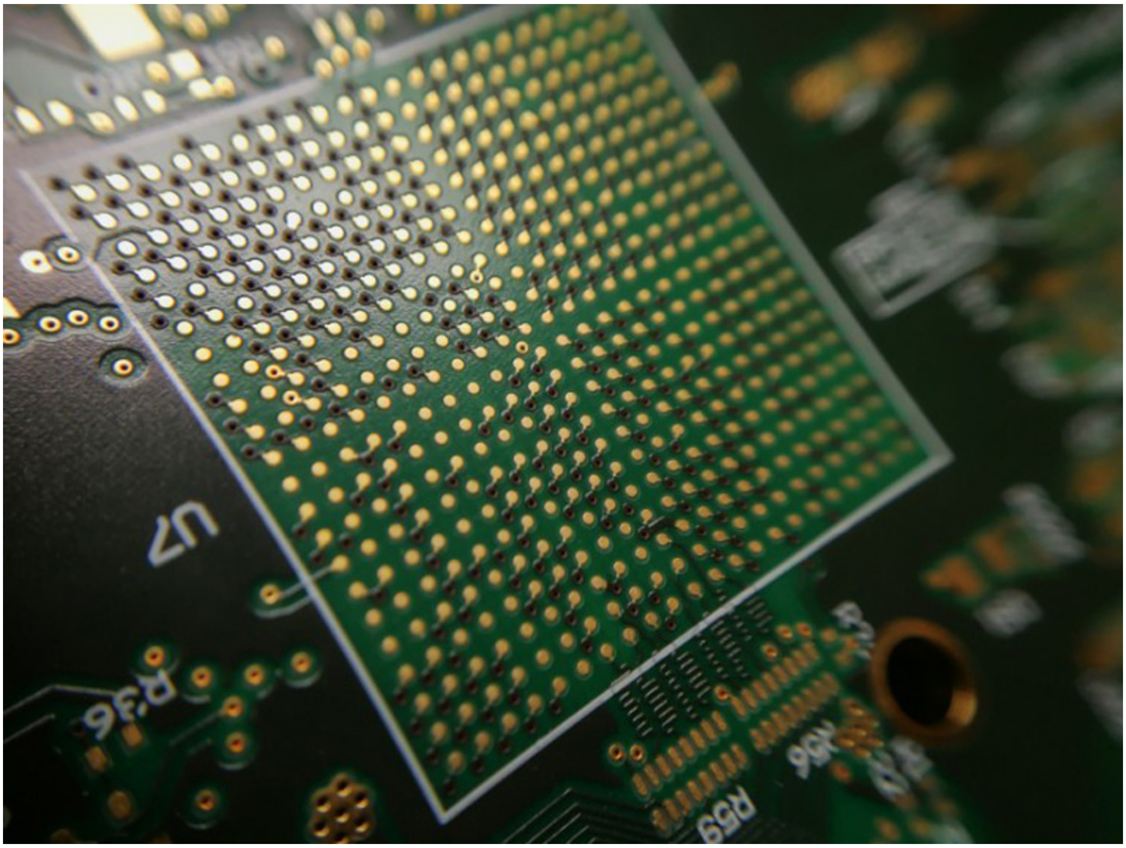

Figure 1. Ultra HDI manufacturing requires tighter process control and closer alignment between design intent and fabrication capability.

Tighter Process Control

Ultra HDI requires tighter process control than most legacy HDI lines were built to handle.

Several factors now shape yield more than in traditional HDI:

- Thermal consistency in lamination
- Tight control of copper growth across the entire panel
- Imaging uniformity within each region
- Coordination between imaging chemistries and plating additives
- Cleaning and surface prep that supports ultra-thin seed layer adhesion

These factors are not new, but their impact becomes amplified as features shrink.

Fabricators often use statistical monitoring, automated sampling and inline measurement systems to watch these variables in real time. The design benefits when the process is stable, and the process becomes more stable when the design supports it. The two are inseparable.

Process Control Beats Inspection

Inspection has always been part of PCB manufacturing, but ultra HDI places a much stronger spotlight on process control. When features reach the 65µm range, yield is shaped less by end-of-line inspection and more by how well each step in the build stays within a very narrow process window.

Shops that succeed with UHDI tend to approach process control like a continuous conversation between imaging, plating, lamination, and material behavior. Each step influences the next, and small variations that were once insignificant suddenly matter. That is why the real gains come from a disciplined system that keeps the entire process stable, rather than relying on any single automation.

A few examples help illustrate how important this control becomes:

- **Imaging consistency** directly determines trace definition. Even minor variations in resist coating, exposure energy, or alignment can affect line width at UHDI feature sizes.
- **Plating chemistry stability** influences copper thickness more dramatically than designers might expect. Small shifts in additive concentration or agitation can alter trace geometry across the panel.
- **Material preparation and handling** play a much larger role. Ultra-thin seed layers and very smooth dielectrics require careful control.
- **Lamination behavior** becomes a bigger part of the equation, especially when hybrid stackups mix thin UHDI layers with traditional cores. Consistent pressure, temperature and ramp rates help keep registration predictable.

Inspection and measurement still matter, but they serve a different purpose in the UHDI environment. Instead of acting as a catchall at the end of fabrication, inspection becomes a real-time validation tool that confirms whether the controls in place are holding. In other words, inspection verifies the process's discipline rather than attempting to compensate for a lack of it.

Freedom, with Discipline

Designing for manufacturability in UHDI is not about memorizing new limits. It is about understanding how finer geometries shift priorities. Small features give you more routing freedom, but they also demand greater discipline. The tradeoff pays off if you design with the process in mind from the beginning.

Teams that treat DfM as a core part of the design phase benefit from:

- More predictable stackup behavior
- Cleaner breakout around advanced BGAs
- Higher yield and fewer surprises in production

- More stable impedance
- Better overall cost structure.

Innovation keeps moving. UHDI is a clear example of how technology can unlock capabilities we did not have before. But real success comes from execution. When designers, fabricators and process engineers collaborate early and build around shared assumptions, Ultra HDI becomes not only manufacturable but reliable – at scale.

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SPACING LIMITS

Consider Manufacturing Complexity When PCB Designs Have Tight Hole-to-Trace Spacing

Tight spacing (less than 8 mils) between drilled holes and copper traces increases fabrication complexity and yield risk.

by AKBER ROY

In the world of PCB manufacturing, knowledge of manufacturing constraints can help you design PCB using techniques that can guarantee reliable, economical and high-yield manufacturing. A wrong approach at the PCB layout stage can impact the complexity and cost of its fab and assembly. Understanding this enables you to develop smart practical design solutions for economical manufacturing and rapid prototyping cycles.

In PCB manufacturing, drilled hole-to-trace clearance (the distance between the edges of a drilled hole) and the nearest copper trace is a critical design parameter. The industry-standard recommendation is ≥8 mils (0.2mm) **(Figure 1)**. When designs fall below this threshold, manufacturing complexity rises sharply, driving up costs, extending lead times, lowering yields and introducing additional challenges related to drilled-hole aspect ratio.

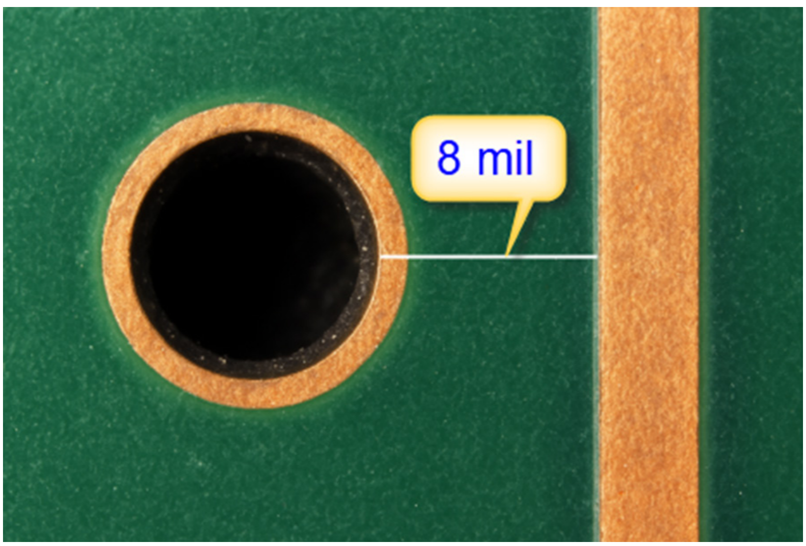

Figure 1. Example of 8-mil hole-to-trace spacing, illustrating recommended minimum clearance between a plated through-hole and adjacent copper to support standard PCB fabrication yields.

Why Clearance Matters

When the clearance between a plated through-hole (PTH) and nearby copper trace or pad edge drops below 8 mils per side, the risk of manufacturing defects increases sharply. Drill bits can slightly wander due to tool deflection, material hardness or machine tolerance. With less than 8 mils spacing, even a slight drill's positional tolerance can cause the hole wall to cut into adjacent copper, which can lead to several issues, including:

- Broken traces or pads if the drill overlaps copper features;
- Reduced insulation between copper and the plated barrel, increasing the risk of shorts or leakage;
- Higher scrap rates and rework, because small spacing pushes the limits of standard PCB fabrication.

In addition, tighter spacing usually means using smaller drill sizes, which increases the aspect ratio (board thickness to drill diameter). The higher the aspect ratio, the more difficult it is to achieve reliable plating, often leading to issues such as barrel cracks or voids. All this adds complexity, raises manufacturing costs, extends lead times, and increases overall risk.

Aspect ratio considerations. Aspect ratio in PCB manufacturing is simply the ratio of board thickness to the diameter of the smallest drill hole **(Figure 2)**. It is calculated by dividing the PCB thickness by the smallest drill diameter, and expressed as

Aspect ratio = PCB thickness / smallest drill diameter

Most PCB manufacturers can accommodate aspect ratios in the range of 8:1 to 10:1. In practical terms, this means that a 0.3mm (about 0.01″) drill hole can be reliably produced in a board that is up to 3mm (about 0.12″) thick. A higher aspect ratio means deeper, narrower holes, which are harder to plate and more prone to reliability issues.

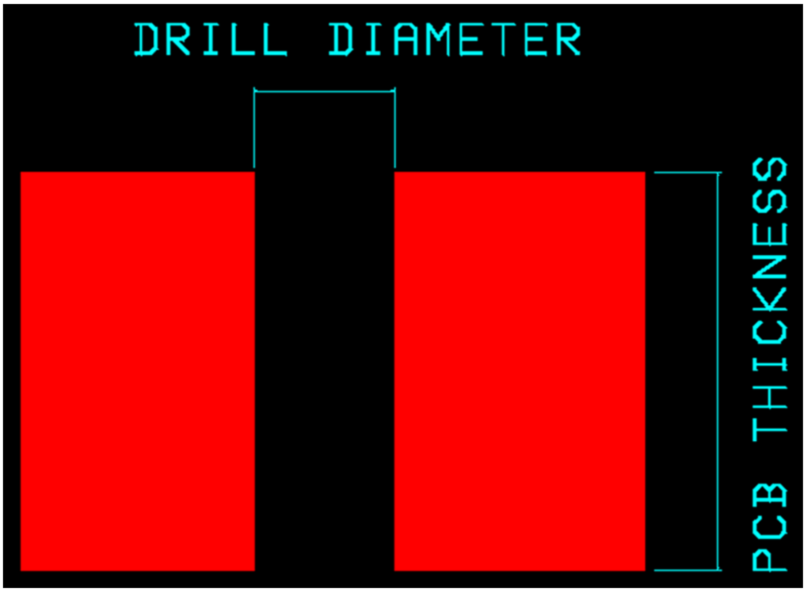

Figure 2. Relationship between drill diameter and PCB thickness, showing how smaller drill sizes increase aspect ratio and introduce plating and reliability challenges.

When drill diameters become smaller to permit tighter routing, the aspect ratio increases. Higher aspect ratios are more difficult to plate properly, and this can result in problems, including barrel cracks, plating voids or reduced via reliability.

If the drill-to-trace clearance falls below 8 mils, challenges increase. Manufacturers must ensure extremely precise drilling while also managing the added challenge of plating high-aspect-ratio holes. This combination significantly increases both cost and risk.

In cases where high aspect ratio holes are required, manufacturers often need to use advanced plating techniques. These may include special plating chemistries or multiple plating cycles, which not only increase complexity but also extend the overall fabrication time.

Manufacturing challenges below 8mil. When drill to trace spacing falls below 8 mil, the PCB moves into a far more complex manufacturing zone. Standard mechanical drilling is often insufficient, and fabricators may need to use processes requiring specialized equipment that significantly increase costs.

At the same time, alignment between drilled holes and copper layers must be nearly flawless, which forces manufacturers to rely on advanced registration systems, including laser direct imaging (LDI), x-ray registration systems and optical targets (fiducials), adding both time and process steps.

Smaller holes also mean higher aspect ratios, and plating these tall, narrow vias is much more difficult, often leading to voids or long-term reliability issues **(Figure 3)**. Also, the tighter spacing magnifies tolerance challenges, so more boards tend to fail inspection or electrical testing, driving down yields and pushing per-board costs even higher.

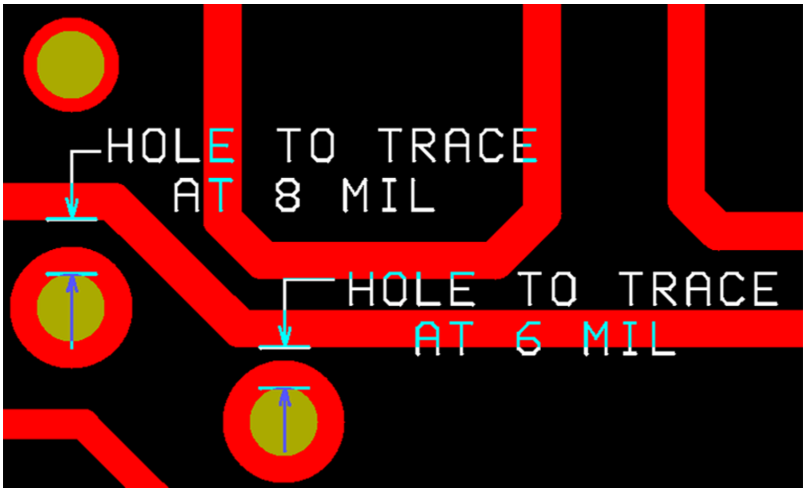

Figure 3. Comparison of hole-to-trace spacing at 8 mils versus 6 mils, highlighting how reduced clearance increases drilling tolerance risk.

Cost and lead time implications. When drill-to-trace clearance stays at or above 8mil with an aspect ratio of 10:1 or less, boards can usually be built using standard processes at normal pricing and lead times. Once the clearance drops below 8 mils and the aspect ratio increases, however, the design is treated as HDI (high-density interconnect). This increases fabrication costs 30–50% because it often requires advanced drilling methods, additional plating cycles, or even resin-filled microvias. On top of that, yields tend to drop, further raising the cost per board. Lead time is also heavily affected; what might normally take five to 10 working days can stretch to 10 or even 20 days or more, depending on the complexity. Because only a limited number of fabricators can meet such tight requirements, sourcing adds delays and expedite options, if available at all, can be extremely expensive.

Industry Standards and Recommendations

Industry standards such as IPC-2221 and IPC-6012 define the minimum drill-to-copper clearance and aspect ratio requirements for reliable PCB designs. Manufacturers build according to these rules with practical limits, while HDI designs may push beyond them, resulting in higher cost and complexity.

IPC-2221 and IPC-6012. These IPC standards set the baseline rules for PCB design and fabrication quality. For Class II and Class III boards, they emphasize maintaining sufficient drill-to-copper clearance and controlling aspect ratios. This ensures reliable plating, strong annular rings and long-term performance.

Manufacturer rules. Most PCB shops follow practical guidelines of at least 8mils drill-to-copper spacing and aspect ratios no greater than 10:1. Staying within these limits keeps fabrication straightforward, yields high and costs reasonable.

HDI designs. In high-density interconnect (HDI) designs, spacing can sometimes be reduced to 7–7.5 mils and aspect ratios pushed up to 15:1. However, this requires advanced processes such as laser drilling, sequential lamination and specialized plating. These capabilities are not standard among all fabricators, and when available, come with higher cost and longer lead times.

Consequences of Ignoring the Rules

Ignoring the minimum drill-to-copper clearance and aspect ratio rules can cause serious problems. At the design review stage, fabricators may reject the board outright, forcing redesigns and delays. Even an accepted design may be reclassified as an HDI build, which significantly raises costs and extends lead times because of the need for specialized drilling, plating and inspection. Additionally, high-aspect-ratio holes are harder to plate consistently, leading to thinner copper, voids or cracks that reduce long-term reliability. In mission-critical applications, these weaknesses can cause field failures such as opens, shorts or barrel cracks – problems that could have been avoided by following the basic clearance and aspect ratio guidelines.

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PROMPT **DISCIPLINE**

AI 'Hallucinates.' Why That's Actually Good News.

Without the right context, AI gives answers that sound right but can quietly derail manufacturing decisions.

by SEAN PATTERSON

It's 9:15 AM on a Tuesday, and Maria – your rising star process engineer – is about to make a $50,000 mistake.

She asked AI a simple question: "What's the recommended cure temperature for FR-4 laminate?" The answer came back instantly, confidently: "Cure at 180°C for 90 minutes." She's two clicks away from updating the work instruction that will go to the production floor for today's run of 24 panels.

Then something makes her pause. Maybe it's the fact that 180°C seems high. Maybe it's muscle memory from her mentor telling her to always verify. She opens the material datasheet.

The actual spec? 170°C ±5°C for 60-75 minutes. AI was close – but in PCB manufacturing, "close" means scrapped boards, delayed shipments and a very uncomfortable conversation with your customer.

Here's what just happened: AI didn't lie to her. It didn't malfunction. It provided her with a statistically plausible answer based on patterns in its training data. But it lacked the specific context of her material, her process, her customer's requirements. And without that context, even the best AI becomes a very expensive guess.

If you tried AI after reading my first article and got results that felt unreliable, you probably blamed the AI. "It hallucinates." "It makes things up." "I can't trust it."

What most people miss, however, is that AI doesn't fail because it's broken. It fails because we don't give it the context it needs to succeed.

This article explains one of the most important skills for working with AI: context control. Master this, and AI transforms from an unreliable assistant into a thought partner you can trust. Skip this, and you'll stay frustrated, or worse, you'll stop using AI altogether and fall behind competitors who figured this out.

Let's fix that.

Seeing Things (for the Better)

First, let's clear up what's happening when AI gives you wrong answers.

AI doesn't "know" anything. It's a pattern-matching engine trained on billions of text examples. When you ask it a question, it predicts the statistically most likely response based on patterns it has seen before. It's incredibly good at this – but it has no understanding of truth, no access to your specific datasheets and no concept of what "Class 3 registration tolerance" means in your facility.

Think of it this way: AI without context is like a process engineer walking onto your production floor for the first time. They have general knowledge about PCB manufacturing. They've read the textbooks. They understand the principles. But they don't know *your* equipment quirks, *your* material suppliers, *your* customer specifications or the tribal knowledge your team has built over years of production runs.

Would you trust that engineer to update work instructions on day one? Of course not. You'd spend time teaching them the context: "Here's how we run this line. Here's why we deviate from the standard process. Here's what the datasheet doesn't tell you."

That's exactly what you need to do with AI.

The good news? This isn't an AI limitation – it's a design feature. AI's flexibility to work across domains only works because it doesn't come preloaded with assumptions about your specific situation. Your job is to provide the context that makes its pattern-matching abilities useful.

And here's the critical insight: the engineers who get reliable AI outputs aren't using better AI – they're providing better context.

This is a learnable skill/art. And once you have it, AI stops being unreliable and starts being indispensable.

The Anatomy of a Reliable Prompt: Building on CRIT

In our December 2025 article, I introduced the CRIT framework: Context, Role, Interview, Task. If you tried it, you probably got better results than you were getting before. But you might have also wondered: "How much context is enough? What should I include? What can I skip?"

Let's refine that framework with specific guidance on what makes context actually work.

Context isn't just background information – it's constraint definition. When you provide context, you're telling AI what boundaries to work within, what assumptions are valid and what success looks like in *your* environment.

Here's what effective context includes:

1. **Specificity over generality.**

Bad: "I'm working on a PCB."
Good: "I'm designing an 8-layer HDI board with 0.4mm pitch BGAs for automotive Class 3 applications."

Why it matters: AI has patterns for "PCB" that span everything from hobby projects to aerospace. Narrow the domain, get better answers.

2. **Your constraints, not industry defaults.**

Bad: "What's the recommended drill size?"
Good: "Our shop's smallest reliable drill is 0.25mm. The customer requires 0.2mm finished holes. What drill size accounts for plating thickness?"

Why it matters: AI knows industry standards. What it doesn't know is *your* equipment capabilities and limitations. That's the context that makes answers actionable.

3. **The outcome format you actually need.**

Bad: "Tell me about impedance control."
Good: "Give me a 3-step troubleshooting checklist I can hand to my technician when we see impedance drift on 50-ohm traces."

Why it matters: You're not writing a research paper. You need outputs you can use Monday morning. Specify the format, and AI delivers it.

4. **What you've already tried (if troubleshooting).**

Bad: "Why is my solder mask cracking?"
Good: "I'm seeing solder mask cracking after reflow. Already verified cure temperature (150°C × 45min), checked for contamination, and confirmed material is within shelf life. What else should I investigate?"

Why it matters: AI won't waste time suggesting what you've already eliminated. And if you are unsure of what more to share, use the "Interview" step in CRIT – you're teaching AI what you know.

Let me show you this in action with a real manufacturing scenario.

Before and after: The same question, radically different results.

Let's say your drill breakage rate just jumped to 3.8% from 0.5% over the past two weeks. You're running 10 mil drills through standard 63 mil FR-4, and suddenly you're breaking 7-8 drills per shift instead of 1-2. That's costing you money in drill replacement, machine downtime and scrapped panels. You decide to ask AI for help.

Version 1: The vague prompt. "Why are my drills breaking?"

AI's response:

> "Drill breakage can result from multiple factors: improper feed rates, spindle speed issues, dull bits, material hardness variations, inadequate chip evacuation, entry material condition or backup board quality. I'd recommend reviewing your drill parameters and conducting a systematic process audit to identify the root cause."

Is that helpful? Technically accurate, sure. But you already knew all that. You just got a textbook answer that doesn't move you forward. You're back to square one, and drills are still breaking.

We have a free vector graph simulation of this on our website.

Version 2: The context-rich prompt. Now, let's apply the four context principles:

CONTEXT: I'm running a Schmoll drill machine on a Class 3 multilayer board. Standard 63 mil FR-4 material, 10 mil drill diameter, 8-layer stack. Breakage rate was stable at 0.5% for six months. Two weeks ago, it jumped to 3.8% and hasn't recovered. Drills are breaking at depth (approximately 40-47 mils into the stack), not at entry or exit.

ROLE: Act as an expert PCB drill engineer who has prior experience at a laminate supplier and a drill bit distributor

SPECIFICS: Using carbide micro-grain drills, same supplier/lot as past 3 months. Spindle speed 120k RPM, feed rate 80 ipm (chip load 0.33 mils/flute). Breaking occurs randomly across the panel, not concentrated in any specific zone. Running 18-up panelization.

CONSTRAINTS: I've already verified spindle runout (within 0.2 mils), confirmed coolant flow and pressure, checked entry/backup board condition, and validated drill program parameters haven't changed. Tried fresh drills from new box – same breakage rate. Material is from the same supplier, but could be a different lot.

INTERVIEW: Ask me questions (ONE AT A TIME) to provide you with more context in order to accomplish the task.

TASK: Provide three specific root-cause hypotheses ranked by probability, with a test I can run THIS WEEK to confirm or eliminate each one. I need to get breakage back under 1%.

AI's response: Note: this is the real AI output.

> "Given the sudden onset, depth-specific breakage pattern, and the fact that you've eliminated tooling and machine variables, here are three hypotheses ranked by likelihood:
>
> 1. **Chip evacuation degradation**
>
> – Test: Inspect vacuum system integrity. Check if you've had recent increase in hole count per panel that's generating more swarf. Examine broken drill tips under scope for evidence of chip packing.

– Why: Poor chip evacuation at depth causes heat buildup and drill binding. Two-week timeframe could align with a pipe leak or accumulated contamination.

– Action: Inspect vacuum system lines for leaks or blockages. Clear any accumulated swarf from vacuum ports. If breakage improves immediately, implement more frequent vacuum system maintenance checks.

2. **Spindle bearing wear causing vibration at depth **

– Test: Run vibration analysis on spindle at operating RPM. Check for frequency spikes. If unavailable, drill test pattern at reduced RPM (100k) and see if breakage rate changes.

– Why: Two weeks suggests gradual bearing degradation. Vibration becomes more pronounced at depth where drill deflection is maximum. Spindle runout might be within spec at rest but develops harmonic vibration under load.

– Action: Check spindle service hours. If approaching PM interval (typically 1500-2000 hours for micro-drilling), schedule bearing replacement.

3. **Wrong Material**

– Test: Request Certificate of Conformance for current material lot vs. previous lot. Inspect internal quality records. Compare Tg and resin system specs. Alternatively, run identical drill program on a panel from old material lot if you have archive samples.

– Why: Breakage at 40-47 mil depth suggests the drill is encountering harder material mid-stack where glass fabric density is highest. Higher Tg material would increase cutting forces at that depth.

– Action: As Tg increases, reduce feed rate 15-20% and monitor breakage.

Start with material lot verification takes 30 minutes. If C of C shows material change, the feed rate adjustment test can run today."

See the difference?

Version 2 gave you an action plan you can execute this week. It prioritized hypotheses based on your specific process and equipment. It didn't waste time on things you'd already eliminated (e.g., drill program, entry material). It recognized the urgency (a five-day deadline to return to <1%) and provided the fastest test first (30 minutes to check material certificate of conformance).

Same AI. Same "question." Completely different value.

Figure 1. A moment of pause at the work instruction screen shows why AI answers without context can turn "almost right" into an expensive manufacturing mistake.

When to Trust AI (and When to Verify)

Getting reliable outputs doesn't mean blindly trusting everything AI tells you. It means knowing when AI's strengths align with your needs, and when you need to verify.

Here's a practical framework for commercial AI that most SMB use.

AI excels at (generally trustworthy):

- **Pattern recognition and analysis:** "Review this failure data and identify trends."
- **Drafting and formatting:** "Convert my meeting notes into a status report."
- **Brainstorming and alternatives:** "Give me five ways to approach this design constraint."
- **Explaining concepts:** "Explain impedance matching like I'm teaching a new technician."
- **Process documentation:** "Create a troubleshooting checklist for this equipment."

AI struggles with (always verify):

- **Math and calculations:** AI is pattern-based, not computational. Use it for explanation, not calculation.
    - **Solution 1:** Use coding-capable AI (Claude Code, ChatGPT with Code Interpreter) to write and

execute Python scripts for calculations.

  - **Solution 2:** Ask AI to explain the formula, then verify the calculation yourself or use a spreadsheet.
  - **Solution 3:** Have AI generate the calculation logic, but always verify the math with a second method.

- **Current facts or data:** It doesn't browse the internet every time.
  - **Solution 1:** Ensure the AI you're using has web search enabled with source citations for information less than 1 year old. Add "use internet" in your prompt to enforce.
  - **Solution 2:** Use AI to draft the query, then manually search databases (e.g., Digi-Key) for pricing.
  - **Solution 3:** Ask AI for the approach/methodology, then plug in current data yourself from verified sources.

- **Your specific procedures:** It doesn't know your company's actual processes unless you teach it.
  - **Solution 1:** Upload procedures into the AI's context window at the start of each session.
  - **Solution 2:** Create a custom GPT or Claude Project with your company documents preloaded.
  - **Solution 3:** Reference specific procedure documents by name in your prompt and paste relevant sections inline.

- **Safety-critical decisions:** Never trust AI for decisions that could cause injury or catastrophic failure without expert review.
  - **Solution 1:** Use AI for initial analysis and recommendations, then require signoff from a qualified engineer or safety officer.
  - **Solution 2:** Implement a "two-person rule" where AI output plus a human expert must both agree before action.
  - **Solution 3:** Limit AI to advisory role only – it suggests options, humans make final safety-critical decisions.

- **Regulatory compliance:** AI can explain regulations but shouldn't be your sole source for compliance verification.
  - **Solution 1:** Use AI to interpret regulations, then verify against official regulatory documents or legal counsel.
  - **Solution 2:** Have AI draft compliance checklists, then human validate each item against current standards (IPC, UL, etc.).

- **Solution 3:** Employ AI for gap analysis of your processes but confirm findings with a compliance expert or auditor.

The 30-Second Verification Habit

For anything that matters, run this quick check before acting on AI's output:

1. **Sanity test:** Does this answer make intuitive sense based on your experience? If something feels off, it probably is.
2. **Source check:** For any specific claim, number or specification, can you verify it against a datasheet, standard, or known reference? If the AI indicates "cure at 180°C," verify the material specification until you trust the AI's use.
3. **Risk assessment:** What happens if this answer is wrong? If the consequence is high (e.g., production impact, customer relationships, safety), verify it with a second source or a subject-matter expert.

This isn't about distrusting AI, it's about using it intelligently. You wouldn't implement a process change based solely on one engineer's opinion, even an expert. You'd verify. Apply the same standard to AI.

The goal is confident use, not blind faith.

What You Do Tomorrow Morning

Here's your assignment: Pick one task you're facing this week. It could be a quality issue, a design decision, documentation you need to create or a process you're trying to optimize.

Don't just ask AI about it. Use what you learned in this article:

Tomorrow's prompt template:

```
CONTEXT: [Your specific situation – be detailed]– What are you working on?
– What constraints are you operating within?
– What's the current state vs. desired state?

SPECIFICS: [The exact details that matter]– Measurements, part numbers, specifications
– Your equipment/material/process specifics
– Timeline or urgency if relevant

ALREADY TRIED: [What hasn't worked]– What have you already eliminated?
– What approaches have you tested?

TASK: [The exact output format you need]– Be specific about format (checklist, analysis, options, etc.)
– Include any deadline or urgency
```

– Specify level of detail needed

[Your specific question here]

That's it. Use this template once tomorrow. See what happens.

You'll get better results than you did before you read this article. Not because AI got smarter – because you did.

And here's what you'll discover: context control isn't just about getting better AI outputs. It's about clarifying your own thinking. The act of defining context forces you to articulate the problem more precisely. Sometimes, just writing the context-rich prompt helps you see the solution before AI even responds.

That's the real skill you're building here. It's not prompting – it's structured problem-solving.

Start tomorrow. One prompt. Full context. Build the habit.

In the next article in this series, we'll build on this foundation and show you how to move from chatting with AI to automating workflows – taking the prompts you've mastered and making them work for you in the background while you focus on higher-value problems. That's Pillar 2: AI in Business Workflows.

But first: practice your context control. You can't automate what you haven't mastered manually.

About this Series

This is the second article in a series exploring practical AI adoption for PCB design and manufacturing professionals. We're building on the Three Pillars framework from article 1:

Article 1: Don't Buy AI, Learn AI (Pillar 1 foundation – why learn vs. buy)
Article 2: Context is King (Pillar 1 core skill – getting reliable outputs) ← You are here
Coming next: Building workflow automations without coding (Pillar 2).

This isn't about buying AI solutions – it's about developing your team's AI capabilities.

SEAN PATTERSON is an accomplished executive with extensive C-suite experience across CRO, COO, and CTO roles who now specializes in humanizing artificial intelligence implementation in business environments, particularly manufacturing; sean@crossgen-ai.com.

Patterson's unique approach to AI implementation stems from his multifaceted leadership experience in the PCB industry, including serving as COO and CTO & head of AI at Summit Interconnect, various senior positions at TTM Technologies, and CRO of Nano Dimension. He built Amazon's tractor trailer division and healthcare platforms. He currently serves as COO of StartGuides, providing military technology working backwards from the soldier. He is also on several nonprofit AI advisory boards in education.

Patteson brings practical insights into how PCB manufacturers can approach AI adoption strategically. His methodology emphasizes cultural adoption from the top, employee empowerment, and then automation. His approach to AI implementation is captured in his often-quoted principle: “AI adoption is not something a leader can delegate.”

Patterson holds a master’s in nuclear science and engineering from MIT and a bachelor’s in systems engineering with a focus on robotics from the United States Naval Academy. He is keynoting the PCB Management Session: Strategic Leadership in the Age of AI, New Technology Adoption, and Talent Scarcity, at PCB East in April.

ENVIRONMENTAL **TESTING**

Vibration Analysis of PCBs for Critical Applications

Laser doppler vibrometry enables simultaneous measurement at dozens of points across populated PCBs, revealing component-level failure risks that accelerometers miss.

by ELADIO MONTOYA, PH.D. and ÓSCAR R. ENRÍQUEZ, PH.D.

Printed circuit boards (PCBs) used in space, defense, aeronautics and transportation cannot tolerate in-service failures. Before deployment, these systems must pass environmental qualification tests, including vibration, shock, thermal cycling, radiation, electromagnetic compatibility (EMC) and ingress protection.

In vibration testing, PCB failures often arise from:

- Solder joint cracking
- Component detachment
- Pad delamination
- Trace fracture.

These failures are all linked to dynamic response under vibratory loading and can compromise an entire mission or system.

Understanding how PCBs actually deform and vibrate under load is essential to achieving uncompromised reliability.

Why Accelerometer-Based PCB Testing Falls Short

Because populated PCBs exhibit complex mass distributions, accurately modeling their vibration modes and the resulting stresses is inherently difficult. Standard tools like accelerometers provide overall board motion but cannot measure vibration at individual components, where failures originate.

Populated PCBs are not uniform flat plates. They have complex mass and stiffness distributions caused by components, solder joints and copper traces. This makes modeling and simulation highly uncertain.

A laser doppler vibrometer permits noncontact vibration measurement, but conventional scanning LDVs capture only one point at a time. This results in long acquisition times, repeated excitations and risk of missing localized behaviors.

Laser Vibrometry

A novel approach uses massively parallel laser doppler vibrometry, based on laser radar and interferometric measurement principles, to capture dozens of measurement points simultaneously. This method provides:

- Noncontact measurement (no mass loading, no wiring)
- High spatial resolution across the surface of the PCB
- Synchronous data across all points without stitching or repeated sweeps
- Clear visualization of vibration behavior at the component level.

It is particularly suited to environments in which PCBs must withstand random vibration, sine vibration, launch loads, weapon recoil, high-speed rail dynamics or continuous fatigue.

Test Setup: PCB Under Vibration Excitation

To demonstrate the viability of LDV, a populated PCB **(Figures 1-2)** was mounted on a linear shaker with vibration applied perpendicular to the plane of the board **(Figure 3)**. Key setup parameters included:

- Vibration driven using the analog output of a novel LDV, amplified for sufficient excitation.
- To determine the eigenmodes of the PCB, it was excited with a chirp signal ranging from DC to 600Hz.
- 65 simultaneous LDV measurement points distributed across components and PCB surface.

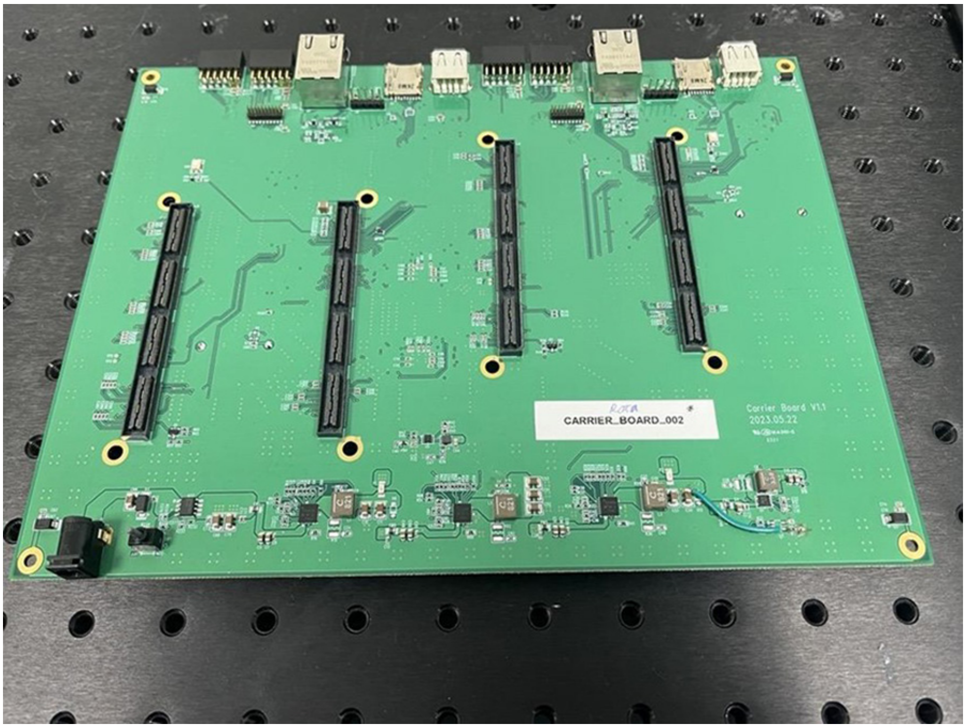

Figure 1. Carrier board topside.

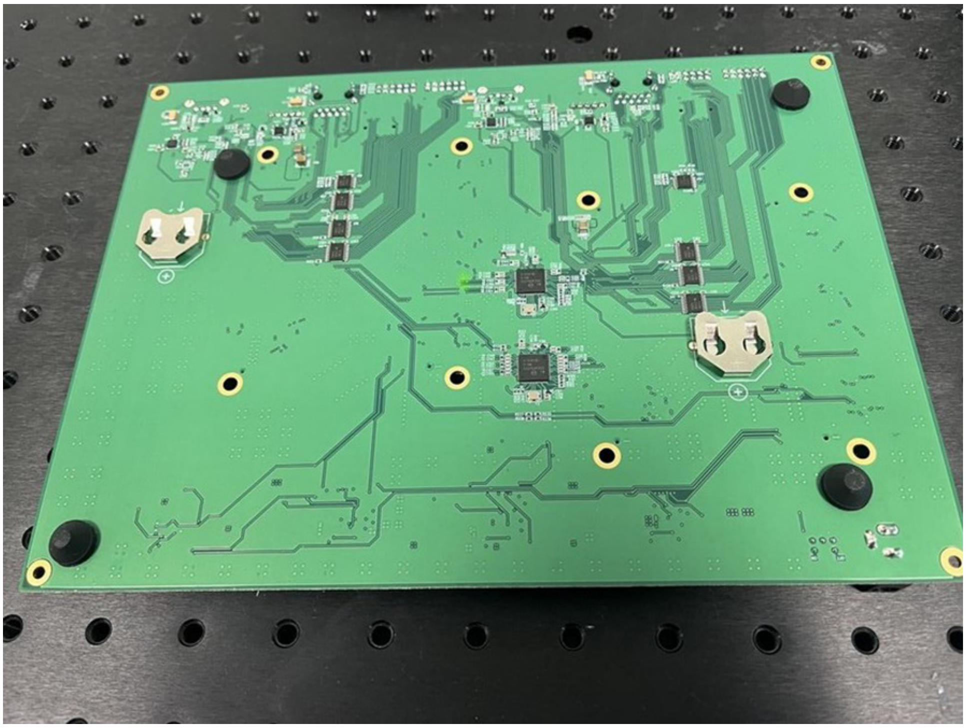

Figure 2. Carrier board bottom side.

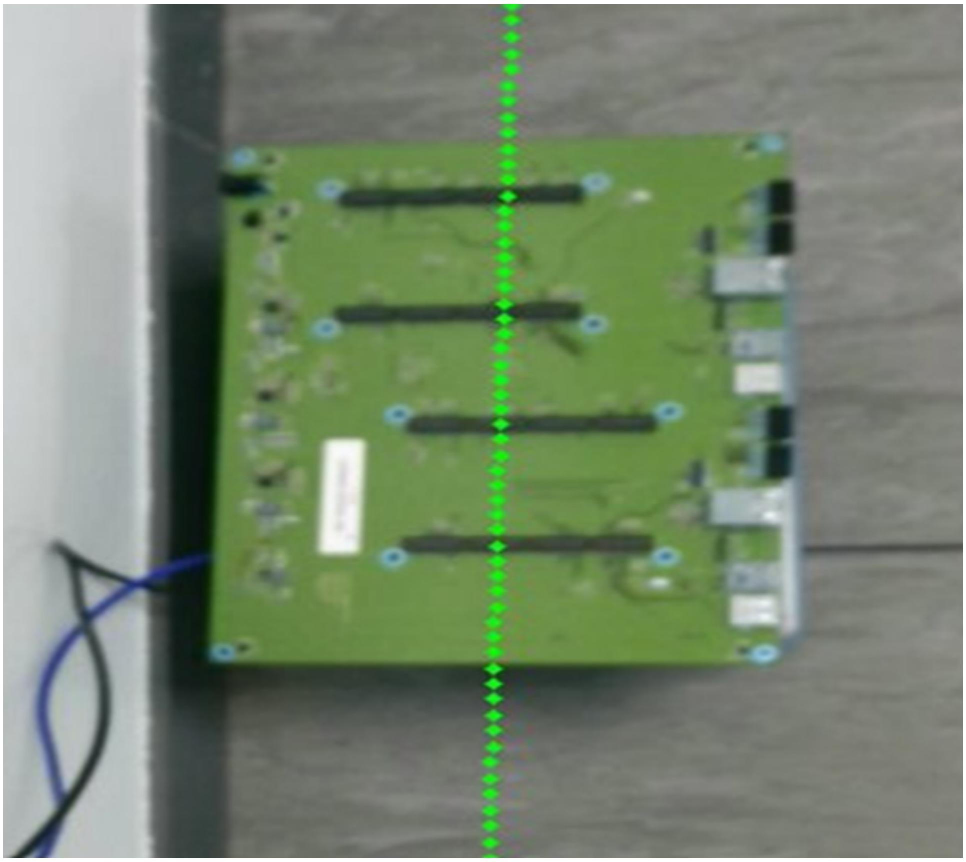

Figure 3. PCB under test, imaged with integrated camera. The line of dots represents the positions of the 65 simultaneous measurement points used for vibration acquisition.

The frequency response revealed three distinct resonance peaks at approximately 150Hz, 200Hz and 250Hz. The shaker was excited individually at each of these frequencies, and the PCB vibration response was scanned. **Figure 4** shows the resulting vibration velocity maps, overlaid with a semitransparent RGB image of the PCB for comparison.

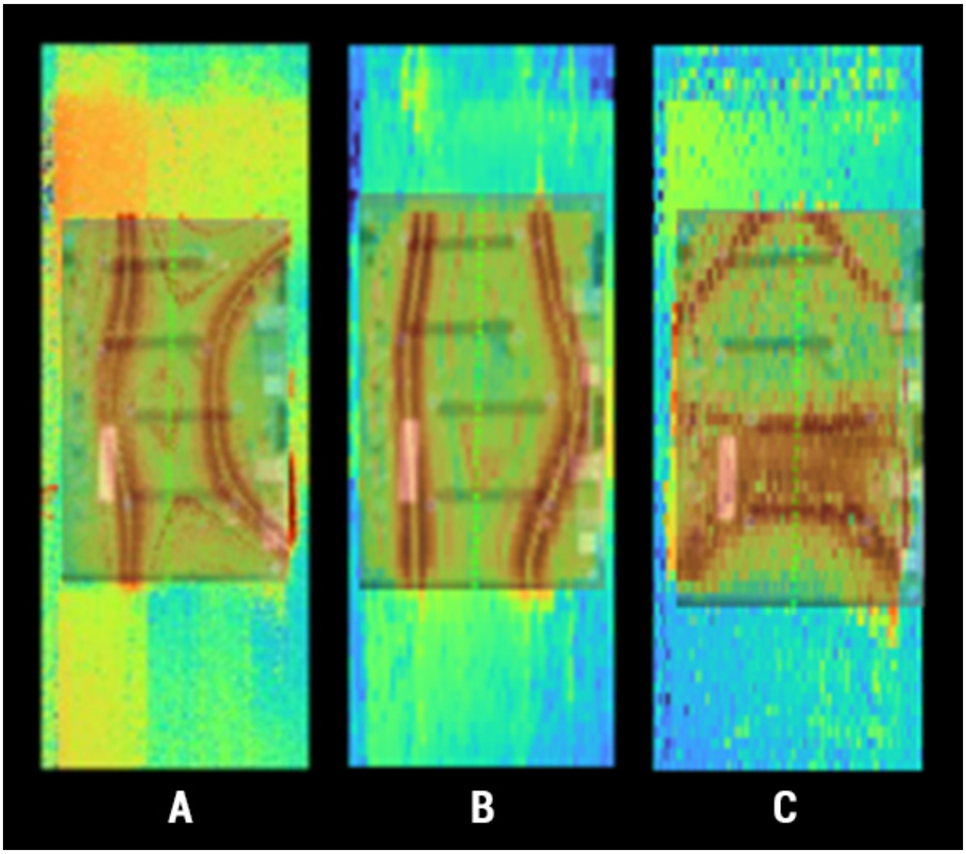

Figure 4. Vibration modes of PCB when excited at 150Hz (a), 200Hz (b) and 250Hz (c).

Critical Observations

The vibration patterns differed significantly from those expected in an ideal flat plate. Components stiffened surrounding regions, altering local deflection patterns. Nodal lines were clearly visible at 150Hz and 200Hz **(Figure 5)**. These high-density modal analyses reveal that component placement on a PCB must be carefully considered. In particular, components located along or across regions of maximum vibration velocity are more susceptible to detachment or solder failure.

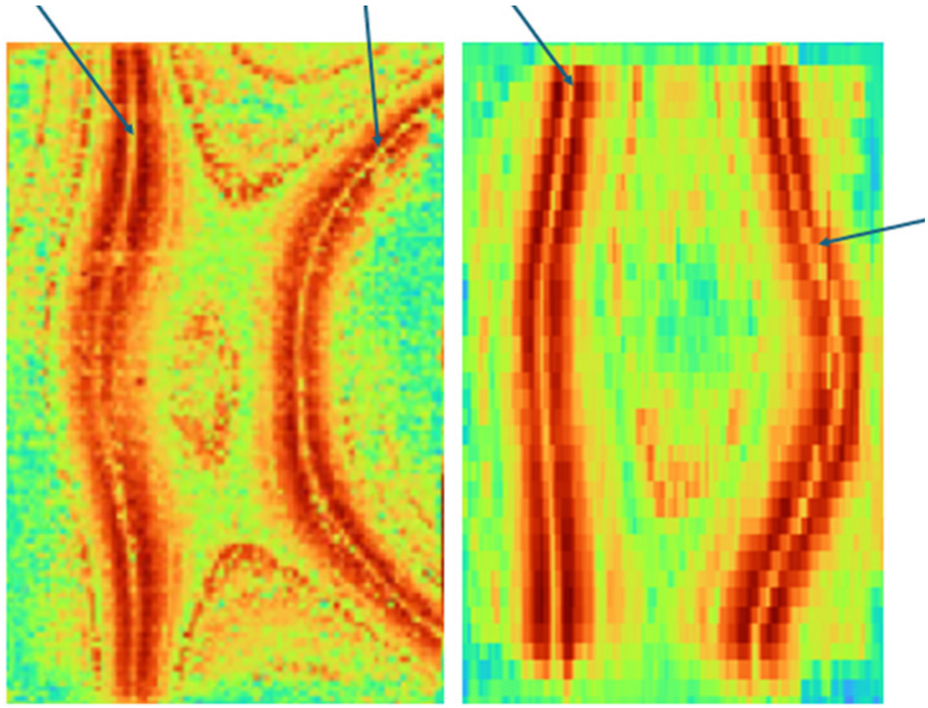

Figure 5. Detail of the nodal lines measured at 150Hz and 200Hz.

Components positioned along high-velocity regions or near nodal lines face a higher risk of solder fatigue, pad delamination, or fracture during launch, flight, transport or impact conditions.

While this technique provides high-density operational deflection data, it is not yet a complete experimental modal analysis. It enables engineers to see how real hardware behaves under load early in the design and qualification process, however.

Why This Matters for Space, Defense, and Aeronautics

For teams developing spacecraft avionics, missile guidance systems, UAV electronics, railway signaling, defense radar systems or flight control computers, this approach offers tangible benefits:

- No accelerometers required. No added mass, no wiring
- Quantitative vibration data at the component level
- Detection of failure-prone areas before qualification testing
- Better correlation between simulation and hardware behavior
- Supports PCB layout optimization for harsh environments.

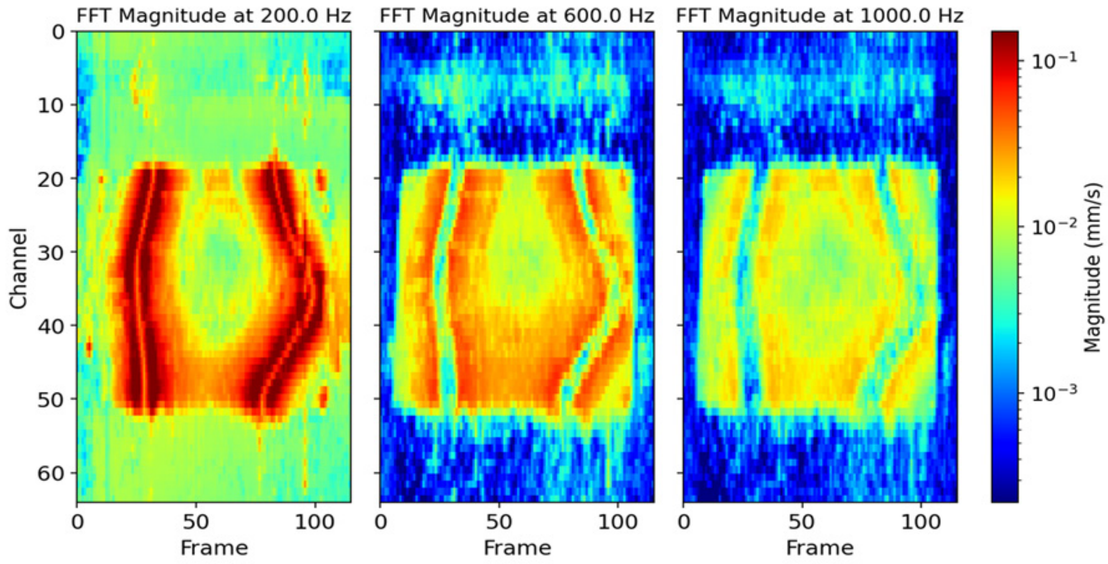

Figure 6. FFT magnitude at 200Hz, 600Hz, and 1MHz.

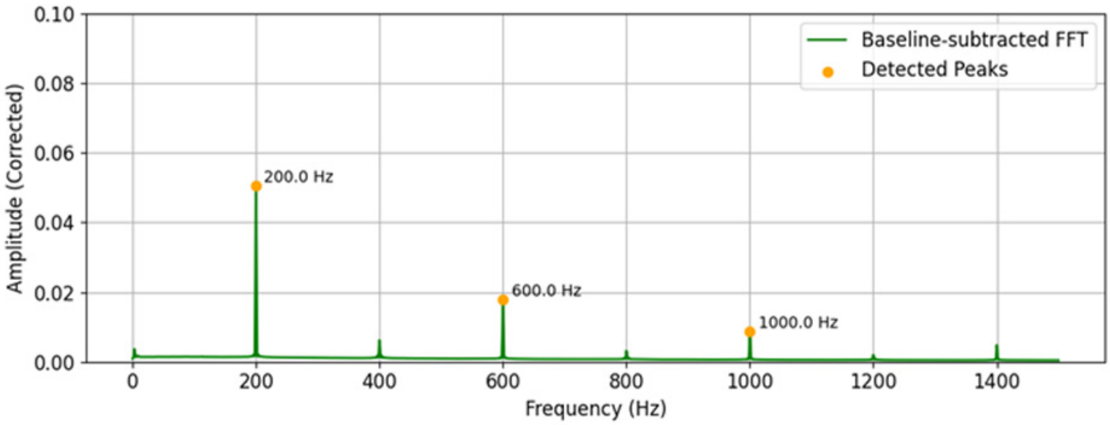

Figure 7. Baseline-subtracted average FFT spectrum with detected peaks.

Summary

In vibration-critical applications, understanding how a PCB deforms under excitation is essential. Using massively parallel LDV based on laser radar and interferometric measurement, engineers can now observe vibration velocities across components, not just board-level motion.

This high-density vibration-response data can serve as the basis for a subsequent full modal analysis with resolution and speed that exceed those of traditional tools.

Future technical notes will demonstrate full modal parameter extraction workflows.

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Force Majeure

A holiday-season scramble exposes how “always on” offshore manufacturing ideals collide with real-world AXI limits.

A YULETIDE SURPRISE, courtesy of The Anthill. The same Anthill that wouldn’t answer emails, phone calls, texts or carrier pigeons the other 332 days of 2025. Things change, and snubs become embraces overnight when year-end revenue is threatened. Lucky us. Their AXI machine was down indefinitely; ours was definitely up. Meanwhile, an impossibly unrealistic, unreasonable, irrational name-brand tech superstar du jour was expecting results, no excuses, to fulfill a product launch.

This being the season of sharing, the Anthill proposed sharing their misery with us. They asked if our small, energetically earnest staff (13) would drop everything else and forego sleep for, well, the next six weeks. At least until Lent, but in pagan time: forget Christmas, and observe abnormal work hours. You’ll sleep and find leisure when you die, goes the motivational thinking, and, apparently, the Anthill practice. Through unremitting toil shall you be saved is progress made. Scrooge lives. Joy to the world. For the right price.

Once upon a time, when dinosaurs roamed the Earth and youthful male tech leaders were still admired (2011), a leading fruit-emblemed toy company CEO told an inquisitive American president that 24/7/365 mass production of certain specialized electronic devices was impossible in the United States. This visionary supplied indigestion to our president, in the form of dinner table examples of the other side’s manufacturing superiority. Deeper supply chain. Better engineering support. Faster response time. Greater flexibility in making changes. Ability to scale from prototype to pilot build to production faster than anywhere else. Regimented social structure. Unquestioning willingness to work 3000 people 36 hours straight to implement an ECO. Worker docility in the guise of hyper-attentive customer service, a techbros’ wet dream. All the attributes of an anthill. This, proclaimed the famous CEO, was manufacturing as it should be. He insisted to our incredulous president that such characteristics could not be replicated in the United States. The implied truth: we’re lazy, as he defines the term, and they’re not.

So, it was with some measure of irony laced with schadenfreude that we observed the Anthill showing up on our front porch one Tuesday afternoon in a mood distinctly inappropriate for caroling. More like lamentations. And begging: Jesus, Mary and Joseph, desperately looking for a manger that can produce at scale.

They supplied an inkling the evening before, with a 7:10 p.m. Monday voicemail inquiring about our AXI capacity that very week. They were experiencing a sudden demand spike and had been referred to us by another high-volume manufacturer as a potential relief valve for said spike. This and the fact that their own machine elected to take the week off (a needed part was at least one week away from installation) made a stressful situation hair-raising. They wanted to talk with us urgently about our programming and inspection capabilities, as well as the response times for each. The anxious edge in the tone of the voicemail carried with it a strong hit of "immediately." As in "tomorrow."

Normally, I'd save my response for the following morning. Overnight rest gives me time to meditate on a calibrated response to match the customer's ineptitude. Call me old school, but I tend to go off duty somewhere between 5-7 p.m., and request that crises be held until dawn. Something about nourishment. Plus, I reserve my evenings these days for experiments in quantum computing (everyone needs a hobby). But this was the Anthill, and Anthill management believes sleep and regular hours are for weaklings or the habitually indolent (to which their management, by their overseas production decisions, apparently lumps the majority of our American workforce). This same Anthill that said "no" to our approach eleven-twelfths of the year, now hints in their message that "yes" might be a better basis for discussion in this season of giving. I called them back, waiting until after dinner, about 8:30 p.m., when they least expected a call. Then I called. You could hear the surprise in my counterpart's voice, as if he was trying to process an un-stereotypical reality. "Wow, this guy's still working."

Once my voicemail counterpart recognized me and audibly acknowledged my presence, muffled voices could be heard, growing in number and volume. He must have been silently beckoning nearby colleagues to gather as soon as my identity was established. Or perhaps the word "RELIEF" on his caller ID carried its own strange magnetism. Either way, the talismanic effect made people talk loudly and frequently over each other. In its own strange, collective, coercive way, like an anthill.

"Do you have a 5DX?"

"Do you have a programmer? Do you have multiple programmers? Do you have multiple programmers who can program around the clock?"

"Are you open 24 hours per day?"

"Can we drop off product to be inspected at all hours of the day or night?"

"Can you run – inspect – product 24 hours a day?"

"Can you run existing programs developed here by us?"

"How fast can you create new programs?"

Reader, you might have the impression from the order of questions given above that they were asked in an orderly way. You would be wrong. All seven questions listed above were asked simultaneously, creating the verbal equivalent of spaghetti, each question representing strands of pasta, intertwined and not *al dente*. Nothing stuck. Each strand at a different volume, rendering the whole barely intelligible. Cacophony, thy name is Anthill. Anxiety in the face of immutable laws (making the tech titan customer happy, or else) does that. Seven almost-simultaneous questions mostly produced white noise. No word on the blood pressure of those asking questions, but on my end, I could feel the tension rising.

The disembodied voice of their leader asked for silence. Having achieved nothing, he decreed we would meet at our office the following morning. He didn't ask for other meeting options.

And so we did. Four nonsmiling killjoy faces arrived the next morning, all wearing their Anthill windbreakers, transporting their grim world of inflexible deadlines to our seasonally festive conference room. An aroma of cigarette smoke permeated the room. Accompanying them, a minder from the OEM, their customer. Also nonsmiling. He was the Grand Mute: for the next two hours, he barely spoke. Mostly grunts and the occasional facial twitch, signaling approval or opinion, in subtle auction house style. Otherwise, his visage was indecipherable, concealed under a baseball cap, to, I suppose, mask suggestive or overly-exuberant reactions. All part of the act. A different kind of drone. A new way to spell "distrust." Joy to the world.

You could feel the anxiety as they filed into the room, like schoolchildren reluctantly returning to class from recess, having just been informed that milk, cookies and naptime had been cancelled for the duration of the semester. Introductions barely finished when vociferous interruptions worthy of a White House press briefing started in force. Multiple variations of the same questions from the previous night, with two underlying themes: stay open for business around the clock and allow us access to your facility anytime. Clearly, innovation allows no fixed time schedule. Work/life balance? For the birds.

The minder, silent, observed.

First question: Can we bring boards at all hours of the day or night? It is not uncommon for our production line to finish at 2 a.m. Can we deliver boards to your facility at 2:30 a.m.?

Our answer: Yes. Longer answer: Let us know in advance that this will happen, so we can arrange to have proper personnel on standby and prepared to work.

Second question: Can you take the existing AXI programs we've developed and transfer them to your machine?

Answer: Only if your machine matches our machine (nope). Otherwise, we'll need to make a new program.

Third question: Can you create, debug and tune an AXI program for one of our representative boards (60 layers, 16″ x 18″, 600-line-item bill of materials, 20,000 components) in less than four hours?

Answer: Nope. It takes a few days, possibly more, even if we work around the clock.

Fourth question: Really?

And a comment: Our customer won't accept that.

Answer: Really.

Plus our comment: Your customer doesn't have a choice. Whether they accept or not is irrelevant.

At this, the minder's sphinxlike appearance was interrupted by a slight upward curl of the mouth at either end.

Fifth question, regrouping: Can't you give us what our customer wants? This is what they want.

Answer: No, we can't. Better to tell you now. Either your customer doesn't know what they're talking about, or they're testing you. Only you and your customer know the answer to that. We're just test engineers, and life's short. Tech prominence can only push the laws of physics, machines and human beings so far.

The minder remained impassive.

Our unspoken thought: We know an initial negotiating position when we see one, so get real.

Sixth question: Can we sit with you when we choose to do so, and can our customer do the same? We'd like to observe the programming and inspection process in detail.

Answer: Yes, if you insist. Why do you, and especially your customer, want to do this? It's about as spine-tingling as watching tariffs getting paid (note contemporary reference in case we are taken hostage).

Their answer: We want to learn from the process. Maybe you have some tricks or techniques we can apply to our own work.

Real answer: We don't trust you.

Seventh question: Can you give us hourly status updates?

Answer: Do you want us to do the work assigned, or do you want reports? Choose only one.

Their answer: The work, obviously.

Our comment: Good answer.

Thus ended the inquisition. The minder made notes, but otherwise looked serene, mental checklist complete. Feeling supreme at another shining example of cause-and-effect.

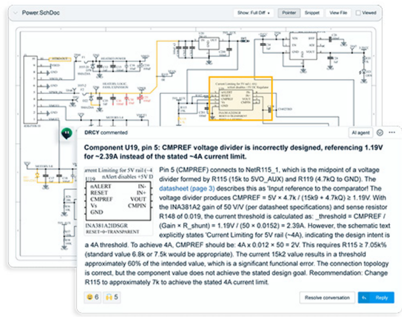
We showed them our AXI system. Explained why it could beat up their AXI system. Told them we were ready to respond with resources, energy, experience and shop time forthwith. As in, now. They liked our style and promised to carry this back to a meeting with their customer to obtain final approval to proceed, which they hinted would come quickly.

The minder gave no hint about his recommendations to management. He departed silently with the Anthill team into the festive afternoon. Quietly terrorizing a supplier was his specialty, and as far as production was concerned, it was the most wonderful time of the year.

To all, a wish for the proper and profitable ruin of your holidays in 2026.

ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.

PCD&F

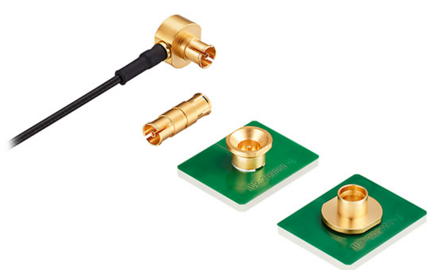


ALLSPICE.IO DRCY AI DESIGN REVIEW AGENT

DRCY AI-powered design review agent is for hardware engineering workflows and automates first-pass schematic and constraint checks. Parses datasheets at scale and cross-references schematics, documented constraints and component data to identify compatibility risks early in the design cycle. Detects issues including incorrect voltage references, pins operating outside specified limits, swapped signals, incorrect packages, reverse-polarity passives, mismatched voltage domains, insufficient drive strength and reset circuitry errors. Designed to surface actionable risks before layout and fabrication.

AllSpice.io

allspice.io



HIROSE PO(M2) SERIES COAXIAL CONNECTORS

PO(M2) Series push-on lock coaxial connectors support multi-board RF applications with operating frequencies up to 6GHz. Uses a three-piece parallel board-to-board configuration with two plug receptacles and an interposer to connect adjacent PCBs in space-constrained layouts. Design supports positional displacement tolerances of

±0.4mm in X and Y directions and 1mm in Z direction to accommodate board misalignment. Supports cable connections using a plug receptacle and locking right-angle jack for mixed interconnect configurations.

Hirose
hirose.com

LUMINOVO ELECTRONICSGPT PROCUREMENT AI AGENT

ElectronicsGPT AI-based tool, for electronics procurement workflows, provides access to component specifications, part alternatives, availability data and supply chain information through a conversational interface. Is based on Luminovo's supply chain datasets and supports queries across millions of electronic components with weekly updates. Functions include datasheet retrieval, extraction of compliance-related technical details and background task execution such as availability monitoring and supplier risk alerts. Available for free.

Luminovo
luminovo.com

OMRON P6K RELAY SOCKET FOR G6K SERIES

P6K surface-mount relay socket is compatible with Omron's G6K PCB terminal-type relay series, including G6K-2P and G6K(U)-2P-Y models. Matches G6K terminal layout and mating structure to support PCB assembly and relay replacement without soldering. When paired with a G6K relay, supports repeated insertion and removal with no increase in contact resistance after 50 cycles.

Omron Electronic Components
components.omron.com

SEICA VALID SL ICT AND FUNCTIONAL TESTER

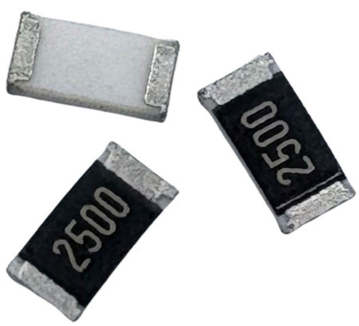
Valid SL in-circuit and functional test system is for high-channel-count electronics testing. Uses a cable-free architecture with 128-channel scanner cards, supporting configurations exceeding 4,480 channels. It supports single-stage and dual-stage test area configurations and multi-job operation through Seica's latest VIVA software interface. Integrates streamlined internal hardware access and supports scalable automation for high-volume and high-reliability test environments.

Seica
seica.com

STACKPOLE RMCA AUTOMOTIVE-GRADE THICK-FILM CHIP RESISTORS

RMCA automotive-grade thick-film chip resistors are surface-mount components qualified to AEC-Q200 for automotive electronic applications. Are manufactured on dedicated automotive production lines using controlled materials and process parameters to support stable resistance performance under automotive operating conditions. Includes RMCA-HP and RMCA-UP variants with power handling approximately two to three times higher than standard RMCA devices of the same size. Come in multiple case sizes, resistance values and tolerance options.

Stackpole Electronics
seielect.com



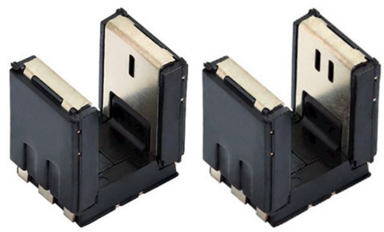
STACKPOLE RNAN THIN-FILM CHIP RESISTORS

RNAN series thin-film precision chip resistor line uses an aluminum nitride substrate for higher thermal conductivity than alumina substrates, enabling increased power density in thin-film resistor designs. Supports power ratings of

0.5W in 0603, 1W in 0805, 2W in 1206 and 6W in 2512, with controlled hot-spot and terminal temperatures. Are intended for high-power, space-constrained applications requiring thin-film resistance characteristics.

Stackpole Electronics

seielect.com

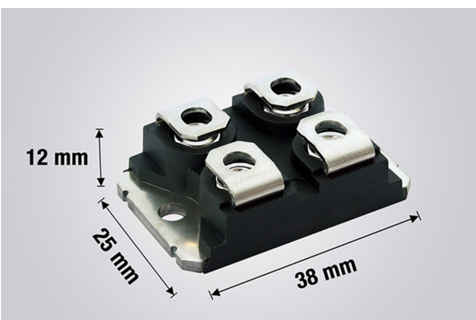


VISHAY VT171P AND VT172U TRANSMISSIVE SENSORS

VT171P (single-channel) and VT172U (dual-channel) surface-mount transmissive sensors are for position sensing in industrial, consumer and telecom applications. Devices integrate an infrared emitter and phototransistor detector operating at 950nm and are housed in a 5.5mm × 4mm × 5.7mm package with increased dome height for added vertical clearance in turn-and-push and code-wheel designs. Typical output current is 1.5mA with a 3mm gap width and 0.3mm apertures, with rise and fall times of 14ms and 21ms. VT172U supports dual-channel detection for direction sensing, while both devices support motion and speed detection in encoders, automation systems, appliances and broadband equipment.

Vishay Intertechnology

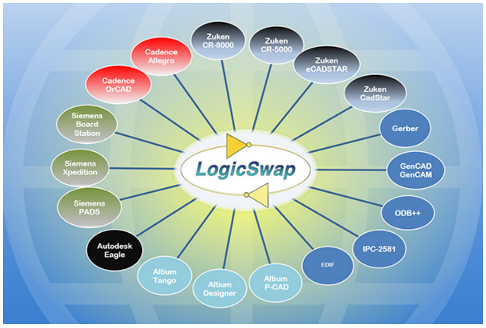
vishay.com



VISHAY 100V GEN 2 TMBS RECTIFIER MODULES

Gen 2 TMBS rectifier module series consists of 100V trench MOS barrier Schottky devices for industrial power conversion. The modules are housed in a fully insulated, industry-standard SOT-227 package and feature forward voltage drops as low as 0.83V with negligible reverse recovery charge. Available configurations include dual-diode parallel modules rated at 100A, 200A and 400A, as well as a 150A single-phase bridge. Devices support operation up to +150°C and are used in high-frequency converters, industrial SMPS, welding equipment, telecom power systems, 48V battery-powered vehicles and battery blocking applications.

Vishay Intertechnology
vishay.com



ZUKEN ORCAD TO ECADSTAR MIGRATION MODULE

OrCAD to eCADSTAR migration module converts PCB layouts, schematics and libraries from Cadence OrCAD into Zuken's eCADSTAR PCB design environment. Supports automated conversion of complete PCB projects, including associated design libraries, to enable continued development without recreating legacy designs. Comes at no cost to licensed eCADSTAR users and includes documentation and technical support provided by LogicSwap Solutions.

Zuken
zuken.com

CA

BOLD LASER AUTOMATION LTX1260A 3-D INSPECTION AND MEASUREMENT SYSTEM

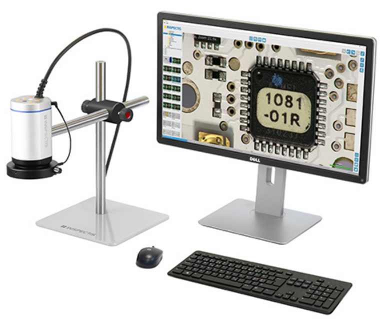
LTX1260A noncontact 3-D inspection and measurement system, for high-precision and delicate components, combines Keyence LJ-X8020 3-D scanner with TMX-5006 profile measurement platform to support automated inspection of surface condition and geometric profiles. Supports dual-station operation for 3-D contamination detection and profile measurement and includes semi-automated fixturing with rotary and linear stages. Integrated data capture supports CSV and Excel export, with an automation-ready architecture for production environments.

Bold Laser Automation
boldlaserautomation.com

INOVAXE INOHD ULTRA-HIGH-DENSITY SMART STORAGE SYSTEM

InoHD is an ultra-high-density smart storage system for SMT and electronic components. Uses servo-driven mobile shelving with integrated sensing and pick-to-light guidance to eliminate fixed storage aisles. Supports storage densities of up to 310 SMT reels per square foot and accommodates more than 10,500 reels within a 4' × 8' footprint. Provides guided access with real-time inventory verification and supports integration with MES and ERP systems.

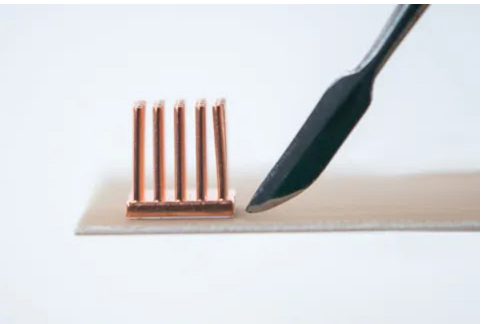
Inovaxe
inovaxe.com



INSPECTIS F40/F40S FULL HD DIGITAL MICROSCOPE

F40/F40s is a full HD digital microscope system for high-resolution optical inspection. Uses an upgraded image sensor with a motorized 40:1 zoom lens and supports full HD video at 60fps with low latency. Features include enhanced sensor sensitivity and dynamic range, fast autofocus, a 7-blade aperture and a free working distance of 226mm. Provides up to 30:1 optical zoom with 1.3× digital zoom and supports integration with Inspectis utility and metrology software.

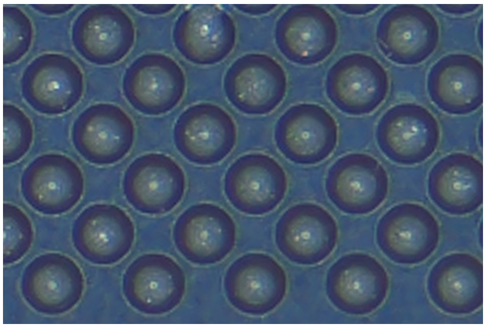
Inspectis
inspect-is.com



MASTER BOND EP54TC ELECTRICALLY INSULATING EPOXY

EP54TC two-component, electrically insulating epoxy is for heat sink bonding and thermal management applications. Delivers thermal conductivity exceeding 6W/(m·K) and uses a 5-30μm filler to support thin bond lines and void filling, achieving thermal resistance of 5-7×10^{-6}K·m²/W. Exhibits a tensile modulus above 1 million psi at room temperature and operates from -73° to +204°C. Supports a recommended cure of 2 hr. at 80°C with a 2-4 hr. post cure at 90°-125°C and comes in ounce through gallon kit sizes.

Master Bond
masterbond.com

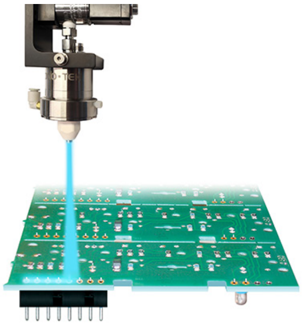


SHENMAO PF606-P266J JET DISPENSING SOLDER PASTE

PF606-P266J high-speed jet dispensing solder paste supports noncontact solder deposition and maintains process stability across a range of jetting parameters. Halogen-free flux system. Supports solder powders from Type 5 through Type 7. Available alloy options include SAC 305, high-reliability alloys for automotive and industrial electronics and low-temperature alloys.

Shenmao

shenmao.com



SONO-TEK SELECTAFLUX 3 ULTRASONIC FLUXING SYSTEM

SelectaFlux 3 selective ultrasonic flux spray system, for selective soldering applications, is offered as a retrofit compatible with major selective solder platforms. Optional flow monitoring module provides noncontact flux volume measurement with ±15% accuracy, per-board flux volume recording, data logging and flow alarms when rates fall outside defined limits. Supports process monitoring and traceability in selective solder operations.

Sono-Tek Corp.

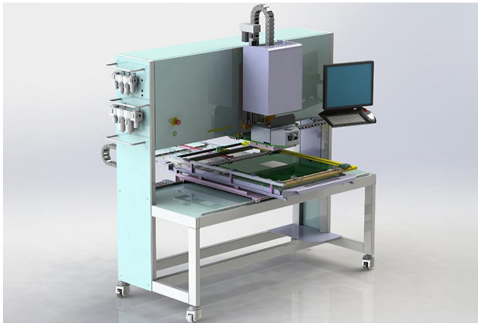
sono-tek.com

TRI TR7600FB SII 3-D AXI

TR7600FB SII 3-D automated x-ray inspects fine-pitch BGAs, multilayer boards and system-in-package (SiP) devices. Newly developed x-ray imaging structure positions x-ray tube close to board surface without structural interference to support detailed internal inspection. Integrates AI-based inspection algorithms with metrology-based measurement and supports AI smart programming.

Test Research Inc.

tri.com



VJ ELECTRONIX SUMMIT LT150 REWORK SYSTEM

Summit LT150 rework system for large, high-density electronic assemblies supports components up to 150mm and PCB sizes up to 24 × 36", with optional support for larger formats. Features large field-of-view vision system for full component visibility and scaled top and bottom heating with dual PID control. Provides increased clearance for tall connectors, heat sinks and power modules while maintaining uniform thermal performance during rework.

VJ Electronix

vjelectronix.com

VJ ELECTRONIX XQUIK V X-RAY COMPONENT COUNTER

XQuik V component counter and inventory verification system uses high-resolution x-ray imaging with increased source power and includes automatic load drawer for reel handling. Integrated barcode camera associates reel identification with count data. Supports inventory control workflows requiring accurate component counts and traceability.

VJ Electronix

vjelectronix.com

YAMAHA MOTOR YRH10W HYBRID PLACER

YRH10W wide-type hybrid placement system supports semiconductor die bonding and surface-mount component placement on a single platform. Accommodates 12" wafers and printed circuit boards up to 510 × 460mm. Combines bare-die handling and SMT placement, supporting bare-chip placement speeds of up to 14,000cph with placement accuracy of ±15μm.

Yamaha Motor
yamaha-motor.com

In Case You Missed It

Circularity

"AI-Enhanced Sorting Enabling Direct, High-Purity Urban Mining of Tantalum: A Novel Pathway from E-Waste to Critical Materials"

Authors: D. Xia, *et al.*

Abstract: Tantalum's supply chain instability demands efficient urban mining from e-waste. Here, the authors present an AI-enhanced process that combines intelligent sorting with sustainable hydrometallurgy for high-yield/high-purity Ta recovery. A hybrid sorting system, cascading an interpretable convolutional neural network (CNN) with automated multi-energy x-ray transmission (MEXRT) spectroscopy, achieved 99.6% precision and 96.9% recall at 3000 components/hour, resolving the Ta/Nb ambiguity. Spatial activation mapping illustrated the visual sorting mechanism, facilitating feature-driven upgrading. Meanwhile, Canny edge detection and K-edge detection enabled real-time and pixel-wise spectral analysis under multithreaded processing. Downstream, streamlined physical separation and thermodynamically guided reverse leaching selectively recovered Ta with 98.2% efficiency under mild conditions. Advanced characterization using transmission electron microscopy and ion beam analysis revealed a quantifiable core-shell Ta/Ta_2O_5 structure in leached products, guiding calcination into >99.8% pure Ta_2O_5. This work establishes a closed-loop urban mining framework, demonstrating how AI and tailored refining enable a circular economy for critical metals. (*Resources, Conservation & Recycling* 227 (2026) 108717. https://doi.org/10.1016/j.resconrec.2025.108717)

Inspection

"PCB Defect Detection Using Machine Learning: YOLOv5 and Inception v3 CNN-Based Approach"

Authors: Tanu Kumari, Theertha Raj, Pasuluru Sanath Darahas, N. Neelima and V. Bhavana

Abstract: Identification of PCB board defects early in the manufacturing process is crucial, as PCB quality control plays an important role in the electronics manufacturing industry. Defective PCBs can lead to product failures, increased costs, and reliability issues. Proposed is a machine learning program for detecting and classifying defects in PCBs using a YOLOv5 object detection algorithm and an Inception v3 CNN-based approach. The dataset consists of annotated PCB images for the YOLOv5 algorithm, and the images are categorized into six defect types: missing holes, mouse bite, open circuit, short circuit, spurs, and spurious copper. The preprocessed defect images are analyzed using the YOLOv5 model for defect location, while the Inception v3 CNN model performs precise defect classification. The results and the output clearly show that the proposed approach achieves high accuracy in both detection and

classification tasks. Hence, the aim is to provide an efficient and automated solution for PCB inspection, outperforming conventional manual checks. (2025 3rd International Conference on Smart Systems for Applications in Electrical Sciences, https://doi.org/10.1109/icsses64899.2025.11009644, June 2025)

"EM-YOLO: High-Precision Electronic Component Detection via Multi-Scale Attention and Dynamic Feature Fusion"

Authors: Zeyi Xu, Jiahui Han, Hongying Qin, Kangsong Gao, Kai Xie and Jianbiao He

Abstract: To address the frequent missed detections and suboptimal accuracy in electronic component circuit board inspection, a target detection algorithm for electronic components, EM-YOLO, is designed with YOLOv11 as the core framework. The overall design employs a three-level optimization strategy: First, in the backbone network part, an efficient feature extraction module C3k2_EMA is designed. Incorporating the Efficient Multi-scale Attention (EMA) mechanism enhances the network's feature representation capability for tiny components. Second, in the neck network part, the BiSPD-FPN structure is proposed, which adds a high-resolution feature map at the P2 level. By combining the bidirectional feature pyramid network (BiFPN) with spatial pyramid depthwise convolution (SPDConv), it optimizes the multi-scale feature fusion capability and reduces detail loss during the downsampling process. Finally, in the detection head part, the Focal-DIoU loss function is introduced to optimize the bounding box regression process and improve the localization accuracy of densely arranged components. Experimental results show that, on the self-made dataset and the public dataset PCB Electronic Components Dataset, the detection accuracy (mAP@0.5) of the improved algorithm has increased by 0.5% and 3.9%, respectively, compared with the benchmark algorithm, while the false negative rate (FNR) has decreased by 1.3% and 4%, respectively, both outperforming mainstream algorithms. Therefore, the algorithm in this paper exhibits good detection accuracy, and the problem of missed detections occurring in the detection process has also been effectively alleviated. It possesses good generalization ability and provides an effective detection scheme for component detection. (*Scientific Reports*, vol. 15, no. 44531, Dec. 24, 2025; https://www.nature.com/articles/s41598-025-28116-0)

RF/Microwave Design

"Quad-Band Metamaterial Absorber with High Shielding Effectiveness Using Bold X-Shaped Ring Resonator"

Authors: Altaf Hussain, *et al.*

Abstract: A novel X-shaped modified split-ring resonator (MSRR) broadband microwave metamaterial absorber for covert applications in the C, X and Ku bands is presented. The absorber features a 0.035mm-thick annealed copper layer with X-shaped resonators on a 1.6mm-thick FR4 dielectric substrate, with a unit cell of 0.254λ × 0.254λ at 7.64GHz. CST Microwave Studio simulations show absorption peaks at 7.64GHz (98.4%), 8.41GHz (97%), 11.4GHz (99.2%), and 12.66GHz (99%). Parametric analyses are employed to optimize these frequencies using E-field, H-field and surface current distributions. The design achieves high absorption for transverse electric (TE) and transverse magnetic (TM) polarization across incidence angles up to 30°, ideal for electromagnetic interference (EMI) shielding and stealth in military contexts. (*Journal of Electronic Materials,* November 2025; https://link.springer.com/article/10.1007/s11664-025-12512-3)