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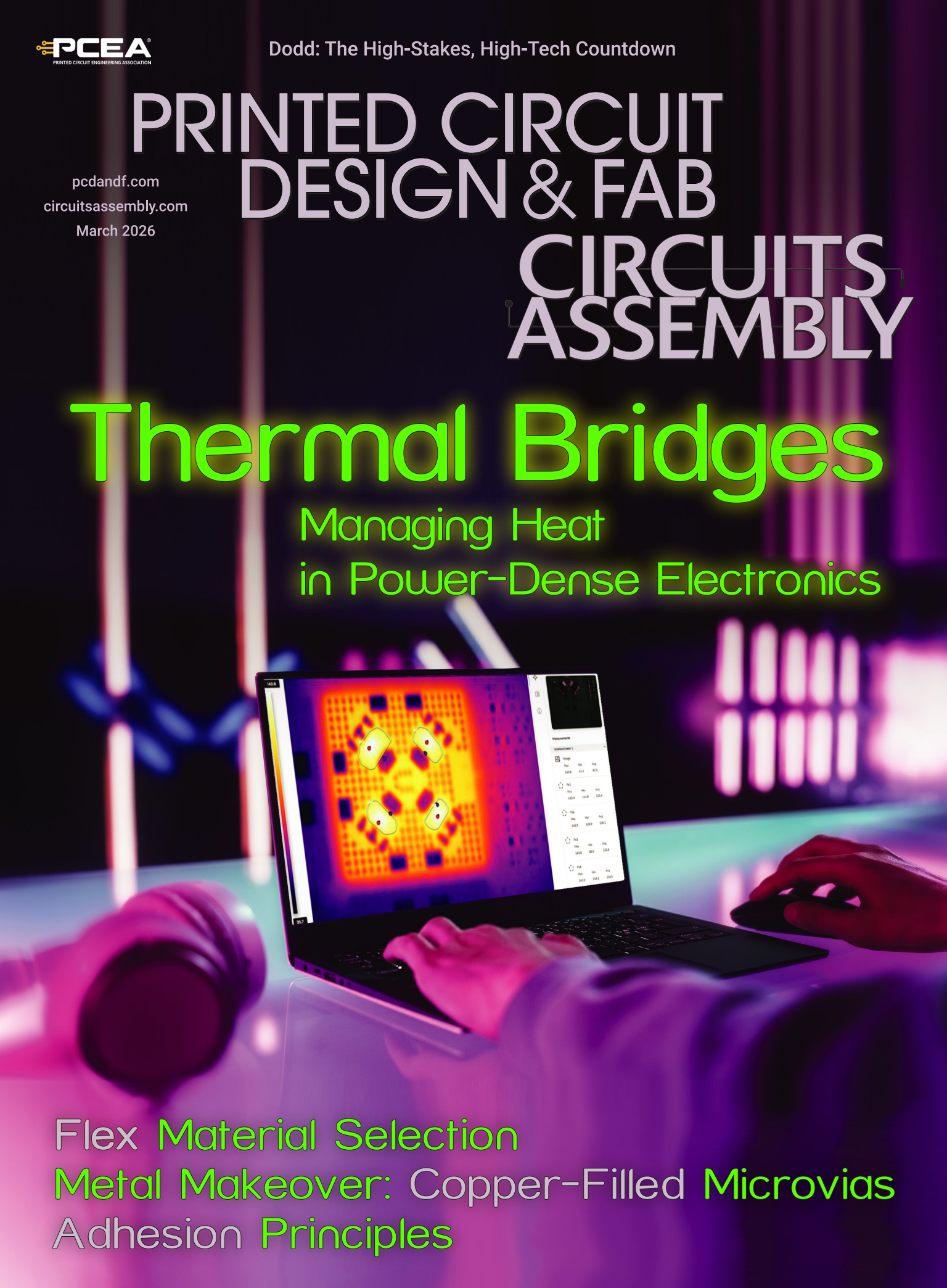
Thermal Bridges

Managing Heat in Power-Dense Electronics



Flex Material Selection

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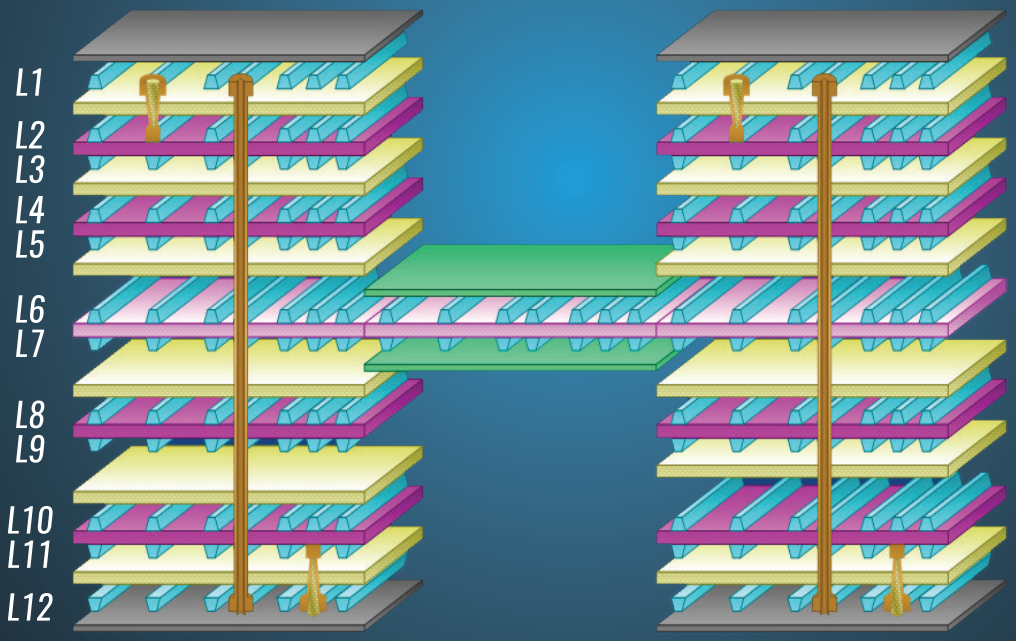

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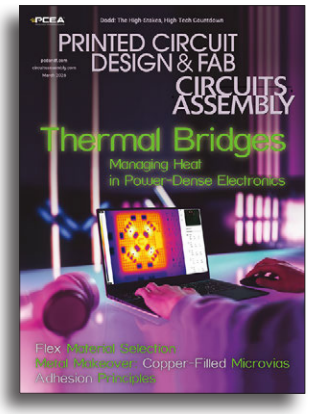
FIRST PERSON

MONEY MATTERS

TECH TALK

DEPARTMENTS

FEATURES



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Europe's Electronics Dilemma: A Will Without a Way

THE EIPC WINTER Conference in February was revealing for several reasons, not the least of which was that the view among the 125 primarily European electronics engineers and executives in attendance was their industry and governments had failed them by not acting more swiftly and vigorously to staunch the offshoring tide.

Europe, in some ways, came out of the dot-com mess in better shape than North America. The number of PCB factories still standing on the continent is estimated at 186, with an aggregate revenue of approximately $1.89 billion last year, according to Data4PCB. That was good for a 2.2% share of the world market. (Data4PCB used data from TPCA and CPCA in its estimates; we will wait for Dr. Hayao Nakahara of N.T. Information for the definitive report later this year.)

That's not great: In 2000, when most Western markets were peaking, it was $5.4 billion and about a 16% share split among more than 550 fabricators. 2020 excepted, it's been operating in a fairly stable band of $1.7 billion to $1.9 billion for more than a decade.

Sound familiar?

In comparison, North America's fall was more precipitous, even if the landing was higher than that of Europe's. Revenues peaked at above $10 billion in 2000, when its share of the world market was neck-and-neck with Japan's at about 30%. The number of shops (meaning individual facilities) – merchant and captive – has plunged to about 230 from well over 1,000 25 years ago. Revenues are now in the $3.75 billion range, and overall share hovers around 4%.

Flummoxed, the US spent the better part of two decades in the wilderness, with no real focused effort to counter the drain of demand and technology. The coordination of the Printed Circuit Board Association of America, coupled with the recognition by a small handful of legislators, has helped bring attention to those who can start the process of revitalizing the domestic industrial base. The heaviest lift, of course, was made by the Semiconductor Industry Association, whose determined lobbying boosted the semiconductor industry's profile in the corridors of Washington. The passage of the Chips Act created an updraft that PCBs are trying to capitalize on.

But Europe remains a mystery. It's central government in Brussels has certainly shown itself capable of drafting and instituting industrywide mandates when it suits them; to wit, the Vienna Convention, which established a framework for negotiating international regulations on ozone-depleting substances and led to the subsequent Montreal Protocol; REACH, which controlled chemical use; WEEE, the overarching recycling and reuse legislation; and of course, RoHS, which forever changed the face of soldering.

The efforts in the US have yet to reap tangible benefits, but attention is rising, and even if dedicated legislation doesn't come about, electronics as an industry is now recognized as vital at the highest levels of government. Absent a similar industry push, it does not appear the European Commission will find on its own the spark that drives a legislative mandate to boost the Continent.

That's why I wholeheartedly agree with the entirety of this letter from the EIPC to the European Commission in support of the printed circuit board industry.

I especially like this statement: "Electronics underpin Europe's economic resilience and strategic autonomy."

The electronics industry has for decades shown spectacular tactical prowess while lacking the strategic plan necessary to fulfill its aims. But the goals must align with the objectives. If national or regional self-sufficiency is the goal, then objectives must be put in place to achieve it. And while we in the trenches understand that, we cannot assume those charged with writing legislation do.

mike@pcea.net
@mikebuetow

P.S. If you believe manufacturing is returning to domestic shores and want guidance on how to outfit the factory, judiciously implement AI, develop workforce training programs and a host of other business issues, check out the management sessions at PCB East. Network with peers while getting clear-eyed wisdom from those who have gone before you.

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

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Elite Material Acquires Factory in Taiwan

TAIPEI, TAIWAN – Elite Material is expanding operations with a newly acquired factory in Taoyuan's Guanyin District, a move aimed at boosting production of copper-coated boards used in AI servers, high-speed switches and data centers.

The company invested about $88 million to acquire the site, which adds roughly 500,000 boards of annual capacity to its Taiwan operations.

The Taoyuan facility complements recent capacity additions in China and Malaysia, part of a broader expansion strategy tied to rising demand for high-speed data transmission. Once all planned facilities are operational, Elite Material expects total production capacity to reach 5.85 million copper-coated boards, with growth driven primarily by server, networking and satellite-related applications.

Aimtron Acquires ICS to Expand US Footprint

DECATUR, IL – Aimtron Electronics has acquired ICS Co., strengthening its presence in North America and expanding its capabilities in mission-critical electronics.

Aimtron acquires US-based ICS to expand ESDM presence globally.

Based on calendar-year 2025 estimates, the acquisition is expected to contribute approximately $17 million in annual revenue, with consolidation planned from the fourth quarter. Aimtron expects the acquired operations to scale to roughly $25 million in revenue within three years.

The acquisition also supports efforts to increase utilization at Aimtron's US facility to nearly 90% from approximately 54% over the next three years.

Founder Mukesh Jeram Vasani said the deal accelerates Aimtron's move toward a full stack global ESDM platform, while ICS founder Dennis Espinoza said the integration will allow the company to deliver broader end-to-end solutions to existing customers.

The acquisition follows Aimtron's recent expansion activities in India and a ₹1 billion fundraising.

Aegis Completes Simio Acquisition

HORSHAM, PA – Aegis has completed its acquisition of Simio, expanding its platform to support end-to-end manufacturing execution, planning and scenario modeling.

The transaction integrates AI-driven digital twin simulation and advanced planning and scheduling into an existing manufacturing execution and operations software portfolio.

The combined organization now supports manufacturing operations across more than 2,200 factories worldwide and plans to continue expanding through platform development and additional acquisitions.

Patton Acquires Practical Technologies

BALTIMORE – Patton LLC has acquired the assets of Practical Technologies, adding a 20,000-sq. ft. Baltimore-area manufacturing facility and expanding its electronics manufacturing and contract services footprint across defense, aerospace and industrial markets.

The acquisition strengthens Patton's end-to-end capabilities, combining engineering, PCB assembly, wire and cable harnessing, electromechanical assembly and potting and encapsulation services across prototype, low-rate and volume production. PTI's facility will complement Patton's existing Gaithersburg, MD, operations.

Patton said the transaction expands capacity without significant incremental capital investment and enhances responsiveness for East Coast customers.

Tide Rock Expands EMS Platform with Analog Technologies Acquisition

SAN DIEGO – Tide Rock has acquired Analog Technologies, expanding its electronics manufacturing services (EMS) platform with additional aerospace and defense-certified capabilities and advanced interconnect technologies.

The acquisition adds PCBA design and engineering, conformal coating, box build and testing capabilities, along with specialized interconnect technologies such as wire bonding, flip chip and silver sintering. The transaction also establishes a second aerospace and defense-certified manufacturing site within Tide Rock's EMS platform.

Tide Rock said the combination enhances operational scale and technical depth across its EMS platform, positioning the group to support complex, performance-critical programs.

Pro-Active Engineering and Analog Technologies are expected to collaborate across engineering and production resources to expand capacity and serve aerospace and defense customers.

Creative 3D Technologies Raises $5M to Scale Modular 'Factory-in-a-Box' Platform

AUSTIN, TX – Creative 3D Technologies (C3DT) has raised $5 million in seed funding to expand its modular "Factory-in-a-Box" manufacturing platform.

The Austin-based advanced manufacturing company secured participation from NJP, MetaLucks, Sher, Greenwood and Tech Bricks. The funding will support expanded production of its EVO system, further development of a semiconductor-focused roadmap, and broader deployments across defense, energy and advanced manufacturing sectors.

C3DT's EVO platform is a rugged, large-format additive manufacturing system designed to process polymer, fiber-based and metal-filled materials at industrial scales. Built around what the company calls "Single-Cell Manufacturing," the system consolidates what would traditionally require an entire factory line into one modular unit.

Future configurations are expected to integrate more than 20 production functions, including additive manufacturing, CNC machining, electronics assembly and pick-and-place through interchangeable toolheads. The goal is to enable localized, industrial-grade production without the infrastructure demands of centralized facilities.

The company reports early pilot programs with customers including the US Army and Disney, reflecting demand for distributed production in both mission-critical and commercial applications.

C3DT is also conducting early-stage R&D on a semiconductor-focused "Fab-in-a-Box" platform targeting specialty and prototype microelectronics.

SEL Breaks Ground on $50M Moscow Manufacturing Expansion

MOSCOW, ID – Schweitzer Engineering Laboratories has begun site preparation for a new $50 million, 250,000-sq. ft. electronics manufacturing facility at its campus here, expanding capacity to meet growing global demand for infrastructure protection systems.

Site preparation underway for Schweitzer Engineering Laboratories' new $50 million manufacturing facility in Moscow, ID.

The new building will be constructed south of the company's printed circuit board factory and is expected to significantly increase production of electronic devices used to protect, monitor, and control electric power systems and other critical infrastructure. Completion targeted for late 2027.

SEL president Dave Whitehead said the investment reinforces the company's long-term commitment to Idaho and the surrounding region. Once fully operational, the facility is expected to employ approximately 1,000 workers.

PCD&F

AdvancedPCB has installed a **MASS** VCP-5000 vacuum via filling system at its Santa Clara, CA, facility.

AdvancedPCB installed a Galaxy 25µ CIMS AOI system at its Orange County facility.

Avedon Capital Partners has taken a stake in **Eurocircuits**.

ChipHub has launched an AI-enabled electronic components procurement tool said to negotiate prices, track spending, and monitor savings in real time.

Eltek received $12.2 million in purchase orders from a US defense customer.

Rabbit Product Design announced expanded IoT electronics design services.

RTX awarded **TTM Technologies** a three-year contract worth up to $200M.

Shenzhen Han's CNC Technology, a PCB equipment maker, seeks to raise up to HK$4.83 billion ($619 million) in its Hong Kong listing.

Siemens has acquired Grenoble-based **Canopus AI** to strengthen its AI-driven semiconductor metrology and inspection capabilities.

Taiyo will suspend production of some E-glass cloth series products to make way for meeting higher demand for low Dk glass cloth.

University of Washington researchers developed OpenTouch Glove, a sensor-embedded wearable that maps pressure across the hand in real time to capture how users grip and interact with objects.

CA

Amber Enterprises completed an acquisition of Pune-based **Shogini Technoarts**.

ASMPT expanded its sales representative agreement with **SMarTsol** to six US states.

Asteelflash plans to expand its operations in Tunisia, aiming to double local revenue and exports through a facility extension.

CalcuQuote rebranded under **Elisa Industriq,** aligning its market identity with the group's industrial

software portfolio.

Connexion Technologies has entered a strategic partnership with **OMR Italia**.

Crown Defence launched a PCB assembly facility in Goa, India.

Demcon has acquired Dutch electronics specialist **Leap Development**, rebranding it as **Demcon Electronics**.

Element Solutions completed its acquisition of the **Micromax** conductive pastes and inks business.

Fornnax Technology partnered with **Dieter Jerschl** to expand sales and support for its recycling solutions across Central Europe.

Incap completed its acquisition of Germany- and Romania-based EMS and ODM provider **Lacon Group**.

K&F Electronics has added a **SASinno** Ultra-i1 selective soldering system.

Keiron Printing Technologies appointed as sales representatives **BarTron** for the Midwest and Ohio Valley and **Yankee Soldering Technology** in New England.

Kitron secured an additional $5.9 million order for autonomous defense electronics, raising the total agreement value to about $14.3 million.

Koh Young Technology appointed **Smartsol** sales representative for Mexico.

Microboard has invested $1.3 million in **Mycronic** MYTower 7+ and 6X inventory towers.

Microsoft has formalized a major outsourcing agreement with **Foxconn** to build Xbox Series consoles in Vietnam.

Note secured a three-year, SEK 135 million ($13 million) defense electronics order from a long-term Nordic customer for advanced PCB assemblies.

Pillarhouse USA appointed **Lean Stream** sales representative for Northern California and Northern Nevada.

Qualcomm Technologies selected **Tata Electronics** to manufacture automotive modules in India.

Scanfil plans to invest in expanding its plant in Suzhou, China, adding 15,700 sq. m of space.

Silicon Mountain Contract Services has rebranded as **SMCS**.

TYRI opened an in-house circuit board manufacturing facility in Kungsbacka, Sweden.

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Daniel G. Korte


Ryan D. McCarthy


Tzyy-jang Tseng

Deswell Industries named **Karen Chan Chi Yin** chief financial officer.

TTM Technologies has appointed **Daniel G. Korte** and **Ryan D. McCarthy** as independent directors.

Unimicron Technology chairman **Tzyy-jang Tseng** has retired.

CA


Mark Sika


Josh Foulger


Mayur Mundra

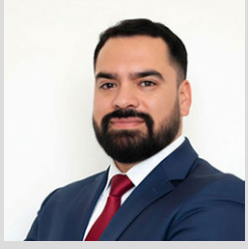

Bruce Moloznik


Benjamin Hein


Adan Galindo


Jorge Lara


Marcos Martínez


Juan Alfaro


Erwin Stoeckinger

Absolute EMS has appointed **Mark Sika** as president.

Dixon Technologies' Padget Electronics subsidiary named **Josh Foulger** president IT hardware and new projects.

Libra Industries appointed **Mayur Mundra** chief financial officer.

MacDermid Alpha Electronics promoted **Bruce Moloznik** to business integration leader, senior vice president.

Merck KGaA appointed **Benjamin Hein** CEO of its electronics business.

Safran Electronics and Defence Services India has appointed **Shiju Jacob** manufacturing unit head – electronics in Bengaluru.

SIA president and CEO **John Neuffer** will retire in mid-2026 after 11 years leading the association.

SMarTsol named **Adan Galindo** director of sales, **Jorge Lara** sales manager and announced **Marcos Martínez** has joined its Dallas operation.

Terran Orbital named **Robert Duval** senior MES engineer.

ViTrox appointed **Juan Alfaro** Mexico sales and support manager.

Zollner promoted **Erwin Stoeckinger** to executive vice president, electronics and business division, Americas.

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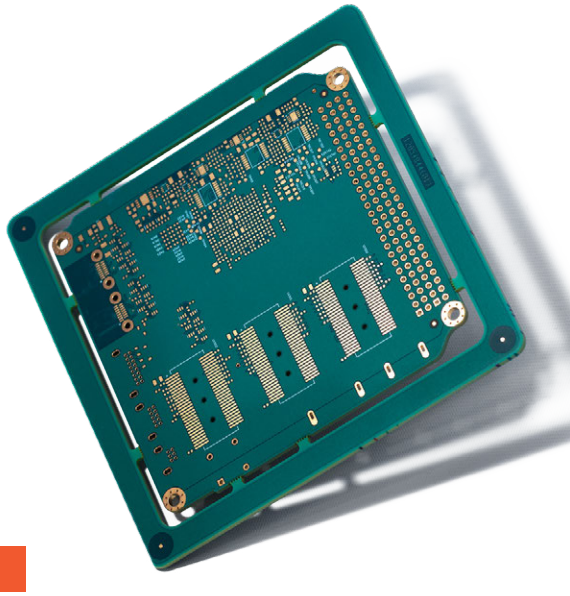

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Tech, Management Talks Highlight Assembly Program at PCB East

PEACHTREE CITY, GA – The PCEA Assembly Conference will take place Apr. 30-May 1, concurrent with PCB East, PCEA announced. The new event will feature three all-day tracks across two days, with two tracks focused on SMT processes and aimed at engineers and operators, and the third track designed for managers and executives interested in supply-chain and business issues.

The conference is split into basics and advanced courses, to help engineers and operators new to the industry and more experienced personnel looking to learn about new technologies.

Among the technical presentations are talks on materials, printing, placement, reflow, cleaning and inspection. The advanced courses will cover stencil design, printer setup, type 5 and beyond solder pastes, placement advancements for AI and data center applications, reflow optimization and formic acid, and cleanliness measurement and conformal coatings.

Among the presenters are experts from Honeywell, Aurora Boardworks, Indium, Parmi, Heller, MacDermid Alpha, Metal Etch, ItDepends and Shea Engineering.

Two half-day, hands-on sessions on hand soldering round out the technical conference.

In addition, an all-day management track includes talks on the future of defense electronics manufacturing, cybersecurity implementation, trusted suppliers, import/export rules, Cooperative Project Management, equipment evaluation, board supplier audits, and AI in assembly.

A panel on workforce training and development rounds out the program.

Strategic Leadership Session Tackles AI, Workforce Issues

PEACHTREE CITY, GA – Strategic Leadership in the Age of AI, New Technology Adoption and Talent Scarcity, a new, full-day program aimed at C-level executives and managers, takes place Apr. 28, concurrent with PCB East at the

DCU Convention Center in Worcester, MA.

Chaired by Gene Weiner and Peter Bigelow, the forum will bring together leaders from across the PCB industry to discuss AI, mentoring and training the next generation of workers, rapid technological and organizational changes, and collaboration between industry and educational institutions.

Sessions include:

- "Build AI vs. Buy AI: Why AI Isn't a Technology Problem … It's a Leadership One – Sean Patterson, CrossGen AI
- AI Needs Hardware: Rebuilding Advanced PCB Manufacturing – Vytautas Ilgunas, TLT Electronics
- PCBAA Update on Washington Legislative Efforts – John Vaughan, Summit Interconnect
- Unintended Consequences! How the AI Infrastructure Build Out Will Reshape the PCB Materials Supply Chain – Alun Morgan, Ventec
- AI's Role in the Future of Electronics Manufacturing Collaboration – Timon Rubin, Luminovo
- Addressing the Skilled/Semi-Skilled Labor Shortage
- Outlook In View of AI Surge in PCB Demand and Severe Material Shortages/ Allocations

Sean Patterson will tackle AI implementation in electronics companies during the PCEA Management Session at PCB East.

Registration for both the technical conference and the exhibition takes place at pcbeast.com. Those who sign up by Mar. 27 can take advantage of the early bird special discounts for the conference.

PCEA Opens Registration for PCB Detroit Conference

PEACHTREE CITY, GA – Registration for PCB Detroit is now open, the Printed Circuit Engineering Association (PCEA) announced. The event, now in its second year, takes place Jun. 15-16 on the campus of Wayne State University in Detroit, MI.

The technical program will feature two full days of in-depth electronics engineering training featuring some of the industry's most esteemed experts. Rick Hartley, Stephen Chavez, Dan Beeker, Tomas Chester, Ethan Pierce and Tim Wang Lee are among the headliners of this year's conference.

PCB DETROIT
Conference & Exhibition

The scope of classes ranges from placement and routing, thermal management, ESD design techniques, AI implementation, flex and rigid-flex design, nondestructive measurement techniques and thin copper, among others. In all, PCB Detroit will offer more than 20 hours of technical sessions for every level (novice to expert).

PCB Detroit will also feature a tabletop exhibition on Jun. 16, followed by a free reception.

"After last year's conference, we heard from registrants who were grateful to an event to call their own, as well as exhibitors that landed new customers," noted Mike Buetow, president, PCEA. "Given the emphasis Michigan is placing on semiconductor and electronics design and manufacturing, we are pleased to return to Detroit to meet the regional demand."

Registration for the two-day technical conference and the tabletop exhibition takes place at pcea.net/pcb-detroit. Conference registration is required for both the conference and tabletop exhibition.

Wayne State University is Michigan's third-largest university, and a licensee of the PCEA Training Certified Printed Circuit Designer curriculum.

For more information about PCB Detroit, visit pcea.net/pcb-detroit or contact pcbdetroit@pcea.net.

PCEA, SMTA Capitol Chapter Sponsoring Design for Sourcing Webinar

PEACHTREE CITY, GA – PCEA in conjunction with the SMTA Capitol Chapter will present a two-part two-hour webinar on sourcing strategies for PCB designers and design engineers starting in April. The webinar, "Design for Sourcing," will be presented by supply chain expert Ed Dodd, vice president of government and defense for Cofactr.

Ed Dodd

This webinar takes place in two one-hour sessions starting at 1 p.m. EDT on April 21 and May 5.

In these sessions, Dodd will empower designers and design engineers with the knowledge and tools necessary to proactively design out supply chain risks during component selection. Attendees will learn about the current landscape of supply chain vulnerabilities, the principles of design for sourcing, and practical strategies to ensure continuity and reliability in their electronic designs.
Attendees will gain the information to make informed decisions that safeguard their projects against disruptions and contribute to a more robust supply chain ecosystem.

For more information or to register, click here.

PCEA Names Leah Spinks Events Planner

PEACHTREE CITY, GA – PCEA in February named Leah Spinks events planner, responsible for pre- and on-site management of the association's conferences and trade shows.

Leah Spinks

Spinks has more than 10 years' experience in events planning, most recently as senior project manager at Enterprise Events Group. She was also a meeting and event manager at Maritz Global Events and events manager at the America's Center in St. Louis. Throughout her career, she has been involved in strategic planning, contract negotiation, customer service, logistics, and other key facets of show management.

"Leah is a strategic and results-driven project and event management professional whose infectious personality and intellect will quickly make its mark with our customers and the industry," said Mike Buetow, president, PCEA.

Spring PCB Design Training Classes Scheduled

PEACHTREE CITY, GA – Registration is open for the PCEA Training Certified Professional Circuit Designer (CPCD) training and certification classes this spring.

Class dates are May 15, 22, 29, Jun. 5 and 12. Registration closes Apr. 16.

The 40-hour instructor-led course is designed for printed circuit engineers, layout professionals and other individuals currently serving in the design engineering industry or seeking to get into it.

The classes cover the gamut of printed circuit design engineering, from layout, place and route to specifications and materials to manufacturing methods. Schematic capture, signal integrity and EMI/EMC are also part of the comprehensive program.

Each class includes a copy of *Printed Circuit Engineering Professional,* a 400-page handbook on circuit board design, and the optional certification exam recognized by PCEA.

There are no prerequisites to enroll. Classes are held online and led by experienced instructors.

To enroll, visit pceatraining.net/registration.

PCEA **CURRENT EVENTS**

ASSOCIATION NEWS

Certification. The following recently passed the PCEA Certified Printed Circuit Designer exam:

- Karim Arabi
- Randy Baggao
- Areeba Mukhtar
- Carl Olthoff

New Corporate Members

- Panasonic Electronic Materials
- Parter AI

Networking. The PCEA Discord server brings together engineers and designers from around the world on a private channel to discuss technical questions and career opportunities. To join, contact PCEA. Recent conversations covered high voltage boards, reflowing through-hole components, and differential signals.

CHAPTER NEWS

Orange County. We are working on our next meeting, tentatively scheduled for the beginning of April.

Portland, OR. Our February meeting featured John Coonrod of Rogers Corp., who gave a foundational overview about PCB substrates for RF and high-speed digital applications. Our March meeting takes place Mar. 26 at 12 PST. John Johnson from ASC will talk about UHDI.

Richmond, VA. Our Feb. 12 Community Hardware Night meetup was a great success. Members joined at Mobius Materials' HQ for open conversations spanning from production, supply chain and even job promotions. The family-friendly event invited kids to play Switch in the media room and partake in conversations like "how do they make a Switch?" and "what's inside a Switch game console and how does it work?" The highlight of the evening was Oday Abushaban's tech fashion prototype – the Tech Bowtie.

The chapter is considering hosting an in-person speaker for the next meeting, and is also interested in business-side topics. That could include starting or managing an electronics business, supply chain, fundraising, finding customers or exploring the regional, national or international ecosystems.

Silicon Valley. We are planning a chapter meeting for late March or April.

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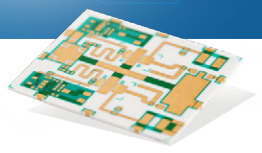

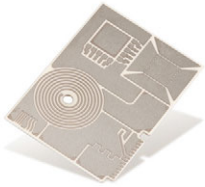

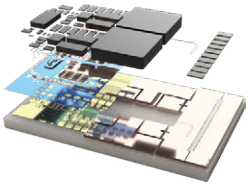

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MARKET **WATCH**

Components Index Reflects Strongest Sales Sentiment in 4+ Years

ATLANTA – ECIA's January survey of component suppliers delivered its strongest sales sentiment reading in more than 56 months, signaling renewed confidence across the electronics component supply chain.

The overall average index score reached 138 in January and is projected to rise to 143.4 in February. A score of 100 marks the threshold between negative and positive sentiment. January's result represents the eighth consecutive month above 110 and the strongest performance since the March through May 2021 period.

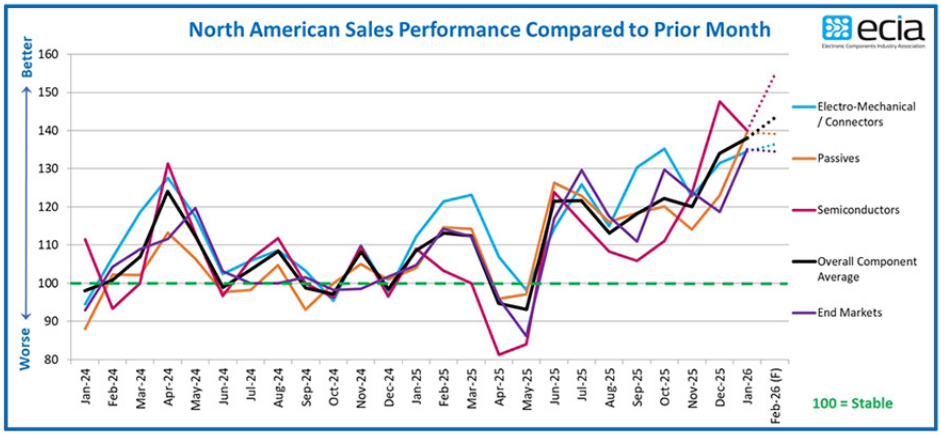


Figure 1. Sales sentiment among component providers is skyrocketing.

Despite a drop in the index score of 7.6 points between December and January, the semiconductor category led among the three major segments with a score of 140. With a surge of 16.7 points over the prior month, passive components nearly matched the semiconductor score with an average of 139.6. Electromechanical/connectors improved modestly to 134.5.

According to survey participants, the electromechanical and passive categories are expected to sustain their strong sales sentiment heading into February, with only minor changes in sentiment. Semiconductors are projected to leap to 154.5.

Memory ICs are at a record-breaking 180 for January and February.

"It is very encouraging to see the authorized supply chain participants' self-image so positive as we begin a new year," said ECIA chief analyst Dale Ford. He cautioned, however, that supply-demand imbalances in advanced memory ICs pose a significant risk.

“The severe mismatch between supply and demand for advanced memory ICs presents one of the greatest concerns for the overall health of the electronics components market. Limited supplies of these components could stall sales in other segments. This has emerged as one of the most critical areas of supply chain management heading into 2026.”

Edging Up

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	OCT.	NOV.[r]	DEC.[p]	YTD
Computers and electronics products	0.2	1.0	0.6	4.8
Computers	3.0	4.2	3.4	16.0
Storage devices	2.0	1.4	0.4	9.0
Other peripheral equipment	6.2	15.9	-7.2	14.4
Nondefense communications equipment	-1.3	6.7	-1.3	8.9
Defense communications equipment	2.4	3.3	0.5	0.8
A/V equipment	-2.7	-0.5	0.2	-5.1
Components[1]	0.6	0.9	1.1	5.1
Nondefense search and navigation equipment	5.0	-3.6	-2.8	3.7
Defense search and navigation equipment	-0.2	-0.3	-0.9	3.1
Electromedical, measurement and control	-0.7	-1.3	-0.7	3.2

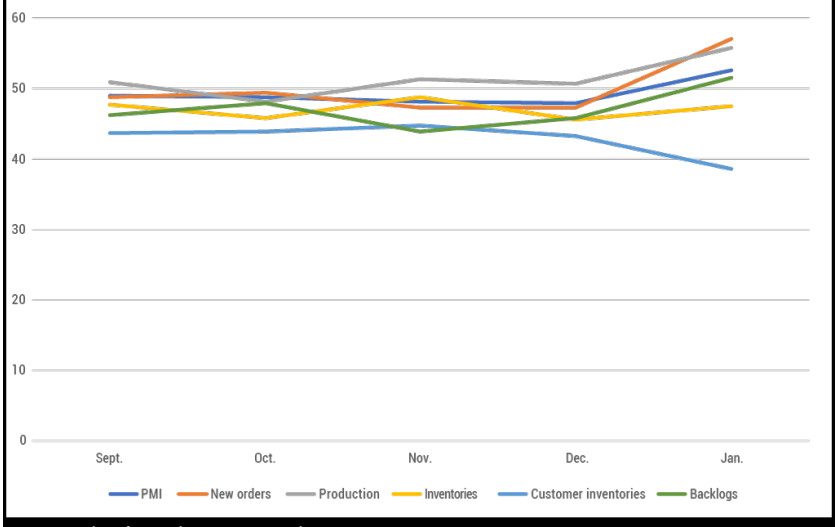
[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, Feb. 23, 2026

Key Components

	SEPT.	OCT.	NOV.	DEC.	JAN.
EMS book-to-bill[1,3]	1.31	1.26	1.17	1.24	TBA
Semiconductors[2,3]	15.3%	27,2%	15.3%	39.4%	TBA
PCB book-to-bill[1,3]	0.92	1.00	1.12	1.18	TBA
Component sales sentiment[4]	121.6%	122.2%	120.1%	120.1%	138.0%

Sources: [1]IPC (N. America), [2]SIA, [3]3-month moving average, [4]ECIA

US Manufacturing Indices



Source: Institute for Supply Management, Feb. 2, 2026

Hot Takes

Global **semiconductor sales rose 25.6%** to $791 billion in 2025, with industry forecasts projecting the market will approach $1 trillion this year. (SIA)

Global **smartphone production** in 2026 is forecast to decline 10% to approximately 1.14 billion units. With memory prices showing no clear signs of easing, the growing gap between higher retail prices and consumer price tolerance is expected to further dampen end demand. (TrendForce)

The global **wearable technology** market is projected to reach $232 billion by 2030, supported by AI-driven features, health monitoring demand and expanding device categories. (GlobalData)

Taiwan's flex board exports in January rose 59% year-over-year. (TPCA)

Global **silicon wafer shipments** rose 5.8% in 2025, while revenue slipped 1.2% as AI-driven demand offset weak pricing in mature markets. (SEMI)

Taiwan's rigid PCB exports in January jumped 39% from a year ago. (TPCA)

North American PCB shipments rose 11% year-over-year in December while bookings also increased 11%. (GEA)

North American EMS bookings increased 28.7% sequentially in December and 5.1% year-over-year. (GEA)

The world's two largest memory makers, Samsung and SK Hynix, warned the memory chip crunch will continue until 2027, driven by AI demand. (Nikkei Asia)

Taipei's top tariff trade negotiator told Washington that its proposal to **move 40% of the island's semiconductor supply chain** to the US was "impossible." (CNBC)

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The Next Materials Reckoning in Electronics Manufacturing

Cost pressure once again may become the industry's biggest driver of change.

NECESSITY IS THE mother of invention, they say. Well, I am not sure necessity is the mother of *all* invention, but it can definitely be tied to a whole bunch, and probably has more than a few still to birth.

Having been in the industry for a long, long time, I can attest that many exciting new products, and the technologies required to develop and enable their mass utilization, have driven much of the innovation our industry is known for. Miniaturization of computers, the growth and speed of communication platforms such as the internet, the exponential expansion of features (functions, apps, etc.) that have enabled virtually everyone to rely on their cellphone, as well as development of a variety of robotics and drones, have all been created because of, and resulted in collateral uses for, exciting technologies.

In other circumstances, however, phenomenal new technology was not the result of a brilliant dream but rather a thorny problem that forced herculean efforts to replace existing technologies, processes and raw materials. Early in this millennium the European Union RoHS directive posed just such a problem. This legislation required all industry to scramble to find a replacement for lead: lead in solder, lead in CRT tubes used in TVs and computer monitors, and a host of other mechanical surface finish applications.

No one was eager to invest the resources in replacing lead, which was virtually bulletproof in so many applications. Companies would have far preferred investing in next-generation products, but given no choice, necessity became the mother of invention, and over time innovation took hold, and reasonable alternatives were found to replace lead in almost all products and applications.

Some of the surface finish alternatives that became popular were more expensive, in particular ones containing gold and silver. Today, ENIG, ENEPIG and SnAg are some of the most common surface finishes utilized in electronics. In addition, I can attest that, having spent nearly a quarter century running a printed circuit board fabricator focused on the RF/microwave and military markets, wire bondable "soft" gold and electroplated "hard" gold are the plating surfaces of choice for many of those segments' applications.

Necessity may once again be mothering invention, however. Gold and silver are precious metals, and as such, pricing is subject to not only industrial and consumer demand but also market speculation. Investors and speculators can drive price spikes that make precious metals no longer financially tenable for business use.

Indeed, back in the early 2000s, gold sold for about $400 per oz. A decade later, the average price had doubled. And in the past few years, prices of all metals (copper, gold, silver, platinum, etc.) have skyrocketed and are forecast to continue to rise. As an example, gold prices increased 71% in the past 12 months and 232% over the past five years. Such increases are not sustainable in a manufacturing environment; a reliable, cost-effective alternative may be needed. Same goes for metals used in soldering, wire-bonding, and critical electronic processes.

As was learned in the early 2000s with the RoHS no-lead mandate, replacing these precious metals is neither a simple, quick nor inexpensive endeavor. Some alternative surface finishes, such as OSPs, should be revisited to see if newer raw materials will increase their shelf life, durability and cost-effectiveness, which historically made them less desirable than precious metals. It may also be time to think outside the box and consider materials used in related emerging applications. Such areas to look at may include plating utilized in microelectronics, or coatings utilized in printed electronics. Different types of organics and nano-chemistries may finally be sufficiently cost-effective and robust for use in consumer and high-reliability applications.

One strategy I would not recommend is waiting for a correction that brings the price of gold, silver and other precious metals back to where they were. The trajectory of pricing for precious metals utilized in manufacturing has always increased at a greater pace than that of other materials used in this sector.

So let the current necessity of finding a cost-effective and reliable alternative to gold and silver lead the industry to invent a truly incredible and universally usable new process technology.

PETER BIGELOW has more than 30 years' experience as a PCB executive, most recently as president of FTG Circuits Haverhill; peterbigelow@msn.com. He is vice chair of the PCEA PCB Management Symposium, "Strategic Leadership in the Age of AI, New Technology Adoption, and Talent Scarcity," taking place April 28 at PCB East.

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BOARD **BUYING**

The Ghost Queue: Why Your "Made in USA" Order May Be Gathering Dust

The current US board market is spookier than it seems.

THE EMAIL CONFIRMATION hits your inbox: *Order Received. Status: In Process.*

For a procurement manager or lead engineer, that notification usually triggers a dopamine hit. It's the sound of progress. You've successfully navigated the internal approvals, you've selected a domestic vendor to avoid the headache of customs and the sting of new tariffs, and you've kept your supply chain close to home. You have done everything right.

But three weeks later, you haven't received a shipping notification. You haven't even received a query about a tolerance issue. You call the shop floor, and after being transferred twice, you find the truth: The material for your boards hasn't been ordered. And several EQs (engineering questions) are still pending. Your project is stuck in what I call the "Ghost Queue."

Figure 1. The Ghost Queue is the silent killer of product development cycles.

Back in March 2025, I wrote about the dangerous disconnect between US manufacturing *ambition* and US manufacturing *reality*. I warned that while policy can shift demand overnight, it takes years to build the infrastructure to meet it. Today, we are living through the consequences of that lag. The Ghost Queue is the silent killer of product development cycles, and it is catching the industry's best engineers off guard.

The anatomy of the ghost queue. To understand the Ghost Queue, look beyond the Open sign on the fabricator's

door.

A Ghost Queue forms when a shop's administrative (and production) capacity to accept orders outpaces its physical capacity to execute them. In the wake of aggressive tariff hikes on the bare PCB and the "get out of China" mantra, domestic shops have been inundated with work. This sounds like a success story – a manufacturing renaissance.

A shop cannot simply scale up like a software company, however. Adding a second shift requires skilled labor that doesn't exist in the current talent pool. Buying a new drill or electrical test machine requires capital and, ironically, a lead time of its own.

So, shops do what any business does when demand spikes: they say "yes" and hope to catch up later. They book the revenue, queue the job and pray for a miracle. Your job enters a digital purgatory. It is technically "in production" according to the ERP system, but physically, it is merely a line item on a backlog that stretches into next quarter.

The tariff paradox. The root cause here is a fundamental misunderstanding of what tariffs achieve in the short term. The prevailing logic is that taxing foreign goods incentivizes domestic production. That is true, but only if the domestic production capacity *exists*.

Tariffs neither build factories nor train workers. Tariffs simply redirect a firehose of demand toward a domestic garden hose of capacity.

When you insist on sourcing domestically purely to avoid the current (depending on technology) 20% or 45% duty, you are often trading a financial cost for a time cost. What you save on tariffs, you give back on time-to-market.

In the hardware startup world or the fast-paced consumer electronics sector, time is the only currency that matters. A four-week delay in prototyping or even a production order doesn't just push back the launch; it bleeds burn rate, delays revenue and gives competitors a window to strike.

The offshore agility. Contrast the domestic gridlock with the current state of offshore manufacturing. While US shops are hyper-saturated, many high-quality shops in Vietnam, Thailand and (dare I say) China are operating with significant slack.

Because the tariff narrative has scared so many Western buyers into reshorting or nearshoring (often indiscriminately), these offshore hubs have retained their agility. They are hungry for work.

I recently spoke with an OEM buyer who was quoted a 12-week lead time for a not-so-simple HDI PCB from a domestic shop. The shop was great; it was just fully booked. He swallowed his pride, sent the files to a shop in China, paid the duty and had the parts shipped in four weeks.

The parts were perfect. The duty cost him an extra $2,400. The eight weeks he saved? That was worth tens of thousands in engineering and sales momentum.

Don't let the project die in the queue. This is not an argument against American manufacturing. I am a

proponent of building local capabilities and shortening supply chains where it makes strategic sense. But Buy American is a strategic tool, not a religion.

Be honest about the current state of the domestic ecosystem. It is overheated. It is understaffed. And for the next year or so, it is going to be plagued by the Ghost Queue.

As you plan your next build, look closely at your vendors. Ask the hard questions before you issue the PO. Don't ask "What is your standard lead time?" Ask "Depending on technology, what are your current lead times today?" And be bold enough to ask, "If I place this order today, when will the material actually be sheared?"

If they can't give you a straight answer, you're looking at a ghost.

There is no honor in letting a project fail because you were waiting for a domestic slot that never opened. Agility is the ultimate competitive advantage. Sometimes that means paying the tariff, looking overseas and getting the parts in your hands while your competitors are still waiting for their confirmation email.

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as the founder of a leading distributor. He is cofounder of DirectPCB (directpcb.com); greg@directpcb.com.

Phase Gates, Not Face-to-Face: Modernizing the EMS NPI Process

The six functions every successful NPI needs.

A RECENT EXCHANGE on LinkedIn about the EMS industry got me thinking about the many good, bad and ugly NPI processes I have been part of or audited over the years. While there is no one right answer to launching first articles in the EMS space, far too many unrepeatable and inefficient NPI processes are "time eaters," enabling first-article failures and taking the NPI team away from their day-to-day duties. This month, we examine some basic principles to consider if your NPI process is not consistent from NPI launch #1 to NPI launch #100.

Figure 1. Dedicated online tools allow NPI team members to track their colleagues' progress and reduce face-to-face meetings.

Let's first agree on the definition of NPI and when an EMS should run the NPI process. NPI (new product introduction) is the process by which the EMS validates all steps and procedures needed for a first-article run that, once inspected and approved by the OEM, would permit the EMS to begin its production runs. A product should go through this process in a number of instances, including:

1. When the factory has a new build it has never before produced.

2. When an existing product currently being built is significantly changed.
3. When a product has not been run in a very long time, say, a year.

Why does an NPI run require a robust and repeatable process? Without a documented process that outlines a conscious decision on what action to take, or not to take, decisions are left to memory and chance. Without a robust process, even if a successful NPI launch does occur, the odds are not good that the next run of first articles will be successful. A solid, well-defined process can also be adopted by other manufacturing sites when an EMS operates more than one facility. With most EMS companies advertising seamless transfers between sites to their OEM clients; it only makes sense that an OEM audit should verify whether the same NPI process is used by alternate sites scheduled to build their product.

A good NPI process is phase-gated, allowing functional participants on the launch to communicate and track the required workflow without meeting in person multiple times a week. The brute-force NPI processes, requiring numerous face-to-face meetings, take the functional participants away from their day-to-day tasks so they can simply be updated on the NPI progress, or lack thereof, and talk about any problems the participants may be experiencing as they move through their duties. This is not an efficient way to conduct business.

I strongly recommend online systems be utilized in which each function can update its specific required tasks, see the other team members' progress (read only) and send notes back and forth to each other if questions or important learning occurs. In my case, the best I have seen was a home-baked system used at one of the EMS providers I worked with.

Even if the EMS has a standalone NPI team, as opposed to the functional areas a general manufacturing group would have, the same functions are required to participate in that NPI process through a successful manufacturing first-article run. The goals of these functions are to mitigate a failure in the handoff to manufacturing for the first-article build, and these functions should include:

1. The business office or program manager (the PM should lead the NPI)
2. Materials
3. Product/manufacturing engineering
4. Test engineering
5. Quality
6. Planning (the gatekeeper).

In my case, every task each functional leader could perform was listed on their respective computer screen. Keep in mind that the individual functional leader is the only participant who can update their own tasks, but each team member can see the other members' screens as read-only. In this way, each member can track the progress of the other functional NPI team members. Very few face-to-face meetings are required.

Not every NPI requires every action to be taken. Listing all possible actions an NPI may need requires functional

leaders to make conscious decisions of which actions to take and which are nonapplicable.

The screens should show:

1. The functional owner of the task force.
2. A list of each possible task or action.
3. After each task/action, the screen should permit updates to include "not started," "in process – add a start date and an ECD (estimated completion date)"; and "completed – state the end date finished." Also, a "not applicable" status should be included.

Even in a dedicated NPI team, the functions are similar to the functional manufacturing participants. Let's review these.

1. **Program manager (PM).** The tasks that should be listed include obtaining the latest revised documents from the OEM, including any purchase agreements applicable to the build. The PCB details, the BoM/AVL, any ECNs, test requirements, quality requirements and a risk assessment may all be needed. Is this a leaded or RoHS deal? Are there any certificate of conformity (C of C) requirements?

A review of the purchase order to ensure that it matches the quote is in order. At this point, the team should also decide whether a DfM and DfT are needed based on the product's complexity and the experience/capabilities of the EMS. (Note: A first article is not the right time to find all the design flaws that may make the product unbuildable.) Decisions to request a charge, or to do so at no charge, should be part of the business office's decisions and communicated to the OEM. The PM should lead the NPI kickoff meeting as well. While the supporting functional areas within the EMS should be able to communicate with their OEM counterparts, a clear distinction must be made that the PM and a single OEM point of contact are the only authorized signatures to proceed with the NPI as-is or make changes to specs, the PO or contract(s).

1. **Materials.** Any task required to drive all raw materials should be planned and executed. If a BoM scrub was not performed at the time of the quote, consider one now. The materials plan will consider costs, any consigned material, minimums, NCNR risks, any regulatory compliance issues to obtain the raw materials, PPV and lead times. They will ensure the MRP load of the BoM/AVL matches the bid on the previous quote and determine the logistics of obtaining needed material. Any unknown material risks discovered that may have changed from the bid will be communicated through the PM to the OEM for agreement on how to proceed.
2. **Product/manufacturing engineering.** They ensure all assembly requirements are documented and communicated to the manufacturing team. All assembly tooling is identified and ordered. Even if the EMS relies on its PCB sources for the panel design, it must approve and document the work. Work instructions are generated in the EMS factory's manufacturing support software system. DfM is performed and any major issue that would prohibit a successful first-article run is explained in detail to the OEM, identifying the specific requested action to be taken by the OEM. This group will also determine where in the factory (which SMT line and any secondary operations) manufacturing will occur. (This assumes there is not a defaulted/dedicated NPI line, which makes this decision much clearer.) During EMS first-article validation, before shipment to the

OEM, all critical inspection points are documented (redlined) to accompany the shipment.

3. **Test engineering.** They ensure all test-related activities are identified and communicated to manufacturing. If applicable, a DfT is completed and communicated to the OEM for any corrections the EMS suggests, or risk assessments are rethought if robust test coverage is absent. Will test software come from the OEM, or will the EMS develop it? ICT, FCT, flying probe and boundary scan plans, as required by the purchase order, are delivered to manufacturing. The validation of any test plan should occur at this time.
4. **Quality.** All requirements needed to meet the OEM's quality levels are considered. Incoming raw material inspection and the manufacturing quality plan are documented and given to manufacturing. Any agency approvals are coordinated, and all first-article final inspection requirements are documented and communicated to the responsible FQA individual on the build team.
5. **Planning.** This is the ultimate gatekeeper of the NPI process. They must ensure all changes are made and monitor each functional team member's progress with their tasks so the kit drop will be timely to meet the EMS's committed first-article ship date. They provide a last look at the BoM structure and manufacturing order, ensuring they are accurate. When a high percentage – say 80% to 90% – of all the teams' tasks are completed, they schedule the kit drop, which acts as the final "clear to build" warning to the NPI team to clean up any unfinished actions, as manufacturing capacity has now been scheduled and the kit drop is imminent.

An online NPI process like this has many advantages.

1. Mitigates numerous time-consuming face-to-face team meetings for updates or questions.
2. Ensures all steps needed for the NPI are completed and establishes a repeatable process that the NPI #100 launch will follow the same process as NPI launch #1.
3. Ensures no critical action is missed, or a non-essential action is taken, leading to more successful initial first-article runs completed by the EMS.
4. Gives the OEM confidence when making sourcing decisions for new product awards.
5. Mitigates missing committed ship dates made by the EMS to the OEM and paves a path for a faster release of follow-on production runs, generating revenue for the EMS.
6. Supports any TTM and TTV constraints the OEM may be under.
7. Knowing the details of such a robust process is an excellent sales and marketing tool to win new clients.

What are the biggest NPI issues I have seen in the EMS marketplace?

1. An NPI process left to individual whims and experience.
2. Employing unrepeatable processes that vary even within the same customer's launches.
3. No DfM or DfT deployed on extremely complex designs, only to find unbuildable issues that stall the expensive SMT lines for days and cause missed ship commitments on the first articles. SMT lines idling while design or manufacturing issues are solved not only hurt committed first-article ship commitments but can negatively

affect other customer commitments.

4. Brute-force NPI processes requiring numerous in-person team meetings every week, chewing up time from other day-to-day tasks. This also impacts other customer issues and leads to dissatisfaction.
5. Critical tasks missed, contributing to first-article failures.
6. First-article failures resulting in an OEM walking away from the EMS after a large, hard-fought deal was won, and a multimillion-dollar revenue stream exiting to a competitor. (It takes a year or two to win most new large deal clients; how does the EMS get that time back?)
7. The EMS missing its revenue plan due to a shortfall of new business caused by failures to launch.
8. For a publicly traded company, missing guidance for the quarter or year due to failures to launch.
9. Inconsistent EMS NPI processes from site to site, causing a first-article failure at a relocated EMS site, after successful builds at the initial site.
10. Changes agreed upon by the OEM and EMS but do not follow a strict signature approval process, costing the EMS unexpected costs and OEM dissatisfaction.

In conclusion, nothing shakes an OEM's confidence in its EMS selection like a failed first article. Moving to a new EMS is risky, and many new customer relationships have dissolved prior to a full-ramp revenue stream due to failed NPI launches.

An online NPI process permitted a small (mid-tier) EMS to divest all the PCBA manufacturing from a high-tech defense industry OEM and conduct over 250 NPIs in under 10 months, as well as continue its normal flow of NPI process with its existing customers.

If you have any off-the-shelf software that handles a similar online process, let us know so the EMS industry can continue to evolve. "Snitches may get stitches," but bad NPI processes bruise our business.

JAKE KULP is founder of JHK Technical Solutions, where he assists OEMs and EMS companies with optimizing demand creation offerings and deciding when and where to outsource manufacturing. He previously spent nearly 40 years in executive roles in sales and business development at MC Assembly, Suntron, FlexTek, EMS, and AMP Inc. He can be reached at jkulp@cox.net.

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REBUILDING **THE BASE**

The Hidden Crisis: Why North America Can't Outsource Its Future

Hope that nothing will interrupt imports of PCBs and parts is not a strategy.

THERE'S A CRISIS in our industry that few want to talk about and even fewer want to admit. It's not a quality crisis. It's not a pricing crisis. It's not even a technology crisis. It's a dependency crisis, and it threatens our companies, our customers and our country.

For decades, North America quietly outsourced its most critical electronic capabilities. First slowly, then eagerly, then recklessly. Printed circuit boards, components, subassemblies, entire supply chains – handed over to overseas suppliers, including near-peer adversaries, under the assumption that efficiency and low cost were the only metrics that mattered.

But the past four years have exposed a truth that is no longer avoidable: A nation that cannot produce its own electronics cannot secure its own future.

And that is the hidden crisis this industry must confront.

The Covid Wakeup Call We Still Haven't Fully Heard

When the pandemic hit, the global electronics industry didn't bend; it snapped.

Factories shut down. Ports stalled. Lead times ballooned. Components vanished. Entire production lines went dark because a single part on the other side of the world couldn't get onto a boat.

And here's the part everyone remembers but few want to internalize: North America discovered just how little of the electronics supply chain it actually controlled.

No transportation strategy, no buffer stock program, no heroics from purchasing departments could change one fact: if essential electronics were stuck overseas, nothing could bring them home.

Covid didn't create the vulnerability; it revealed it.

And yet, incredibly, many companies have slipped back into old patterns: chasing the lowest quote, assuming the global system is stable again, convincing themselves the disruptions were a one-time event.

Common sense says otherwise.

The Geopolitical Tensions No One Can Ignore

If Covid was the wakeup call, China is the blaring alarm that won't shut off.

The electronics supply chain is more concentrated in China than oil production is in the Middle East. It's a choke point, a single point of dependency, a geopolitical wildcard waiting to become a strategic catastrophe.

Tensions rise. Threats escalate. The world becomes more complex. And our industry still relies on the hope – not the plan – that nothing will interrupt shipments of PCBs, ICs and assemblies from across the Pacific.

Hope is not a supply-chain strategy. Hope is not a national security policy. Hope is not a business model.

Common sense: If a single country holds the keys to your manufacturing, then your future is not your own.

This isn't about demonizing foreign suppliers. It's about recognizing reality. The US, Canada and Mexico need resilient domestic capacity not because it's patriotic – but because it's practical, responsible and essential.

Defense readiness depends on manufacturing readiness. Here is the question every aerospace and defense company should be asking: How do you defend a nation with weapons you can't build without foreign supplies?

Missiles, fighter jets, satellites, secure communications, radar systems – each relies on PCBs, microelectronics and assemblies.

If those cannot be produced domestically at scale, the defense industrial base is an illusion. If production can be disrupted by geopolitical decisions outside our borders, then readiness is compromised before the first shot is fired.

The Pentagon knows this. Congress knows this. Every OEM building mission-critical technology knows this.

The bottleneck is not awareness. The bottleneck is action.

And this is where PCBAA steps in.

Figure 1. Industry companies are finding their voice through PCBAA.

PCBAA: The Unified Voice Industry Has Needed for Years

The Printed Circuit Board Association of America exists for one simple reason: North America cannot afford to lose control of its electronics manufacturing.

PCBAA is not another trade group sending newsletters and hosting polite conferences. It's a coalition with a mission: rebuild domestic PCB and PCBA capacity, restore capability, and return strategic independence to an industry that gave it away too cheaply (freely)?

Here's what PCBAA is doing right now:

1. **Driving policy that moves the needle.** PCBAA has taken the lead in educating Congress, the Department of War, and the whole of government on the vulnerabilities that come from overseas dependence. The organization was instrumental in the introduction of the bipartisan Protecting Circuit Boards and Substrates (PCBA) Act (H.R.3597) – the first major piece of legislation in decades aimed at revitalizing our sector.

This isn't abstract advocacy. This is the work that brings incentives, grants, and investment home.

2. **Giving manufacturers a collective voice.** One company speaking to Washington is a whisper. Eighty companies speaking together is a force.

PCBAA amplifies the voice of manufacturers, assemblers, suppliers and innovators that understand that the US cannot remain competitive if 96% of the world's PCBs are made elsewhere.

When we speak together, we get heard. When we move together, we get results.

3. **Building real momentum for reshoring.** Everyone says reshoring is important. PCBAA is the organization making it happen.

By uniting the full ecosystem – from fabrication to assembly to materials to equipment and testing – PCBAA is accelerating potential investments in new capacity, new technologies, and new domestic partnerships. Members are connecting with OEMs, actively moving work home. They're aligning with federal priorities. They're positioning themselves to lead, not follow, the next decade of electronics manufacturing.

Why Membership Matters

Joining PCBAA is not symbolic. It's not a gesture. It's not a line on a website.

Membership is a commitment to shaping the future of the industry rather than being shaped by it.

Here's the simple truth: The companies that join PCBAA are helping decide what the next 20 years of North American electronics manufacturing will look like.

They are the ones:

- influencing legislation
- guiding federal priorities
- supporting strategic investment
- and rebuilding the industrial base every OEM depends on.

This industry is at an inflection point. Either we rebuild domestic capability now – while we still can – or we continue drifting toward a future where North America is a customer rather than a maker of its own technology.

Common sense says the choice is obvious.

Your Voice Matters More Than You Think

Every company in this sector, large or small, shares the same vulnerability – and the same opportunity.

If you build PCBs, assemble electronics, design hardware, supply materials or support manufacturing in any way, you have a stake in where this industry is heading.

And if you believe North America should be able to build the technology that powers its defense, infrastructure and innovation, then you have a place in PCBAA.

The hidden crisis is real. The risks are rising. The time for passive concern has passed.

Joining PCBAA is how this industry takes back control, rebuilds resilience, and ensures that our future is made here – not imported with fingers crossed. More information at pcbaa.org.

The future is too important to outsource.

DAN BEAULIEU is a longtime management consultant to the printed circuit industry and a member of the PCBAA; danbbeaulieu@aol.com. PCBAA is exhibiting at PCB East this spring in the Boston suburbs.

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ON THE FOREFRONT

AI Data Center Packaging Challenges Highlighted at Nepcon Japan

How fully has AI taken over packaging, power and manufacturing priorities?

WITH MORE THAN 92,000 visitors and 1,850 exhibitors, Nepcon Japan celebrated its 40th anniversary in Tokyo in late January. Exhibit areas included IC and sensor packaging, power devices and modules, test, electronic component and materials, fine process technology and printed wiring boards, plus halls devoted to automotive, smart factory and robotics.

Almost every booth in the smart factory section mentioned AI. Automotive components and analysis services were on display. In Automotive World, MarkLines displayed its teardown of BYD's new, higher-priced (¥23 million or $146,818) SUV. The teardown focused on the frame, battery and electronic boards and included a BoM analysis. LTEC featured automotive boards the company examined for its IP analysis. Inventec, known for its PC and server design and manufacturing, provided details of its expansion into automotive electronics with IATF 16949-certified facilities in Taiwan, China, the Czech Republic, Mexico and Thailand. Solutions focused on vehicle computing, e-cockpit domain controller/cluster, connectivity and smart mobility (digital key/wireless charger) with hardware and software integrated solutions. The robotics section included Sony's OmniBall, a wheel used for robotics that can move on a step with a height close to the diameter of a ball.

Crowds overflowed the special conference sessions on advanced packaging focused on high-performance packaging trends driven by the AI data center demand. Resonac provided an update on consortia activities. The Kawasaki Packaging Solution Center's research focused on 300mm wafer and 510mm x 515mm panel development for silicon and organic interposers with technology developments in fine bump interconnection (10μm), fine circuitry (1μm lines/spaces) for interposers and large package (140mm x 140mm substrate) reliability. The new advanced panel-level interposer center development activities will cover production developments for large interposers (8x to 12x reticle size) on panels. At least 27 companies are participating in this research at the Ibaraki site. The new packaging and power solution center in Oyama will focus on power module development, including power device performance, materials and thermal management.

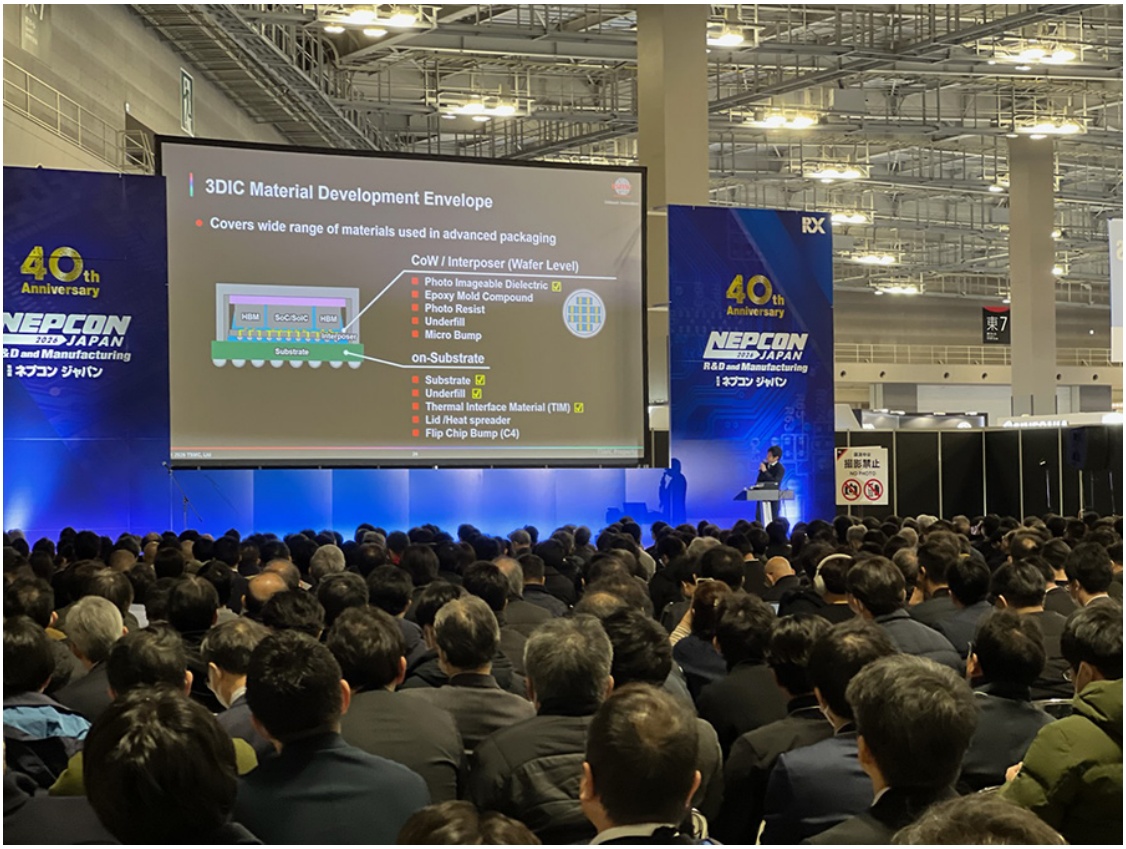

Figure 1. Large crowds adorned Nepcon Japan.

The TSMC Japan 3DIC R&D Center's presentation focused on the challenges of AI compute packaging and described the rapid evolution of chip-on-wafer-on-substrate (CoWoS) interposer technology at TSMC. While Si interposer (CoWoS-S) has been in production for more than a dozen years, redistribution layer interposers (CoWoS-R) and CoWoS-L, which include a silicon bridge for higher density, are moving into production to handle the demand for larger interposers. TSMC indicated that by next year, a 9.5 reticle-size CoWoS-L will be ready to support hybrid bonded solutions and high-bandwidth memory (HBM) integration. TSMC described the drive to panel-level production of RDL interposers to support the increased number of HBM stacks. TSMC introduced its Compact Universal Photonic Engine (COUPE) stacking process using hybrid bonding for photonic and electronic chips **(Figure 2)**. The solution is expected to be in production in 2027 for copackaged optics networking applications. Packaging challenges including substrate warpage control, thermal management, new materials needs and test issues were highlighted.

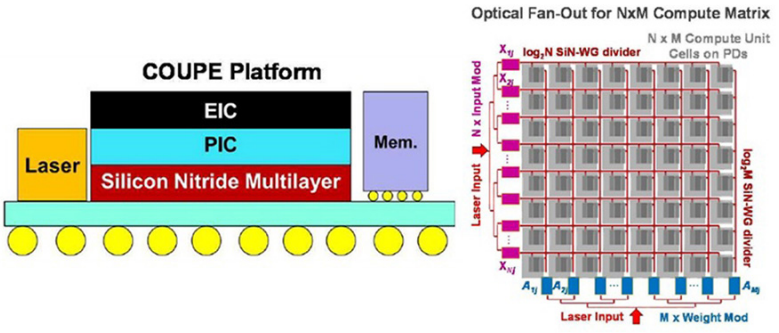

Figure 2. TSMC's COUPE stacking process integrates ICs directly onto photonic integrated chip (PIC) wafers.

Intel described some of the latest glass-core substrate developments and indicated that an electrically functional test vehicle with three buildup layers on each side of a glass core was demonstrated with a 75µm through-glass via (TGV). A 78mm x 75mm package with an 800µm glass core substrate and 10 buildup layers on each side has been fabricated and singulated without cracking. Assembly and board-level reliability tests are underway.

Another IFS presentation emphasized the company's embedded multi-die interconnect (EMIB) technology that first shipped in 2017 and is being expanded to finer pitch using a bridge with through-silicon vias (TSVs). The FOVEROS R (RDL) and B (Bridge) technology offerings were mentioned. FOVEROS direct stacking options with microbumps and hybrid bonding (<10µm pad pitch between die) were also described.

Copackaging Advancements

Samsung introduced technology to support advanced packaging, including a 120mm x 120mm substrate with 11 build-up layers on an eight-layer core with options for Si capacitors and MLCC capacitors. The substrate can support copackaging of memory, logic and optics. Trends toward fine features (5µm ~2µm L/S) with 10µm diameter vias, die-to-die interconnects and/or direct RDL on build-up substrates to support HBM that provide signal and power integrity were discussed. Samsung also described R&D on glass core substrates and plans to establish a prototype line.

Rapidus, Japan's new foundry startup, highlighted its panel-level package developments focused on a 600mm x 600mm panel with 2µm line and space capability. The line is expected to be ready in 2028.

3D SiP Addresses Power Challenges

Data center power delivery challenges were also highlighted at the conference. The emerging trend toward 800V DC in new data center architectures is driving demand for advances in power delivery. As racks reach up to 500kW, high-voltage direct-to-rack, or near-rack architectures, are driving changes to provide the required power density. ASE and others have noted the high-end computing power supply migration from 12V and single-stage power converter to 48V input, multi-stage power converter with the introduction of integrated voltage regulators, and the addition of L/C to the chip and package. ASE is proposing its 3D SiP technology and embedded technology for reduced X-Y area, reduced Z height, higher component density, shorter electrical and thermal transmission path, and lower power consumption. Vertical power delivery technology, in which the power modules are positioned directly beneath the processor to reduce the distance current must flow through the substrate, can significantly decrease power delivery network losses. Suppressing power noise is also critical. ASE notes that vertical power delivery provides an 8% power savings and a 30% size reduction compared to lateral power delivery.

Providing efficient power delivery to high-performance devices such as AI training and inferencing ICs is driving the development of new high-performance capacitors and even the adoption of embedded capacitors and voltage regulators in package substrates. Exhibitor Saras Micro Devices highlighted its high-density capacitor and integrated voltage regulator technology **(Figure 3)** that can be embedded in the substrate.

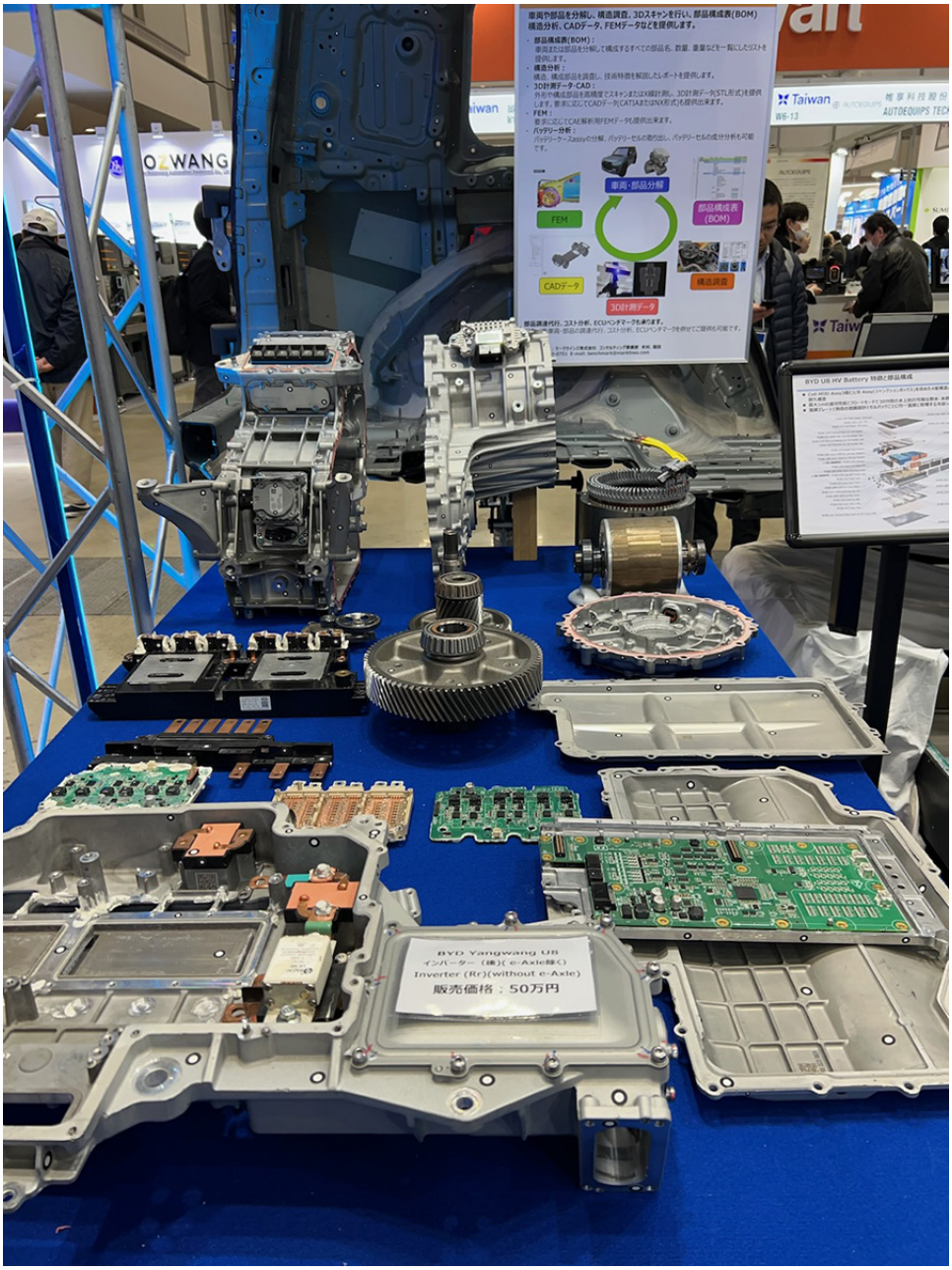

Figure 3. Saras Micro Devices' multi-domain, integrated passive module.

Power modules were a major focus of the show, with hundreds of exhibitors and numerous presentations. Infineon described its power module options, highlighting its module developments to support higher voltages. As data centers move to higher voltage, the importance of this segment of the industry will grow, and Nepcon will be an important show to attend to follow this trend and other key developments.

E. JAN VARDAMAN is president of TechSearch International (techsearchinc.com) and a contributing editor for PCD&F/CIRCUITS ASSEMBLY; jan@techsearchinc.com.

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Splitting a PCB for Concurrent Design

As PCB designs grow more complex, partitioning and teamwork become part of the layout strategy.

PRINTED CIRCUIT BOARD design grows in complexity with each passing year. Many protocols must be implemented. An ASIC (application-specific integrated circuit) or an FPGA (field-programmable gate array) may be the center of attention, but there will likely be a memory bus along with other architectures, such as ethernet or USB, to move data around. Interacting with the world around us requires some sort of sensor to read the room, while other circuits are used to feed this processed data back to the user.

As mixed-signal designs become more common, it makes sense to divvy up the work to those who have the necessary skills. Printed circuit board designers tend to fall into a specialty. Their first job becomes an anchor that pulls them back to that same technology.

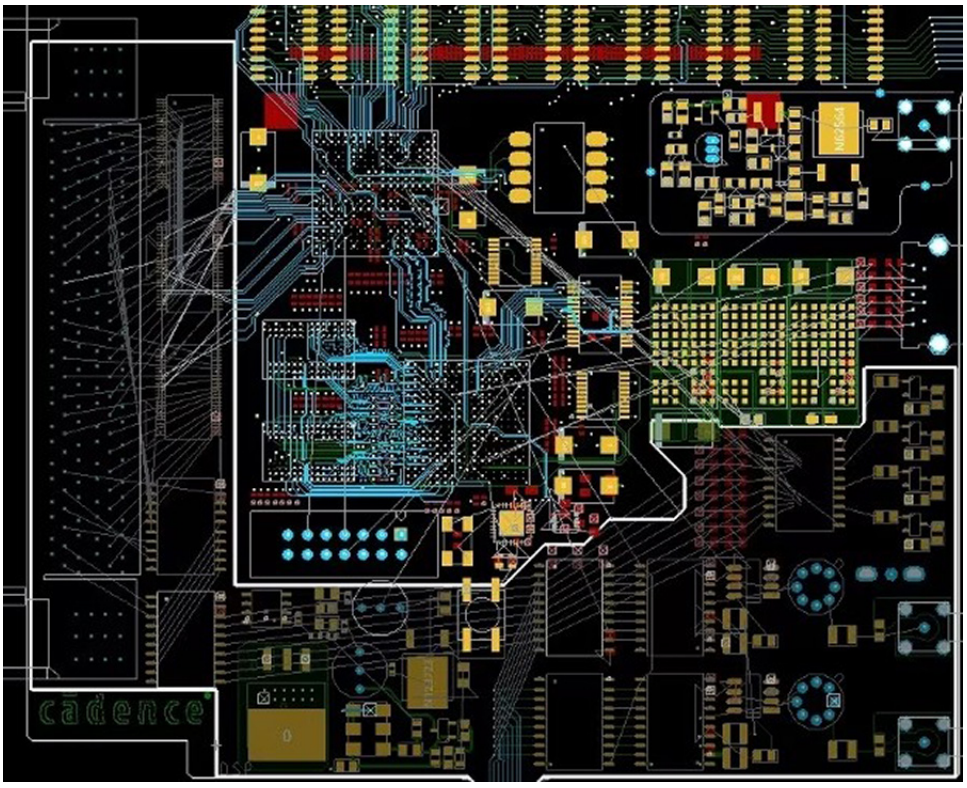

Figure 1. The initial partition is gerrymandered from the upper left to the lower right, containing 108 components. Note that the components within the partition are dimmed and locked from editing. The small pocket in the upper right corner with 38 components might be worth another partition. (Source: Author)

At least, that's how it worked for me and an analog layout. I didn't see a DDR (double data rate) memory device until 2013. By 2017, the DDR was stacked above the processor, eliminating the routing effort altogether. When I saw my first Xbox One X main logic board, the DDR5 was a beautiful 12-package array, locked down and off-limits. While I have struggled through the constraint capture and routing of a smaller DDR3 memory circuit, I'll never be an expert.

The process of compartmentalizing the board must follow high-level placement as a minimum. This floor planning revolves around the SI/PI goals. Identifying and capturing the design parameters is a must before anything gets turned loose. As the owner of the deliverables, it's best to concentrate on the PDN study since it's everywhere. You can optimize bottlenecks and other conflicts of interest early in the design cycle.

The second priority when defining a partition is to minimize the number of connections to and from the circuit block. The overall placement will drive data flow. Routing to an SD card or some other I/O is often suboptimal in terms of trace length. These inevitable rivers of traces can and will be routed from one partition to another. The person working inside the box will see where the traces come in and can go from there.

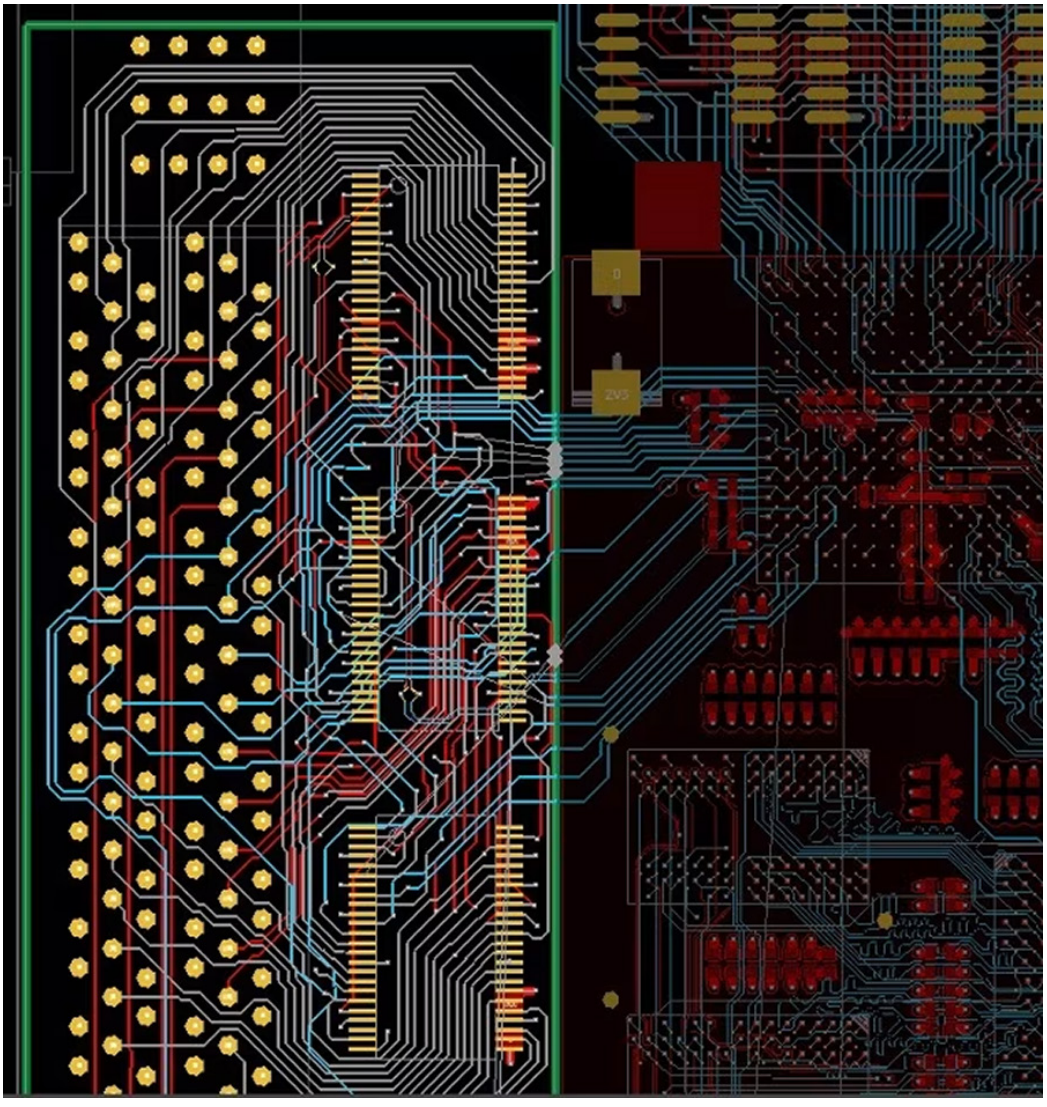

Figure 2. This is the point of view while working inside the partition. Completing the connections that span from the dark side to the bright side is a high priority. A few left here can be completed when the layout is all together. (Source: Author)

Our use case involves a service bureau and an internal resource, with me in the driver's seat. A hierarchical schematic may not be for everyone, but in this case, it allowed us to decouple from the wireless portion of the design. That's a high-touch effort, so we kept it in-house. For reference, this was a breakout board for a smartphone. The main function was to measure current, plus the typical P1 experiments you do when it's two years before production starts.

The RF section was essentially "set it and forget it." My day-to-day area of concern took place under the footprint of the Qualcomm chip. At that point in time, the chip didn't exist, and neither did a reference design. I got to fan out my very own Snapdragon!

The power integrity engineer sent me back to the drawing board three times before signing off. It came with a warning not to change any of the shapes, not even a little. It was then that I understood why Qualcomm staff told me not to touch the SoC while routing the SDIO (secure digital input/output) lines back in the day. Mobile chips are very sensitive to power distribution. Solving all this drama makes me want to stick with radio boards.

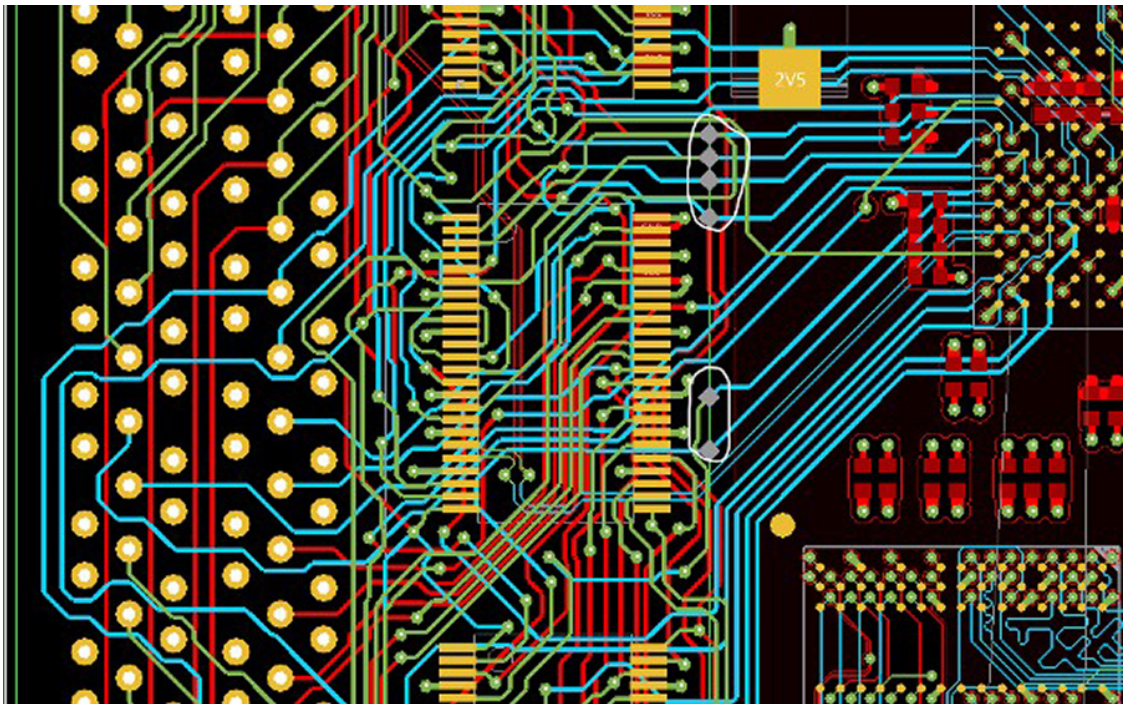

Figure 3. The side and main jobs are merged. Result: the big connector is squared away. One lesson learned: I put more space between the guideposts (gray diamonds) that preset the crossover points. With the left edge secured, we will have new instructions and primary routing to the southern edge done before re-exporting the partition. (Source: Author)

Meanwhile, the service bureau had a large board area sectioned off with some big connectors on one end and a whole bunch of op amps and sense resistors to enable across the board. I fanned out one big connector to the LC filters and told them to do the others the same way. Leaving them a few examples was better than hoping that they could read my mind.

At some point, all these things had to be brought back together under one design. Importing the completed section could take a few hours. I learned some things about documenting what's inside the partition before sharing. It's very easy to list the components in an area.

It would have saved me some time to set up the display and other options with a script. Playing back the script would have reset the environment to its exact conditions so everything would come back as planned. I encourage satellite workers to start a script that can play back their contribution if the reimport process runs into a jam.

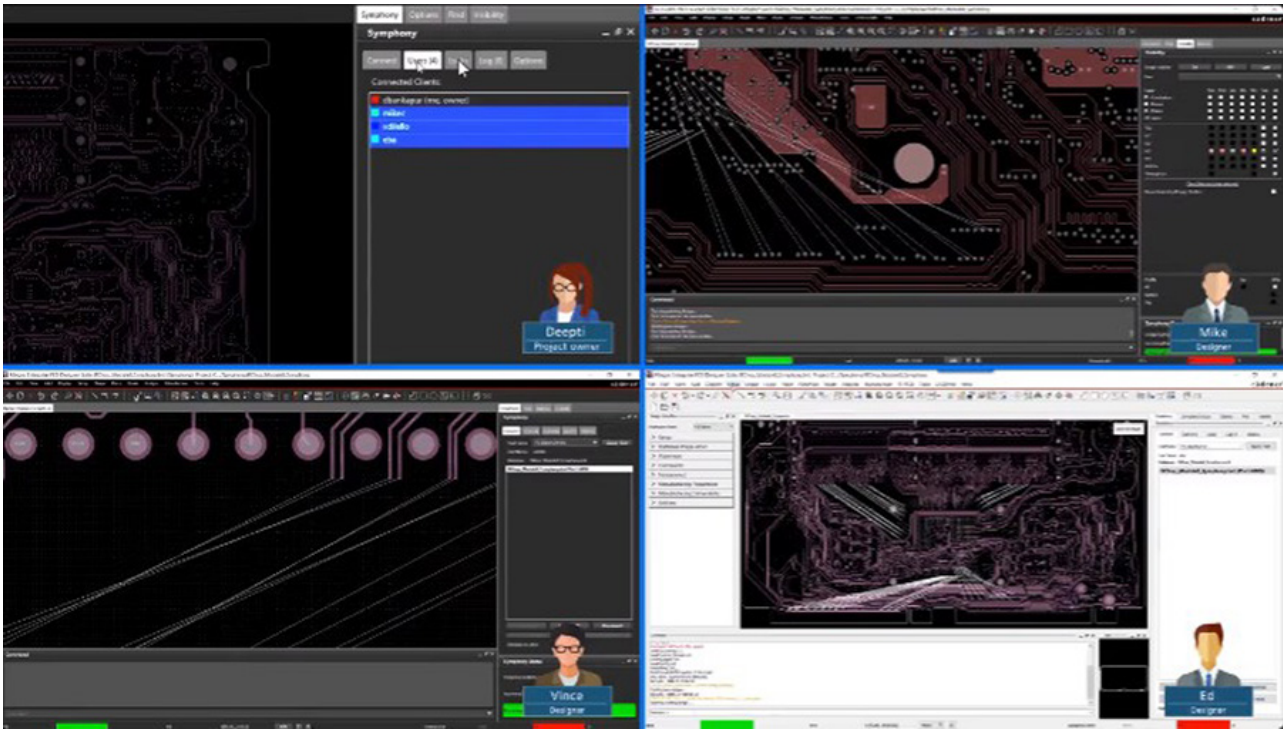

Figure 4. A screen grab of a multiuser design environment in Allegro X. Each user can work on different sections of the board in parallel to get designs completed earlier. As a human, I have a knack for length-matching; not sure if that's universal. (Source: Cadence)

With the process limits of this approach in mind, the key players creating enormous printed circuit boards will take a fully networked approach to design. A team of designers can combine efforts in real time with a single networked database.

A certain mojo goes along with online role-playing games. People with similar personality defects form bonds while going through video game battles against space monsters or villains. That kind of "solve it to win" scenario can also be found when three people are distilling strategy into tactics that solve a printed circuit board with "a million" pins.

Having a few subject matter experts in your corner sounds like a good deal.

JOHN BURKHERT, JR. is a principle PCB designer in retirement. For the past several years, he has been sharing what he has learned for the sake of helping fresh and ambitious PCB designers. The knowledge is passed along through stories and lessons learned from three decades of design, including the most basic one-layer board up to the high-reliability rigid-flex HDI designs for aerospace and military applications. His well-earned free time is spent on a bike, or with a mic doing a karaoke jam.

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DESIGN **BEST PRACTICES**

Beyond DRC: Constraint-Driven Design as an Ongoing Relationship

Why the most reliable PCB designs are built through continuous dialogue with fabricators, not one-time rule checks.

IN THE RELENTLESS pursuit of innovation, the world of PCB design often spotlights the heroics of schematic capture and layout. We meticulously route traces, place components, and then, with a sigh of relief, hit the "run DRC" button. Design rule checks are crucial – they are digital sentinels, guarding against fundamental manufacturing flaws and ensuring our designs adhere to basic geometric and electrical principles. But true reliability, peak efficiency and market success in PCB design hinge on something more profound than passing a DRC: cultivating a dynamic relationship with your PCB fabricator, and transforming this supplier into your most powerful ally.

Your Fabricator – An Unsung Hero

Let's paint a common picture. You've just completed a complex PCB design, brimming with cutting-edge features.

You confidently send your manufacturing output files to two different fabricators.

- **Fabricator A:** Upon receiving your files, its expert CAM engineers meticulously review every detail. They identify a subtle, yet critical, aspect of your design – perhaps a tight impedance control requirement clashing with a specific material stackup, or a fine-pitch component landing pad that pushes the limits of its standard etching capabilities. They pause production, issue a detailed technical query (TQ) outlining the potential issue and propose solutions, seeking your input.
- **Fabricator B:** It receives your files, runs its automated checks and proceeds with manufacturing without a word. It might produce the boards exactly as designed, even if that means compromising yield, increasing costs or subtly introducing latent reliability issues that won't surface until much later in the product's life cycle.

At first glance, Fabricator B might seem like the easier choice, because they just "got the job done." But consider the long-term implications. Fabricator A, by raising that TQ, is not trying to be difficult; it is actively protecting your product's integrity and your company's reputation. It is performing a critical, often thankless, role as your invisible team member. It is doing its due diligence, acting as a proactive partner to ensure your design is optimally manufacturable, reliable and cost-effective.

We often inadvertently penalize Fabricator A for its thoroughness, viewing TQs as delays. It's time we shift our perspective. This fabricator is your early warning system, your quality control gatekeeper and your manufacturing consultant, all rolled into one. Ignoring its invaluable contribution is akin to ignoring a critical member of your internal design team.

The Transformative Power of a Strong Designer-Manufacturer Relationship

Moving beyond a purely transactional relationship with your PCB manufacturer is not just beneficial; it's transformative, and yields tangible, long-lasting advantages:

Bringing manufacturing inputs to the point of design (proactive prevention). Imagine designing a complex system without understanding the power supply's limitations or writing software without knowing the processor's architecture. Unthinkable. Yet many PCB designs are initiated without a deep understanding of the manufacturing process that will bring them to life. A strong relationship with your fabricator changes this entirely. It allows you to integrate its specific manufacturing constraints and capabilities directly into your design process from the start. This means understanding its preferred trace width and minimum spacing, standard laminate materials and stackups, panelization capabilities, and cost drivers before you lay down the first trace. It's about designing with manufacturing in mind, not just for manufacturing. This proactive approach drastically reduces costly redesigns, accelerates time-to-market and optimizes your bill of materials (BoM).

Building a more reliable product: engineering for longevity. When your design inherently recognizes the real-world manufacturing environment, you naturally engineer a more robust and reliable product. Think of it as designing a house with the builder's tools and techniques in mind from day one, rather than handing over blueprints

and hoping they can figure it out. Fewer manufacturing iterations mean less stress on components and materials. Fewer last-minute design changes translate to a more stable and predictable production flow. A higher first-pass yield from the fabricator directly correlates to a product that performs as intended, right out of the gate, reducing field failures and warranty claims. This proactive reliability engineering, baked in through collaborative constraint-driven design, is a hallmark of truly high-quality products.

Collaborative handoff: A smooth baton exchange, not a "wall toss." The traditional model of design handoff often resembles a "throw it over the wall" scenario. The design team completes its work, bundles the files and sends them off, often with minimal direct interaction. This approach is ripe for misinterpretations, missed details and inefficiencies. A strong relationship, however, fosters a truly collaborative handoff. It's akin to a perfectly executed baton exchange in a relay race – smooth, synchronized and with a shared understanding of the next steps. This involves clear communication channels, pre-production meetings and mutual understanding of expectations. The fabricator isn't just executing instructions; they're an extension of your design team, ensuring a seamless, error-free transition from digital blueprint to physical product.

The Evolution of Trust

Early in my PCB design career, the constant stream of fabricator TQs was a significant bottleneck, causing frustrating work stoppages and hindering project timelines. This recurring challenge wasn't just an annoyance; it was a drain on efficiency and a direct impact on time-to-market.

This experience ignited a critical shift in my design philosophy. I realized that true efficiency lay in preemptive problem-solving and a proactive DfM strategy. By leveraging advanced DfM tools, my goal was clear: to mirror the fabricator's exact DfM rule checks. This would allow me to eliminate TQs, deliver truly DfM error-free data and dramatically accelerate the fabrication cycle.

Obtaining these critical, proprietary DfM rule files proved to be an unexpected hurdle, however. Despite persistent efforts, initial requests were consistently met with resistance. It became clear that access to these invaluable resources was not a given, but a privilege earned through sustained collaboration and trust. It took dedicated effort across several projects and a considerable timeframe to build the relationships necessary to secure these vital DfM rule sets. This breakthrough not only streamlined my workflow but also underscored the immense value of strategic partnership in achieving seamless, efficient production from design to delivery.

Over time, I learned that it's not uncommon for manufacturers to initially be hesitant to share their proprietary manufacturing constraints. Their processes, their unique capabilities and their internal "secret sauce" are often considered intellectual property. This reluctance is understandable. But once a foundation of trust is established – built on consistent communication, mutual respect, and a shared commitment to quality – this dynamic shifts dramatically.

When a manufacturer perceives you not just as a customer, but as a valued partner, it becomes significantly more willing to open its books. It will share insights into equipment tolerances, preferred panelization strategies, material purchasing power, and upcoming technology upgrades. This isn't just about design for fabrication (DfF); it extends

powerfully to design for assembly (DfA) as well. Understanding your assembler's capabilities – component placement accuracy, preferred soldering profiles, automated optical inspection (AOI) limitations and testing methodologies – allows you to optimize layout for efficient, reliable and cost-effective assembly. This holistic approach, driven by the collaborative sharing of manufacturing and assembly constraints, elevates your design from merely functional to truly exceptional. It's about co-creating a product that is optimized across its entire lifecycle.

Shared Concerns

Ultimately, when you invest in establishing a deep, trusting relationship with a manufacturer, you gain something immeasurably valuable: a genuine partner who is as invested as you are in the success of your product. It becomes an extension of your team, a vested stakeholder in your outcomes. This means:

- **Proactive suggestions.** The fabricator might suggest a slight modification to a pad shape that significantly improves solder joint reliability or recommend an alternative material that offers better performance at a lower cost.
- **Early issue flagging.** The fabricator will flag potential issues before they escalate, offering solutions rather than just pointing out problems.
- **Shared problem-solving.** When challenges inevitably arise, the fabricator will work alongside you, leveraging its deep manufacturing expertise to find creative and effective solutions.
- **Long-term visions.** The fabricator understands your product roadmap and offers insights that can help you plan future iterations, ensuring scalability and continuous improvement.

This level of commitment transforms the manufacturing process from a mere service transaction into a true collaboration. It ensures that your innovative designs not only come to life but thrive in the competitive real world, delivering consistent performance and reliability.

So, the next time you embark on a PCB design project, remember that constraint-driven design is far more than a static checklist of rules or a one-time DRC pass. It's about cultivating a dynamic, ongoing relationship with your fabricator – that indispensable, invisible team member. It's about leveraging its invaluable expertise, engaging in open dialogue and building a foundation of trust. This isn't just good practice; it's an essential strategy for achieving unparalleled reliability and efficiency, and ultimately lasting success in the complex landscape of modern electronics. It's an ongoing dialogue, a shared journey and the ultimate recipe for bringing truly exceptional products to market.

STEPHEN V. CHAVEZ is a senior printed circuit engineer with three decades' experience. In his current role as a senior product marketing manager with Siemens EDA, his focus is on developing methodologies that assist customers in adopting a strategy for resilience. He is an IPC Certified Master Instructor Trainer (MIT) for PCB design, IPC CID+, and a Certified Printed Circuit Designer (CPCD). He is chairman of the Printed Circuit Engineering Association (PCEA); stephen.chavez@siemens.com. He will speak on HDI and UHDI design at PCB East in April.

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KEYNOTE: Advanced Packaging and the Future of System Optimization

Global AI infusion is redefining performance, power, and integration requirements, placing advanced packaging at the forefront of semiconductor innovation. As chip architecture complexity increases, the industry is progressing beyond device-level scaling toward system-level optimization. Advances in heterogeneous integration and packaging-enabled co-design are shaping more efficient, scalable, and resilient systems. Moving forward, system-centric strategies that align architecture, packaging, and collaboration across the ecosystem are paramount to shaping the golden era of AI and semiconductors.

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ECAD TIPS & TRICKS

How to Determine Your PCB Design Statistics

The Summary Drawing Report in OrCAD X compiles key PCB layout metrics to support design accuracy checks.

WHEN COMPLETING A PCB design, it is important to obtain a summary of the design to determine your PCB design statistics and verify accuracy. PCB design statistics can include:

- Layers and design thickness
- Number of padstacks
- Minimum drill size
- Number of holes in the design (plated and unplated)
- Drilling requirements for holes and vias
- Completed and missing connections
- Number of placed and unplaced components
- Trace summary

This information helps to verify that the design is completed and communicates critical design information to stakeholders and manufacturers. OrCAD X creates a summary report containing PCB design statistics for efficient review of critical design information. This how-to provides step-by-step instructions on how to determine PCB design statistics by creating a summary drawing report in OrCAD X.

Determining Your PCB Design Statistics

1. Open the desired design in OrCAD X PCB Designer.

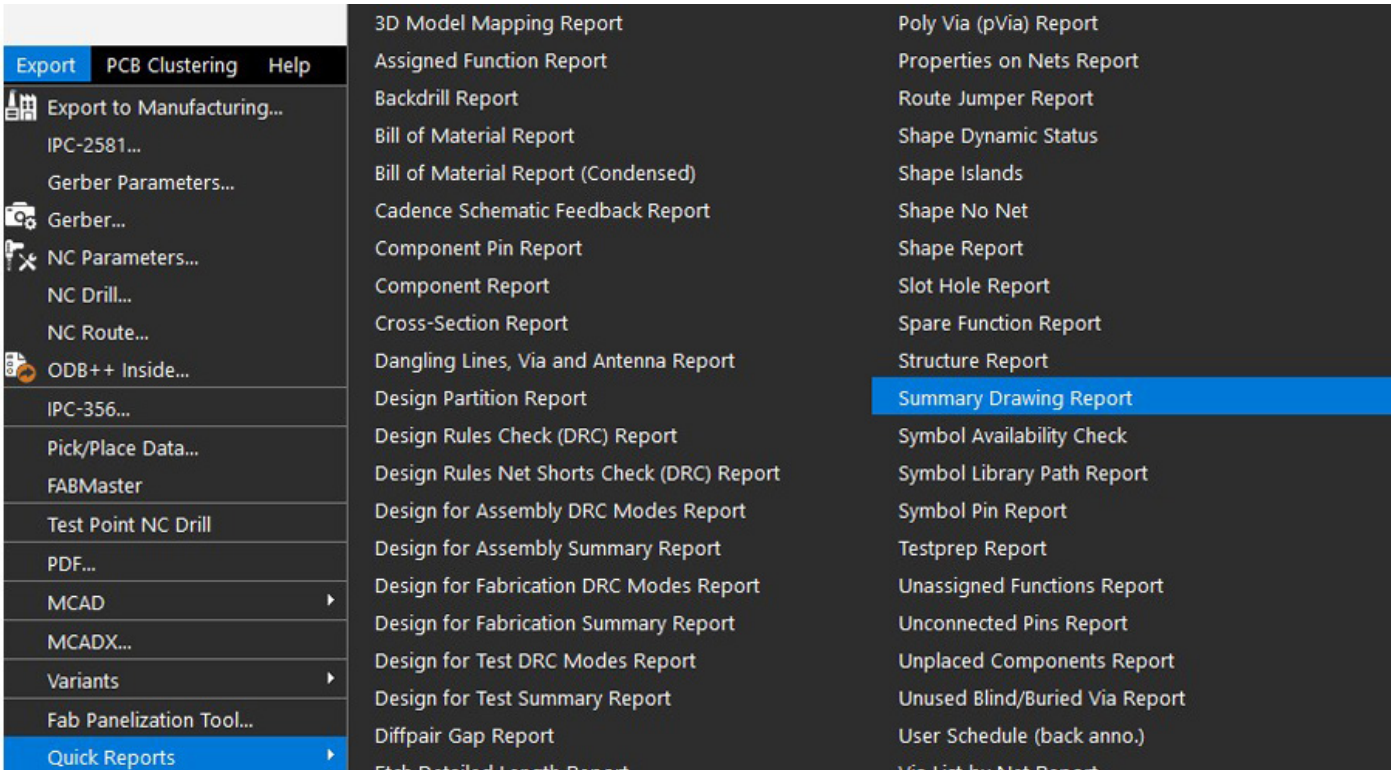

Figure 1. Generating a Summary Drawing report in OrCAD X.

2. Select Export | Quick Reports | Summary Drawing Report from the menu.

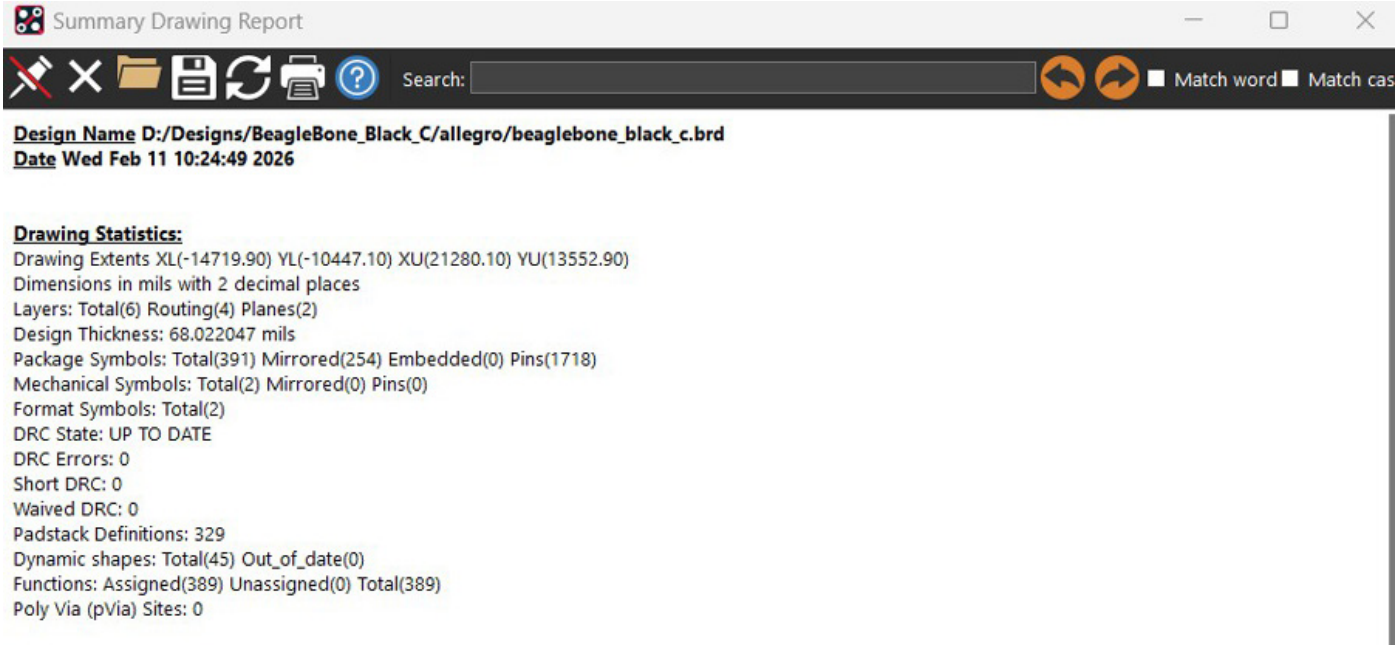

Figure 2. Determine your PCB Design Statistics with OrCAD X.

3. View the Drawing Statistics. Information reported here includes:

- Total layers
- Design thickness

- Total package symbols and mechanical symbols
- Design rule check information

4. View the Drilling Statistics. Information reported here includes:

- Minimum drill size
- Number of drills, standard and non-standard
- Number of holes, plated and non-plated
- Number of vias

5. View the Connection Statistics. Information reported here includes:

- Number of connects
- Completed connections
- Missing connections
- Dangling connections
- Trace length

6. View the Layout Statistics. Information reported here includes:

- Components
- Component class breakdown
- Route keep-in
- Pins
- Layout Area
- Pin Density

7. View the Trace Layer Statistics. Information reported here includes:

- Board layers
- Number of clines per layer
- Number of shapes per layer
- Number of component pins per layer

8. View the Trace Widths By Layer. Information reported here includes:

- Board layers
- Trace width per layer

9. Verify the completeness and accuracy of the design.

Additionally, this information can be used for reporting, design reviews, manufacturing, software quoting and more. Save or print the Summary Design Report as required, then close the window.

Wrap Up and Next Steps

Quickly obtain a summary of the design to determine your PCB design statistics and efficiently review critical design information with the Summary Drawing Report in OrCAD X.

SHANNON HENRY is electrical engineer at the Rochester Institute of Technology and technical marketing engineer with EMA (ema-eda.com).

Design for Sourcing WEBINAR

In today's volatile supply chain environment, the responsibility of sourcing transcends beyond purchasing and supplier management. It is imperative for engineers to integrate supply chain resilience into the very fabric of their designs.

This two-hour workshop will empower engineers with the knowledge and tools necessary to proactively design out supply chain risks during component selection.

Attendees will learn about the current landscape of supply chain vulnerabilities, the principles of Design for Sourcing, and practical strategies to ensure continuity and reliability in their electronic designs. By the end of this session, participants will be equipped to make informed decisions that safeguard their projects against disruptions and contribute to a more robust supply chain ecosystem.

Webinar led by
Ed Dodd

Ed Dodd is vice president, government and defense for Cofactr, a leading procurement automation company that is fusing supply chain assurance with procurement automation. Previously, he was director of US Army Programs at Ansys, where he advocated for physics-based digital thread and automated analysis from part to mission, and DfR Solutions, where he consulted across automotive and aerospace industries on various electronics reliability challenges.

Key Points to be Covered

- Importance of design for sourcing in today's environment
- Current trends and challenges
- Case studies of supply chain disruptions
- Criteria for component selection
- Innovations in supply chain management

What You Will Learn

- Role of engineers in sourcing decisions
- Assessing supplier reliability and stability
- Tools and techniques for risk assessment
- How to enhance cross-functional collaboration with between engineering and supply managers

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Adding Prudence to Our Appetite for Progress Can Deliver Innovation that Benefits All

From x-ray hype to AI black boxes, progress works best when curiosity is paired with caution.

THROUGHOUT HISTORY, OUR enthusiasm for new technology has often outpaced our ability to fully comprehend its risks. From the industrial revolution to the digital age, we have repeatedly embraced innovations with excitement while ignoring caution, sometimes overlooking potential hazards in our eagerness to advance. In healthcare, where technological breakthroughs promise transformative benefits, new capabilities can come with severe risks that demand careful scrutiny.

The early 20th century witnessed widespread adoption of radioactivity in consumer products and medical devices, long before its dangers were understood. Luminous watch faces and the health problems experienced by workers painting the dials by hand provide an example. Similarly, x-rays, discovered in 1895, quickly became a marvel for clinicians and the public alike. However, the excitement led to routine, unshielded exposure for patients and practitioners, resulting in severe health consequences for both groups.

The shoe-fitting fluoroscope is a striking example. A popular feature in shoe stores in the US and Europe from the 1920s, these devices used x-rays to reveal how shoes fit on children's feet. There were various brands – the Foot-O-Scope, or the British-made Pedoscope – often housed in nothing more substantial than a wooden enclosure. Marketed as a modern convenience, they were later recognized as hazardous, earning a place among *Time Magazine*'s "Worst Ideas of the 20th Century." Its popularity persisted for decades, despite the radiation risks posed to all in the vicinity. Clearly, concern began to mount as investigations from the late 1940s documented dosages both within the machine and at various distances above and around it. The results are startling, noting accumulated doses of up to 140mSv to the foot during a 20-second exposure. That's about six times today's typical annual occupational exposure limits for radiographers, clinicians and industry workers.

Despite such purely novel applications, the evolution of x-ray systems has delivered extremely valuable benefits across industries as well as in the medical field. As the dangers of radioactivity became clear, the medical community began to recognize and mitigate the risks associated with imaging technologies, prioritizing safety alongside innovation. Protective measures, such as lead shielding and regulated exposure times, were introduced to safeguard both patients and healthcare workers.

As other imaging modalities have emerged, such as computed tomography (CT), magnetic resonance imaging (MRI) and positron emission tomography (PET) using injected radioactive tracers, development has continued to reduce

doses while simultaneously improving image quality. Ongoing innovation in x-ray equipment has included improvements in source and beam control to reduce scattering and to sharpen focusing and steering. In this way, ensuring that more of the beam's energy reaches the target tissue reduces the transmitted energy. It shows how risk-aware innovation can realize the benefits of technological progress without compromising safety. We have also seen digital detectors replace traditional chemically based film, which converts only a small fraction of incoming x-ray photons into a usable image. These are more efficient, with better low-dose performance, lower noise and greater dynamic range, producing not only high-quality images from reduced dosages but also reducing retakes.

There's a democratizing benefit here as well, as these advancements have enabled equipment to become smaller and more lightweight, and more affordable to acquire and operate, due to reduced shielding, lower transmitter power, and reduced reliance on photographic plates and film, which are consumable and inconvenient. It's making high-quality healthcare more accessible to more people. Today, over 2 million scans are performed every day in the US alone, including some 1.5 million x-rays and 250,000 CT scans.

Right now, AI is arguably the most influential technology transforming medical imaging. Deep learning models are also driving further dose minimization by enabling high-quality image reconstruction from lower radiation exposures. These innovations improve both patient outcomes and operational efficiency, demonstrating the positive potential of technology when thoughtfully applied.

It's also helping to increase the speed and efficiency with which healthcare services are delivered. Using AI algorithms to assist in triage is already an established practice, reducing clinicians' fatigue and helping identify urgent cases more rapidly. By automating routine tasks and flagging anomalies, AI reduces the likelihood of human error and streamlines diagnostic workflows.

As the world's population grows and ages, demanding more medical assistance, capturing these benefits is imperative. On the other hand, the rise of AI brings new challenges, such as the "black box" problem. This is a key concern as algorithms grow more complex and their decision-making processes become increasingly opaque, even to expert users. This lack of transparency raises concerns about accountability, trust, and the potential for unintended consequences in diagnostics.

Healthcare professionals must grapple with the reality that, while AI can outperform humans in certain tasks, our understanding of how these systems arrive at conclusions could become increasingly limited. We need to address this issue if we are to continue directing and driving innovation. Ongoing collaboration among technologists, clinicians and ethicists is vital to ensure that AI remains a tool for empowerment, not confusion.

I often talk about lessons from history, and there's an important one here. Technological progress comes with risks, and we must balance our excitement with a commitment to identify these as early as possible and prioritize mitigation. It's easier said than done, as we are dealing with many unknowns as we try to move forward. Could early scientists have understood the health risks from radiation with little to no data – anecdotal or empirical? Today, as we contemplate the risks posed by AI, opinions are polarized, although a consensus has not been established.

In medical technology, and beyond, responsible innovation that benefits us all lies not in unchecked adoption, but in

thoughtful advancement. By recognizing past missteps and proactively addressing emerging challenges, we can harness the power of new technologies to serve humanity's best interests.

ALUN MORGAN is technology ambassador at Ventec International Group (venteclaminates.com); alun.morgan@ventec-europe.com. He is presenting at the PCEA PCB Management Symposium, "Strategic Leadership in the Age of AI, New Technology Adoption, and Talent Scarcity," taking place April 28 at PCB East. His column runs monthly.

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The PCB Podcast

DATA TRANSFER

What Are You Waiting For? Move to IPC-2581 and Leave the Chaos Behind

IPC-2581 replaces fragmented PCB data handoffs with a single intelligent file.

FOR DECADES, THE electronics industry has accepted a painful reality: design data handoffs are messy, incomplete and almost always require follow-up emails, spreadsheets and PowerPoints to clarify intent. We've normalized inefficiency.

But here's the real question: Why are we still working this way in an AI-driven world?

There is a smarter path forward – and it's called the IPC-2581 standard. And the IPC-2581 Consortium is here to assist in your migration process.

IPC-2581 is not just another file format. It is:

- The only open and neutral standard on the market
- An AI-ready PCB data standard
- A complete machine-readable digital product model
- A single-file solution that eliminates fragmented packages.

Everything needed to fabricate, assemble and test a PCB can exist in one intelligent XML file **(Figure 1)**. No reverse engineering. No guessing. No reconstructing intent. Just build-ready data.

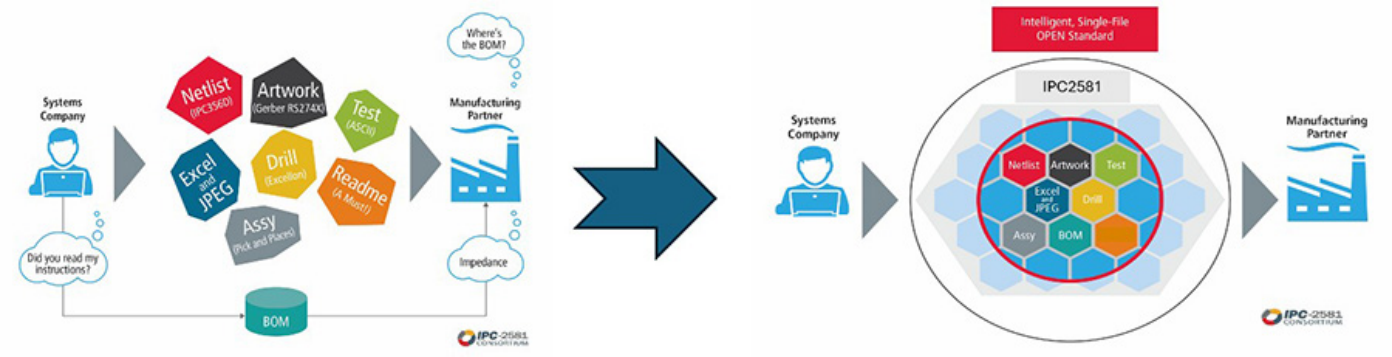


Figure 1. From reverse engineering and email chaos to an intelligent digital product model.

Why IPC-2581 Makes Sense Today

1. **Complete machine-readable data.** IPC-2581 includes fabrication, assembly, test, stackup, impedance, drawings, dimensions – everything – in a structured format tools can interpret automatically **(Figure 2)**.

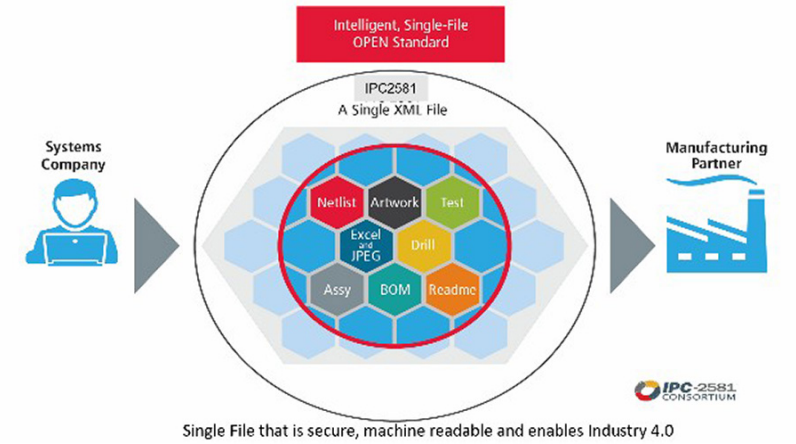
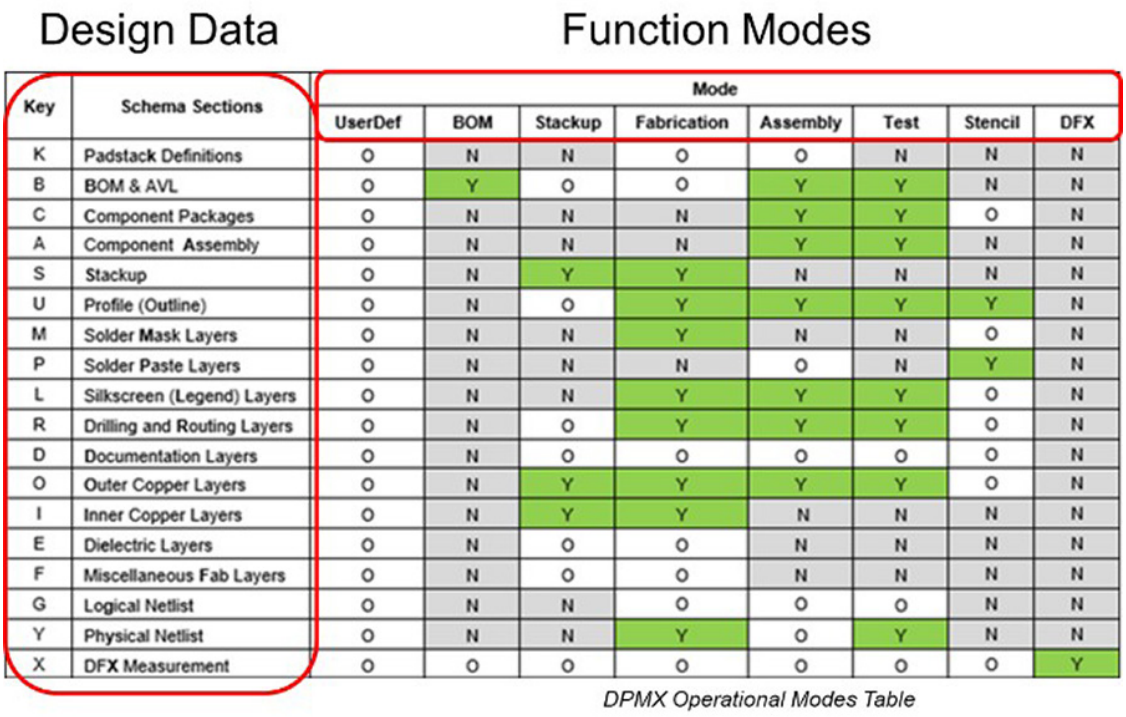


Figure 2. IPC-2581 consolidates netlist, drill, BOM, test and documentation data into a single XML file.

This is critical in an AI era. AI agents cannot efficiently process fragmented, partially reconstructed data. Even if the AI agent could reconstruct it, can you depend on it? IPC-2581 gives AI what it needs: clean, structured intelligence. Some companies are using AI tools to analyze the data (DfM, etc.) before sending it to their manufacturing partners. Others use IPC-2581 to send design data to analysis tools to ensure the circuit will work as intended. Wouldn't you want to build what you simulated/tested?

2. **Single file with zero confusion.** Alternative formats still rely on multiple files and definitions. IPC-2581 consolidates everything into one file, which means simpler data management, easier archiving, cleaner PLM integration and no missing attachments.

3. **IP protection through function modes.** One of IPC-2581's most powerful capabilities is Function Modes **(Figure 3)**. It outputs fabrication-only package, assembly-only package, stencil-only package, and more. Many software vendors support additional function modes, and some allow creation of a user-defined mode that includes or excludes data of your choice. (Read more about it here.) Manufacturers receive only what they need – nothing more. This protects intellectual property while enabling precise manufacturing collaboration.



Key	Schema Sections	Mode							
		UserDef	BOM	Stackup	Fabrication	Assembly	Test	Stencil	DFX
K	Padstack Definitions	O	N	N	O	O	N	N	N
B	BOM & AVL	O	Y	O	O	Y	Y	N	N
C	Component Packages	O	N	N	N	Y	Y	O	N
A	Component Assembly	O	N	N	N	Y	Y	N	N
S	Stackup	O	N	Y	Y	N	N	N	N
U	Profile (Outline)	O	N	O	Y	Y	Y	Y	N
M	Solder Mask Layers	O	N	N	Y	N	N	O	N
P	Solder Paste Layers	O	N	N	N	O	N	Y	N
L	Silkscreen (Legend) Layers	O	N	N	Y	Y	Y	O	N
R	Drilling and Routing Layers	O	N	O	Y	Y	Y	O	N
D	Documentation Layers	O	N	O	O	O	O	O	N
O	Outer Copper Layers	O	N	Y	Y	Y	Y	O	N
I	Inner Copper Layers	O	N	Y	Y	N	N	N	N
E	Dielectric Layers	O	N	O	O	N	N	N	N
F	Miscellaneous Fab Layers	O	N	O	O	N	N	N	N
G	Logical Netlist	O	N	N	O	O	O	N	N
Y	Physical Netlist	O	N	N	Y	O	Y	N	N
X	DFX Measurement	O	O	O	O	O	O	O	Y

DPMX Operational Modes Table

Figure 3. IPC-2581 Function Modes enable controlled data exchange by tailoring fabrication, assembly, test, stencil and DfX outputs.

4. **True bidirectional exchange.** This is where IPC-2581 truly stands apart. With its DfX module and stackup exchange, feedback becomes electronic and structured – not ePaper (spreadsheets, PowerPoint, emails, etc.). IPC-2581 is the only true bidirectional standard, sidestepping the drawbacks of traditional one-way handoffs. IPC-2581C introduced the DfX module, which permits electronic exchange of DfM data and TQs. This module can either accompany the complete set of design data or be distributed on its own, in a manner similar to stackup information.

The latest IPC-2581 release (version 4.0) enhances the DfX module capabilities, thanks to feedback from IPC2581 Consortium and IPC 2-16 committee members. By adopting the DfX Module, designers and manufacturers can finally eliminate ePaper – no more emails, Word docs or PowerPoint slides – saving time and reducing errors **(Figure 4)**. Better, the contextual data exchanged can be analyzed by AI agents to recommend process improvements and minimize unnecessary iterations. Design teams can compare changes across sources, while manufacturers can pinpoint which customers consume the most time, and incentivize better collaboration. This streamlined process accelerates new product introduction and creates a genuine win-win for everyone involved.

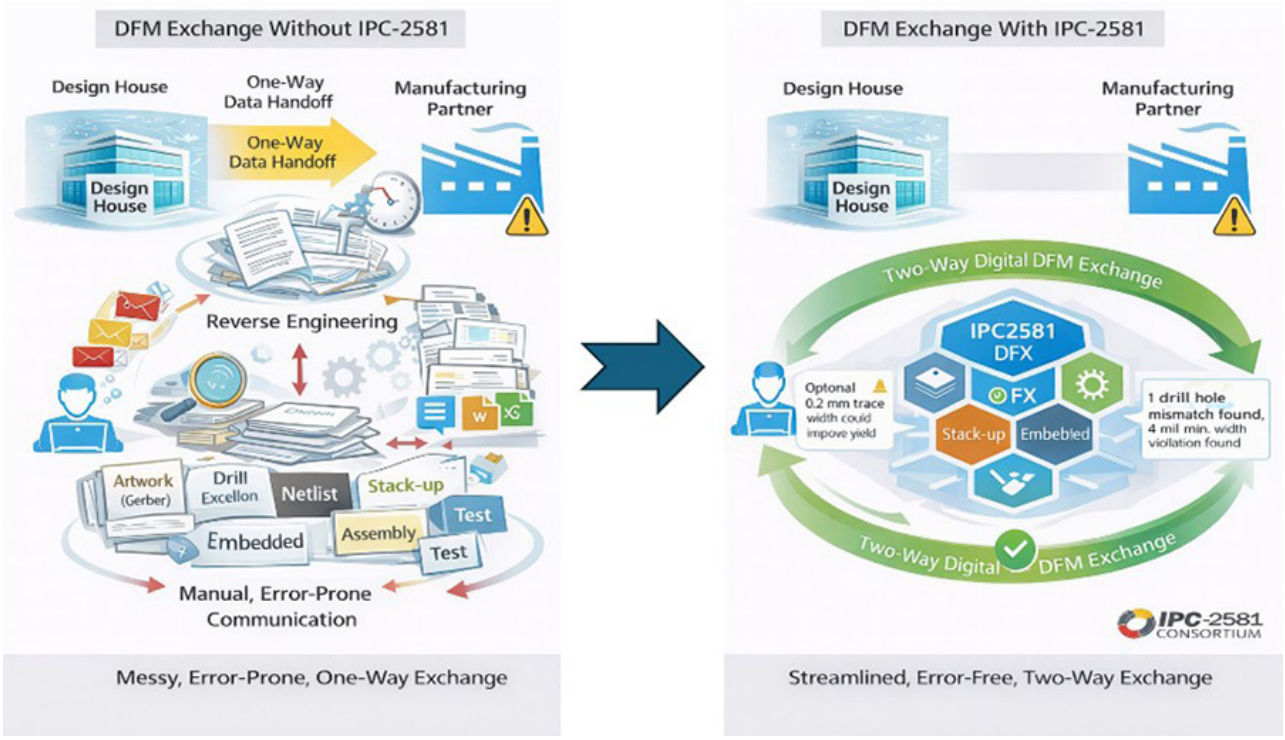


Figure 4. IPC-2581 replaces fragmented, one-way DfM handoffs with a structured two-way digital exchange.

For DfM/TQs, design and manufacturing tools can:

- Send technical queries electronically
- Link issues directly to coordinates and objects
- Track approvals and rejections
- Store approved DfM inside the design file

For stackup exchange, design and manufacturing tools can send stackup data that are electronically read in, eliminating manual stackup data entry on the design side. Manufacturers can send exact material information to the design, which can then perform an accurate simulation for high-speed signals.

No more manual correlation work. No more spreadsheets. No more error-prone back-and-forth. Free PCB designers and manufacturing engineers to do real work.

Real Industry Support

IPC-2581 is supported by all major EDA vendors (Altium, Cadence, KiCad, Pulsonix, Siemens and Zuken, among others). On the manufacturing side, companies using software from these companies can seamlessly read IPC-2581:

- Frontline /KLA Tencor (Genesis 2000, InCAM, InSight PCB)
- Downstream/Siemens (CAM350)

- Aegis Software (FactoryLogix, CircuitCAM)
- Wise Software (VisualCAM, Wise2581 Viewer)
- Siemens (TestExpert, UniCAM FX, UniDoc FX)
- Vayo (VayoPro – DfM, SMT, Test Expert)
- A complete list of software companies that support IPC-2581 is available.

The IPC-2581 Consortium (ipc2581.com) was formed in 2011 with 12 founding members. Today, it has grown to over 141 members, including:

- OEMs such as Apple, Intel, Cisco, NVIDIA, Amazon, Ericsson
- Fabricators
- Contract manufacturers
- EDA and CAM suppliers
- PLM and analysis software providers.

The support matrix on ipc2581.com is updated based on information received from manufacturers or their customers reporting support for IPC-2581. Many more companies support IPC-2581 than are listed in the matrix. Contact your manufacturer and ask them to support your desire to move to IPC-2581. Often, the consortium has found that the manufacturers' sales and marketing teams may not know whether the factory supports IPC-2581. Visit ipc2581.com to see the growing support matrix.

Who Is Actually Using It?

This is not theoretical.

During one of the IPC-2581 Adoption Summits, one fabricator reported more than 2,300 boards were built using IPC-2581 as input since 2018. This remarkable figure demonstrates the growing acceptance of the standard while underscoring the reliability and effectiveness of the IPC-2581 standard in high-volume manufacturing environments.

Aegis Software, which provides MES software for manufacturing companies, further emphasized this trend, sharing that 33 companies, including large multinational contract manufacturers and smaller enterprises, have successfully integrated IPC-2581 into their workflows. These numbers highlight the growing recognition of IPC-2581 as a standard that meets the needs of manufacturers of all sizes.

Axiom Electronics noted that IPC-2581 is its preferred format and has been helpful in streamlining its paper-free factory process. A significant number of its customers have been providing IPC-2581 as input for building boards for many years now.

Cisco standardized on IPC-2581 last year and now requires all suppliers to support it for fabrication and assembly. They migrated from Gerber-based packages to an intelligent, open standard IPC-2581 file for design data exchange. IP Protection was their number #1 reason to move to IPC-2581. Having bi-directional stackup exchange and electronic DfM/TQ exchanges improves efficiency. IPC-2581 is also AI-ready compared to any other package available today. "We made a strategic decision to protect our intellectual property and eliminate inefficiencies in our supplier interactions by transitioning from Gerber-based handoffs to IPC-2581 bidirectional data exchange," said Terry Hoffman, senior technical leader, Cisco. "IPC-2581 provides a single, intelligent, and consistent digital product model – everything our suppliers need to build, assemble and test our PCBs. It removed the ambiguity, eliminated multiple disconnected files and replaced guesswork with precision."

Apple joined the IPC-2581 Consortium last year and drove several enhancements to the standard's latest version – Version 4.0 (new naming convention). It felt it could influence and drive the standard to meet its needs.

Intel joined the IPC-2581 Consortium a month ago and is actively participating in the consortium meetings to drive the standard. Its reason for joining: "Intel believes in open, vendor-neutral industry standards and would like to drive the standard for automated AI-enabled board design workflows and data exchange that will accelerate innovation in electronics design and manufacturing."

Dana Korf, senior technical director at Victory Giant (VGT), summarized it best: "In reality, most traditional data packages are not manufacturing-ready when they arrive. IPC-2581 dramatically changes that – eliminating conflicting documentation, data and netlist errors which significantly reduces NPI cycle times."

That says it all.

Why This Matters Now

We talk about:

- Digital transformation
- Smart factories
- AI-driven DfM
- Secure data exchange
- Faster NPI.

None of this scales on top of fragmented, reverse-engineered, one-way handoffs.

IPC-2581 enables:

- AI-ready data
- Secure IP exchange

- True bidirectional collaboration
- Reduced errors
- Faster product introduction
- Paperless manufacturing.

This is not just about file format. It is about transforming how our industry works.

If the industry already supports it … if OEMs are standardizing on it … if it reduces errors, protects IP and accelerates NPI … what are you waiting for?

Move to IPC-2581 and leave chaos behind. Reach out to the IPC-2581 Consortium (info@ipc2581.com) with questions or for assistance on using or migrating to the IPC-2581 format.

HEMANT SHAH is an EDA veteran and chair of the IPC-2581 Consortium (ipc2581.com). Shah led the effort to create an industry-wide consortium of design and supply chain companies to get IPC-2581 – the standard for transferring PCB design data to manufacturing – adopted.

He spent 20 years at Cadence as product manager for various PCB design products. Shah also led the industry adoption of the IBIS-AMI algorithmic modeling standard. Prior to joining Cadence, Shah worked at Xynetix and Intergraph. He is passionate about developing and marketing leading-edge software products for PCB design.

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THERMAL MANAGEMENT

Experimental Evaluation of High-Thermal Dielectric Materials and Surface-Mount Thermal Bridges in Multilayer PCB Designs

A study shows how high-thermal dielectrics outperform FR-4 for bulk heat spreading, with surface-mount thermal bridges serving as targeted tools for hotspot control.

by CHRIS PARKER, MARTIN ANSLEM, PH.D., and FRANCISCO AGUILAR

As power density continues to increase across power electronics, industrial controls, automotive electrification and data center infrastructure, printed circuit boards (PCBs) are increasingly required to function as active thermal management structures rather than passive interconnect platforms. Localized hotspots, rising junction temperatures and constrained form factors are pushing conventional FR-4 substrates beyond their practical thermal limits. In response, PCB designers are adopting a combination of material-level improvements within the PCB stackup and localized heat-spreading solutions. One such approach is the use of surface-mount thermal bridges (SMTBs), passive SMT components designed to conduct heat away from power devices and redistribute it into larger copper regions of the PCB without providing an electrical function.

This study presents a controlled experimental comparison between standard FR-4 and an advanced high-thermal dielectric PCB material, evaluated both with and without SMTBs. Identical six-layer test vehicles were designed, fabricated and assembled, and then tested under repeatable power-cycling conditions at Rochester Institute of Technology (RIT). Thermal performance was quantified using infrared (IR) thermography, with validation through thermocouple measurements. Multiple experimental iterations were conducted to examine the effects of substrate material, SMTB presence, SMTB size and overall board temperature on thermal behavior.

Results show that boards fabricated with the advanced thermal dielectric consistently operated at lower temperatures than FR-4 across all quadrants and test configurations. SMTBs provided measurable reductions in peak component temperature on both substrates; however, their relative impact diminished on the higher-performance dielectric, indicating that bulk heat spreading through the PCB material becomes the dominant thermal pathway as substrate conductivity improves. These findings support the use of advanced thermal dielectric materials as drop-in replacements for FR-4 in high-power designs and position SMTBs as a complementary, fine-tuning thermal solution for managing localized hotspots.

Thermal Challenges in High-Power Designs

Electronic systems are undergoing a sustained increase in power density driven by electrification, automation and high-performance computing. Power conversion stages, motor drives, battery management systems and AI accelerators now concentrate significant heat generation into increasingly compact footprints. In many of these systems, the PCB itself is required to dissipate a substantial portion of this heat, particularly when airflow is limited or mechanical heat sinking is constrained.

Traditional PCB thermal management strategies, such as increasing copper weight, adding thermal vias or attaching external heat sinks, are often insufficient to address localized hotspots at the component level. These approaches may reduce average board temperature but frequently fail to prevent excessive junction temperatures in high-power surface-mount devices. As a result, designers are increasingly exploring material-level solutions within the PCB stackup.

Surface-mount thermal bridges (SMTBs) are passive SMT components used to reduce localized hotspot temperatures in surface-mount power devices. They are mounted on the PCB using standard assembly processes and serve no electrical function. Instead, SMTBs create a low thermal resistance path that conducts heat away from a hot component and distributes it to larger copper areas of the board, thereby increasing the effective heat-spreading area.

During operation, heat flows from the component pad into the SMTB and is redistributed into connected copper planes, thermal vias or other heat-spreading features within the PCB stackup. This reduces thermal bottlenecks at the component interface and lowers peak device temperatures. Because SMTBs rely on conduction rather than airflow, they are well-suited for compact, enclosed or passively cooled systems.

The effectiveness of an SMTB depends strongly on the thermal performance of the PCB material. On conventional FR-4, SMTBs can provide meaningful temperature reductions by compensating for limited heat spreading in the dielectric. As part of a thermal design strategy, SMTBs are most effective when used as a complementary solution alongside appropriate substrate selection and PCB layout optimization.

Substrates Comparison

FR-4 remains the dominant PCB substrate due to its balance of cost, electrical performance, mechanical stability and compatibility with standard fabrication and assembly processes. However, FR-4 has a relatively low thermal conductivity, typically on the order of 0.3–0.4 W/m·K, which limits its ability to spread heat both laterally within copper layers and vertically through the board thickness. As component power density increases, this limitation results in steep local temperature gradients, elevated junction temperatures and reduced thermal margin at the device level. In high-power surface-mount applications, these effects can accelerate failure mechanisms such as solder joint fatigue, dielectric aging and reduced semiconductor lifetime.

High-thermal-dielectric materials such as the novel SFL-12, with a through-plane thermal conductivity of approximately 12W/m·K, provide a substantial improvement in bulk heat dissipation compared with standard FR-4. In the RIT study, identical six-layer test vehicles fabricated with SFL-12 consistently operated at significantly lower temperatures than their FR-4 counterparts under the same power-cycling conditions.

From a design perspective, these quantitative differences translate directly into increased thermal headroom and improved reliability margins. A 26°C reduction in peak temperature can significantly extend component lifetime and enable higher allowable power dissipation within the same board footprint. By improving heat transfer through the PCB stackup rather than relying solely on copper geometry or localized thermal features, high-thermal dielectrics can reduce thermal bottlenecks at the material level.

Advanced high-thermal-dielectric materials are engineered to enhance heat transfer without compromising electrical isolation or mechanical stability. When combined with localized heat-spreading elements such as surface-mount thermal bridges, these materials offer a hybrid approach that addresses both bulk heat spreading and hotspot mitigation.

Thermal Physics of Heat Dissipation

Heat dissipation in multilayer printed circuit boards is governed by the balance between in-plane heat spreading within copper layers and through-plane heat conduction across dielectric layers. While copper planes provide very high in-plane thermal conductivity, their ability to remove heat from a surface-mounted power device is limited by the efficiency with which heat can conduct vertically through the dielectric into those planes. In conventional FR-4 constructions, the low dielectric thermal conductivity creates a dominant thermal resistance in the heat-flow path, causing heat to remain concentrated near the component and resulting in elevated junction and case temperatures. Once this dielectric bottleneck is reached, further increases in copper weight or plane area offer diminishing thermal benefit.

The measured 26°C reduction in peak component temperature observed in quadrant 1 directly reflects the impact of improving this through-plane thermal path. By replacing FR-4 (≈0.3–0.4W/m·K) with a high-thermal dielectric material (≈12W/m·K), the dominant thermal resistance in the stackup is substantially reduced, permitting heat to flow more efficiently away from the component and into internal copper layers and surrounding board structures. From a thermal physics standpoint, this shifts the heat-transfer regime from localized conduction near the component interface to bulk heat spreading through the PCB, resulting in lower peak temperatures even in the absence of additional localized thermal features such as surface-mount thermal bridges.

This same mechanism explains why the relative benefit of surface-mount thermal bridges diminishes on high-thermal dielectric substrates. On FR-4, SMTBs provide an alternate conduction path that partially compensates for poor dielectric heat transfer and produces measurable temperature reductions. However, once the dielectric itself enables efficient vertical heat flow, as evidenced by a 26°C reduction in baseline temperature, the PCB stackup becomes the primary heat-spreading element. In this regime, SMTBs contribute only incremental improvements by fine-tuning local heat distribution rather than overcoming a fundamental material limitation **(Figure 1)**. These results reinforce a substrate-first thermal design approach, where improvements in dielectric thermal conductivity yield the largest temperature reductions, and localized thermal solutions serve as secondary optimization tools.

Figure 1. Quadrant 1 of FR-4 with no SMTBs.

Study Objectives

The primary objective of this study was to experimentally validate the thermal performance improvements achieved by using a high-thermal-dielectric prepreg laminate stackup compared with a standard FR-4 baseline. The study was designed to quantify the effect of enhanced dielectric thermal conductivity on heat dissipation within a multilayer PCB under controlled operating conditions. In addition, the work aimed to evaluate the effectiveness of SMTBs as a localized thermal management strategy when combined with high-thermal-conductivity dielectric materials.

To achieve these objectives, the study focused on the following specific goals:

- Quantitatively compare the steady-state and transient thermal behavior of electrically and mechanically identical FR-4 and high-thermal prepreg test boards
- Evaluate the temperature reduction achieved through use of SMTBs on both standard and high-thermal dielectric substrates
- Assess the influence of SMTB size and placement on peak component temperature.

Experimental test vehicle design. Two electrically identical six-layer PCBs were fabricated for this study: one using standard FR-4 materials and the other using a high-thermal-dielectric prepreg laminate **(Figure 2)**. The boards

were designed with the same layer count, copper weights and finished thickness in order to isolate the impact of dielectric thermal performance on overall heat dissipation.

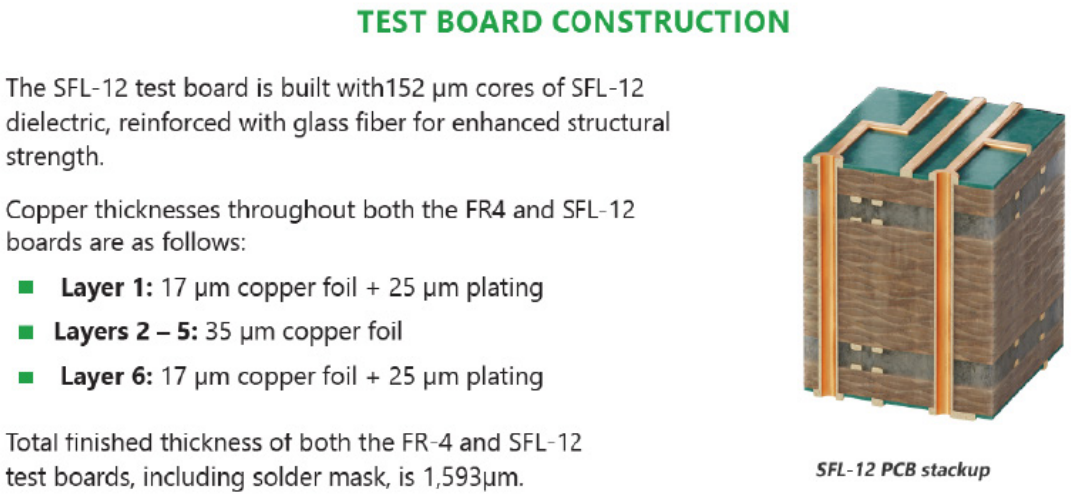

Figure 2. Test board construction and SFL-12 PCB stackup.

Each board incorporated 152µm dielectric core layers reinforced with glass fiber, resulting in a total finished thickness of approximately 1.6mm, including solder mask. Copper thicknesses were held constant across both material sets, with plated outer layers and uniform copper distribution on the internal layers, ensuring that any observed thermal performance differences could be attributed primarily to the dielectric and prepreg materials rather than variations in copper geometry or board construction.

The test vehicles were designed using established PCB thermal management techniques, including heavy copper layers and strategically placed thermal vias, to promote efficient heat dissipation. Component placement within each quadrant was intentionally arranged to create localized thermal hotspots while preserving symmetry across the board.

This symmetrical layout ensured consistent thermal boundary conditions across all quadrants, enabling direct and repeatable comparison of thermal performance between different dielectric materials and test configurations without introducing layout-driven bias.

Surface-mount thermal bridge configurations. Three SMTB designs were evaluated, representing a range of thermal resistances and package constructions. These bridges were mounted adjacent to the power devices and connected to dedicated copper planes intended to spread heat laterally and through the board thickness.

Different experimental phases evaluated boards with no thermal bridges, one thermal bridge per quadrant, and two thermal bridges per quadrant to study scaling effects.

Test environment and fixture design. All testing was conducted at RIT using a custom fixture designed to ensure repeatable positioning, airflow isolation and consistent infrared thermal imaging. A fixed gap was maintained

between the PCB and IR camera to minimize measurement variability. Ambient temperature was monitored throughout testing and remained stable across all trials.

Each test followed a standardized 20-minute cycle consisting of a 14-minute powered-heating phase, followed by a 6-minute unpowered cooldown phase. This protocol enabled evaluation of both transient heating behavior and near-steady-state conditions. Multiple trials were conducted for each quadrant and configuration to establish repeatability.

Thermal data were captured using a calibrated FLIR infrared camera, with images recorded at 30-second intervals throughout each test cycle **(Figure 3)**. Component temperatures were extracted from the infrared images and plotted as a function of time to evaluate both transient and steady-state thermal behavior.

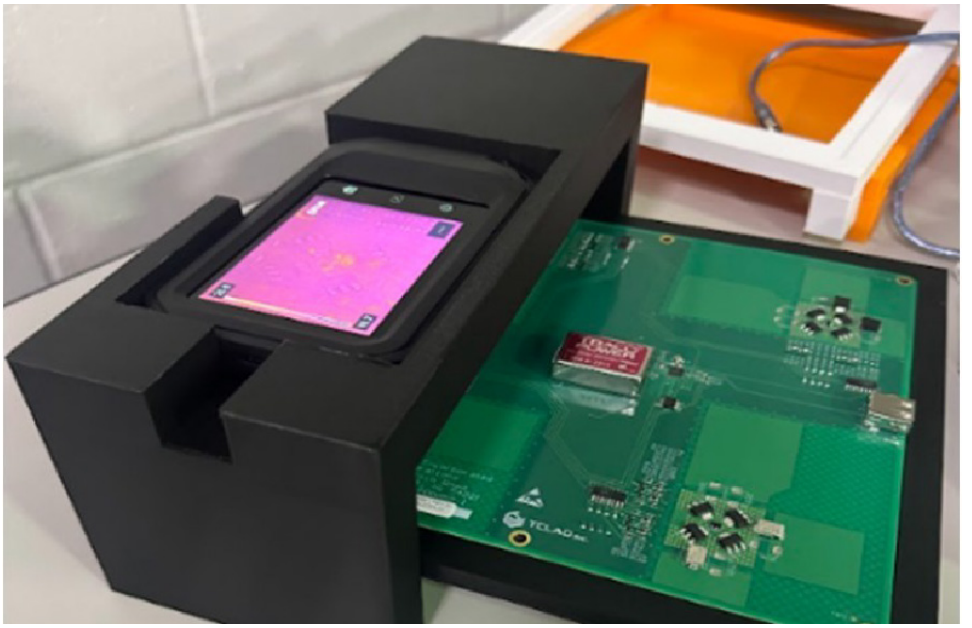

Figure 3. Design test fixture with FLIR mounted above test board.

To validate the infrared measurements, a subset of experiments incorporated K-type thermocouples attached directly to selected transistors. Thermocouple data were logged simultaneously with IR imaging, enabling direct comparison of the measurement methods and the identification of systematic offsets, while confirming overall thermal trends.

Infrared measurements consistently reported slightly higher absolute temperatures than thermocouples. Relative trends between materials and configurations remained consistent across both measurement techniques, however.

To instill confidence in the experimental results, thermal measurements were obtained using both infrared (IR) thermography and direct-contact thermocouples, allowing cross-validation of the observed temperature trends. The FLIR infrared camera provided noncontact, spatially resolved temperature data across the test vehicles, enabling consistent identification of peak component temperatures during both transient heating and near-steady-state conditions **(Figures 4** and **5)**. To verify the accuracy of these measurements, K-type thermocouples were attached directly to selected power transistors and logged simultaneously with IR data under identical power-cycling conditions. This dual-measurement approach ensured that observed temperature differences between materials and test configurations were not artifacts of a single measurement technique.

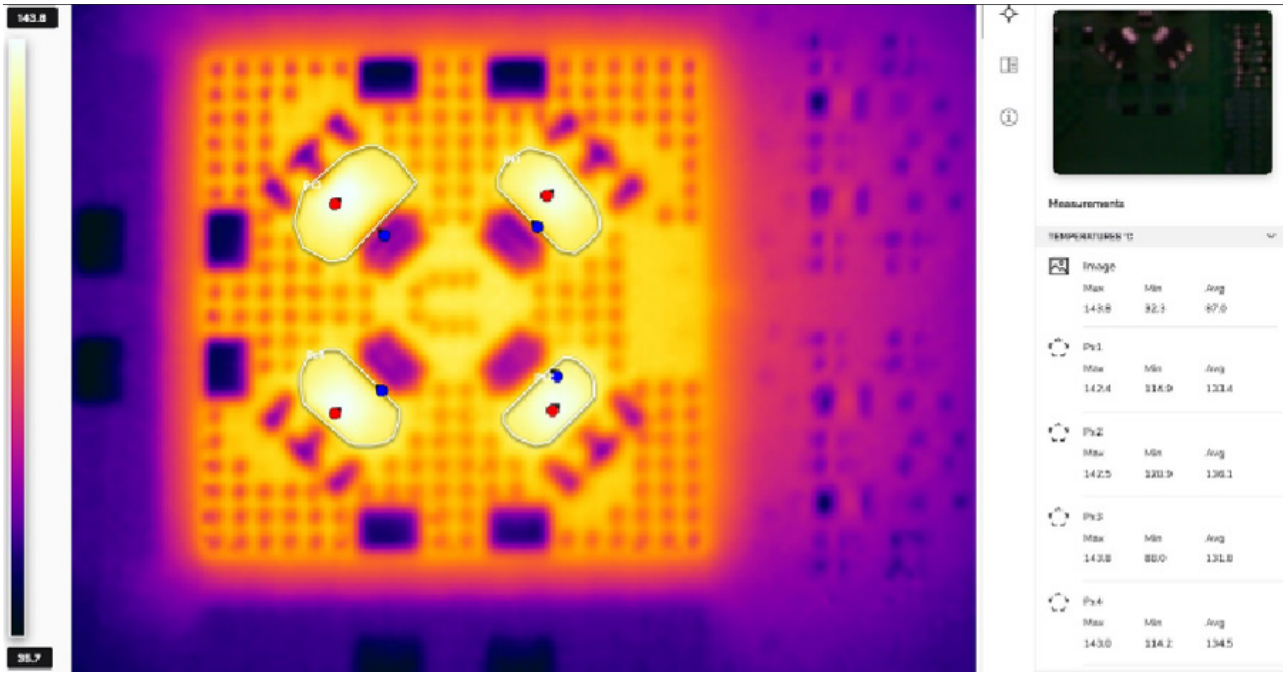

Figure 4. FR-4 FLIR test results.

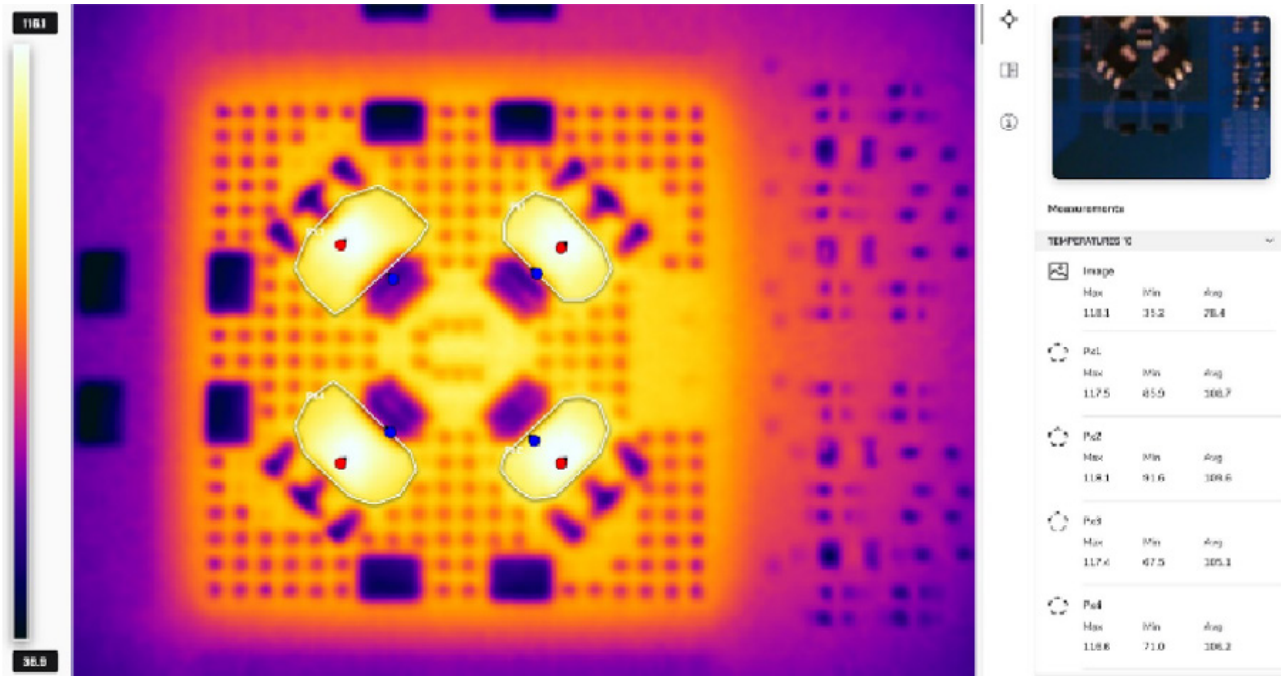

Figure 5. SFL-12 FLIR test results.

Across all validation trials, the average temperature difference between the IR camera and thermocouple measurements was approximately 4°C, with the IR camera consistently reporting temperatures 2°–5°C higher than the thermocouples. This systematic offset is consistent with known differences between non-contact IR measurements and direct-contact sensors and is commonly attributed to factors such as assumptions about surface emissivity, sensor contact resistance and localized heat spreading at the measurement point. Importantly, the magnitude of this offset remained stable across test runs and did not vary with substrate material or SMTB configuration.

Because the offset between measurement techniques was both small and consistent, the infrared thermography data is

considered reliable for comparative analysis of thermal performance. Relative temperature differences between FR-4 and high-thermal dielectric boards, as well as between SMTB configurations, were preserved across both measurement methods. As a result, the reported temperature reductions, particularly the 26°C baseline difference observed between substrates, are significantly larger than the measurement uncertainty and therefore represent true, material-driven thermal performance improvements rather than measurement artifacts **(Figure 6)**.

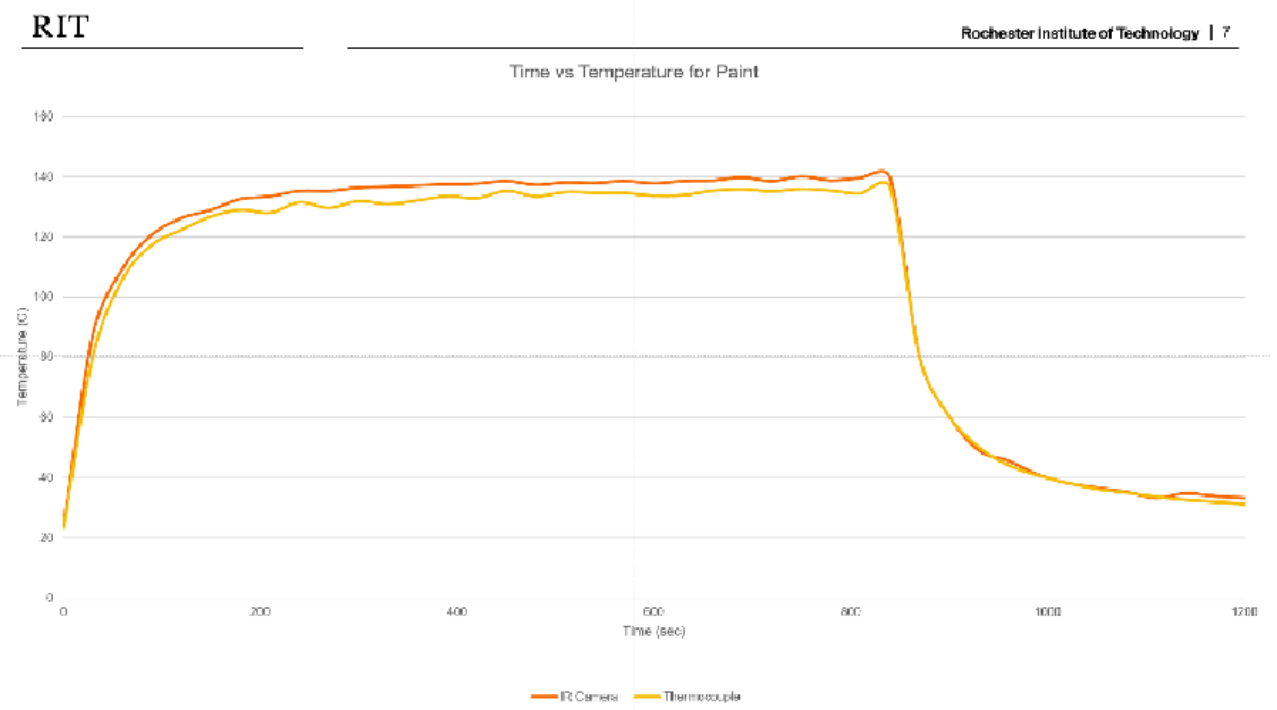

Figure 6. Time-temperature response under power cycling.

Results

Quadrant 1 results: Impact of advanced high-thermal dielectric materials. A direct comparison between FR-4 and the high-thermal dielectric material was performed in quadrant 1, where no surface-mount thermal bridges were present. Under identical operating conditions, infrared measurements showed a maximum component temperature of approximately 144°C on the FR-4 test board **(Figure 7)**, compared to approximately 118°C on the high-thermal dielectric test board **(Figure 8)**, resulting in a temperature reduction of 26°C.

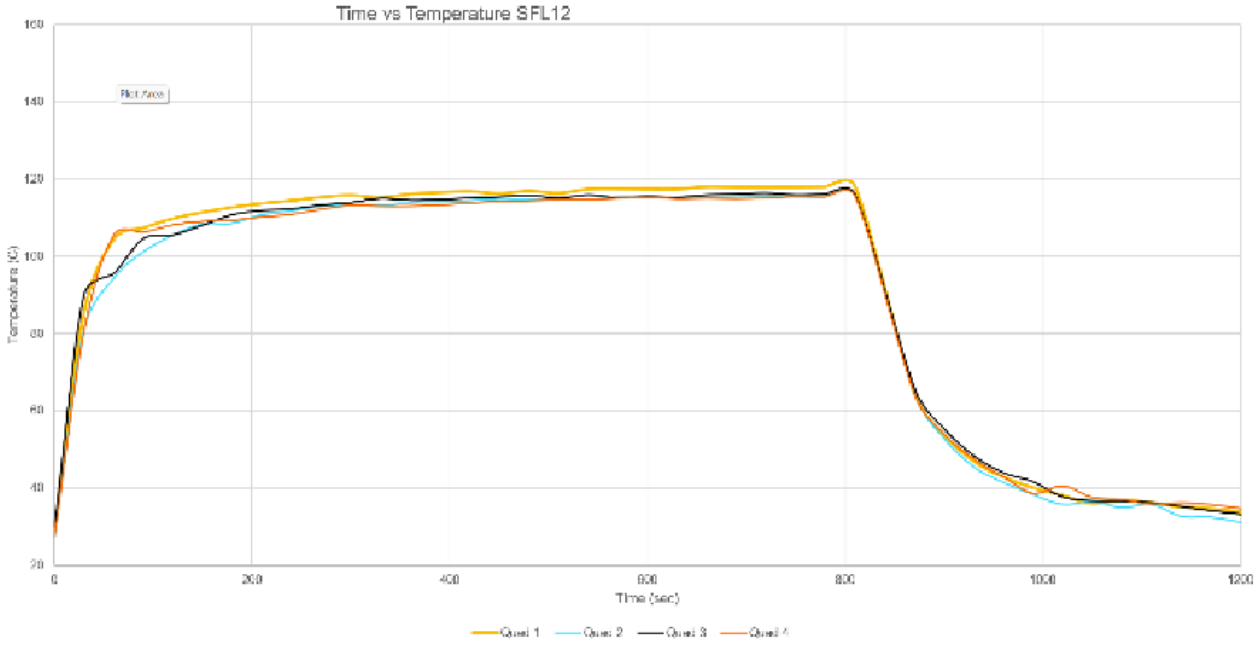

Figure 7. Time-temperature comparison across FR-4 test configurations.

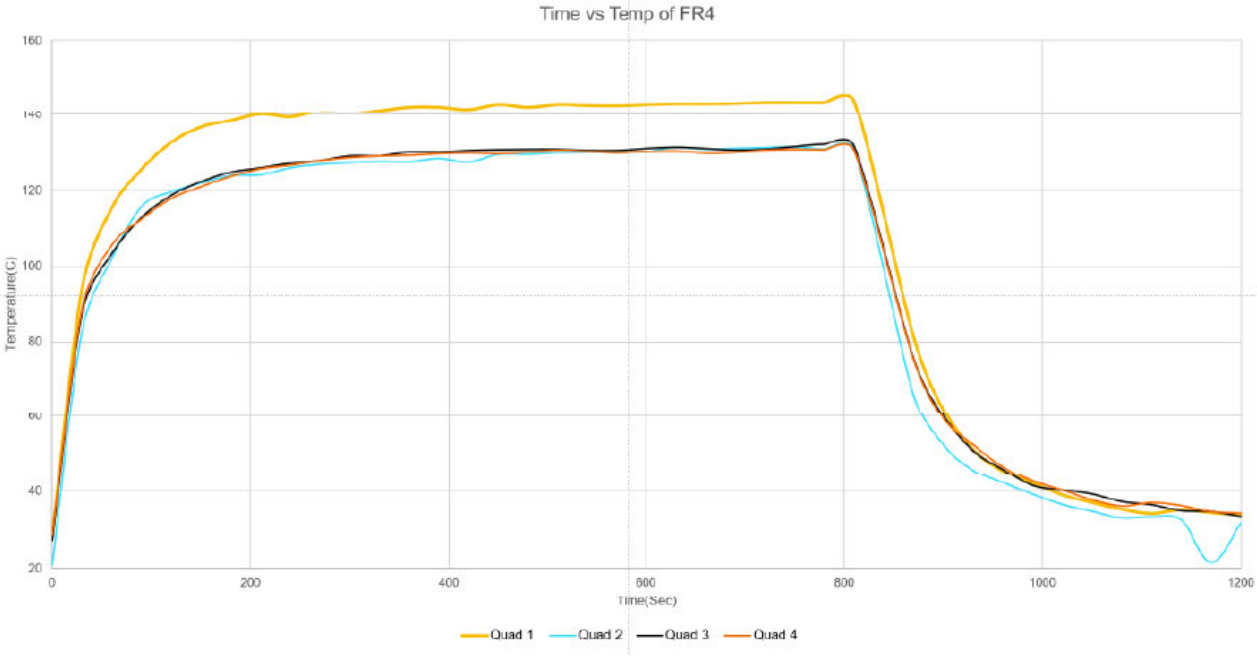

Figure 8. Time-temperature response for SFL-12 high-thermal dielectric test boards.

This result highlights the direct impact of increased dielectric thermal conductivity, approximately 12W/m·K, on heat dissipation at the component level. The significant reduction in peak temperature demonstrates that improved bulk heat spreading within the PCB stackup alone can substantially lower device operating temperatures, even in the absence of additional localized thermal management features.

Quadrants 2–4 results: impact of SMTBs. Results from quadrants 2 through 4, which incorporated surface-

mount thermal bridges, show a consistent reduction in peak component temperature on the FR-4 test boards compared to quadrant 1, where no SMTBs were present. Across the different SMTB sizes evaluated, the FR-4 boards exhibited similar thermal performance, with an average temperature reduction of approximately 14°C relative to the no-bridge condition. These results indicate that, within the tested power range, SMTB size had a limited influence on peak temperature reduction and that the presence of an SMTB itself was the dominant factor.

In this test configuration, two SMTBs were installed per quadrant. Additional experiments conducted with only one SMTB per quadrant showed a smaller temperature reduction of approximately 5°C. Based on these observations, it is reasonable to infer that each SMTB contributed roughly 5°C of peak temperature reduction on the FR-4 substrate. This finding suggests that SMTBs can be an effective localized thermal management strategy for FR-4-based designs operating near their thermal limits, where incremental reductions in component temperature can meaningfully improve design margin.

In contrast, the high-thermal dielectric test boards exhibited a significantly different response to the addition of SMTBs. Across quadrants 2 through 4, the average temperature reduction associated with SMTB use was approximately 2°C. This reduced impact indicates that bulk heat spreading provided by the high-thermal-dielectric material dominated the system's thermal behavior, diminishing the relative contribution of localized heat-spreading elements. These results demonstrate that, while SMTBs can provide measurable benefit on lower-conductivity substrates, their effectiveness is strongly dependent on the underlying dielectric material and becomes less pronounced as intrinsic PCB thermal performance improves.

Conclusion

This study demonstrates that material-level thermal performance within the PCB stackup plays a decisive role in managing heat in power-dense electronic designs. Under controlled, repeatable test conditions, six-layer PCBs fabricated with a high-thermal-dielectric material consistently operated at substantially lower temperatures than equivalent FR-4 boards.

In the baseline configuration without surface-mount thermal bridges, the high-thermal dielectric board exhibited a 26°C reduction in peak component temperature compared to FR-4 **(Table 1)**, clearly illustrating the impact of increased through-plane thermal conductivity on heat removal at the component level. This result confirms that improved bulk heat spreading within the PCB alone can significantly reduce junction and case temperatures without changes to copper geometry or board architecture.

Table 1. Key Measurements of Both Test Board Types at Various Locations

Key Measurements	FR-4	SFL-12
Peak Temperature Q1	144°C	118°C
Peak Temperature Q2-Q4	130°C	116°C
Delta Temperature with SMTBs	14°C	2°C
Delta Temperature between Substrates	26°C	26°C

The study further shows that surface-mount thermal bridges can provide meaningful localized temperature reductions on conventional FR-4 substrates. In quadrants 2 through 4, the addition of SMTBs reduced peak temperatures on FR-4 boards by 14°C when two bridges were used.

These findings indicate that SMTBs can be an effective mitigation strategy for FR-4-based designs operating near their thermal limits, where incremental reductions in component temperature can improve design margin and reliability. SMTB size had a limited influence within the tested power range, however, suggesting that the presence of a thermal bridge is more critical than its specific form factor under these conditions.

In contrast, the high-thermal dielectric boards exhibited only a modest additional temperature reduction of approximately 2°C with SMTBs. This diminished impact indicates that once bulk heat spreading through the PCB stackup is significantly improved, localized heat-spreading elements provide only incremental benefit.

Together, these results support a substrate-first thermal design approach, in which advanced high-thermal dielectric and prepreg materials serve as the primary mechanism for reducing peak temperatures, while SMTBs function as a complementary, fine-tuning solution for managing residual hotspots. For circuit board designers facing increasing power density and constrained form factors, these findings validate high-thermal dielectric materials as effective drop-in replacements for FR-4 and provide practical guidance on when SMTBs offer the greatest value within an overall PCB thermal management strategy.

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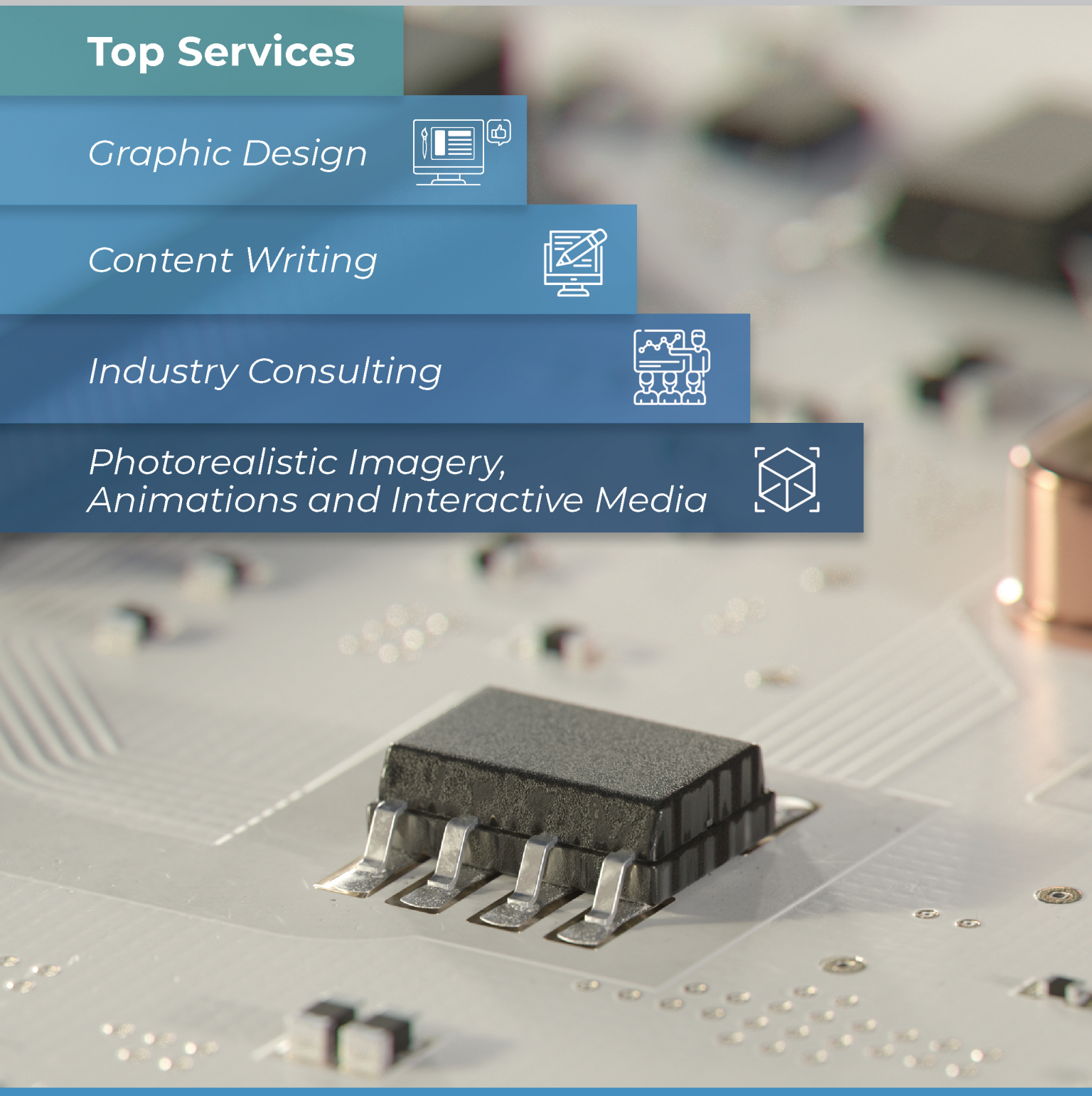

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VIA EVOLUTION

The Via Revolution: Stacked, Staggered and Copper-Filled

Copper-filled microvias, controlled aspect ratios and fabrication-aware design are redefining vias.

by ANAYA VARDYA

If you want a front-row seat to the evolution of PCB technology, look no further than vias. While ultra-fine lines tend to capture the spotlight, real transformation is happening in the via structures that connect those lines from layer to layer.

Vias are no longer simple drill-and-plate features. In ultra HDI, they are engineered elements that require the right geometry, material set and process window to work.

Let's take a look at what is driving this shift. As BGA pitches slide below 0.5mm and layer counts continue to climb, designers are leaning on microvias that must be smaller, more precise and far more reliable than only a few years ago.

Good interconnects start long before a board hits the shop floor. They begin with a design that accounts for limits, opportunities and the realities of building ultra HDI.

Copper-Filled Microvias

One of the most significant changes shaping UHDI is widespread adoption of copper-filled microvias. In HDI, nonconductive fill was often adequate. As features shrink, electrical and mechanical demands quickly escalate, however. That is where copper fill earns its place.

Copper-filled microvias bring two major benefits:

- They support stacked structures. A solid, planar landing pad provides the next microvia with something stable to sit on.
- They distribute stress more evenly. Copper does not deform as resin does, so the interconnect is better prepared to handle thermal cycling.

From the fabrication side, none of this happens by accident. Producing a reliable copper-filled via requires a well-tuned plating process. Bath chemistry, temperature and agitation patterns all interact to drive a consistent fill. When

these are in balance, the via fills cleanly and planarizes smoothly. Copper via-fill isn't just a material choice. It's an entire process commitment.

Small Ratio, Big Consequences

Via diameter and depth are often addressed separately, but aspect ratio is the real story. A microvia that's too deep for its width becomes difficult to plate up evenly and harder to drill cleanly. For ultra HDI, most fabricators prefer aspect ratios of 0.75 to 1:1. Some can push tighter, but only with specifically tailored materials and equipment.

Why does staying within this window matter?

When a via is too deep relative to its diameter, plating uniformity drops sharply and increases the risk of voids and weak spots. Very thin dielectrics also make laser drilling less predictable, complicating depth control and consistency. In addition, debris removal becomes more difficult, permitting residual material to remain in the via where it may introduce long-term reliability risks. Aspect ratio can significantly impact yield. It's one of those details that feels minor but has a real consequence on the finished board. A little knowledge upfront saves a lot of headaches later.

Stacked Vias

Stacked vias are quickly becoming the norm in UHDI builds, especially when routing channels narrow and there is no room to stagger. Copper fill enables stacking, but it also raises the bar for process control.

Stacked via structures depend on consistent dielectric thickness, so each laser drill can reliably reach its intended depth. They also require precise layer-to-layer registration as spacing shrinks, along with planar, well-filled microvias that remain stable and do not deform during lamination.

When all these elements are aligned, stacked vias deliver impressive density and performance. If a single process step shifts, however, alignment issues or stress concentration become visible.

Stacking is doable and predictable, especially when treated as a precision-engineered structure.

Staggered Vias: The More Forgiving Alternative

While ultra HDI may receive considerable attention for stacked vias, staggered vias are a smart choice in many designs. The structure, offsetting each microvia, permits the dielectric to absorb mechanical strain rather than concentrating it in a single column of copper.

Staggered via structures are especially useful when the dielectric system has higher CTE values or when dielectric thickness varies across the stackup. They are also well-suited for products that experience wide temperature swings and for designs where long-term reliability is more important than maximum routing efficiency. The tradeoff is straightforward: staggering consumes more board real estate. However, for many applications such as wearables, portable electronics or anything facing harsh thermal conditions, the extra robustness is worth the added routing

effort.

From a fabrication standpoint, the difference between a via fence and American Standard Circuits' Via Wall shows up in yield and consistency. A via fence is usually placed for electrical reasons and tolerated as long as it functions. A Via Wall is engineered as part of the build process itself, with tighter spacing and registration intent, giving the fabricator a more stable structure to control movement, drilling accuracy and copper fill behavior as microvia counts climb **(Figure 1)**.

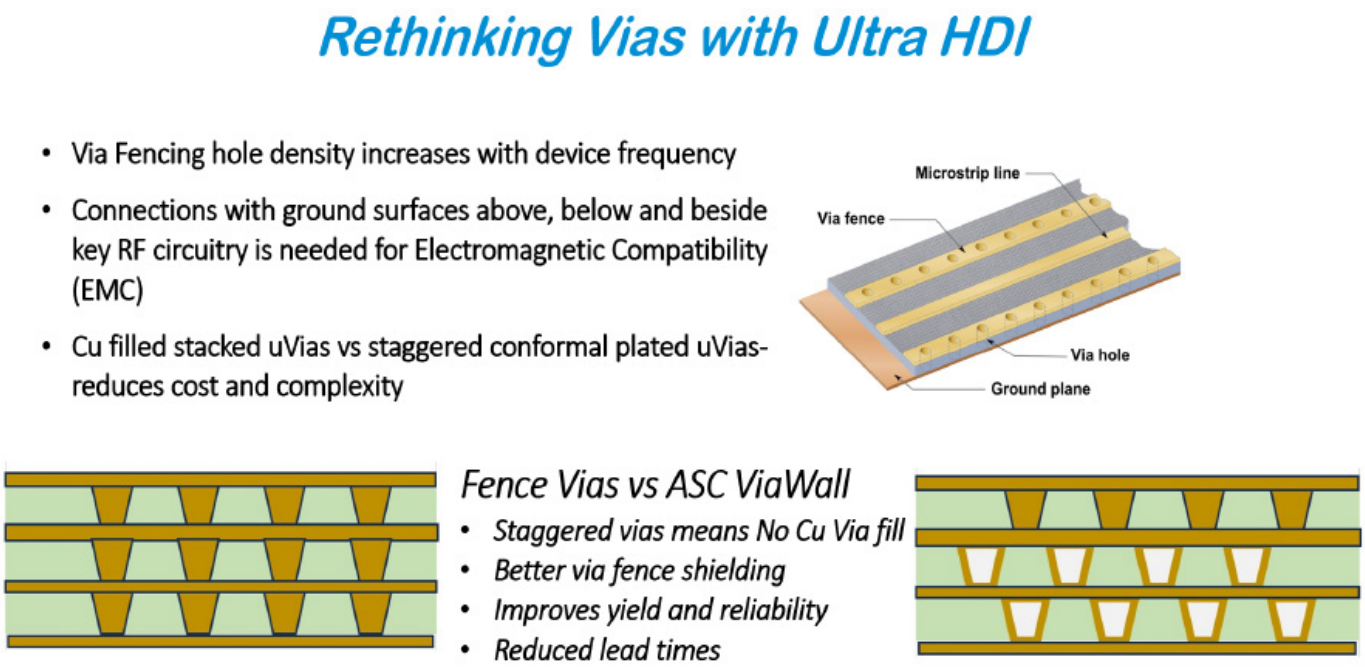

Figure 1. ASC's novel RF fence via option.

Materials and Via Wall Integrity

Selecting the right materials has always mattered in PCB design, but in UHDI, the margins get tighter. Materials considerations include:

- **Dielectric response to laser drilling.** With new materials and thin dielectrics, even small variations can begin to affect consistency and depth control.
- **Copper adhesion and foil roughness.** Very low-profile and ultra-low-profile coppers contribute to signal integrity at high speeds, but do not always give the same kind of mechanical anchoring when compared to rougher foils. That could affect the bonding of microvia walls to the surrounding material.
- **Resin recession.** During thermal cycling or reflow, resin can pull back from copper. In thin dielectrics, even a few microns of recession can impact via wall support.

It's not about adding complexity but choosing materials that behave predictably with the processes the fabricator uses.

Designing with Real Process Windows

Innovation is exciting, but implementation takes the prize. The most successful ultra HDI designs grow out of early conversations with fabrication partners. Once their drilling capability is understood, via fill processes, registration tolerances and material preferences, design structures can be designed that build cleanly and yield well.

Practical suggestions:

- Keep aspect ratios conservative, unless the fabricator confirms it can support more aggressive geometries.
- Treat stacked microvias as engineered features rather than just vertical routing lines.
- Material selection aligned with processes for drilling, filling and laminating the board.
- Provide spacing representative of real-world registration tolerances.

When the design intent aligns with the fabrication capability, UHDI becomes predictable rather than challenging. And predictable is what we need when long-term reliability counts.

Takeaways

The via revolution in UHDI is not just about feature-size reduction; it is about a complete ecosystem that permits these small features to perform reliably over time. Copper-filled microvias, precise aspect ratios, well-controlled laser drilling, and thoughtfully chosen materials all work together to deliver designs that hold up under demanding conditions.

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CORE MATERIALS

Adhesive vs. Adhesiveless Polyimide Core Materials Used in Flex and Rigid-Flex Applications

How polyimide core technology determines whether electronics survive extreme conditions.

by AKBER ROY

Deciding which processes and materials to adopt for a PCB design depends on the designer's awareness of the factors that influence those decisions. For example, which regions are targeted for your product? The supply chain cycles for materials are greatly impacted by geography and demographics. What are the limits of environmental conditions (heat and pressure, etc.) the product will be exposed to? Such factors also affect the choice of materials used in PCB manufacturing. Similarly, your awareness about the purpose, the scope and the type of industry that will use the product will also help you choose the right materials and processes for manufacture.

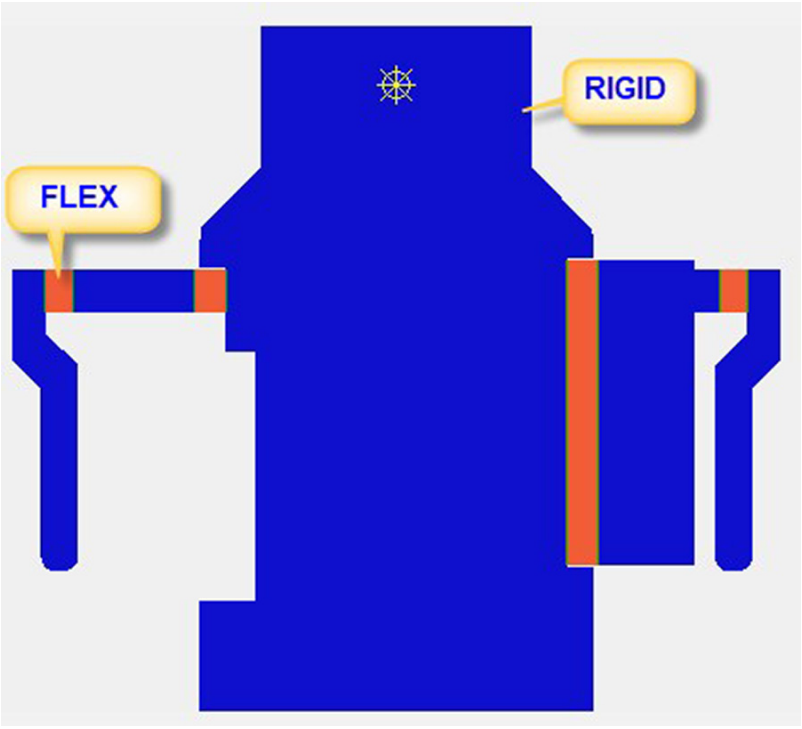

Figure 1. A rigid-flex PCB structure showing flexible arms extending from a rigid core section.

Awareness of these tradeoffs helps engineers design smarter, prevent failures and allow industries to balance

performance with cost.

Understanding materials ensures more reliable products, better sourcing and competitiveness in high-tech markets. Why should anyone outside of engineering care about this? Because the choice of core material shapes the devices we use and trust every day.

Look at a smartphone, car sensors or even satellites orbiting above us. What permits them to keep working reliably in blazing heat, freezing cold or under constant stress? Most people point to the chips and processors, but the real unsung hero is the PCB.

If chips are the brain, the PCB is the nervous system, with its copper pathways carrying signals and power. But not all PCBs are created equal, and their performance often depends on their core material.

Polyimide, a high-performance polymer valued for toughness, flexibility and heat resistance, is a popular choice. Yet even here, engineers must decide between adhesive-based and adhesiveless cores.

It may sound like a small detail, but this choice affects whether a phone bends without breaking, the automotive electronics survive under the hood or satellites stay connected in orbit. This article unpacks both technologies in plain language to show why such a decision truly matters.

Polyimide – Built for the Tough Stuff

Let's start with the basics: why is polyimide so desirable? Imagine a material that can sit in an oven at around 260°C (500°F) without a problem, stand up to strong chemicals and remain tough even when it's as thin as paper. That's polyimide.

Because of these attributes, polyimide offers certain standout qualities. It doesn't break down in high heat, making it a fit for soldering and hot environments. It's tough yet flexible, so it won't easily crack or snap when bent – perfect for foldable phones and wearable devices. It also keeps electrical signals clean and stable, even at very high speeds, which is vital for applications such as 5G and radar. Because it resists harsh chemicals, it withstands the demanding steps of PCB manufacturing.

This is why polyimide is found everywhere: in the flexible circuits inside foldable gadgets and medical devices, in high-frequency systems like 5G towers and aerospace communications and in extreme places like car engines, oil drilling equipment and satellites. It also makes today's slim smartphones and laptops possible by supporting boards packed with tiny components. In many ways, polyimide serves as a canvas for modern electronics.

The next big question is: how do we attach the copper wiring to this canvas? That's where adhesive and adhesiveless cores come in.

Polyimide Cores with Adhesive: The "Classic" Approach

It's a lot like making a sandwich. You have your bread (the polyimide film), spread on mayo (the adhesive resin) and

then add slices of meat (the copper foil). Press it all together under heat and pressure, and you've got a laminated panel: copper / adhesive / polyimide / adhesive / copper **(Figure 2)**.

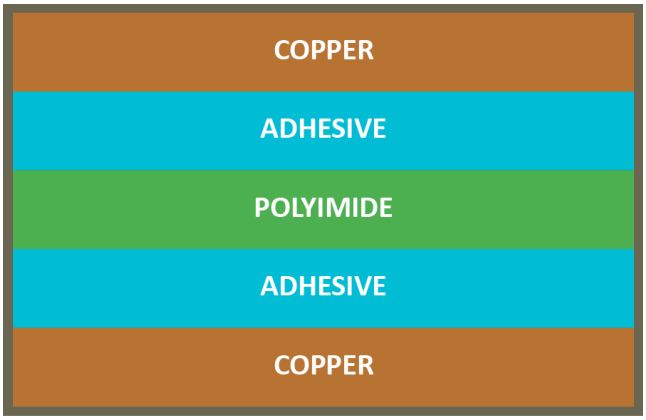

Figure 2. Cross-section of an adhesive-based polyimide core.

Benefits of Adhesive Cores

Adhesive-based cores have been the industry standard for decades for a few good reasons:

- **Cost-effective and mature.** Adhesive-based cores have been around for a long time, which means the processes are well understood. They are easy to source, simple to manufacture and much more affordable than newer alternatives.
- **Strong, reliable bonding.** The adhesive layer creates a dependable link between copper and polyimide. This bond helps the board stay durable during handling, assembly and everyday use.
- **Thick copper friendly.** Adhesive systems can easily work with thicker copper layers. This makes them a good choice for power electronics, where carrying higher currents and extra strength are important.

Limitations of Adhesive Cores

Like any classic design, an adhesive core has limitations:

- **Thermal bottleneck.** Adhesives can't handle heat like pure polyimide can. They may soften or outgas during soldering, causing delamination.
- **Expansion mismatch.** Adhesives expand more with heat than copper or polyimide. This puts stress on vias, leading to cracks over time.
- **Signal loss.** Adhesives have higher electrical loss at high frequencies, reducing signal clarity in GHz circuits.
- **Added bulk.** Adhesive layers make the core thicker and less flexible.
- **Moisture absorption.** Adhesives soak up more water, which can turn to steam during soldering and cause blistering.

Adhesive cores are like a family sedan. Affordable, dependable, perfect for everyday commutes. But ask it to run a Formula 1 track, and it starts to show its limits.

Adhesiveless Polyimide Cores – A Smarter Solution

Enter the adhesiveless core. Instead of gluing copper to polyimide, engineers figured out ways to bond them together directly **(Figure 3)**.

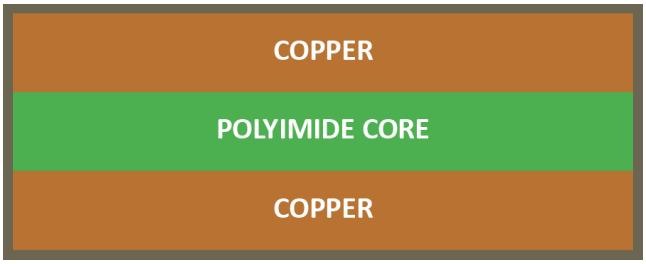

Figure 3. Cross-section of an adhesiveless polyimide core with copper bonded directly to the polyimide layer.

Two common methods are typically used. In the cast polyimide process, liquid polyimide is applied directly onto copper foil and then cured, forming a seamless bond between the materials. In the second method, the polyimide film undergoes surface treatment and is seeded with a thin metal layer through sputtering, after which copper is plated onto the surface to complete the bond.

Benefits of adhesiveless cores. Adhesiveless cores offer several advantages. They provide strong thermal endurance, permitting exposure to lead-free soldering and harsh operating environments without degradation. Because the copper and polyimide expand at more similar rates, they deliver improved dimensional stability and reduce stress on vias. They also support better high-frequency performance with lower signal loss, making them well-suited for applications such as 5G and radar. Without an adhesive layer, the construction is thinner and lighter, enabling slimmer device designs. In addition, pure polyimide absorbs less moisture, reducing the risk of soldering-related defects.

Limitations of adhesiveless cores. Adhesiveless cores bring a variety of tradeoffs. This technology is generally more expensive to produce, as it requires specialized materials and tighter process control. The manufacturing process itself is more complex, often demanding advanced equipment and technical expertise. In addition, integrating very thick copper layers can be more challenging compared to adhesive-based constructions. If adhesive cores are sedans, adhesiveless cores are Formula 1 cars. Costly, precise and not for everyone, but unbeatable when conditions are demanding.

Making the Best Choice

So, which option is really better? It depends on the needs. Both adhesive and adhesiveless cores have unique strengths, and the right choice depends on cost, performance and the environment the board will operate in.

Adhesive cores make sense when:

- Budget is the priority (consumer gadgets, appliances).
- The environment isn't too harsh.
- Thick copper is needed for power; and
- Speed and supply chain familiarity matter.

Adhesiveless cores are the best choice when:

- Reliability is non-negotiable (aerospace, automotive safety, medical devices);
- High-frequency performance is critical (5G, radar, high-speed servers).
- Extreme conditions are the norm (space, drilling, under-hood electronics).
- Devices must be thin, light, and compact (wearables, smartphones).

Feature	Adhesive Core	Adhessiveless Core	Suitable For
Cost	Lower	Higher	Budget builds
Thermal Performance	Limited	Excellent	Harsh environments
Via Reliability	Weaker	Strong	Automotive, Aerospace
High Frequency	Lossy	Clean	5G, Radar
Thickness	Thicker	Thinner	Miniaturized devices
Moisture Resistance	Lower	Higher	Humid environments

The Key Point

The decision whether to use adhesive or adhesiveless polyimide cores may seem like a technical footnote, but the choice involves performance, reliability, size and cost.

- Adhesive cores remain the dependable, cost-effective backbone of countless devices.
- Adhesiveless cores enable cutting-edge applications from foldable phones and wearables to aerospace systems and medical implants.

As electronics keep pushing boundaries, e.g., faster, smaller, hotter and lighter, then adhesiveless cores are stepping into the spotlight. The next time you look at your latest device, keep in mind that it is not just the chips that matter, but also the unseen materials working behind the scenes to make it reliable.

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SUPPLY CHAIN SECURITY

The Victory Plan Reborn: Forcing the Surge of America's Drone Industrial Base

Leveraging artificial obsolescence to operationalize the domestic supply chain.

by ED DODD

In my previous article, we explored the 1941 Victory Plan as a masterclass in industrial foresight, where the US moved from isolation to becoming the "Great Arsenal of Democracy." As President Franklin Delano Roosevelt noted in 1940[1] the goal was not just to design weapons, but to produce them in sufficient volume to save future generations the "agony and suffering of war." Today, as we face a new era of near-peer competition, the Victory Plan has been reborn, with a new focus shaped by the modern battlefield. While the 1940s emphasis was on steel and aircraft, our current challenge lies in the rapid, high-volume production of electronics and sensors like those that power modern unmanned systems.

In this new reality, the ability to scale manufacturing has become as important as the ability to innovate. Secretary Hegseth has signaled that the Department of War will do business only with industry partners that share a relentless focus on speed and volume above all else.[2] This pivot moves the priority from a handful of massive prime contractors toward dynamic vendors capable of surging American manufacturing at scale. As Hegseth noted during his nationwide tour, the goal is to transform factories of the heartland into the foundries of a new golden age of peace through strength.[3] For manufacturers, this is a call to move beyond prototyping and demonstrate the industrial capacity to sustain a protracted, high-attrition conflict.

While declarations of acquisition reform are not new for DoW leadership, they often lack specifics and typically result in policy changes that have less impact on the broader industry than hoped. Secretary Hegseth's Arsenal of Freedom speech talked about changes aimed at enabling a larger part of the national industrial base and spoke in general terms about the potential opportunities those changes would have for those nimble enough to achieve speed and scale. Now, just months after Secretary Hegseth's speech, the December 2025 FCC drone ban has effectively moved the conversation from general strategy to a specific opportunity for the American electronics industry.

The Dependency Trap

The Chinese drone industry accounts for more than 90% of the commercial drone market. This is a result of a 10-year program called Made in China 2025 launched in 2015.[4] Under this initiative, the Chinese government provided huge, multilayered subsidies to companies like DJI, ranging from direct capital investment, low-interest loans from state-owned banks, to subsidized land and R&D tax credits. These financial advantages enabled Chinese firms to engage in

aggressive product dumping, selling drones and drone components at prices often below cost. This artificially low pricing suppressed the emergence of a domestic US manufacturing base, since American startups couldn't match the scale or prices offered by Chinese companies.

Despite these obvious signs of market manipulation, formal anti-dumping actions were avoided for years, primarily due to the complex interdependence of the global electronics supply chain. Federal regulators and industry leaders feared that aggressive trade litigation would lead to retaliatory strikes on critical components, such as the rare earth magnets and lithium-polymer batteries, where China holds a near-monopoly. By the time the US began discussing targeted restrictions, the dependency trap was already set: there was so little domestic industry that immediate decoupling threatened to ground the very public safety and infrastructure programs the government sought to protect.

Dependency as a Strategic Risk

Concerns over Chinese dominance of the drone market are more than simply economic. Reliance on foreign-produced UAS and their components presents a significant risk regarding surveillance and data security. These systems can enable foreign actors to monitor US territory, military bases and critical infrastructure. The security risk extends beyond the airframe to include subsystems like flight controllers, navigation systems and data transmission devices, all of which can provide remote access to sensitive information.

Beyond data security threats, foreign-produced unmanned aircraft systems (UAS) pose significant risks of remote system disruption. National security determinations have highlighted that foreign-manufactured drones can be "disabled at will via software updates," effectively permitting a foreign adversary to shut down or cripple critical equipment on demand. This capability is particularly concerning for drones used in public safety and emergency response, where any reduction in operational performance could have immediate, life-threatening consequences.

The risk of disruption is a critical priority when considering the kinetic and operational threats to mass gatherings, especially as the United States prepares for high-profile events such as the 2026 FIFA World Cup, the America250 celebrations and the 2028 LA Olympics. The FCC and interagency commissions have noted that foreign-made UAS and their critical components could enable "destructive operations" over these dense urban areas, making the transition to secure, domestic technology a highest-priority national security mandate.[5]

The other risk associated with the Chinese government-sponsored market dominance is the continued suppression of the domestic drone supply chain. The dependence on foreign manufacturers has hollowed out American manufacturing capacity, resulting in chronic supply chain fragility. This strategic bottleneck means that even as the US attempts to pivot toward secure systems, it remains dependent on an adversary's production lines for the very components required to keep domestic alternatives flight-ready.

This dependency grants foreign actors substantial control over when and how supplies would be cut off. Whether through a sudden halt in parts exports or a malicious firmware update, the operational lifespan of US drone technology is largely subject to foreign influence. By controlling the flow of essential parts and the software that governs them, Chinese companies and their government sponsors decide when a fleet becomes obsolete or non-

functional. To avoid being at the mercy of a nation at a time when conflict may be imminent, the US must take control of that timing, and do it in a way that is gradual enough to avoid a collapse of US drone manufacturing, but fast enough to provide the demand shock necessary to shore up existing domestic suppliers and encourage new market entry.

The Regulatory Pivot: A New Victory Plan

Back in 2024, Congress laid the foundation for action in the drone market. Section 162 of the 2025 National Defense Authorization Act (NDAA) established a legal mandate for the supply chain resiliency of small UAS, while Section 164 prohibits the procurement of LIDAR made in restricted countries, including China.[6] This created budgetary and legal pressure for the Executive Branch to act against foreign drone technology dependency.

In 2025, two executive orders (EOs) were issued. The Restoring American Airspace Sovereignty EO acknowledges the risks that drones pose to public safety in the hands of bad actors, and establishes a range of activities to minimize any exposure to the risk of drones to public infrastructure, military and federal facilities and large events.[7] The Unleashing American Drone Dominance EO establishes efforts to accelerate the testing and operation of UAS while encouraging the expansion and scale-up of domestic production.[8]

Section 7 specifically addresses strengthening the American drone industrial base and requires the Secretary of Commerce to propose rulemaking to secure the United States drone supply chain against foreign control or exploitation." The proposed Commerce action to ban or restrict Chinese drones and components was met with industry resistance, with one expert responding, "Immediately removing all foreign adversary-based sources of supply for critical drone components would have a catastrophic effect on the American drone industry."[9]

While the FY2025 NDAA included some language to encourage the domestic drone industry, stronger language from the Countering CCP Drones Act was originally incorporated into the House Version of the NDAA. The Senate did not include that language in its version, indicating a successful lobbying effort by DJI and drone operators, many of whom cited that DJI provided data. Commerce action was met with similar resistance to include domestic drone manufacturers that depend on Chinese-made parts. Active efforts to ban Chinese drones and components have not been effective. There was a ticking bomb inside the NDAA, however.

Section 1709 of the FY2025 NDAA required the executive branch to assess whether DJI communication and surveillance technology or services pose an "unacceptable risk to the national security of the United States." Furthermore, the section includes a clause stating that if no determination is made, the FCC will automatically add them to the covered list, a list of equipment that under the Secured Networks Act cannot be authorized, imported or sold in the United States.

Essentially, if the government did not assess the DJI technology in time, an automatic ban would be put in place. On December 21, 2025, the FCC released a draft of its National Security Determination on the Threat Posed by Uncrewed Aircraft Systems (UAS) and UAS Critical Components Produced in Foreign Countries.[5] On December 22, the FCC added UAS and critical components to the covered list.[10] This was revised based on the DoW's January 7th input to

temporarily include a few exceptions. Next, we will unpack what this means.

Artificial Obsolescence and the Domestic Mandate

As of December 22, no new UAS or UAS critical components will be approved for import or sale in the United States; previously approved items may continue to be sold. In the short term, this does two things: freezes the level of technology being imported and starts the clock on availability. In the medium term, it provides drone manufacturers and commercial operators with the current equipment they need to stay in business while establishing the urgency needed to nurture the domestic supply chain.

Figure 1. Government measures to overcome subsidized foreign dumping and establish clear standards for compliant tech create a guaranteed demand for domestically manufactured components.

Key drone components include

- Flight controllers and autopilots: The strategic brain of the aircraft, these are the highest priority targets for replacement.
- Radio and data Transmission links: Critical for data security.
- Ground control stations (GCS): Trusted HW and SW prevent data breaches at the point of operation.
- Navigation and positioning modules: Control where the drone is permitted to fly and what it can see.
- Sensors and LIDAR: Essential for high-fidelity mapping.
- Smart batteries and power management (BMS): A potential point of remote system disruption.
- Propulsion systems (motors and ESCs): High turnover consumables that must be produced at scale.

By targeting only new equipment authorizations, the FCC has effectively frozen the level of foreign technology permitted within the US national airspace. This move prevents further entrenchment of sophisticated foreign sensors

and communication protocols that have become increasingly difficult to audit. While legacy systems currently in the field can continue to operate, they are now technologically "static," unable to introduce new hardware-based capabilities that might pose further security risks. For the first time in a decade, American manufacturers are no longer chasing a subsidized, moving target; the foreign technological "ceiling" has been fixed, permitting domestic firms to close the capability gap without the fear of being undercut by a state-funded iteration before their products even hit the market.

While the technological freeze provides a temporary baseline, it simultaneously triggers a state of artificial DMSMS (diminishing manufacturing sources and material shortages). In a typical product lifecycle, obsolescence occurs naturally as newer, more efficient parts replace the old. Here, however, obsolescence is being dictated by legislation. By prohibiting new authorizations, the government has essentially placed a "death date" on the foreign-made fleet currently in use. There will come a time when manufacturers commit resources to manufacturing new versions of their products. While these versions might technically be compatible upgrades for existing equipment, they will not be authorized in the US, and it will be as though the product ceased to be manufactured, with no replacement. For operators, this creates an immediate, high-stakes countdown. Even if a foreign-made drone is physically functional today, the inability to import new, authorized replacement parts or certified subsystems means the entire platform is on a predetermined path to operational extinction.

To ensure this countdown does not lead to a catastrophic collapse of public safety and commercial operations, the government has provided a critical bridge through the Blue UAS initiative. On January 7, the Undersecretary of War for Acquisition and Sustainment carved out exceptions for items on the Blue UAS Cleared List and for components that qualify under the Buy America Act.[11] While they provide some flexibility and may soften the shock of the ban, these exemptions are temporary and expire at the end of 2026.

Managed by the Defense Contract Management Agency (DCMA), the Blue UAS Cleared List is a curated catalog of drones and components that have undergone rigorous cybersecurity scrubs and are verified as NDAA-compliant.[12] By excepting these vetted systems from the most stringent restrictions, federal policy ensures that the pipeline for verified, secure components remains open. This framework provides a stable environment that enables operators to maintain their missions as the domestic market prepares to take the lead.

Ultimately, this managed transition is designed to clear a huge space in the market that only domestic electronics manufacturers can fill. By removing the pressure of subsidized foreign dumping and establishing clear standards for compliant tech, the government has created a guaranteed demand for domestically manufactured components. This is the new Victory Plan in action: a policy-driven shock that signals to investors and engineers that the era of foreign dependency is over. As the US prepares to secure its skies for the 2026 World Cup and beyond, the market space has been created, and the opportunity for a domestic industrial surge is now clear and actionable.

Conclusion

The vacuum created by the FCC is more than a policy shift; it is a generational invitation to the American electronics industry. The Victory Plan of 1941 succeeded because America's foundries rose to meet a challenge that seemed

industrially impossible. Today, our foundries are our clean rooms and assembly lines. Our steel is the PCB and SMT parts that make autonomous flight possible. The artificial obsolescence of foreign drone technology has cleared the board, but that vacancy will only be filled if domestic manufacturers move with speed, at scale.

As the clock winds its way through 2026, the era of convenient dependency has officially ended. We are no longer waiting for the market to correct itself against subsidized foreign dominance. The government has stepped in to force that correction. For the domestic innovators and investors willing to seize this moment, the mandate is clear. Build the vetted sub-systems that will define the next century of aerospace. The Arsenal of Freedom is being rebuilt, and its success will be measured, in part, by the resilience of the American-made components that secure our skies.

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SURFACE **READINESS**

The Principals of Adhesion: Understanding Adhesive Chemistry, Application and Surface Science for Optimal Bonding Performance

An investigation of surface energy effects on adhesive bond strength.

by DAVID DWORAK

Reliable bonding depends on three critical variables working in synergy **(Figure 1)**. If any of these pillars is weak or inconsistent, overall bond performance is compromised.

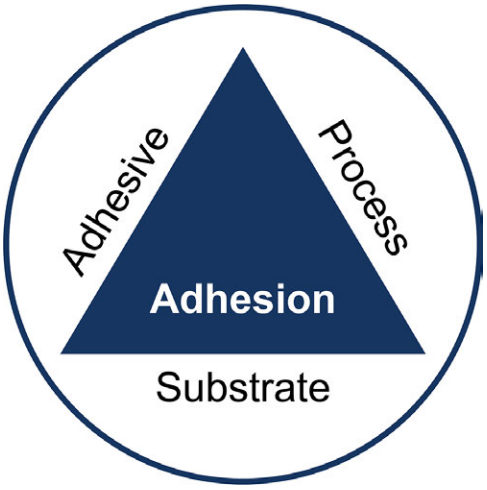

Figure 1. Three pillars of reliable adhesive bonding.

1. Adhesive chemistry. Adhesive performance begins with formulation. Polymers, such as acrylics, epoxies and silicones, are blended with fillers, crosslinkers and other additives to tune properties for strength, toughness, flexibility, cure speed and environmental resistance.
2. Process controls. Even the most advanced adhesive cannot perform as intended without proper processing. Correct storage, handling, mixing (for two-component systems), dispensing and curing are all critical to achieving full polymerization and consistent bond strength.
3. Substrate surface energy. The condition of the bonding surface plays a critical role in an adhesive's ability to wet the substrate and form a durable bond. Low surface energy, often caused by contaminants, oxidation and manufacturing residues, impedes wetting and can significantly reduce bond performance.

While advances in adhesive chemistry and processing have made the first two pillars easier to optimize, substrate surface variability remains the most persistent cause of inconsistent adhesion and often the most overlooked. Understanding and managing substrate surface energy is therefore essential to achieving reliable, high-performance bonds. Only with an understanding of all three pillars and careful alignment and management of them will one be able to optimize adhesive bonding.

Following is a more in-depth look at each pillar:

Pillar 1: Adhesive chemistry. Adhesives today are used in electronics assemblies and applications to address many needs beyond bonding, such as providing a method to absorb stress from substrate CTE mismatches, providing thermal conductivity, electrical conductivity or flame retardancy. Adhesive formulations have evolved into an advanced science delivering the end-user with one's specific, desired product properties. In addition to these advanced product properties, adhesives can be formulated to enhance adhesion, targeting specific substrates. It is important to consult the adhesive manufacturer for guidance on selecting the appropriate adhesive for a particular application.

Chemical formulation, including polymer architecture, cross-link density and additive selection, plays a central role in adhesive performance. These factors govern curing speed, viscosity, rheology, strength, toughness and flexibility. Additives, such as adhesion promoters, coupling agents, fillers and diluents, can further enhance compatibility with difficult-to-bond substrates. Together, these formulation choices influence how effectively an adhesive wets and conforms to surface topography.

Yet even the most advanced formulation cannot completely compensate for an adhesive that was stored, dispensed or cured incorrectly or applied to poorly prepared, low-energy surfaces. While formulation allows chemists to tailor adhesives for specific needs, proper handling and processing of the adhesive and proper substrate conditioning remains essential for consistent, long-term bond reliability.

Pillar 2: Process and application controls. Proper handling and processing of adhesives are critical to their ultimate performance. This includes receiving the adhesive from shipping, storage, thawing and mixing if required, management of pot life, dispensing and curing. Each of these steps affects the adhesive's performance and should be optimized in accordance with the adhesive manufacturer's guidelines.

One-component (1K), heat-curing adhesives typically must be shipped in dry ice and stored frozen, while two-component (2K) adhesives are mostly room-temperature stable. Adhesives that were stored frozen require a thawing step before use. Proper thawing technique is required to avoid introducing air voids into the adhesive. Also, as soon as the adhesive is removed from the freezer, careful time tracking is required to monitor adhesive pot life. UV curable adhesives are unique in that they are 1K adhesives, but mostly are room temperature stable and do not require frozen storage. UV curable adhesives also typically have an unlimited pot life, so there is no need to track time when in use.

2K adhesives require a mixing step to blend the two parts in the appropriate ratio prior to use. The adhesive manufacturer will provide the mix ratio of the two components, and it is critical that this mix ratio is properly achieved. Typically, mixing each component separately to address filler settling, then mixing the two components together is required.

The adhesive must be dispensed and cured, again according to manufacturer guidelines. Heat or room-temperature exposure is a common method to achieve a cure, typically lasting 30 min. to 24 hr. UV light-curing adhesives will cure in seconds.

Each of these steps is important for properly processing the adhesive. Follow the adhesive manufacturer's guidelines and optimize the manufacturing process. In conjunction with the other pillars, this will ensure the best opportunity for a successful bond.

Pillar 3: Substrate surface condition. While pillars 1 and 2 are critical components to achieving a successful bond, they are mostly well understood and optimized. Pillar 3 and understanding the impact the substrate surface condition has on the adhesive bond are many times overlooked. The root cause of many adhesive failures is substrate-related and poor conditioning of the substrate surface.

The following are insights into substrate surface energy, a key property determining a substrate's readiness to bond with an adhesive, as well as practical methods for measuring surface energy.

Surface Energy Principles and How to Measure It

Atoms and molecules at a substrate's surface exist in a higher-energy, more reactive state than those within the bulk material. This property, known as surface energy, determines how readily the surface interacts with other materials. In practical terms, it governs whether a liquid, such as water, an adhesive, a coating, or ink, will spread out (wet) or bead up on the surface.

For an adhesive to bond effectively, it must wet the substrate by spreading out to make intimate surface contact. Whether wetting occurs depends on the balance of interfacial energies between the liquid, the solid and the surrounding air. Each interface (liquid-solid, liquid-air, and solid-air) has an associated energy, and the system as a whole naturally seeks a lower-energy, more stable state. If spreading reduces the total interfacial energy, then the liquid wets the surface. If spreading increases the total energy, the liquid retracts and beads up.

Water contact angle measurement is a practical method for evaluating surface energy **(Figure 2)**. By placing a small water droplet on a surface and measuring the angle at the liquid-solid-air interface, engineers can quickly assess surface condition and bond readiness. Water is particularly useful for this test because its high polarity and sensitivity to surface chemistry correlate well with adhesion performance.

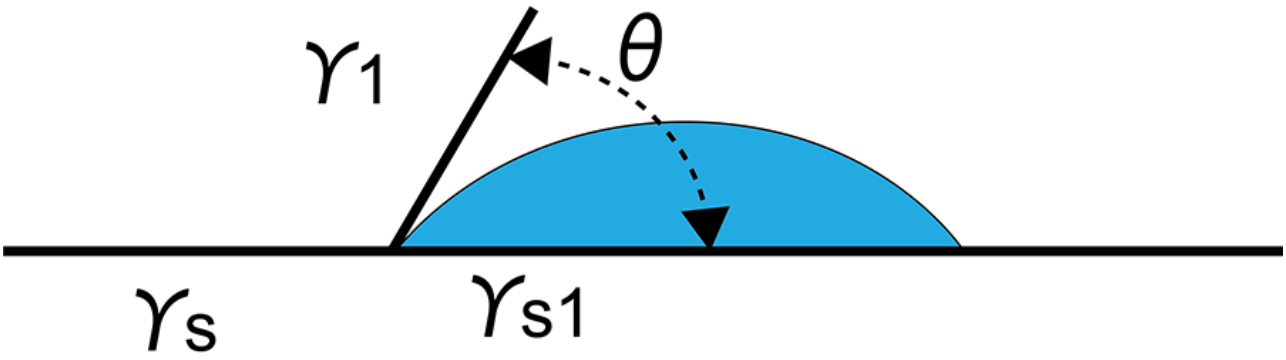

Figure 2. Contact angle (Θ) is determined by the balance of interfacial energies: liquid surface tension (γl), solid surface energy (γs) and the remaining interfacial energy (γsl).

Low-energy surfaces. Polymeric substrates such as untreated polyethylene, polypropylene or polytetrafluoroethylene (PTFE) have inherently low surface energy due to their chemically inert structures. Since water is more strongly attracted to itself than to these surfaces, droplets remain nearly spherical, producing high contact angles (typically 70°-90°) **(Figure 3)**. These low-energy surfaces exhibit poor wettability and limit adhesive flow, resulting in weak and unreliable bonds. To improve adhesion, these surfaces can be modified using plasma, corona discharge or flame treatments, or by applying chemical primers – all of which increase surface reactivity and promote improved wetting.

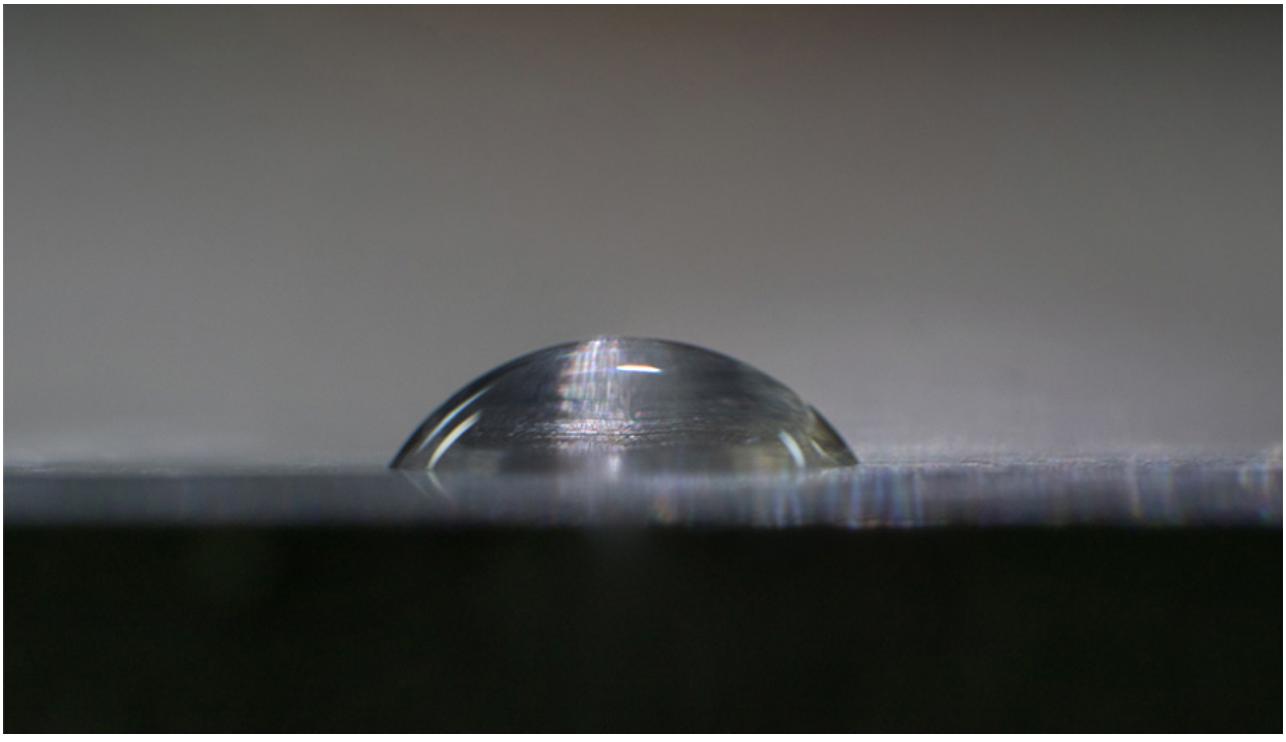

Figure 3. Low-energy surface (liquid beads up, indicating poor adhesion).

High-energy surfaces. When a water droplet is placed on a high-energy surface, such as freshly cleaned metal, ceramic, glass or a substrate, the droplet is more strongly attracted to the surface than to itself and spreads out, producing a low contact angle (typically <50°) **(Figure 4)**. This behavior reflects strong molecular attraction between the liquid and solid and indicates excellent wettability. In practical terms, good wettability permits the adhesive to

make intimate surface contact, flow into microscopic surface features and establish strong chemical and mechanical bonds.

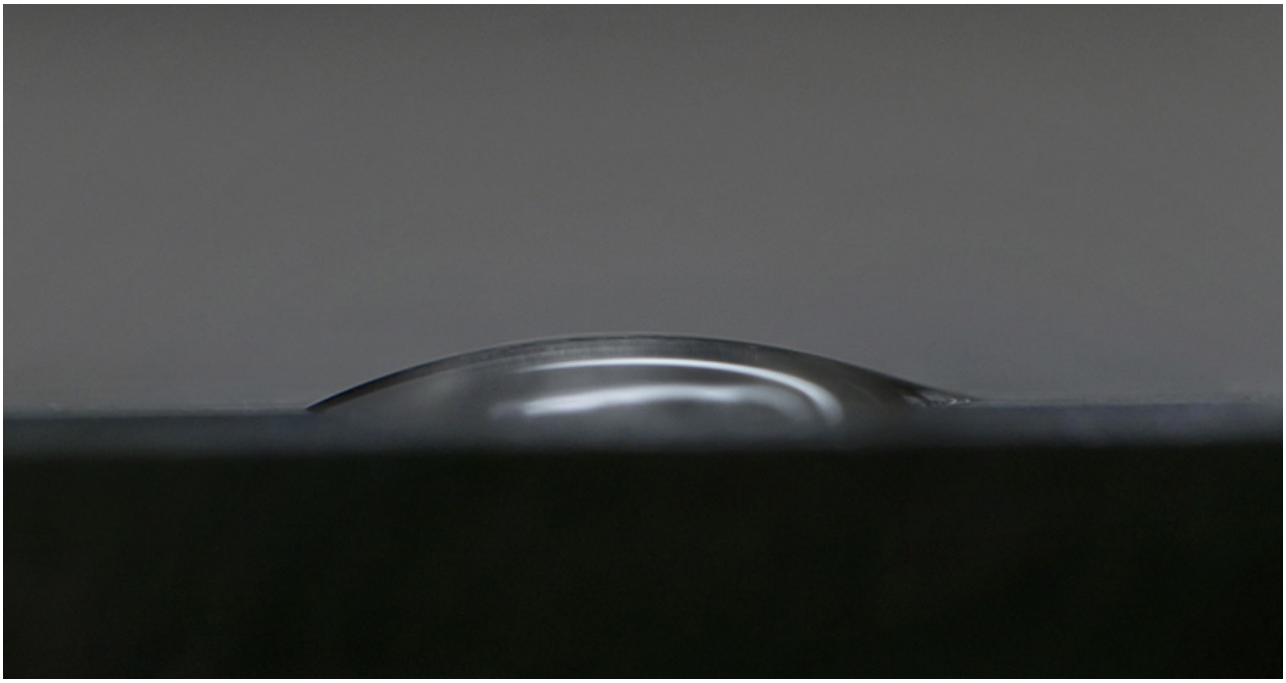

Figure 4. High-energy surface (liquid spreads out, indicating good adhesion).

Moderate-energy surfaces. Moderate-energy surfaces exhibit limited attraction to water and other liquids, sufficient for partial wetting, but not strong enough to fully overcome a droplet's cohesive forces. Consequently, adhesives may show inconsistent or marginal performance on these surfaces unless additional surface preparation is performed.

Graphical Correlation between Surface Energy and Water Contact Angle

Figure 5 shows the inverse relationship between water contact angle and surface energy. High surface energy results in low contact angles, indicating that a liquid can spread and wet the surface effectively. Conversely, low surface energy results in high contact angles, where liquids bead up, and wetting is poor.

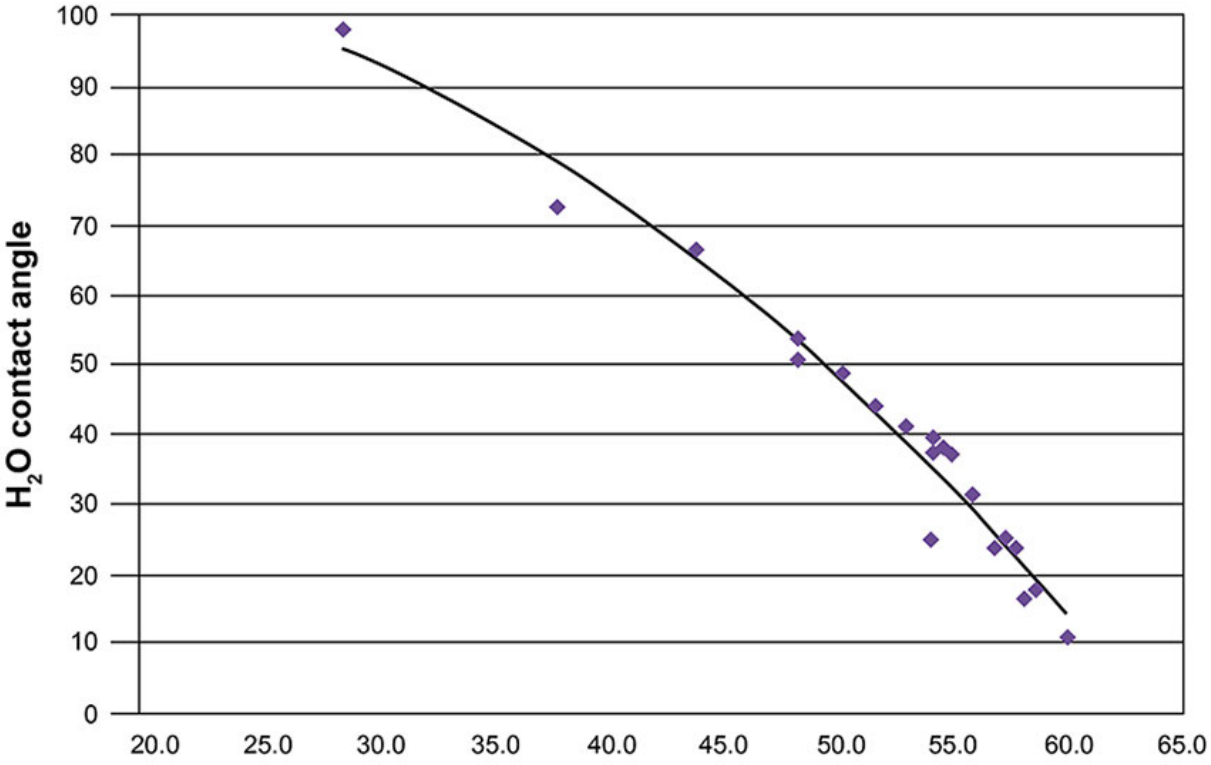

Figure 5. Surface energy versus water contact angle.

Fundamentals of Surface Chemistry

Although mechanical bonding, created when an adhesive wets and flows into microscopic surface features, contributes to bond strength, adhesion primarily originates from chemical interactions between the adhesive and the substrate at the molecular level.

In hard materials such as metals and glass, atoms are arranged in tightly bound, well-ordered lattice structures. At the surface, the structure is incomplete because exposed atoms lack bonding partners, however. As a result, these materials naturally have high surface energy and interact strongly with their surroundings. This high surface reactivity makes metals susceptible to oxidation, which can impede adhesion. When the oxide layer is removed by cleaning processes such as grit blasting, the freshly exposed high-energy surface readily forms strong, reliable adhesive bonds.

Polymeric substrate surfaces behave very differently. Their organic molecular structures exhibit far less intrinsic surface reactivity than inorganic materials, and their long, flexible polymer chains tend to move and reorient to minimize surface energy. Reactive groups may rotate inward or even diffuse beneath the surface, leaving a top layer dominated by low-energy loops and chain ends that interact weakly with adhesives. As a result, adhesives often struggle to bond to polymeric substrate surfaces without additional surface treatment.

Polymeric substrates vary in reactivity. Not all polymeric substrate surfaces exhibit the same bonding potential. Polar polymers, such as polycarbonate and polyamides (nylons), contain functional groups like hydroxyls and amides that create permanent dipoles. These increase surface energy and improve wetting, enabling stronger interactions

with adhesives and other liquids. In contrast, non-polar, chemically inert polymers such as untreated polyethylene, polypropylene or PTFE, lack these functional groups, resulting in low-energy surfaces that inherently resist bonding.

Time-driven decay of surface energy. Because surface atoms are highly reactive, they constantly interact with their environment. As a result, surface energy decreases during storage and handling as water vapor, hydrocarbons and other contaminants adsorb onto the surface. Metals oxidize rapidly, often unevenly, introducing variability in bond performance and highlighting the need for tightly controlled processing windows. Activated polymers treated by plasma, flame, or corona show a similar decline as newly formed polar groups migrate or reorient into the bulk. This time-dependent loss of surface energy can significantly reduce wettability and bond strength.

The rate and extent of surface energy decay depend largely on the material's initial surface energy. High-energy surfaces, such as freshly cleaned metals or glass, degrade quickly because their strong reactivity accelerates oxidation and contaminant adsorption **(Figure 6)**. Low-energy surfaces, such as untreated polyethylene or polypropylene, change more slowly and may exhibit minimal measurable decay **(Figure 7)**.

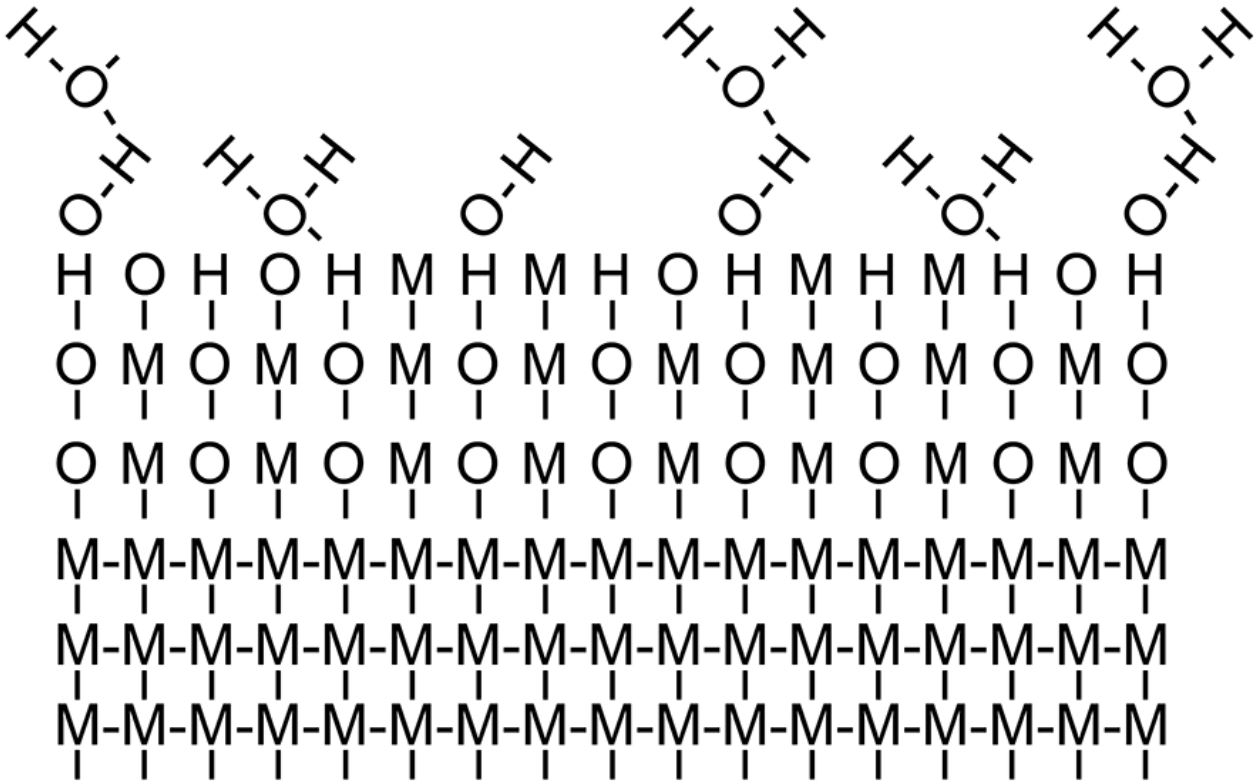

Figure 6. Chemical structure of an air-exposed metal surface composed of high-energy oxide and hydroxide groups*along with small amounts of adsorbed water.

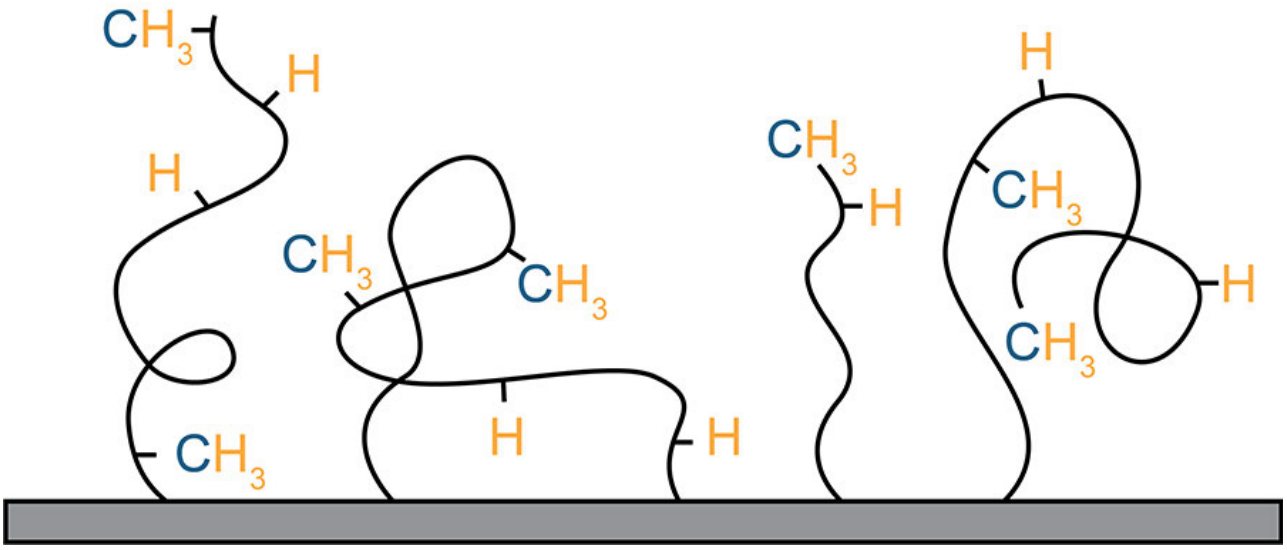

Figure 7. Illustration of a low-energy polymer surface composed of non-reactive hydrocarbon molecules.

Figure 8 shows the exponential decline in surface energy over time for freshly cleaned metal. Immediately after cleaning, the surface reacts rapidly with oxygen and water vapor to form a thin oxide layer, followed by slower adsorption of airborne hydrocarbons. Glass undergoes similar degradation as moisture and environmental chemicals react with its surface to form a silica film or alkali-rich layer. To maximize bond strength, adhesives or coatings should be applied promptly after surface preparation, before these changes compromise wetting and adhesion.

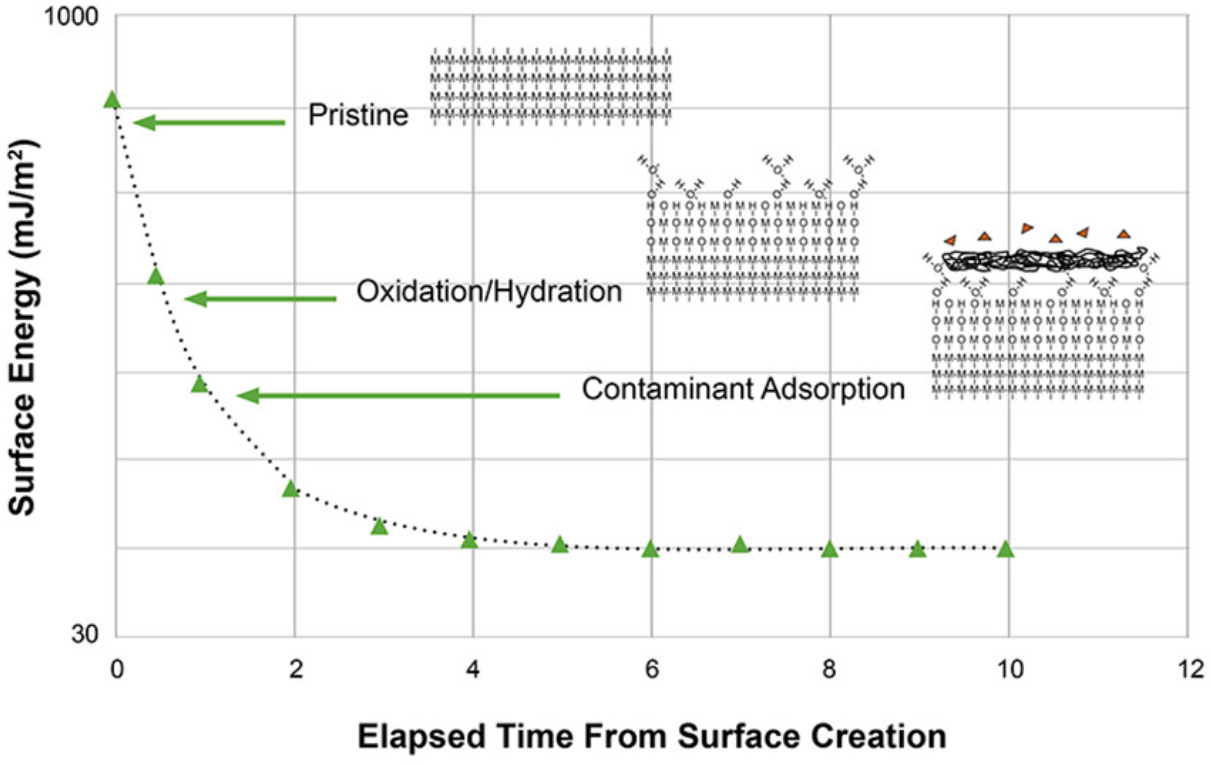

Figure 8. Surface energy decay of a freshly cleaned metal (no time scale is included because reaction rates depend on the environment).

Using contact angle to monitor surface energy changes. Water contact angle is highly sensitive to small

changes in surface energy. Even slight contamination or oxidation from surface aging can increase the contact angle, indicating reduced wettability and an increased risk of bond failure. Because such shifts can affect whether an adhesive forms a durable bond or fails prematurely, contact angle measurement serves as both a convenient diagnostic tool and an essential process-control method for verifying surface readiness and predicting adhesion performance.

Adhesive Curing Comparison

Different adhesive chemistries possess distinct curing mechanisms that influence how they interact with surfaces. Understanding these differences is important to achieving reliable adhesion.

- **UV-curable acrylates and epoxies.** These adhesives cure rapidly on demand, supporting high-throughput manufacturing with minimal thermal stress on components. Their adhesion, however, is highly dependent on surface preparation. Even slight contamination can significantly reduce bond strength. When paired with clean, high-energy substrates, UV-curable adhesives form strong, reliable bonds very quickly.
- **Two-part (2K) epoxies.** These adhesives cure through chemical crosslinking, creating strong bonds with excellent thermal and chemical resistance. Most conventional formulations require clean, well-prepared surfaces to ensure reliable adhesion. Some specialized 2K systems are engineered to tolerate modest variations in surface cleanliness and surface energy, however. Their chemistry permits them to absorb and displace small amounts of moisture and contaminants during curing.
- **Silicone adhesives and sealants.** Silicones feature a flexible siloxane backbone that provides exceptional elasticity, thermal stability and environmental durability. While they adhere to many substrates, their ultimate bond strength is limited by their low surface energy and low cohesive strength, making them best suited for applications requiring high flexibility. Silicones are highly sensitive to surface contamination. Even thin films of oil, mold-release agents, or residue can inhibit wetting and compromise adhesion, underscoring the critical importance of surface cleanliness.

Adhesive Performance Study

Taking into consideration all the nuances and interactions with substrate surfaces and adhesives previously discussed. Dymax, a global manufacturer of advanced adhesives and coatings, partnered with Brighton Science, a leader in surface intelligence technologies, to conduct a structured investigation to quantify the correlation between substrate surface energy and water contact angle with adhesive performance.

Experimental Setup

Four adhesives commonly used in electronics manufacturing were tested:

1. UV-curable acrylate – single-component, translucent, acrylated urethane chemistry
2. UV-curable epoxy – single-component, opaque, epoxy-based chemistry

3. RTV silicone – single-component, room-temperature-vulcanizing, silicone-based chemistry
4. 2K epoxy – two-component, room-temperature-curing, epoxy-based chemistry.

Two substrates frequently used in electronics manufacturing were evaluated:

1. Polycarbonate (PC)
2. FR-4 glass fiber-reinforced epoxy laminate.

The following techniques were used to prepare substrates for bonding:

1. As-received (no treatment)
2. Kimtech isopropyl alcohol (IPA) solvent wipes
3. Plasma treatment (bonded within minutes of treatment)
4. Aged plasma treatment (bonded after 24 hr. storage).

Surface energy was assessed using water contact angle measurements taken prior to adhesive application. Multiple independent point-to-point measurements were taken for each test condition to verify consistency across the surface.

Single-lap joint specimens were prepared by bonding PC to FR-4 for each combination of surface preparation method and adhesive system. All samples were tested according to ASTM D1002, the standard tensile test method for determining shear strength of adhesively bonded joints. Five replicates were produced for each test condition.

Experimental Results

Figures 9 and **10** present water contact angle measurements for PC and FR-4 across different surface preparation methods. The spread within each data group reflects the variability in contact angle for that condition, for comparison of the uniformity and consistency of surface energy across the substrate.

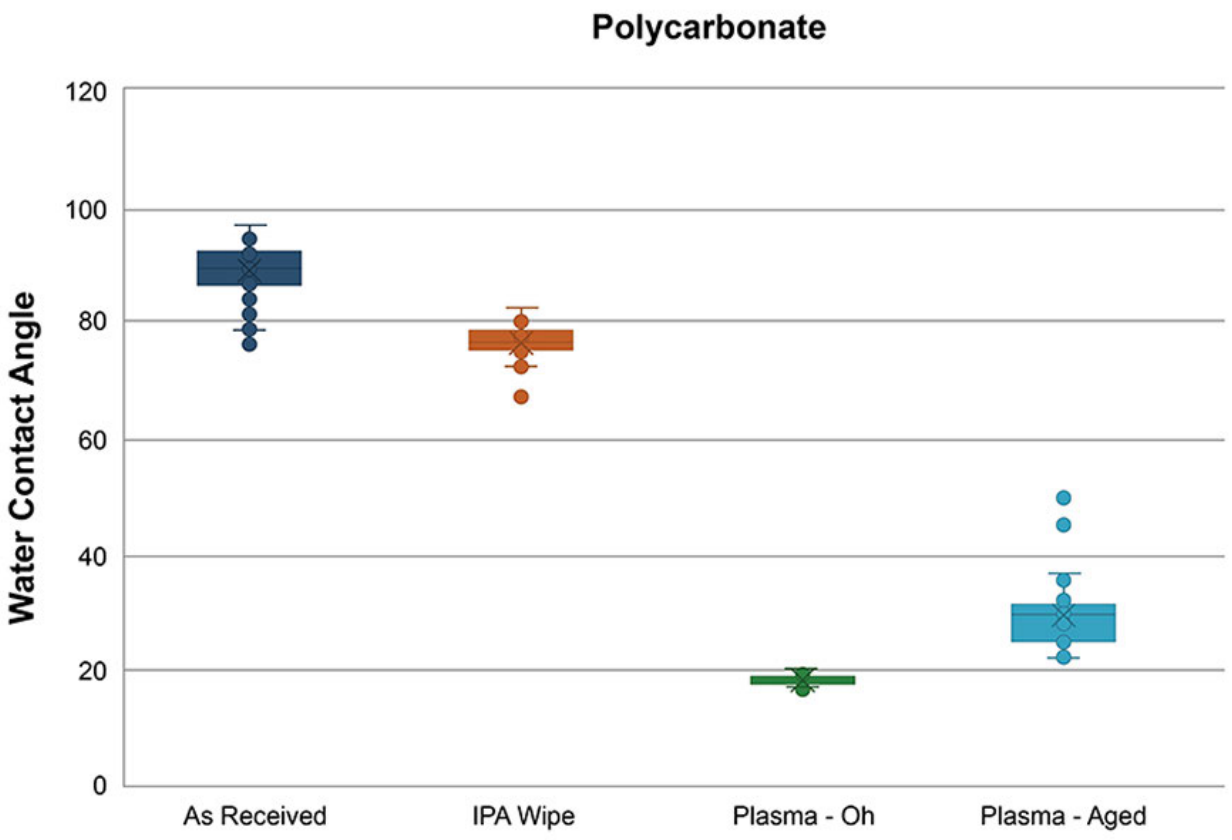

Figure 9. Polycarbonate contact angles by surface preparation method.

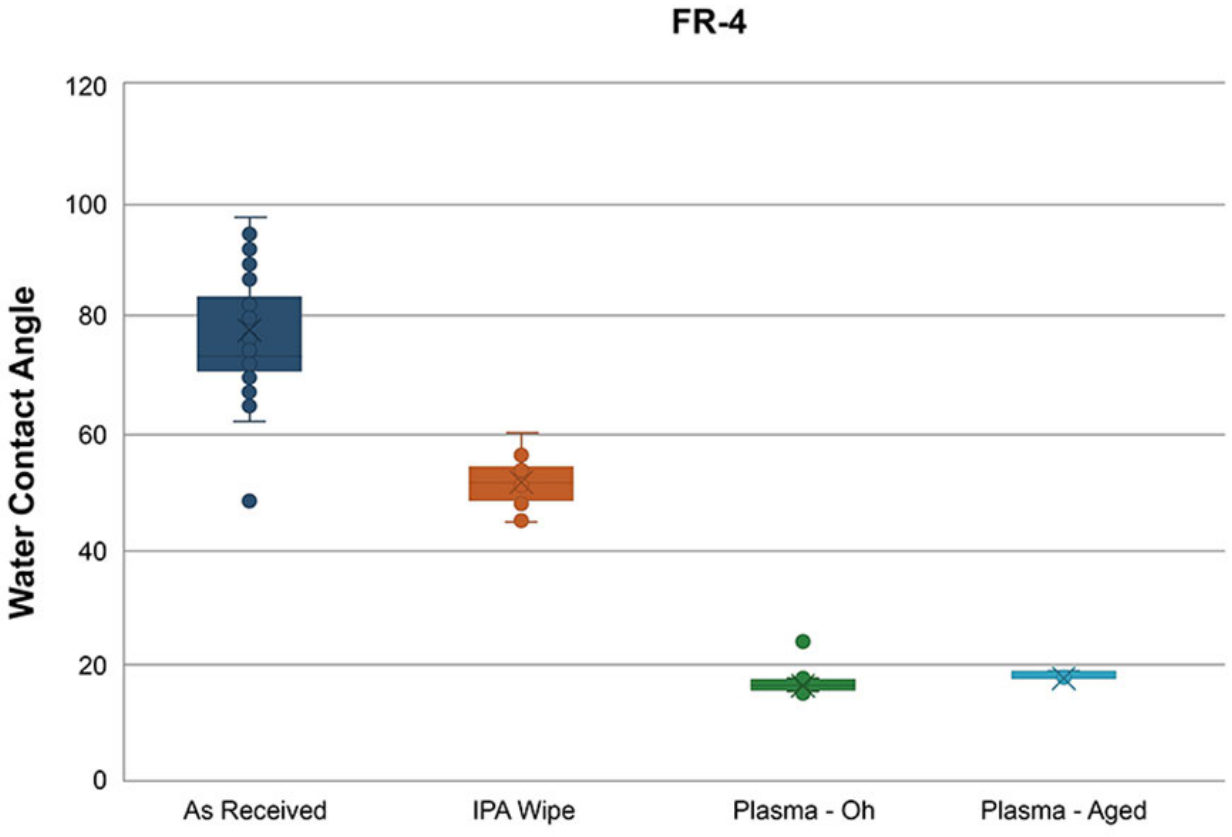

Figure 10. FR-4 contact angles by surface preparation method.

Water contact angle assessment.

- As-received surfaces showed the highest contact angles (around 80°) with significant point-to-point variability, reflecting inconsistent levels of contamination from handling and storage. These elevated values suggest a high likelihood of poor adhesion.
- IPA wiping produced a measurable reduction in contact angles across both substrates, indicating that IPA-soluble contaminants were removed. Contact angles were still high (above 50°), however, suggesting that IPA cleaning alone may not be sufficient to achieve strong adhesion.
- Plasma treatment generated the largest decreases in contact angle compared to untreated specimens, falling below 20° for both polycarbonate and FR-4. These low values indicate a surface highly favorable for bonding.
- Aged plasma treatment displayed a noticeable increase in contact angle, demonstrating that plasma-activated surfaces quickly react with the environment and lose surface energy during storage.

Figures 11 to **14** show that water contact angle correlates with lap shear strength for polycarbonate bonded to FR-4 across all adhesive systems and surface preparation methods. **Figure 15** consolidates these results, comparing lap shear strength across all adhesives and surface conditions tested.

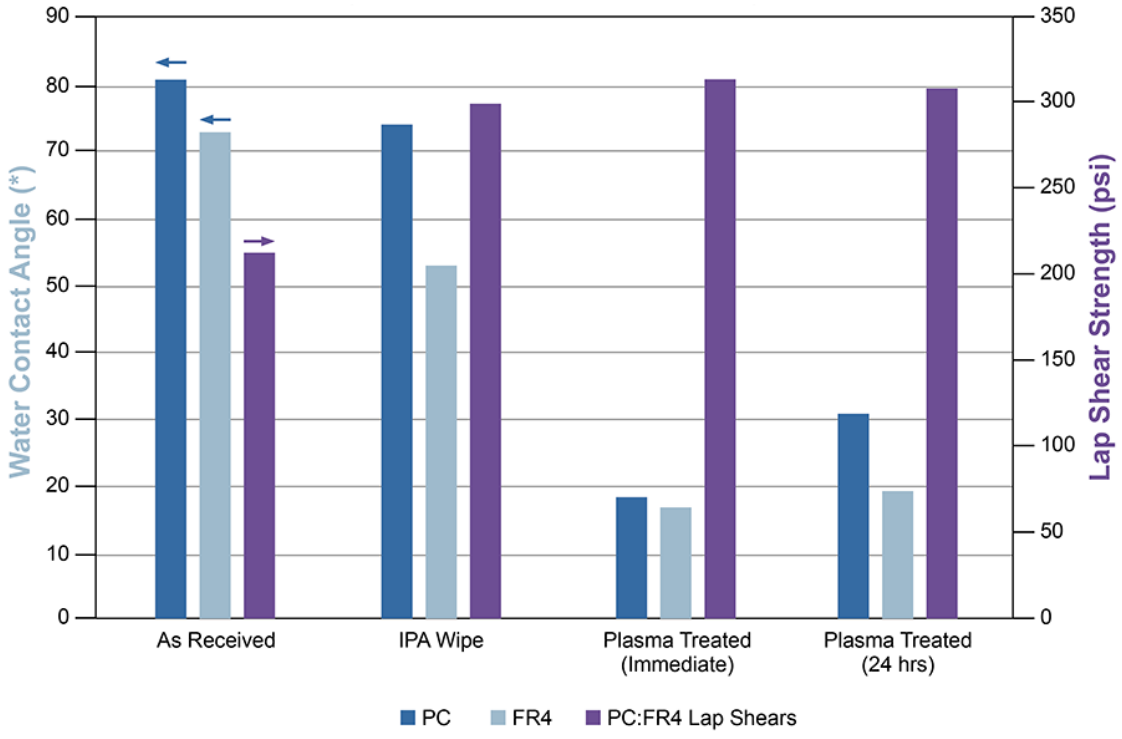

Figure 11. Effect of water contact angle and adhesion strength after various substrate surface treatments (Adhesive: UV epoxy; substrates: PC:FR-4)

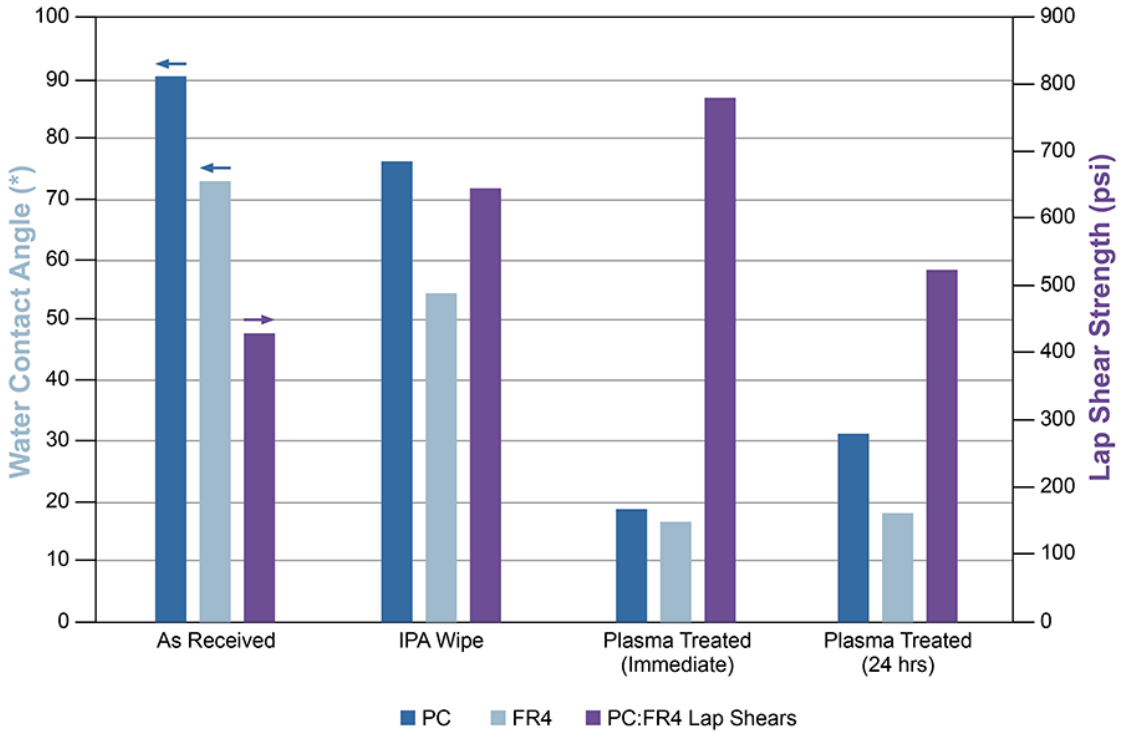

Figure 12. Effect of water contact angle and adhesion strength after various substrate surface treatments (Adhesive: UB acrylate; substrates: PC:FR-4)

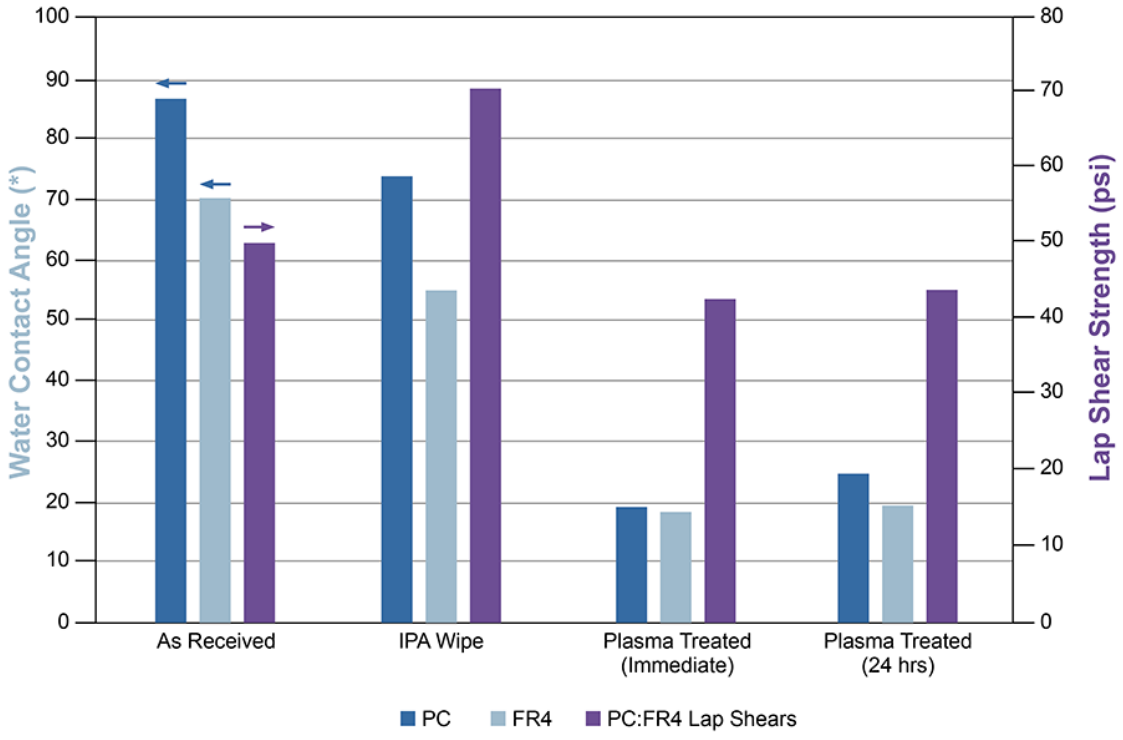

Figure 13. Effect of water contact angle and adhesion strength after various substrate surface treatments (Adhesive: 1K silicone; substrates: PC:FR-4)

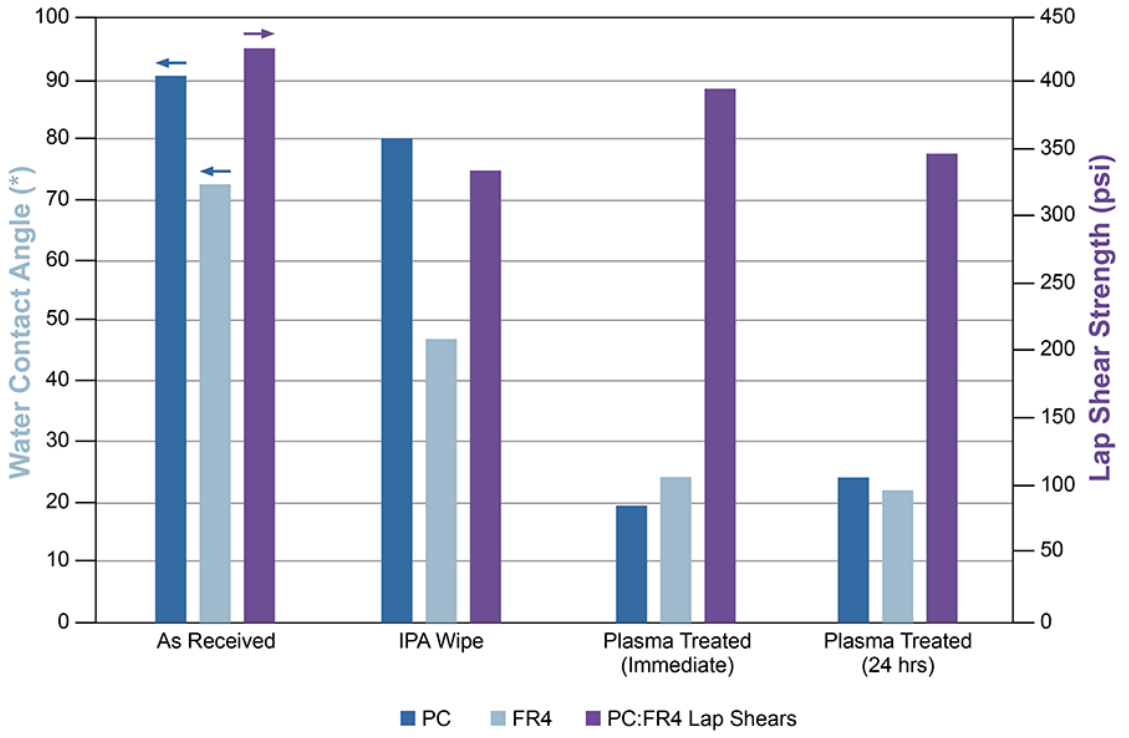

Figure 14. Effect of water contact angle and adhesion strength after various substrate surface treatments (Adhesive: 2K epoxy; substrates: PC:FR-4)

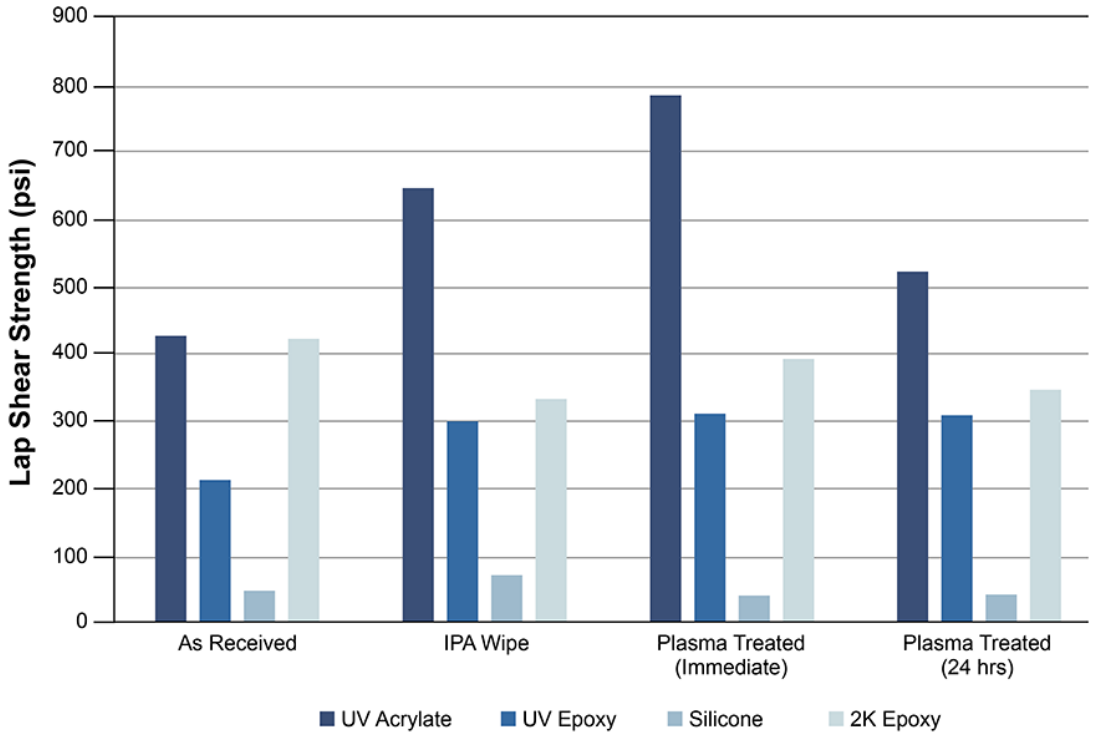

Figure 15. Adhesive chemistry comparison after surface preparation (PC/FR-4 lap shears)

Bond strength vs. surface preparation technique.

- UV-curable acrylate showed the most pronounced improvements with surface cleaning, with bond strength

increasing in a clear stepwise manner as contact angle decreased. This indicates a strong sensitivity to surface cleanliness. When bonding was delayed 24 hours after plasma treatment, lap shear strength dropped by an average of 33%, confirming the time-dependent decay of surface activation.

- UV-curable epoxy demonstrated a similar trend, with bond strength improving as surface energy increased, though the effect was less pronounced than with the acrylate adhesive. Plasma treatment yielded the highest bond strength, but the overall gain was smaller than that of the acrylate system.
- RTV silicone showed only modest improvements in bond strength with surface treatments. IPA wiping produced the most noticeable gain, while plasma treatment provided little to no measurable benefit. This behavior reflects silicone's inherently low surface energy and limited cohesive strength, both of which reduce the bond's tensile strength.
- Two-component epoxy demonstrated strong lap shear performance across all surface conditions, including the as-received baseline. This suggests the adhesive is not highly dependent on surface activation, likely due to its inherent tolerance for minor surface contamination. Notably, bond strength decreased slightly after cleaning, indicating that surface treatments may have unintentionally reduced surface energy or otherwise altered the substrate in a way that diminished adhesion.

Conclusions and Recommendations

This study demonstrated a strong relationship among the three pillars of adhesion – adhesive chemistry, process control and surface energy. In particular, it showed a clear correlation between surface energy and bond strength, where lower water contact angles (indicating higher surface energy) consistently produced stronger bonds. Even modest increases in contact angle after only 24 hr. of surface aging measurably reduced bond performance, highlighting the value of surface energy assessment as a predictor of bond success.

Water contact angle testing is a practical, repeatable method for verifying that surfaces are ready for bonding and is especially valuable in electronics manufacturing. FR-4 circuit boards may carry solder mask, flux or other residues that impair adhesion of underfills, conformal coatings and encapsulants. Polycarbonate components, often bonded to achieve slim form factors, can also lose bond strength when contaminants migrate during assembly. Real-time contact angle measurement provides a fast, quantitative assessment of surface bondability and serves as an early-warning process-control tool for identifying surfaces at risk of poor adhesion before bonding, helping prevent rework, scrap and field failures.

Modern hand-held instruments make contact angle testing practical even in high-volume production. These devices dispense and analyze microdroplets of ultra-pure water within seconds, providing operators and quality engineers an immediate means to validate cleaning effectiveness or detect contamination. When the contact angle is correlated with mechanical metrics such as lap shear strength, manufacturers can establish quantitative specifications for surface cleanliness and treatment, thereby supporting statistical process control and more consistent bonding outcomes.

Adhesive manufacturers can help put these strategies into practice to improve bond performance and ensure long-term adhesion reliability. Backed by decades of formulation and application expertise, adhesive manufacturers can:

- Troubleshoot bonding challenges
- Recommend the most suitable adhesive for the application
- Suggest appropriate surface preparation methods
- Provide detailed processing guidelines and training

By combining data-driven surface characterization with advanced adhesive technologies and expert technical support, electronics manufacturers can achieve reliable, high-performance bonds in demanding applications – from automotive and aerospace electronics to medical and industrial systems – even as devices become smaller, more functional and more complex.

Acknowledgments

The authors would like to extend their sincere thanks to the following individuals for their assistance with data collection: Kaitlin Carroll, Fran Schute, Joann Hilman, Lauren Ratliff, Gail Blanco, Matthew Hontanosas, Emma Busch, Brett Fellows and Chris Siroonian.

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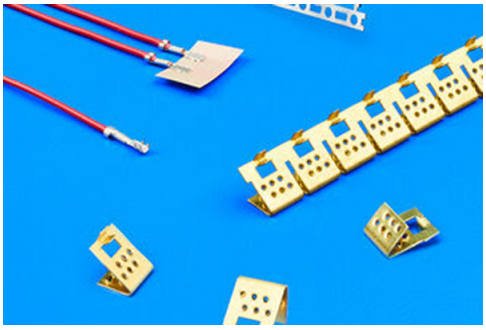
PCD&F

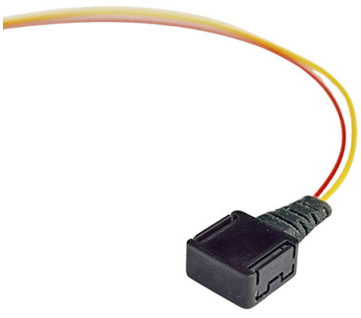


ETCO TFC AND FWC SERIES FLEX CIRCUIT CONNECTORS

TFC and FWC series flex circuit connectors are designed for attaching lead wires to flexible circuits and laminates used in space-constrained or dynamic applications. Use lances that embed into aluminum- or copper-foil and film laminates and terminate to lead wires using an F-crimp. Intended for flex circuits that bend, fold or move during operation in consumer, medical, aerospace and military electronics. TFC series supports thin films measuring 0.01"–0.025" with 18–22AWG wire, while FWC series supports foil or film laminates measuring 0.01"–0.04" with 16–22AWG wire. Both series come in brass or tinned high-brass and are supplied in strip form for automated production.

ETCO Inc.

etco.com



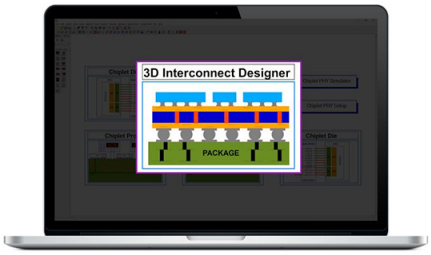
INNEOS CHEETAH 25G OPTICAL TRANSCEIVER

Cheetah 25G optical transceiver is built on the company's OptoBGA platform and supports high-speed data transmission in applications where copper interconnects face limitations related to electromagnetic interference, weight, power and system cost. Designed for systems requiring 25G connectivity across wide temperature ranges

and harsh operating environments. Supports high-volume assembly processes while maintaining signal integrity at high data rates.

Inneos

inneos.com

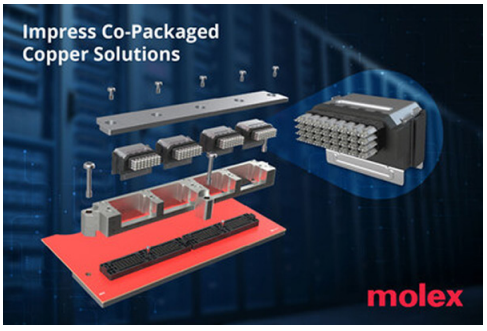


KEYSIGHT 3D INTERCONNECT DESIGNER

3D Interconnect Designer software supports design of complex interconnect structures in chiplet and 3-D IC packages used in AI infrastructure and data center applications. Addresses manual optimization challenges in multi-die and stacked-die designs, including vias, transmission lines, solder balls and micro-bumps. Supports advanced geometries such as hatched and waffled ground planes used in silicon interposers and bridge-based architectures. Validates designs against emerging standards including UCIe and BoW and incorporates electromagnetic-based simulation for electrical analysis of PCB- and package-level 3-D interconnect structures.

Keysight Technologies

keysight.com



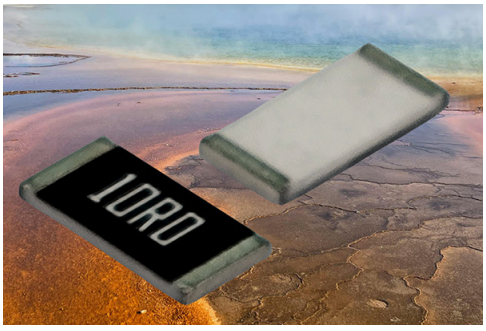
MOLEX IMPRESS CO-PACKAGED COPPER SOLUTIONS

Impress Co-Packaged Copper Solutions is a compression-based connector and cable assembly for near-ASIC connectivity in high-speed data center systems. Supports data rates up to 224Gbps PAM-4 and is intended for next-generation AI and hyperscale computing architectures. Places connection interface directly on ASIC package

substrate to reduce signal path length through PCB. Two-piece system consists of compression-attached socket and mating cable assembly designed to manage signal integrity and power distribution in high-density environments. Compression attachment minimizes substrate stress and supports maintenance or rework. Enables 1.6T and 3.2T networking transitions in AI and cloud infrastructure environments.

Molex

molex.com

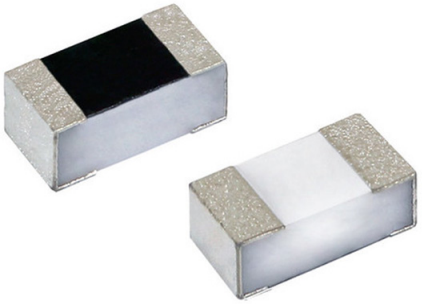


STACKPOLE RNCA RESISTORS

RNCA Series AEC-Q200 qualified thin-film chip resistors offer anti-moisture and anti-sulfur performance, for automotive applications. Are said to cut failure rates by a factor of 10 or more compared to conventional thin-film resistors while meeting automotive qualification requirements.

Stackpole Electronics

seielect.com



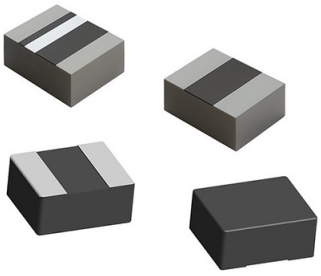
VISHAY CRCW0201-AT E3 RESISTORS

CRCW0201-AT e3 series AEC-Q200 qualified thick-film resistors come in 0201 case size measuring 0.6mm × 0.3mm × 0.23mm. Designed to reduce PCB space requirements by approximately 50% compared to 0402 components. Provide a power rating of 0.05W at +70°C, maximum operating voltage of 30V and operating temperature range of -55° to +155°C. Resistance values range from 10Ω to 1MΩ, including a 0Ω jumper option, with tolerances of ±1% and ±5%

and temperature coefficient of ±200ppm/K.

Vishay Intertechnology

vishay.com



VISHAY IHLL AND IHLP SERIES POWER INDUCTORS

IHLL (commercial grade) and IHLP (AEC-Q200 automotive grade) power inductors come in 0806 and 1210 case sizes. Include IHLL-0806AZ-1Z, IHLL-1210AB-1Z, IHLP-0806AB-5A and IHLP-1210ABEZ-5A models supporting inductance values from 0.22µH to 4.70µH with typical DCR as low as 6.6mΩ. Operate at temperatures up to +165°C. Use composite powdered-iron construction that fully encapsulates windings. Automotive versions feature side-plated terminations to support solder fillets and inspection, while commercial versions use bottom-only terminations.

Vishay Intertechnology

vishay.com

VISHAY RCA-SR E3 THICK-FILM RESISTORS

RCA-SR e3 Series AEC-Q200-qualified thick-film chip resistors are for sulfur-containing environments and come in 0201, 0402, 0603, 0805 and 1206 case sizes. Provide resistance values from 10Ω to 10MΩ, including 0Ω jumpers, with tolerances of ±1% and ±5% and TCR of ±100ppm/K and ±200ppm/K. Rated for power up to 0.25W and operating voltages from 30V to 200V, with operating temperature range of -55°C to +155°C. Meet ASTM B809-25 sulfur resistance testing with maximum resistance drift of 1% after 1000hr. at 60°C and specify $\Delta R/R \leq 1\%$ after 1000hr. of rated power at 70°C. Feature protective coating and pure matte tin terminations compatible with lead-free and lead-containing solder processes.

Vishay Intertechnology

vishay.com

ADAPTSYS 3DINSPECT AUTOMATED CARRIER TAPE INSPECTION SYSTEM

3DInspect is an automated system for inspecting carrier tape pockets and generating Certificates of Conformance. Measures carrier tape dimensions and produces inspection reports automatically, reducing inspection time per reel from up to 30min to approximately 1min. Replaces manual inspection and documentation processes. Can be used as a standalone inspection tool or integrated into tape-and-reel operations.

Adaptsys Group

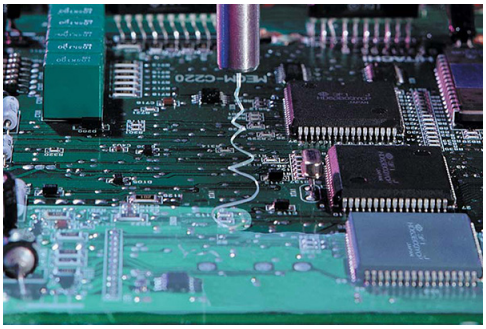
adaptsys.com

COUNT ON TOOLS LARGE-FORMAT VACUUM NOZZLE

Large-format vacuum nozzle is designed for Yamaha YRM pick-and-place platforms to improve handling stability and pickup reliability for larger and heavier SMT components in high-mix production environments. Features a 25mm base diameter to increase surface contact during vacuum pickup and is precision-machined to fit ANE locations 64, 66 and 68. Includes 15mm O-ring.

Count On Tools

cotinc.com



HENKEL LOCTITE STYCAST UV 7998 CONFORMAL COATING

Loctite Stycast UV 7998 solvent-free conformal coating provides UL 94 V-0 flame retardancy for printed circuit boards and components. Protects against moisture, dust, chemicals and other contaminants. Offers self-leveling behavior, wetting and uniform coverage without voiding. Cures within seconds under UV light, followed by a secondary moisture cure. Formulation is solvent- and VOC-free.

Henkel
henkel-adhesives.com

INSPECTIS HD-124-WUV DUAL WHITE & UV RING LIGHT

HD-124-WUV Dual White & UV Ring Light is for use with digital microscope systems. Integrates 32 white LEDs and 8 high-power UV LEDs arranged in dual rings for sequential or independent illumination control. Features integrated on/off switch, electronic dimmer and dedicated UV and segment control switches to adjust lighting zones. Powered directly through the digital microscope to reduce cable management. Includes detachable diffuser with optional polarizer/analyzer filter kit available.

Inspectis
inspect-is.com

KOH YOUNG REVOLUTION TO SUCCESS (RTOS) INSPECTION SOFTWARE

Revolution to Success (RtoS) inspection software platform unifies programming, review, analytics and process optimization within a single operating environment. Designed to manage inspection data more efficiently and consolidate inspection functions into one interface. Supports integration across AI-powered inspection systems, including closed-loop optimization in printing and placement processes.

Koh Young

kohyoung.com

KURTZ ERSA HR 600 XL HEATING HEAD

HR 600 XL heating head supports controlled rework of large-format and high-density assemblies. Designed for BGAs, QFNs, connectors and complex components. Integrates with vision alignment and process control to deliver repeatable thermal profiles.

Kurtz Ersa

kurtzersa.com

KURTZ ERSA I-CON TRACE NETWORKED SOLDERING STATION

i-CON TRACE soldering station provides traceability, IoT connectivity and IPC CFX certification for hand soldering operations. Captures process data to support quality documentation, compliance requirements and connected factory integration.

Kurtz Ersa

kurtzersa.com

KURTZ ERSA VERSAFLEX 2.0 SELECTIVE SOLDER MODULE

VersaFlex 2.0 selective solder module enables independent, parallel processing of two PCBs within a single system. Supports automatic nozzle changing and matrix-controlled preheating to improve throughput, setup consistency and

repeatability in high-mix production environments.

Kurtz Ersa

kurtzersa.com

MAGNALYTIX OE IN A BOX OBJECTIVE EVIDENCE KIT

OE in a Box is an objective evidence kit designed to support J-STD assembly cleanliness and reliability validation. Consolidates materials required for surface insulation resistance testing and objective evidence generation, including B-52 Legacy 2 SIR test cards, components and supporting materials, into a single package. Intended to streamline objective evidence workflows and align with third-party validation and reporting requirements used in assembly qualification and compliance programs.

Magnalytix

magnalytix.com

OM DIGITAL SOLUTIONS TG-7 INDUSTRY NY-TGV SUPER ADAPTER KIT

TG-7 Industry NY-TGV Super Adapter Kit is a digital camera and microscope adapter system for digital imaging from binocular stereoscopic microscopes used in inspection, research and testing. Integrates TG-7 Industry digital camera and NY-TGV Super Adapter to enable image capture and live viewing without modification to the optical system. Supports HDMI output to external monitors, wireless image transfer and remote operation. Includes dedicated microscope adapter mode, date stamping and support for write-once memory cards for documentation.

OM Digital Solutions

om-digitalsolutions.com

In Case You Missed It

Artificial Intelligence

"The 2025 AI Index: Documenting Sociotechnical Features of Deployed Agentic AI Systems"

Abstract: Agentic AI systems are increasingly capable of performing complex tasks with limited human involvement. The vast majority of agentic AI systems disclose nothing about what safety testing, if any, has been conducted, and many systems have no documented way to shut down a rogue bot. The 2025 AI Agent Index documents the origins, design, capabilities, ecosystem, and safety features of 30 prominent AI agents based on publicly available information and correspondence with developers. (MIT, February 2026, https://aiagentindex.mit.edu)

EMI Shielding

"Quad-Band Metamaterial Absorber with High Shielding Effectiveness Using Bold X-Shaped Ring Resonator"

Authors: Altaf Hussain, *et al.*

Abstract: This article presents a novel X-shaped modified split-ring resonator (MSRR) broadband microwave metamaterial absorber for covert applications in the C, X and Ku bands. The absorber features a 0.035-mm-thick annealed copper layer with X-shaped resonators on a 1.6-mm-thick FR-4 dielectric substrate, with a unit cell of $0.254\lambda \times 0.254\lambda$ at 7.64GHz. CST Microwave Studio simulations show absorption peaks at 7.64GHz (98.4%), 8.41GHz (97%), 11.4GHz (99.2%), and 12.66GHz (99%). Parametric analyses are employed to optimize these frequencies using E-field, H-field, and surface current distributions. The design achieves high absorption for transverse electric (TE) and transverse magnetic (TM) polarization across incidence angles up to 30°, ideal for electromagnetic interference (EMI) shielding and stealth in military contexts. *(Journal of Electronic Materials,* Nov. 7, 2025; https://link.springer.com/article/10.1007/s11664-025-12512-3)

Flexible Electronic Devices

"Flexible Electronics in Robotics Systems: From Devices to Applications"

Authors: Xuyang An, *et al.*

Abstract: The rapid advancement of flexible electronic technology has enabled the creation of diverse, innovative flexible devices, greatly facilitating the development of next-generation intelligent robots. Specifically, the integration

of such advanced flexible electronics into robotic systems has significantly enhanced human–robot interaction, improved the level of intelligence of robots, and refined their operational performance. These breakthroughs span various aspects of robotics and reveal substantial application potential. In this review, the authors categorize flexible electronic devices based on their functional roles and systematically summarize the latest progress in the development of novel flexible electronic components. Furthermore, they conduct in-depth analyses of innovative applications of flexible electronic devices in robotic command input, intelligent decision-making, and the enhancement of manipulation performance. The review comprehensively demonstrates the considerable improvements that flexible electronics bring to intelligent robotic systems. It is hoped that the review can offer valuable insights and inspiration for the future development of flexible electronic devices and novel applications in intelligent robotics. *(SmartBot,* Jan. 24, 2026; https://onlinelibrary.wiley.com/doi/10.1002/smb2.70017)

Memory

"8-Layer Vertical Filament-Free Bulk RRAM with High Dynamic Range and Energy Efficiency for 3D Multilevel Compute-in-Memory"

Authors: Yucheng Zhou, *et al.*

Abstract: Bulk switching RRAM technologies have been developed to address nonidealities of filamentary RRAM for embedded compute-in-memory applications. However, high-density 3D integration and scalability to nano regime have yet to be experimentally demonstrated. Here, the authors present a scalable, filament-free 3D 8-layer vertical bulk RRAM (b-RRAM) technology optimized for embedded compute-in-memory (CIM) applications. This forming-free device features reliable cycling, multi-level switching, and enhanced speed via hydrogen doping. Guided by multiscale device simulations to optimize the switching stack, the authors demonstrate 40×40nm² b-RRAM cells with MΩ-level resistance and current nonlinearity, enabling accurate, energy-efficient matrix-vector multiplications (MVM) in selector-less crossbars. A hyperdimensional computing-based continual learning algorithm is implemented on 3D b-RRAM for edge AI tasks, achieving ~90% accuracy – comparable to high-precision floating-point (FP) baselines – while delivering substantial energy savings. (IEEE International Electron Device Meeting, December 2025; https://iedm25.mapyourshow.com/8_0/sessions/session-details.cfm)

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