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PCEA
PO BOX 237
PORTSMOUTH, NH 03802

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CIRCUITS ASSEMBLY
pcdandf.com
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MANAGEMENT

PRESIDENT
Mike Buetow 617-327-4702 | mike@pcea.net

VICE PRESIDENT, SALES & MARKETING
Frances Stewart 770-361-7826 | frances@pcea.net

PCD&F/CIRCUITS ASSEMBLY EDITORIAL

MANAGING EDITOR
Ryann Howard 912-803-9780 | ryann@pcea.net

CONTENT ARCHITECT
Andy Shaughnessy 770-315-9901 | andy@pcea.net

COLUMNISTS AND ADVISORS

Jeffrey Beauchamp, Dan Beaulieu, Peter Bigelow, Robert Boguski, John Burkhert, Jr., Stephen Chavez, Mark Finstad, Geoffrey Hazelett, Nick Koop, Jake Kulp, Alun Morgan, Susan Mucha, Greg Papandrew, Hemant Shah, Chrys Shea, Jan Vardaman, Gene Weiner

PRODUCTION

ART DIRECTOR & PRODUCTION
blueprint4MARKETING, Inc. | production@pcea.net
Nathan Hoeller | nathan@pcea.net

SALES

VICE PRESIDENT, SALES & MARKETING
Frances Stewart 770-361-7826 | frances@pcea.net

SENIOR SALES EXECUTIVE
Will Bruwer 404-313-1539 | will@pcea.net

EVENTS/TRADE SHOWS

EXHIBIT SALES
Frances Stewart 770-361-7826 | frances@pcea.net

TECHNICAL CONFERENCE
Mike Buetow 617-327-4702 | mike@pcea.net

WEBINARS
Andy Shaughnessy 770-315-9901 | andy@pcea.net

EVENTS MANAGEMENT
Leah Spinks 912-239-7730 | leah@pcea.net

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No Shortcuts to Success

NOT TO BEAT a dead horse, but we've been speaking the past few months about corporate mergers and the intersection between academia and industry, and while these are separate topics, to be sure, I am motivated to continue both conversations.

In the wake of Cadence's acquisition of EMA Design Automation, I warned of the risks to EMA's customer-centric culture as it assimilates into its new parent. I also pointed out the possibility that the investment in EMA's novel tools could wane: a $5 billion company might not see value in supporting products that, in their entirety, might be worth less than a single average-sized customer.

There's a bigger issue, however. Every growth company has talent, and that talent sometimes gets lost in the mix of the larger entity.

To be sure, I'm not speaking directly to the Cadence-EMA integration. Rather, there is a long industry tradition of M&A in which the acquired company does not mesh with its new ownership. The reasons vary, of course: personality conflicts, lack of product synergy, territorial disputes, and so on. But the opportunity remains for all the creativity and talent of the smaller ones to disappear in short order.

Raise your hand if you remember some of the smaller companies that have been bought by larger ones in this space, only to be bought back by their founders for pennies on the dollar a few years later. And that goes not only for ECAD suppliers but also for fabricators and EMS companies as well.

If electric potential (V) can be defined as $V = W/q$, where W is the work done to move the charge (q), then perhaps the failure to achieve *business* potential could be $V_f = W/I$, where P_f is the *failure* to achieve potential, W is the work done divided by the initiative (I) to begin and complete that work. The lack of initiative dooms these deals. And that missing element is generally a management failure, whereby leadership ignores the very basic process of setting goals and establishing objectives that are aligned with those goals for both the incoming workers and their new colleagues.

We are in the midst of an exciting time for startups, mostly in the ECAD and OEM spaces. The rapid appearance of so many new and relatively well-funded companies is at once exciting and concerning, since we've seen this play before and know how it ends. Most of them won't make it; they will fail because their business model is weak, their sales team is lacking, or their offering is undifferentiated versus the competition (or just plain doesn't work). Some of the "lucky" ones will be bought, possibly on great terms for their founders and investors. And when that happens, a generation of entrepreneurship and new energy will disappear.

Let's not let that happen again. We need these new bright minds and the teams they put together to stick around for a change. No one knows their business like a founder – and no one has their passion to make it a reality.

Some acquirers look at their new colleagues as barbarians at the gate to the castle. Management might want to look a little deeper: The worst case is to spend a lot of money on something and be left with nothing to show for it.

On the topic of having nothing to show for your investment, among the considerable masses we had the pleasure of meeting at PCB East this year (attendance grew 48% year-over-year) were a few college undergraduates.

And while last month I questioned an industry that on the one hand agonizes over the lack of interest from the younger generation while simultaneously giving the Heisman to the opportunity to actually, you know, show that generation what we do, it cuts both directions.

To wit: The schools that are compromising their students' education by putting expediency above quality. We met at PCB East with some wonderful and creative students who are taking a class on PCB design administered through their college. And it was discouraging to hear how little interaction they are receiving from their instructor, and how limited their instruction has been. For instance, while they showed us a board they had developed, they were unfamiliar with basic elements such as fiducials and tooling holes, and made a fundamental routing mistake that any competent designer would have caught.

And therein lies the rub. Too often, programs are developed and pitched to an academic bureaucracy that simply does not have the background to assess good and bad. It's the equivalent of sending your design to the board shop on the corner with a flashlight for imaging and an electric skillet for curing (IYKYK). Instructors with no experience in board design – or sometimes, in electronics – are asked to lead classes and are heading into the semester with literally no syllabus. The students don't know the difference and ultimately are paying for an education no better than what they could have received from watching a few YouTube videos. It's a mess.

It calls for more interaction between industry and academia to ensure the latter knows what it *doesn't* know. Circuit theory is important, but it's only part of the design-to-manufacture equation. Success knows no shortcuts. Designers and engineers need to know both, and the best way to learn it is from those of us who live it every day.

mike@pcea.net
@mikebuetow

MIKE BUETOW is president of PCEA (pcea.net); mike@pcea.net.

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Cern Releases Open Source KiCad Component Library

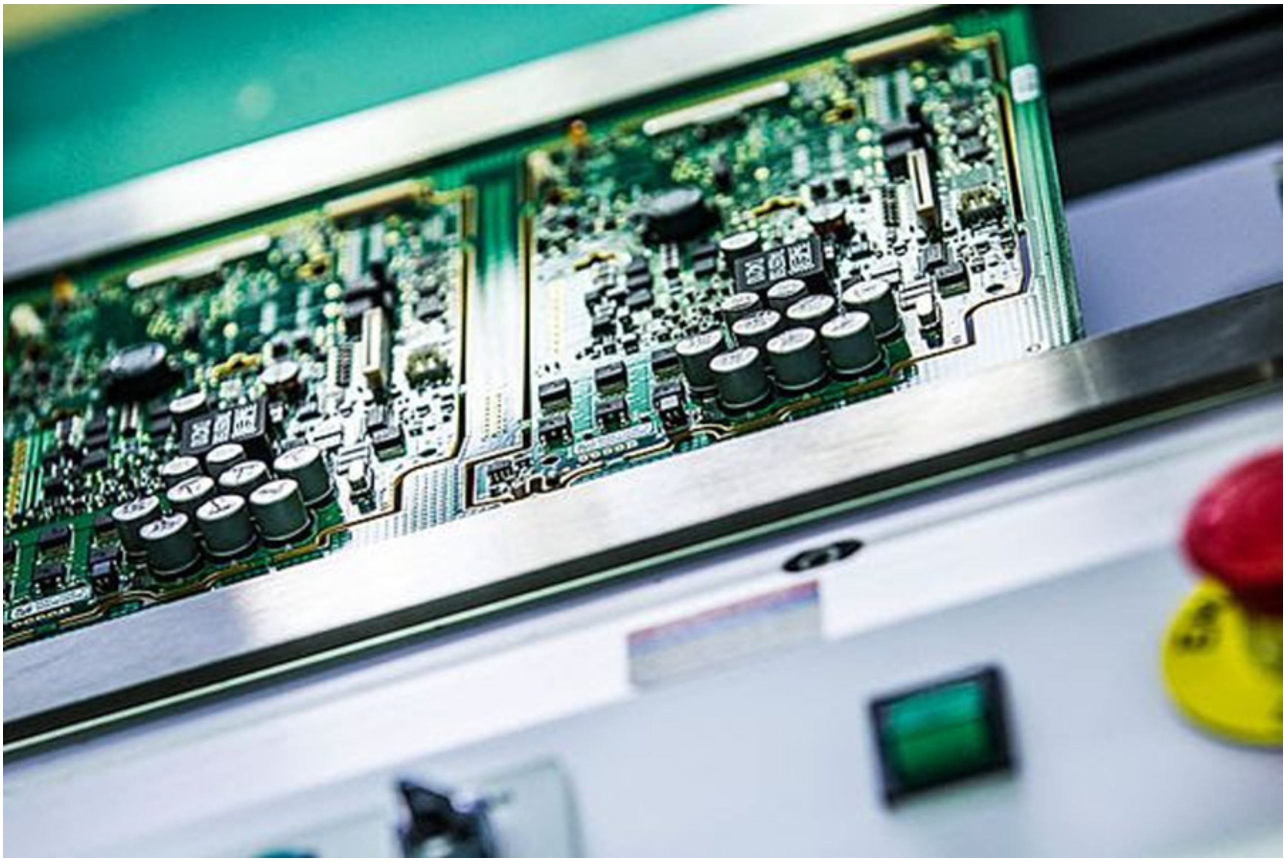
GENEVA – Cern released its complete KiCad component library under an open source license, making more than 17,000 electronic component symbols and footprints available to PCB designers worldwide.

The library supports KiCad, the open source PCB design software suite, and includes the same component resources used internally by Cern hardware designers. Cern said the release aligns with its broader open science and open hardware initiatives.

The organization added that engineers can now access, modify and redistribute the library within open PCB design workflows.

PTC Integrates Onshape with Altium for Cloud PCB Collaboration

BOSTON – PTC integrated its Onshape CAD platform with Altium to improve cloud-based collaboration between electrical and mechanical engineering teams.



PTC integrated Onshape with Altium to enable real-time cloud-based collaboration between electrical and mechanical engineering teams.

The connector enables PCB designs created in Altium to transfer directly into Onshape while synchronizing updates between both platforms in real time. PTC said the integration eliminates manual file transfers and format conversions traditionally required in ECAD-MCAD workflows.

The system supports browser-based access and is intended to improve enclosure verification, design review and engineering change management throughout product development.

Doosan Invests $135M in Thailand PCB Materials Facility

ARAYA, THAILAND – Doosan is investing approximately $135 million to establish a new copper clad laminate production facility in Thailand to support growing AI infrastructure demand.

The 73,000sqm site will produce CCL materials used in PCB manufacturing for high-performance computing and semiconductor applications. Construction is expected to begin this year, with mass production targeted for the second half of 2028.

Doosan said the investment will expand production capacity for PCB materials as AI data center demand accelerates globally.

Ventec Evaluates US Manufacturing Expansion for PCB Materials

PINGZHEN CITY, TAIWAN – Ventec International Group is evaluating the potential establishment of a US manufacturing facility focused on high-performance laminate and prepreg materials for mission-critical PCB applications.

The proposed facility would support aerospace, defense, industrial and medical markets while strengthening regional supply chain resilience and localized manufacturing capabilities. The evaluation is part of Ventec's broader "China + Taiwan Plus One" strategy aimed at diversifying production and improving supply continuity.

Comments from industry sources suggest that the laminates maker is strongly considering Arizona for the site.

The company said any final investment decision remains subject to board approval.

ASE, Wus to Team on Advanced Packaging Manufacturing Plant

KAOHSIUNG, TAIWAN – Advanced Semiconductor Engineering (ASE) and Wus Printed Circuit in May announced a strategic collaboration for the construction of a state-of-the-art manufacturing facility in the Nanzih Technology Industrial Park here. The two companies plan to jointly deploy resources to expand advanced manufacturing capacity that will reinforce Taiwan's critical position in the global semiconductor value chain.

The new facility will focus on advanced packaging processes, including fan-out chip on substrate (FOCoS) and flip chip ball grid array (FCBGA) technologies to serve the emerging AI, cloud computing and autonomous driving applications. The facility will also integrate automation and smart manufacturing processes, the companies said in a joint release.

"This landmark agreement is a strategic collaboration between ASE and WUS to improve land use efficiency and allow ASE to expand our manufacturing capacities to meet market demands," said Mike Hung, executive vice president, ASE. "We are also excited to establish a new benchmark for future collaborative industrial development."

Flex to Spin Off AI Infrastructure Business, Targets 75% Growth

AUSTIN, TX – Flex announced plans to spin off its cloud and power infrastructure segment into a standalone public company focused on AI data center infrastructure, power management and thermal technologies.

Flex plans to spin off its AI infrastructure business into a standalone public company focused on data center power and thermal systems.

The new company, referred to as SpinCo, will focus on digital and electrical infrastructure systems for AI and mission-critical applications, while Flex continues operating as an advanced manufacturing provider serving healthcare, automotive, industrial, communications and lifestyle markets.

Flex said the transaction is expected to close during the first quarter of calendar 2027. Revathi Advaithi will become CEO of SpinCo while remaining chairman of Flex during a transition period, with Michael Hartung set to take over as CEO of Flex.

The company is targeting approximately 65% to 75% revenue growth for SpinCo in fiscal 2027, accelerating to more than 80% in fiscal 2028 as AI infrastructure spending continues to rise.

Wislab EMS Buys Fremont Headquarters for $61M

FREMONT, CA – Wislab EMS purchased its headquarters and manufacturing facility in Fremont for $61 million, expanding its long-term manufacturing presence in Silicon Valley.

Property records filed May 5 show the EMS provider acquired the 126,000 sq. ft. facility through an all-cash transaction. The company said it currently employs at least 125 workers at the site and is actively hiring across engineering, procurement and manufacturing operations.

Wislab manufactures PCBs and electronics products supporting mission-critical computing, networking, storage and communications applications.

Industry Coalition Pushes Congress to Extend Semiconductor Tax Credit

WASHINGTON, DC – A coalition of 18 business and trade groups led by the Semiconductor Industry Association is urging Congress to extend and expand the Advanced Manufacturing Investment Credit beyond its scheduled 2026 expiration.

The groups called for the semiconductor production tax credit to also support semiconductor design and research and development activities. The coalition represents industries spanning semiconductors, AI, aerospace, cloud computing, wireless communications, medical technology and manufacturing.

Industry organizations said extending the incentive would encourage additional domestic investment, strengthen supply chain resilience and reinforce US competitiveness in advanced technologies.

PCD&F

AdvancedPCB installed two **Schmoll** Falcon drilling systems at its Wisconsin and California facilities.

Busan Equity Partners is reportedly renewing its bid for flex CCL maker **Nexflex**.

China Jushi will invest $653 million to expand electronic-grade glass fiber and cloth production for PCBs.

CircuitHub raised $28 million to expand its automated PCB manufacturing platform and scale AI-driven electronics production facilities across the US and Europe.

Edge and **Icape Group** signed an MoU to explore joint development and localize PCB and electronic subsystem supply within the UAE.

Gowin Semiconductor and **JLCPCB** will collaborate to offer access to FPGA devices for prototype developers.

A **Korea Institute of Machinery and Materials team** developed a roll-to-roll process enabling continuous production of large-area flexible circuit boards, improving scalability over traditional batch methods.

Lava International plans to invest $114 million over five years to expand domestic production of smartphone components including display modules, camera modules, multilayer PCBs and enclosures in India.

Renesas completed its acquisition of **Irida Labs.**

UK-based **siliXon** raised $1.5 million to develop AI tools that generate circuit board designs from text prompts.

Topoint Technology, a manufacturer of PCB drills, has reportedly secured up to $19 million in investment commitments from **Unimicron Technology, Gold Circuit Electronics** and **Zhen Ding Technology.**

CA

Absolute EMS added a **SASinno Americas** PF-6T connector press-fit system, implemented **Luminovo**

with NetSuite integration, and expanded support for LEO, MEO and GEO satellite programs.

BGA Technology added a **Creative Electron** TruView Simplex x-ray.

CE3S is now offering **Desco Industries'** Compact Static Field Meter.

Circuitwise Electronics is reportedly on the block by its owner **Quadrant Private Equity.**

Elin Electronics in May reported a controlled fire at its electronics factory in Ghaziabad, India, causing no injuries but forcing a temporary shutdown of the affected area.

Express Manufacturing added a second **TRI** 3D AXI and an **Acculogic Scorpion** 980E flying probe.

GKG appointed **Etek Europe** official distributor for its SMT printers.

H&L Instruments, a maker of optical measurement systems, has closed after 45 years.

Iljin Electronics (India) and **Sumitronics** have entered into a strategic alliance to strengthen electronics sourcing and manufacturing in India.

Javad EMS installed four **Nordson** SQ3000 AOI systems.

Lite-On Technology is eying a $300 million headquarters in the Dallas suburbs.

Nordson Test & Inspection named **Quiptech Mexico** representative in Mexico.

PCBSync, a PCB and EMS company, announced a strategic partnership with **Capital Group.**

Scanfil expanded its manufacturing partnership with **Bruker AXS**. The EMS company also announced a manufacturing agreement valued at approximately €25 million ($28 million) with an industrial automation company.

SMT Thermal Discoveries named **Etek Europe** UK representative for its convection and vacuum reflow soldering systems.

Ubersmt expanded its SMT production line with **Juki** printing and placement systems and a **Heller** MK7 reflow oven.

VJ Electronix appointed as manufacturers' representatives **The Murray Percival Co.** for Illinois and Southern Wisconsin and **MaRC Technologies** in the Pacific Northwest.

PCDF


Ramakanth Alapati


Alun Morgan


Theophile Sardain

Cyient DLM appointed **Ramakanth Alapati** president and chief strategy and growth officer.

Jiva Materials named **Alun Morgan** chief technology officer.

Newgrange Design named **Theophile Sardain** PCB design assistant.

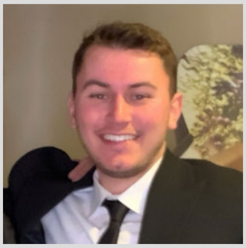
CA


Max Ramos


Tom Carrubba


Revathi Advaithi


Michael Hartung


Michael English


Kaveh Faghihi


Iiris Heiskanen


Colin Forgy


Hermes Gonzalez

Amtech Systems appointed **Thomas Sabol** chief financial officer.

Aven Tools appointed **Max Ramos** distribution partner operations manager.

Blue Origin named **Tom Carrubba** senior vice president of manufacturing operations.

Flex announced chairman and CEO **Revathi Advaithi** will become CEO of its spinoff SpinCo, and promoted president **Michael Hartung** to CEO.

Intelligent Manufacturing Solutions named **Michael English** manufacturing engineering manager.

Metal Etch Services hired **Kaveh Faghihi** as quality production coordinator.

Scanfil appointed **Iiris Heiskanen** CFO.

Semi-Kinetics appointed **Colin Forgy** manufacturing manager at its Idaho facility.

The Test Connection named **Hermes Gonzalez** test development engineer.

PCB West 2026 Conference Registration Now Open

PEACHTREE CITY, GA – PCEA opened registration in May for the technical program at PCB West 2026, featuring over 50 classes and more than 120 hours of in-depth electronics engineering training on circuit board design and assembly.

Rick Hartley, Karen Burnham, Susy Webb, Stephen Chavez, and Tomas Chester are among the headliners of this year's conference. It will be held Sept. 29 to Oct. 2 at the Santa Clara Convention Center in Santa Clara, CA. It features classes for every level of experience, from novice to expert.

Registration for both the technical conference and the exhibition takes place at pcbwest.com. Those who sign up by Aug. 21 can take advantage of the early bird special discounts for the conference.

The scope of classes ranges from the basics of design engineering, libraries and circuit grounding to more advanced fare such as power distribution, EMC, stackups, and thermal management.

More than 25 of the presentations are new to the conference, including ones for advanced dielectrics for thermal PCBs, AI, and time budgets for new projects.

"PCB West is the leading conference and exhibition for printed circuit design and manufacturing in the world," said Mike Buetow, conference director, PCB West. "It is the best place to find subject matter experts designing and building everything from popular consumer devices to the most sensitive and critical high-reliability technologies."

PCB East 2026 Attendance Up Almost 48% Over Last Year

PEACHTREE CITY, GA – Attendance for the PCB East 2026 conference and exhibition rose nearly 48% year-over-year, the Printed Circuit Engineering Association (PCEA) announced. Attendance at the technical conference was up 38%, while overall registration grew 42% from a year ago.

The annual trade show was held April 28 through May 1 at the DCU Center in Worcester, MA. In all, more than 85 leading suppliers of electronics design tools, manufacturers of bare boards and assemblies, suppliers of fabrication and assembly equipment and materials, and related industry companies exhibited at the show.

PCB East will be remembered for its new location and busy vibe.

“The East Coast market once again showed its incredible vibrancy,” said Mike Buetow, conference director and president, PCEA. “Due to demand, we moved to a larger space for 2026, which resulted in the addition of 20 more exhibitors. The industry response speaks for itself.”

“There were some great classes at PCB East 2026,” said conference attendee Paul Brydges, principal PCB designer at Evident Scientific.

“It was a great PCB East and a great week meeting old friends and making new connections,” said exhibitor Carrie Guenther, marketing manager for RBB Systems. “Thanks to PCEA for arranging such a great PCB East in a new location!”

“PCB East was a blast,” said exhibitor Brandon Bourn, founder of Zenode, which printed custom ID cards for attendees. “Over 200 people had their custom Titan card made. Countless more stopped by booth 214 to see Zenode in action.”

“It was wonderful making new connections and catching up with industry friends,” said exhibitor Jeffrey Beauchamp, director of technology and engineering with NCAB Group. "We're grateful to everyone who made PCB East such a meaningful and successful event."

PCB West 2027 will take place April 26-30, again at the DCU Center.

Lackey to Lead Flex Webinar this Month

Dave Lackey

PEACHTREE CITY, GA – Flex and rigid-flex circuit design and manufacturing expert Dave Lackey will present a free webinar for PCEA members this month.

The talk, Fundamentals of Flex and Rigid-Flex, takes place Jun. 24 from 1 to 2 p.m. Eastern. To register, click here.

The presentation will cover material selection, cost considerations, fabrication notes, design tool considerations, panel/array usage, manufacturability and much more. Whether you are starting with a simple flex design or a complex rigid-flex design, this presentation will give you a different perspective.

Lackey is vice president of business development with ASC/Sunstone, where he has worked since 2008.

Online Learning Classes Now on PCEA Site

PEACHTREE CITY, GA – PCEA now hosts its online learning platform, Printed Circuit University, on the pcea.net website. Through this addition, PCEA members have access to various training videos and other content on board design, fabrication and assembly. In addition, past chapter meeting recordings are available on the site.

Access to much of the content is free to individual members, while some extended tutorials are available via subscription.

PCEA CURRENT EVENTS

ASSOCIATION NEWS

Certification. The following recently passed the PCEA Certified Printed Circuit Designer exam:

- Carter Cailor
- Benjamin Corrington

- Alex Watson
- David Weaver

New Corporate Members

- Elsyca
- PCB Cart
- PCB Technologies

Networking. The PCEA Discord server brings together engineers and designers from around the world on a private channel to discuss technical questions and career opportunities. To join, contact PCEA. Recent conversations covered high voltage boards, reflowing through-hole components, and differential signals.

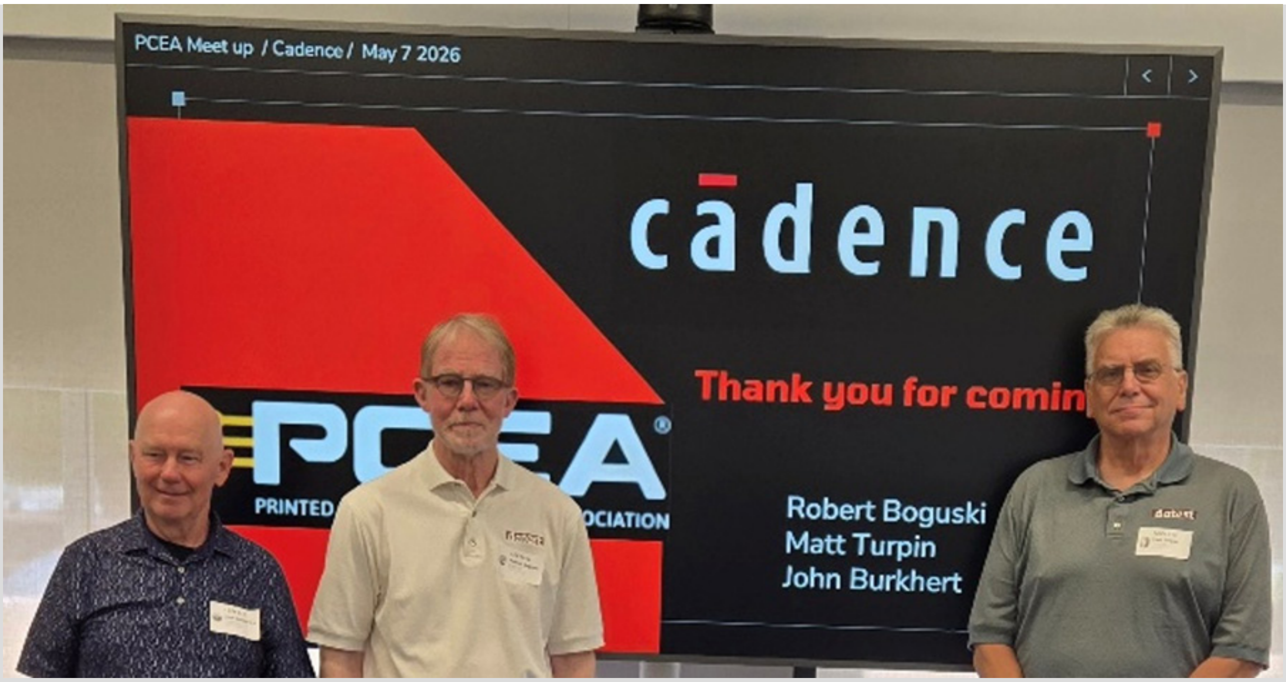
CHAPTER NEWS

National. Upcoming PCEA Training Certified Professional Circuit Designer (CPCD) training and certification classes will be held:

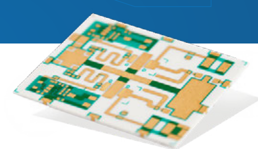
- Sept. 4, 11, 18, 25, Oct. 9
- Sept. 28 – Oct. 2 (live abridged class, taught in-person in conjunction with PCB West)
- Oct. 16, 23, 30, Nov. 6, 13

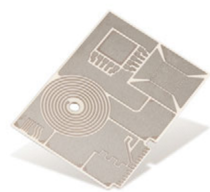
Portland, OR. The next meeting is tentatively scheduled for June 25, from 12 – 1 p.m. Pacific. Speaker and meeting link to be announced.

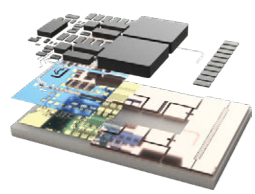
Silicon Valley. Our May chapter meeting was held on May 7 at Cadence Design Systems in San Jose. Featured speakers were John Burkhert, Jr. and Robert Boguski, both column contributors for PCD&F magazine. Burkhert talked about design for test. Boguski, along with Matt Turpin, both from Datest, talked about optimum test methods and test coverage. We also announced that Edwin El-Kareh of Albans Design will take over as chapter leader from Bob McCreight, who is retiring after leading the chapter for 20 years.



Burkhert (left), Boguski and Turpin at the Silicon Valley Chapter meeting.







AI Computing Surge Reshaping PCB Material Landscape

TAOYUAN, TAIWAN – As AI computing continues to drive a comprehensive upgrade in hardware specifications, the global printed circuit board industry is undergoing a profound structural transformation. According to a report released in May by the Taiwan Printed Circuit Association (TPCA) and the Industry, Science and Technology International Strategy Center (ITRI), the global copper-clad laminate (CCL) market is expected to exceed $21.5 billion in 2026, driven by AI demand, with annual growth projected to reach 34%.

While Taiwanese suppliers have established competitive advantages in high-speed materials and key process consumables, high-end IC substrate materials and glass fabrics remain largely dominated by Japanese manufacturers. In response to supply bottlenecks and geopolitical uncertainties, Taiwan's supply chain is accelerating high-value positioning through deeper independent R&D, further strengthening its critical role in the global AI supply chain.

In the CCL sector, strong demand from AI servers for large-format, high-layer-count PCBs with more than 40 layers and ultra-low-loss characteristics has placed the market in a strong growth cycle driven by both volume and pricing. The global CCL market reached $16 billion in 2025 and is forecast to expand sharply to $21.5 billion in 2026, supported by AI-related specification upgrades, representing annual growth of up to 34%.

As of 2025, Taiwanese suppliers held a combined global market share of 37% in this segment, with Elite Material the global leader at 19%. To address high-speed transmission requirements, Taiwanese suppliers are also actively developing next-generation materials such as low Dk2 glass fabric, quartz fabric and PTFE, aiming to strike an optimal balance between high-speed signal integrity and processing reliability, and to reinforce the material foundation for high-performance computing.

Flex circuit materials. In the flexible copper-clad laminate (FCCL) market, polyimide benefited from demand for battery management systems and advanced driver assistance systems in electric vehicles, as well as a recovery in the PC market. These factors lifted the market size to $1.01 billion in 2025. Rising memory prices have increased downstream device costs, however, and polyimide output value is projected to edge down slightly to $990 million in 2026.

In high-frequency applications, MPI and LCP remain key materials for advanced communications. Growth momentum has been constrained by moderate smartphone market expansion and design changes, however. The MPI market is forecast to reach approximately $240 million in 2026. Meanwhile, LCP, known for its ultra-low-loss advantages, saw demand decline by more than 10% in 2025 due to changes in iPhone antenna designs. Looking ahead to 2026, the market is expected to remain weighed down by weak consumer electronics demand, with overall scale estimated at around $280 million.

IC substrate materials. Japanese manufacturers continue to maintain a high level of technological dominance in semiconductor substrate materials, extending their influence to the very upstream end of the industry chain. Data for 2025 show that in the ABF substrate materials market, Ajinomoto held a 97% market share, effectively controlling a critical material supply point for global AI chip packaging.

Japanese suppliers also held more than 70% market share in BT substrate materials and low-CTE glass fabrics. Since AI applications are relatively less price-sensitive, suppliers have prioritized AI-related orders, resulting in structural supply bottlenecks. This has even begun to affect capacity allocation for automotive and traditional consumer electronics glass fabrics.

High-end raw materials. As AI servers evolve toward B300 and GB300 platforms, the PCB supply chain is benefiting from both higher value-added requirements and incremental demand growth. Taking HVLP copper foil as an example, demand for HVLP4 products with extremely low surface roughness, such as Rz 0.5µm, is rising rapidly. Driven by the AI wave, global HVLP copper foil capacity grew 48% in 2025 to 23,400 metric tons. Japanese suppliers currently account for more than 60% of supply.

At the same time, the high-layer-count and thick-board structure of AI servers has significantly increased processing complexity, directly raising technical requirements for PCB drill bits, a key process consumable. To address challenges such as chip evacuation and drill breakage, the market is accelerating its shift toward high-performance coated drill bits to enhance processing stability. As microvia drilling shortens drill-bit service life, the global drill-bit market climbed to $860 million in 2025. In 2026, supported by rising drilling volume and the high-value transformation of consumables, drill-bit output value is expected to grow 29% to $1.11 billion.

Margin Call

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	JAN.	FEB.[r]	MAR.[p]	YTD
Computers and electronics products	1.6	1.0	0.5	6.2
Computers	1.3	2.0	-0.5	17.5
Storage devices	4.9	7.7	0.9	12.2
Other peripheral equipment	6.7	10.4	-2.8	53.7
Nondefense communications equipment	5.2	1.4	3.5	21.6
Defense communications equipment	6.3	-6.0	-3.2	-0.6
A/V equipment	-1.6	-0.7	-0.9	-8.6
Components[1]	-0.1	-0.2	-0.6	4.5
Nondefense search and navigation equipment	3.8	1.8	-1.7	4.4
Defense search and navigation equipment	3.4	2.7	2.5	11.8
Electromedical, measurement and control	1.7	-0.3	-0.2	0.0

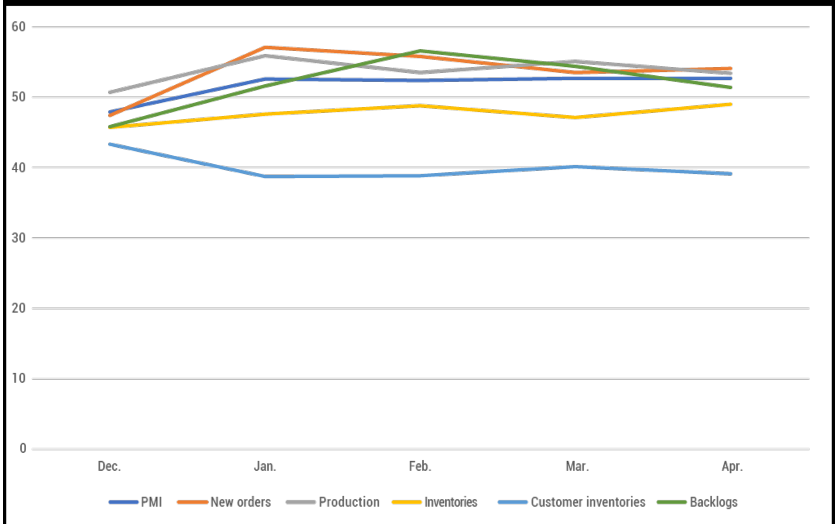
[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, May 4, 2026

Key Components

	DEC.	JAN.	FEB.	MAR.	APR.
Semiconductors[1,3]	25.6%	46.1%	61.8%	79.2%	TBA
PCBs[2,3]	1.18	1.09	1.08	TBA	1.24
EMS[2,3]	1.24	1.25	1.32	1.29	TBA
Electronics mfg. orders[2]	n/a	113.0	122.0	120.0	118.0
Electronics shipments[2]	n/a	110.0	117.0	117.0	115.0
Component sales sentiment[4]	120.1%	138.0%	139.7%	149.2%	146.6%

Sources: [1]SIA, [2]GEA, [3]3-month moving average, [4]ECIA

US Manufacturing Indices



Source: Institute for Supply Management, May 4, 2026

Hot Takes

The **AI memory chip boom** could slow by 2028 as Chinese chipmakers rapidly expand DRAM and NAND production capacity and global AI spending growth moderates. (Samsung)

Growing **shortages of advanced build-up substrates** for AI, server and networking packages are increasing as layer counts and larger substrate sizes strain industry capacity. (TechSearch International)

MLCC prices are expected to rebound due to rising demand from high-end applications and increased channel stocking activities for consumer-grade components. (TrendForce)

Global semiconductor sales reached $299 billion in the first quarter, up 25% from the fourth quarter of 2025. March sales totaled $99.5 billion, increasing 79% year-over-year and 11.5% sequentially. (Semiconductor Industry Association)

North American **PCB shipments** rose 5.8% in April from the previous year, and 15.6% sequentially. Year-to-date are up 8.9%. Bookings climbed 25.5% year-over-year and 36% sequentially, and are up 4.1% for the year. (GEA)

Growing concern over **US dependence on Chinese rare earth supplies** is increasing attention on recovering valuable magnets and materials from domestic electronic waste to support electronics, defense and AI-related industries. (Chatham House)

Global semiconductor materials revenue rose over 6% to a record $73 billion in 2025. (SEMI)

AI-driven demand for **higher-performance computing hardware** is accelerating growth in the copper-clad laminate market as Taiwan's PCB supply chain pushes to secure second-source materials capacity. (TPCA)

Global server shipments rose about 4% sequentially in the first quarter, with agentic AI driving demand for both GPUs and CPUs and boosting growth in general-purpose servers. (DigiTimes)

Global **silicon wafer shipments** rose 13% year-over-year to 3.28 billion square inches in the first quarter. (SEMI)

The top five North American cloud service providers (CSPs) will significantly increase their **procurement of rack-scale AI servers** in 2026 to expand the deployment of AI training and inference models. (TrendForce)

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ROI

AI Boom Sparks PCB Materials Warning

Vendors are shifting capacity from traditional PCB materials to advanced dielectrics. They should be increasing both.

I HAVE SOME good news, and some bad news. (Spoiler alert: This should be a wake-up call to all companies that produce materials and supplies that go into printed circuit boards.)

First the good news. During the PCEA PCB Management Forum at PCB East in May, industry leaders shared long-awaited optimism about the printed circuit industry in North America, Europe and globally. Much of the discussion focused on how AI will impact manufacturing, particularly the massive increase in demand for advanced PCBs required to support the growing number of AI servers and data centers.

What kind of volumes are we talking about? If a single AI data center requires 100,000 GPUs, and those GPUs require roughly 12,500 AI servers, with each server using about 15 advanced PCBs, one data center alone could consume more than 175,000 circuit boards, not including supporting electronics used to manage the facility. With projections calling for 400,000 to 600,000 AI data centers globally over the next five years, demand for advanced PCBs could reach between 8 million and 12 million boards, creating a significant impact across the global supply chain.

But that's not the only demand driver. Ongoing military support efforts tied to Ukraine and recent Middle East conflicts have significantly reduced existing weapons stockpiles, and those systems will eventually need to be replenished. Missiles, drones, aircraft and ground-based defense systems all rely heavily on printed circuit boards, meaning future replenishment orders could create another major surge in PCB demand.

Globally, AI data centers are expected to drive a dramatic increase in PCB demand, not only in Asia but also across North America and Europe. At the same time, Western defense spending is rising as the US works to replenish depleted munitions stockpiles and Europe expands its own defense reserves to reduce reliance on the US. Together, these trends are creating what could become a perfect storm for the PCB industry. But beyond industry discussion, independent analysts are now projecting the same trajectory.

In late 2025, before the latest developments in the Middle East, Goldman Sachs released a report examining the impact of AI data centers on the PCB and copper-clad laminate (CCL) industries. According to the report, AI server demand is expected to grow from roughly $3 billion in 2024 to $27 billion by 2027. Goldman Sachs also projected that CCL demand could rise by 140% to 200% during that same period. After years of uncertainty, the industry finally appears positioned for significant growth across Asia, North America and Europe.

Now comes the bigger question: Is the supply chain prepared?

While demand for both advanced and traditional PCBs is climbing rapidly, the supply base is tightening. Glass fiber, a key material used in laminate production, is already facing shortages. The same is true for CCL, where the existing supply is struggling to meet current demand. Conditions are even tighter in North America and Europe, where domestic production capacity remains limited. Compounding the issue, many suppliers are shifting capacity away from traditional materials and toward advanced low-Dk and ultra-thin glass products designed for next-generation applications. Similar changes are occurring in CCL manufacturing, where lower-copper-weight materials are increasingly replacing more traditional offerings.

The challenge is that traditional materials remain critically important across large segments of the electronics industry. Rather than expanding capacity for both advanced and legacy technologies, much of the investment is simply being redirected from one category to another.

Ventec recently announced plans to build a laminate facility in the United States, a move that could help strengthen regional supply. New capacity may not come online quickly enough to meet the accelerated demand forecasts tied to AI infrastructure growth through 2027, however.

Although much of the AI data center buildout is expected to occur in Asia, North America and Europe will still require substantial secure infrastructure to support sensitive controlled unclassified information (CUI) and intellectual property. At the same time, ongoing supply shortages are already extending lead times for laminate and other PCB materials while increasing costs across the supply chain.

The broader message for suppliers is clear: Global demand is returning, and the industry needs more capacity – not less. This is not the time to shut down facilities or walk away from legacy materials that remain essential to large segments of the electronics manufacturing industry. Supply chain challenges remain, but they also highlight the value of strengthening regional production capabilities. The coming years could represent one of the strongest periods the PCB industry has seen in decades, provided the supply base is prepared to support it.

PETER BIGELOW has more than 30 years' experience as a PCB executive, most recently as president of FTG Circuits Haverhill; peterbigelow@msn.com.

Stop Paying Tooling and NRE Charges Twice

Understanding tooling and NRE charges can help buyers avoid redundant PCB manufacturing costs and improve supplier negotiations.

PURCHASING BARE PRINTED circuit boards for an OEM or EMS firm often means losing money in places that aren't immediately visible.

In the high-mix, low-to-medium-volume PCB sector – where hundreds of different part numbers may be managed across dozens of product lines – margins are won and lost in the details. And there is no detail more universally misunderstood and historically abused than tooling and nonrecurring engineering (NRE) charges.

Whether based in the US, Canada or Mexico, the supply chain mechanics remain exactly the same. Without a clear understanding of how PCB factories and traditional domestic brokers calculate and apply tooling costs, those charges are often paid twice – sometimes even three times.

It's time to stop the money loss. Here is the unvarnished truth about NRE, how the "double charge" trap works and how to negotiate a way out of it.

What Actually Is Tooling and NRE Today?

To understand how buyers are being taken advantage of, it is first necessary to understand what is purchased when a supplier invoices for NRE.

Decades ago, tooling meant something highly physical. It involved generating photographic mylar films for every layer of a board, physical drill tapes, and custom-routed plates. The process was labor-intensive and expensive, with tooling charges averaging roughly $100 per PCB layer count.

Today, PCB manufacturing is overwhelmingly digital – no multiple layers of phototools or physical drill tapes stored in climate-controlled rooms. Tooling or NRE generally covers two specific things:

1. **CAM engineering.** A computer-aided manufacturing (CAM) engineer at the factory must review the files, run design for manufacturability (DfM) checks, panelize the boards and convert design data files into the specific machine code used by local drillers, routers, and imaging equipment.
2. **Electrical test (ET) fixtures.** For low-volume prototypes, factories use flying probe testers, which use robotic arms to test connections digitally. No physical fixture exists. For medium-to-high-volume production, however, they build a bed-of-nails or grid fixture, a physical jig made of pins that tests the entire board at once.

This requires physical materials and precise drilling.

Here is the secret: CAM time is relatively cheap. A standard 4-layer board might take a skilled CAM engineer an hour or two to process. The engineer is usually a salaried position, so whether only one part number is "cammed" in a day or eight, the daily cost to the factory is the same.

The only truly expensive physical asset is the hard ET fixture for higher-volume runs. Keep this in mind because it is the key to defending the budget.

The "Hostage" Situation: How to End Up Paying Twice

The high-mix PCB buyer usually gets hit with double NRE in two specific scenarios: the "supplier switch" and the "prototype-to-production" trap.

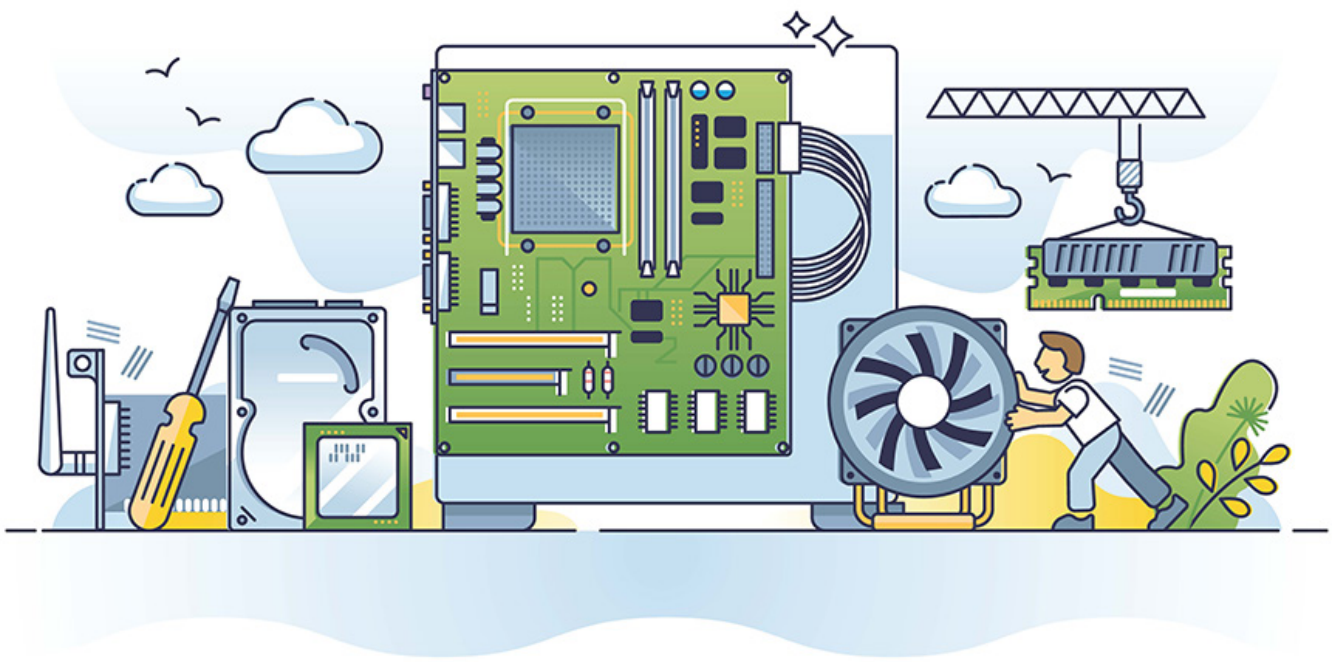

Figure 1. Flying probe and bed-of-nails testing approaches each carry different cost and tooling implications for PCB production.

Scenario 1: The supplier switch. Let's say a company has been buying Part #12345 from PCB supplier A for three years. The $250 NRE charge has already been paid. Then Broker or Manufacturer A gets greedy and raises the unit price, so the decision is made to move the part to Broker B.

Broker B quotes a great unit price, but at the bottom of the quote is a $250 tooling charge. When questioned, Broker B says, "We have to use our own factory, and they have to do the CAM work from scratch. We don't have your tooling."

This is technically true. The new factory must do the CAM work. But buyers need to understand that the traditional broker model relies on holding part numbers hostage. Because some brokers may mask which factory in China is actually building the board, the tooling can't simply be transferred elsewhere.

Scenario 2: The prototype-to-production trap. A new board is designed and sent to a broker for 10 prototype pieces. The broker charges a $150 NRE fee for the prototype run, which uses flying probe. The board works perfectly. A month later, an order is placed for 2,000 production pieces.

The broker then sends a new invoice with an additional $350 tooling charge. Its explanation? "The prototype was done on a flying probe. For 2,000 pieces, the factory needs to build a hard electrical test fixture. That costs money."

Again, technically true. But CAM engineering had already been charged during the prototype phase. The engineering time is effectively being billed twice, wrapped under the vague umbrella of tooling.

Beyond that, many buyers take issue with paying for electrical test tooling on repeat production orders. If the supplied files have already been proven electrically correct, the question becomes: why should the customer pay for a fixture simply to verify that the supplier's manufacturing process is functioning properly?

As a buyer, the goal is to commoditize the tooling. Stop accepting NRE as a fixed, mandatory tax, and use these tools to negotiate.

Ask for "transfer tooling" waivers. When moving a high-mix package of established business from one broker to another, the new broker should be hungry for the volume. Do not pay tooling to switch suppliers.

Tell the new broker: "I have 50 active part numbers I want to move to you. The unit pricing looks good. But I am not paying NRE to retool parts that have been running perfectly for three years. If you want this $250,000 in annual spend, you will absorb the CAM costs at your factory."

A transparent broker will waive those charges to win the long-term unit volume.

Ask for the "proto-to-prod" credit. When placing a prototype order, get the production tooling rules in writing before issuing the PO.

Make an agreement that any NRE paid on a prototype will be credited toward the hard tooling required for the first production run. Alternatively, if no revision changes are made between proto and production, demand that they only charge for the delta (the exact cost of the physical test fixture) rather than a blanket NRE fee that includes the CAM work already completed.

Ask for the NRE breakdown. Never accept a generic $400 tooling line item. Ask the broker to itemize it. How much is CAM? How much is the ET fixture? Is it flying probe or bed-of-nails? If a broker is opaque and refuses to break this down, it could indicate a hidden profit margin in the NRE charges. I have seen traditional brokers take a $50 CAM charge from a Chinese factory and mark it up to $300 to the OEM. Transparency is the best weapon.

But before demanding a breakdown, consider the order's overall dollar value. The larger the order value, the greater the leverage to push for transparency. Many smaller-dollar-value orders use tooling charges to push a part number over a minimum order value (MOV), so it is feasible to build and ship.

An MOV that includes tooling charges will usually yield a better piece price for the buyer and allow the factory to ship a lower-value order. But be careful when it is time to reorder that same part number, as a minimum order quantity (MOQ) might be required to maintain that same piece price.

When NRE is Actually Justified

To be a strong negotiator, it's important to be fair. There are times when NRE is completely legitimate, and refusing to pay it will only strain supply-chain relationships. Expect to pay tooling when:

- **It is a genuine first-time build.** The factory has never seen these design data before and must invest hours of engineering time to panelize and prepare them.
- **There is a revision change.** Even a "minor" trace move requires the factory to scrap the old data, reprocess the CAM and build a brand-new electrical test fixture. A new revision is a new board.
- **Complex HDI and blind/buried vias.** High-density interconnect boards require significantly more engineering and complex layer-by-layer testing protocols. NRE on these will be higher, and rightly so.

The final piece of the puzzle is internal discipline. Buyers at OEMs and EMS companies are incredibly busy. Brokers know this, and they rely on the fact that an EMS buyer placing an order for 40 different boards in a single month isn't going to cross-reference every part number to see if tooling was paid two years ago.

It's important to have a tooling ledger. Whether it is a custom field in the ERP system or a simple, shared spreadsheet for the purchasing department, it's paramount to track the part number, revision level, date tooling was paid, broker/supplier it was paid to and the type of testing paid for (flying probe versus hard fixture).

If the ERP shows that NRE was paid on Rev B of Part 12345 in 2024 and a broker tries to slip a $200 tooling charge onto the 2026 reorder, immediately strike it from the quote.

In the high-mix, low-volume PCB world, margins are tight. Every dollar spent on redundant tooling is a dollar stripped directly from the company's bottom line.

Stop viewing NRE as a standard cost of doing business. View it as a negotiable service. Work with brokers or suppliers that clearly explain what is being paid for, demand waivers when moving established business and track tooling data meticulously. The factories are doing the hard work. Don't let the middlemen use tooling as an excuse to pick your pocket.

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as the founder of a leading distributor. He is cofounder of DirectPCB (directpcb.com); greg@directpcb.com.

FOCUS ON BUSINESS

Developing a Good Account Strategy

Strategic account planning can help EMS program managers align customer relationships with long-term growth, profitability and operational goals.

FOR MANY ELECTRONICS manufacturing services (EMS) program managers, just managing tactical account issues is more than a 40-hour-a-week job. Thinking about strategy can be difficult when an inbox is full of urgent emails and the phone is ringing with additional problems to solve several times a day. While blocking out time to develop a broader-picture account strategy doesn't necessarily eliminate that workload, it does create a foundation for determining whether adequate resources are devoted to that account and whether the account is a really good fit for the EMS provider's business model.

The basics are simple. List the following:

- Core decision-making team
- Current business dynamics
- Core value proposition
- Subordinate value propositions
- Service enhancement needs
- Growth opportunities
- Competitive issues
- Revenue/profitability trends
- Near-term goals
- Strategic goals
- Overall account assessment.

The goal of putting this into a strategic plan is to develop a broader view of what is working and not working in the account and to better align the account with organizational goals. It can be tempting to put one-line answers to this list; however, the end goal is to drive critical thinking in each of these areas.

For example, the core outsourcing decision team usually includes more people than just the day-to-day contacts working with a program manager. Understanding who those people are and developing relationships at higher levels of the customer can be the difference between accounts that grow and accounts that simply get the business that other competitors don't want. Having relationships across the entire team is also beneficial when a team member leaves.

The next several points look at account dynamics. What level of product is being built? Is the business growing or shrinking? What does the customer most value about the relationship? Are there smaller points of value that also appeal to the customer? Once those elements are understood, can they be built upon to improve the value delivered to the customer?

Sometimes service enhancement simply means doing a better job on the basics. If an EMS provider has invested in better technology or enhanced operational efficiency, however, the service enhancement opportunity might be based on more effectively leveraging those investments to provide the customer with improved service, quality or scheduling flexibility. The pace of technological change is outpacing operational improvement, making it harder to leverage the increased ability to automate tasks. Doing a once-a-year sanity check of available tools against program management processes may reduce workload when evaluating service enhancement options.

What are the growth opportunities? More of the same business or options that increase the value add, such as board-level assembly expanding into box-build, or box-build expanding into fulfillment and repair depot services? Each additional level of value-add helps increase customer stickiness. Can the customer's core team provide introductions to other divisions? Intercompany referrals are often easier to win because they carry the added credibility of an existing business relationship. Often, these types of growth opportunities go untapped because the questions needed to gauge likelihood never get asked. Creating a list of potential growth opportunities is the first step toward setting goals to explore opportunities beyond the business already coming in.

Competitive issues are another area for improvement. Years ago, an EMS provider I worked for had a customer whose demand was dropping. We shared the business with a competitor that, according to the customer, did not perform as well as our company. The program manager asked why the business kept dropping. The customer told us its overall demand was below forecast, and our competitor was imposing penalties for being below forecast, so it was moving business to the competitor to avoid the penalty. We instituted penalties, and the business moved back because our quality and delivery were better. While not a sterling example of customer service, it illustrates the importance of understanding the competitive playing field.

The account goal-setting bullets are also beneficial. Hectic environments often foster a firefighting mentality that doesn't prioritize metric improvement. Setting goals for revenue and profitability sets the stage for improvement of those metrics. Mapping out long- and short-term goals to achieve desired account outcomes also sets a clock ticking on the improvements needed in the account.

Finally, the overall assessment of the account is important as well. Does the account still align with business model goals, or is it a legacy account that likely would not be booked today? If there is no good answer to that question, what account behavior would reinforce the value of keeping it, or serve as the triggering event to begin disengagement? Understanding those factors makes it easier to determine when accounts are no longer a good fit for the business. The old EMS adage that 20% of customers cause 80% of problems is not wrong.

Having a clear understanding of account dynamics helps determine where resources are best allocated and opens the door to business growth opportunities that may otherwise go unexplored. While developing the initial plan may be time-consuming, it can be kept up to date with short quarterly reviews. Developing this discipline helps grow a business that aligns with internal business model goals.

SUSAN MUCHA is president of Powell-Mucha Consulting Inc. (powell-muchaconsulting.com), a consulting firm providing strategic planning, training and market positioning support to EMS companies and author of *Find It. Book It. Grow It. A Robust Process for Account Acquisition in Electronics Manufacturing Services.* She can be reached at smucha@powell-muchaconsulting.com.

Why OEMs Should Care: The Supply Chain Is Only as Strong as the Manufacturers Behind It

North American PCB and PCBA manufacturing capacity is becoming a strategic issue for OEMs facing supply chain, workforce and compliance pressures.

HERE'S THE TRUTH nobody ever says out loud in the boardroom: Innovation, speed and resilience are only as strong as the PCB and PCBA manufacturers behind them. Not the brand. Not the R&D budget. Not the glossy renderings the design team produces. Success rides on the shoulders of the companies that actually turn engineering intent into real, functioning hardware.

And right now, those companies – the North American PCB and electronics manufacturers – are fighting for their lives.

For OEMs, prime contractors, aerospace integrators, medical device companies and others responsible for mission-critical technologies, the health of North America's electronics supply base is not a "vendor issue." It is not a quiet back-office procurement concern. It is a strategic vulnerability that affects lead times, product reliability, compliance posture, innovation pipelines and national security obligations. If the ecosystem collapses, everything built on top of it collapses with it.

This is why organizations like the Printed Circuit Board Association of America (PCBAA) exist, and why OEMs must engage, support, and strengthen the ecosystem that supports them.

When the Supply Chain Falters, the Product Fails

In every industry – defense, aerospace, medical, industrial automation – there's a dangerous assumption: that the manufacturing capacity will always be there when it's needed. That the PCB shops will always take an order. That the assemblers will always squeeze in prototypes. That someone, somewhere, is still building the boards, substrates and assemblies products require. But that's not how reality works.

Over the past two decades, North America has lost over 80% of its PCB manufacturing capacity and a significant portion of its assembly base. Entire technologies moved offshore. Skilled workers aged out with no replacement pipeline. Critical materials were consolidated into single-country choke points.

OEMs got used to "just-in-time." Meanwhile, the supply chain entered "just-barely-surviving."

When a domestic PCB shop closes – a very real trend – the next product launch gets delayed, redesign costs spike and validation cycles get stretched out by months. The R&D teams lose momentum, and competitors gain ground.

The supply chain is not a background function. It is the backbone of the innovation engine. And the backbone is showing cracks.

There may be a perception of diversification. Offshore suppliers may appear stable. Contract manufacturers may seem to "handle all that." But here are the hard, undeniable truths:

If a PCB or PCBA vendor fails, the OEM fails. Schedules slip. Customer commitments break. Revenue falls behind plan. No amount of "strategic sourcing" fixes a broken factory.

The world is one geopolitical incident away from shutting off supply. China-Taiwan tensions, export controls, rare-earth and raw material dependencies – the supply chain is only as stable as the global environment. That is not a risk aerospace, defense or medical companies can afford to ignore.

Lead times are not the problem – capacity is. Once North American manufacturing capacity disappears, it does not come back quickly. A new PCB shop cannot be conjured out of thin air. One hundred trained engineers cannot be hired overnight. When domestic sources are needed for compliance, security or speed, they must already exist.

Suppliers are aging out. The average PCB technician in North America is over 55. Many are over 60. Without investment, training and workforce development, the knowledge base evaporates.

Compliance is coming whether the industry likes it or not. DFARS, CMMC, ITAR, onshoring incentives and national security provisions are pushing manufacturing back home. If suppliers cannot meet the new requirements, neither can their customers.

OEMs do not need more supplier scorecards. They need a stronger ecosystem.

We love to talk about design innovation. Breakthroughs. Next-generation products. But innovation doesn't live in CAD files. It lives on production floors.

When prototype builds stretch to 14 weeks instead of two, engineering changes require multiple redesign cycles, and test vehicles get trapped behind offshore logistics delays, the innovation pipeline slows to a crawl. Designers lose the ability to iterate quickly. Engineers cannot verify designs efficiently. Product teams miss revenue targets, and customers wait longer for next-generation technology.

When local PCB and PCBA manufacturers are thriving, innovation accelerates. When those suppliers struggle, innovation stalls. The effects are already visible across the industry, with aerospace teams waiting months for HDI prototypes, defense contractors redesigning products because certain technologies are no longer available domestically, medical device companies dealing with offshore quality-control issues, and startups missing market opportunities because boards cannot be delivered fast enough.

Every one of these problems traces back to the same issue: a weakening supply chain.

China invests heavily in its electronics ecosystem. Europe invests. Korea invests. Taiwan invests. These regions view manufacturing not as a cost center, but as a strategic advantage.

Meanwhile, manufacturing in North America is often treated as something to outsource, squeeze or "optimize," and the consequences are becoming increasingly difficult to ignore. Heavy reliance on offshore suppliers leaves supply chains vulnerable to tightening export regulations, geopolitical conflicts that disrupt shipping lanes, lead times that can stretch from six weeks to 26, evolving ITAR or EAR classifications, and growing customer demands for domestic content.

Under those conditions, the supply chain stops being an advantage and becomes a liability. Competing globally requires speed, security, resilience and responsiveness – all of which depend on a strong domestic manufacturing ecosystem.

Why OEMs Should Join and Support PCBAA

This isn't charity. This is strategic self-preservation. PCBAA is the only organization fighting specifically for the survival and growth of the North American PCB and PCBA industry. When OEMs join, something powerful happens:

Supporting organizations such as PCBAA strengthens the domestic electronics manufacturing ecosystem while helping ensure PCB and PCBA suppliers can continue investing in equipment, workforce development and long-term capacity growth. It also gives manufacturers and OEMs a stronger voice in Washington on issues ranging from reshoring incentives and workforce programs to secure supply chain legislation and compliance requirements.

The need for trained technicians, engineers and operators is becoming increasingly urgent as workforce shortages continue to grow across the industry. At the same time, compliance, traceability, security and domestic-content requirements are all becoming more important for future products and programs.

Membership and industry participation also send an important message to PCB fabricators and assembly partners that their role in the supply chain is valued – and that long-term collaboration matters.

OEMs depend on a healthy, innovative and financially sustainable North American electronics supply chain. But that ecosystem will not survive on its own amid global competition, labor shortages, shrinking margins and decades of offshoring pressure.

Supporting organizations such as PCBAA represents more than industry symbolism. It is a strategic investment in the long-term stability of domestic PCB fabrication, PCB assembly and electronics manufacturing capacity.

Ultimately, every OEM depends on the same reality: a supply chain is only as strong as the manufacturers behind it. Strengthening that ecosystem strengthens the businesses that rely on it.

Visit www.pcbaa.org to learn more.

DAN BEAULIEU is a longtime management consultant to the printed circuit industry and a member of the PCBAA; danbbeaulieu@aol.com.

Printed Circuit Board Design for Test

Effective PCB testing depends on balancing electrical validation with manufacturable design practices throughout product development.

"DON'T GET TESTY with me." People might say those words when they're annoyed by a challenging statement. The point of testing is to challenge assumptions. It's the "find out" phase of product development. Printed circuit boards benefit from testing at multiple stages of production. Let's dive into the deep end.

Here, we will delve into:

- A brief overview of test equipment
- Different types of test boards
- Why DfX matters to test boards.

The first electrical test is performed on the bare board before populating it with components. A standard note on a PCB fabrication drawing instructs the vendor to perform continuity testing using the supplied IPC-356 netlist. The purpose of the test is to ensure that all the desired connections are made and that no unwanted connections exist.

A continuity tester provides limited continuity checks. Shorts and opens can be checked by hand using a continuity tester **(Figure 1)**. This is a simple piece of equipment consisting of two probe points. In between is basically a flashlight or a buzzer, perhaps both. When the two probes touch metal that is connected, the circuit is complete, and the light turns on, or a small buzzer is activated. If the contact points are not connected, then the buzzer or light remains dark or silent.

Figure 1. This one is a simple continuity checker. The alligator clip allows the technician to clamp onto a lead or test terminal and verify connectivity with the other one. (Source: Menda)

A multimeter can do this sort of testing along with measuring voltage, amperage or resistance. These meters generally have a dial that selects the measurement type and sets the range, ensuring the proper sensitivity for whatever is being measured. Generally, these meters are for making static (steady-state) measurements, although some fancy digital multimeters can measure current or voltage fluctuations.

Oscilloscopes, tone generators, network analyzers and other gear fill up the technician's workbench. It can be very expensive to provide everything necessary to perform the sorts of data collection required for system testing. One thing I can say about this is that it comes at the end of the line. Every delay in product development squeezes the testing schedule. There will be times of heroic effort on the part of the bring-up team.

Evaluation boards vs. bring-up boards. Printed circuit designers enable the test team by creating dedicated evaluation boards for individual chips and sprawling bring-up boards for characterizing entire systems **(Figure 2)**. Neither of these has anything to do with the form-factor production boards. What they do is give them confidence in their component choices, thereby derisking the whole program.

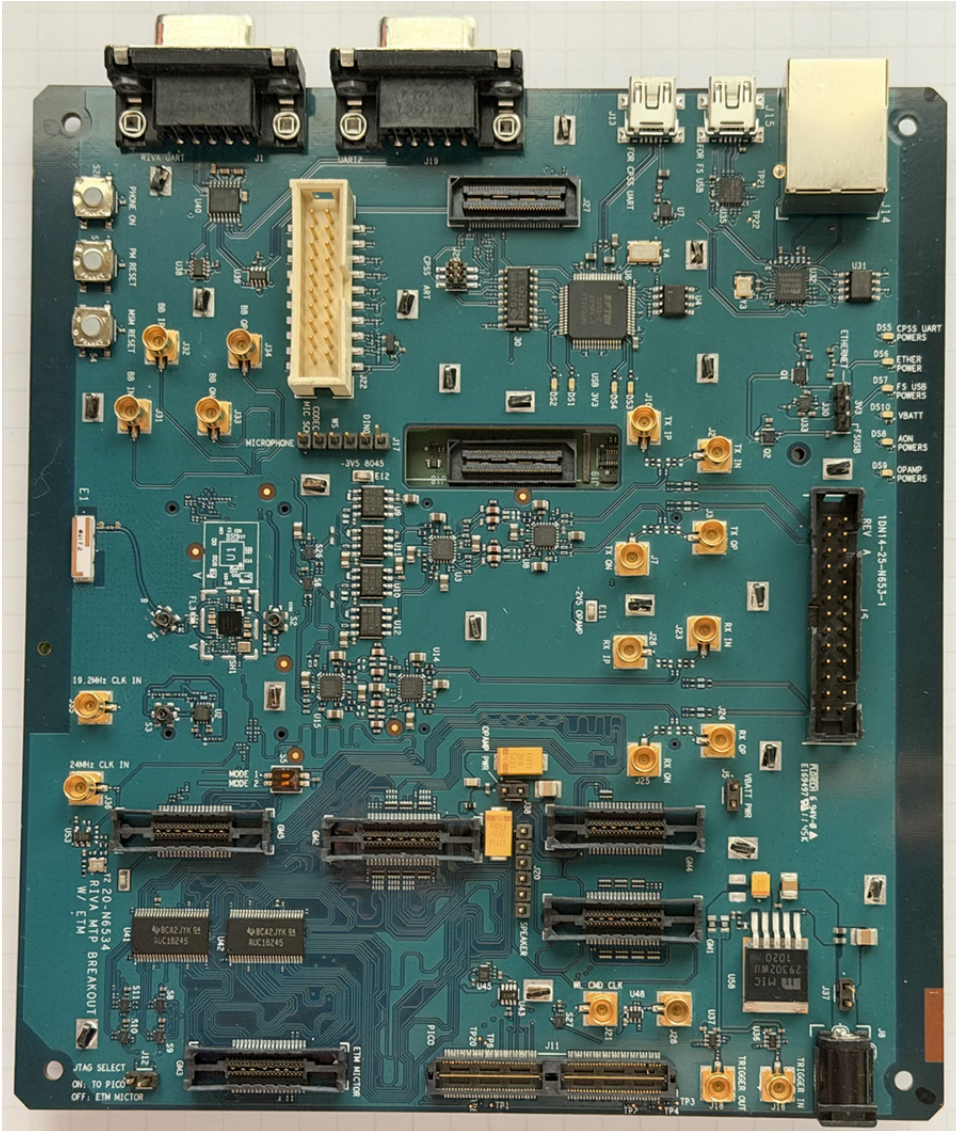

Figure 2. Notice the slot in the middle of this bring-up board. There is a test mule that is connected to the bring-up board through that slot. This minimizes trace length from the device to the test circuits. (Source: Author)

That said, the PCB designer needs to account for all DfX considerations when doing the layout of test fixtures. Case in point: A brilliant young engineer approached me about doing an eval board for an RF amplifier. This was a high-power chip that wound up in the little hut that accompanies those ubiquitous base station antenna towers. Thus, it was not a consumer device but part of the infrastructure that supported the mobile phone system. It needed to be rugged and reliable.

Design for test leverages the entire DfX suite. Pulling back the curtain a little, the young gentleman asked if I would move four capacitors closer to the amplifier's leads. I said no. The caps were already as close as our DfA rules would permit. He said, "Ah, man, this is just a Z-jig for dialing in the impedance." I relented and placed them in a way that broke the solder dam between the IC and the caps. He was happy and went about his day.

The next thing you know, the amplifier worked quite well, and he wanted a board that used three of these chips; one for the pre-amp and two more for the main stage. I wanted to correct the placement of the capacitors. "No! It works.

Don't change a thing." The multi-carrier amplifier used a total of six of these boards. Samsung loved it and wanted 900 amplifiers delivered per month for the 3G rollout.

That's four avoidable solder defects per chip, three chips per board, six boards per unit times 900 units, month after month. Do the math: 4x3x6x900. That's 64,800 potential rejects a month! Who do you think caught the heat for that fiasco? I will remember that for as long as I remain sentient **(Figure 3)**.

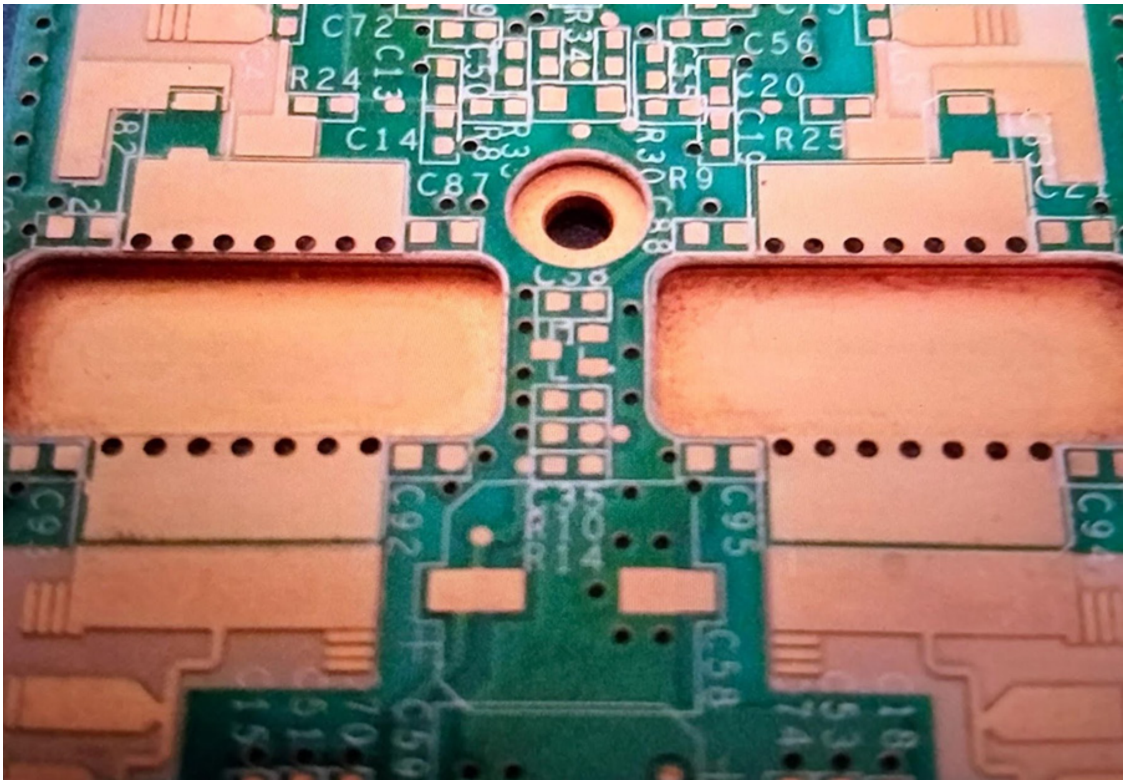

Figure 3. The four capacitors along the edges of the device were the ones that caused the commotion. This is a later revision in which the solder dam was restored to its original condition. Lesson learned: Any test vehicle has the potential to become a product. (Source: Author)

A few decades and several companies later, my manager at Qualcomm wrote in my review that I treat these boards "like they were my children." I'm not sure if that was meant as a compliment or a criticism. What I do know is that my eval boards are going to be manufacturable. For your sake, I hope yours are too.

Bring up, debugging, root cause and corrective action. Entire systems are also subject to test. The density of the form-factor boards is too tight to fully probe. Additionally, we need to insert extra electronics to measure current usage, especially when the product runs on batteries. The breakout/bring-up boards can be the size of a pizza, while the actual board is closer to a credit card **(Figure 4)**.

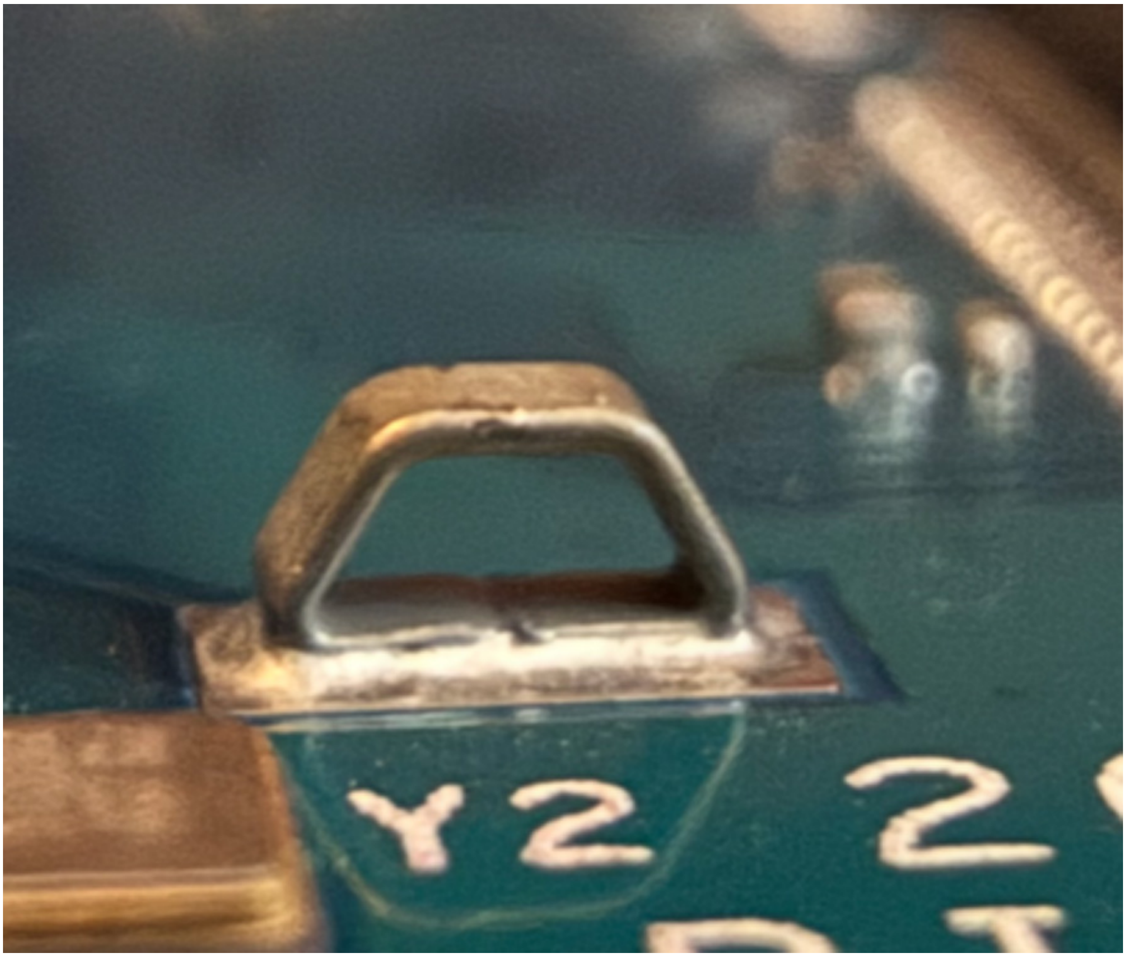

Figure 4. This trapezoid-style hook may seem a bit much, but it helps the test engineer anchor the meter to the probe point by clamping onto the loop. That leaves both hands free to take measurements. Similar test hooks are scattered around in Figure 2 and Figure 5. (Source: Author)

The first phase of testing is sometimes called a smoke test. Power up the unit and stand back. It's a good sign when the lab doesn't burn down. Even better if the device under test (DUT) gets warm but not so warm that the magic smoke comes out. The story is that a certain amount of smoke is built into every chip, and once it's released, it's game over for that unit.

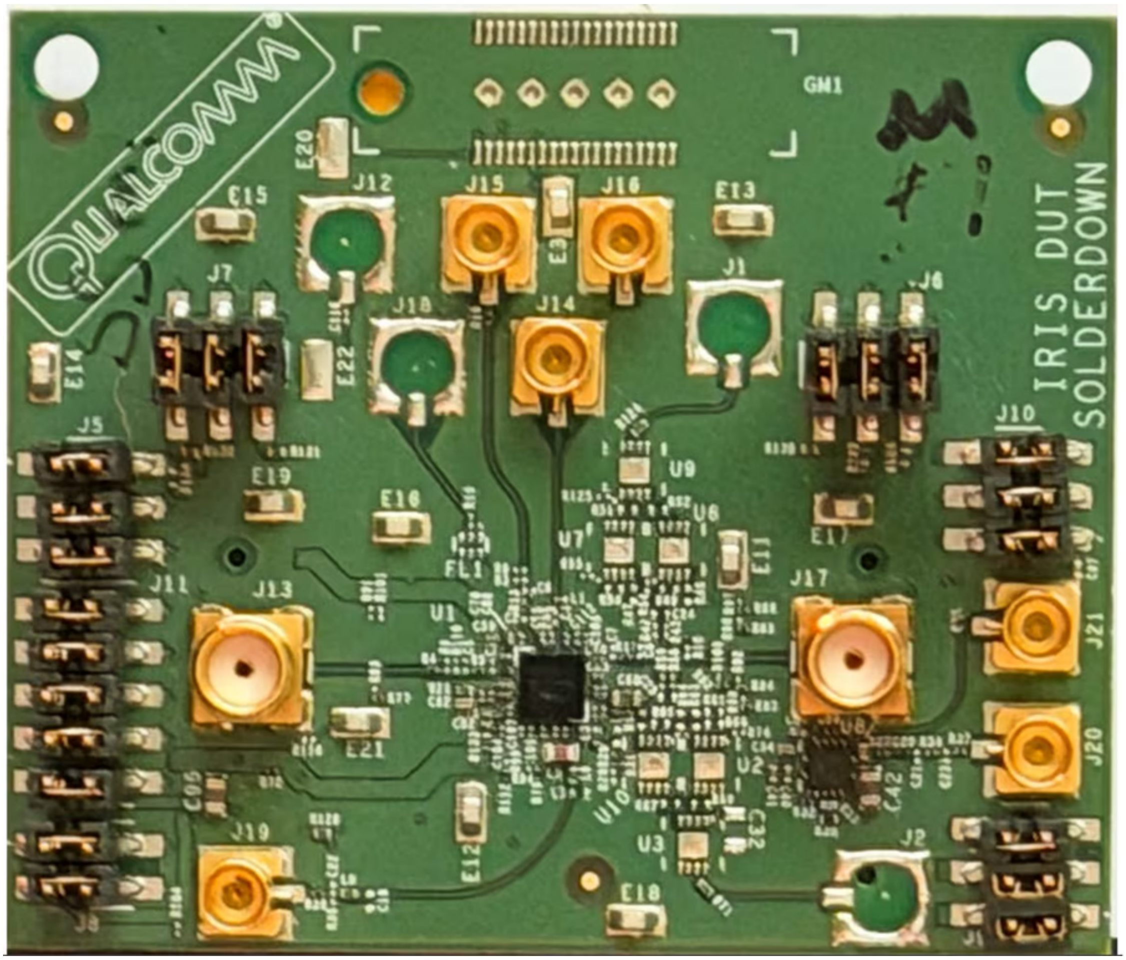

Figure 5. The integrated circuit at the heart of this evaluation board enabled cellphones to become WiFi hotspots. It took many iterations of this so-called DUT card before the WiFi, Bluetooth and FM radios would work together in this small space. (Source: Author)

When the populated boards come back from assembly, the fun starts. The test engineer may be the same person who is doing the electrical engineering for the whole project. They will be fiddling with the test instruments to take readings of various nodes around the board. When those outputs are outside of the expected results, they roll up their sleeves and figure things out. Satisfying the test technicians at the end of the line must stay on our minds so they don't get testy with us!

JOHN BURKHERT, JR. is a principle PCB designer in retirement. For the past several years, he has been sharing what he has learned for the sake of helping fresh and ambitious PCB designers. The knowledge is passed along through stories and lessons learned from three decades of design, including the most basic one-layer board up to the high-reliability rigid-flex HDI designs for aerospace and military applications. John's well-earned free time is spent on a bike, or with a mic doing a karaoke jam.


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ECAD **TIPS & TRICKS**

Precise PCB Keepout Area Control with CR-8000

PCB engineers need more flexibility than all-or-nothing keepout rules.

MODERN PCB LAYOUTS demand precise routing control. As board designs become denser and constraints become more difficult to manage, PCB engineers need more flexibility than all-or-nothing keepout rules.

The Track Keepout feature in CR-8000 Design Force enables PCB designers to selectively permit traces or copper fills within designated keepout areas. This gives layout engineers more granular control over routing behavior while helping reduce DRC issues, routing inefficiencies, and unwanted electrical connections.

Why Use Keepout Areas?

Keepout areas are protected regions on a PCB that restrict where conductive elements can be placed. PCB designers use them to prevent traces or copper fills from causing electrical, manufacturing, or reliability issues.

A PCB designer may define certain keepout zones to:

- Prevent traces from routing beneath high-speed devices where additional signals could introduce electrical noise or interference.
- Maintain required spacing around high-voltage circuitry to meet safety and clearance requirements.
- Block routing and copper placement near component bodies to avoid assembly or soldering problems.

As layouts become denser and more complex, keepout areas help designers maintain control over routing and copper distribution throughout the board.

Why PCB Designers Need More Granular Keepout Control

Traditional keepout rules are often defined as all-or-nothing restrictions, blocking both routing and copper placement within a region. Many PCB layouts require more selective control so designers can restrict one type of conductive element while still permitting another, however **(Figure 1)**.

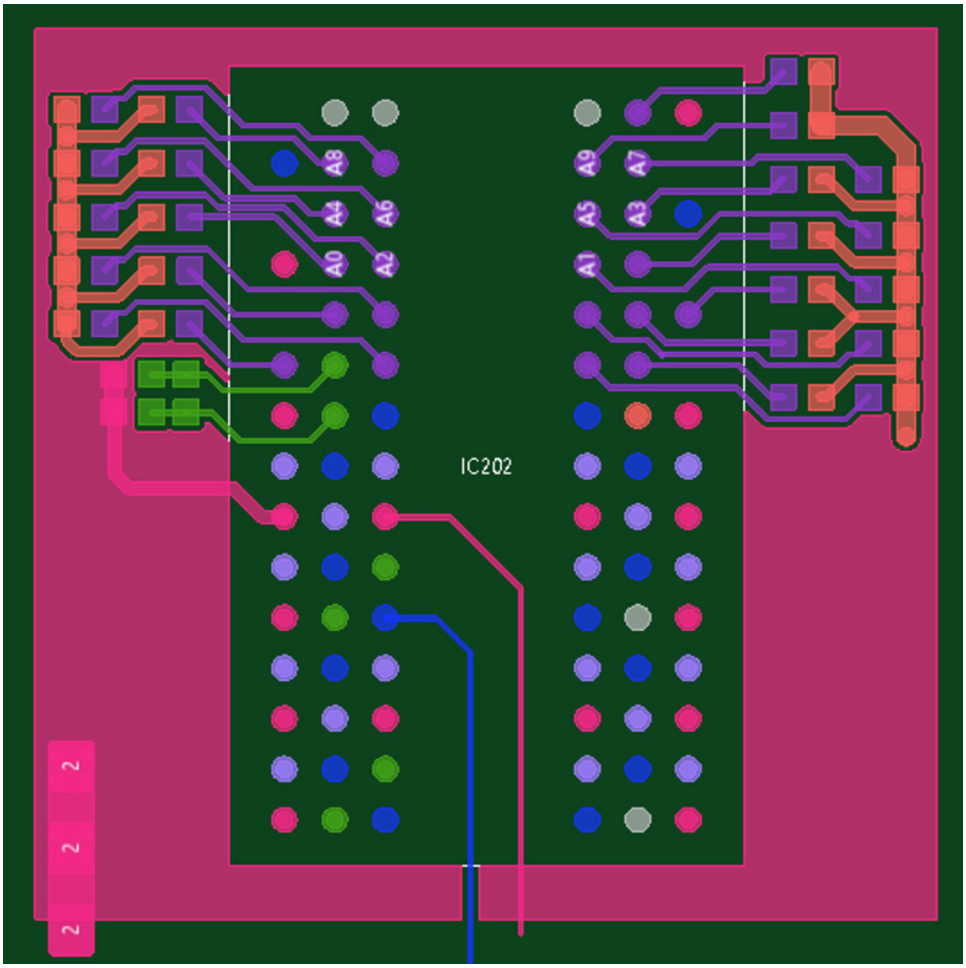


Figure 1. This keepout area (purple) permits traces, but not copper fills.

- **Permit traces and vias, prevent copper fills:** A designer may need traces and vias to pass through a constrained region near a component, while blocking copper fills that could create unintended electrical connections or spacing violations.
- **Permit copper fills, prevent traces:** A designer may want a ground copper fill beneath a sensitive device for shielding or thermal performance, while preventing traces from routing through the same area to reduce electrical noise or interference.

Without this level of control, engineers may create overly restrictive rules that complicate routing. In other cases, designers may override DRC warnings to achieve the desired layout, increasing the risk of costly errors and rework later in the design process.

How to Use the Track Keepout Feature

The Track Keepout feature works by combining designated keepout layers with configurable keepout rules. In CR-8000 Design Force, PCB designers define the keepout area and specify whether lines or area fills are permitted within that region **(Figure 2)**.

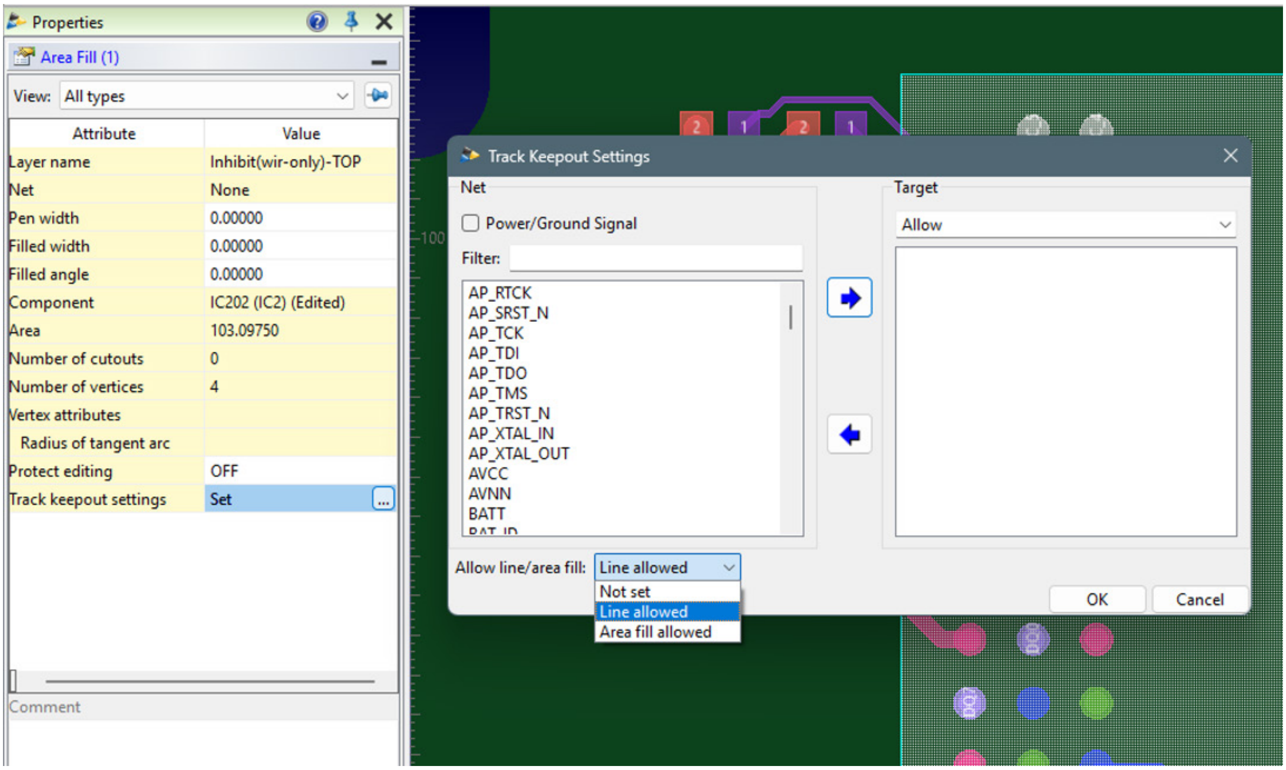


Figure 2. Define track keepout settings to permit either lines (traces) or area fill (copper fill).

The feature uses these three steps:

1. Create an "Inhibit track only" layer.
2. Define the keepout area geometry.
3. Set whether lines or area fills are permitted.

With proper setup, traces and fills are automatically restricted in appropriate keepout zones.

Keepout areas are often associated with components. If the keepout is input on the board but not the component, the component pins trigger DRC errors **(Figure 3)**. To reduce false DRC warnings, define the keepout area within the component footprint or use the "Make Figure into Component" feature in Design Force so the DRC engine correctly interprets the designer's intent.

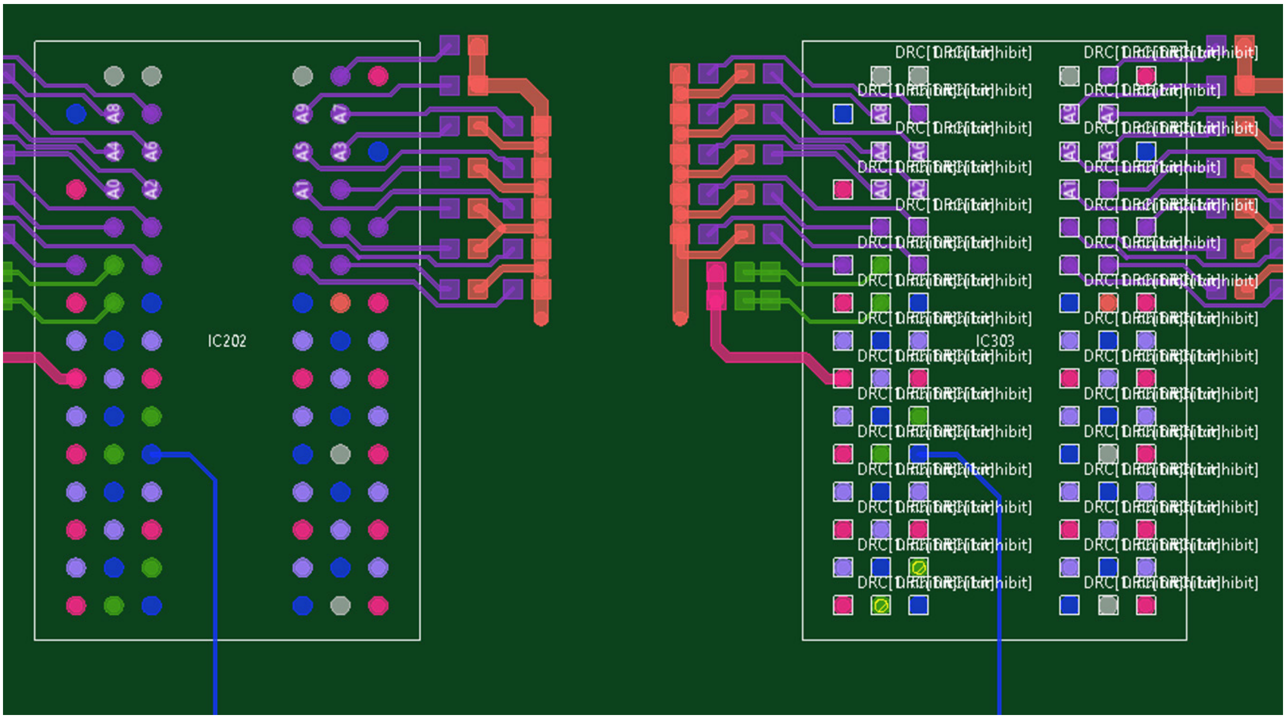


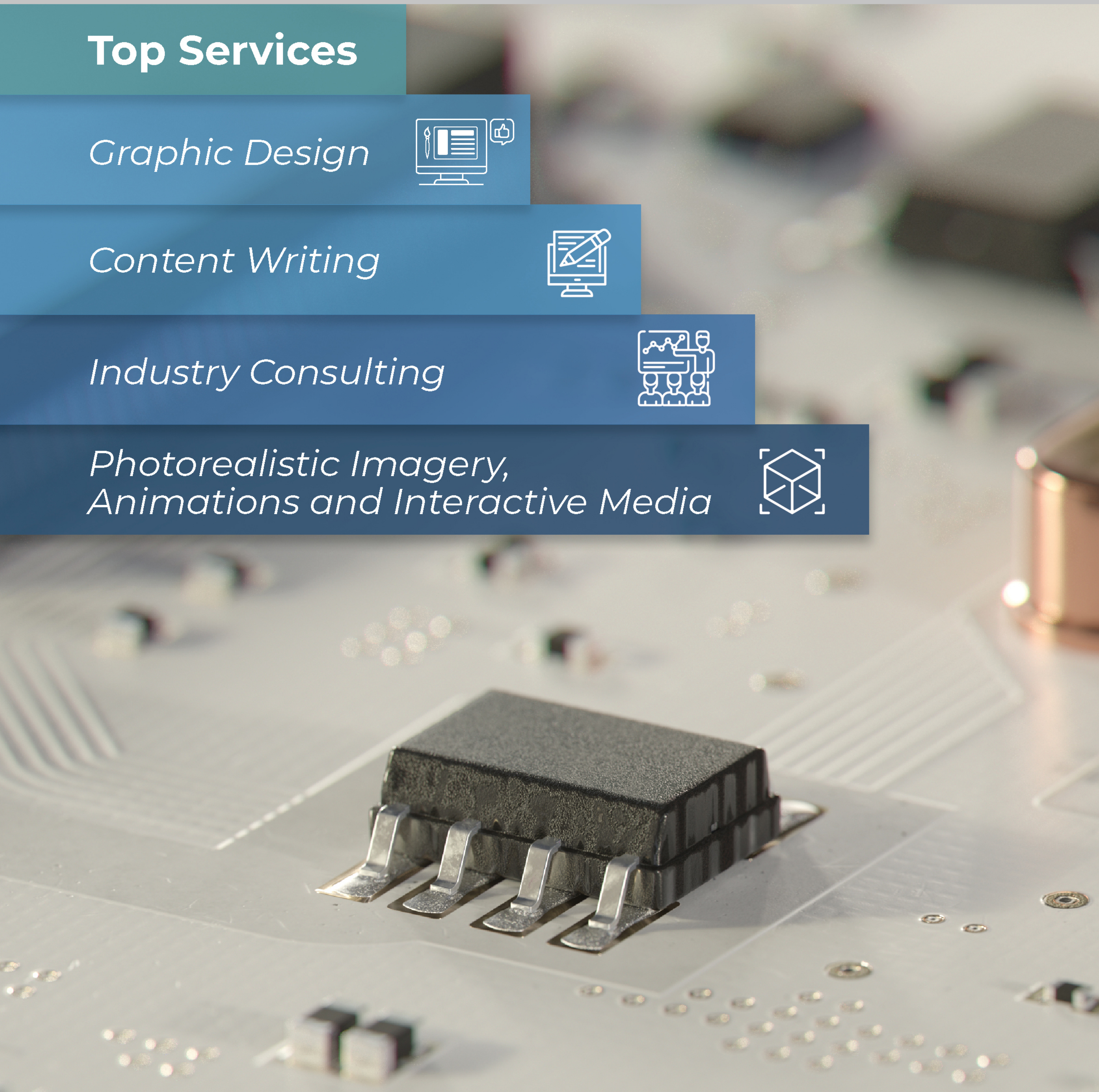
Figure 3. The IC on the left is associated with its keepout area, while the IC on the right is not, resulting in numerous DRC warnings.

Who Benefits from the Track Keepout feature?

- **PCB layout engineers:** Improve routing flexibility while maintaining precise control over copper placement and spacing restrictions.
- **Signal integrity engineers:** Reduce electrical noise and interference by controlling where traces and copper fills are permitted.
- **Library and CAD engineers:** Create more accurate component footprint definitions and reduce false DRC warnings during layout.

This video shows how Track Keepout Control works ↗

TAKASHI ICHIKAWA is an applications engineer at Zuken (zuken.com), focusing on customer support for CR-5000/CR-8000 and Cabling Designer. PCD&F/CIRCUITS ASSEMBLY shares this column each month as a benefit to its corporate customers and to provide real-world help to its members.



AI, Humanoid Robots and the Next Leap in Human Imagination

As the PCB industry absorbs AI's impact on nearly every aspect of business, the latest humanoid robots are showing how the technology can multiply our ability to imagine.

AI IS ONE of my favorite subjects, as you may have noticed, and I make no apology. It's already transforming our lives, and this will continue for years to come. Fixating on those two letters is easy, as they are currently evoking many emotions, including both excitement and fear. In the PCB industry, we are seeing how AI server demand is drastically reshaping the board market and the supply chain for substrate materials. So much so that, within Ventec, we feel the market will never be the same again.

Instead, I'd like to look at how this technology is giving us new tools to realize innovations that have driven our fantasies for generations. Humanoid robots, for example. Humanoids were probably the first types of robots people imagined. They have existed in stories since long before the word "robot" was coined, even in Greek mythology. And of course, we have seen early humanoids, such as Asimo, with its endearing, close-to-authentic human gait. Some may have found it comforting to focus on that awkwardness, feeling reassured that robots will never beat us.

Well, now, something big is happening, and the outlook has changed. Suddenly, humanoid robots are performing complex dance routines in perfectly coordinated troupes, balanced, fast and with fluent movements. They are also running, and the best are already faster than human athletes. More than 100 humanoid robots from institutions across China took part in a robot half-marathon held recently in Beijing's E-town. The winner's time, 50 minutes 26 seconds, was almost seven minutes faster than the current human record. I'm expecting that margin to have grown significantly by the next event.

Footage on YouTube, showing a humanoid robot chasing a group of boars in an urban street, is another impressive display of speed and balance while running. What's also interesting in this clip is that the robot seems to decide for itself when the boars have been seen off, waving them away with a gesture as if to say, "And don't come back!"

This is a noticeable – and sudden – shift from Asimo's cute baby steps just a short time ago to the bad-to-the-titanium-bone machines we see today. And AI is the key to the breakthrough. This is partly enabled by robotics moving beyond constraining bottlenecks in areas like computing, sensing, actuation and algorithms. More fundamentally, however, AI now lets robots *learn* to move rather than following explicit instructions that *tell them how* to move. Leveraging techniques such as reinforcement learning with model-based perception and control, they can dynamically balance, coordinate their limbs, adjust their position and compensate for errors. It's the reason humanoid robots can now move so fluidly, adapt, coordinate in groups, and run faster than human beings – even if that's partly due to the optimized physiology of the winning machine, with its large hip motors, liquid-cooled power modules and lightweight upper body.

Some observers have noted that the dancing humanoids are following a prescribed choreography and that the half-marathon winner was running on a pre-laid course. This means the robots cannot generalize to fit their learning to changing or unfamiliar surroundings.

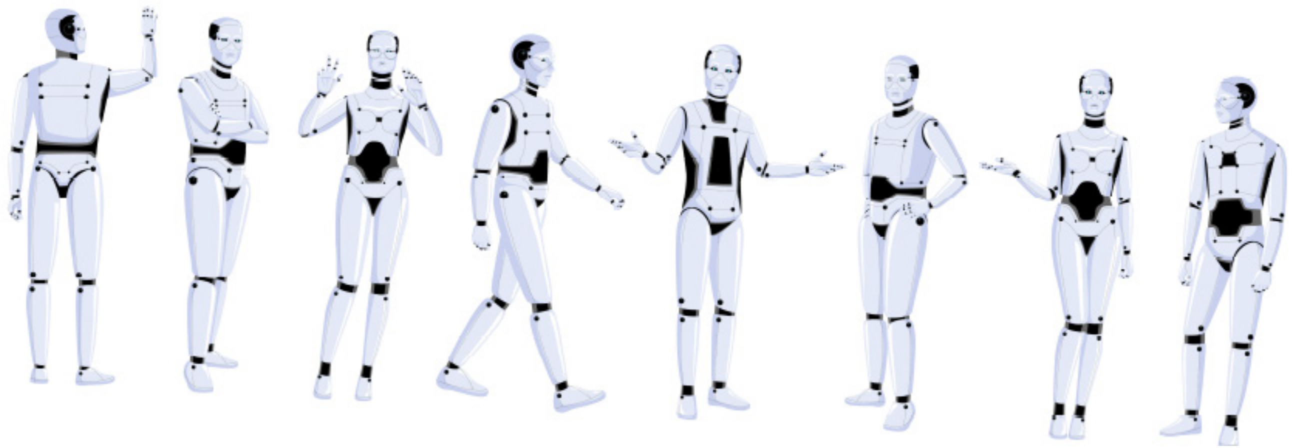


Figure 1. Modern humanoid robots are showcasing the next phase of AI-assisted mobility, coordination and adaptive learning.

Although this is true, robotics recognizes multiple types and levels of generalization. While the early Asimo had no ability to generalize and could perform only basic, prescribed actions in a controlled space, today's humanoids can adapt in limited ways to handle small variations in their environment and unexpected events. Research is now aiming for much broader generalization, and as these goals are reached, humanoids will begin to challenge human abilities. We're not there yet, but we can expect rapid improvements now that simple generalization is complete.

At some time in the future, then, we know robots will approach our position as the planet's apex generalist. We need to address how we task these machines so we can stay in control. Isaac Asimov's Three Laws of Robotics, from the "I, Robot" stories of the 1940s, constrain robots and impose ethical standards that protect and grant authority to humans. They are often cited in these discussions, but are these laws already being pushed aside as robot technology is increasingly pervading military activities? Drones, for example, are transforming today's conflicts by using techniques such as loitering over a target and dropping instantly when commanded. It contravenes Asimov's entire construct in one action.

We are probably only at the very beginning of military robotics. Its relatively low cost – in terms of procuring equipment and in the risks to trained soldiers – raises the prospect of wars becoming increasingly affordable and faster and easier to launch.

We have known for some time that working out ethics will be the most difficult aspect of coming to terms with AI's influence on our world. Governments, while having the power to legislate, are also keen to leverage the opportunities AI can provide.

But let's not dump Asimov just yet. He was not the first, by thousands of years, to conceptualize what we now call humanoid robots. But he and similar writers show us the role of talented imaginations to make our fantasies visible and desirable. This is a powerful catalyst for scientists and engineers to begin exploring the possibilities, using their skills and knowledge to bring them to life in the world.

ALUN MORGAN is technology ambassador at Ventec International Group (venteclaminates.com); alun.morgan@ventec-europe.com. His column runs monthly.

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A Beginner's Guide to BGA Routing That Won't Come Back to Bite You

Successful BGA routing depends less on pushing density limits and more on making fabrication-aware decisions early in the layout process.

FOR A LONG time, I have wanted to provide engineers with straightforward, specific guidance when starting a ball grid array (BGA) layout to complement the overall guidelines from many PCB fabricators. BGA routing often appears straightforward during layout, but many of the real challenges emerge later during fabrication, assembly, testing or field use. A design may pass CAD checks but still cause avoidable manufacturing problems if routing decisions are made without considering how the board would be built. For engineers new to BGAs, the objective should not be to maximize density or use advanced techniques prematurely. The goal is to apply disciplined design choices that are manufacturable, reliable and scalable.

The first factor to evaluate is the package pitch. Pitch determines how easily signals can escape the device and what routing strategies are realistic. At 1.0mm pitch, routing is relatively simple, with ample channel space and conventional fan-out methods working well. At 0.8mm, designs remain manageable but require more intentional planning. By 0.65mm, routing density increases enough that a clear breakout strategy is needed. At around 0.5mm pitch, high-density interconnect (HDI) techniques such as microvias, blind/buried mechanical vias and sequential lamination often become necessary to use innerlayers to relieve surface congestion. At 0.4mm pitch, HDI is typically unavoidable, and forcing conventional methods usually creates downstream manufacturing issues. Once a 0.35mm pitch is reached, engineers will need HDI and most certainly every layer interconnect (ELIC) buildups.

A common mistake is designing for the tightest trace and space capabilities available rather than the most robust. Although some suppliers can process ultra-fine geometries, manufacturability and yield often improve significantly when designs remain at 3mil trace and 3mil spacing or larger. Conservative geometries provide process margin, improve portability between fabricators, and reduce cost and yield risk. Tighter features should be reserved for designs that truly require them.

Another common mistake is simply reducing the diameter of the through-holes to permit space to reroute the breakout. To maintain manufacturability, I recommend a minimum 6mil finished hole size/8mil drilled hole. This will permit the widest global manufacturing capability.

Escaping signals from the BGA marks the beginning of routing complexity. Larger-pitch packages are commonly handled with dogbone fanouts, in which vias are placed just outside the pads, and traces are routed outward. As pitch decreases, via-in-pad structures become more practical because they permit signals to transition directly into internal layers and free surface routing space. Routing traces between pads becomes increasingly limited as the pitch shrinks. In many successful designs, a hybrid approach is used: dogbone fanout where possible and via-in-pad where necessary.

Approach via-in-pad solutions carefully. While attractive in layout, they shift complexity to fabrication because vias must be filled, planarized and plated reliably. Combining via-in-pad structures with aggressive trace and space dimensions compounds manufacturing risk and increases cost. When via-in-pad is used, the cap process adds an additional plating step, which generally requires a larger than 3/3 trace and gap. A good rule of thumb is to plan for a 3.5/3.5 trace and gap when working with via-in-pad. If spacing cannot permit this, then use caution and communicate directly with your PCB fabricator. For 0.5mm and especially 0.4mm pitch devices, via-in-pad may be necessary, but it should be used strategically.

When HDI enters the design, it should be part of the original plan rather than a late-stage correction. Microvias are commonly used to route signals from outer rows into innerlayers, preventing outer layers from becoming congested. More complex designs may require sequential buildup structures to maintain route ability. If HDI is added after routing difficulties arise, the result is often inefficient in-layer usage, compromised stackups and unnecessary complexity.

It is also important not to focus solely on fanout at the expense of signal integrity. Signals still require continuous reference planes, controlled impedance and clean return current paths. Every layer of transition introduces the need to consider returning to the current continuity. A clean breakout under the BGA provides little benefit if the signal path becomes electrically discontinuous deeper in the stackup.

Finally, passing design rule checks does not guarantee manufacturability. Designers should evaluate whether vias are right for board thickness, whether stacked microvias are truly needed, and whether pad-to-via relationships can be drilled and plated consistently. Early collaboration with the fabricator is especially valuable for designs at 0.5mm pitch and below.

Successful BGA routing is not about using the most advanced techniques available. It is about selecting the simplest structure that meets the electrical and mechanical requirements, then increasing complexity only when the design demands it. Conservative, fabrication-aware decisions made early in layout often prevent the most expensive problems later in production.

JEFFREY BEAUCHAMP is director of technology & engineering at NCAB Group USA (ncabgroup.com); jeffreybeauchamp@ncabgroup.com. He started his career in the PCB industry in 2003 at P.D. Circuits, now part of NCAB Group, and works with PCB customers to provide optimal solutions. His column runs quarterly.

THE **FLEXPERTS**

IPC-6013F Updates Flexible Circuit Requirements for HDI, Backdrilling and ENIG Defaults

The latest rev the flexible circuits spec has new requirements for HDI, backdrilling, and surface finishes.

IN ANTICIPATION OF revision F of IPC-6013 being released, this is a great time to highlight some of the biggest changes that impact manufacturers and end-users.

With every revision comes quite a few editorial changes. Sometimes requirements are not fully clear or hard to translate into other languages. Often, these come to light when there is a difference of opinion on how to interpret a certain requirement. Committee members do their best to channel their inner English teachers to improve grammar and clarity.

While these often do not change a requirement, they are intended to eliminate disagreements. GEA (IPC) committees are always on the lookout for these situations and welcome interpretation questions to build into the next revision.

Another place to make things clearer is when a figure is updated. Again, figures can be misinterpreted or not as clear as one would like. Often, someone can bring a better visual example to the table that is more "true to life." Some new figures reflect technology changes, such as microvias and backdrilling.

Beyond these types of updates are technical changes that add or modify requirements. These changes are driven by evolving technologies that introduce new circuit attributes, updated requirements that address manufacturing challenges tied to emerging features and the addition of new methods for validating finished product quality. Here are some of the changes to be aware of.

Table 1-1 is the Default Table. When a drawing is silent on a particular attribute, the default table provides a requirement. Historically, this table has listed solder as the default final finish. It will now note ENIG as the default for all new designs upon release of the document. This change reflects the drive toward Pb-free assemblies and ever-shrinking HDI features. ENIG is the preferred final finish in many markets and applications, and the new revision reflects that.

The table also adds a thinner minimum dielectric spacing requirement on new designs, permitting 65µm where it used to be 90µm. Again, this reflects some of the HDI designs with thin dielectric build-ups.

Many heavy users have come to know where certain sections land in the specification. They can even tell if it is on an odd or even page. With some changes in this revision, some of that memory will need updating.

Terms and definitions have moved out of IPC-6013 and now reside in IPC-T-50.

Another big change: All the copper plating tables have moved! They are now in the microsection portion of the document, in 3.6.2.11. The idea is that requirements should be located where inspection takes place. Some wording was changed to be clear that this is copper plating for drilled holes. Note that this move will affect the entire IPC-601X series.

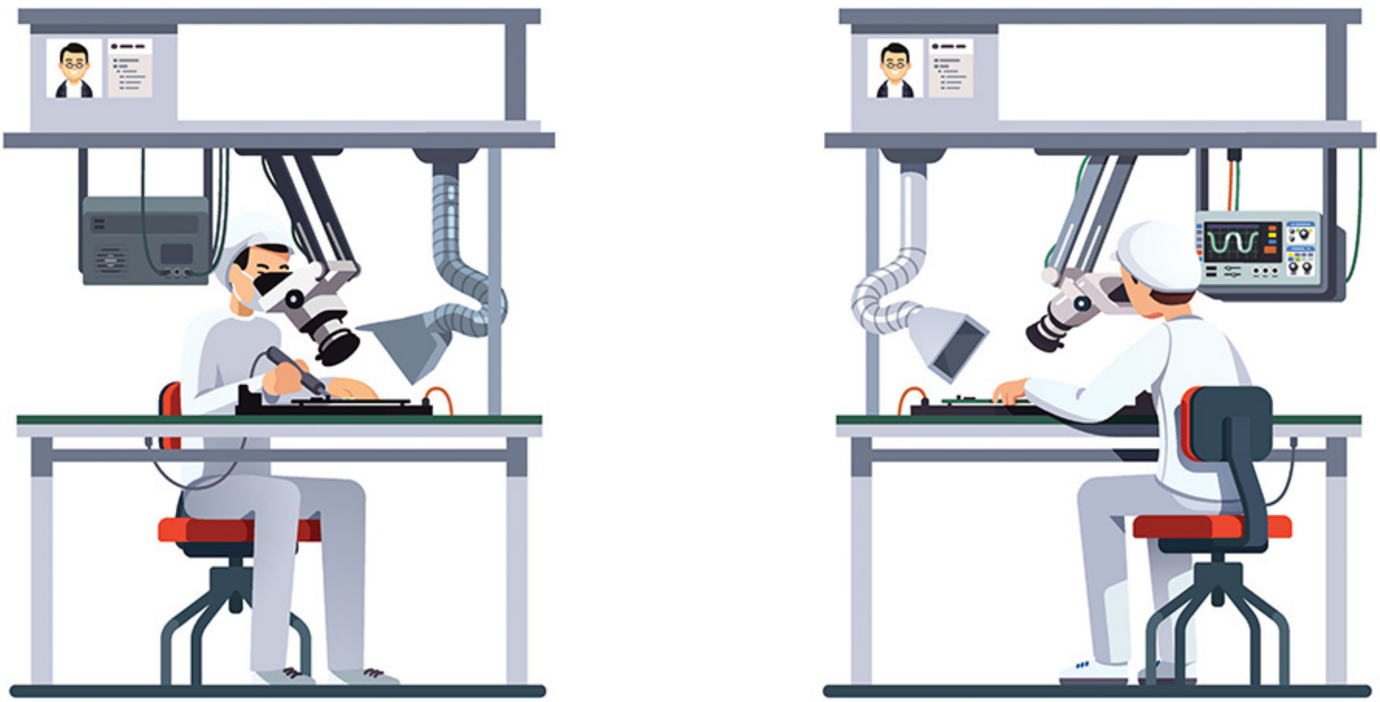

Figure 1. IPC-6013F repositions copper plating tables to the microsection inspection section.

Electrical test requirements have moved to 3.10.18 to consolidate all electrical tests in one location. Some of the new requirements provide direction for attributes not previously covered.

Some additions may have been long overdue. Section 3.3.1 adds requirements related to board edge plating, while section 3.3.1.3 clarifies that board thickness should not be measured within the transition zone due to potential highs and lows caused by prepreg, coverlay and bondply overlaps. Section 3.3.9 introduces allowances for strain relief variations, including skips, voids and extension onto the rigid cap, replacing Rev. E's AABUS language that had generated frequent questions and concerns. The revision also adds a section on backdrilling in 3.3.10, largely incorporating IPC-6012 requirements, along with section 3.6.2.19 covering backdrill microsection evaluation. Section 3.3.11 introduces a section on cavities, again drawing from IPC-6012 guidance.

Additional revisions include updates to the minimum annular ring requirements in Table 3-8 (formerly Table 3-11), which now separate external annular ring requirements for filled and capped vias from those for non-filled and capped structures, given the difficulty of assessing capped vias without microsection analysis. Section 3.5.4.5 on dewetting adds figures illustrating irregular HASL thickness as part of expanded tutorial-style guidance. Sections 3.5.4.8 and 3.5.4.9 add allowances for depressions and protrusions in non-soldered via locations for cap-plated filled holes and copper-filled microvias to avoid rejecting functionally acceptable parts for cosmetic reasons.

Table 3-12, covering PTH integrity, replaces the term "overall dielectric removal" with "copper penetration" and revises the maximum limits to better control extension beyond internal pad edges while maintaining adequate lateral spacing as annular rings continue to shrink. The same table also adds a note discouraging etchback for designs of all classes that permit tangency due to the risk of minimum spacing violations. Section 3.6.2.6.1 introduces new "evidence of etchback" language as an alternative to measurable etchback values, while section 3.6.2.6.3 rewords copper penetration requirements and updates associated figures to better balance larger pad designs with tighter geometries. References to "wicking" have been removed entirely.

Elsewhere, section 3.6.2.9 expands annular ring evaluation guidance for blind and buried vias and clarifies how sequentially laminated via structures should be assessed. Section 3.6.2.11, now renamed "Hole Copper Plating" from "Plating/Coating Thickness," clarifies that the requirement applies to plated through-hole copper rather than surface finish thickness. The revision also allows manufacturers to forgo multiple measurements and averaging if the thinnest observed measurement already exceeds the requirement and adds Figure 3-34 to demonstrate proper measurement locations. Finally, section 3.6.2.17 lowers minimum dielectric requirements for new designs, reflecting HDI constructions that increasingly rely on thinner cores and prepreg materials for microvia structures.

Other small changes were made, but these are probably the most impactful.

It is also worth noting that the Global Electronics Association (GEA) has created a new method for tracking changes in these documents, which is expected to roll out across all documents moving forward. The goal was to automate and standardize how GEA communicates document changes from one revision to the next. GEA tested out a couple of methods to capture document changes and got feedback from a group of committee chairs.

The update is intended to make revisions easier to identify, particularly for training and implementation purposes, while improving consistency across documentation updates.

Finally, none of the various specifications is set in stone. If you see something amiss, say something. Make recommendations for changes; the specs only get better with input.

NICK KOOP is director of flex technology at TTM Technologies (ttm.com), vice chairman of the IPC Flexible Circuits Committee and co-chair of the IPC-6013 Qualification and Performance Specification for Flexible Printed Boards Subcommittee; nick.koop@ttmtech.com. He and co-"Flexpert" **MARK FINSTAD** (mark.finstad@flexiblecircuit.com) welcome your suggestions.

How Flexible Circuits are Revolutionizing Electronics

Flex PCBs are enabling smaller, lighter and more reliable electronic systems by improving packaging efficiency, mechanical durability and electrical performance.

by AKBER ROY

In today's fast-changing electronics industry, new technologies play an important role in improving performance and functionality. One major advancement is the flex circuit board, which has transformed modern electronic design. Flex circuit boards not only save space and reduce weight but also provide exceptional design flexibility, expanding what electronic devices can achieve. That's why flex circuit boards are widely used today, as their unique features support smaller, lighter and more efficient products.

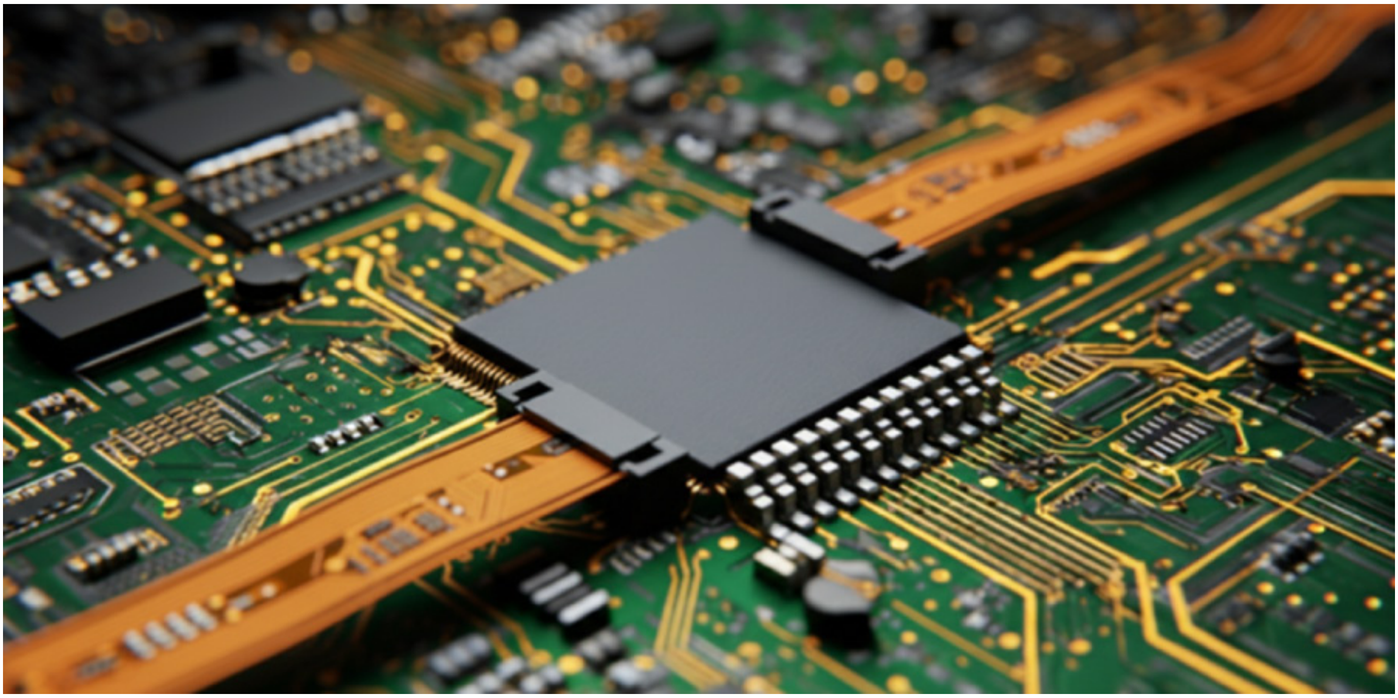

Figure 1. Flexible circuit boards enable compact, lightweight electronic designs by allowing circuits to bend, fold and conform to complex product geometries.

The use of flex circuit boards in electronic design is growing due to their many benefits, such as lightweight structure, the ability to fit complex shapes and improved heat management. As industries move toward smaller, multi-functional devices, flex PCBs are changing traditional manufacturing methods and supporting new design solutions across sectors.

Knowing the main benefits of flex printed circuit boards helps engineers and designers use them effectively to meet modern electronics requirements. The following are the key advantages of flex circuits that are helping transform the electronics industry.

 

Figure 2. Flex PCBs reduce connectors and wiring complexity, improving mechanical efficiency and reliability in compact electronic assemblies.

Space optimization and compact product design. One of the most significant benefits of flex PCBs is their ability to dramatically reduce the space required for electronic interconnections. Traditional rigid PCBs rely heavily on connectors, cables and mechanical fasteners to link multiple boards within a system. These interconnects consume valuable space and impose constraints on enclosure design. Flex PCBs eliminate or reduce the need for such components by directly connecting circuit sections through flexible conductors.

By allowing circuits to fold and wrap around internal structures, flex PCBs enable true three-dimensional packaging. This design freedom allows engineers to place electronics closer together and utilize otherwise unused volume within a product. In smartphones, cameras and compact medical devices, this space-saving capability directly translates into thinner profiles, reduced footprint and improved overall functionality.

Weight reduction and mechanical efficiency. Weight reduction is a critical factor in many electronic systems, particularly in portable, wearable and aerospace applications. Flex circuit boards help reduce weight and size, allowing designers to create small and lightweight devices without losing performance. Unlike rigid boards, flex circuits can bend to fit tight spaces and complex shapes.

Additionally, the elimination of connectors, cables and metal fasteners further reduces system weight. This reduction in mass improves not only portability but also mechanical efficiency. Lighter assemblies experience lower inertial forces during movement and vibration, reducing stress on solder joints and interconnections. In applications such as drones, satellites and wearable electronics, even small weight savings can result in improved performance, longer battery life and enhanced user comfort.

Improved reliability and reduced interconnect failures. Electronic system reliability is often limited by interconnect failures rather than component defects. Connectors and cables are common sources of failure due to wear, corrosion, vibration and mechanical shock. Flex PCBs address this issue by replacing multiple discrete interconnects with continuous copper traces embedded in a flexible substrate.

By reducing the number of connection points, flex circuits significantly lower the risk of intermittent failures and signal loss. Their ability to absorb vibration and mechanical stress makes them particularly suitable for harsh operating environments. In automotive and industrial systems, where constant vibration and temperature cycling are present, flex PCBs provide a more robust and durable interconnection solution than traditional wiring harnesses.

Enhanced signal integrity and electrical performance. Flex offers clear advantages over traditional rigid boards in signal integrity and layout precision. Rigid materials, made from resin and fiberglass, can suffer from glass-weave skew, which affects trace consistency, whereas polyimide-based flex materials avoid these issues and provide stable dielectric properties.

Shorter interconnection paths in flex circuits reduce parasitic inductance and capacitance, while eliminating connectors minimizes impedance discontinuities. Polyimide also ensures uniform traces and controlled impedance, making flex PCBs ideal for high-speed, high-frequency applications like high-resolution displays, camera modules and RF systems.

Resistance to vibration, shock and mechanical stress. Flex PCBs are inherently more resistant to vibration and mechanical shock than rigid boards. Their ability to flex and absorb energy allows them to withstand dynamic stresses without cracking or delaminating. This characteristic is particularly valuable in environments where electronics are exposed to continuous motion or impact.

In automotive electronics, flex circuits are commonly used in dashboards, sensors and control modules that experience constant vibration. In aerospace and defense applications, their resilience under extreme mechanical conditions contributes to long-term reliability and mission-critical performance. This mechanical robustness makes flex PCBs a preferred choice for demanding operating environments.

Thermal performance and heat management. Thermal management is becoming more critical in compact electronic systems. Flex PCBs help improve heat control by spreading heat more evenly across the assembly. Their thin structure allows heat to dissipate efficiently, especially when combined with proper thermal paths and materials. To further enhance thermal conductivity, fillers such as aluminum oxide (Al_2O_3), boron nitride (BN) or aluminum nitride (AlN) are added to the flex PCB substrate.

In some designs, flex circuits also allow direct contact between heat-generating components and metal housings or heat spreaders. This reduces thermal resistance and improves overall system reliability. As power levels continue to increase, the thermal benefits of flex are becoming even more important in system design.

Cost considerations and long-term value. Although flex PCBs typically have higher initial design and fabrication costs than rigid PCBs, their overall system-level cost can be lower over the product lifecycle. The reduction in connectors, cables, and assembly steps often leads to savings in materials, labor and warranty-related costs.

Additionally, the improved reliability of flex circuits reduces field failures and maintenance requirements. In applications where downtime or repair costs are high, such as medical equipment or industrial systems, the long-term value of flex PCBs outweighs their higher upfront investment. As manufacturing processes continue to mature, the cost gap between flexible and rigid circuits is steadily narrowing.

The benefits of flex PCBs have driven their adoption across a wide range of industries. Consumer electronics rely on flexible circuits to achieve slim designs and advanced functionality. Medical devices benefit from their reliability, biocompatibility, and compact form factors. Automotive systems use flex for sensors, lighting and control modules, while aerospace and defense applications depend on their durability and weight savings.

Wearable technology represents one of the fastest-growing application areas for flex circuits. Devices such as smartwatches, fitness trackers and health monitors require electronics that conform to the human body while maintaining reliability and comfort. Flex PCBs uniquely address these requirements, making them indispensable in wearable design.

AKBER ROY is CEO and founder of RUSH PCB. an electronics manufacturing company specializing in PCB design, fabrication and assembly services; roy@rushpcb.com (rushpcb.com).

UHDI MARGINS

Ultra HDI PCB Design: Why Registration, Alignment and Tolerance Stackup Drive Manufacturability

As PCB layouts move into UHDI territory, registration, alignment and tolerance stackup become critical factors in determining whether designs can be manufactured consistently and reliably.

by ANAYA VARDYA

Ultra high-density interconnect (UHDI) design gets attention for all the right reasons. For PCB designers, UHDI enables smaller feature sizes, higher routing density, fewer layers and greater flexibility in areas where conventional HDI begins to run out of room. Those benefits are real. Just as important is the shift in design mindset that comes with them, however. Once a layout moves into UHDI territory, the challenge is no longer only whether the design can be routed. The challenge is whether the design can still align, repeat, and build consistently during fabrication.

That is where registration, alignment and tolerance stackup begin to matter in a very different way. In traditional PCB design, there is often enough physical margin that small process shifts can be absorbed without materially changing the outcome. In UHDI, the available margin shrinks quickly. The result is that many structures that look clean and acceptable in CAD only remain acceptable if the design has been developed with realistic process behavior in mind.

What registration means in PCB fabrication. At its simplest, registration is the ability to hold intended positional relationships between different features during fabrication. In practice, that includes copper layer-to-layer alignment, drilled features to capture pads, solder mask openings to copper and imaged geometries to their intended dimensions. None of those considerations is new. What changes in UHDI is how little extra room remains once those relationships begin to move.

A positional shift of ±10–15µm may be of little consequence in a more forgiving design. On a UHDI structure built around 50–75µm laser-drilled microvias, fine solder mask openings and reduced capture pads, that same level of shift can materially reduce usable margin. This is not because UHDI is inherently unstable. It is because the design works at a scale where ordinary process variation consumes a much larger percentage of the available geometry.

Why tolerance stackup matters more in UHDI. Tolerance stackup is not a new concept. Every PCB design lives with it. What changes in UHDI are how quickly several individually acceptable variations begin to interact. A board may contain 50–75µm microvias, small capture pads, thin dielectric layers, fine solder mask openings and very tight breakout geometry. Each of those choices may be reasonable on its own. The problem begins when multiple features drift slightly in the same direction at the same location.

That is when the design can become noticeably tighter on the manufacturing floor than it looked on the screen. The typical failure mechanism is not that one dimension was wildly incorrect. More often, the issue is that several "good enough" assumptions are stacked together in one place. That stackup can reduce effective annular engagement, shift a microvia closer to the edge of its landing target, narrow an already-small mask dam, or reduce the exposed solderable area of a pad. In stacked microvia architectures, it can also propagate layer by layer, becoming cumulative rather than isolated.

Figure 1 illustrates this point. Registration is not best viewed as a single number attached to one process step. In UHDI, it is the combined result of material movement, lamination behavior, imaging accuracy and drilling position through the entire build sequence.

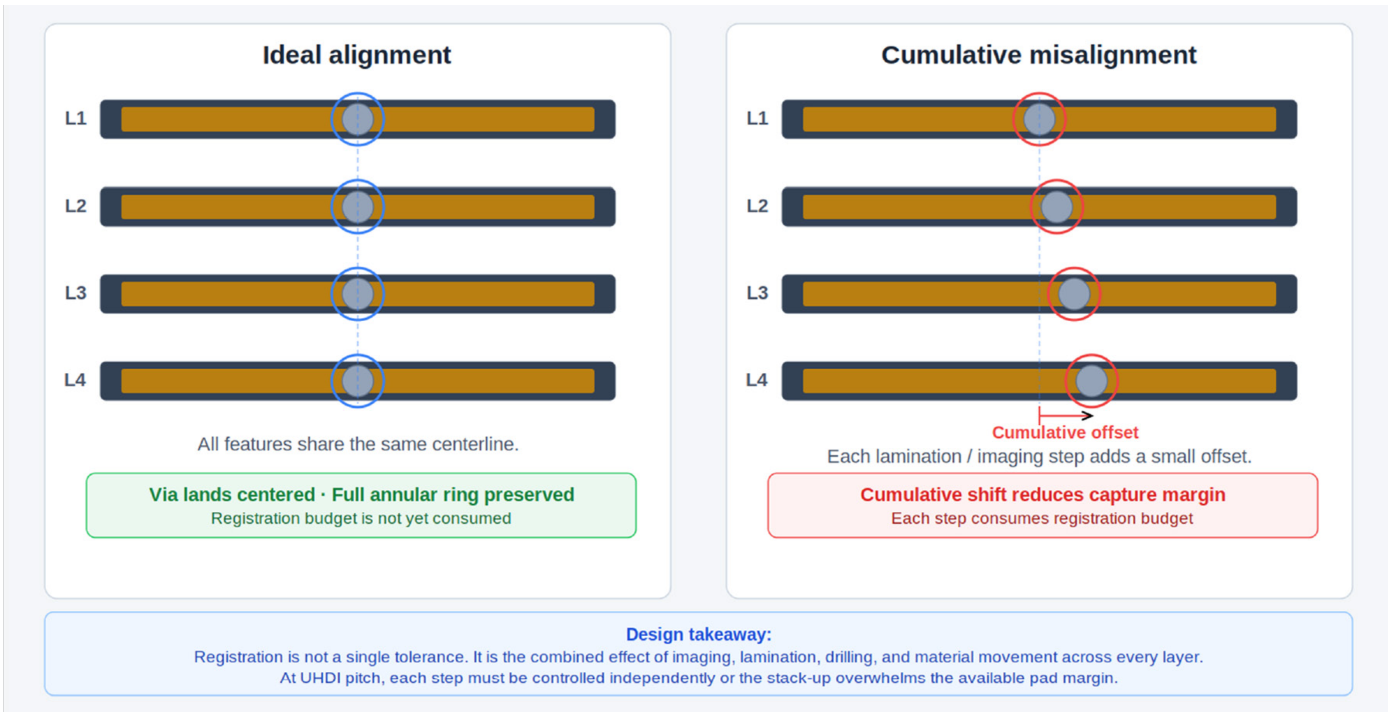

Figure 1. Registration stackup concept showing how small layer-by-layer shifts accumulate into meaningful final misregistration in a UHDI structure.

One of the most important mindset shifts for designers moving into UHDI is understanding the difference between ideal geometry and physical manufacturing behavior. In CAD, pads are perfectly centered, clearances are exact and mask openings align exactly as intended. In fabrication, materials expand and contract, layers register under real lamination conditions, drilling introduces positional variation and panels behave like physical objects rather than perfect mathematical models.

That is not a flaw in manufacturing. It is manufacturing. The most successful UHDI designs are not the ones that assume perfect behavior. They are the ones that leave enough room for the process to perform consistently within a realistic process window.

Microvias and small capture pads. As via diameters shrink, the landing target beneath them shrinks as well. This makes small positional shifts matter more than they do in more forgiving HDI structures. The issue becomes especially important in stacked via structures, where the accuracy and quality of each layer influences the next. A design that uses the smallest possible via without preserving adequate landing margin may still be routable, but it becomes less robust to ordinary process variation.

This is one reason UHDI should not be framed as a race to the smallest possible via. The better engineering question is whether the via structure maintains a workable margin throughout the actual fabrication window. **Figure 2** shows how a modest offset can materially reduce pad engagement and increase the likelihood of breakout or reduced interconnect robustness.

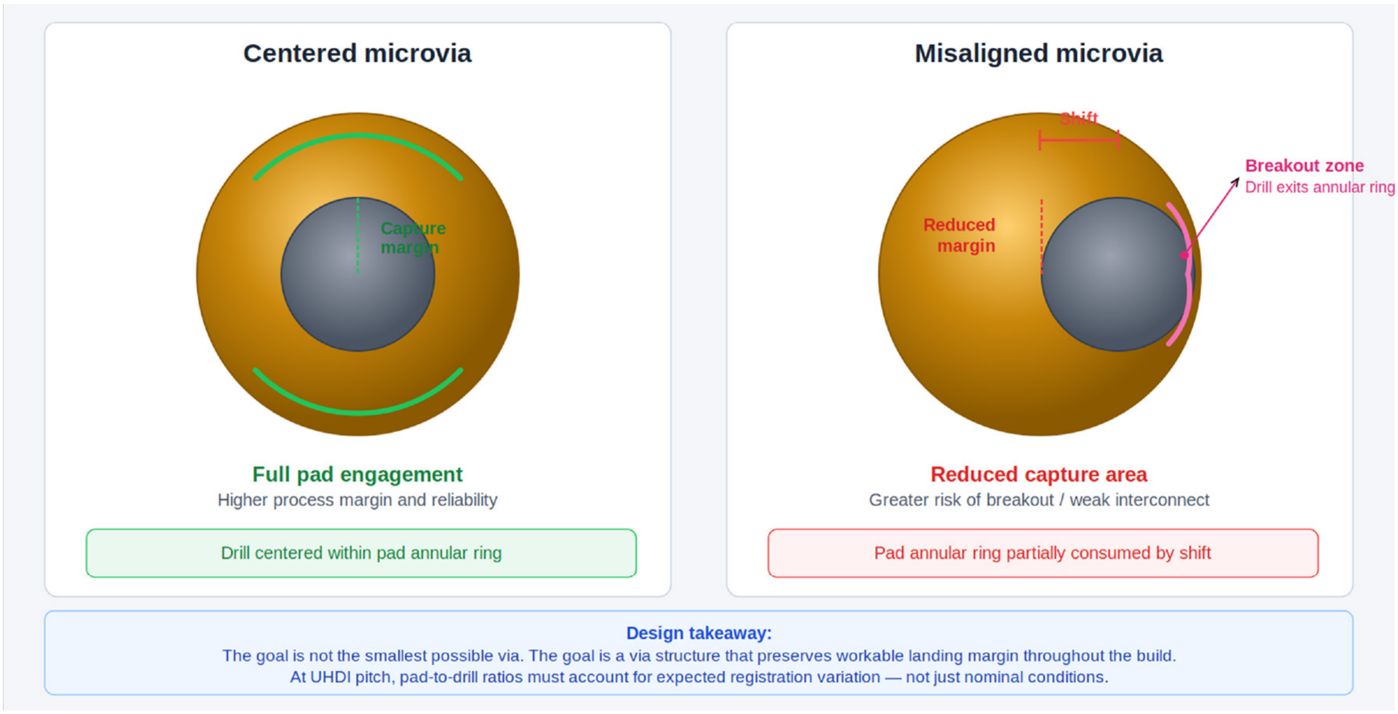

Figure 2. Microvia capture sensitivity. As capture pad geometry shrinks, even a modest positional shift can significantly reduce usable landing margin and long-term reliability.

Solder mask over fine-pitch features. Solder mask is one of the most underestimated design constraints in UHDI. At larger geometries, it often appears to simply follow the copper. At UHDI pitch, it becomes an active design parameter. As pad openings shrink and dams narrow, registration tolerance determines whether the intended isolation and exposure can be achieved. A layout can look acceptable in CAD but become difficult to build if the mask strategy assumes greater positional precision than the process can comfortably deliver.

That means solder mask can no longer be treated as a finishing detail. At fine pitch, it directly affects pad definition, isolation, assembly yield and the robustness of the overall design. **Figure 3** highlights how even a moderate mask shift can reduce exposed pad area and consume dam width in already-tight geometries.

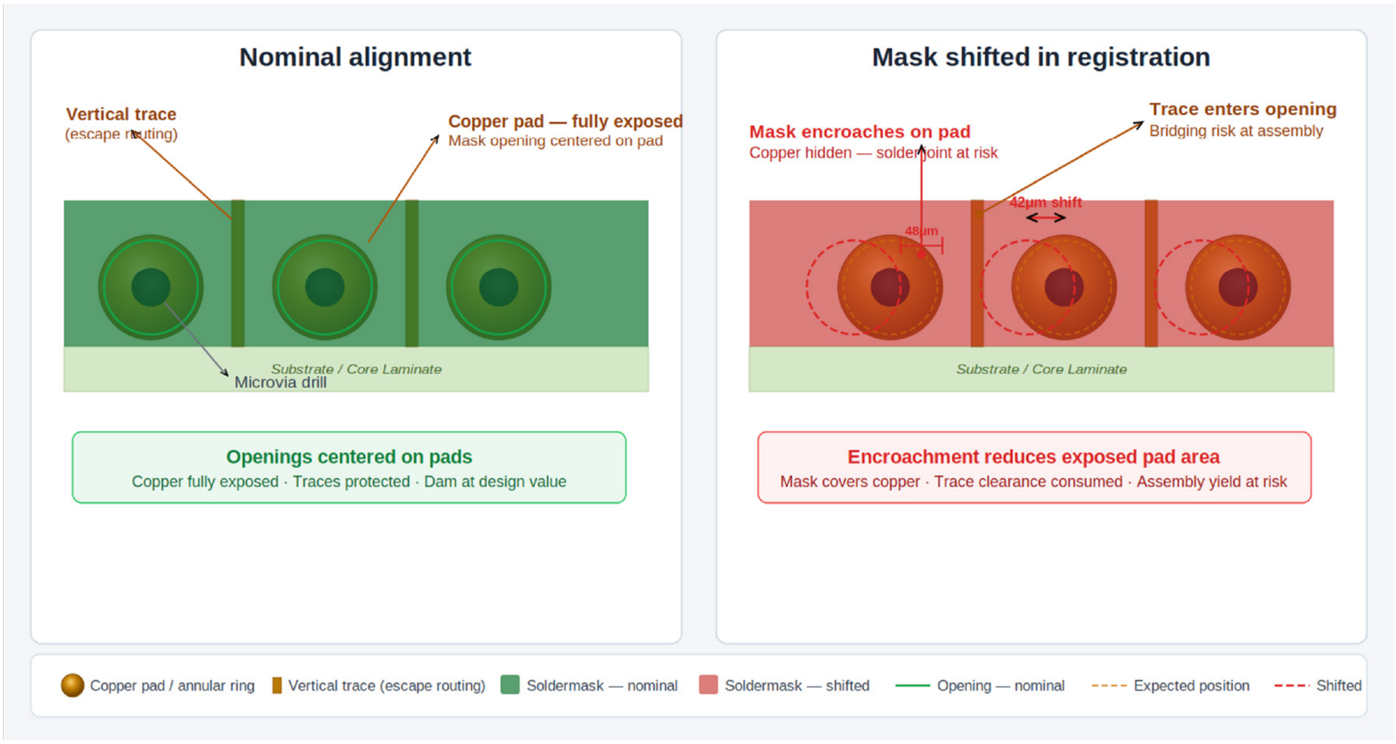

Figure 3. Fine-pitch solder mask alignment. Realistic registration shift can reduce exposed pad area and narrow mask dams enough to affect isolation and assembly yield.

Outer-layer trace-to-pad spacing. Outer-layer spacing is not only about copper-to-copper clearance. It must also account for how the pad is defined, how solder mask interacts with the feature and how much usable margin remains once alignment is considered. This is especially important in dense breakout areas where several marginal geometries are already competing for space.

High-density breakout zones. Fine-pitch BGAs, narrow escape channels, small vias and tight outer-layer spacing all converge in breakout regions. These areas tend to be the least tolerant of movement and the most vulnerable to cumulative tolerance effects. A useful review question is simple: where is this board least tolerant of positional variation? The answer usually identifies the first places yield will become uncomfortable.

Understanding likely failure modes helps a designer move from abstract discussions of tolerances to an actionable design review. In UHDI, the most common registration-driven issues include partial microvia capture, microvia breakout, stacked via misalignment through successive layers, solder mask encroachment onto pads, insufficient mask dam leading to bridging risk and trace exposure caused by shifted outer-layer relationships. None of these are random events. They are predictable consequences of insufficient design margin in the presence of normal process variability.

Practical UHDI Registration Design Guidelines

One of the most common mistakes in advanced layouts is using process minimums everywhere simply because they exist on a capability chart. If only one region of the board truly requires aggressive geometry, preserve margin elsewhere. Relaxing non-critical areas makes the overall design more manufacturable without sacrificing the dense region that actually drives the stackup.

In UHDI, solder mask affects pad definition, isolation, manufacturability and assembly yield. Designers should evaluate whether solder mask-defined features are appropriate, whether narrow dams are realistic, and whether the mask strategy needs to change in especially fine-pitch areas. Waiting until fabrication review to think about mask usually means the design has already given away too much margin.

One of the most useful anchors in UHDI remains the relationship between via size and dielectric thickness. A via structure that is too aggressive for the dielectric it is crossing becomes less forgiving and harder to build reliably. That affects more than drilling. It changes how much margin remains once registration, plating and stackup behavior are considered together.

Traditional design review often asks: do these features clear each other? UHDI review should ask a different question: do these features still work if they move slightly? That leads to better questions. Where is copper barely protected? Where is mask margin smallest? Where are vias landing with the least tolerance? Which structures depend on near-perfect alignment? This shift in perspective materially improves design robustness.

The right tolerance target is not ideal alignment. It is the actual process window that the fabricator can repeatedly hold. In practice, that means designing for realistic registration behavior, not for the best-case result shown by CAD. Preserving an extra increment of capture pad, mask clearance or spacing where possible often has an outsized impact on yield and repeatability.

UHDI is highly process-dependent, so generic assumptions are often insufficient. Early engagement with the fabricator can answer the questions that matter most: Is the mask strategy realistic? Is the capture pad too aggressive? Where is registration most likely to drive yield loss? Which areas would benefit from a little more margin? Designing for a real fabrication process is far more effective than designing for a theoretical capability chart.

This collaboration is also where tradeoffs become clearer. If a board absolutely requires one especially aggressive feature, the fabricator can often help identify where margin should be restored elsewhere so the overall design remains practical to build.

UHDI is not simply a more complex version of HDI. It is a more precise design environment. That means registration, alignment and tolerance stackup matter more, earlier and more directly than they do in traditional technologies. The good news is that these factors are not outside the designer's control. Designers who understand them can make better decisions earlier in the layout process and improve manufacturability before the board ever reaches the shop floor.

That is ultimately what makes UHDI worth mastering. When registration and alignment are treated as core design parameters rather than secondary fabrication concerns, UHDI delivers what it promises: better routing freedom, lower layer counts, improved electrical performance and new possibilities in dense, high-performance PCB architectures.

Conclusion

UHDI PCB design is not limited by what can be drawn in CAD. It is defined by what can be built repeatedly, reliably and within process capability. Registration, alignment and tolerance stackup are therefore not secondary manufacturing details. They are foundational design drivers. Teams that account for these factors early achieve higher yields, improved reliability and faster transitions to production. As UHDI adoption expands across RF, aerospace, medical, advanced computing and other high-density applications, those considerations will increasingly define successful PCB design.

ANAYA VARDYA is CEO of American Standard Circuits and ASC Sunstone Circuits. ASC works closely with customers and design teams on advanced PCB technologies, including RF, HDI, rigid-flex and ultra HDI, with a focus on turning complex fabrication realities into practical design guidance.

SUPPLY **CONSTRAINTS**

From Design Intent to Manufacturing Reality: Why Early Collaboration Still Wins in PCB Development

As laminate shortages reshape PCB development timelines, early collaboration is becoming critical to keeping complex designs manufacturable and on schedule.

by **GEOFFREY HAZELETT**

Printed circuit board development timelines continue to compress, driven by faster design cycles, tighter launch windows and increasing product complexity. While EDA tools and automation have improved dramatically, one long-standing challenge persists: translating design intent into a manufacturable, buildable and repeatable product.

In recent years, this challenge has been exacerbated by ongoing supply chain disruptions, most notably those affecting laminate materials. What was once a relatively stable assumption in stackup planning is now a dynamic engineering variable that directly impacts lead time, cost and program risk. In this environment, early collaboration between design, fabrication and assembly partners is no longer optional; it is foundational to successful execution!

The cost of late-stage discovery. Late-stage discovery of manufacturing constraints remains one of the most common drivers of PCB program delays. Issues such as unsupported drill-to-copper spacing, marginal aspect ratios, overly tight impedance tolerances or ambiguous fabrication notes often surface during front-end CAM review rather than during layout.

By the time these issues are identified, design decisions are already locked in. Resolving them may require stackup changes, rerouting, impedance recalculation or updated documentation, with each step introducing delay and risk. While these problems are technically solvable, they are far more costly to address after release than during initial layout planning.

Laminate supply-chain constraints are now a design variable. Laminate availability has become one of the most significant and least visible risk factors in PCB development. Lead times for certain resin systems, glass styles and high-speed materials remain volatile. Even within common material families, availability can vary by thickness, copper weight, glass weave or region.

Designs that specify a single laminate or tightly constrained stackup without alternates may unintentionally introduce supply chain risk. From an engineering standpoint, the issue is rarely that a material cannot meet electrical requirements; it is that the design does not allow flexibility when that material becomes constrained.

High-speed digital and RF designs, like PAM4 224G, which require controlled impedance traces, are particularly sensitive. Small changes in dielectric thickness, Dk, Df or glass style can affect impedance targets, insertion loss and skew. If these variables are not considered early, material substitutions become difficult or impossible without significant redesign and re-simulation.

In some cases, the constraint is so severe that the only viable mitigation is to secure laminate material early, sometimes even before the design is fully placed and routed. This approach may feel counterintuitive from a traditional workflow perspective, but it reflects the reality that material availability can now dictate schedule as much as layout complexity. This is not unheard of for designs with specialty connectors that have upwards of six-month lead times.

A real-world example. A customer recently released a high-layer-count, controlled-impedance design specifying a preferred laminate system based on prior builds. Electrical properties of the material were appropriate and well characterized. During front-end review, the fabricator identified a six-week lead time on the specific laminate family required to support the defined stackup, however.

Because the design allowed no approved alternates, the team faced a decision: accept the extended lead time or revisit the stackup, design and signal integrity model.

Due to strong cross-functional teams and strong alignment with their fabrication partner, the laminate material was identified and purchased ahead of layout completion, effectively decoupling material lead time from routing and release. While this required earlier cross-functional coordination, it significantly reduced schedule risk and eliminated last-minute material-driven redesigns.

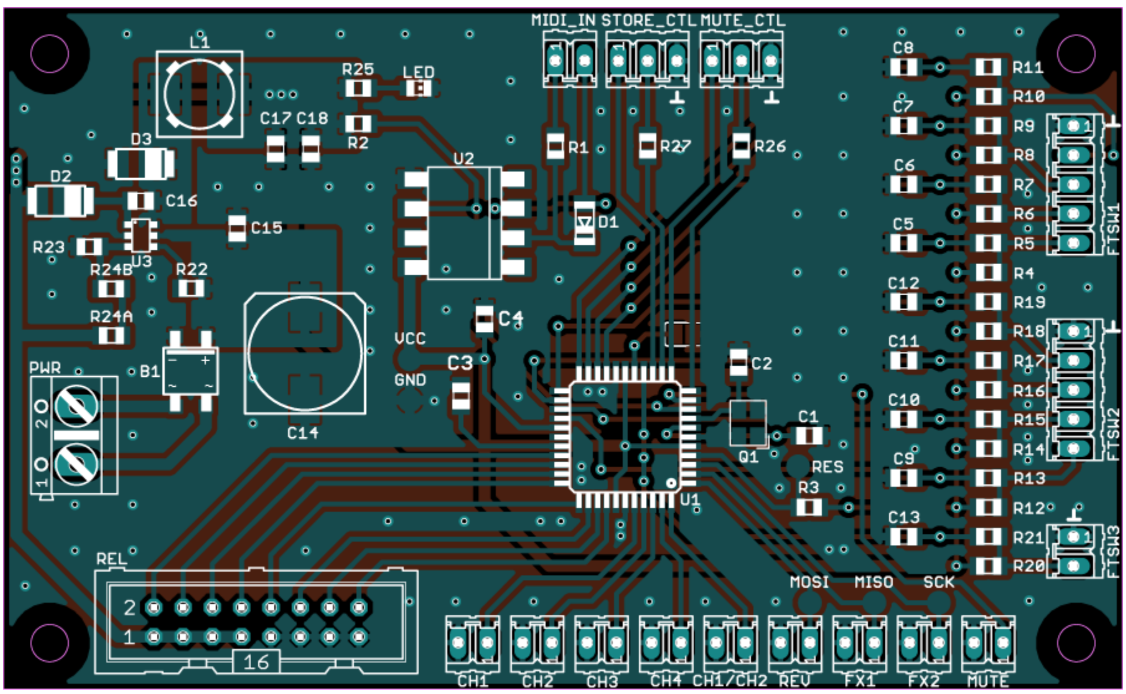

Figure 1. Early collaboration between PCB design, fabrication and assembly teams is becoming increasingly critical as laminate availability and stackup constraints reshape development timelines.

The takeaway was not that early purchasing is always required, but that laminate availability must now be considered alongside electrical and manufacturing constraints during design planning.

Shifting DfM and stackup planning left. Leading organizations are moving DfM activities earlier in the design cycle, engaging fabrication expertise during layout rather than after release. In today's environment, this approach must extend beyond traditional DfM into stackup planning with supply chain awareness.

Effective early collaboration often includes:

- Developing stackups with multiple electrically equivalent laminate options.
- Aligning impedance targets with materials that are broadly available and scalable.
- Identifying where early laminate procurement may be warranted to protect the schedule.
- Understanding which glass styles or resin systems introduce risk or long lead times.
- Evaluating where impedance tolerances can be relaxed without impacting performance.

By addressing these factors early, design teams gain clearer constraints, and fabricators receive data packages that reflect real-world manufacturing and sourcing conditions. Front-end engineering teams and external CAD service providers play a critical role in bridging the gap between design intent, fabrication capability and material availability. These teams often identify laminate risks during initial stackup definition – well before routing begins – and can recommend alternates or procurement strategies that preserve electrical performance while improving schedule certainty.

From an engineering standpoint, this collaboration helps ensure stackups remain impedance viable across multiple material sets, tolerances stay realistic for selected constructions and designs can withstand material substitutions without requiring layout changes. It also helps guide material procurement decisions based on actual design constraints. For OEMs and startups alike, leveraging experienced front-end and CAD support can be especially valuable when designs push high-speed, HDI or mixed-material boundaries.

Better RFQs Start with Better Engineering Assumptions

Many RFQ delays trace back to overly rigid or incomplete design data. Clear fabrication notes, well-defined impedance requirements, and realistic tolerances all contribute to faster, more accurate quoting for the PCB fabricators and assemblers. Increasingly, this also includes transparency around material flexibility and procurement timing.

Design packages that specify acceptable laminate alternates – or acknowledge when material has already been secured – tend to move through quoting faster and with fewer surprises. When engineering teams understand how material choices and availability influence cost, lead time and risk, RFQs become more predictable for everyone involved. Despite advances in tools and automation, PCB development remains a fundamentally collaborative process. In an era of ongoing laminate supply uncertainty, communication between design, fabrication, assembly and purchasing teams is more critical than ever.

Organizations that invest in early collaboration consistently experience fewer design spins, smoother transitions to production and more predictable schedules. By aligning design intent with manufacturing and material realities – sometimes even before layout begins – teams can reduce risk and deliver better outcomes.

As an industry, the solution is not more complexity but earlier-informed engagement, better assumptions and closer collaboration. When design and manufacturing work as a single engineering team, everybody wins.

GEOFFREY HAZELETT is a business development executive at Freedom CAD Services with deep expertise in printed circuit board design, fabrication, and assembly; geoffrey.hazelett@freedomcad.com. Outside of work, he spends time with his Border Collie and two Siamese cats.

BEYOND **BOOTHS**

PCB East 2026: The Conversations Kept Going

PCB East 2026 combined nonstop show-floor traffic, technical learning and after-hours networking into one of the event's busiest and most connected years yet.

by RYANN HOWARD

Trade shows have always had two versions of themselves.

There's the official one: conference sessions, booth demos, technical discussions, product launches and meetings squeezed between coffee runs and glances at schedules. Then there's the version that starts forming somewhere around the end of expo day, when people finally loosen their lanyards a little, gather in groups outside the venue and continue the exact same conversations they'd been having all day – just with food and slightly louder laughter.

PCB East 2026 felt like both versions operating at full speed. And honestly, I think Worcester had a lot to do with that.

The move to the DCU Center gave PCB East a noticeably different energy this year. The facility itself was an upgrade: open hallways, better traffic flow, bright spaces, conference rooms that were easy to locate and an exhibit hall that somehow managed to be packed without ever feeling claustrophobic. Attendance numbers reflected it too, with overall attendance up nearly 48% year-over-year and conference attendance climbing 38%.

Figure 1. Attendees packed the PCB East 2026 exhibition floor at the DCU Center in Worcester, where conversations, handshakes and impromptu reunions kept traffic moving from booth to booth throughout expo day.

The downtown location changed the rhythm of the show. Restaurants stayed full of engineers and fabricators long after sessions ended. Small groups formed naturally on sidewalks and at crosswalks. Conversations that started at booths somehow continued three hours later over appetizers. The after-hours atmosphere felt less like people escaping the conference and more like the conference simply spilling outward into the city.

And the people willing to spend all day talking to strangers on a busy trade show floor? Unsurprisingly, they were also the exact same people brave enough to grab a karaoke microphone later that night.

At one point, I remember standing on the third floor of the DCU Center looking across the street and noticing a glowing karaoke sign. I joked to a few people nearby that we should absolutely go after the expo wrapped up. It was one of those passing comments you make, expecting it to disappear into the noise of the evening.

Except this industry apparently operates on the most efficient game of telephone ever created.

The next day, people kept approaching me asking, "So … are we doing karaoke tonight?"

And somehow the message had fully circled back to me without a single distortion. Just pure, high-speed PCB industry communication infrastructure at work.

That openness is something I keep noticing the more shows I attend. Back in our November issue, I wrote about how trade shows remind us that none of us works in this industry alone. I thought that feeling was strong then. PCB East somehow amplified it even further.

You'll spend ten minutes talking impedance control with someone, only to discover twenty minutes later that they also know three people you spoke with at lunch and one person you met six months ago at another event entirely. Information moves quickly in this industry, but kindness somehow moves even faster.

People continue to be incredibly generous with their time, advice, introductions and encouragement. At this point, I'm not even sure I get addressed by my actual name most of the time anymore. It's usually just, "Oh, you!" followed immediately by a conversation already in progress.

Of course, there was still the usual trade show chaos mixed in with everything else.

The show floor traffic barely slowed down all day. Every aisle seemed full from the moment the exhibition opened. You'd stop to talk to one person and accidentally look up 20 minutes later, standing in the middle of a completely different conversation than the one you started in.

I kept having the same recurring panic all week: realizing there were still dozens of people I wanted to catch up with before the show ended. Which, let's be honest, is probably inevitable when your natural instinct is to continue talking indefinitely.

The technical side of the conference reflected that same energy. The exhibit hall stayed busy throughout the day with designers, assemblers, fabricators, students, software companies, test engineers and manufacturers all moving through the same space at once.

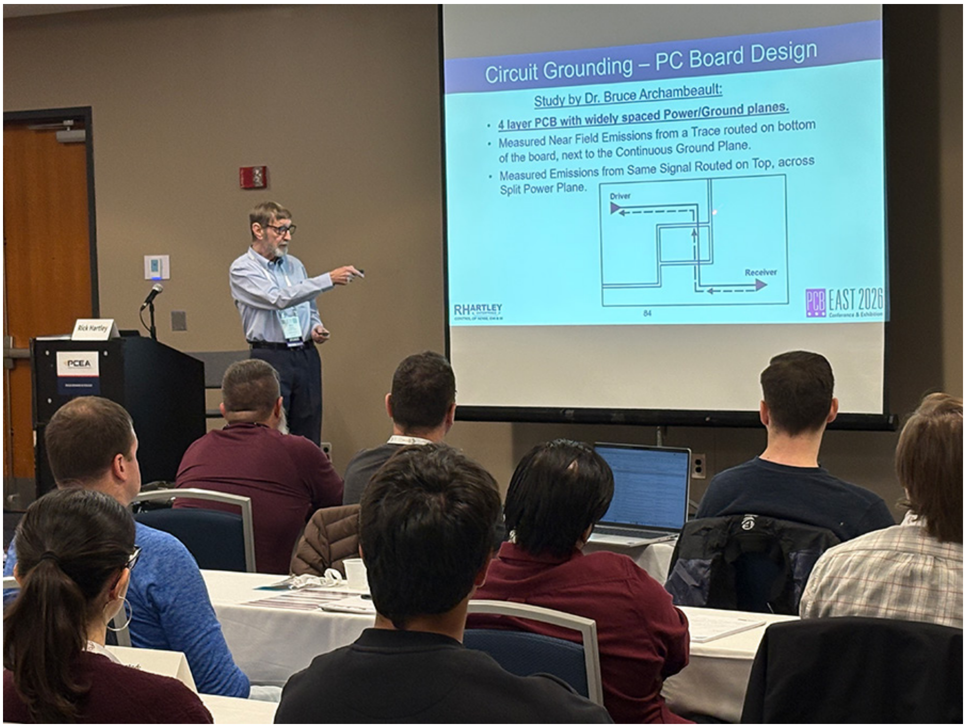

Figure 2. Rick Hartley's sessions once again drew packed rooms at PCB East 2026, as attendees gathered for practical design guidance from one of the industry's most recognizable instructors.

And then there were the moments that had absolutely nothing to do with PCB design whatsoever, but somehow still became part of the memory of the show.

Cofactr's after-hours arcade gathering turned into an unexpectedly competitive proving ground. I'm happy to report that I successfully claimed victory in arcade motorcycle racing. Unfortunately, I must also transparently disclose that Dance Dance Revolution and race car simulators humbled me almost immediately.

Some losses build character. Others simply build witnesses.

By the end of the week, the days had blurred together in the strange way trade shows always do. The hours moved fast. The conversations moved faster. Somehow, you're constantly exhausted and energized at the exact same time.

And that's probably the best way I can describe PCB East 2026 overall. The event felt alive.

Not just professionally successful – though it absolutely was – but genuinely alive in the way only strong industry communities can feel when everyone is fully engaged at once. The venue upgrade helped. The attendance growth helped. The nonstop traffic certainly helped. But the real heartbeat of the show was still the people willing to keep showing up for each other year after year.

The Yearbook Effect

A few days after I got home, my PCB East card from Zenode ended up sitting on my desk. You know the one – the custom Titan cards everyone was lining up for on the show floor. Mine happened to feature a photo of me in a blazer, professionally lit and looking significantly more organized than I usually am.

My four-year-old son spotted it almost immediately. He picked it up, stared at it for a second, then looked at me with complete sincerity and said, "That doesn't look like you."

Which, honestly, was devastating in the funniest possible way. Especially because, at the time, I had just gotten home from a workout, with my hair doing things no brush could reasonably fix and wearing gym clothes anchored by a decade-old Braves T-shirt my father gave me years ago. Standing there next to the polished version of myself on that badge photo felt less like "business professional" and more like catching a glimpse of an alter ego I apparently only unlock near convention centers.

What can I say, kids are honest.

I assured him that yes, it was in fact me. That's just apparently what I look like when I go on work trips and briefly transform into a person who owns multiple blazers and willingly wears plaid pants in public.

To prove it, I pulled up photos from our new PCB East yearbooks – one of my favorite additions to this year's event. What started as us simply taking too many photos turned into something bigger: a snapshot of the community itself. Conversations on the show floor. Friends reconnecting. Speakers teaching packed rooms. Booth teams posing together after long days. Tiny moments that would've otherwise disappeared once the booths came down.

Figure 3. The NCAB Group team's matching shirts and energy were captured in the PCB East 2026 Yearbook.

So I sat there scrolling through photo after photo.

"There's me in another blazer." "There's me pretending I know how to take a selfie." "There's me standing next to people I've talked about all week." "Yes, somehow the plaid pants happened more than once."

And the funniest part was watching him slowly realize that this whole other world exists when I leave for these events. To him, I'm just Mom working from home, typing at a laptop while occasionally muttering about deadlines and trying to remember where I left my coffee. Trade shows probably sounded imaginary.

But those yearbook photos captured something I've started appreciating more every time I attend one of these events: this industry feels incredibly human.

Behind all the technical discussions, challenges and packed schedules are people who genuinely enjoy seeing each other again. People who stay connected between shows. People who welcome new faces quickly. People who somehow turn a professional conference into a place where a karaoke plan can spread across an entire industry in under 24 hours.

And now, apparently, people who unintentionally convinced my son that I secretly live a double life in business casual sweaters.

Maybe that's part of what makes these events stick with me long after the flights home and unpacked suitcases. The yearbooks preserve the people inside the conference. The laughter between sessions. The conversations that ran long. The familiar faces that somehow start feeling like part of your routine.

And somewhere between the show floor photos and my son realizing I apparently own nicer clothes than he thought, I found myself appreciating something simple: for a few days each year, this industry becomes a place you can physically walk through. A place full of voices, personalities, friendships and stories – all moving faster than the crowd at the front door.

RYANN HOWARD is managing editor of PCD&F/Circuits Assembly; ryann@pcea.net.

PCB East 2026: Bigger Venue, Bigger Crowds

PCB East 2026 celebrated its move to Worcester with an increase in conference classes, exhibitors and attendance.

by ANDY SHAUGHNESSY

I've always enjoyed attending PCB East, but this year was even better because I was there as a PCEA staff member.

As some of you may recall, I worked with Mike Buetow and Frances Stewart years ago as editor of *PCD&F* and conference chair for PCB East and PCB West. The show felt like Homecoming Week. It's funny how the old "show mentality" kicked back in after I spent years away from putting on shows and conferences.

There's never a dull moment in trade show world.

"Where's the power drop for these booths?"

"Are we going to run out of food?"

"Does anyone know the venue's Wi-Fi password?"

The show's relocation from Boxboro to Worcester was the hot topic of conversation. Attendees, speakers and exhibitors that I spoke with were universally happy with the new venue, the DCU Center in downtown Worcester.

This is reflected in the show numbers, with attendance up almost 48% over last year. Realtors often point to the importance of "Location, location, location," and that certainly holds true in the Boston metro area. We learned one lesson years ago: Many people avoid driving into Boston.

Figure 1. Speakers Rick Hartley and Susy Webb check in at the registration desk.

The second PCB East was held in 1997 at the Hynes Convention Center in downtown Boston, and attendance was lighter than expected. Later, designers and manufacturers in New England told us that they'd rather commit hara-kiri than drive into the city.

Since that show, PCB East has been held outside the city in suburban areas. The Boxboro Regency was home to PCB East for years, but the hotel's layout wasn't ideal for a trade show. By 2025, it was clear that the show had outgrown that venue.

The move to the DCU Center in Worcester turned out to be a huge upgrade. This venue is light and bright, and much more open, with a better traffic flow in and out of the show floor. And, as one speaker joked, the conference rooms are all in the same zip code. The DCU Center is also within walking distance of a variety of restaurants and bars, which is a bonus.

Figure 2. The high-speed design classes at PCB East were very popular, as usual.

Another topic on everyone's mind was AI. Many of the classes covered AI in design or manufacturing, and Sean Patterson's PCB Management Forum keynote discussed what managers need to know to implement AI within their companies. As he pointed out, it's up to managers to lead with AI and not just farm it out to an "AI guy" in the IT department.

I visited the conference classes, and the two classes that were standing room only both dealt with EMI: Rick Hartley's "Circuit Grounding to Control Noise and EMI" and Gerry Callahan's "SMPS Layout – PCBA Design Practices to Avoid EMI." Both classes had over 50 attendees.

The rain that was forecast for the week of PCB East was delayed for a few days, and the sun was shining on expo day. The show floor was jammed for the first couple of hours, and it stayed busy throughout the day. Among the expo attendees, I ran into designers, fabricators, EMS providers, test engineers, and even a few chip designers.

Figure 3: The show floor was busy all day, from opening through teardown.

I also met quite a few college students, which is a big plus. We need to expose as many students as we can to this industry, because I don't think they get much PCB content at their universities. That's one benefit of having a show in Worcester: there are dozens of colleges nearby, including eight in Worcester. (For music trivia fans, the Jimi Hendrix Experience album "Live at Clark University" was recorded there in 1968, with tickets selling for $3 and $4.)

Exhibitors were happy with the new location and the turnout. "Beer on the Floor" was a big hit, of course. Overall, everyone I spoke with was bullish on the future of PCB design and manufacturing, and excited about new technology. Designers were a little worried about filling the open PCB designer positions as the boomer class heads toward retirement.

But the number of young people at PCB East was a good sign. Are PCB design and manufacturing careers becoming hip again?

I spent much of expo day conducting interviews for our *Talking Heads* video program. These engineers and managers were excited to share the news about their latest innovations, equipment and processes.

It's nice to see so many technologists becoming more at ease with the video interview format. Not long ago, companies in this industry might have had one person with the chops to do an on-camera interview. Now, each member of the design team or process flow wants to be interviewed. I think we can thank Joe Rogan, Amy Poehler and their fellow podcasters for helping to eliminate the "fear of the red light."

Now, we're all getting ready for PCB West. The show must go on!

I'm so happy to be back working with Mike and Frances again, as well as my new co-workers Ryann Howard, Will Bruwer and Leah Spinks. I'm lucky to work with such a great team.

I'll see you all again on the road!

ANDY SHAUGHNESSY is content architect of PCD&F/Circuits Assembly; andy@pcea.net.

WORKFLOW **MATURITY**

From Chat to Workflow: Turning AI Habits into Automated Processes

Moving from personal AI habits to standardized workflows can help manufacturing teams save time, improve consistency and scale practical AI use across operations.

by **SEAN PATTERSON**

It's 6:47 a.m., and Robert is doing what he does every morning before the production standup. He opens his AI chat, pastes in last night's shift handoff notes and types the same prompt he's typed every day for three weeks: "Summarize these production notes. Flag anything that needs immediate attention. Prioritize by customer impact."

Twelve seconds later, he has a clean briefing. The plating line hiccuped on the second shift. The AOI false-positive rate is creeping up on the flex jobs. The Acme order that shipped two hours late. He scans it, adds his own judgment on the Acme situation and walks into the standup with a clear picture instead of a foggy one.

Here's what Robert hasn't noticed yet: he just built a workflow.

Not the kind with flowcharts and IT tickets. The real kind. The kind where a task that used to eat up 20 minutes of his morning now takes two. The kind where the quality of his standup prep no longer depends on whether he got enough sleep. He has a repeatable process that produces consistent results. That's process engineering. He just didn't recognize it because no one had drawn a value stream map.

If you followed along with the first three articles in this series, you've probably built a few of these yourself. A prompt you keep coming back to. A way of feeding AI your context that works better than it used to. A habit that stuck. Good.

Now it's time to do something with it.

This article begins the second pillar of AI maturity: moving from personal AI habits to business workflows. Not because the habits weren't valuable. They were the foundation. But a prompt you type by hand every morning is a manual process. And if there's one thing manufacturing professionals understand, it's that manual processes don't scale.

This is where most people get stuck. BCG's June 2025 *AI at Work* report found that 72% of workers use AI regularly, but only 13% have AI agents running inside their actual workflows.[1] That gap, between using AI and having it embedded in how work gets done, is exactly what Pillar 2 closes.

If you've spent any time in process engineering, you've seen this progression a hundred times:

Level 1: manual. Someone does a task from memory. Results vary by who does it and how their day is going. This is where most people start with AI. Open the chat, type something, get something back.

Level 2: documented. Someone writes down the steps. Now, anyone can do it the same way. In AI terms, this is when you save your prompt. You stop rewriting it from scratch every time. You have a template with blanks to fill in. MIT Sloan's David Robertson put it bluntly in August 2025: "The current state of the art in prompt engineering is to not do prompt engineering."[2] For repeatable tasks, templates beat rewriting every time.

Level 3: standardized. The documented process gets refined. Inputs are defined. Outputs are consistent. Quality checks are built in. For AI, this means your saved prompt includes specific context fields, output format requirements and verification steps. You know exactly what to feed it and exactly what to expect back.

Level 4: automated. The standardized process runs with minimal human intervention. Triggers fire it. Data flows in. Results flow out. A human reviews the output, not the process. This is where AI workflows live. Your morning production summary pulls shift notes automatically, runs through your proven prompt and lands in your inbox before you pour your coffee.

You've been climbing this ladder in manufacturing for your entire career. Every work instruction, every SPC chart, every automated test sequence followed this same path. Someone did it manually first. Then they wrote it down. Then they standardized it. Then they automated it.

AI adoption follows the same progression. The difference is speed. What took months with a new piece of shop floor equipment takes days with AI. You already have the mental model. You just need to apply it.

And the daily habit matters more than most people realize. A February 2025 Federal Reserve Bank of St. Louis study on AI productivity found that workers who use AI daily are nearly three times more likely to save four or more hours a week than workers who use it occasionally.[3] Frequency of use is what turns AI from a curiosity into a measurable return.

The question isn't whether you can build AI workflows. You already proved that with your daily habits. The question is: which habits are worth promoting to the next level?

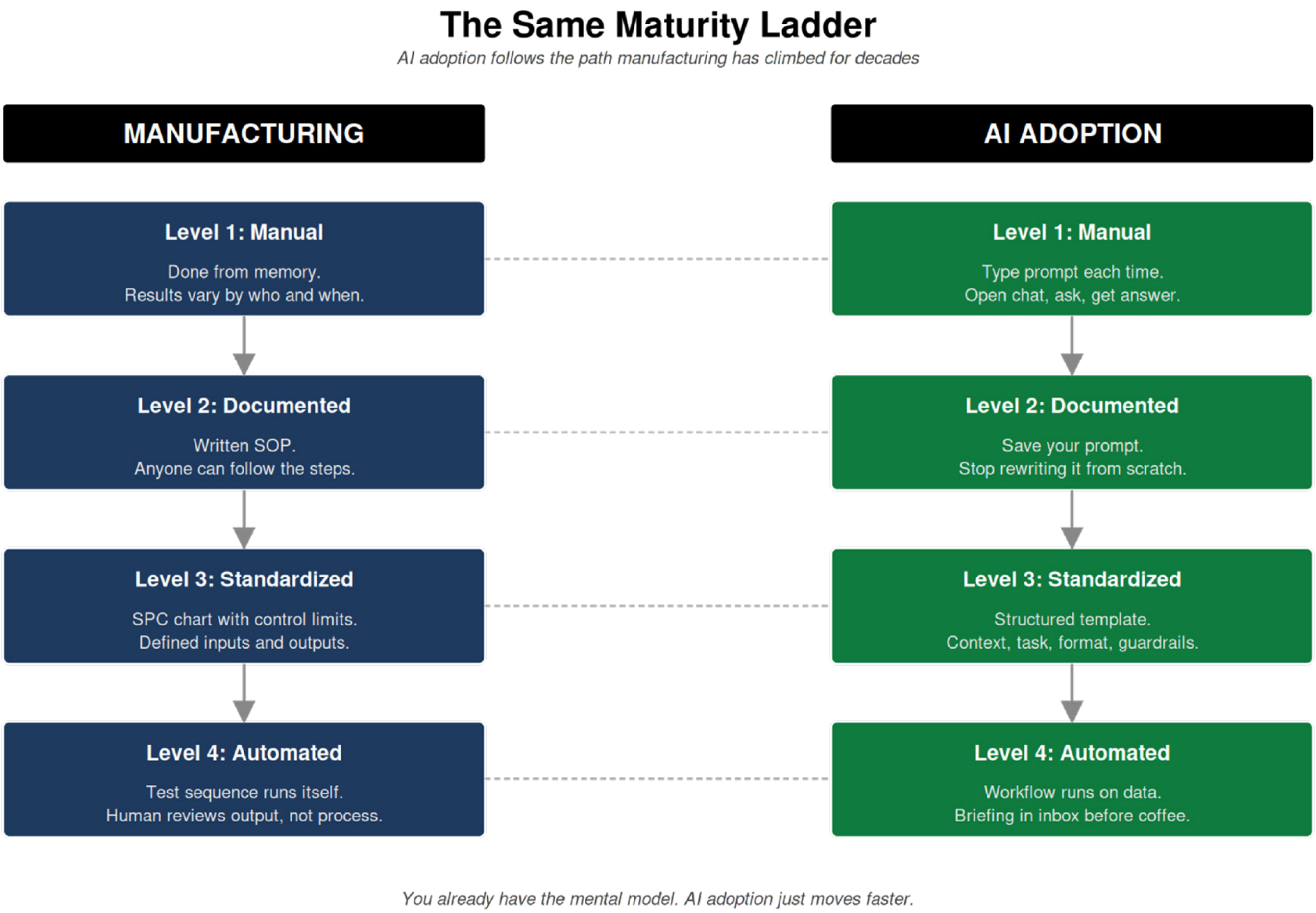

Figure 1. AI adoption in manufacturing environments often follows the same progression as traditional process maturity, moving from manual tasks to documented, standardized and eventually automated workflows.

The Three-Question Filter

Not every AI habit deserves to become a workflow. Some prompts you use once a month. Some require so much human judgment that automating the input would save you 30 seconds and lose you 30 minutes of nuance. The goal isn't to automate everything. The goal is to automate the right things.

Here's a simple filter. Ask three questions about any AI prompt you use regularly:

1. **Do I do this more than twice a week?** Frequency is the first signal. Robert's morning production summary happens every single day. His quarterly board report happens four times a year. Both use AI, but only one has the repetition to justify building a workflow. If you're doing something daily or multiple times per week, the cumulative time adds up fast. Five minutes a day, five days a week, 50 weeks a year. That's over 20 hours on a single task. For Robert specifically, 15 minutes saved each morning adds up to 60-plus hours a year back in his pocket.
2. **Does the input come from somewhere predictable?** Robert's shift notes come from the same MES every morning. The format is consistent. The location is known. That's a predictable input. Contrast that with a one-off customer complaint email that could come from anywhere, about anything, in any format. Predictable

inputs mean you can connect the data source to the workflow directly instead of copying and pasting by hand.

3. **Does the output go somewhere consistent?** Robert's morning briefing goes to his standup meeting. Every time. Same audience, same format, same purpose. If your AI output always ends up in the same report, email or dashboard, that's a workflow candidate. If the output goes to a different place every time, it might be better as a manual prompt with flexibility.

Three yeses? That's a workflow. Two yeses? Worth turning into a saved template. One or zero? Keep it as a manual habit. That is still Pillar 1 working exactly as it should.

Walk through your AI usage from the past two weeks. You'll probably find two or three prompts that pass all three questions. Those are your starting points. Don't try to automate 10 things. Pick the one that saves the most time or causes the most frustration when you forget it.

Run Robert's morning briefing through your own filter. Does he do it more than twice a week? Yes, daily. Does the input come from a predictable source? Yes, the same MES, the same format, every morning. Does the output go somewhere consistent? Yes, the standup, same audience, same time. Three yeses. That's a workflow.

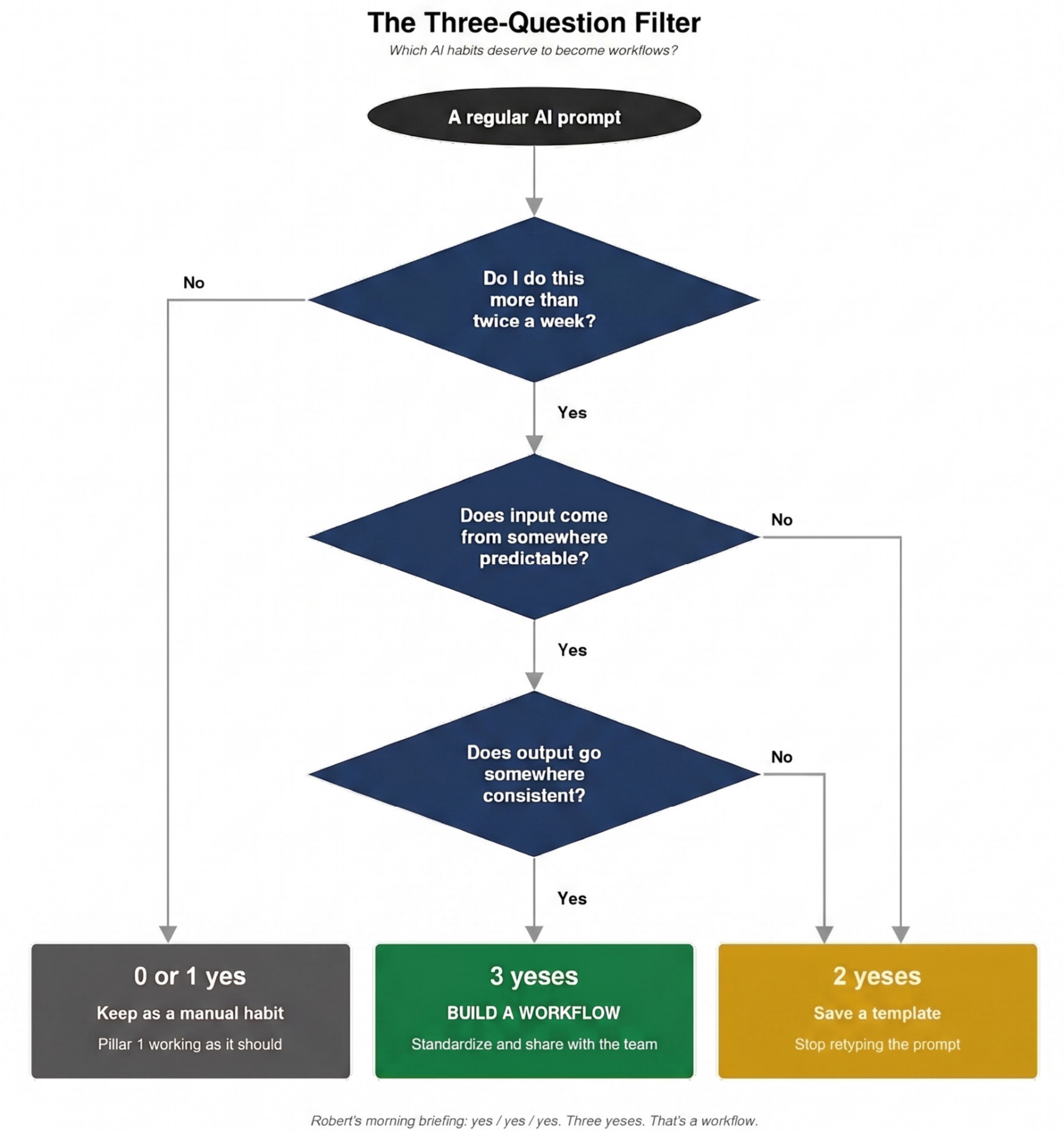

Figure 2. The "three-question filter" offers a simple framework for identifying which recurring AI habits are ready to become structured workflows within engineering and manufacturing environments.

The Daily Production Briefing

Let's take Robert's morning habit and turn it into a real workflow. Here's what he started with, the prompt he typed by hand every day: "Summarize these production notes. Flag anything urgent. Prioritize by customer impact."

That worked. But it's Level 1. Manual. Depends on Robert remembering to do it, remembering the right phrasing, and having time to paste in the notes before standup. Here's what the same task looks like as a Level 3 standardized workflow template. Level 3 is standardized and repeatable but still requires you to paste your shift notes each morning. Level 4, where the notes flow in automatically, is a later article. For now, Level 3 is the right goal because it is the step most people skip.

[WORKFLOW TEMPLATE]
DAILY PRODUCTION BRIEFING WORKFLOW

CONTEXT: I am a fabrication operations manager responsible for [number] production lines running [product types]. My standup meeting is at [time] with [audience: shift leads, quality, planning].

INPUT – Paste last shift's handoff notes below:

[PASTE SHIFT NOTES HERE]
TASK: Analyze these shift notes and produce a standup briefing with the following structure:

1. IMMEDIATE ACTIONS (must address before end of today)
    - Safety issues first
    - Customer-impacting quality escapes
    - Equipment down affecting throughput
    - Overdue preventive maintenance on production equipment
2. WATCH LIST (monitor today, act if trending)
    - Yield trends outside +/- 2 sigma
    - Process parameter drift
    - Delivery schedule risks
3. WINS AND IMPROVEMENTS (celebrate progress, reinforce standards)
    - Jobs completed ahead of schedule
    - Quality metrics improving
    - Process improvements showing results
4. QUESTIONS FOR THE TEAM
    - Items that need input from specific people
    - Decisions that cannot wait until next standup

FORMAT: Keep each item to one sentence. Use plain language, not system codes. Flag the single most important item with [PRIORITY].

IMPORTANT: Do not fabricate data. If the shift notes don't contain enough information to assess a category, say "insufficient data" rather than guessing.

[END WORKFLOW TEMPLATE]

Notice what changed. The context is defined. The input location is clear. The output format is specified. The guardrails are built in. Anyone on Robert's team could use this template and get a consistent, useful briefing. That's the difference between a habit and a workflow.

What this replaces: 15 to 25 minutes of reading raw shift notes, mentally sorting priorities, and hoping you didn't miss something buried on page three. AFPM documents full-shift handover meetings that run 15 to 30 minutes for most operations; the manager's pre-standup note review is a meaningful slice of that window.

What AI does here: Organizes, prioritizes and formats information you already have. It applies a consistent framework, so nothing falls through the cracks.

What AI does NOT do: Generate production data, make go/no-go decisions on quality holds, assess customer relationship sensitivity or replace your engineering judgment on which issues are truly urgent. You still make the calls. AI organizes the information so you can make better calls faster.

When to use it: Every morning, 15 minutes before standup. Make it the first thing you do when you sit down. If you built the habit from article 3, you're already doing this. The template just makes it consistent.

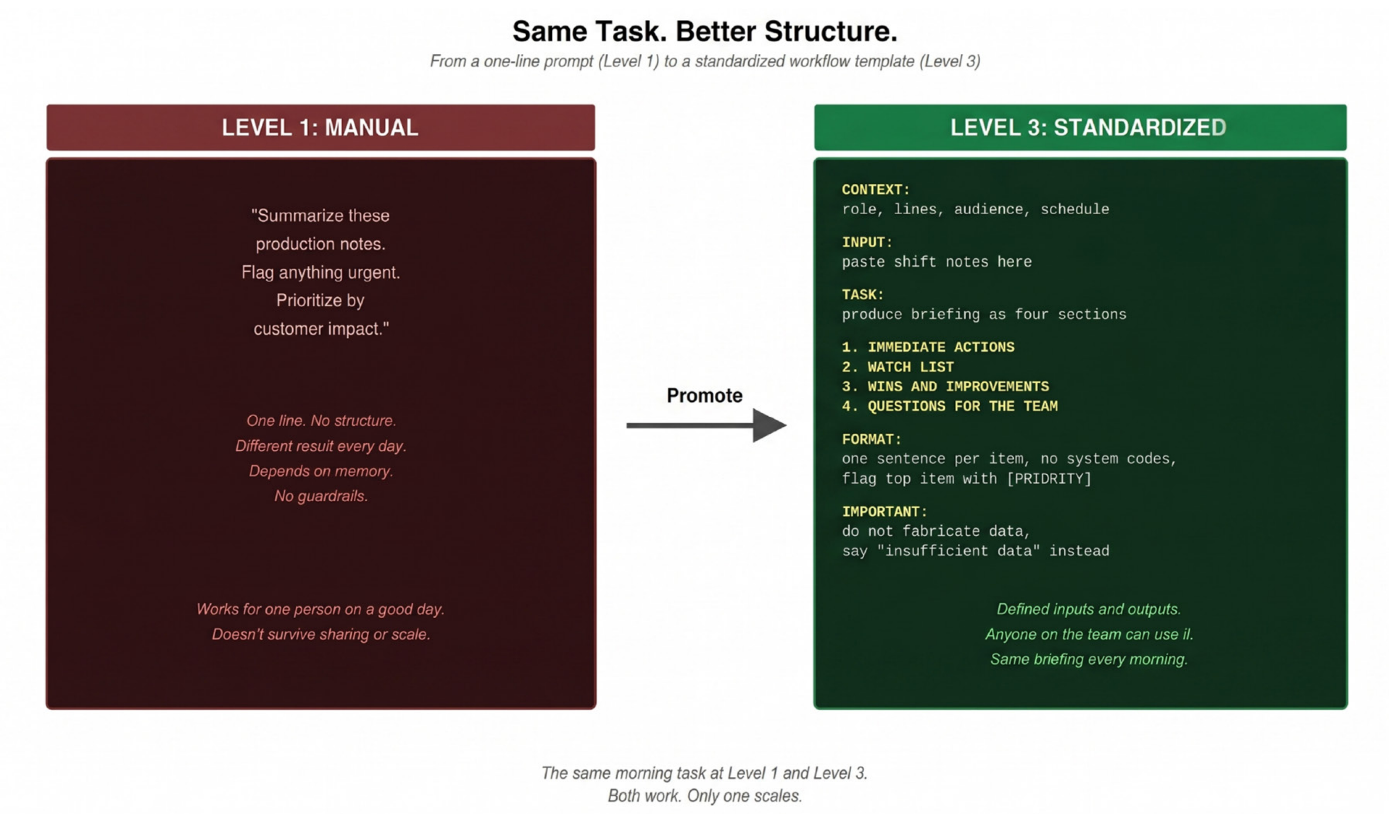

Figure 3. Standardized AI workflows replace inconsistent one-off prompts with structured templates that define context, inputs, tasks, formatting and output expectations for repeatable team use.

Here's where the real value appears. Robert built that production briefing workflow for himself. It saved him 15 minutes a morning. That's good. About 60 hours a year, he gets back. But Robert manages three shift leads. Each of them faces the same morning problem: raw notes, limited time, inconsistent prioritization.

So, Robert shares the template. Not with a training session or a PowerPoint deck. He drops it in a shared folder and says, "Try tomorrow morning. Paste your shift notes where indicated. Tell me if it works."

Two of the three leads try it that week. One of them modifies the output format to include a section for maintenance requests because his shift has more equipment issues. The other adds a customer-specific section because she handles the high-reliability military contracts. Within a week, they've adapted it to their context. They didn't need Robert's permission or IT's involvement. They just used it.

This is what "teach your team to automate" looks like in practice. Robert didn't automate his team. He didn't hand them a tool and walked away. He shared a working pattern and let them make it their own. The workflow became a team standard because it earned its way there, not because someone mandated it.

This isn't just a preference. PwC and the Manufacturing Institute, in a Q3 2025 survey of operations leaders, found that 45% of failed AI initiatives in manufacturing traced back to excluding frontline leaders from design and rollout.[4] Mandated tools fail. Templates that earn their way through demonstration succeed. The data is unambiguous.

This is not just a fab floor dynamic. A design engineer I work with took the same framework and built a template for her PCB design reviews. Same four-section output structure, but her INPUT field is a netlist diff and a stackup change list, and her IMMEDIATE ACTIONS section flags impedance-critical traces and DRC violations instead of plating issues. Same workflow, different domain. The structure is universal because the underlying problem is universal: turn raw input into a prioritized briefing without losing what matters.

In 25 years of running operations across submarines, PCB fabrication and high-volume manufacturing, and in my work with hundreds of engineers and managers since, the pattern is consistent. The workflows that stick are those that start with one person solving their own problem, then spread to the team through demonstration. Not the ones that start with a company-wide rollout.

The progression looks like this: One person builds a habit. That habit becomes a workflow. That workflow gets shared. The team adapts it. Now you have a standard process that everyone owns because everyone helped shape it. That's continuous improvement. You've been doing it for decades. AI just accelerated the cycle.

A note on data sensitivity: When sharing AI workflow templates with your team, keep proprietary data out of the template itself. The template defines the structure and instructions. The sensitive data, your shift notes, yield numbers, and customer names, get pasted in at runtime by each user in their own AI session. The template travels. The data stays local. This matters for IP protection and customer confidentiality.

Conclusion

It's 6:42 a.m. on a Monday, five weeks after Robert first noticed his morning pattern. His production briefing workflow is saved. Each of his three shift leads has their own version. The second-shift lead added a section on maintenance priorities. The flex circuit specialist customized her output to flag impedance-critical jobs separately.

Robert opens his briefing. It's already formatted the way he likes it. The plating line is running clean. The AOI false-positive rate dropped back to baseline after they recalibrated on Friday. One customer delivery is at risk because of a material delay, flagged as the priority item.

He didn't build a software system. He didn't file an IT request. He didn't attend a training seminar. He took a habit, gave it structure, and shared it with his team. Five people now start their mornings with consistent, prioritized information instead of raw data. The total investment to get here was maybe two hours spread across a month.

That's the second pillar of AI maturity. Not buying a platform. Not deploying a solution. Building workflows from the habits you already have, then letting your team make them better.

Your action this week: Take your most-used AI prompt. Run it through the three-question filter. If it passes all three, convert it into a structured workflow template using the format in this article. Share it with one colleague by Friday. Ask them what they'd change.

Next article, we'll tackle the workflow opportunity that every single person in manufacturing shares, regardless of role: the administrative burden that eats your actual engineering time. Documentation, reporting and the paper trail that never ends.

About This Series

This is the fourth article in a series exploring practical AI adoption for PCB design and manufacturing professionals. With this article, we begin Pillar 2 of the Three Pillars of AI Maturity: building business workflows from the daily habits established in Pillar 1.

Article 1: Building Relationships with Technology (Why personal capability beats purchased solutions)
Article 2: AI 'Hallucinates.' Why That's Actually Good News.(How to get reliable, specific outputs from AI)
Article 3: Why Your AI Training Isn't Sticking (Turning knowledge into daily habits)
Article 4: From Chat to Workflow (Turning habits into automated workflows) ← *You are here*
Coming Next: Administrative Burden Reduction. The workflow opportunity every person in manufacturing shares: documentation, reporting and the paper trail that never ends.

This isn't about buying AI solutions. It's about developing your team's AI capabilities.

We can help.

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SEAN PATTERSON is an accomplished executive with extensive C-suite experience across CRO, COO, and CTO roles who now specializes in humanizing artificial intelligence implementation in business environments, particularly manufacturing; sean@crossgen-ai.com.

Patterson’s unique approach to AI implementation stems from his multifaceted leadership experience in the PCB industry, including serving as COO and CTO & head of AI at Summit Interconnect, various senior positions at TTM Technologies, and CRO of Nano Dimension. He built Amazon’s tractor trailer division and healthcare platforms. He currently serves as COO of StartGuides, providing military technology working backwards from the soldier. He is also on several nonprofit AI advisory boards in education.

Patteson brings practical insights into how PCB manufacturers can approach AI adoption strategically. His methodology emphasizes cultural adoption from the top, employee empowerment, and then automation. His approach to AI implementation is captured in his often-quoted principle: “AI adoption is not something a leader can delegate.”

Patterson holds a master’s in nuclear science and engineering from MIT and a bachelor’s in systems engineering with a focus on robotics from the United States Naval Academy.

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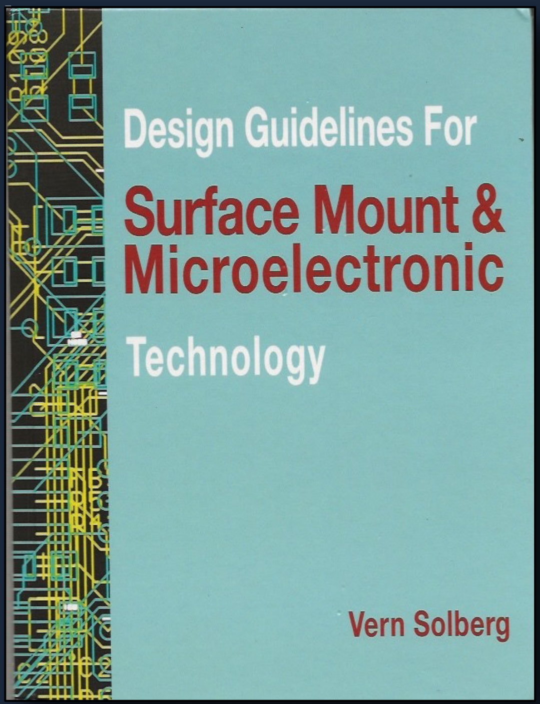

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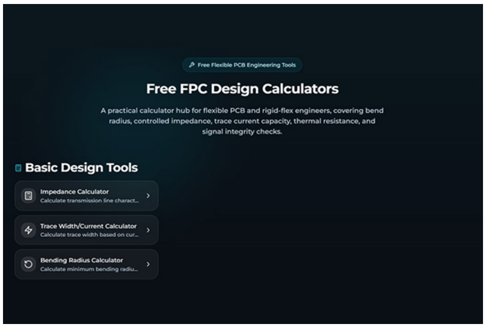

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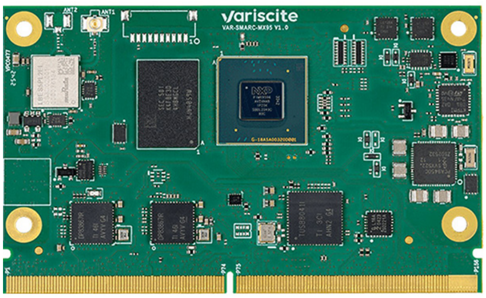

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In Case You Missed It

Conductive Adhesives

"An Electrically Conducting Water-based Reversible Adhesive"

Authors: Bassam A. Aljohani, Ama B. Asiedu-Asante, Adriana Sierra-Romero, Katarina Novakovic, Volker Pickert and Mark Geoghegan

Abstract: An electrically conducting reversible adhesive with conductivity up to 2.9×10^5 S m^{-1} and lap shear strength of up to 1.5MPa is presented. The reversibility of the glue enables debonding of surfaces on exposure to alkaline media. The adhesive comprises polyelectrolyte-stabilized nanoparticles synthesized by emulsion polymerization and silver nanoparticles as conductive filler. The conductivity of these formulations is comparable to, or exceeds, that of commercially available conductive adhesives, while their mechanical performance is consistent with typical water-based adhesive systems. Adhesion is reversed by immersing the bonded joints at pH 14. By heating to 85°C and stirring the solution (500rpm), the debonding time can be reduced to ~30 min or less. Separation can also be achieved at 85°C at pH 7. Short debonding times can also be achieved at room temperature by using acetone, a recognized green solvent. This electronically conducting reversible adhesive, therefore, presents a great opportunity to improve the reuse or recycling of electronic components. *(Advanced Electronic Materials,* May 14, 2026; https://advanced.onlinelibrary.wiley.com/doi/10.1002/aelm.202500617*)*

Electrothermal Modeling

"Simulation of Electrothermal Transient Responses in Power PCB Modules Using Comsol, Spice, and Asonika-TM"

Authors: K. O. Petrosyants, I. A. Kharitonov and M. S. Tegin

Abstract: Large temperature jumps in the structures of power semiconductor devices when they are turned on and off significantly reduce the reliability of power circuits. The widely used electrothermal modeling approaches for thermal circuits have a number of disadvantages: the use of interconnected Spice simulators and the numerical 3-D thermal field modeling tool requires a detailed description of 3-D structures and significant computer time; the use of only Spice-like simulators of electrical circuits for mixed electrothermal modeling requires the creation of electrothermal models of power components and significant CPU time costs due to the large difference in the time constants of the electrical and thermal parts. In this study, an improved scheme for multilevel automated electrothermal modeling and simulation of power electronic components is proposed and implemented, using the Comsol software at the semiconductor device level, Spice simulation at the circuit level, and the Asonika-TM system

at the printed circuit board (PCB) level. The developed additional software tools for implementing the proposed route are described, providing automation of power-calculation processes for components of power circuits, transferring the obtained values to a thermal simulation tool, and forming electrothermal models of the circuit components. The correctness of the proposed modeling scheme is confirmed by the results of thermal-imaging analysis using an IR camera. The effectiveness of the proposed methodology is demonstrated through the example of a real PCB design with high-power MOSFETs for controlling a power stepper motor. In the analyzed circuit, a possible thermal failure of the output DMOSFETs due to their overheating is revealed. To improve the conditions for reducing their temperature, it is proposed to use a larger electrode radiator with lower thermal resistance. *(Russian Microelectronics,* December 2025; https://doi.org/10.1134/S106373972570009X*)*

Flex Circuits

"Scalable Roll-to-Roll Approach for Encapsulating Long-Length Flexible Printed Circuit Boards"

Authors: Chan-Woo Lee, Eun-Ji Gwak, Doo-Sun Choi and Byoung-Youn Cho

Abstract: The encapsulation process in flexible printed circuit board (FPCB) manufacturing typically involves laminating a flexible copper-clad laminate (FCCL) with a coverlay film, using heat and pressure in methods such as hot press lamination. When they are applied to long-length FPCBs for electric vehicle applications, however, traditional hot press methods face challenges in scalability and productivity. To overcome these challenges, this study proposes a scalable roll-to-roll approach for encapsulating long-length FPCB. This approach enhances scalability to meet the requirement of long-lengthening continuously, but this can lead to incomplete filling in narrow circuit patterns due to insufficient flowability of the B-stage adhesive. To enhance flowability, a roll-to-roll system was developed that incorporates a rubber roll and a steel roll for the adhesive material. The effects of copper width dimensions and process parameters on encapsulation performance were investigated in the experimental analysis, based on rheological and thermomechanical characterizations of the B-stage adhesive. These results were quantified through image analysis and visualized using contour mapping to exhibit the influence of process parameters on the filling area. The reliability and durability of the developed approach were validated by analyzing adhesive properties and electrical performance. The developed roll-to-roll approach to the encapsulation process enables scalability while ensuring the durability and reliability of the long-length FPCB. *(ACS Applied Materials & Interfaces*, Aug. 21, 2025, vol. 17, no. 36; https://pubs.acs.org/doi/10.1021/acsami.5c09839*)*

Novel Substrates

"High-Density Papertronics via Laser-Written Hydrophilicity on Hydrophobic Parchment Paper"

Authors: Zahra Rafiee, Ruohan Zhang and Seokheun Choi

Abstract: High-resolution paper-based electronics are fundamentally limited by uncontrolled ink spreading within porous cellulose networks, which constrains device density and functional integration. Here, the authors introduce a laser-induced hydrophilic patterning strategy on commercially available hydrophobic parchment paper that

fundamentally redefines the resolution, scalability, and design freedom of papertronics. Local laser modification converts selected regions into ink-guiding, hydrophilic microchannels, enabling deterministic confinement of functional materials without the need for wax, masks, or high-temperature processing. This strategy supports few-hundred-micrometer-scale patterning, achieving a >200% reduction in device footprint relative to wax-based approaches and offering a clear route toward further miniaturization via optical refinement. Using this platform, the authors realize fully printed resistors, low-loss interconnects, interdigitated capacitors, and integrated low- and high-pass RC filters within a single paper layer, exhibiting predictable, tunable electrical behavior consistent with circuit theory. Importantly, the predominantly cellulose-based substrate preserves biodegradability and disposability, while optional elastomeric encapsulation confers environmental robustness without compromising performance. By unifying high-resolution patterning, functional integration, and environmental compatibility, this work establishes laser-patterned parchment paper as a scalable and sustainable electronics platform, bridging the gap between laboratory papertronics and deployable electronic systems. *(ACS Applied Materials & Interfaces*, vol. 18, no. 16; https://pubs.acs.org/doi/10.1021/acsami.6c03065*)*