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July 2026

Breaking the Frequency Barrier

Pushing Past the 100GHz Limit

Selective UHDI

Backdrill Done Right

Controlling Reflow Shift

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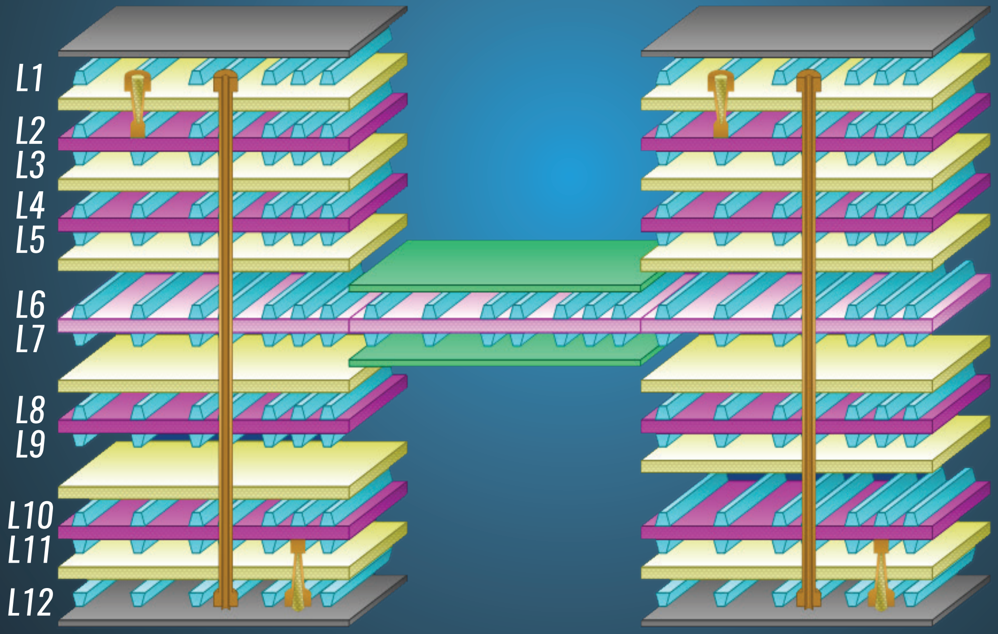
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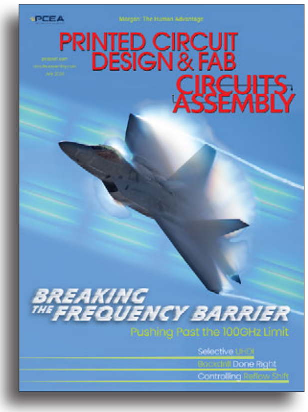

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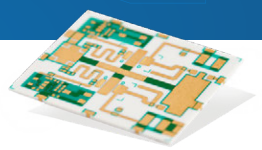

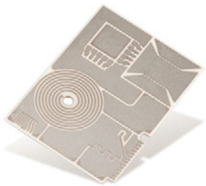

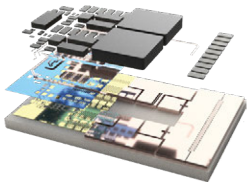

As the Chair Turns, One Last Time

TWENTY-SIX YEARS. That's how long I've sat in this chair as an editor for this publication. Long enough that a reader or two out there was born right about the time I took the job, in January 2000, first as editor in chief of *PC FAB*, to which my then-boss Pete Waddell soon added *Printed Circuit Design,* and then, in 2005, *CIRCUITS ASSEMBLY*. (Now I really feel old. Thanks a lot.)

I mention it not to be sentimental – though I'll ask your indulgence for a little of that – but because this is the last editorial I'll write from this vantage point. After more than a quarter century, I'm handing over the keys. More on that in a moment.

First, a confession. Across all those years and all those issues, I never missed one. Over 318 consecutive issues (which must be an industry record, however dubious), not a single deadline was skipped. I wrote editorials on three continents and over two oceans. I wrote one on my honeymoon. And I wrote one from a hospital recovery room the day my first son was born – because with little else to do, I'd started counting the circuit boards in the equipment around me. (I'm a nerd. I have the receipts.)

When I look back at what filled this space, certain subjects kept circling back, like an aircraft stuck in a holding pattern. The geography of our industry rearranged itself under our feet. We were proud to publish the annual NTI-100 ranking of the world's largest fabricators, and year after year the chart told the same uncomfortable story: the center of gravity moved east, and the number of North American and European names near the top dwindled to a precious few. I spent a lot of ink arguing that bigger isn't always better – and that in the rush to get big, we shouldn't forget the little guys, the job shops and prototype houses and quickturn specialists where this industry has always done some of its most inventive work.

I worried, too, about who comes next. I called it the juniority problem: an industry graying faster than it hires, institutional knowledge walking out the door at retirement parties, and not enough young engineers walking in to replace it. If I nagged you about mentoring, about writing down what's in your head before it leaves the building, about making room for the next generation, well, I'd do it all again.

I wrote more than my share about standards and certification, occasionally from the odd vantage point of someone who was actually in the room when the first designer certification program was drafted back in the 1990s. I believed then, and believe now, that a credential is only as good as the body of knowledge – and the practitioners – standing behind it.

And then there was the technology itself, forever promising to make us obsolete and never quite getting around to it.

When the AI-and-CAD evangelists insisted the machines were about to replace the designers, I tended to answer the way the genuinely smart people in the field do: no, and no. The tools change. The craft endures.

Running through all of it was one thread I kept tugging at: progress means change. I borrowed that line years ago and never gave it back. Our industry has changed almost beyond recognition since 2000, and yet the questions are stubbornly familiar — how to build it better, faster, closer to home, and with the people we'll need tomorrow.

The biggest change of all came in January 2022, when we sold the magazines, the trade shows, the newsletters and the rest to the Printed Circuit Engineering Association – an organization I now have the privilege of leading. Bringing these properties under PCEA's roof was, I'm convinced, the right home, and the work here will keep me plenty busy. So while I'm stepping out of the editor's chair, I'm not going far. You'll still find me at PCB West and PCB East, still working on training programs for designers and engineers, still meddling in the affairs of an industry I love.

Which brings me, at last, to the person taking over. Andy Shaughnessy is assuming the role of content architect for *PCD&F/CIRCUITS ASSEMBLY*, and I can think of no one better to steward these pages. Andy has spent decades covering this industry with the curiosity and the plain affection it deserves. He knows the people, he knows the technology, and – just as important – he knows the difference between a press release and a story. The publication is in very good hands.

As for me, I'll sign off the way I should: with gratitude. To Pete, who handed a young writer a chair and let him keep it. To the engineers, designers, fabricators and assemblers who answered my calls, returned my emails, argued with me, corrected me, and trusted me with their work. To the colleagues who caught my typos and my worst ideas. And to you, the reader, who let me onto your desk a dozen times a year for more than two decades. It has been the honor of my professional life.

While this column is named *The Route*, an homage to the newsletter I developed for Dieter Bergman and Gary Ferrari on behalf of the Designers Council more than 30 years ago, I named the predecessor *Caveat Lector*, meaning let the reader beware. You always did. And you kept me honest for it.

Thank you.

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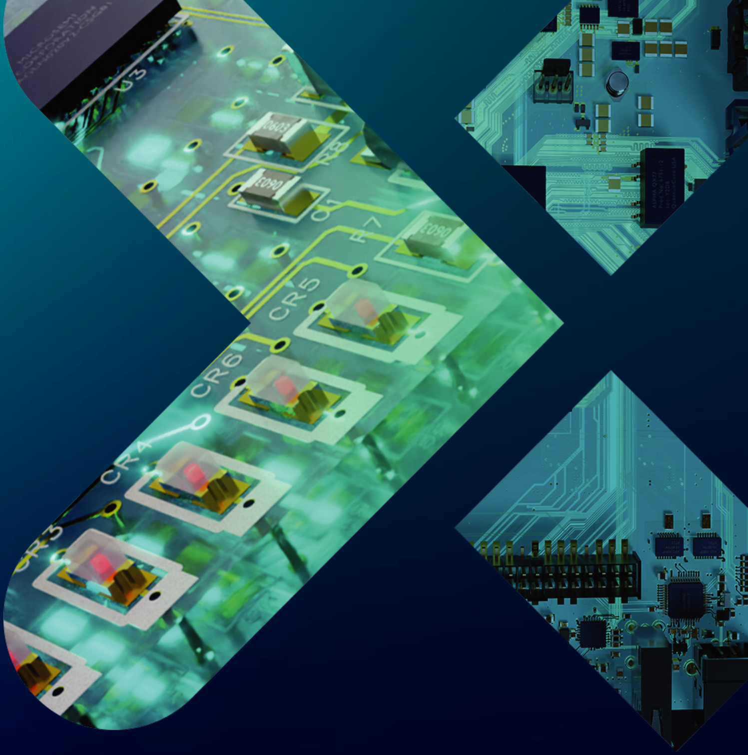
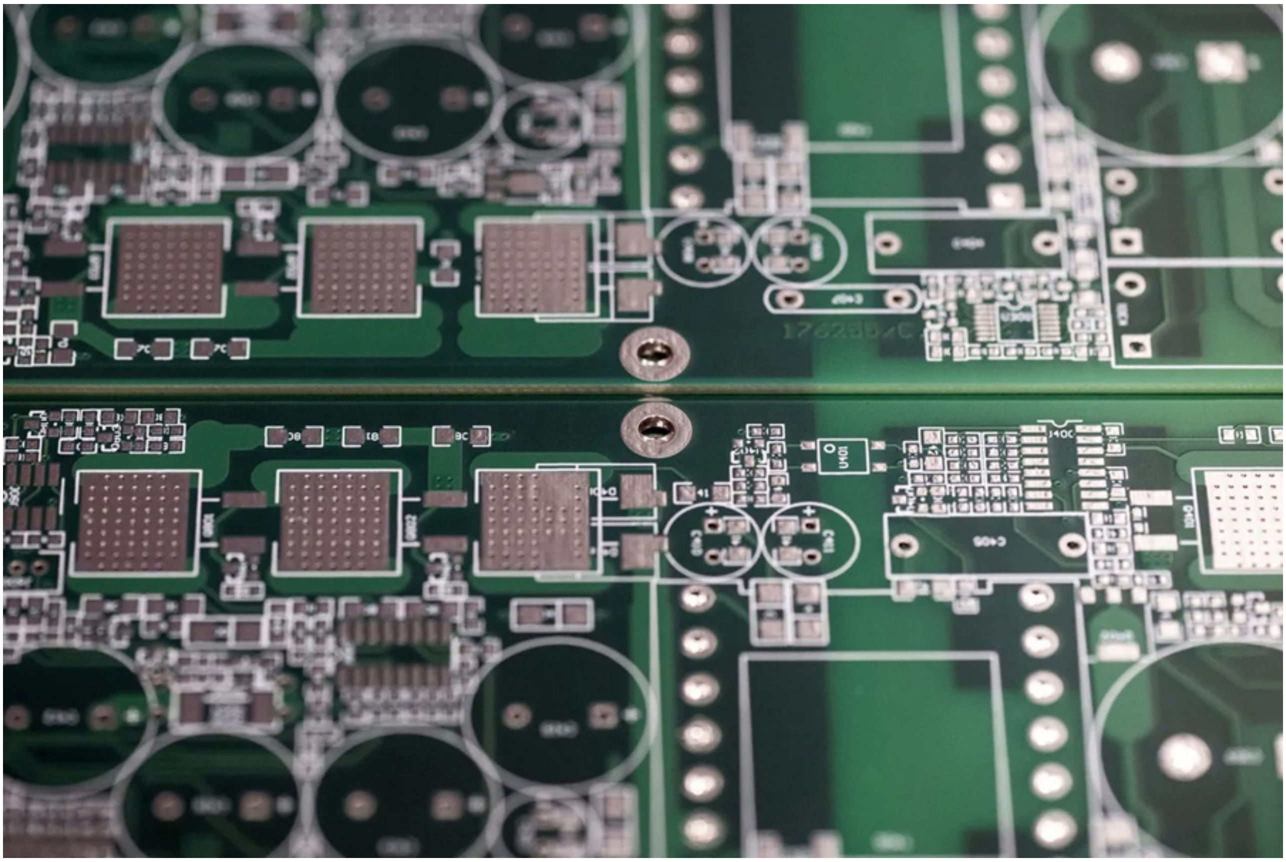


Principal Mineral Acquires Isola, Secures $280M for Expansion

DALLAS – Principal Mineral in June acquired PCB materials manufacturer Isola Group and secured approximately $280 million in new funding to support expansion, technology development and supply-chain investments. Financial terms of the deal were not disclosed.

The acquisition adds Isola's copper-clad laminate and dielectric prepreg portfolio to Principal Mineral's existing operations, which include Camden Copper, a producer of electrodeposited copper foil. Together, the businesses supply two key materials used in printed circuit board manufacturing, strengthening the company's position in advanced electronics supply chains.



Principal Mineral's acquisition of Isola combines copper foil, copper-clad laminate and prepreg manufacturing capabilities under a single supplier serving advanced PCB applications.

Principal Mineral said the funding will support integration of the combined company, expansion of manufacturing capacity and investments across North America, Europe and Asia. Following the transaction, the company will employ approximately 1,300 people across 10 facilities worldwide.

The company said the combination is intended to improve supply-chain resilience for industries including aerospace, communications, satellite systems, AI infrastructure and energy.

Kingboard to Expand PCB Capacity, Sells Stake in Laminate Unit

HONG KONG – Kingboard Holdings plans to raise approximately $1.5 billion through a stake sale in subsidiary Kingboard Laminates Holdings to expand production capacity and support growing demand for AI-related printed circuit board materials.

Kingboard Laminates, one of the world's largest producers of copper-clad laminates, will use the proceeds to increase multilayer and high-density interconnect (HDI) PCB capabilities, expand manufacturing capacity, accelerate research and development efforts, and repay debt.

The move comes as AI infrastructure investment continues to drive demand throughout the electronics supply chain. Major cloud providers are expected to spend more than $800 billion on AI infrastructure in 2026, increasing demand for advanced PCB materials and manufacturing technologies.

Kingboard said the investment will strengthen its position as a vertically integrated supplier of electronic materials and support future growth in AI, networking and data center applications.

AT&S Announces $1.7B IC Substrates Expansion

LEOBEN, AUSTRIA – Citing continued strong demand for AI infrastructure and advanced packaging technologies, AT&S in June announced plans to invest €1.5 billion to €2 billion ($1.7 billion to $2.27 billion) to expand production capacity for high-end IC substrates.

The plans are supported by key customers, including AMD and another undisclosed technology company, AT&S said. The agreements will support the installation of additional production capacity at the fabricator's existing plant in Kulim, Malaysia, and in a previously unused building of a second plant there.


The AT&S plant in Kulim.

The deals are fully supported and financed by long-term customer commitments, which remain subject to final negotiation and execution, AT&S added.

TTM Completes $130M New York UHDI Facility

DEWITT, NY – TTM Technologies has completed construction of a $130 million advanced manufacturing facility in DeWitt, NY, expanding domestic production of ultra-high-density interconnect (UHDI) printed circuit boards for defense applications.

The 215,000-sq.-ft. facility, known as Syracuse Diamond, is expected to create up to 400 engineering and manufacturing jobs and increase TTM's Central New York workforce to approximately 1,000 employees.

The project received $30 million in funding from the US Department of Defense and is intended to strengthen the domestic defense electronics supply chain. TTM said the facility will produce UHDI PCBs used in advanced military systems and support ongoing research and development efforts related to advanced packaging and substrate technologies.

Chase Acquires Sheldahl from Flex

WESTWOOD, MA – Chase Corp. in June completed its acquisition of Sheldahl from Flex, adding a portfolio of coated films, laminates and flexible circuit technologies used in aerospace, automotive, industrial and medical applications. Financial terms were not disclosed.

Sheldahl specializes in advanced materials and flexible circuitry, expanding Chase's capabilities in specialty manufacturing and strengthening its position in high-reliability markets. Financial terms of the transaction were not disclosed.

The acquisition aligns with Chase's focus on advanced materials and is expected to broaden its product offerings and market reach. Sheldahl's technologies support a range of applications requiring lightweight, flexible and durable electronic solutions.

Sheldahl is one of the oldest PCB fabricators in the world, having been founded in 1946.

Schmid Plans New China Manufacturing Campus to Expand Capacity

FREUDENSTADT, GERMANY – Schmid Group has signed a preliminary agreement with local authorities in Zhongshan, Guangdong Province, to establish a new manufacturing campus in China aimed at supporting future growth and increasing production capacity.

The planned facility will consolidate the company's manufacturing operations currently spread across two leased sites into a single company-owned campus. According to Schmid, the new site is expected to nearly double the effective manufacturing capacity of its existing China operations through expanded floor space, improved workflows and more efficient logistics.

The investment is part of Schmid's "In China for China" strategy and is intended to support growing demand for advanced wet-process equipment used in the production of high-density interconnect boards, IC substrates, AI server boards and other advanced electronic applications.

The project is expected to require approximately €11 million ($12.5 million) in investment for land acquisition, construction and infrastructure. Schmid anticipates securing most of the financing through local Chinese banks, with construction beginning following completion of land transfer, permitting and a final binding agreement.

The company expects the facility to begin operations in mid-2027.

Green Circuits Changes Hands, Adds Canadian EMS

SAN JOSE – Green Circuits, one of the largest quickturn prototype electronics manufacturers in North America, changed hands in May. Financial terms were not disclosed.

Reichmann Segal Capital Partners in June acquired the EMS company from Praesidian Capital, which in turn had provided the capital to support Evolve Capital's acquisition of Green Circuits in 2018. Reichmann Segal launched a fund, Metatron Private Equity, to acquire Green Circuits and

Green Circuits is joining forces with OES.

Reichmann Segal plans to group Green Circuits with OES Inc., which it acquired last year, London, ON-based OES was founded in 1981 and is a leader in LED video scoreboards, EMS and custom technology solutions.

Green Circuits chief executive Michael Hinshaw will remain with the company, which performs printed circuit board assembly and electronics manufacturing services for aerospace and defense, medical, industrial and other markets.

Polymatech Opens Singapore Hub for LED Packaging and Memory Module Assembly

SINGAPORE – Polymatech has opened an advanced electronics manufacturing facility in Singapore that will serve as its Asia-Pacific hub for LED chip-on-board (CoB) packaging and advanced memory module assembly.

Backed by an investment of approximately $25 million, the facility is located at Mapletree Hi-Tech Park and is designed to support optoelectronics, advanced packaging and computing applications. The site includes dispensing, packaging, curing, inspection, testing and module assembly systems for high-precision electronics manufacturing.

Polymatech's new Singapore manufacturing facility will serve as the company's Asia-Pacific hub for LED chip-on-board packaging and advanced memory module assembly.

The operation will focus on LED CoB packaging for UV, infrared and full-spectrum products used in horticulture, medical and industrial applications, as well as memory module assembly for high-performance computing, enterprise and embedded systems. Polymatech said the facility will strengthen supply-chain resilience and improve access to semiconductor markets across the Asia-Pacific region.

The Singapore site becomes part of Polymatech's global manufacturing network, which includes operations in France, India, Estonia and the United States.

Nano Dimension Nears End of Strategic Review, Teases Next Move

WALTHAM, MA – Nano Dimension said it is nearing a decision on its long-term strategic direction after completing major restructuring efforts, divesting businesses and reducing operating expenses as part of a three-phase plan aimed at maximizing shareholder value.

In a letter to shareholders, CEO David Stehlin said the company has made significant progress since launching a strategic review in September 2025. The review was designed to streamline operations, reduce cash burn, monetize product lines and identify the most compelling path forward for the business.

Nano reported that standalone operating expenses declined approximately 22% year-over-year in the first quarter, while operating cash burn has fallen each quarter since the third quarter of 2025. The company also completed the sale of its AME and Fabrica product lines and announced the $42.5 million all-cash sale of MarkForged to Stratasys.

According to Stehlin, the board and management team have narrowed their review to a small number of strategic alternatives focused on higher-growth opportunities.

Interflex Invests $18M to Expand Vietnam PCB Manufacturing

SEOUL – Interflex will invest approximately $18 million in its Vietnamese subsidiary, Korea Circuit Vina, as part of an ongoing effort to expand printed circuit board manufacturing capacity in Vietnam.

The investment will increase South Korea-based Interflex's ownership stake in Korea Circuit Vina from 83.5% to 89.3%. Located in Vinh Phuc province, the facility serves as a PCB manufacturing base supporting the Korea Circuit Group's regional production strategy.

Interflex's latest investment in Korea Circuit Vina will expand PCB manufacturing capacity in Vietnam.

Interflex, a major supplier of flexible printed circuit boards, operates manufacturing facilities in South Korea, China and Vietnam. The company said the latest investment is intended to strengthen overseas manufacturing operations and enhance competitiveness in global electronics markets.

Somacis Completes Acquisition of ACB Group

MILAN, ITALY – Somacis in late June completed its acquisition of France- and Belgium-based PCB manufacturer ACB Group, expanding its European manufacturing footprint and strengthening its position in the high-reliability printed circuit board market.

The transaction, first announced in February, includes ACB's production facilities at Atlantec in Malville, France; Cibel in Bellême, France; and ACB NV in Dendermonde, Belgium. Financial terms of the deal were not disclosed.

The acquisition expands Somacis' manufacturing, research and development, and customer support capabilities across Europe, complementing its existing operations in Italy, the United Kingdom and Switzerland. The company said the combined organization will be better positioned to serve customers requiring high-technology, high-reliability PCBs in demanding applications.

"It is an important milestone for Somacis," said Giovanni Tridenti, CEO of Somacis Group. "ACB's expertise complements that of Somacis and will enable us to broaden the range of solutions offered to customers worldwide."

NCAB Acquires Board Shark to Expand US PCB Presence

SUNDBYBERG, SWEDEN – NCAB has acquired 100% of Florida-based Board Shark, expanding its US printed circuit board presence through a deal valued at up to $26 million.

The acquisition includes an upfront purchase price of $15 million, with an additional earn-out of up to $11 million tied to Board Shark's financial performance over the next 24 months.

Founded in 2016 by Carl and Rachelle Moehring, Board Shark specializes in PCB solutions for customers in the aerospace, industrial and medical sectors, with a particular strength in quickturn deliveries. The company employs five people and maintains a network of regional sales representatives, giving it a strong presence in the western United States.

NCAB said the acquisition is expected to contribute positively to earnings in 2026, with anticipated synergies in supplier relationships, logistics, payment terms and cross-selling opportunities, including prototyping services.

"Board Shark's development over the past few years has been impressive," said Peter Kruk, CEO of NCAB Group. "Its business model is closely aligned with that of NCAB, and Board Shark holds a solid market position on the US West Coast with promising opportunities for further growth."

PCD&F

Meiko Group broke ground on a $500 million PCB manufacturing facility in Vietnam.

Nano Dimension has entered a nonbinding term sheet for a proposed merger with **Infinite Epigenetics**, an AI-powered preventive health and diagnostics company.

Saturn Electronics installed an **Excellon** Cobra Hybrid laser drill.

Samsung Electronics America plans to relocate its US headquarters from New Jersey to Plano, TX, by the end of the year, affecting approximately 1,000 employees.

Schmid Group reported more than $30 million in new orders from customers in China, Taiwan, South Korea and Europe since mid-May, driven by demand for advanced PCB and substrate manufacturing equipment used in AI infrastructure, high-speed networking and optical communication applications.

CA

Automated Production Equipment expanded manufacturing capacity for PCB eyelets and funnellets.

Benchmark Electronics has expanded its manufacturing partnership with **Ouster** to produce lidar sensors.

CE3S partnered with **SpecialTeam** to expand support for cleanroom and medical device manufacturers.

Celestica appears to be planning a new hub in Austin, including office space and an R&D lab focused on data server components.

Esprit Electronics purchased two **Koh Young** Zenith 2 AOI platforms.

Federal Electronics added an environmental test chamber with a temperature range of -70° to +200°C.

Finnish defense group **FORCIT** is building an electronics assembly plant in Salo, Finland.

Gigavis secured a nearly $7 million order from a major Japanese semiconductor substrate manufacturer for AOI, AOR and VRS inspection systems.

Incap's electronics manufacturing facility in Pennsylvania temporarily suspended operations in June following a power outage caused by severe storms in the region.

Inter-Company installed a **Yamaha** SMT production line.

Jabil will establish a manufacturing facility in Virginia for **Siemens**, and is expected to create 352 jobs in the region.

Matric Group installed a **Panasonic** NPM-GH placement platform.

Metal Etch Services opened a Detroit facility to expand stencil manufacturing capacity.

Niche Electronics completed a 20,000 sq. ft. expansion of its Sarasota facility, adding production capacity and new AOI and laser-marking equipment.

The US Pentagon added **Alibaba, BYD, Baidu, Nio, Unitree** and more than a dozen other Chinese firms to its list of companies with alleged military ties.

Regal Technology Partners installed a **Hanwha** SM481 Plus, **Hanwha** SM485 Plus and a 10-zone reflow oven.

Seho Systems named **Altus Group** distributor.

Smartsol Technologies Mexico will exclusively distribute **Creative Electron**'s x-ray systems in Mexico.

Sumitomo Electric Industries is planning a $74 million expansion in Laguna, Philippines, to add flexible printed circuit and SMT assembly manufacturing capacity.

Syrma SGS and **Kaga Electronics** have signed a pact to form a joint venture that will focus on production for Japanese clients.

Volex will close its **Servatron** PCB assembly facility in Spokane Valley, WA, by the end of 2026, eliminating 124 jobs and consolidating US manufacturing operations at its site in Irvine, CA.

Walton shipped its first export order of PCB assemblies to the United States, where the products will be used in security systems.

Wiwynn selected **Test Research, Inc.** as inspection equipment partner for advanced server board manufacturing.

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NCAB GROUP

25
Newgrange Design
Celebrating 25 years

PCDF


Jon Johnson


David Ierardi


David Guerin


Claude Jodoin

Dyconex named **Jon Johnson** director of sales, North America.

Lavelle Medical named **David Ierardi** VP of operations.

K2 Space Corp. named **David Geurin** principal PCB design engineer.

Vertiv named **Claude Jodoin** senior engineer core electronics.

CA


Marcus Pee Nai Quan


Jonathan Wol


Adam Szychowski


Adam Ryder


Doug Kay


Nik Thomas


Kevin Morrisette


Jim Kircher

AIM Solder appointed **Marcus Pee Nai Quan** sales engineer for Southeast Asia.

Fuji America appointed **Jonathan Wol** senior director of sales and applications.

Green Circuits promoted **Adam Szychowski** to chief revenue officer.

Incap appointed **Adam Ryder** managing director of its UK electronics manufacturing operation, **Murthy Munipalli** president of Asia Pacific and **Ralf Hasler** president of Europe.

MicroCare named **Doug Kay** director of market and new business development.

Microscreen promoted **Nik Thomas** to director.

Pica Manufacturing Solutions named **Kevin Morrisette** general manager of electronics assembly.

SigmaTron appointed former Norwood Medical CEO **Jim Kircher** chief executive officer.

Technica USA appointed **Will Gutierrez** business development/account manager for its West South-Central territory.

ZTest Electronics announced **Steve Smith** has resigned as president and chief executive. Day-to-day operations will continue under **Suren Jeyanayagam**, president of Permatech Electronics.

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- **Al Block** *DfM and the Art of Qualifying Board Shops*
  PCB Manufacturing Strategist, Direct PCB
- **Levin Liu** *Levin's First Trip to the U.S.*
  Engineering Sales Engineer, Direct PCB
- **Jim Rathburn** *UHDI Fabrication Today and Tomorrow*
  Founder and President, Precision Circuit Technologies

PCEA®
PRINTED CIRCUIT ENGINEERING ASSOCIATION

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PCB West Keynote: The Physical AI Boom Starts at the Circuit Level

PEACHTREE CITY, GA – The Printed Circuit Engineering Association (PCEA) announced that AJ Cooper, CEO and cofounder of Itera, will keynote PCB West 2026.

His keynote, "The Physical AI Boom Starts at the Circuit Level," takes place Sept. 30 from 11 a.m. to 12 p.m. at the Santa Clara (CA) Convention Center.

Itera, a new deep tech startup, has developed the world's first "fluid" circuit board, which can rewire itself in real time. Built upon an electrowetting platform, the system replaces copper traces with reconfigurable liquid metal interconnects embedded in glass. When the design is updated digitally, the system reroutes the liquid metal traces to match the new design. The company says that this technology can make hardware iteration 1,000 times faster than the traditional PCB design process.


AJ Cooper

In his keynote, Cooper will discuss fluid PCB technology, its potential for accelerating development of AI infrastructure, and why he believes that hardware updates will eventually be as simple as a software update – triggered with the push of a button.

Cooper served as director of hardware engineering for Lyft and head of electrical engineering for Uber, as well as a director of engineering at Flex. He holds a Ph.D. and an M.S.E.E., both from the University of Virginia.

"AJ Cooper has a deep understanding of the fabrication and assembly issues designers face in trying to realize their novel ideas," said Mike Buetow, president, PCEA. "Itera has developed a unique process for overcoming the up-to-now inherent obstacle that affects every designer and design engineer: in getting a printed circuit board design from a drawing board to a working prototype."

PCB West will be held Sept. 29 – Oct. 2 at the Santa Clara Convention Center in Santa Clara, CA. The event includes a one-day exhibition on Sept. 30.

PCB West Assembly Program to Focus on Paste, Process Developments

PEACHTREE CITY, GA – PCB West this fall will feature a dedicated program of electronics assembly tracks, including nine sessions led by leading practitioners in solder paste, placement, reflow, stencil design and cleaning. The assembly program runs Sept. 29 and Sept. 30 at the Santa Clara (CA) Convention Center.

Spanning introductory through advanced material, the tracks give assemblers, process engineers and manufacturing professionals practical, noncommercial training on the core processes that determine circuit assembly yield and reliability. Registration is open at pcbwest.com.

The sessions kick off on Sept. 29 with A Data-Driven Solder Paste Qualification Process, a 3.5-hour workshop from Chrys Shea of Shea Engineering. There are numerous avenues by which assemblers can enhance reliability, reduce costs and increase the yields of their products through the qualification of a new solder paste. The problem they face is how to do it. Solder pastes have many properties to consider and test for, and there are many pastes to choose from. It can appear to be a daunting task, and a potentially risky one if something gets overlooked in the process. The solder paste selection scorecard simplifies the process.

On Sept. 30, the morning sessions cover an introduction to circuit assembly processes. Scheduled talks include:

- The SMT Printing Process – Chrys Shea, Shea Engineering
- Introduction to Placement – Daniel Stanphill, Aurora Boardworks
- The Basic Components of Solder Paste – Anna Lifton, MacDermid Alpha
- The Basics of Cleaning – Doug Pauls, ItDepends

In the afternoon, the presentations go more in-depth, looking at advanced circuit assembly processes:

- Advanced Solder Pastes – Type 5 and Beyond – Anna Lifton, MacDermid Alpha
- Stencil Design / Cutting – Elias Malfavon, Metal Etch
- Driving Forces for Advanced Placement – Daniel Stanphill, Aurora Boardworks
- Advanced Reflow Technology: Formic Acid Soldering – Ryan Mayberry, Indium Corporation
- Cleanliness Measurement and Conformal Coatings – Doug Pauls, ItDepends

"Electronics assembly is where a great design either comes to life or comes apart," said Mike Buetow, conference director, PCB West. "This year's assembly tracks bring together some of the most respected process experts in the industry to walk attendees through printing, placement, reflow and cleaning – from the fundamentals all the way to the most advanced techniques."

PCEA Board Voting Begins this Month

PEACHTREE CITY, GA – Voting for nominees for the PCEA board of directors for the 2027-28 term will be circulated among PCEA individual members this month.

In accordance with PCEA bylaws, any PCEA member in good standing is eligible to be nominated for the board of directors. Board members are nominated by a nominating task group and voted on by the general membership, with ballots circulated a minimum of 60 days prior to the annual meeting.

The annual meeting takes place Sept. 29, 2026, at PCB West.

PCEA **CURRENT EVENTS**

ASSOCIATION NEWS

PCB West 2026 features over 50 classes and more than 120 hours of in-depth electronics engineering training on circuit board design and assembly. Rick Hartley, Karen Burnham, Susy Webb, Stephen Chavez, and Tomas Chester are among the headliners of this year's conference. Those who sign up by Aug. 21 can take advantage of the early bird special discounts for the conference.

Printed Circuit University in June added a new webinar on flex design and manufacturing. I Access to much of the content is free to individual members, while some extended tutorials are available via subscription.

Certification. The following recently passed the PCEA Certified Printed Circuit Designer exam:

- Troy Allman
- Albert Yang
- Alexander Yang

New Corporate Members.

- Jove PCB
- Parmi

Networking. The PCEA Discord server brings together engineers and designers from around the world on a private channel to discuss technical questions and career opportunities. To join, contact PCEA. Recent conversations covered specifying laminates, pin delays and stacking microvias.

CHAPTER NEWS

National. Upcoming PCEA Training Certified Professional Circuit Designer (CPCD) training and certification classes will be held:

- Sept. 4, 11, 18, 25, Oct. 9
- Sept. 28 – Oct. 2 (live abridged class, taught in-person in conjunction with PCB West)
- Oct. 16, 23, 30, Nov. 6, 13

Richmond, VA. The Richmond PCEA chapter on Jul. 1 is holding a PCB open discussion session. Drop in any time between 5 and 8 p.m. to discuss PCB design, schematics, layout, component libraries, manufacturing outputs, design challenges or ECAD workflows. Bring a project you're working on, a question you've been stuck on, or just stop by to meet other engineers and designers in the area. We will have a laptop with KiCad and Altium installed, and attendees are welcome to bring other tools and projects to share. Whether you're an experienced designer, a student, a hobbyist, or simply curious about PCB design, you're welcome to come by.

No presentation, agenda, or commitment required – come for fifteen minutes or stay the whole evening. The location is Libbie Mill – Henrico County Public Library, 2100 Libbie Lake East St, Richmond.

Portland, OR. The next meeting is tentatively scheduled for July 23, from 12 – 1 p.m. Pacific. Speaker and meeting link to be announced.

AI Computing Power Demand Drives Upstream PCB Material Prices Wildly, Entering a 'Super Cycle'

TAIPEI – Demand for upstream PCB materials is accelerating as AI servers push PCB layer counts and performance requirements to unprecedented levels, driving a sharp increase in the value of the materials used to build them.

According to industry data, successive generations of Nvidia's computing platforms have dramatically raised the value of PCBs used in standalone AI racks. The H100 platform introduced in 2022 utilized roughly 16 to 20 layers, with PCB content valued at about $5,000 per rack. By the time the GB300 platform arrives in 2025, layer counts are expected to exceed 26 and PCB value per rack is projected to reach $35,000.

The next inflection point could come with Nvidia's Rubin architecture, scheduled for volume production in the second half of this year. PCB stackups are expected to jump to between 32 and 40 layers, lifting PCB value per rack to approximately $116,000 – a 233% increase over the GB300 generation. By 2027, the Ultra architecture could require as many as 78 layers.

The increase in complexity is reverberating throughout the materials supply chain. The copper-clad laminate market, the foundation of PCB manufacturing, is forecast to grow to $18.7 billion in 2027 from $1.5 billion in 2024, representing a 12.5-fold increase.

Kingboard Laminate, the world's largest laminate producer, implemented eight rounds of price increases between February 2025 and May 2026, resulting in cumulative hikes of 25% to 30%.

Premium materials are commanding substantial margins. Processing fees for high-end HVLP-4 copper foil have surpassed NT$20,000 per ton, more than 10 times the level of conventional HTE copper foil. Goldman Sachs estimates the supply gap for HVLP-3+ copper foil capacity could approach 38% between 2027 and 2028.

Electronic fiberglass cloth is experiencing similar pressures. Quartz fiber cloth suitable for Rubin-based systems sells for more than NT$200 ($6.30) per meter, compared with NT$4 to NT$6 per meter for conventional electronic fabric. Industry projections indicate the supply-demand imbalance could exceed 60% by 2027.

Geopolitical instability in the Middle East has further strained the market. Approximately 70% of global PPE resin capacity was disrupted, sending prices from 120,000 yuan ($17,700) per ton to 600,000 yuan ($88,560). The resulting shortages caused some PCB prices to rise by as much as 40% in a single month in April.

Meanwhile, efforts to expand high-end PCB production remain constrained by equipment availability. Lead times for critical tools such as laser drills are now extending into 2027.

Margin Call

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	FEB.	MAR.[r]	APR.[p]	YTD
Computers and electronics products	1.0	0.6	0.5	6.7
Computers	2.0	-0.2	0.4	18.1
Storage devices	7.7	2.6	3.1	13.0
Other peripheral equipment	10.4	-1.7	7.8	50.1
Nondefense communications equipment	1.4	3.5	0.9	23.5
Defense communications equipment	-6.0	-3.2	4.7	0.0
A/V equipment	-0.7	-0.7	-1.0	-9.0
Components[1]	-0.2	-0.4	0.2	4.6
Nondefense search and navigation equipment	1.8	1.2	3.0	5.6
Defense search and navigation equipment	2.7	2.5	0.1	13.3
Electromedical, measurement and control	-0.3	-0.1	0.3	0.2

[r] Revised. [p] Preliminary. [1] Includes semiconductors. Seasonally adjusted.

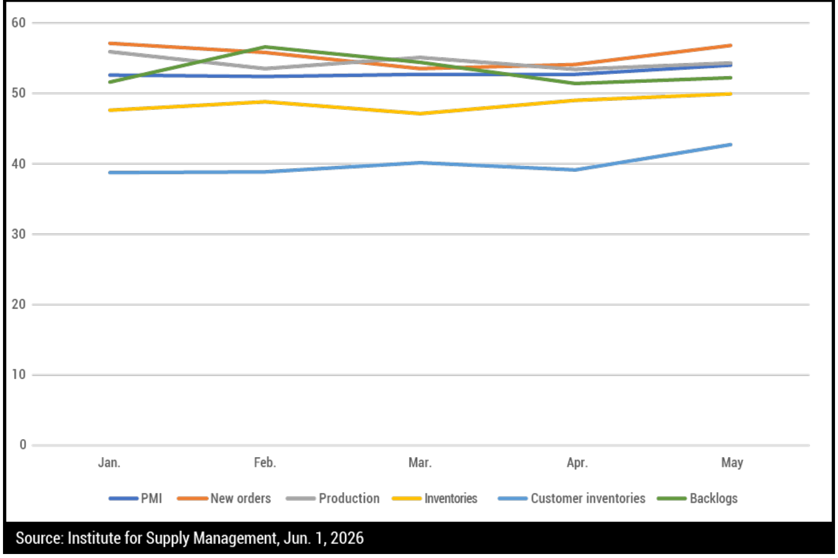
Source: US Department of Commerce Census Bureau, Jun. 1, 2026

Key Components

	JAN.	FEB.	MAR.	APR.	MAY
Semiconductors[1,3]	46.1%	61.8%	79.2%	79.0%	TBA
PCBs[2,3]	1.09	1.08	1.08	1.24	TBA
EMS[2,3]	1.25	1.32	1.29	1.36	TBA
Electronics mfg. orders[2]	113.0	122.0	120.0	118.0	TBA
Electronics shipments[2]	110.0	117.0	117.0	115.0	TBA
Component sales sentiment[4]	138.0%	139.7%	149.2%	146.6%	146.6%

Sources: [1] SIA, [2] GEA, [3] 3-month moving average, [4] ECIA

US Manufacturing Indices



Source: Institute for Supply Management, Jun. 1, 2026

Hot Takes

A bipartisan Senate bill would extend the **Chips Act manufacturing tax credits** to future semiconductor fabrication facilities in space, aiming to support US competitiveness in emerging microgravity chip production technologies. (Washington Times)

The **global copper-clad laminate** market is expected to exceed $21.5 billion in 2026, driven by AI demand, with annual growth projected to reach 34%. (Taiwan Printed Circuit Association and Industry, Science and Technology International Strategy Center)

Taiwan's printed circuit board fabricators are expected to see domestic and overseas output rise 15% year-over-year to NT$1.05 trillion (US$3 billion) in 2026. (TPCA)

A Cambodian government study identified **semiconductors as a future strategic industry,** highlighting Thailand's experience as evidence that building a PCB manufacturing base is an important first step. (Khmer Times)

The European Commission unveiled **Chips Act 2.0,** a revised semiconductor strategy focused on accelerating innovation, expanding manufacturing incentives, streamlining permitting and strengthening Europe's semiconductor supply chain competitiveness. (SEMI)

Surging memory prices forced Chinese smartphone makers to reduce shipments of mid- to low-end models and raise product prices in the first quarter of 2026, causing **global smartphone shipments** for the quarter to fall 5.6% year-over-year to 278 million units. (TrendForce)

First quarter revenue among vendors of external OEM **enterprise storage systems** in 2026 was $9.2 billion, up 23% from a year ago. (IDC)

Taiwan's major server manufacturers reported strong May revenue growth as continued investment in AI infrastructure fueled demand for data center hardware. (DigiTimes)

PCB manufacturers in India are seeking price increases of up to 50% and tariff relief on imported components as supply chain disruptions linked to the Iran conflict drive up material costs and extend lead times. (Economic Times)

The **worldwide server market** reached $122.6 billion in vendor revenue in the first quarter, up 30% year-over-year. (IDC)

Notebook OEMs reported shipments fell 33% sequentially in April due to weakened channel stocking momentum and a high base period. (DigiTimes)

Glass-core substrates are projected to grow 67% compounded annually from 2028 to 2040. (SEMI and Global Net)

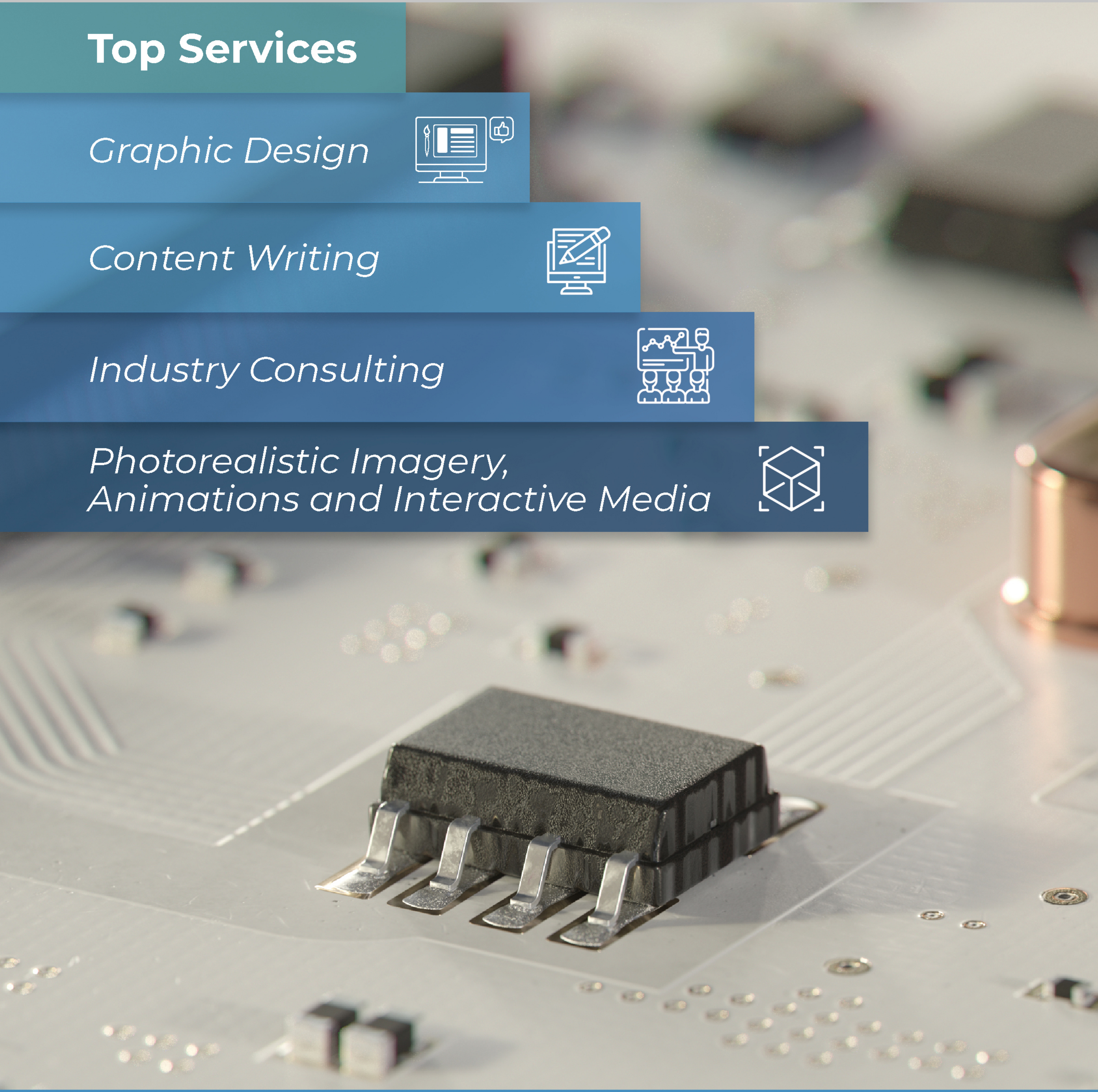
Global **semiconductor equipment billings** rose 14% year-over-year to a record $36 billion in the first quarter, driven by AI-related manufacturing investments. (SEMI)

US defense officials and industry advocates warned that **reliance on Chinese-made PCBs poses supply chain and security risks** as AI demand grows, backing legislation that would provide a 25% tax credit for domestic PCB purchases and $3 billion for US manufacturing. (CNBC)

Notebook OEM shipments fell 33% sequentially in April due to weakened channel stocking momentum and a high base period. (DigiTimes)

Electrical and electronic products are now leading **Bangladesh's engineering exports** sector as manufacturers expand into higher-value goods, including PCBs and PCB assemblies. (The Business Standard)

DDR2 contract prices will rise by approximately 55-60% in the second quarter, followed by a further 35-40% increase in the third quarter. (TrendForce)



Why Humanoid Robots Aren’t Ready for the Factory Floor

> Despite rapid advances in artificial intelligence, humanoid robots still face major hurdles in mobility, communication and energy efficiency.

WITH ALL THE attention, headlines, discussion, expectations, hopes, fears and, yes, hype surrounding artificial intelligence (AI), there is one area that appears far from ready for prime time: humanoid robotics.

Some may argue that robotics is not really AI at all. That perspective comes from traditional automation, which has been used for decades to load and unload equipment, stock inventory in warehouses or move parts along assembly lines. These systems relied on straightforward programming tailored to specific tasks. In the 1990s, many printed circuit board companies had fleets of loaders and unloaders. More recently, warehouse automation was expected to revolutionize logistics. In both cases, productivity improved significantly, and the automation introduced was indeed transformative.

Today, however, both the technology and the expectations have changed.

Traditional automation has advanced dramatically. Improved sensors can now detect pressure, temperature, weight and location with a level of accuracy that would have been difficult to imagine just a decade ago. Yet even with these advances, most factory automation remains tied to a specific machine or location and relies on fixed power sources or charging stations.

At the same time, humanoid robotics has made impressive progress. For many people, the benchmark remains C-3PO from *Star Wars* – a robot that could walk, talk, reason and even display something resembling human emotions. Nearly 50 years after that character first appeared on screen, it still shapes expectations of what a humanoid robot should be.

The challenge is that functioning like a human being is extraordinarily difficult.

One way to understand the problem is to look at how humans develop. A baby begins by learning to see and hear. Next comes basic body control: clapping, crawling, standing and eventually walking. Communication follows, along with the ability to process and learn from the constant stream of information coming from the surrounding environment. Over time, humans learn to understand situations, interpret context and respond appropriately. Finally, they become capable of functioning productively for hours at a time without needing a nap.

AI development has followed almost the opposite path. Machines first gained the ability to store and process information. Communication capabilities came next. Physical movement and body control have proven to be among the last and most difficult challenges. In many ways, AI-driven humanoid robotics is developing in reverse order from human development.

That is where the real difficulty lies.

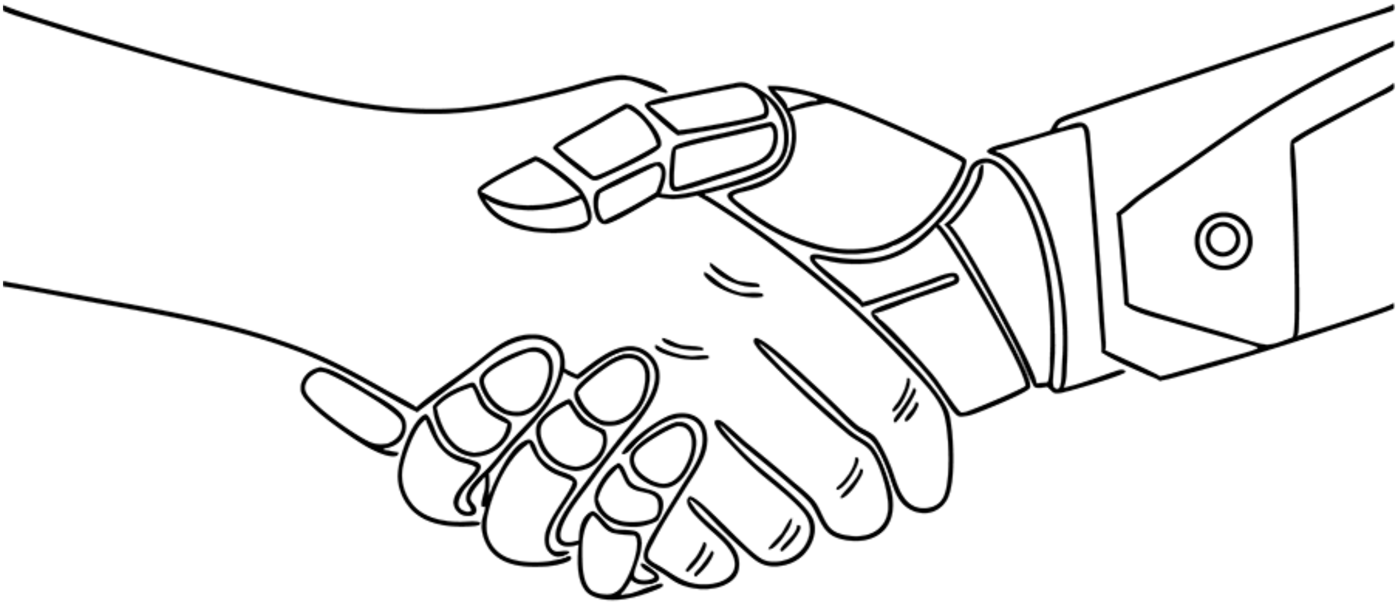


Figure 1. Humanoid robots continue to improve in mobility and interaction, but significant challenges remain in movement, communication and energy efficiency.

For machines, movement remains one of the biggest obstacles. A robot may be able to run faster than a human being, but often that is because running is the only task it was specifically designed to perform. Human movement, by comparison, involves balance, dexterity, adaptability and the ability to perform countless motions under changing conditions. Replicating that flexibility is a far greater challenge.

Communication presents another hurdle. AI systems can exchange information with other machines quite effectively. Communicating naturally with people is another matter. Humanoid robots can increasingly handle factual exchanges, but they still struggle with the nuances of human interaction. People respond not only to words but also to tone, context and emotion. That level of communication remains a work in progress.

The greatest challenge, however, may be energy.

Human beings are remarkably efficient. With three meals a day, a person can typically work eight to 12 hours and, when necessary, much longer. Humanoid robots operate under very different constraints. They require significant power, and the more functions they perform, the farther they travel and the more complex their calculations become, the greater their energy demands.

Military leaders have long understood that an army is only as effective as its supply lines. The same principle applies to humanoid robotics. Their effectiveness is limited by how much energy they can carry and how long that energy lasts. Battery technology, more than software, may ultimately be the factor that determines how quickly humanoid robots become practical.

For workers on the factory floor who move materials, install equipment or perform tasks requiring mobility and adaptability, there is little reason to fear replacement by humanoid robots anytime soon. The limitations of movement, communication and energy consumption continue to outweigh the advantages these systems can currently provide.

Given the challenges involved, along with the costs of developing mechanical solutions compared with software-based ones, humanoid robotics appears likely to remain a work in progress for many years to come.

PETER BIGELOW has more than 30 years' experience as a PCB executive, most recently as president of FTG Circuits Haverhill; peterbigelow@msn.com.

The Most Dangerous Word in EMS: Pretending

Successful EMS companies understand their strengths, acknowledge their limitations and avoid making promises their operations cannot support.

IN THE ELECTRONICS manufacturing services (EMS) world, it is critical for companies to understand who they are and what they stand for, rather than adopting aspirational marketing taglines that make them appear indistinguishable from everyone else in the industry. Without that level of self-awareness, mistakes can occur when pursuing new business or serving existing customers.

Time for some honesty. Occasionally, nothing is more satisfying than a tall glass of cold milk and a homemade cookie. The comfort of a great piece of meatloaf with a side of mac-and-cheese, or a slice of pizza paired with a robust glass of cabernet, can be hard to beat. While none of these choices may qualify as health food, acknowledging the enjoyment they provide makes it easier to appreciate them without regret the next day.

The same principle applies to business. EMS companies benefit from recognizing and accepting the realities of their operations.

Pursuing business that does not fit the company's model, making promises that cannot be delivered after an account is won, placing excessive stress on operations that are already operating at their limits, or damaging a hard-earned reputation among OEM customers are just some of the consequences that can result from trying to be something the organization is not.

Many industry myths have persisted since my career in electronics manufacturing began in 1979, and several remain surprisingly common today. While not every EMS company makes claims that stretch reality, and certainly not every organization suffers from delusions of grandeur, some marketing messages continue to reflect aspirations more than facts.

Every EMS company benefits from periodically comparing its claims against operational reality and making the adjustments necessary to ensure its business model accurately reflects its true capabilities. Here are some examples I have encountered over the years.

Myth: Claims are made that "we want to grow our business."

Fact: There is little to no investment in sales to growing existing customers or obtaining new ones, no expanding of the services offered, no M&A plans, and no evidence in marketing activity to increase brand awareness.

Myth: Taglines such as "we manufacture the world's leading technologies."

Fact: The reality is most EMS companies build medium technology at best and lack the manufacturing capital equipment, experience or process controls to support bleeding-edge technology, nor do they possess the needed inspection or test systems capable of validating the builds.

Myth: "We measure everything."

Fact: Making that claim indicates that nothing is important. Correct KPIs are critical to managing a complex business. This claim means you are just data-collecting and unable to make effective decisions on a daily, weekly or monthly basis.

Myth: "Quality is job #1."

Fact: There is no evidence of a BoM scrub, capability for DfM/DfT, lacking critical quality certs, lower than usual yields, bone piles of offline WIP are stacking up, the MRB cage is full of outdated material, or there are unacceptable scrap and RMA percentages. I have even seen end-of-month forced billings (shipments) with known nonconforming products approved to "make a number."

Myth: "We manage risk well."

Fact: No evidence exists of standard terms and conditions on every quote and online, vendor terms and conditions are missing, excess-obsolete-slow moving inventory coverage is nonexistent, A/R is high, turns are low, and all OEM contracts are just signed as-is.

Myth: "We have SMT setup time down to only a very few minutes."

Fact: While dialing out old jobs and dialing in the next job that has been offline validated, this can't include the first piece run through, allowing the next production run to proceed. Is it more important to advertise an unrealistic changeover time or have a measurement of the actual time it takes to dial out the old job, setup and validate the new run and conduct a first piece validation run indicating production readiness?

Myth: "We can build whatever our customer needs."

Fact: You have never performed an honest SWOT analysis on your entire business and do not know what you are capable of, what you excel in and what you don't do very well. BTW, no EMS can be everything to every customer.

Myth: "We offer engineering design services."

Fact: Most EMS companies do not have actual design services in-house and at best only offer design for supply chain (DFSC), design for manufacturing (DfM), and design for test (DfT, which is just a point-to-point capture).

Myth: "We manage our customers' BoMs better than our customers are able."

Fact: The best management of material is a strong partnership with your customer, where input and details are traded back and forth to overcome the inventory issues we see daily. A collaborative effort for BoM expansion, BoM early-warning details (NCNR, NRND, obsolete, sole-sourced) and notices of changes in part-number status as the

BoM ages should be offered. As many material teams are bogged down in the tactical execution of day-to-day issues, leaving no time to act strategically, a hard look at your investment in this function may be needed.

Myth: “Our board of directors is engaged and supports us.”

Fact: The board has little to no factual knowledge of the company’s day-to-day operations and isn’t investing in the EMS’s growth needs. The quarterly data dump rarely provides the board with the knowledge they need to make decisions that can move good EMS companies toward greatness.

Myth: “We know who our best customers are.”

Fact: Many EMS companies have never done an analysis of each customer, by part number, to assess the actual profitability of that customer and rely on revenue size and a gut feeling to guess who the best customers are. In almost every case, I drove this process; EMS companies were shocked to find those they thought were their best customers weren’t.

Myth: “Our people are our greatest asset.”

Fact: Performance reviews and guidance are only given once a year, small percentage raises are doled out evenly as no KPIs are considered, and mediocrity is rewarded the same as excellence, morale is bad, there is little intracompany communications, and successes are not celebrated with the entire company. How does your employee base know if they had a good week or a bad week?

Myth: “We invest consistently and proactively to keep up with technology changes seen in our dynamic industry.”

Fact: Many EMS companies have lumpy and inconsistent year-over-year capital equipment expenditures, usually investing when one piece of equipment ceases to be functional and quality, OTD, and customer satisfaction are impacted. Even with strong preventive maintenance measures in place, machines wear out.

EMS is a complex business, and it is easy for smoldering issues to go unnoticed amid the daily demands placed on leadership teams. When operational challenges consume most of the workday, finding the time and objectivity needed for honest self-assessment can be difficult. That is why many organizations benefit from engaging an unbiased, experienced third party to conduct a comprehensive SWOT analysis. Such an assessment can identify what is working well, what should be discontinued and what opportunities may be overlooked.

Ignoring reality rarely improves performance. Confronting it often becomes the first step toward meaningful progress.

JAKE KULP is founder of JHK Technical Solutions; jkulp@cox.net. He assists OEMs and EMS companies with optimizing demand creation offerings and deciding when and where to outsource manufacturing. He previously spent nearly 40 years in executive roles in sales and business development at MC Assembly, Suntron, FlexTek, EMS, and AMP Inc.


VOLUME
TUNING

Beating the NRE Game: Changing Designs Without Paying Tooling

Knowing which PCB specification changes require new tooling and which do not can help designers and buyers reduce nonrecurring engineering costs while avoiding unnecessary delays.

NRE (NONRECURRING ENGINEERING) is a one-time fee charged by the fabricator for each revision of a design for a particular printed circuit board.

This fee covers the CAM engineering time, checking for design errors and providing a report for those items that need to be addressed. It also includes designing a sub-array panel that will work well for the assembler, generating photographic films or programming the LDI (laser direct imaging) machines, writing CNC drill and optimized routing programs and providing stackup details and material specifications.

There is often a separate fee for electrical test, test connectivity (including top-side pad connections to bottom-side pads), and programming the flying probe tester, or creating the electrical test (e-test) fixture, often dependent on quantity to be built.

Buyers often ask me: "We need to make a change to this PCB design. Are we going to get hit with another NRE charge?"

The answer depends on what changed and how well the changes are documented. To the PCB fabricator, reusing existing tooling from a previous vendor's NRE is somewhat limited. The "design" is the physical layout dictated by the details of the fabrication drawing, including stackup and impedance requirements, referenced specifications, electronic CAD files and NC drill files.

The golden rule of NRE and electrical test is this: If the changes impact connectivity and require the CAM engineer to generate new films, a new drill tape, a new routing path and a new e-test program, both the NRE charge and electrical test charges apply.

If the design engineer moves a single via or changes the board's outline/stackup, that is a hard design change. The fabricator, if not using LDI, may have to discard the old phototooling and start from scratch, so some NRE and electrical test charges will apply. A PCB design also includes fabrication specifications and fab drawing notes, however. Several significant changes can be made to a PCB's specifications that alter the final product without triggering a new NRE or tooling charge.

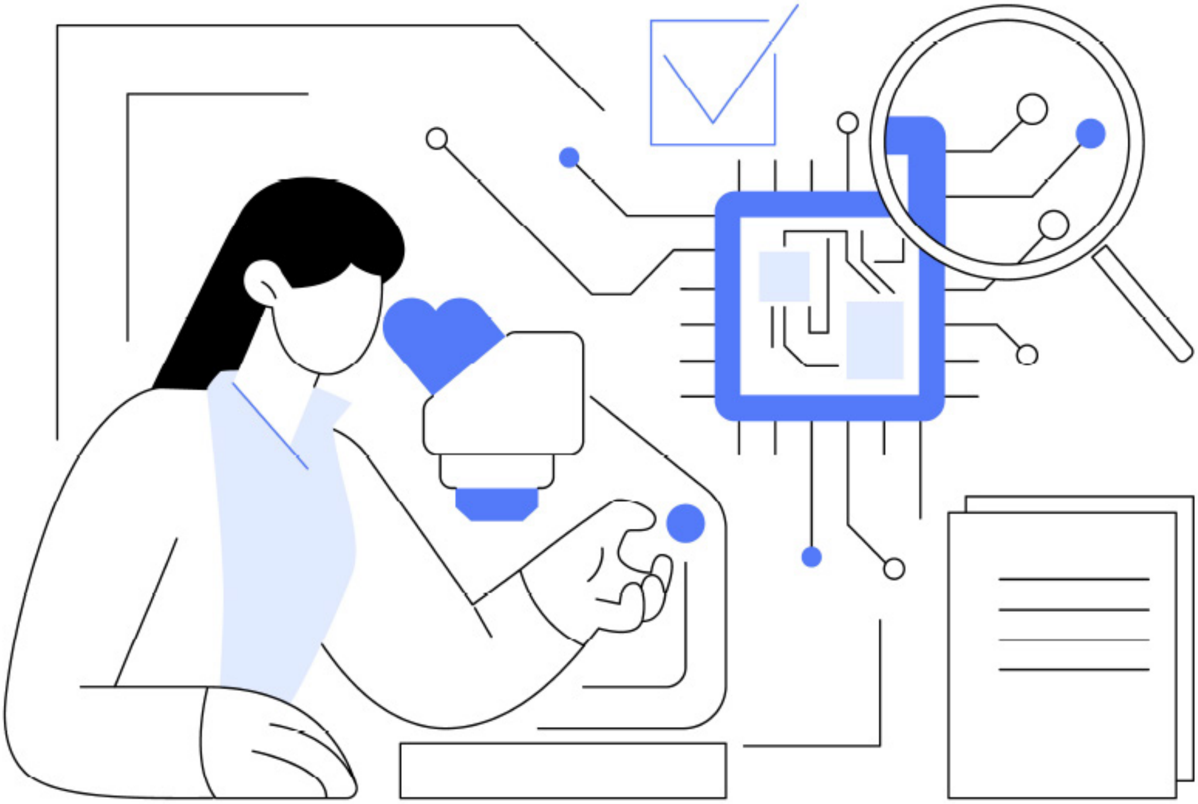


Figure 1. Changes that affect PCB layout, drilling, routing or connectivity typically require new NRE and electrical test programming, while specification changes such as solder mask color, surface finish or laminate material often can be made without new tooling charges.

Here are the changes you can make safely:

Solder mask and silkscreen colors. Changing a board from green solder mask with white silkscreen to matte black solder mask with yellow silkscreen typically will not incur an NRE charge. The physical layout – where the solder mask is applied and where the legend is printed – remains unchanged. The fabricator simply uses a different solder mask color or routes the panels through a different coating process. The unit cost may increase slightly for nonstandard colors because the application process differs, but the tooling remains the same. In some cases, however, tighter solder mask clearances achievable with green solder mask may not be possible with black solder mask.

Surface finish. If a board is originally designed with HASL (hot air solder leveling) and the assembler requires ENIG (electroless nickel immersion gold) to accommodate fine-pitch SMT components, the surface finish can typically be changed without incurring an NRE charge. The copper pads remain in the same locations; the fabricator simply routes the bare copper panel through the ENIG process instead of applying HASL. While the unit price may increase, the tooling does not change.

Base laminate material (Tg rating). Upgrading the FR-4 material is a common requirement. A design may originally specify standard Tg130 FR-4, only to later determine the board will operate in a high-temperature environment requiring Tg170 or Tg180 material. Because the change simply requires the fabricator to use a different laminate during board fabrication, the electronic design data remains unchanged and significant NRE charges may not apply. The material upgrade may increase the cost of the order, extend lead times if the laminate is not readily available and require updated impedance calculations that affect trace widths and spacing.

Overall board thickness. Changing the overall thickness of standard FR-4 (for example, from 1.6mm/0.062″ to 2.4mm/0.093″) generally does not incur an NRE charge, provided the layer count remains the same and the aspect ratio of the smallest drilled holes stays within the fabricator's capabilities. The CNC drill coordinates remain identical; the drill bit simply travels slightly deeper. If the increased thickness affects impedance calculations, however, additional engineering charges may apply.

Moving copper traces, pad or ground plane modification. As long as a plated through hole is not being repositioned, moving a copper trace that is too close to an edge, shaving or increasing a pad size or modifying the fill of a ground plane usually avoids NRE, especially when LDI is in use where there are no physical films involved.

Adding standard manufacturer markings. If a UL logo, date code or flammability rating is omitted from the original silkscreen layer, the fabricator can typically add it through the fabrication notes. The CAM department applies its standard, preapproved UL markings to the silkscreen layer automatically. Because this is a standard administrative addition rather than a custom layout change, most offshore fabricators will waive any NRE charge.

The Bottom Line

Designers and buyers need to communicate in advance with their board fabricators what changes are needed to a particular board and the impact they may have on the present tooling package.

Even if the change is simple, time and effort are needed for documentation. Revision changes must be recorded on both the drawing and the silkscreen of the board itself to prevent a "down-rev" from being built and/or assembled by mistake, and that documentation incurs some cost for the fabricator.

GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as the founder of a leading distributor. He is cofounder of DirectPCB (directpcb.com); greg@directpcb.com.

ECTC Focuses on Challenges for AI Data Center Packaging and Energy Use

Thousands of attendees gathered at ECTC to explore the latest advances in advanced packaging, AI-driven design, heterogeneous integration and thermal management.

MORE THAN 2,700 attendees conversed about the latest developments in packaging and assembly at the IEEE Electronics Components and Technology Conference (ECTC) in May in Orlando.

Conference organizers dedicated the event to the memory of industry icon Dr. William (Bill) Chen, who was instrumental in the formation of the Heterogeneous Integration Roadmap and a visionary in the industry. During the keynote, Tien Wu, CEO of Advanced Semiconductor Engineering, highlighted Dr. Chen's contributions and offered insights into advanced packaging trends and the future of system optimization.

Organizers devoted a full day to the Heterogeneous Integration Roadmap workshop, covering topics including additive electronics manufacturing for advanced packaging; metrology for advanced packaging, including challenges, innovations and industry impact; and emerging technologies such as neuromorphic computing.

Special sessions. Many of the overlapping special sessions on Tuesday focused on the role of artificial intelligence (AI). MIT Lincoln Laboratory and Nvidia chaired the special session "Quantum Infrastructure for AI Applications: Packaging Challenges and Roadmap," one of the first public discussions to address packaging for quantum AI infrastructure. Panelists represented MIT Lincoln Laboratory, IBM, IonQ, Google Quantum, Microsoft Quantum and PsiQuantum.

Ecole Centrale de Lyon and the University of Illinois Urbana-Champaign chaired the session "AI-Enabled Electronic Design Automation for Multi-Physics Advanced Packaging," with participants from EPFL, Arizona State University, Synopsys, Zhejiang University, Penn State University, Nvidia Research and TechSearch International.

CEA LETI and Corning led the session "Photonic-Based Systems for AI and Exascale Computing," which examined the AI-driven push toward co-packaged optics, including photonic chiplet architectures and photonic interposers. Panelists from Lightmatter, Scintil Photonics, TSMC, Cisco Systems and Mixx Technologies discussed 3-D hybrid bonding, laser integration challenges and implementation in foundries and outsourced semiconductor assembly and test (OSATs).

Cisco and Qnity Electronics chaired the panel "System Integration Challenges of Large-Size and High-Power

Components for High-Performance Computing and AI Applications." The panel examined system-level design challenges for packages larger than 100mm × 100mm and power levels exceeding 1,000W in high-performance computing (HPC) and AI network systems. Panelists from Cisco, AMD, the University of Texas Arlington, Marvell and Nvidia discussed current challenges and potential solutions.

AT&S and Rapidus chaired the session "New Packaging Technologies Enabled by Panel Level Integration," featuring panelists from the Georgia Institute of Technology, Qualcomm, Ajinomoto, Applied Materials, MKS Atotech, Yole and Broadpak. Discussions covered IC package substrate trends and developments in panel-level packaging (PLP). ASE, MKS and Volantis Semiconductor also explored PLP during the panel Enabling Next-Generation Advanced Packaging Technology from Wafer to Panel. Panelists from Resonac, ASE, Samsung Electro-Mechanics, AMD and LAM Research examined larger interposer and substrate requirements, embedded components, organic interposers and glass core substrates.

Sandisk and UCLA chaired the panel "Electrical-Thermal-Mechanical Co-Design in High-Performance Packaging," where panelists from Samsung Electro-Mechanics, AMD, ASE, Synopsys and MediaTek emphasized the need for co-design methodologies that integrate thermal, mechanical and electrical considerations as packaging complexity grows to support AI, HPC and heterogeneous integration.

Yield Engineering Systems and EV Group chaired the panel "Innovative Materials for Advanced Packaging." Resonac, Ajinomoto, Brewer Science and IMEC discussed polyimide and EMC materials, build-up materials, hybrid bonding dielectrics, adhesion and stress buffer layers and interconnect materials.

Rapidus organized an evening panel "Redefining System Integration: The Rise of Organic Substrates in the Chiplet Era." Panelists from Shinko Electric, Unimicron, ASE, Intel and Synopsys discussed substrate options, including embedded bridge technology, trends in build-up substrates and developments in glass core substrates.

Thursday's plenary session "Efficiency is Not Enough: Are We Solving the Wrong Problem in Data Center Energy Use?" featured panelists from AMD, Google, Microsoft Research, Accelsius, Marvell and IBM. The discussion focused on improvements in system architectures, including power delivery and thermal solutions. Panelists also explored customized chip-to-data-center power management; hardware and software infrastructure innovations; liquid cooling; codesign of optics, packaging, power delivery, memory and networking as a unified system; and use of simulations to evaluate software and hardware solutions, tradeoffs and optimization.

Binghamton University, Amkor and Auburn University organized Friday's plenary discussion "Data Centers in the Age of AI: Challenges and Solutions," featuring panelists from IBM, Nvidia, Cisco and Binghamton University. The panel examined the growing data center energy crisis, cooling technologies, the need for hardware-software co-design and the potential of co-packaged optics.

Startup competitions. ECTC featured two startup competitions. The ECTC Student Innovation Challenges Competition recognized finalists in two categories: BS/MS science and Ph.D.

A team from Georgia Tech won the undergraduate/master's category with its research, "Low-Cost Robust Thermal

Solution for High Power AI/Datacenter Processors." Nanyang Technological University in Singapore won the PhD category with its research, "Tetrahedral Amorphous Carbon as a Cu Diffusion Barrier in Through Silicon Vias Deposited by Filtered Cathodic Vacuum Arc."

Rapidus and Broadpak also organized a startup session focused on photonics companies.

Developments in RDL, Glass Substrates and CPO

Many presentations focused on high-performance packaging using molded redistribution layer (RDL) packages in both wafer and panel formats. Several speakers also provided updates on the status of glass core substrates, although few presentations included board-level reliability data from commercial products. Dai Nippon Printing (DNP) presented research on the use of a stress buffer layer to suppress SEWARE (glass cracking), reporting positive results following thermal shock and highly accelerated stress testing of a daisy-chain structure with 100 vias. Researchers and companies also highlighted improvements in through-glass via (TGV) fabrication and glass processing, including advances in TGV liner materials from Georgia Tech, SUNY Binghamton and Simmtech. AnyCasting of South Korea presented a metallization method that achieves zero voids in TGVs.

Nearly 30 presentations focused on co-packaged optics (CPO). SPIL discussed challenges related to optical engine integration. IME A*Star presented its PIC-in-mold interposer demonstration, while Sumitomo Bakelite described work on an RDL interposer for a waveguide. AIST and Kyocera demonstrated an embedded silicon photonic transceiver in an optical RDL. Corning, DNP and LPKF examined the role of glass in CPO, and Marvell highlighted CPO developments for networking applications.

Hybrid bonding and alternatives. More than 100 papers explored hybrid bonding and alternative technologies. CEA Leti presented research on ultra-low-temperature annealing, while cleaners demonstrated die-to-wafer (D2W) bonding down to a 1µm pitch for multi-die stacking integration. Researchers at IME A*Star examined the advantages and challenges of hybrid bonding for HBM. IBM introduced a dielectric integration approach to improve die thinning and intergap filling, and ASML reported its collaboration with IMEC to enable scalable D2W assembly.

Sony provided updates on its face-to-back die-to-wafer hybrid bonding work and also presented a wafer-to-wafer (W2W) process achieving 0.4µm pitch bonding. Applied Materials showcased 450nm pitch W2W bonding developed at its EPIC Center and presented joint work with EV group (EVG) that achieved 300nm pitch W2W bonding. IMEC discussed W2W bonding with a 200nm interconnect pitch using silicon carbon nitride (SiCN) to create a flat surface, while TEL presented research demonstrating 140nm pad pitch W2W bonding. Adia introduced a potential repair option performed before the annealing step.

Researchers also highlighted alternatives to hybrid bonding, including UCLA's Cu-to-Cu thermocompression bonding (TCB) and UC San Diego's TCB process with molded underfill. Several papers examined polymer processes that reduce particle contamination. ASE discussed low-temperature Cu/polymer hybrid bonding, and Rapidus presented a solder-polymer interconnect option featuring 25µm pitch microbumps.

Thermal discussions. IEEE's Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (iTherm) took place alongside ECTC. Conference tracks covered component- and system-level thermal management, mechanics, reliability, data center thermal technologies and emerging applications.

Approximately 25 iTherm presentations focused on data center energy use, noting that rack densities exceeding 200kW with 800V power distribution will require single- and multi-phase liquid cooling as well as integrated power conditioning. Speakers addressed thermal management from the die level through complete systems, data centers and grid infrastructure. Technical presentations covered microfluidic channels in glass substrates, real-time data and machine learning for data center cooling models, high-performance heat sinks and cold plates and heat capture and reuse. Additional presentations examined predictive analytics, machine learning and metrology. One presentation explored diamond heat spreaders grown on HEMT devices to improve thermal dissipation and reduce hotspots, while a professional development course provided an update on diamond research and applications.

ECTC returns to Colorado in 2026, and iTherm will once again be co-located.

E. JAN VARDAMAN is president of TechSearch International (techsearchinc.com) and a contributing editor for PCD&F/CIRCUITS ASSEMBLY; jan@techsearchinc.com.

DESIGNER'S **NOTEBOOK**

ICT vs. Flying Probe: Factory Testing of PCB Assemblies

From test coupons and burn-in chambers to ICT and flying probes, effective factory testing is essential for delivering reliable products and maintaining process control.

FACTORY TESTING COMES in numerous flavors. The goal is to ship products that work in the field. Failures erode gross margins, which in turn affect the company's market perception. Good customer relationships depend on the timely delivery of products that meet the requirements, which is the definition of quality. IPC-TM-650, *Test Methods Manual* covers the test procedures in detail.

This column covers the following topics:

- Disposition of defective materials
- Statistical process control
- Stress testing power delivery networks
- Bed-of-nails and flying probe test fixtures.

On the factory floor, units come off the line in rapid succession. Testing is performed, although resources for troubleshooting may not always be available. Rejected units may be recycled or repurposed after the removal of higher-value components, depending on the industry and component mix.

When a unit fails, it may be sent to a caged area of the factory known as the material review board (MRB), where it remains until the next review meeting. MRB teams typically meet weekly, although critical issues may warrant an immediate review. Quality engineers, manufacturing engineers, planners and other stakeholders determine the appropriate disposition: use as is (UAI), return to vendor (RTV), rework or scrap.

Test coupons and solder samples. Impedance coupons and solder samples may be included as part of the qualification process. The impedance coupons contain transmission lines similar to those used on the board and are measured at frequencies representative of normal operation. The impedance of the bare board typically must fall within ±10% of the specified nominal value before assembly can proceed.

Solder samples are subjected to tests intended to identify warpage, measling, delamination and other defects associated with the soldering process. These requirements are typically specified in the purchase order. The purchase order supersedes information on the fabrication drawing, while local and state regulations ultimately govern the agreement. Some purchase orders also require a certificate of compliance. Electrical testing using an IPC-356 netlist is commonly certified in this manner.

Tests exist for nearly every aspect of a printed circuit board. Warpage can be measured using a granite table and go/no-go gauges. A light table can reveal internal board features, while x-ray inspection is used to evaluate hidden solder joints beneath BGA devices. Simple adhesion testing can determine whether solder mask and silkscreen materials are properly bonded to the board.

Statistical process control. The goal in manufacturing is to ship products with at least Three Sigma quality. That is where 99.7% of the products work right out of the box. This level of quality is enough to say that the process is in control. Satellites, submarines and other stuff may call for Six Sigma quality where 99.99966% of the articles meet the requirements. The nondestructive testing may be performed on all units, but more likely, a random sample is selected.

If one or more samples fail to meet the acceptable quality level (AQL), the entire lot is rejected. The number of inspection samples for the next lot may be increased. That's also when destructive testing of the defective samples starts. The reliability lab will tear down some or all the units to find root causes and solutions.

It will probably not be economically or environmentally viable to put the whole batch into the dumpster. Instead, the units may be earmarked for a 60-day warranty rather than the usual year or two. The marginal lot would then end up with a reseller on Temu or perhaps a Dollar Store chain rather than a big-box retailer.

Behavior under less than ideal conditions. One of the key things to test, aside from the physical attributes, is whether the product can operate across the full range of acceptable voltage parameters. Every voltage domain has a minimum and a maximum input range. The standard +5V could range from 4.5V to 5.5V. The +/-10% may apply to 3.3V, 2.8V, 1.2V, and so on.

One phase of the test process would have the +5V cranked up to +5.5V while all other voltages are set to their minimum allowable values. Every possible combination of acceptable min and max power is tested. The "corner cases" may seem extreme, but they are emblematic of the methods used to evaluate electronics. More voltage domains equal more combinations to test.

While running at the various corners, look at the performance metrics. It could be an eye diagram or a Smith chart, whatever metric applies to the product. This type of stress testing will reveal any shortcomings in the power domain and signal integrity concerns.

Operating at high temperatures or cycling through temperature extremes will prematurely age electronics. A burn-in chamber will be used for this purpose. Sometimes the product goes full tilt until something breaks. A month-long burn-in at 80% of rated capacity is an example. If it survives that, then the "infant failures" are out of the way, granting the confidence necessary to ship the product.

Automated testing of printed circuit assemblies. Narrowing down the fault is sometimes done with in-circuit testing (ICT). A bed of nails is a type of fixture with spring-loaded pogo pins that align with a pattern of test points on the PCB. The least costly of these uses one side of the board for probing as many connections as possible.

Figure 1. An in-circuit test (ICT) fixture for simultaneous probing of both sides of the PCBA. (Source: Q1Test)

Placing test points on both sides will require a more costly clamshell fixture. Placing the test points close to one another is also a cost driver. It’s OK to be near low-profile components, while taller components will have more generous space. Of course, more test points are better when implementing a test fixture.

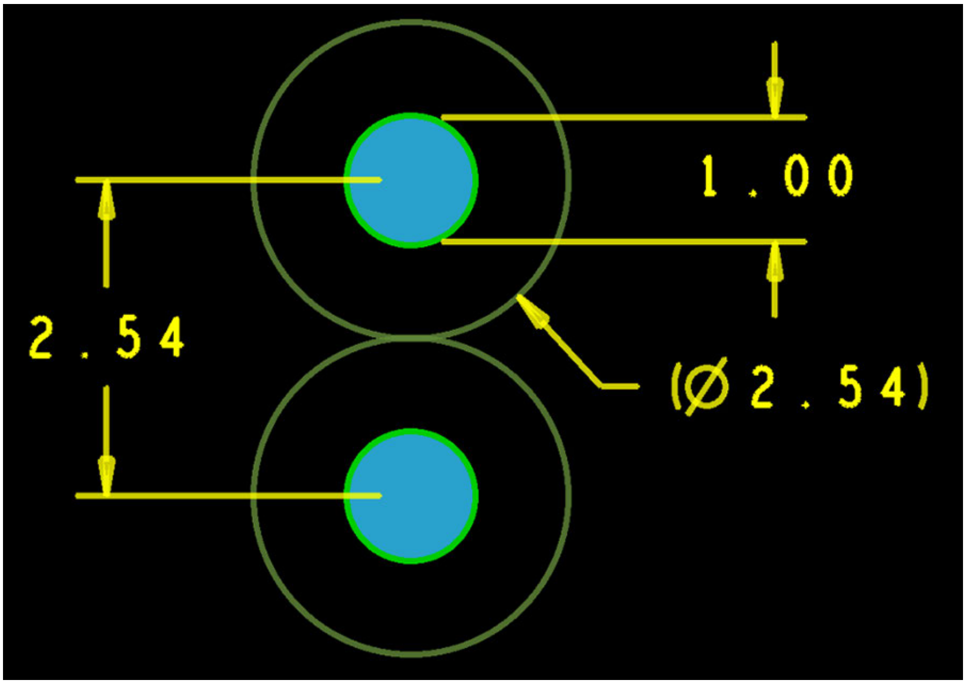


Figure 2. Nominal size and spacing for an ICT test point. (Source: Author)

In a perfect world, test points would be placed on a coarse grid and not clustered in a specific area. Each ICT probe will exert some force on the assembly. The result could be that the board flexes under the strain of dense test point placement.

```
PIN TP40.1 @          (84.250 3.700)    PEX_JTAG_TMS
PIN TP39.1 @          (84.250 2.300)    PEX_JTAG_TDO

Dist =            1.4000   Total Dist = 1.4000
Manhattan Dist = 1.4000   Dx = 0.0000  Dy = 1.4000
Pick Angle =      90.0000  degree
Air Gap =         0.690000   On layer:  BOTTOM
```

Figure 3. Test point spacing for flying probe testing, 0.7mm pad on 1.4mm pitch. This is a column of JTAG pins. (Source: Author)

Personally, I use the design for assembly (DfA) tool, which allows me to assess a part's proximity to other parts on a case-by-case basis. The DfA table has rows and columns to account for every part type. I give test points their own attribute, so they can cozy up to the short parts, give some room to the taller ones, and set a larger value for test point-to-test point spacing. That's the trick to getting the lowest cost ICT fixture.

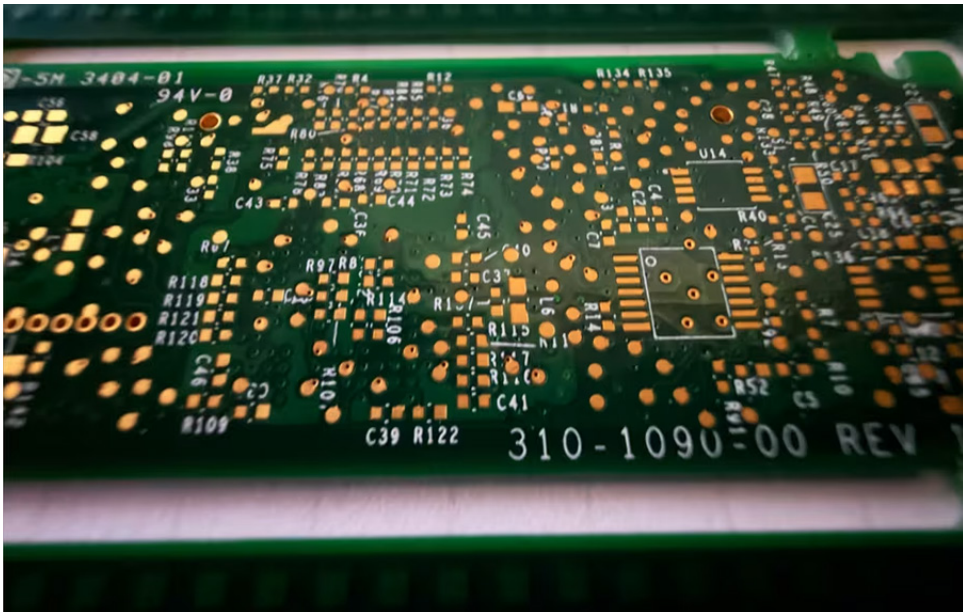
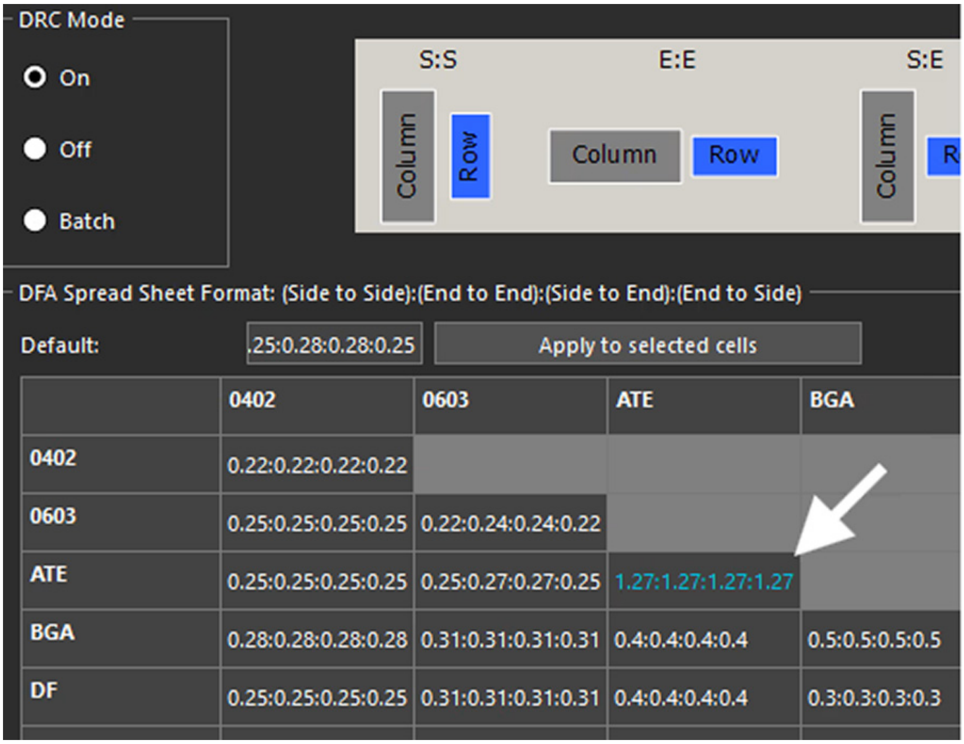


Figure 4. The secondary side is used for flying probe ICT and selecting components. (Source: Author)

Flying probe testing. An alternative to the expensive ICT fixture is a flying-probe machine. It works sort of like a pick-and-place machine. Instead of placing parts, it has multiple probe heads that "fly" around the board and take electrical measurements between pin pairs. These machines perform better if a number of gratuitous test points are in the power and ground planes scattered around the board.



DRC Mode

● On

○ Off

○ Batch

DFA Spread Sheet Format: (Side to Side):(End to End):(Side to End):(End to Side)

Default: .25:0.28:0.28:0.25

	0402	0603	ATE	BGA
0402	0.22:0.22:0.22:0.22			
0603	0.25:0.25:0.25:0.25	0.22:0.24:0.24:0.22		
ATE	0.25:0.25:0.25:0.25	0.25:0.27:0.27:0.25	1.27:1.27:1.27:1.27	
BGA	0.28:0.28:0.28:0.28	0.31:0.31:0.31:0.31	0.4:0.4:0.4:0.4	0.5:0.5:0.5:0.5
DF	0.25:0.25:0.25:0.25	0.31:0.31:0.31:0.31	0.4:0.4:0.4:0.4	0.3:0.3:0.3:0.3

Figure 5. An oversized courtyard at the intersection of the ATE values will single out test points for spacing rules around other test points. The category name is performed at the symbol level while the actual component spacing is constrained within the PCB editor. (Source: Author)

Once programmed, the flying head probes will run the test repeatedly. The time it takes will depend on how many pin pairs it must probe. Flying probe is generally a slower process than a bed-of-nails fixture. The benefit is they are much more agile when it comes to a board revision where a few test points were moved, added or subtracted.

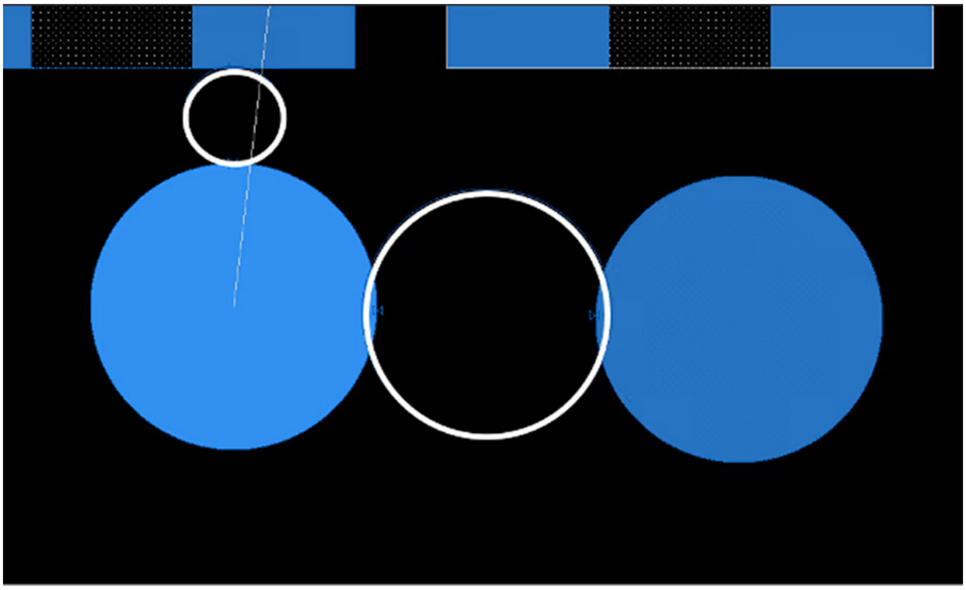


Figure 6. The different values in the DfA table create specific guidance in terms of spacing. The test point can be nearer to the capacitor than to another test point. (Source: Author)

Wrapping It Up

Tests and measurements become more difficult as component density increases. Competition to create the smallest, most efficient form factor drives products that are dominated by the need to do more with less. A JTAG connector may be our only access, if even that. Designers of embedded electronics are pulled in several directions at once. Be flexible.

JOHN BURKHERT, JR. is a principle PCB designer in retirement. For the past several years, he has been sharing what he has learned for the sake of helping fresh and ambitious PCB designers. The knowledge is passed along through stories and lessons learned from three decades of design, including the most basic one-layer board up to the high-reliability rigid-flex HDI designs for aerospace and military applications. John's well-earned free time is spent on a bike, or with a mic doing a karaoke jam.

DESIGN **BEST PRACTICES**

When the BoM Breaks the Design: Why Supply Chain Resilience Starts at the Engineer's Desk

Supply chain disruptions may be inevitable, but the ability to design around them doesn't have to be an afterthought.

IF IT FEELS like supply chains are back in the headlines again, that's because they are. Only this time it's not a pandemic driving the disruption; it's geopolitics.

The current conflict between the US and Iran is yet another reminder of how interconnected and fragile the global electronics ecosystem has become. Semiconductor manufacturing depends on complex networks of raw materials, fabrication capacity, assembly operations, transportation infrastructure and energy resources spread across multiple regions of the world. When instability affects any one of those areas, the consequences can ripple across the entire product development lifecycle.

For those of us involved in electronics design, however, none of this should come as a surprise.

We've lived through it before. And if the past several years have taught us anything, it's that supply chain volatility is no longer an exception to plan around – it has become a baseline design condition.

Let me rewind to a story I've shared before because, unfortunately, it remains just as relevant today. Early in the Covid era, I was leading PCB layout on a project that should have been relatively straightforward. Requirements were stable. The customer was well known. The design itself wasn't pushing technological boundaries.

Yet we redesigned that board 12 separate times. Not because requirements changed. Not because the design failed electrically. Not because manufacturing discovered a problem. We redesigned it because components kept disappearing.

Every time we thought we were ready to move forward, another part of the BoM became unavailable. Approved alternates disappeared. Lead times stretched beyond acceptable limits. Parts that looked secure one week became unattainable the next.

The result was a constant cycle of schematic updates, library requests, engineering reviews, and layout rework. For months, the most common phrase heard during project meetings was simple: "Another part on the BoM isn't available."

At the time, many organizations viewed this as a temporary disruption. Looking back, it was exposing a much larger weakness in how we develop products.

While component shortages create immediate challenges, they also expose something deeper: many engineering organizations still operate with workflows built for a more predictable world.

The traditional process remains largely sequential. Engineering designs the product. Layout progresses. Momentum builds. Then, the supply chain and procurement perform a detailed BoM assessment focused on availability, lifecycle status, lead times and cost. For years, this approach worked reasonably well. Today, it increasingly does not.

When a significant portion of the BoM suddenly becomes unavailable, the process enters a familiar cycle of stop, rework, restart and repeat. Engineering loses momentum. Schedules slip. Resources are consumed by redesign activity rather than innovation.

As a PCB designer, I have experienced this firsthand. By the time those discoveries occur, engineering effort has already been invested. The layout has progressed. Constraints have been validated. Decisions have been made. The later the issue is discovered, the more expensive the correction becomes. This is precisely why supply chain resilience can no longer be treated as a downstream activity. It has become an engineering consideration.

Breaking Organizational Silos

One of the most persistent challenges I have observed throughout my career is the separation between engineering and supply chain functions. Engineering operates in one domain.

Procurement operates in another. Supply chain teams operate in yet another. Each group possesses valuable information, but that information often arrives too late to influence the decisions that matter most.

Meanwhile, engineers frequently attempt to compensate for this lack of visibility themselves. They search distributor websites, compare availability across suppliers, review lifecycle notices, and build their own spreadsheets to assess risk. The problem isn’t a lack of effort. The problem is a lack of connected intelligence.

Modern product development requires more than isolated expertise. It requires visibility across traditionally disconnected functions so decisions can be made with complete context rather than assumptions.

This is where the conversation shifts less from procurement and more toward engineering methodology. The objective is not to turn engineers into buyers. The objective is to provide engineers with actionable component intelligence at the point where design decisions are being made.

When engineers have visibility into availability trends, lifecycle status, supplier concentration, pricing volatility and risk factors while selecting components, the quality of those decisions improves significantly. More importantly, the cost of change remains low. This represents a fundamental shift from reactive BoM validation toward continuous component intelligence integrated directly into the design process.

Much like design reuse, automation, and abstraction have transformed other aspects of engineering productivity, supply chain intelligence must become part of the broader engineering workflow rather than a disconnected downstream activity. Organizations that successfully make this transition will spend less time recovering from disruptions and more time delivering innovation.

Covid also revealed another important lesson: reacting to uncertainty can be just as costly as the uncertainty itself. Many organizations responded to shortages by adopting aggressive purchasing strategies to secure inventory months or even years in advance. While understandable, these decisions often created new risks.

When designs changed, requirements shifted or technologies evolved, companies found themselves carrying inventory they could no longer effectively use. Capital became trapped. Flexibility decreased. Margins suffered.

This highlights an important reality that experienced engineers eventually learn: Good design decisions cannot be separated from cost, risk, manufacturability, and supply chain considerations. Engineering does not operate independently from business outcomes. It directly influences them.

A Permanent Change in the Design Environment

The current geopolitical environment simply reinforces what many engineering organizations should already recognize. Global supply chains have become increasingly interconnected, complex and vulnerable to disruption.

Whether the catalyst is geopolitical conflict, trade restrictions, tariffs, natural disasters, climate events, transportation bottlenecks or future pandemics is almost beside the point. The source of disruption may change. The existence of disruption will not. This means uncertainty itself has become a design constraint. And like any design constraint, it must be accounted for early, continuously and deliberately.

Designing for supply chain resilience is not about predicting the future. It is about making better decisions with the information available today. It means bringing risk awareness upstream. It means replacing assumptions with visibility. It means reducing rework instead of repeatedly absorbing it. Most importantly, it means recognizing that resilience is no longer solely a supply chain objective. It is an engineering discipline.

The organizations that thrive in the years ahead will not be the ones that react fastest to disruption. They will be the ones who design resilience into their processes, workflows, and engineering decisions from the beginning.

Because in a world where uncertainty has become a permanent design constraint, resilience is not something to bolt on at the end. It is something to intentionally design in from the start.

STEPHEN CHAVEZ is a senior printed circuit engineer with three decades' experience. In his current role as a senior product marketing manager with Siemens EDA, his focus is on developing methodologies that assist customers in adopting a strategy for resilience. He is an IPC Certified Master Instructor Trainer (MIT) for PCB design, IPC CID+, and a Certified Printed Circuit Designer (CPCD). He is chairman of the Printed Circuit Engineering Association (PCEA); stephen.chavez@siemens.com. He will speak on a variety of design topics at PCB West in September.

PCB WEST 2026

Conference & Exhibition

Exhibition: Wed., Sept. 30

Conference: Sept. 29 - Oct. 2

Santa Clara Convention Center

WHO'S EXHIBITING (to date)

ABeetle Corporation
Advanced Chip & Circuit Materials, Inc.
Aismalibar NA
All Flex Solutions, Inc.
Allspice.io
Altium
Arlon-EMD Specialty Materials LLC
ASC Sunstone Circuits
atopile
Bay Area Circuits
Best Technology Circuit Co., Limited
Boardera Software Inc
Breadboard
Cadence
Cadstrom.io
Cicor Group
Circuitly
Cofactr
Cybord
DirectPCB
DYCONEX AG
Element Materials Technology
Eleprint S.R.L.
EMA Design Automation
ESPEC North America Inc.
Fineline Global
Flexible Circuit Technologies
FTG Corporation
Freedom CAD Services, Inc.
Glory Faith Electronics Co., Ltd.
GS Swiss PCB AG
Horizon Industrial Systems, Inc.
IBE Electronics Inc.
Imagineering, Inc.
Intec Display
InstaDeep
IPC-2581 Consortium
Ironwood Electronics
Isola Group
JetPCB
Jinsung Electronics Co. Ltd.
JITX
JS Circuit
Kayaku Advanced Materials
KiCad EDA
Lin Horn Technology Co., Ltd.
Luminovo Inc.
MaRCTech2. Inc.
MFG Innovations Inc.
MFS Technology
Millennium Circuits Limited
Multiline Technology
Newgrange Design
NextPCB
Noritake
Numerical Innovations Inc.
Oak-Mitsui Technologies LLC
OKI Circuit Technology Co., Ltd.
Oneida Research Services, Inc.
Optiprint AG
PalPilot International Corp.
Panasonic Industry – Electronic Materials
Parter
PCB Technologies – USA
PCBWay
Pentalogix, Inc.
Polar Instruments, Inc.
Polyonics
PNC, Inc.
Precision PCB
Quantic Ohmega – Ticer
REMTEC
Rogers Corporation
Sanmina Corp.
Screaming Circuits
SEP Co., Ltd.
Shenzhen Jove Enterprise Limited
Siemens
Sierra Circuits
SiliconExpert Technologies
Sotatronix
Sourceability
Sun Chemical
Sunshine Global Circuits
Suntech Circuits
SVTronics, Inc.
TCLAD
The Test Connection / TTC-LLC
TLT Electronics
Trylene Inc.
United Pacific Electronics, Inc.
Vayo Technology
Ventec International Group
Victory Giant Technology (VGTPCB)
Voltai
Winonics
Zenode
Zuken USA Inc.

pcbwest.com

ECAD TIPS & TRICKS

PCB Stackups: A Brief History

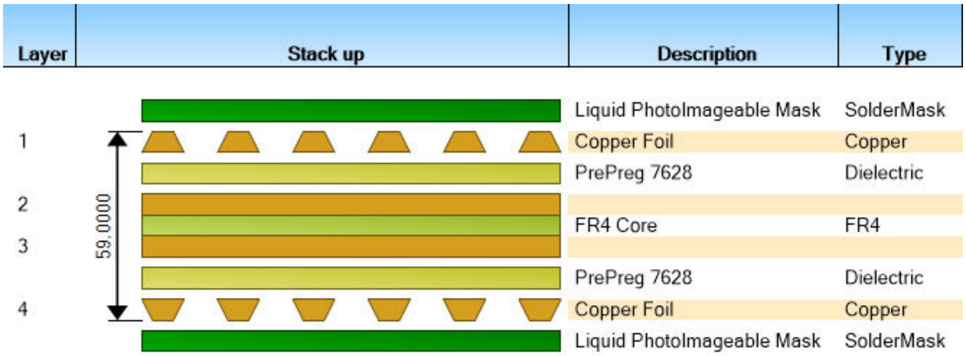
The evolution of layer stackups, from simple constructions to sequential lamination.

STACKUP, THE BUILDUP of PCBs, has grown in importance over the past few decades. In the early days PCBs functioned primarily as interconnect, and the need for stackup was minimal. On a single-sided PCB, the "stack" is simply one piece of clad material. Even the board thickness was rarely a consideration unless it had to plug into an edge connector.

With the advent of multilayer PCBs, however, the stack of materials is more critical and, as always, cost is often the underlying driver. Stackups can range from the simplest four-layer PCB to complex stackups requiring sequential lamination.

Let's take the humble four-layer PCB. PCB designers not familiar with fabrication may be forgiven for thinking that the four-layer board consists of two double-sided rigid boards bonded together with an additional layer of unclad material. It may come as a surprise, then, that most four-layer boards are stacked as a central two-layer PCB with two sheets of copper foil laminated on the outside, with the bonding provided by a layer or two of glass cloth "pre-impregnated" with uncured resin (prepreg).

Foil and core builds. This most basic four-layer stackup (and simplest to build for the fabricator) is called a "foil build" **(Figure 1)**, with a foil on the outer layer of the stack. This is the most common build for even higher-layer-count boards.



Layer	Stack up	Description	Type
		Liquid PhotoImageable Mask	SolderMask
1		Copper Foil	Copper
		PrePreg 7628	Dielectric
2			
		FR4 Core	FR4
3			
		PrePreg 7628	Dielectric
4		Copper Foil	Copper
		Liquid PhotoImageable Mask	SolderMask

Figure 1. A four-layer foil build stackup.

A common question is, When are two two-layer boards laminated together? Most often, this construction is used in microwave applications where expensive microwave materials are laminated together with a lower-cost internal bonding layer. This type of four-layer (or more) stackup is called a “core build” because it comprises core materials on the outer layers **(Figure 2)**.

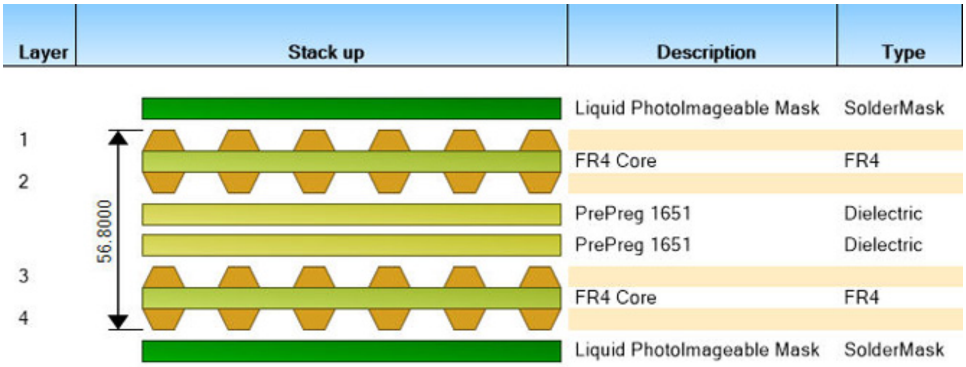


Figure 2. A four-layer core build stackup.

Outside of the microwave world – where designers working with ever-higher device integration need more layers for routing – some of those layers or layer groups (sometimes called cells of layers) may comprise high-speed materials. These may require different processing, but invariably, high-speed materials are higher in cost. So, for volume use, designers try to build stackups with a mix of appropriate materials for each layer type, resulting in even more complex stackups.

Sequential lamination. By taking the PCB through the production process multiple times, boards can be built with drilled holes that appear to go only through parts of the stack. The process for this type of complex stackup is called sequential lamination. It can offer benefits for signal integrity (shorter vias) and provide greater flexibility in interlayer interconnect than a traditional stackup, which uses holes drilled through the entire board.

HDI stackup. The icing on the cake for complex rigid multilayers is the HDI stackup, where additional layers are laminated with multiple passes through the production process and laser-drilled to provide even greater interconnect density and enhanced signal integrity. A typical HDI build with its three press cycles is shown in **Figure 3**. From a stackup perspective, consideration should be given to glass styles that benefit from laser drilling, such as flat or spread glass.

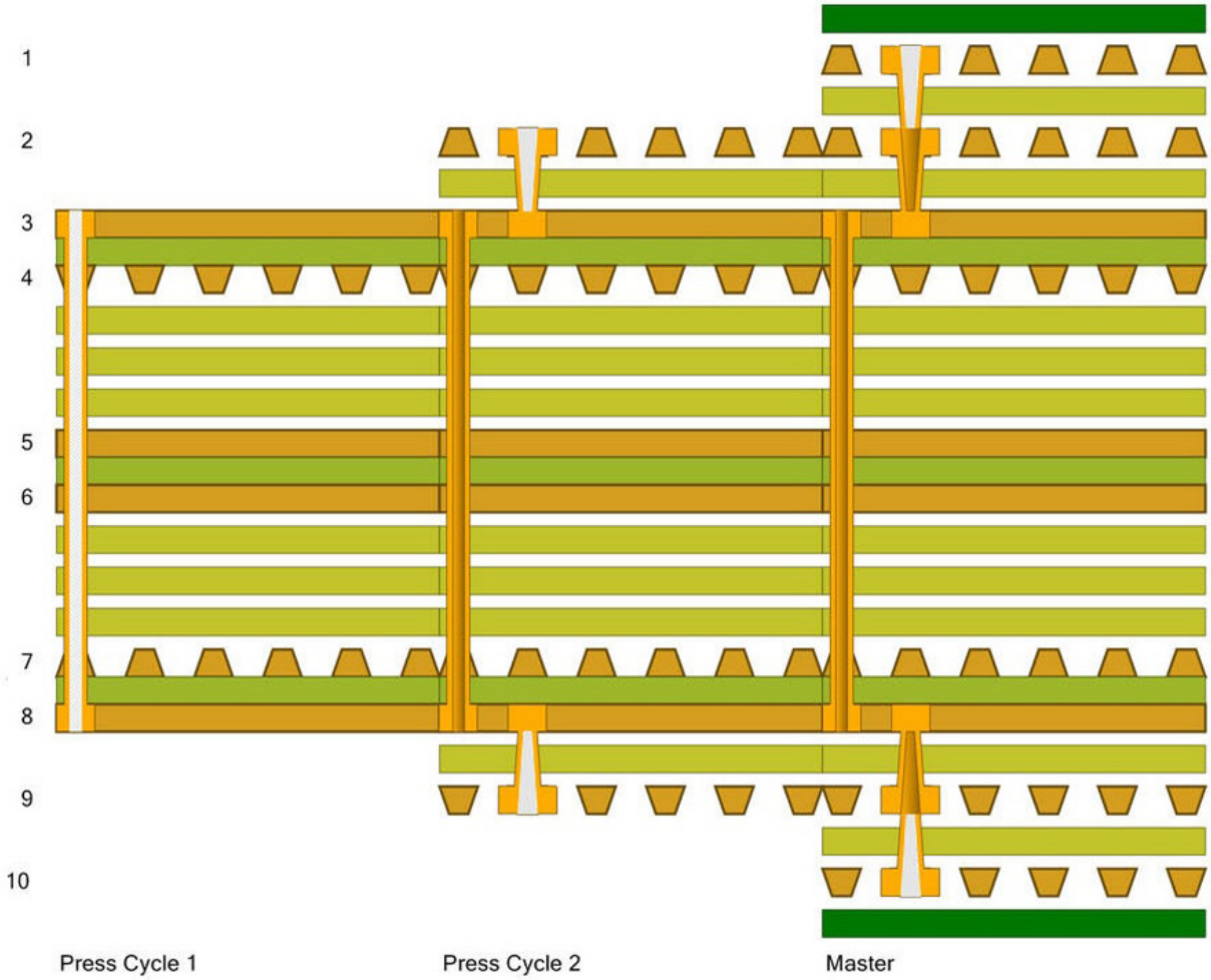


Figure 3. A multiple press cycle HDI build.

Complex? Yes. From its humble origins, the PCB has developed into a complex interconnect device containing components including fabricated inductors, capacitors and transmission lines. PCB design engineers have the task of ensuring that the layer stackup is designed in a cost-effective, reliable way that is appropriate for the application and the lowest cost and easiest to fabricate. Flex and flex-rigid PCBs bring in a whole new layer (excuse the pun) of complexity.

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Why Human Expertise Still Matters in High-Performance Computing

High-performance computing has moved out of its niche to become a mainstream requirement and continues to rely on human skills to deliver its optimum potential.

HISTORICALLY, SUPERCOMPUTING HAS been a niche discipline, the preserve of rare and almost mythical machines embodying esoteric design principles. Only a tiny number of organizations, such as national laboratories, top-tier businesses and elite universities, had workloads that justified using them. Also, there were only a few engineers and scientists in the world capable of running them.

Now, thanks to several generations of technology scaling, compute performance is more readily and cheaply available at any level, from tiny, embedded microcontrollers to desktop machines, rack servers and hyperscale cabinets. Together with innovative concepts like Beowulf clusters, which build supercomputers from general-purpose off-the-shelf computers at a fraction of the cost, these have created a democratizing effect that has helped set the scene for practicable and affordable high-performance computing (HPC) as we know it today. The PCB industry has played its part, providing substrates that not only support high signal speeds but also critically address the thermal issues intrinsic to HPC.

Driving this ingenuity, of course, are the market dynamics affecting today's businesses and research institutions. Companies can no longer rely on incremental product improvements or greater supply chain efficiency to compete for market share, and researchers seeking progress in increasingly complex fields need to deliver results quickly to meet funding obligations. The key to success in these times is computational. As more computing means greater advantage, more organizations need HPC to handle workloads such as retail demand forecasting, biotech simulations, financial risk modeling and digital twinning. While they may not be "supercomputer workloads" in the old sense, these are the challenges HPC was built for.

Where should HPC be implemented, and how? There are several options, and all have their advantages and drawbacks. On-premises HPC can suit organizations with steady, intensive, tightly coupled workloads that justify owning specialized hardware and the staff to run it. The Beowulf clusters I mentioned earlier, which rely on tuning instinct and tacit knowledge within the management team, are less common now than vendor-supported hardware that offers advantages such as predictability and lifecycle management.

The alternative is the cloud. Running HPC workloads here can offer greater flexibility and faster access to new hardware options, providing a pay-as-you-go model that can help companies reduce capital expenditure. Some workloads can be more expensive to perform in the cloud, while hazards can include latency and performance variability. Also, opportunities for users to fine-tune the hardware can be limited.

The importance of fine-tuning highlights the value of human know-how in running an enterprise HPC system. While managing ordinary enterprise IT prioritizes standardization, repeatability and risk minimization, running an on-premises HPC cluster emphasizes optimization and maximizing hardware performance. Key concerns are density, requiring concentrated processing power closely coupled with storage, and latency across memory interfaces and in data exchanges. Typical ways to address latency include high-bandwidth interfaces such as InfiniBand and kernel-bypass techniques that enable direct access to data storage and hardware resources. Techniques like these can bring latency down into the single-digit microsecond range and are usually specific to HPC, quite unlike the standardization and generalization sought by enterprise IT teams.

Managing on-premises HPC effectively requires an intimate grasp of the organization's computational workloads, as well as the technicalities of building and running the machines. With the option to move HPC to the cloud, organizations need to retain this human-contained value that truly understands the minute details of workloads and their interactions with hardware.

Figure 1. High-performance computing has evolved from specialized supercomputers to widely accessible clusters and cloud platforms, enabling organizations to tackle increasingly complex computational workloads while still relying on human expertise for optimization and management.

Into this discussion comes the concept of infrastructure as code (IaC), which automates the provisioning of compute resources. IaC permits repeatable builds and faster adoption of new hardware, with provision for version control. It also eases scaling, makes workloads portable, and supports system rebuilds, thereby aiding disaster recovery. While

IaC can bring these qualities to on-premises HPC, it's an essential tool for companies seeking to run part or all their HPC in the cloud. It becomes possible to build, run and tear down a cluster in hours on rented hardware that can then be reassigned to another subscriber.

We could perceive IaC as yet another instance in which automation, powered by software-defined-everything, is forcing humans out of the equation. But it's changing, rather than replacing, the role of the enterprise HPC team. Instead of tending to the tangible equipment in the computer room, in-house teams are focusing on high-level activities, working with the company's HPC users to define the compute environment that automated tools must then reproduce. This makes it possible for the HPC engine to be hosted on-premises, in the cloud, in a hybrid of the two, or even on multiple clouds. The team's expertise makes this possible by applying their combined understanding of workloads and infrastructure to optimize profiles, ensure the cluster behaves as desired, and manage cost/performance trade-offs.

The story of HPC is intriguing and, in many ways, closely parallels the general arc of progress in the high-tech economy. It's become a defining requirement for organizations, both large and small, and a critical capability for competing. Enabled by the commoditization of powerful compute and high-density memory, it has democratized supercomputing and is transforming the business landscape as well as the hardware sitting in on-premises server rooms. Off-premises, the big computing companies offer HPC services that leverage automated tools, allowing customers to configure their own HPC clusters to handle specific workloads. Either way, ensuring that users' needs are met effectively and as efficiently as possible remains contingent on human skills and expertise.

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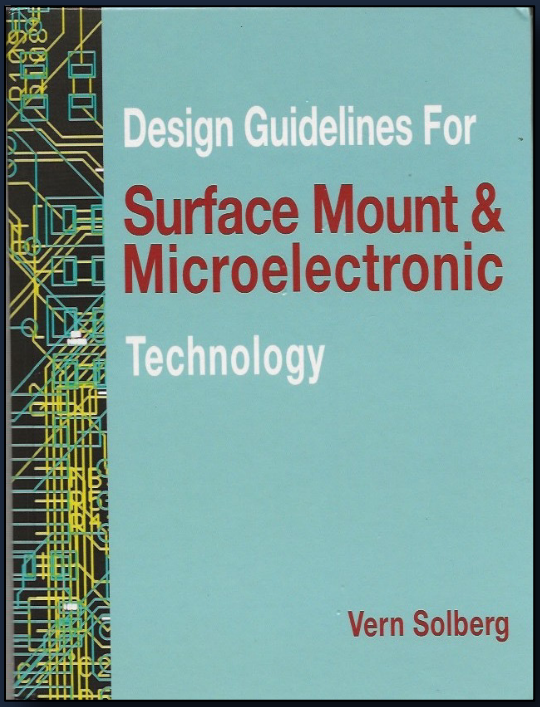


It’s Time to Move Beyond Gerbers

As PCB designs grow more complex, IPC-2581 offers a different approach to manufacturing data exchange.

THE ELECTRONICS INDUSTRY has spent decades perfecting PCB design tools, automating verification, embracing digital twins and accelerating product development using AI tools. Yet when it’s time to send a design to manufacturing, many organizations still fall back on a process that hasn’t fundamentally changed in decades – export Gerbers, generate drill files, create spreadsheets, collect PDFs, zip everything together, and email the package.

This isn’t happening because there isn’t a better alternative. It’s happening because old habits are hard to break.

Today, virtually every major PCB design system – including Cadence, Altium, Siemens Pads and Xpedition, Zuken CR-8000 Design Force, Pulsonix, KiCad and Easy-PC – can generate IPC-2581 directly from the PCB editor. There are no additional translators to purchase, no special software to install and no licensing costs to create the file. For most designers, generating IPC-2581 is simply another output option already built into the tool they use every day.

The barrier is no longer technology. The barrier is mindset.

IPC-2581 was created by the industry, for the industry. It is an open, neutral global standard managed by GEA, not by any single software vendor. More than 120 companies worldwide now participate in its development and adoption because they recognize that modern manufacturing requires something more intelligent than a collection of disconnected files.

Instead of sending dozens of files that someone on the manufacturing side must interpret, IPC-2581 delivers a complete digital product model in a single intelligent file. Stackup, artwork, drill data, netlist, bill of materials, component placement, impedance requirements, fabrication notes and manufacturing specifications all travel together as one consistent dataset.

Manufacturers report reductions of up to 30% in pre-CAM engineering time because they spend less time searching for missing information, resolving inconsistencies and asking questions before production can begin. Once you account for the bidirectional capabilities of IPC-2581, eliminating endless, frustrating back-and-forth on package validation and the DfM exchange, both the designer and their manufacturing partners can save several weeks.

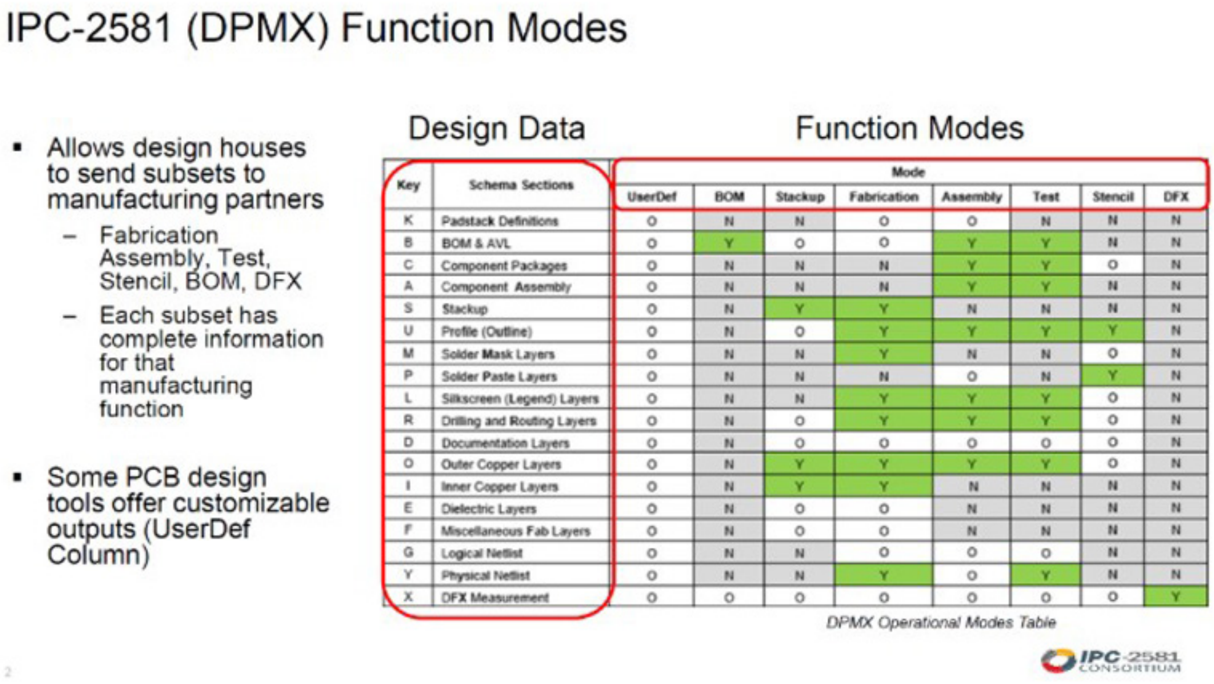
But efficiency is only one benefit. The real opportunity comes from changing the way design teams think about manufacturing data exchange.

Traditional Gerber packages, and even many ODB++ workflows, follow a one-way handoff model. Once the package leaves engineering, the entire design is typically shared with every manufacturing partner, regardless of how much information it actually needs. Fabricators, assemblers, stencil suppliers and test houses often receive the complete design database even though each partner requires only a portion of the information.

That approach made sense years ago. It doesn't make sense today.

Modern product development is collaborative, connected and increasingly focused on protecting valuable intellectual property. IPC-2581 introduces capabilities that simply didn't exist in any other manufacturing format.

Its function mode allows engineering teams to generate purpose-built datasets for fabrication, assembly, stencil creation, testing, stackup review, DfX analysis and more. Each manufacturing partner receives only the information required to perform their specific task, and nothing more. That's IP protection; the benefit is huge **(Figure 1)**.



IPC-2581 (DPMX) Function Modes

- Allows design houses to send subsets to manufacturing partners
  - Fabrication Assembly, Test, Stencil, BOM, DFX
  - Each subset has complete information for that manufacturing function
- Some PCB design tools offer customizable outputs (UserDef Column)

Design Data

Function Modes

Key	Schema Sections	Mode							
		UserDef	BOM	Stackup	Fabrication	Assembly	Test	Stencil	DFX
K	Padstack Definitions	O	N	N	O	O	N	N	N
B	BOM & AVL	O	Y	O	O	Y	Y	N	N
C	Component Packages	O	N	N	N	Y	Y	O	N
A	Component Assembly	O	N	N	N	Y	Y	N	N
S	Stackup	O	N	Y	Y	N	N	N	N
U	Profile (Outline)	O	N	O	Y	Y	Y	Y	N
M	Solder Mask Layers	O	N	N	Y	N	N	O	N
P	Solder Paste Layers	O	N	N	N	O	N	Y	N
L	Silkscreen (Legend) Layers	O	N	N	Y	Y	Y	O	N
R	Drilling and Routing Layers	O	N	O	Y	Y	Y	O	N
D	Documentation Layers	O	N	O	O	O	O	O	N
O	Outer Copper Layers	O	N	Y	Y	Y	Y	O	N
I	Inner Copper Layers	O	N	Y	Y	N	N	N	N
E	Dielectric Layers	O	N	O	O	N	N	N	N
F	Miscellaneous Fab Layers	O	N	O	O	N	N	N	N
G	Logical Netlist	O	N	N	O	O	O	N	N
Y	Physical Netlist	O	N	N	Y	O	Y	N	N
X	DFX Measurement	O	O	O	O	O	O	O	Y

DPMX Operational Modes Table

IPC-2581 CONSORTIUM

Figure 1. Built-in function modes enable IP protection. Some vendors allow users to create a user-defined mode to customize what content to send to a specific manufacturing partner.

IPC-2581 also enables something the industry has wanted for years: true bidirectional collaboration.

Instead of exchanging stackup revisions, manufacturability questions and engineering clarifications through disconnected emails and spreadsheets, IPC-2581 provides dedicated stackup exchange and DfX modules that allow technical information to move electronically between design and manufacturing teams. Questions become traceable. Feedback becomes structured. Communication becomes part of the digital product model rather than an external conversation.

No other manufacturing data standard provides this level of intelligent collaboration.

The good news is that adopting IPC-2581 doesn't require changing your PCB design software. It doesn't require purchasing expensive add-ons. It doesn't require redesigning your products. In most cases, it simply requires selecting a different export option and committing to a smarter workflow.

Digital transformation isn't about replacing people or replacing tools. It's about replacing outdated processes with better ones.

Our industry has embraced model-based design, AI-assisted engineering, cloud collaboration and digital manufacturing. Yet many organizations continue to exchange manufacturing data using workflows that belong to another era.

The technology has already caught up. The standards are mature. The software is ready. The ecosystem supports it.

Now the only remaining question is whether we're ready to leave behind the habits of yesterday and embrace the intelligent, secure, collaborative data exchange that modern electronics manufacturing deserves.

Here's a simple challenge: spend 10 minutes generating an IPC-2581 file from an existing PCB design. It's surprising how easy it is. Anyone familiar with generating Gerber or ODB++ data already understands most of the process.

Start by setting up the design as normal for manufacturing output, all artwork layers, drill data, fabrication details and other manufacturing information. Then, instead of selecting Gerber or ODB++, simply choose IPC-2581 from the PCB design tool's File → Export (or Import/Export) menu **(Figures 2**, **3** and **4)**.

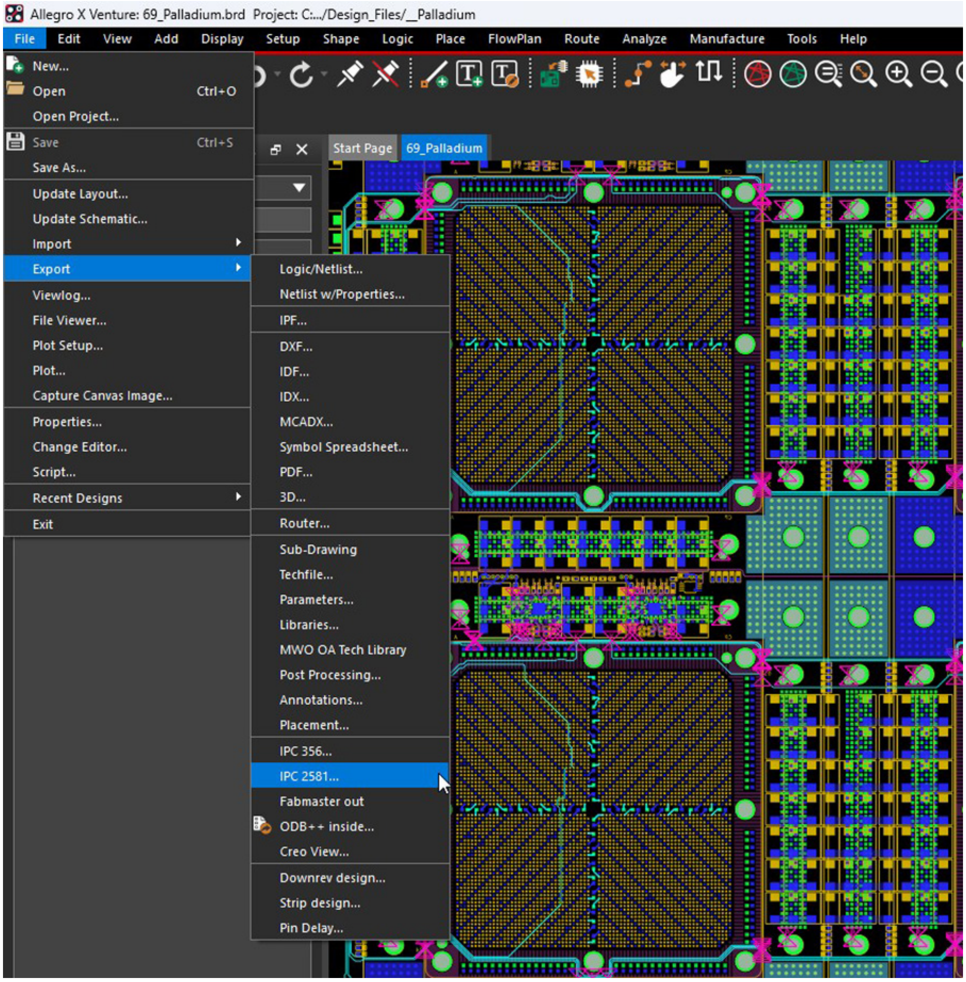
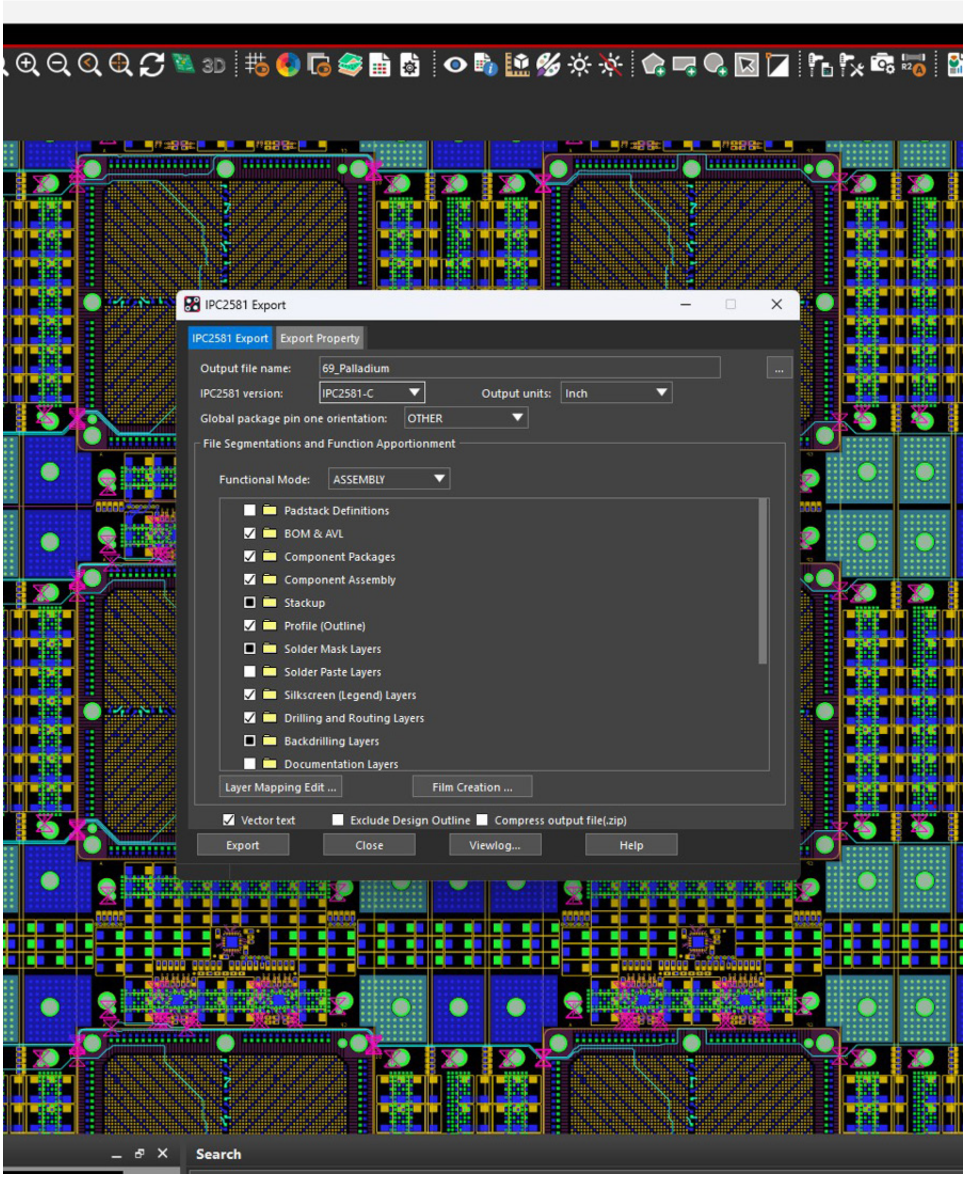


Figure 2. Exporting data to an IPC-2581 file is easy.



Output file name: 69_Palladium

IPC2581 version: IPC2581-C

Output units: Inch

Global package pin one orientation: OTHER

File Segmentations and Function Apportionment

Functional Mode: ASSEMBLY

- ☐ Padstack Definitions
- ☑ BOM & AVL
- ☑ Component Packages
- ☑ Component Assembly
- ☐ Stackup
- ☑ Profile (Outline)
- ☐ Solder Mask Layers
- ☐ Solder Paste Layers
- ☑ Silkscreen (Legend) Layers
- ☑ Drilling and Routing Layers
- ☐ Backdrilling Layers
- ☐ Documentation Layers

☑ Vector text ☐ Exclude Design Outline ☐ Compress output file(.zip)

Figure 3. IPC-2581 export options are built directly into most major PCB design tools, making file generation a straightforward part of the manufacturing output process.

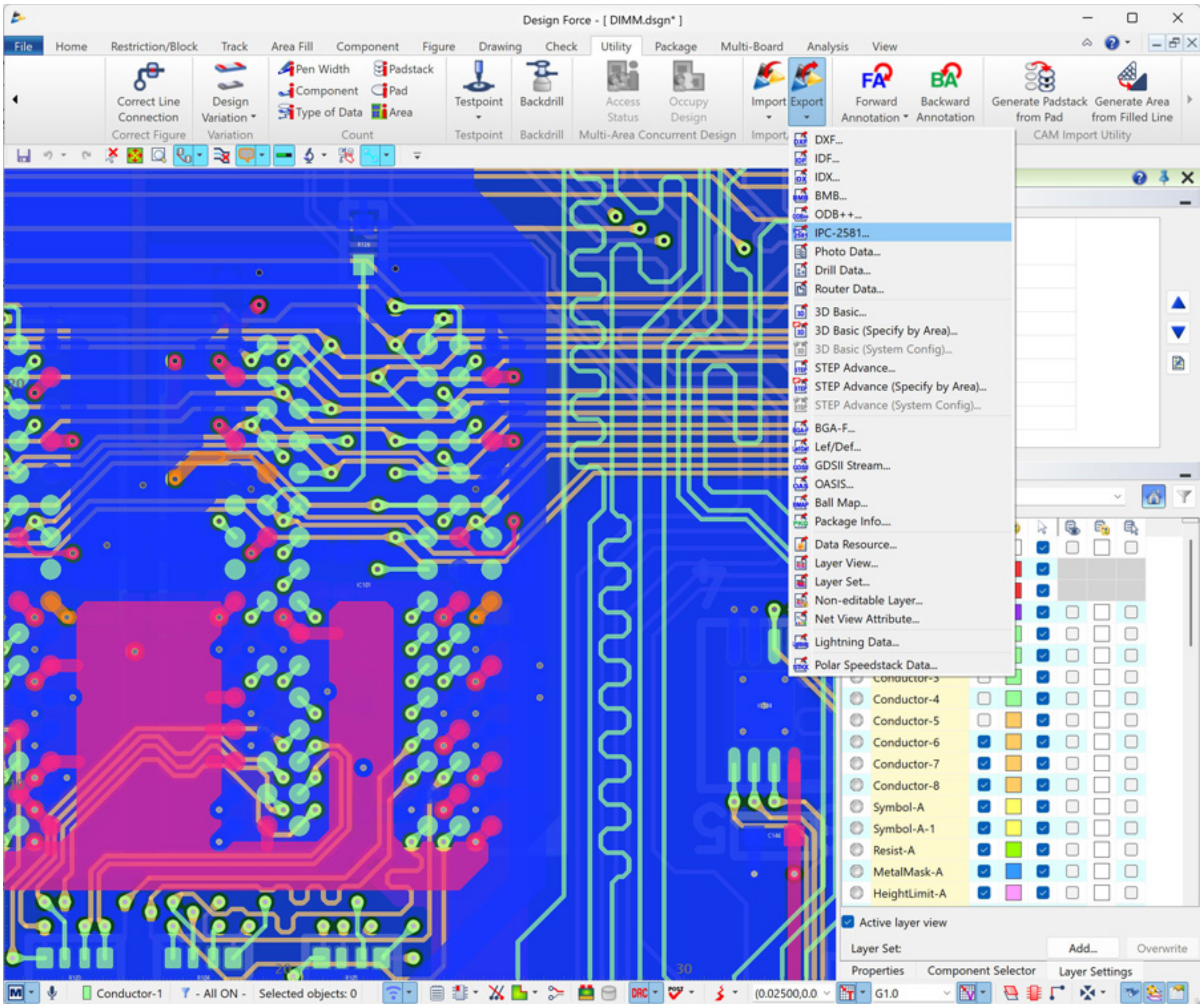


Figure 4. Creating an IPC-2581 file typically requires only a few configuration selections before generating a complete digital manufacturing dataset.

Most PCB design tools will ask for just a few additional choices:

- **Select the IPC-2581 revision.** Choose the version supported by your manufacturing partner. Today, most fabricators and assemblers support IPC-2581B or C.
- **Select what to export.** This is where IPC-2581 stands apart. Unlike traditional manufacturing packages, it does not require every dataset to be shared. Available export options include fabrication data only (excluding component information), assembly data only (excluding innerlayer artwork) and stencil, DfX, stackup or other purpose-specific datasets. Many companies use this capability to protect valuable intellectual property by sharing only the information each manufacturing partner needs.
- **Choose a filename and generate the file.**

That's it.

After the file is exported, it can be reviewed directly in many PCB design tools that support IPC-2581 import and visualization. For tools without native support, free IPC-2581 viewers are available from providers including Wise

Software, Siemens, ZofzPCB and PCB Preflight. Download links for these viewers can be found on the IPC-2581 Consortium website under Resources → Free Viewers.

Spend a few minutes exploring what is inside the file. Compare it with the collection of Gerbers, drill files, spreadsheets, PDFs and notes normally sent to manufacturing. The contrast between fragmented manufacturing packages and an intelligent digital product model quickly becomes apparent.

The hardest part of adopting IPC-2581 isn't learning how to generate it. It's deciding that it's time to move beyond a workflow we've outgrown.

The tools are ready. The ecosystem is ready. The standard is mature.

The only question left is whether we're ready to let go of yesterday's habits and embrace a smarter, more secure and collaborative way of exchanging manufacturing data. You can reach out to the IPC-2581 Consortium if you have any questions – just fire off an email to info@ipc2581.com. What are you waiting for?

HEMANT SHAH is an EDA veteran and chair of the IPC-2581 Consortium (ipc2581.com). Shah led the effort to create an industry-wide consortium of design and supply chain companies to get IPC-2581 – the standard for transferring PCB design data to manufacturing – adopted.

He spent 20 years at Cadence as product manager for various PCB design products. Shah also led the industry adoption of the IBIS-AMI algorithmic modeling standard. Prior to joining Cadence, Shah worked at Xynetix and Intergraph. He is passionate about developing and marketing leading-edge software products for PCB design. The IPC-2581 Consortium is holding a free IPC-2581 Adoption Summit on Oct. 1, 2026, as part of PCB West.

BANDWIDTH **OPTIMIZATION**

Breaking the 100GHz Barrier with Ground Guard Sheets in mmWave PCB Design

Breaking through the 100GHz bandwidth limit for coplanar waveguide design with a ground guard sheet in mmWave applications.

by CHANG FEI YEE

Millimeter wave (mmWave), or millimeter band, is an electromagnetic (EM) frequency range below infrared (IR). The frequency spectrum of mmWave is applied for high-speed telecommunications, such as 5G and potentially 6G network deployment.[1,2] Referring to **Figure 1**, the mmWave wavelength ranges from 10mm at 30GHz to 1mm at 300GHz.

Wireless communication in the mmWave band is fast and low-latency, enabling higher data rates than other telecommunications in lower-frequency bands, such as existing cellular networks. With its higher data rate and capacity, the mmWave network handles more data traffic than other frequency bands. Furthermore, mmWave does not propagate or interfere with the neighboring cellular network system.

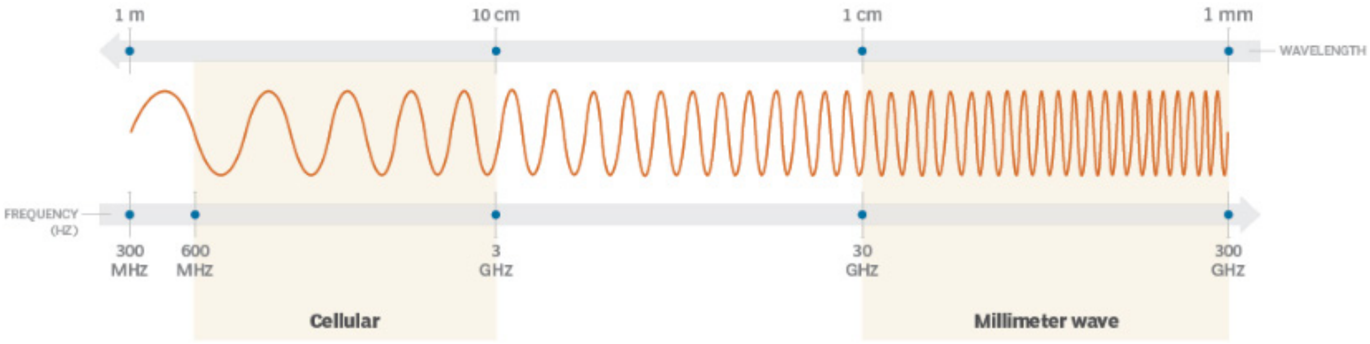


Figure 1. Frequency spectrum and wavelength of mmWave versus cellular.

To minimize transmission line loss in the PCB used in the mmWave application, stringent signal trace routing is required. To align with this aim, this paper presents an optimization study of the coplanar waveguide (CPW) structure in terms of transmission-line design to achieve minimal loss and a resonant dip across a bandwidth beyond 100GHz.

The work detailed here involves two phases, i.e., three-dimensional electromagnetic (3DEM) modeling of the CPW transmission line using Keysight EMPro in phase one, followed by analyzing the insertion loss (S21) and time domain reflectometry (TDR) using Keysight Advanced Design System in phase two to compare the loss performance between

CPW design with ground guard sheet versus conventional guard vias.

Analysis and Results

Loss performance analysis for CPW with conventional guard vias. The CPW 3DEM models with guard vias are constructed in EMPro, and the top view is shown in **Figure 2**. The signal trace and its side ground planes on layer one have a 1oz. thickness, a 7mil trace width, and a 4mil gap (edge-to-edge on each side), laid 4mil above a solid ground plane on layer two, with the Megtron 6 dielectric laminated between the two copper layers. The CPW structure is 500mil long. The nominal characteristic impedance of the signal trace is 50Ω, calculated based on the six equations shown in **Figure 3**.[3] There is a row of guard vias on each side of the signal trace, connecting the ground planes on layers one and two. Each via's diameter is 10mil. Ports 1 and 2 are positioned at each end of the signal trace.

The parameters Dx (spacing between two vias, center to center) and Dy (spacing between via and trace, center to center) are varied for four microstrip models to investigate the guard via position impact on the transmission loss performance of CPW, i.e., model A1 is set with Dx 15mil and Dy 30mil, model A2 is set with Dx 15mil and Dy 60mil, model B1 is set with Dx 30mil and Dy 15mil, model B2 is set with Dx 60mil and Dy 15mil.

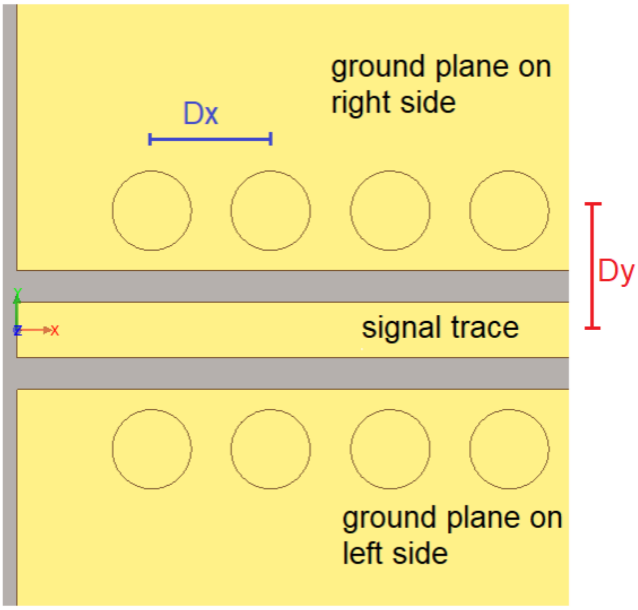


Figure 2. Top view of CPW 3DEM models in EMPro.

$$Zo = \frac{60.0\,\pi}{\sqrt{\varepsilon_{eff}}}\;\frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k1)}{K(k1')}} \qquad \text{(Eq. 1)}$$

$$k = \frac{a}{b} \qquad \text{(Eq. 2)}$$

$$k' = \sqrt{1.0 - k^2} \qquad \text{(Eq. 3)}$$

$$k1' = \sqrt{1.0 - k1^2} \qquad \text{(Eq. 4)}$$

$$k1 = \frac{\tanh\left(\frac{\pi\,a}{4.0\,h}\right)}{\tanh\left(\frac{\pi\,b}{4.0\,h}\right)} \qquad \text{(Eq. 5)}$$

$$\varepsilon_{eff} = \frac{1.0 + \varepsilon_r\,\frac{K(k')}{K(k)}\,\frac{K(k1)}{K(k1')}}{1.0 + \frac{K(k')}{K(k)}\,\frac{K(k1)}{K(k1')}} \qquad \text{(Eq. 6)}$$

Where

Zo = signal trace characteristic impedance

K() = elliptic integral

a = trace width

b = sum of trace width and gaps on either side

h = laminate thickness

Ɛr = dielectric constant

Ɛeff = effective dielectric constant.

Figure 3. Equations used to calculate characteristic impedance and effective dielectric constant for coplanar waveguide structures.

The resulting plots of S21, TDR and electric field with varied parameter Dy are depicted in **Figure 4** and **Figure 5**, respectively. Referring to Figure 4, CPW model A1 with Dy 30mil and A2 with Dy 60mil encounter a resonant dip at 73GHz and 32GHz, respectively. Based on Eq. 7,[4] the quarter wavelength at frequency 7 GHz and 32GHz on PCB laminated with Megtron 6 is 21.6mil and 49.3mil, respectively.

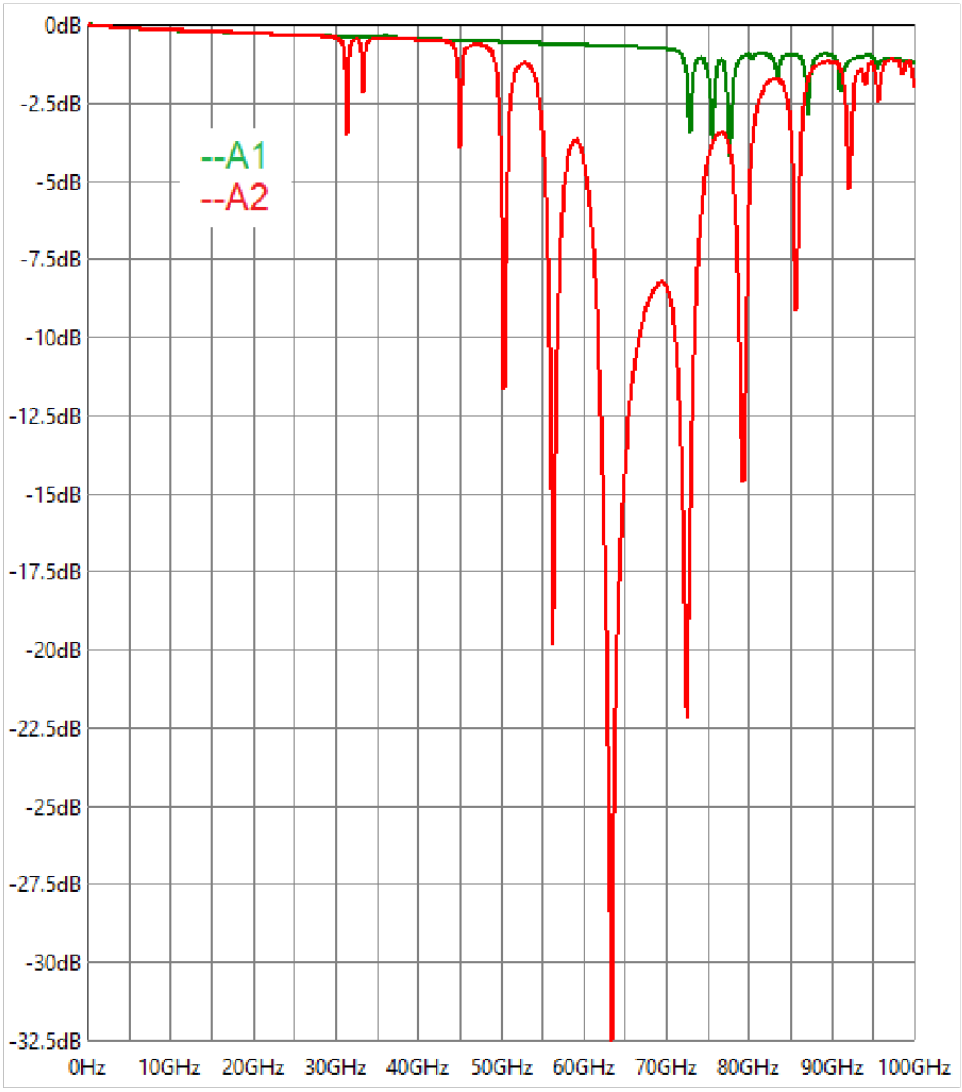


Figure 4. S21 plot for CPW models with varied Dy.

$$\lambda = \frac{c}{f\ \mathrm{x}\ \mathrm{sqrt}(\mathcal{E}r)}$$

Where

λ = signal wavelength

c = speed of light

f = signal frequency

$\mathcal{E}r$ = dielectric constant.

Eq. 7

On the other hand, referring to the TDR plot in Figure 5, CPW model A1 faces a slight impedance fluctuation, and model A2 suffers a larger fluctuation due to dielectric dispersion.

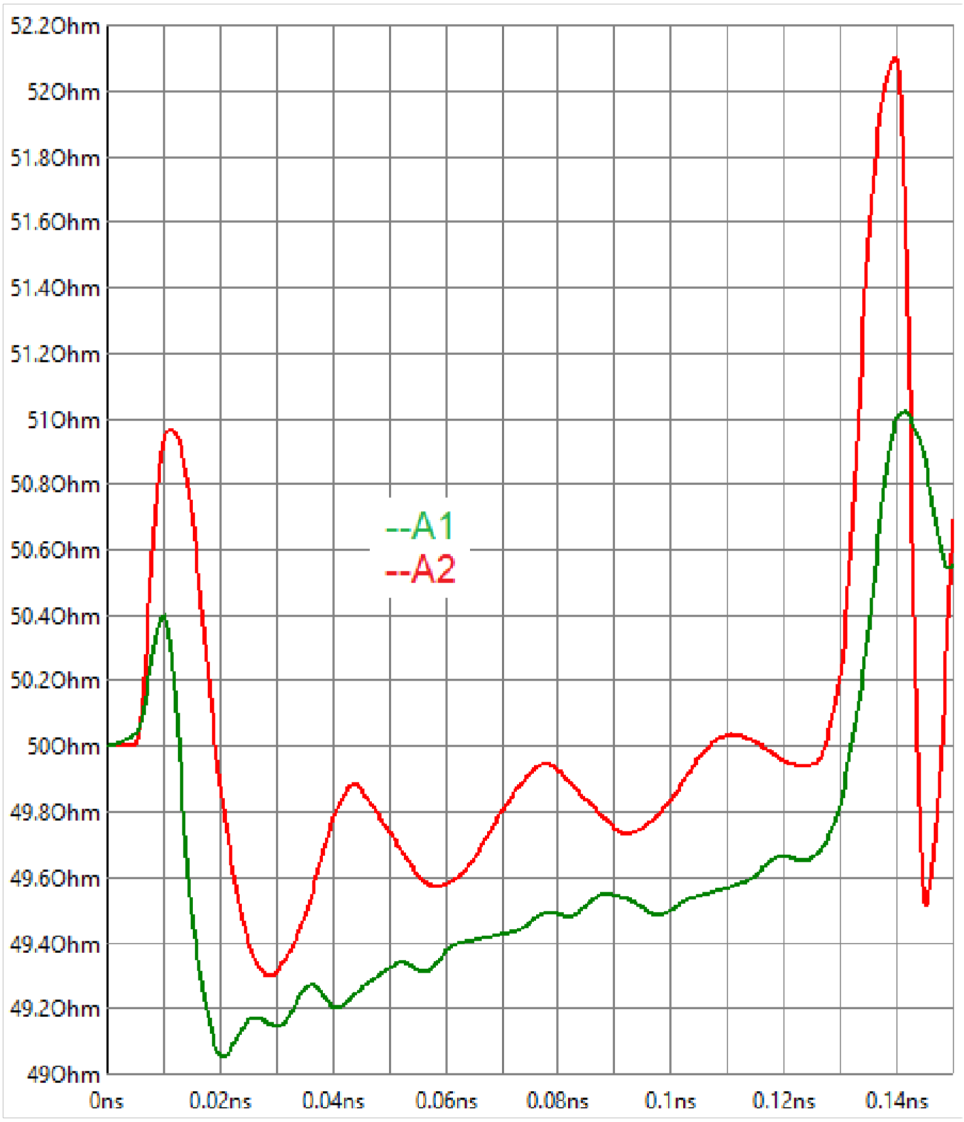


Figure 5. TDR plot for CPW models with varied Dy.

Meanwhile, **Figure 6** shows that the electric field is more localized around the transmission line for CPW model A1, compared to A2.

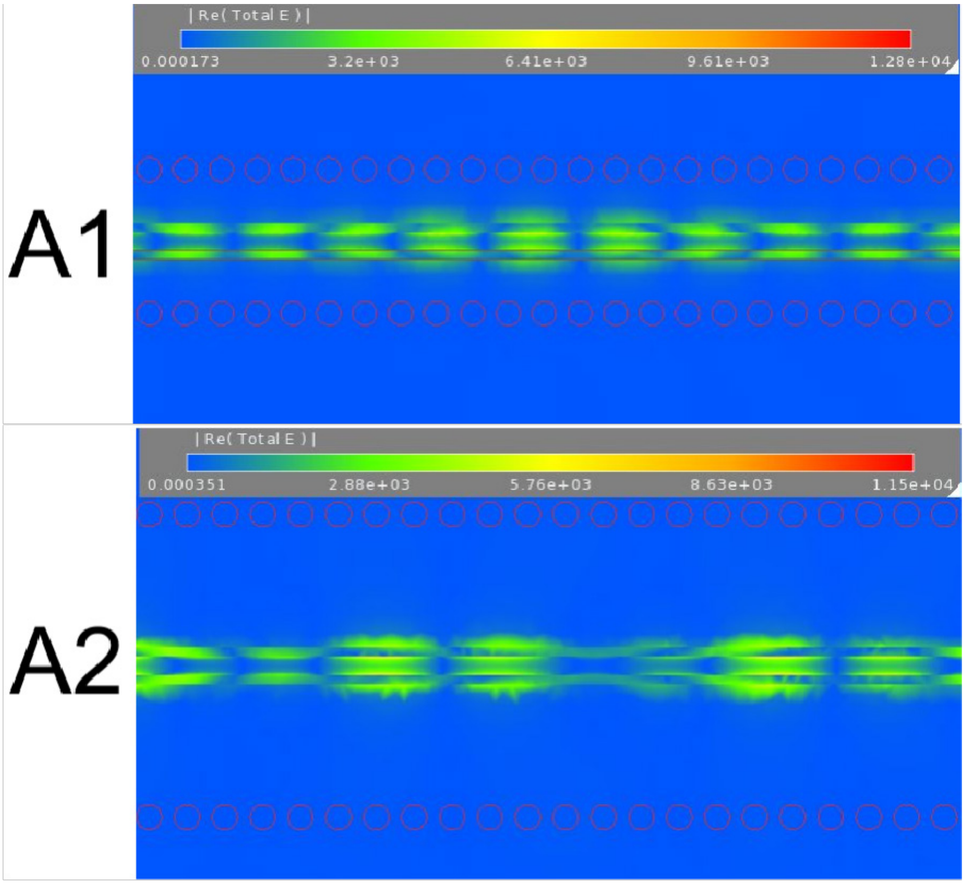


Figure 6. Electric field plot for CPW models with varied Dy.

The signal transmission line also serves as an electromagnetic radiation source that emits an electromagnetic wave outward, with approximately a quarter wavelength. Besides that, the electric field is more localized in CPW with more closely positioned guard vias, or vias' center to center spacing below quarter wavelength, which helps minimize the electric field radiation, spurious coupling, and dielectric dispersion, which in turn mitigates impedance fluctuation and insertion loss.[6,7]

Subsequently, the resulting plots of S21, TDR, and electric field for varying Dx are depicted in **Figure 7**, **Figure 8** and **Figure 9**, respectively. Referring to Figure 7, CPW model B1 with Dx 30mil and B2 with Dx 60mil encounter a resonant dip at 76GHz and 32GHz, respectively. Based on Eq. 7,[4] the quarter wavelength at frequency 76GHz and 32GHz on PCB laminated with Megtron 6 is 20.75mil, 49.3mil, respectively.

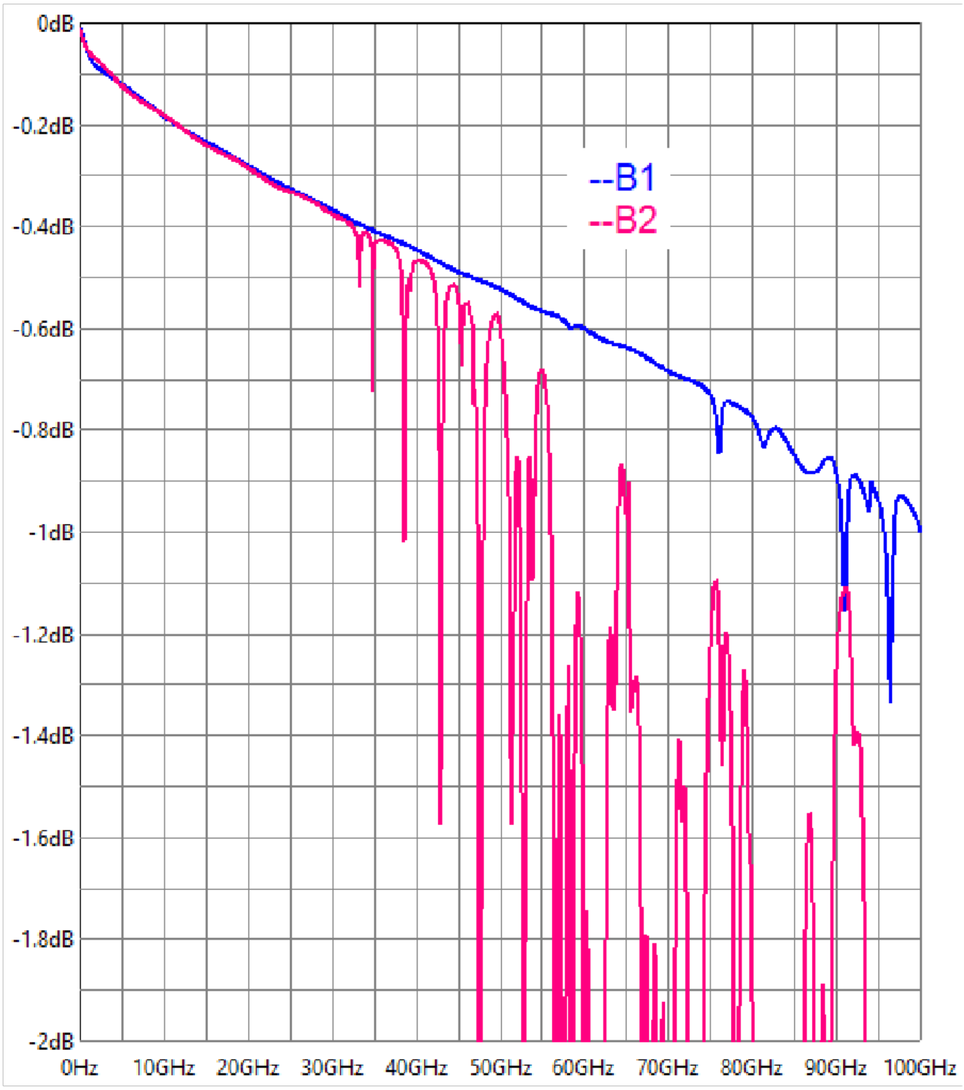


Figure 7. S21 plot for CPW models with varied Dx.

On the other hand, referring to the TDR plot in Figure 8, CPW model B2 exhibits greater impedance fluctuations than model B1 due to more severe dielectric dispersion.

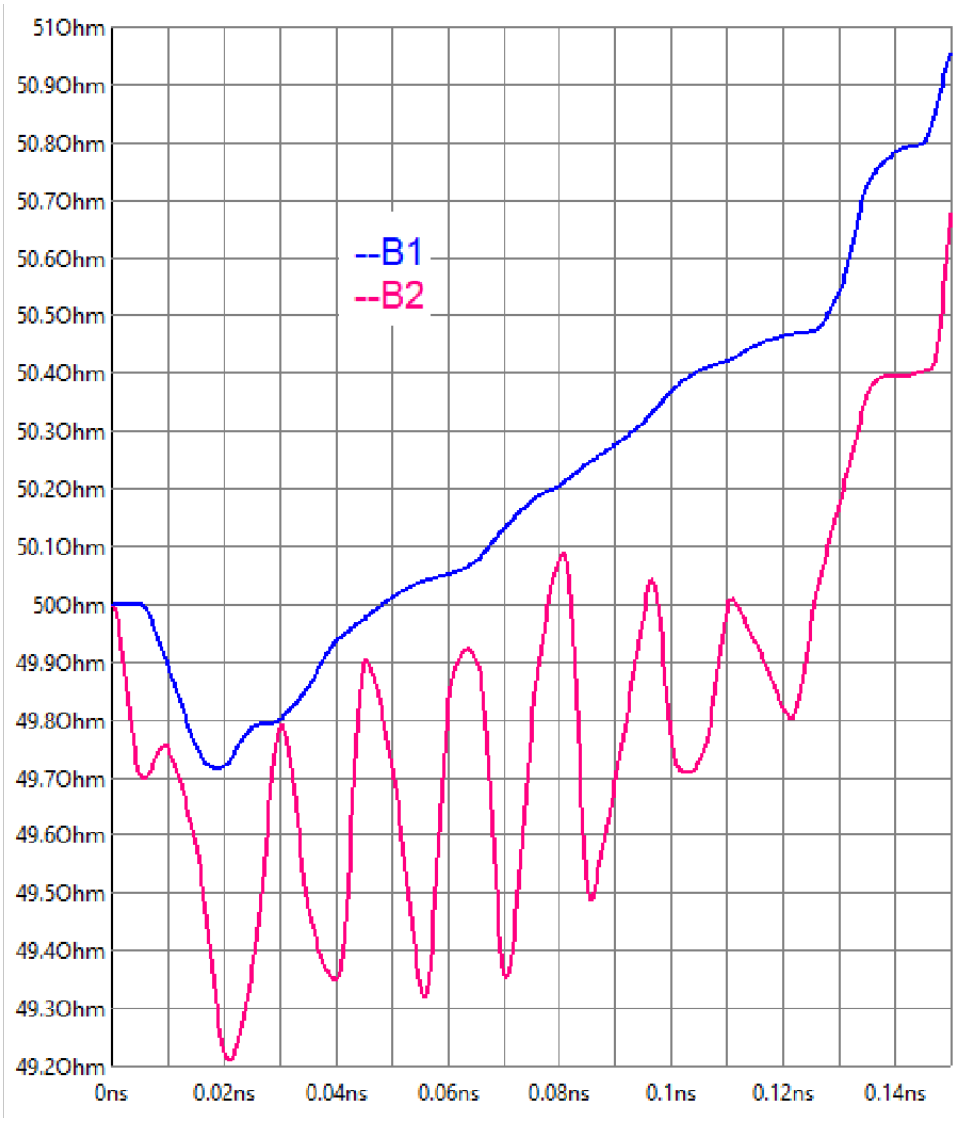


Figure 8. TDR plot for CPW models with varied Dx.

Meanwhile, **Figure 10** shows that the electric field is more localized around the transmission line in CPW model B1 than in B2. As a result, model B2 suffers from more critical dielectric dispersion and impedance fluctuation.

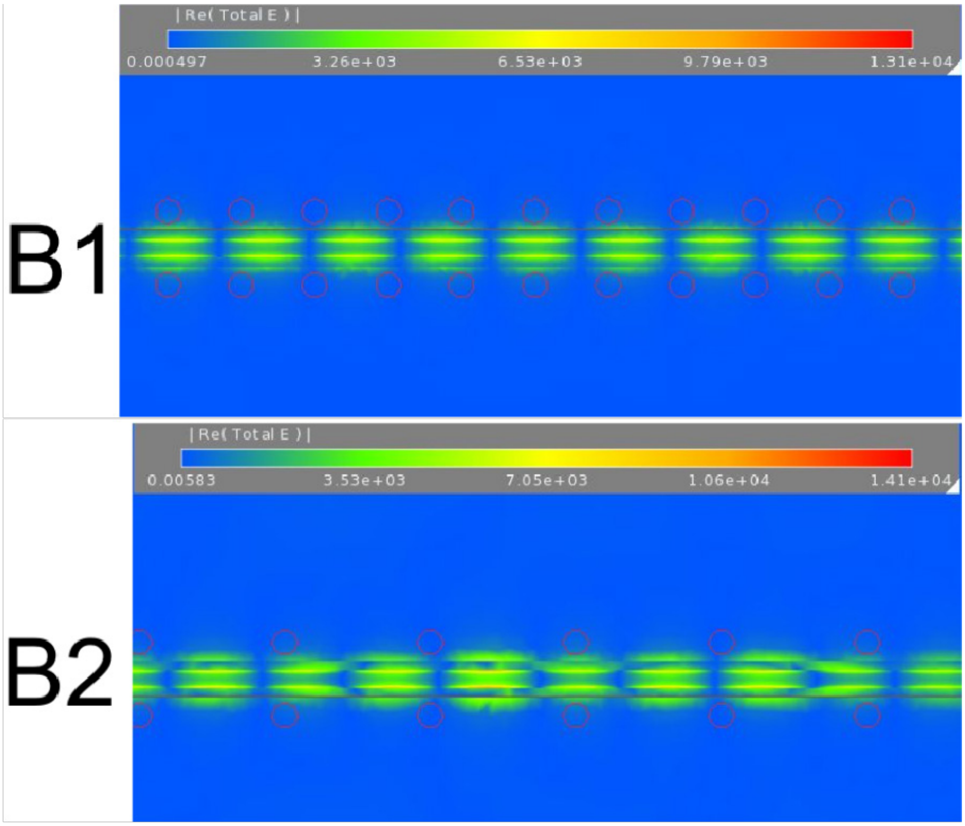


Figure 9. Electric field plot for CPW models with varied Dx.

Loss performance analysis for CPW with ground guard sheet. The 3DEM Model C uses the same PCB stackup and physical constraints as the other four models but replaces the guard vias with 1mil thick guard sheets positioned on either side of the signal trace. The guard sheets connect the ground planes on layers 1 and 2 and extend 500mils along the transmission line. The electric field distribution, TDR response and S21 performance of the guard-sheet design were analyzed and compared with those of a conventional CPW using guard vias.

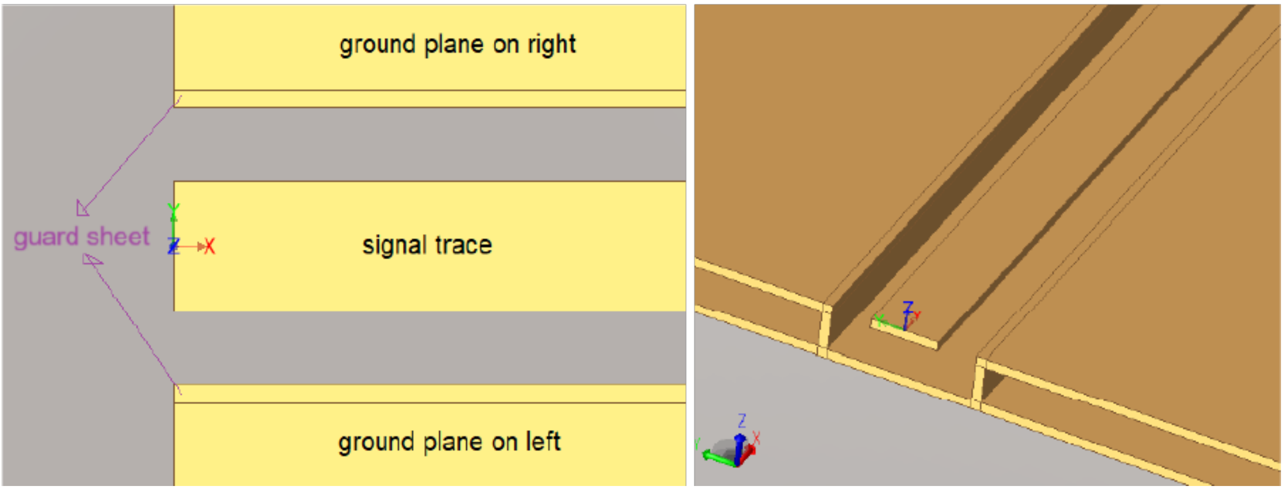


Figure 10. Top view (left) and 3-D view (right) of CPW model C.

Referring to E-field, TDR, and S21 plots in **Figure 11**, **Figure 12** and **Figure 13**, respectively, the E-field experienced by CPW model C with guard sheet is more localized around the transmission line vs. CPW models A1, A2, B1 and B2. The E-field hardly radiates through the solid guard sheet. As a result, dielectric dispersion is less severe, which in turn contributes to a more stable, smoother impedance profile around the nominal 50Ω level. Ultimately, CPW model C can experience a smooth S21 curve, without a significant resonant dip, up to 170GHz. Its S21 of –1.6dB at 170GHz is caused by Megtron 6 dielectric attenuation.

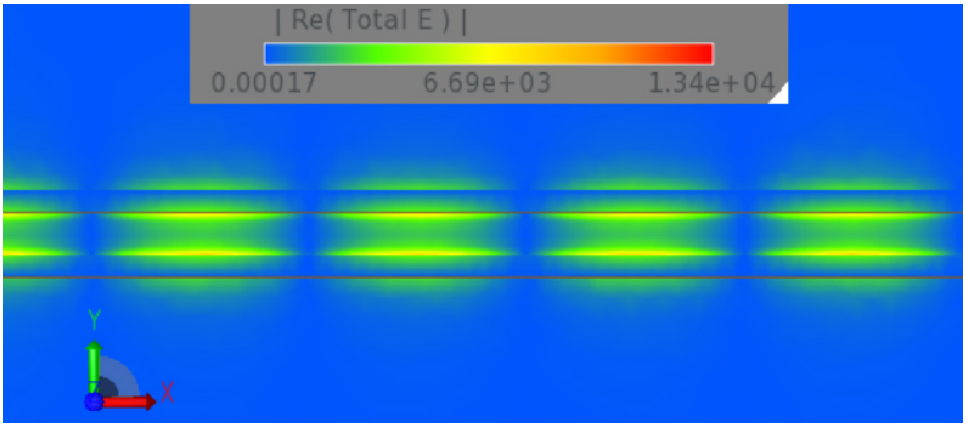


Figure 11. E-field profile for CPW model C.

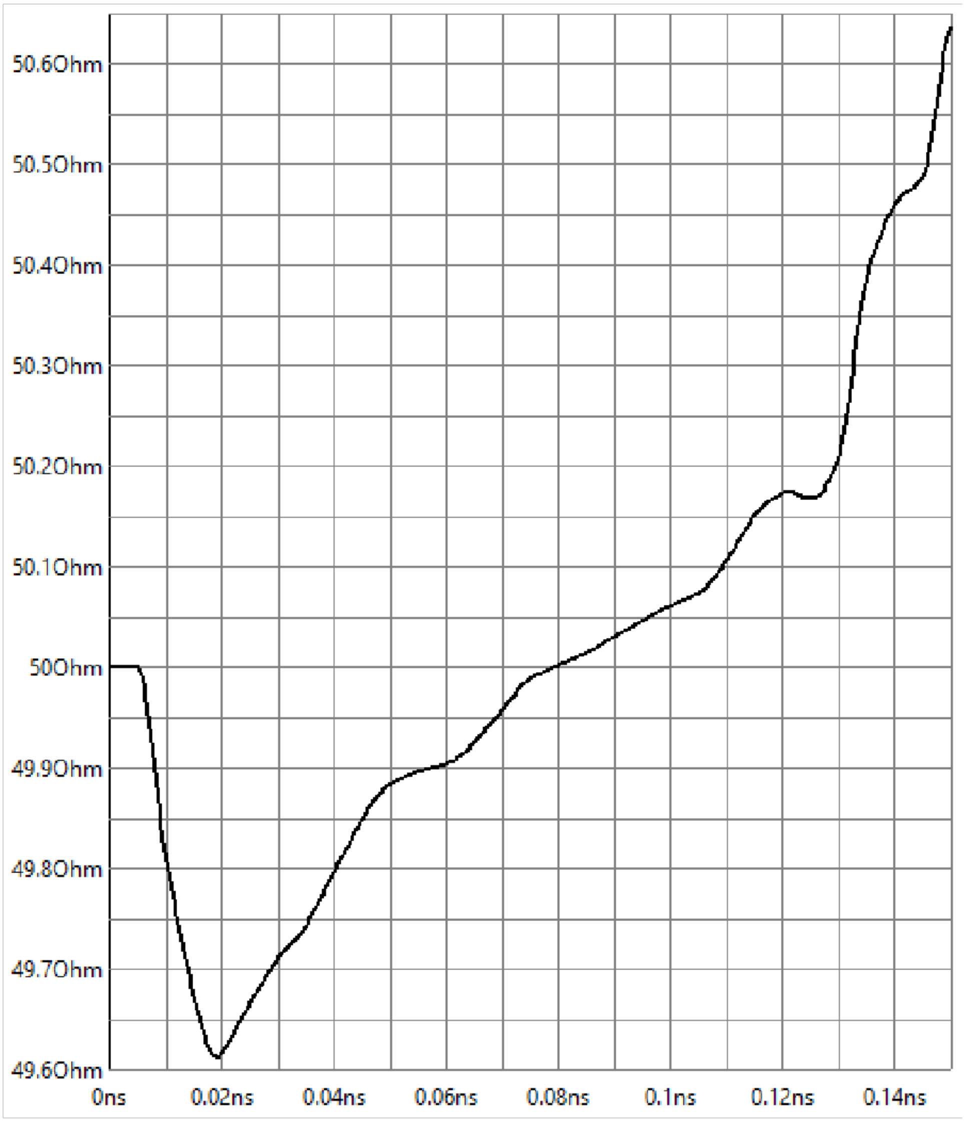


Figure 12. TDR plot for CPW model C.

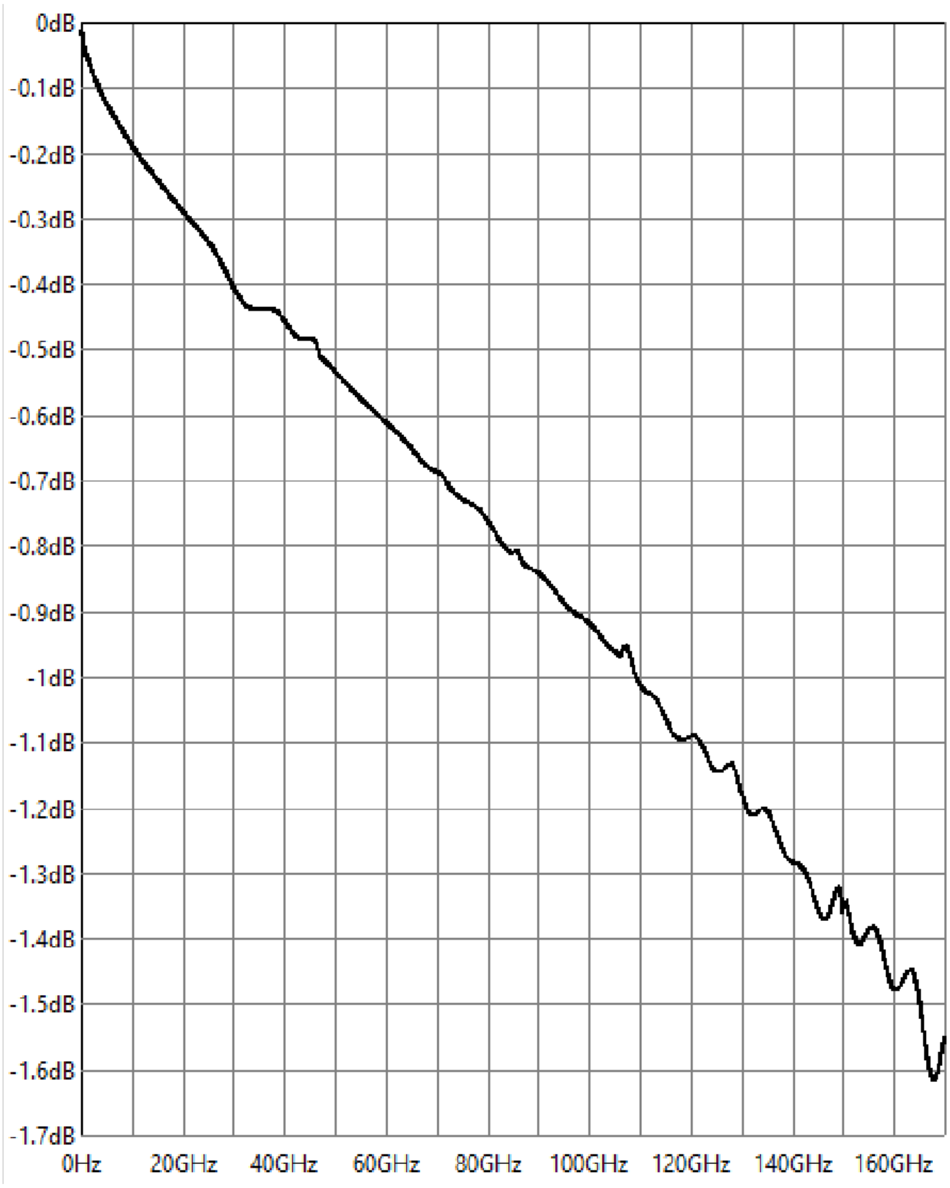


Figure 13. S21 plot for CPW model C with ground guard sheet.

Based on Eq. 7, 170GHz signal bandwidth and beyond has a quarter wavelength below 9mil. The standard PCB capability can only be achieved via a pad diameter as small as 15mil,[8] which means that the via center-to-center distance is at least 15mil. Even the advanced PCB capability can only fabricate a board with a via pad diameter as tiny as 10 mil and hence a center-to-center spacing of 10 mil minimum.[8] Therefore, the guard vias hardly impede the 170GHz E-field radiation and dielectric dispersion. On the contrary, the analysis results indicate that the solid guard sheet without any voids is an ideal alternative for hindering E-field radiation, dielectric dispersion, and resonant dip up to 170GHz. In practice, a ground guard sheet can be implemented on a PCB using 3-D printing[9] or PCB milling.[10]

Conclusion

This work provides an overview of the mmWave and frequency range used in 5G and 6G telecommunications. Besides that, this work also presents a study that alleviates transmission loss in CPW beyond 100GHz. Analysis results show that by substituting the conventional guard vias with a solid guard sheet for a CPW with 500mil length, the insertion loss is held below -1.7dB without a significant resonant dip up to 170GHz bandwidth.

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From Fab Note to Process Control: How to Validate PCB Backdrilling

How to specify, validate and monitor PCB backdrill requirements during NPI and production.

by JOE CLARK

As PCB designs incorporate higher-speed signals, and reducing via stubs becomes critical to function, backdrilling is often treated as a simple requirement added to the fabrication drawing. Designers trust the PCB fabricator's process to meet their stub requirement, but validation of this critical requirement is often overlooked.

The backdrill note in the fabrication drawing can be perfectly clear, but the fabricator may still fail to meet the stub length requirement. This will not appear at bareboard electrical tests, and it may show up later as margin loss, intermittent high-speed failures or unexplained channel performance variation. The fabricator's success in their backdrill operation depends on clear design requirements, stackup accuracy, layer registration, primary drill and backdrill registration and process repeatability. These factors can be validated in several ways: coupon inspection, first-article CT scan, time domain reflectometry (TDR) or destructive physical analysis (DPA).

Here are recommendations for high-speed backdrill requirements and validation methods to use with your PCB fabricator.

Specify the requirement. In my experience reviewing high-speed PCB designs for manufacturability, I have found inconsistencies in the way backdrill requirements are specified. I've seen long, detailed fabrication notes, backdrill tables with conflicting requirements or simply backdrill layers without any stub length tolerance specified. For the PCB fabricator to be successful, the fabrication drawing and data package must include the target backdrill stub length, tolerance, layer span and the must-not-cut (MNC) layer for each backdrill.

Listing the backdrill size is optional, since allowing the PCB fabricator to choose the backdrill drill bit size allows them to optimize the bit when compared to the primary drill size and surrounding copper features or anti-pads. Avoid using maximum backdrill depth as part of the acceptance requirements, as it may conflict with the stub length and MNC layer requirements once the fabricator models the stackup.

The electrical intent with backdrilling is to maintain residual stub length and avoid drill damage to the MNC layer. The fabricator will translate these requirements into their own drill depth targets. I also suggest referencing the applicable revision of IPC-6012, *Qualification and Performance Specification for Rigid Printed Boards*, as part of the general PCB acceptance criteria since IPC-6012 includes microsectioning requirements for backdrilled holes.

An example of a backdrill requirement might look like this:

Table 1. Backdrill Requirements by Layer Span

Layer Span	Backdrill Size[1]	Stub Length	Tolerance	MNC layer
L40-9	16mil	7mil	+/- 5mil	8
L20-9	12mil	4mil	+/- 2mil	8

[1] Backdrill diameter may be modified by the PCB fabricator with customer approval, provided the change remains within approved antipad, spacing and adjacent-copper clearance limits.

Design factors that affect process capability. Stackup design affects the success of the backdrill operation. The backdrill operation must account for a laminated panel larger than the resulting PCB with tolerances for dielectric thickness, copper distribution, resin flow and primary drill registration. As the stub length tolerances decrease, the fabricator's control of each of these tolerances matters. With a balanced single-lamination design, some advanced fabricators may be able to demonstrate very tight residual stub control, even as low as 4+/-2mils. But this target is quite difficult to meet if the stackup is unbalanced, the backdrill depth exceeds standard capability, or multiple laminations are involved.

Process artifacts like floating copper or copper stripes may appear in the backdrill section of the hole. See **Figure 4** for an example of a copper stripe. These artifacts may cause the same issues as a residual stub over the target. Fabricators need to incorporate specialized processes to achieve such tight tolerances, such as layer mapping or drill mapping. Specialized equipment may map the thickness across a panel, measure the MNC layer depth after the primary drill, or electrically sense a target layer with features in a non-plated hole.

When determining the stub length target, don't just choose the best stub length that the fabricator can achieve. Choose the stub length target based on the design speed. A rule of thumb for Intel Xeon reference platforms was that PCIe Gen 5 used 7+/-5mils, PCIe Gen 6 used 6+/-4mils, and PCIe Gen 7 would use 4+/-2mils. Keep the same requirement across a layer span for consistency in the fabricator's process, so in a multi-lamination stackup, a through-hole may use a 7+/-5mils requirement while the sub-lamination blind vias may use a 4+/-2mils requirement.

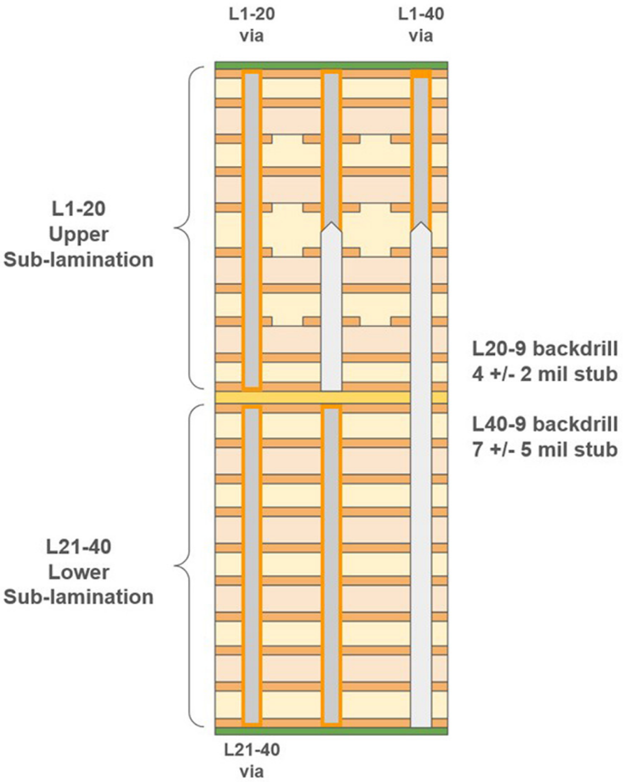


Figure 1. Example of multilamination stackup showing separate backdrill requirements for through-hole and sub-lamination vias.

Validate the result. With the requirements set, the next challenge is validating that the fabricator has achieved the target. There are some steps a fabricator will take on their own to verify their process against the acceptance criteria. The fabricator may design coupons that reflect the backdrill area padstacks to physically measure a microsection for the backdrill stub. This coupon stub length should be correlated to the PCB design's stub length by performing a DPA on a failed or sample board from the lot.

The fabricator may use automated x-ray inspection to verify registration between the primary and backdrill holes, with a CT scan for any nonconforming results or for first-article testing when available. I've seen newer equipment that uses TDR to identify via-stub reflections and correlate the response with residual stub length, but I have yet to see this used in production environments. Don't expect that insertion loss coupons, such as delta-L, characterize backdrill stub length; specialized test coupons or probes are required for this type of testing.

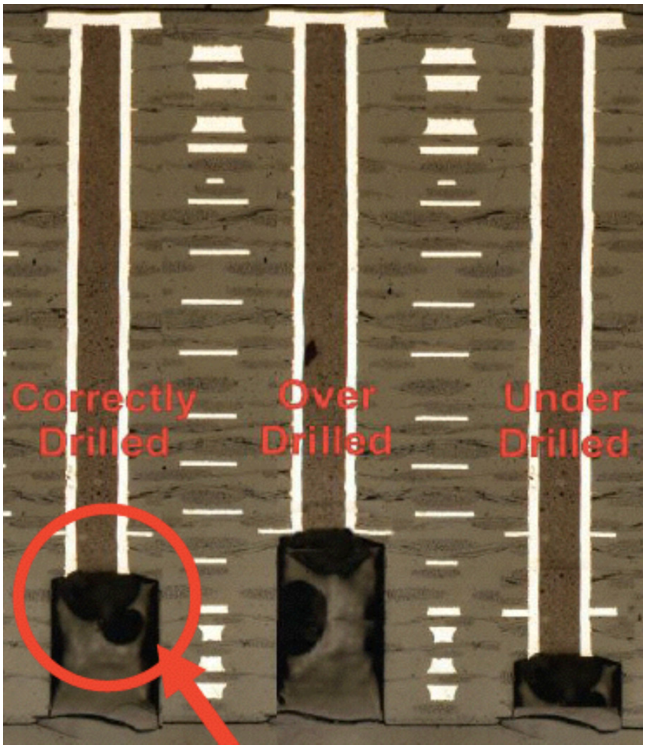
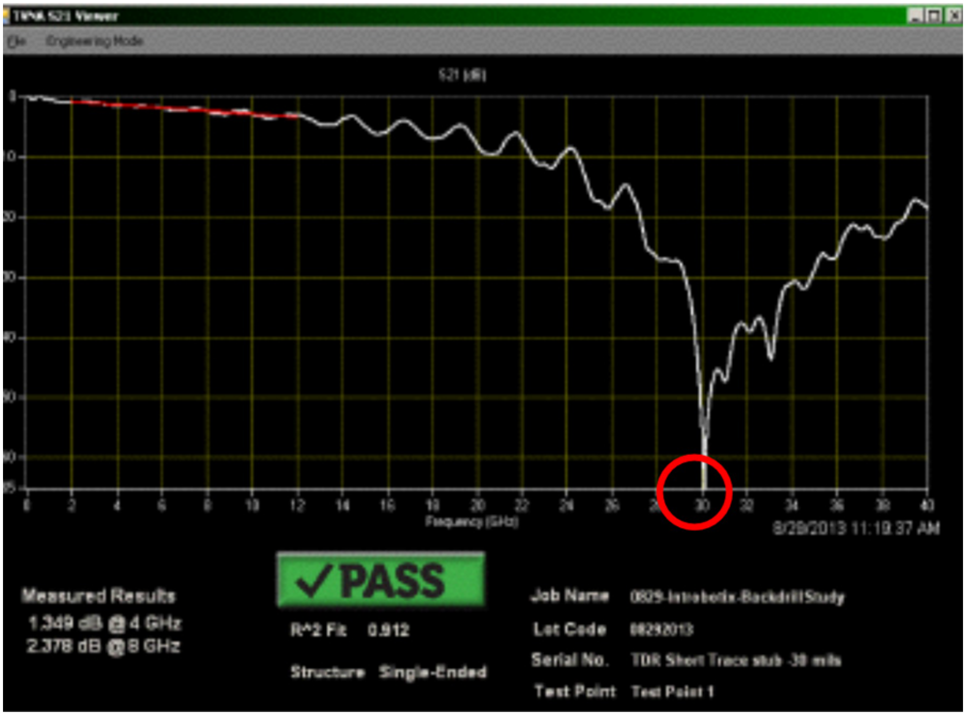


Figure 2. Backdrill microsection showing nominal, over-drilled and under-drilled conditions.



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Measured Results
1.349 dB @ 4 GHz
2.378 dB @ 8 GHz

R^2 Fit 0.912

Structure Single-Ended

Job Name 0829-Introbotix-BackdrillStudy
Lot Code 08292013
Serial No. TDR Short Trace stub -30 mils
Test Point Test Point 1

Figure 3. TDR measurement showing backdrill stub reflection.

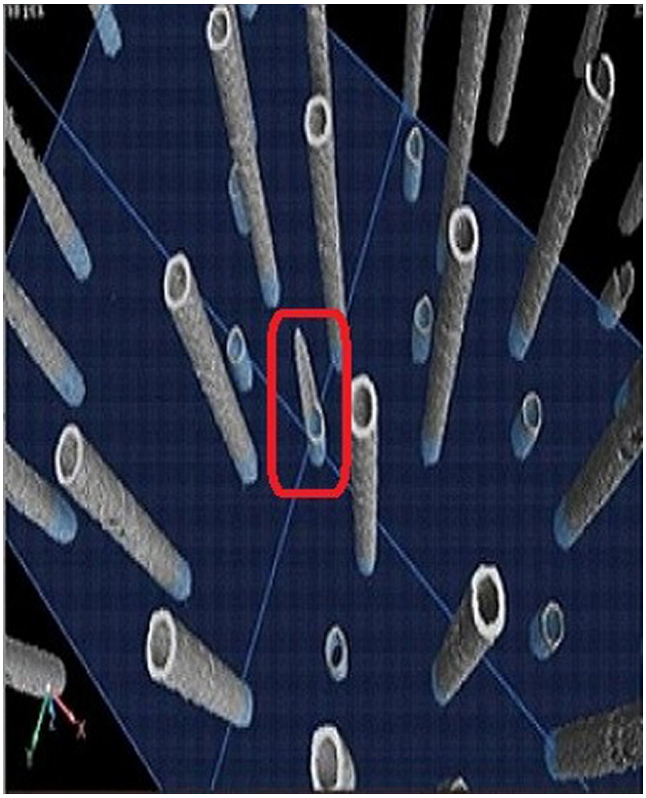

Figure 4. CT scan showing backdrill stripe.

Table 2. Backdrill Validation Tools, Applications and Limitations

Method	What it validates	Best use	Limitation
Backdrill coupon microsection	Residual stub on representative coupon	Routine lot or NPI evidence	Coupon may not fully represent product geometry
Product DPA	Actual board stub length	NPI correlation or failure analysis	Destructive and sample-limited
X-ray / CT	Drill registration, depth features, anomalies	First article or high-risk builds	Cost, resolution, and availability vary
TDR / reflection method	Electrical signature of residual stub	High-speed validation or correlation	Availability varies, Requires interpretation and correlation
Insertion-loss / Delta-L coupon	Channel loss impact	Electrical performance monitoring	Does not directly measure backdrill residual stub length

What to ask the fabricator. How should the implementation of these process checks be monitored? The most important step is direct communication with the PCB fabricator. Design feedback should be requested on copper balancing within the stackup, where the backdrill stub is critical to function. A clear understanding should be established regarding the process controls the fabricator will implement to meet the specified requirement and whether any capacity limitations may affect production volumes.

During NPI, measured evidence should be provided that correlates coupon results to product DPA. At minimum, the data should include the measurement method, sample size, measured stub lengths, mean, range and variation relative to the specified tolerance. For high-risk designs, requirements should define whether a 3σ or Cpk-based process capability target is necessary.

Backdrill stub lengths should be spot-checked on any material or failure analysis performed by the PCBA contract manufacturer. Product functionality should be monitored during NPI testing for issues that may be attributed to PCB stub lengths. Changes to the design or stackup that would require process revalidation should be identified in advance.

Finally, the need for a sampling plan during high-volume manufacturing should be determined based on the fabricator's demonstrated process capability.

Treat Backdrill as a Controlled Process

Backdrilling is not just a fabrication requirement; it is also a manufacturing process to be validated. A good backdrill fabrication note defines the stub length target, tolerance, and must-not-cut layer, and gives the fabricator the right information to control their process. A good NPI plan will verify that the fabricator's process meets the design requirement. Work with the PCB fabricator to implement the right design requirements, design feedback, process controls and sampling plans.

JOE CLARK is senior principal NPI engineer at SambaNova with 10+ years of experience across OpenAI, Intel and Lockheed Martin.

Selective UHDI: Using Ultra HDI Where Needed, Not Everywhere

Applying UHDI only where density and performance demands require it can reduce layer counts, improve yields and lower costs without sacrificing electrical performance.

by **ANAYA VARDYA**

One of the most common assumptions PCB designers make when investigating ultra HDI (UHDI) technology is that every layer must be built with ultra-fine geometries using semi-additive processing (SAP) or modified semi-additive (mSAP) processing. In practice, most UHDI stackups are a combination of conventional layers and UHDI layers. This approach – call it selective UHDI – places UHDI layers exactly where they deliver the most benefit and lets conventional layers handle the rest, resulting in a mixed-process stackup.

Apply UHDI selectively, not to every layer. Selective UHDI is the practice of applying UHDI fabrication only to the layers that need it, rather than across the entire board. The result is a mixed-process stackup: a PCB architecture that combines UHDI layers, built using semi-additive processing (SAP) or modified semi-additive (mSAP) processing, with conventional subtractive layers in the same board. The mix here is one of fabrication processes, not dielectric materials, which sets it apart from the material hybrid stackup that combines laminates such as Rogers and FR-4.

The distinction between HDI and UHDI is based on the feature thresholds defined by the Naval Sea Systems Command (NAVSEA) Crane. High-density interconnect (HDI) is characterized by BGA pitches of 0.8 to 1mm, trace and space around 75µm (3mils), and microvias of 100µm (4mils) or greater. UHDI extends each of the following: BGA pitches of 0.5mm or less, trace and space of 65µm or less, microvias of 50 to 75µm (2 to 3mils), and impedance control within 3 to 5%.

Do all layers in a UHDI PCB need ultra-fine geometry? No.

Not every layer in a UHDI board requires ultra-fine geometry, and applying it where it isn't needed adds cost and process complexity without adding design value.

From a fabrication standpoint, UHDI processing carries tighter process windows than conventional subtractive layers. Every layer committed to those tighter windows is a layer where plating distribution, imaging accuracy, seed layer uniformity and registration all need to perform at a higher level. Applying UHDI only where needed improves yield, reduces costs and keeps the fabrication process stable.

Where UHDI layers should be placed in the PCB stackup. BGA breakout zones and dense signal regions need semi-additive geometry for smaller capture pads, tighter via structures and sub-65µm routing. Power planes, ground references and broader signal layers don't. Keeping conventional processing where it belongs leaves those layers stable and predictable. A 0.5mm pitch BGA, for example, may require UHDI routing on the outer build-up layers to escape cleanly, while inner layers handling power distribution remain entirely conventional. However, where VIPPO and copper-filled microvias are required on the outer layer, don't add the complexity of UHDI there; keep those structures below the outermost layer.

Impedance-sensitive nets in RF and high-speed regions are the other natural fit. The more consistent copper geometry and straighter sidewalls produced by semi-additive processing translate directly into tighter impedance control and more predictable electrical behavior, a benefit that applies even beyond fine-line features.

How should designers plan a selective UHDI stackup? Start early.

Selective UHDI planning works best when it starts early, before routing begins, not after the design is nearly complete.

Identify which areas of the board are actually driving the density or performance challenge. In most designs, that comes down to a specific region: fine-pitch BGA breakout, a dense RF section or a cluster of high-speed nets with tight impedance requirements. Those areas map to specific layers.

The question becomes: which layers can remain conventional without compromising the design intent? In many cases, the answer includes most of the stack. Routing away from dense breakout zones, the power delivery structure, and the reference planes rarely require anything beyond standard subtractive-layer capability.

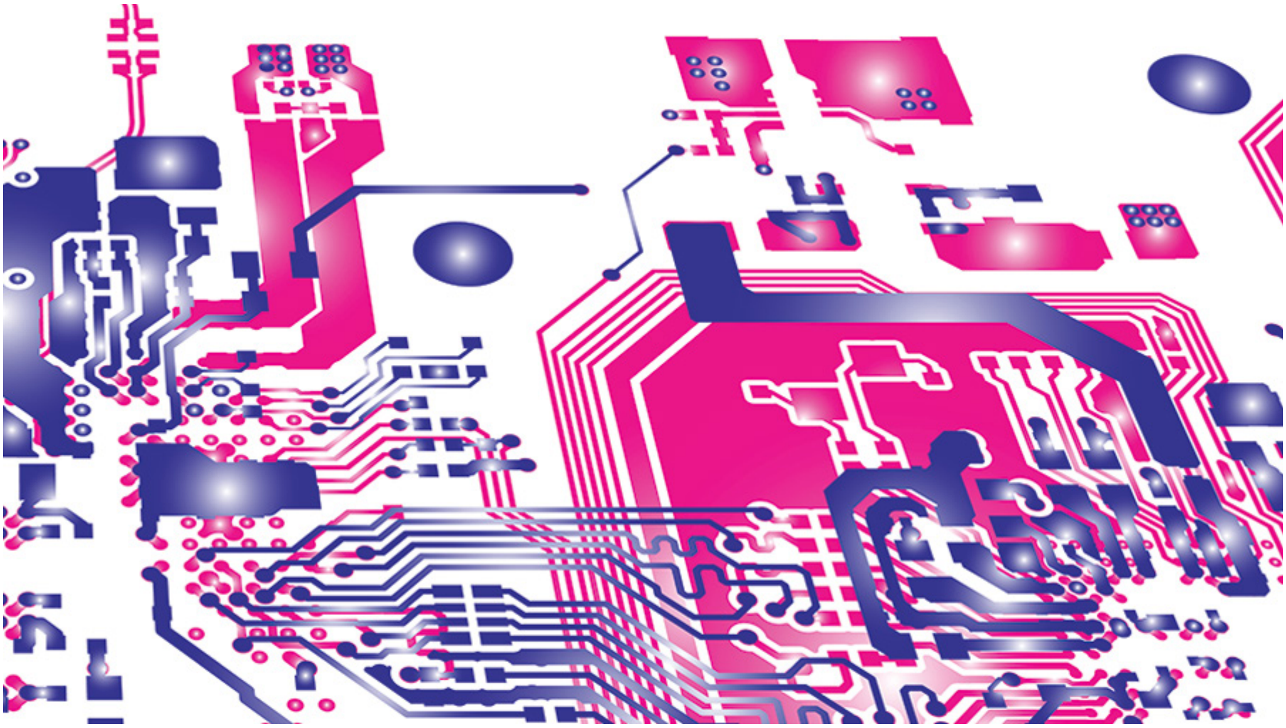

Figure 1. Selective UHDI applies ultra-fine geometries only where density and performance demands require them, while conventional layers handle power distribution and general routing.

Why should designers involve their fabricator early?

Fabricators who regularly produce mixed-process boards have worked through those variables and know which material combinations behave predictably together, where registration is most sensitive, and how to sequence the build to keep the process stable from start to finish. That accumulated knowledge does not appear on a capability chart, but it directly affects yield.

Early fabricator involvement results in a collaborative effort designed around a real process window. That alignment between design intent and fabrication reality is where yield improves, surprises decrease, and first-article builds run more smoothly.

Early fabricator engagement is also the right time to discuss opportunities for layer count reduction. UHDI's routing efficiency often enables the same electrical design to be achieved with fewer total layers than a conventional HDI approach would require. In a mixed-process build, that reduction can come from the UHDI layers opening routing channels that previously required additional conventional layers to resolve. The effect can be dramatic: escaping a 0.5mm pitch BGA with conventional 75µm routing can demand as many as 12 routing layers, while fine UHDI geometry can resolve the same escape in as few as two, collapsing layers that would otherwise exist only to break out a single dense component. Fewer layers mean fewer lamination cycles, with direct implications for reliability, weight and overall cost.

When selective UHDI make sense. Selective UHDI makes sense when one or more of the following conditions are present:

- BGA pitch is at or below 0.8mm, and escape routing is driving layer count up.
- Line and space requirements below 75µm are confined to specific board regions.
- RF or high-speed nets require tighter impedance control than conventional processing can reliably deliver.
- Miniaturization goals are pushing board size and layer count, but not every layer needs ultra-fine geometry.
- Cost and yield need to be balanced against routing density requirements.

Selective UHDI vs. Full UHDI: Which Do You Need?

The decision comes down to scope: how much of the board actually needs ultra-fine geometry? When only specific regions drive the density or performance challenge – a fine-pitch BGA breakout, a dense RF section or a cluster of high-speed nets – selective UHDI is the right fit: UHDI where it is needed, conventional layers everywhere else. A full UHDI build only makes sense when the entire board genuinely requires sub-65µm features throughout, which, in most designs, is not the case.

Does Selective UHDI Cost Less Than Full UHDI?

In most cases, yes. Every layer committed to UHDI processing carries tighter process windows and lower yield than a conventional subtractive layer, so confining UHDI to the layers that need it, rather than applying it across the whole board, lowers both cost and risk. A mixed-process build keeps the tightly controlled, higher-cost processing on the fine-pitch breakout, dense routing, and impedance-sensitive layers, while conventional layers handle power, ground and general routing at standard cost. The savings come from higher yield on those conventional layers and from the layer-count and lamination-cycle reductions that UHDI routing efficiency makes possible.

The question is never really "should we use UHDI?" The more useful question is "which layers actually need it?" Answer that thoughtfully, build the stackup around it, and the benefits of tighter routing, fewer layers and better electrical control follow naturally. The best designs have always been intentional ones. UHDI just raises the stakes.

Selective UHDI planning. Layer assignment should be driven by where the design challenge actually is, not by applying the smallest possible features everywhere.

UHDI layers belong around fine-pitch BGA breakout zones, dense signal regions and impedance-sensitive RF or high-speed nets. Conventional layers handle power distribution, ground references, and broader routing and perform better when they are not pushed into tighter process windows unnecessarily.

Clear communication in the data package about which layers are UHDI and which are conventional is one of the most avoidable sources of first-article delay. Fabricator involvement before the stackup is locked in is not optional; it is where mixed-process builds either come together cleanly or create problems that are expensive to unwind.

ANAYA VARDYA is CEO of American Standard Circuits and ASC Sunstone Circuits. ASC works closely with customers and design teams on advanced PCB technologies, including RF, HDI, rigid-flex and UHDI, with a focus on turning complex fabrication realities into practical design guidance.

POGO **ALIGNMENT**

SMT Pogo Pins Shifting (Post-Reflow)

A stencil aperture modification eliminated pogo pin tilt during reflow, maintaining alignment within customer specifications.

by AKBER ROY

Pogo pins are specialized, spring-loaded electrical connectors used to establish reliable temporary or permanent connections between electronic circuits. Comprised of a plunger, barrel and spring, they provide consistent contact force – typically around 1 Newton –ensuring stability against vibration and accommodating thermal expansion in compact devices.

A post-solder reflow inspection revealed SMT pogo pins with angular shifts exceeding the customer's allowable tolerance of ±0.1° from the required 90° orientation.

Figure 1. SMT pogo pins after reflow soldering, showing angular displacement beyond the customer's ±0.1° tolerance from the required 90° orientation.

Pogo pins are mounted perpendicular to the PCB surface to ensure maximum structural integrity, reliable electrical contact and even spring compression over thousands of repetitive cycles. Strictly perpendicular mounting prevents the plunger from binding or bending within the barrel, which can lead to premature failure or intermittent connectivity.

They are typically mounted perpendicular to the PCB because their performance and reliability depend on axial compression. When the pin is compressed directly along its centerline, the internal spring operates as intended, providing consistent contact force and minimizing wear. Mounting the pin at an angle can introduce side-loading, causing the plunger to scrape against the barrel, increasing friction and reducing service life.

Maintaining perpendicularity also helps prevent plunger binding. During mating, an angled pin can place uneven stress on the internal spring, increasing the likelihood that the spring will buckle or that the plunger will become stuck in a compressed position. Vertical alignment ensures that spring force is transferred directly to the target pad, providing stable, low-resistance electrical contact and supporting the high cycle counts for which pogo pins are designed.

In applications that use arrays of pogo pins, such as test fixtures, perpendicular mounting is particularly important because even a single misaligned pin can affect overall alignment, resulting in uneven contact pressure and unreliable connections.

Vertical placement also improves manufacturing stability during surface mount assembly, as properly aligned pins are less likely to shift during reflow soldering, reducing the risk of defects such as poor solder joints or electrical shorts.

The root cause was excessive solder paste volume on certain SMT pads. During reflow, the excess solder created enough lift to raise and tilt some of the pogo pins, resulting in angular shifts that exceeded the specified tolerance. Analysis showed that the issue was not related to component placement accuracy, but rather to the amount of solder deposited beneath the pins.

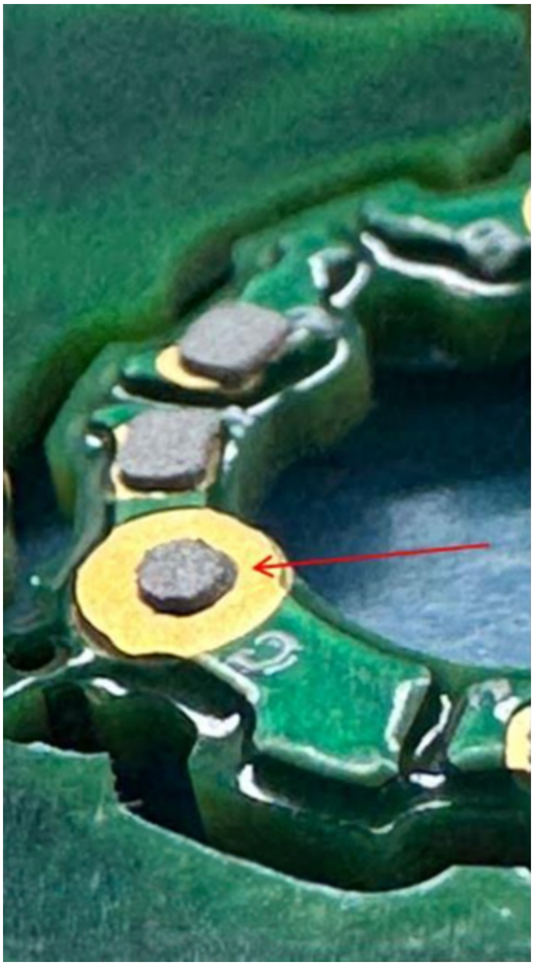

Figure 2. Excess solder paste volume on the SMT pads created lifting forces during reflow, causing pogo pins to tilt and shift out of alignment.

Figure 3. Reducing the stencil aperture to 50% of the pad area limited solder volume and maintained proper pogo pin perpendicularity after reflow without the need for a holding fixture.

To address the problem, the stencil aperture was reduced to 50% of the SMT pad area rather than a full 100% opening.

This adjustment provided sufficient solder volume to meet IPC-A-610 requirements while preventing excess solder from lifting the components during reflow. As a result, the pogo pins maintained proper perpendicular alignment after soldering, eliminating the need for an auxiliary fixture to hold them in position throughout the reflow process.

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MENTORSHIP **MATTERS**

Finding a Place in PCB Design

Lauren Waslick and Kristen Aguiar discuss mentorship, visibility and the career few people know exists.

by RYANN HOWARD

One of the PCB design community's greatest talents is hiding in plain sight.

Ask a room full of high school students what they want to be when they grow up and you'll hear doctor, lawyer, engineer, teacher, maybe even influencer if we're being honest. In my own case, I wanted to be a writer. I simply failed to anticipate that the characters would be engineers.

What you probably won't hear is "printed circuit board designer." Which is somewhat ironic, given that modern life would come to a grinding halt without them.

PCB design remains one of the most rewarding careers that few people know exists. Unlike medicine, law or software development, it rarely appears on a student's radar. Most designers find their way into the field through chance conversations or job postings that open a door they didn't know was there.

Lauren Waslick and Kristen Aguiar of Newgrange Design are no exception.

Today, both are respected instructors at PCB East and PCB West, helping train the next generation of designers. Yet neither encountered PCB design prior to starting their degrees, and neither imagined it would become the foundation of a long-term career.

For Aguiar, the search was less about circuit boards and more about finding a way to use the STEM skills she had spent years developing.

"I was just sort of looking for something that had a little bit more science, a little bit more math, something where I felt like I could utilize the skills I was learning in college," she said on an episode of PCB Chat. "And so I just stumbled across the job description, didn't know anything about circuit boards, but it had training from the ground up."

Waslick's path wasn't much different.

"With my degree in math, getting toward the end of my college years, I was trying to figure out what you can do with a math degree," she said. "I knew about going into finance or teaching or grad school, and none of that was really calling to me."

A job posting in electronics caught her attention. She applied, hoping it might be more interesting than the alternatives. Fifteen years later, she's leading design teams and teaching at industry conferences.

Figure 1. Lauren Waslick (left) and the author at PCB West 2025.

Mentorship in Real Time

Aguiar remembers those first years as overwhelming.

"PCB design is one of those things where you don't really learn about it in college," she said. "Going into a job as a young adult where you really don't know anything and having to sort of learn from your peers, self-teach yourself in a very technical field, I found that to be a lot."

What helped both women navigate that learning curve was mentorship.

For Waslick, that mentorship came directly from Aguiar and Newgrange founder Matt Leary. Working in a small team created opportunities for constant feedback and one-on-one coaching.

“Once I realized that was what it was going to be like, I was able to settle much faster,” Waslick said. “It’s years of learning and growing, which for someone like me, who is a math major, that’s exactly where I want to be.”

Aguiar also credits Leary with helping her build confidence in addition to technical skills. One piece of advice he gave her early in her career stayed with her. “I don’t understand why you don’t talk in phone calls,” she recalled him saying. “You know more than you think you do. You know more than the customer.”

At the time, she thought the idea was ridiculous. “I always thought he was so crazy for saying that,” she said. “What are you talking about? I’m only like two years in.”

Twenty years later, she admits he was right. “A lot of engineers that I was talking to, they don’t really know that much about PCB design.”

As Lauren and Kristen talked about mentorship, I found myself becoming less focused on the questions I had prepared and more focused on the answers.

I don’t normally host the PCB Chat podcast. In fact, before this episode, I never had.

When PCEA president Mike Buetow asked me to conduct the interview, I agreed without giving it much thought. Looking back, that’s probably unusual. Most people would at least spend a little time wondering whether they were qualified, whether they would ask the right questions or whether they would accidentally talk over the guests.

I never really got that far.

Part of the reason was that Mike seemed completely unconcerned about any of those possibilities. He asked me to do it with the kind of confidence that made it seem obvious I could. When someone you respect places that kind of trust in you, it’s surprisingly easy to borrow their confidence until you find your own.

Mentorship is one of those things that’s easy to recognize in hindsight.

Rarely does someone sit you down and announce, “Congratulations, you are now being mentored.” More often it looks like being trusted with something slightly bigger than you’re ready for. Hosting this podcast was simply the latest example.

I’ve always liked a line from Flannery O’Connor: “Accepting oneself does not preclude an attempt to become better.”

The longer I spend in this industry, the more I think that’s what good mentorship looks like. The best mentors don’t convince you that you’re already perfect. They simply help you see that being inexperienced and being capable are not mutually exclusive.

Figure 2. Kristen Aguiar (left), Lauren Waslick and Newgrange Design founder Matt Leary. Both Aguiar and Waslick credit mentorship and hands-on guidance with helping them build successful careers in PCB design.

Seeing Yourself in the Room

I'll admit it: one of the first things I did when I started attending PCB conferences was look around the room and ask myself a very scientific question: Where are the girls?

The PCB industry has made tremendous progress, but it remains a field where women are often outnumbered. Early on, I found myself paying attention whenever I saw women teaching classes or leading discussions. It wasn't that it was unusual, but that it was reassuring.

That's one reason Lauren Waslick and Kristen Aguiar stood out to me.

When I first encountered them at PCB East and PCB West, they were instructors. They were the people standing in front of a room full of engineers, teaching technical material, answering questions and sharing expertise. As someone still finding my footing in the industry, that visibility mattered.

Waslick remembers attending conferences early in her own career and often feeling like an outlier. "I think I was the only woman in the room, at least for some of the classes," she said. "And I also felt out of place because I was probably the youngest one in the room."

Today, both women have become part of the next generation of industry leaders, helping others feel more comfortable walking through those same doors.

“I feel like I owe it back to the industry to sort of put myself out there,” Aguiar said. “It just makes it seem so much more doable for the next generation.”

Fortunately, the demographics are changing. Slowly, yes, but noticeably. In fact, during our conversation, I pointed out that PCB East had recently achieved a milestone that probably won’t appear in any official industry report.

“We had enough girls this last show that we were able to do the Spice Girls at karaoke,” I joked.

No economist is likely to add that metric to a market forecast anytime soon, but it felt like progress nonetheless. Sometimes it shows up in conference photos. And occasionally, it shows up in an impromptu Spice Girls lineup.

An Industry Built on Hand-Me-Down Knowledge

Community came up repeatedly throughout my conversation with Lauren and Kristen. Again and again, they described an industry willing to teach, answer questions and help newcomers succeed.

“It was really surprising to me how open and helpful and just positive this whole community was as a whole,” Waslick said.

I found myself nodding along. That’s been my experience as well. Every industry likes to describe itself as welcoming. The PCB industry is one of the few I’ve encountered that seems determined to prove it.

Perhaps it’s because PCB design occupies such a specialized corner of engineering. The industry seems to operate on the understanding that if you learn something useful, you’re probably going to end up teaching it to someone else eventually.

By the end of our conversation, the discussion had shifted from career advice to encouragement. “If you like engineering, go for it,” Aguiar said. “We need more women.”

Most careers in PCB design start with curiosity, a willingness to ask questions and someone willing to answer them. Sometimes, that’s all it takes to find a place at the table.

RYANN HOWARD is managing editor of PCD&F/Circuits Assembly; ryann@pcea.net.

GETTING **LEAN**

Finding the Right Lean Tools

Choosing the right continuous improvement methodology can help manufacturers solve problems more effectively, sustain gains and strengthen lean operations.

CONTINUOUS IMPROVEMENT IS central to realizing the benefits of lean manufacturing. Even well-designed processes can benefit from periodic review and refinement. Two widely used methodologies for driving continuous improvement are PDCA (plan-do-check-act), also known as the Deming Cycle, and DMAIC (define-measure-analyze-improve-control). Both provide structured approaches to problem-solving, helping teams analyze issues, test solutions, measure results and standardize successful changes. The best choice depends on the complexity and scope of the improvement effort.

PDCA follows an iterative cycle focused on incremental improvement. During the plan phase, a team identifies a problem and develops a proposed solution. The do phase involves implementing the change on a limited scale. Results are evaluated during the check phase, and if the improvement proves successful, the act phase focuses on standardizing and expanding the solution. Because of its simplicity and flexibility, PDCA is particularly effective for smaller-scale improvement initiatives.

For example, SigmaTron's facility in Vietnam experienced an increase in functional test failures on a product, even though subsequent checks with a volt-ohm-milliammeter (VOM) found no defects. This suggested the issue was related to the testing process rather than the product itself. During the plan phase, the team developed a problem statement and established goals to reduce failure rates to below 0.5% and increase functional test throughput by 20%. A Pareto analysis revealed that most failures stemmed from voltage measurements that fell outside specification during testing. The team concluded that replacing a low-resolution voltmeter in the tester with a higher-resolution model would address the issue. They also identified opportunities to improve throughput by optimizing the C# test software and streamlining the load/unload process.

These changes were implemented during the do phase and evaluated during the check phase. Once the improvements proved effective, they were standardized and deployed across all testers during the act phase. In this case, PDCA provided the appropriate framework for a relatively straightforward process improvement.

DMAIC, a core Six Sigma methodology, takes a more rigorous, data-driven approach. In the define phase, teams establish the problem statement, identify critical-to-quality (CTQ) requirements, define project objectives, and assess business impact, customer impact, project scope and team responsibilities. During the measure phase, relevant process variables are quantified using tools such as cause-and-effect diagrams and Gage R&R studies. The analyze phase focuses on identifying trends, root causes and potential corrective actions. Improvements are then implemented and validated in the improve phase, often using design of experiments (DoE) techniques. Finally, the control phase establishes procedures to ensure gains are sustained over time.

DMAIC is particularly well-suited for complex, data-intensive problems where root causes are not immediately obvious. Trained SigmaTron Green Belt teams use this methodology to address more challenging improvement opportunities.

Both approaches offer distinct advantages. PDCA's straightforward structure makes it an effective introduction to continuous improvement and a practical tool for smaller projects requiring quick, focused solutions. DMAIC provides a more comprehensive framework for organizations tackling complex problems, involving cross-functional teams or addressing high-visibility, time-sensitive issues. It is especially valuable when the root cause of a problem is unclear or when multiple variables must be evaluated.

Understanding the strengths of each methodology and selecting the approach that best matches the challenge at hand is key to maximizing the benefits of lean manufacturing and continuous improvement initiatives.

KIET LE QUANG is general manager of SigmaTron International's Vietnam facility (sigmatronintl.com).

Silence as a Mission Statement

Silence may be golden, but it's terrible customer service.

SOMEBODY OWED US money for a project we performed in October and November 2025. They needed x-rays – instantaneous, naturally – to validate a project for a large, anonymous commercial spaceflight company with a fondness for overwrought usage of the letter X. Something about qualifying a Cu-Ag braze alloy sandwiched between an alumina inner cylinder and a Kovar outer cylinder. Danger lurks within. Our job: find it.

We did the job. Nine separate jobs, actually; many of them same-day turnarounds. Data were furnished very fast, enabling process upgrades so egos, er, X-rockets could fly. Just doing our part.

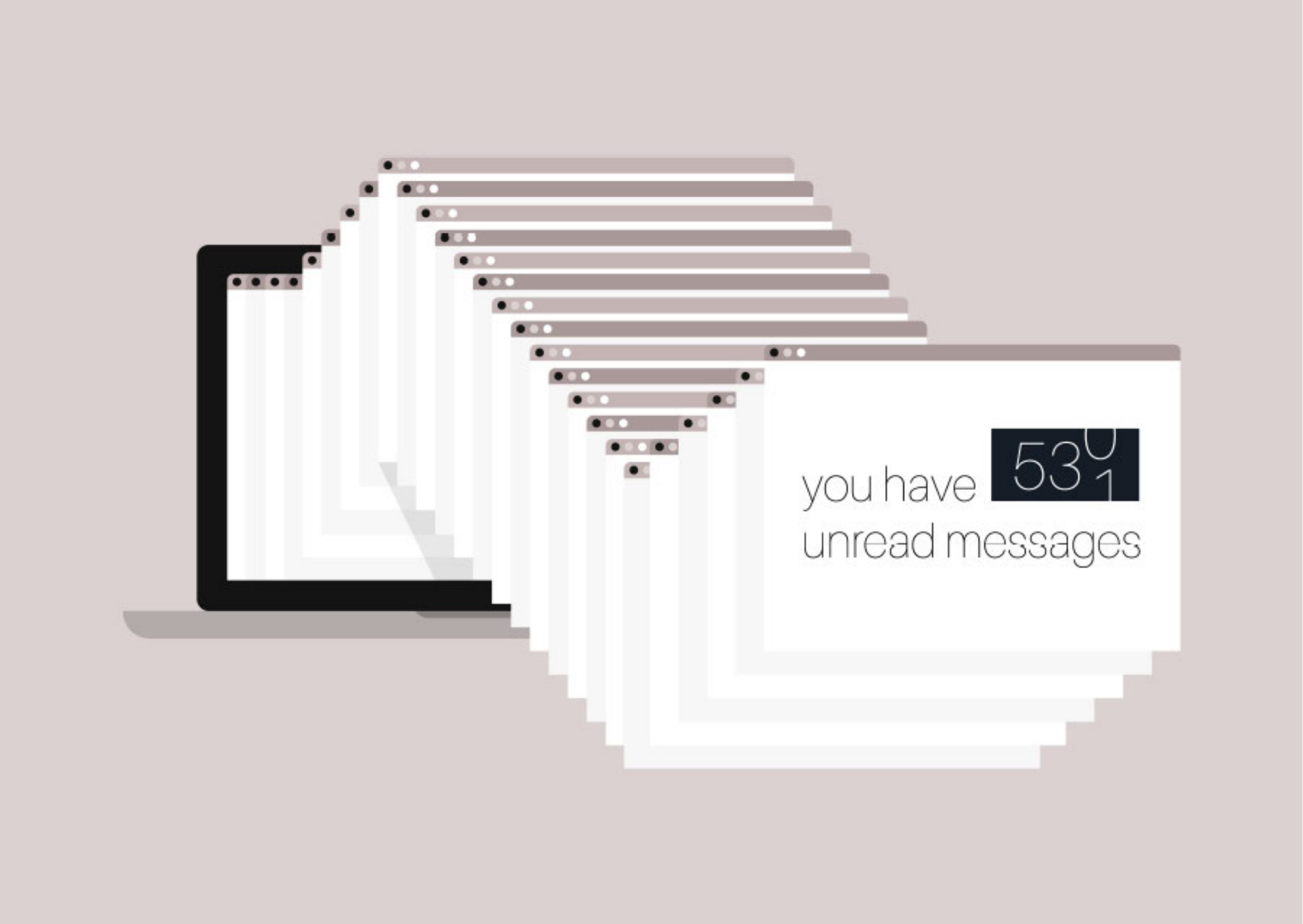
It's June 2026, and we're still awaiting full payment for services rendered eight and a half months ago. Curiously, the customer neglected mentioning their desire for net 270 terms. When we email them to seek payment status, with the subject line emphasizing the eighth request, the response is dead silence. Perhaps their accounting department wishes we'd just go away; accounts payable logic says that if they don't answer, the issue will spontaneously resolve itself into a non-issue, a question read only by intelligent life on distant galaxies. Maintain silence, and all will be well. Herewith a striking lesson illustrating why people should study the humanities in addition to accountancy.

Another day, another example. A customer with flying probe systems identical to ours in every way except the knowledge of its operators needs our assistance. Help is freely given. Upon completion of program debug, we transfer the finished program to the customer via FTP. The customer insists that they do the program installation themselves; in fact, their test engineer will only communicate with our test engineer by means of SMS. Something about a lack of confidence in English language proficiency.

We send them the completed, fully-debugged program. Weeks go by in silence. Follow-up emails to confirm all is well go unanswered. The presumption of tranquility on our end lingers, until the SMS pleas burst forth like incoming rockets, requesting written assistance with program installation. Written assistance. Cascading, line-downish requests, all via SMS, all the same. We respond, in writing, to every request. Requests by us for Teams meetings and remote login to their system to troubleshoot go into thin air.

Increasingly anxious SMS requests multiply. Each claims nothing is working, that they are unable to load and run our programs. A small remnant is surrounding, surviving on boiled potatoes and grit, seeking air support. They have a queue of finished production boards to test, but are unable to test them. Management is noticing. Our engineers offer to log in and help, but their technicians refuse to enable remote access to verify the problem in real time. Only written SMS communications are permitted. The excuse, once again, is limited English proficiency. Each message peels the skin of subterfuge off a bit more, and the clouds part; experience-based suspicion builds. Poor understanding of the elementary functions of the flying probe test system is manifestly apparent. Put plainly, these guys didn't know what they were doing.

But they're hiding behind text messages, thinking we can't unmask them.



Communication breakdowns, delayed responses and unmet expectations can create costly obstacles long before technical issues become the real problem.

It's not every day that my own engineers ask me to charge a customer for our time, but that's exactly what happened here. Frustrated, indignant, our folks drew the line. The fact that the customer's technicians were either untrained, poor learners or both was not, fundamentally, our problem. So, if by circumstance, and the need to move production testing forward, we resorted to remedial training, we should get paid. That's engineering logic. I'm good with that. So, respecting my team's judgment, we asked to be paid.

Pandemonium.

Crucially, the customer's test engineering manager was not good with that. In a well-aimed killjoy move designed to ruin Friday afternoon tranquility, we received an email detailing how uncooperative and unsupportive our company had been to his company. As relayed to him (in person!) by his trusted employees. He lamented that our programs would not work on his machines (never mind that they ran flawlessly on ours). He insinuated we were gaining a poor reputation among the technicians at his facility (who, it might be noted, were accomplished corporate infighters). To make matters worse, asking for payment for hours spent training fanned the flames. Contract manufacturing managers take a dim view of surcharges. Moreover, this manager had found another company which, he claimed, could generate programs that did run on his machines with little or no difficulty. In 750 words, he expressed one word: *J'accuse!*

Nothing prompts a lightning response faster than an injustice broadcast through the megaphone of a large corporation. A phone conference was arranged within hours. Three on our side; the test engineering manager, alone, on his side. No technicians present. The test engineering manager droned on about how difficult we were to work with, as his employees relayed to him. We tried defending ourselves, but it was one of those monologues where he just kept talking, right over our objections. He had his script and wasn't deviating from it. At a certain point, experience dictates you remain silent and let the customer delight in himself, degrading content and context in the process. Just let him finish. We take notes.

Upon completion, we ignored his lengthy indictment and asked the Great Man if we might assist, and in what form. He responded that we could help by guiding his technicians step by step through the program installation process. Naturally, we replied that we'd be glad to do so; in fact, serendipitously, we'd been doing so all along. (His valued team members had neglected to inform him about that. Knowledge is power. So is withholding it.) He noted that *his* customer intended for him to produce 60 flying probe programs this year, and that if we could successfully guide his people through this first rough patch, good things would follow. So, we did. Our lead engineer spent *seven hours* online with the customer's test technician, guiding him/her via SMS (again!) through the installation process, step by excruciating step. Until finished. And it worked: boards got tested. After the seventh hour, our engineer rested. Amen.

Two weeks later, I followed up again. I wanted to know the status of the much-anticipated 60-part numbers. Shockingly, there was no response to my email.

I tried a second time two weeks after that and, again, a month after that. Same result one month later. Radio silence.

My scam antenna was acquiring strong signals. On the one hand, there is no second, independent source for the exact kind of flying-probe programs this customer needs that would be plug-and-play on his machines. Other than his own internal resources, coming from another site, we represented his only drop-in solution. Other options require elaborate conversion steps. Given the extended silence, we began to get the feeling of having been played.

As of the date of this writing, in June 2026, we're still waiting.

Another customer, an OEM, needed AXI (automatic x-ray inspection) services. They design very large boards, the kind that don't fit in many AXI systems, including their EMS provider's AXI system. The latter informed their customer of this inability to provide in-house inspection services on a large backplane. So, both OEM and EMS company, separately, called us. Could we help, stat? Except they used the tired euphemism "support" as in "We need you to support this requirement." Like Atlas, holding up the world. All systems go.

Until they got the quote.

In what had to be a new first in creativity, the OEM purchasing manager lectured us in an email that our AXI program pricing was unacceptably high because our programming engineering rates matched those of *elite* programmers and software engineers, the kind involved in AI development. He looked this up on the Bureau of Labor Statistics website. Surely the comparison, and his criticism, was on target. He was, after all, a Supply Chain Professional, therefore unimpeachably correct.

Well, no.

Setting aside the relativizing insult to our programming skills, and setting aside the purchasing manager's purely abstract understanding of the AXI process, what remains is a unique board. It will fit in exactly one machine within a 50-mile radius of my desk. Coincidentally, that one machine resides 40 feet from my office. So, their one solution remains here, and no amount of statistical wizardry by the BLS or APICS or IEEE or GEA or SMTA or anybody else will alter that reality.

So: Mr. Know-It-All OEM Purchasing Manager, make my day.

Two months later, we are still awaiting a purchase order. The latest excuse is that management is still reviewing. Some people have a unique sense of urgency. Which is fine.

They still have a problem. We still have the only solution (cue sinister Spaghetti Western gunfighter music).

Between declaration of problem and its resolution, three months (and counting) have elapsed. Like the Voyager spacecraft exiting the solar system, the gap increases daily, filled mostly with silence. Problem-solving with the velocity of a banana slug.

These people and their conspiratorial, bureaucratic little minds really exist. They share in the miscalculation of gross national product.

Speaking of the silence of unanswered prayers and unresolved problems, another EMS customer was forced to use our services by its OEM. In this case, we were favorably disposed to the use of force.

The complexity and use of the PCBA in question (failure is not an option) dictated a three-fer: every board in the run would be tested using flying probe, inspected at every solder joint with AXI, and manually x-rayed in certain critical areas by a high-end 2D/2.5D x-ray system. Upon completion of testing, each thrice-tested board is accompanied by its weight in data. Which nobody reads.

Setting up three programs (yes, even manual x-ray needs a program to speed repetitive steps) takes time. More than the one-day notice the EMS gave us. For the eighteenth time, we were forced to explain to our slow learner that we are not a vending machine: you don't insert a Susan B. Anthony dollar and out pops a tested board. Like magic.

Perhaps this failure to inform us until the eleventh and three-quarter hour had something to do with their never intending to use us in the first place, until the OEM laid down the law. So, they scrambled. Which they've been doing a lot because the board was a handful, requiring all hands-on deck at the assembly site and making the OEM the program manager, practically speaking. Whatever the reason, they were late. One week late. A case of rapidly diminishing lead time (The testing guys are good sports; they'll make up the difference, right?) But between declaration of intent and delivery of boards, our requests for status went unanswered. Until the board showed up, just in time to ruin somebody's three-day holiday weekend. But now the shoe was on the other foot, and they demanded up-to-the-minute status reports.

In business, like marriages, communication is essential. Silence suggests bad things are happening. Prolonged silence confirms it.

We could tell you some of the details, but proprietary information and consequent NDAs require that we remain silent.

ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.

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The 2.92mm solderless PCB connectors support high-frequency stripline and microstrip applications to 40GHz. Available as vertical PCB jacks, the connectors use a threaded interface to eliminate solder joint variability and maintain consistent connector-to-PCB contact. Support impedance control across different PCB stackups while allowing installation, removal and reuse during prototyping and validation. Constructed with passivated stainless steel bodies, gold-plated beryllium copper contacts and ULTEM insulators. For microwave, millimeter-wave, test and measurement, aerospace, defense and advanced communications applications.

Amphenol RF

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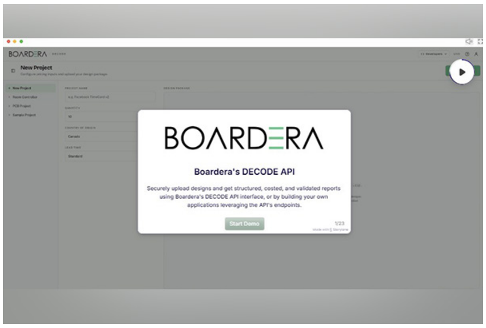

BOARDERA

Boardera's DECODE API

Securely upload designs and get structured, costed, and validated reports using Boardera's DECODE API interface, or by building your own applications leveraging the API's endpoints.

BOARDERA DECODE API MANUFACTURING AUTOMATION PLATFORM

Decode API manufacturing automation platform supports integration of PCB fabrication, assembly and quoting workflows into ERP, customer-facing and manufacturing systems. Processes Gerber and ODB++ design packages to extract stackup, board dimension, drill, DfM and fabrication data while supporting BoM analysis, component sourcing, assembly planning and pricing. Returns structured manufacturing data for fabrication, assembly and turnkey production estimates. Includes SpeedDfM analysis, version-controlled JSON schema support, BoM sourcing automation and assembly planning capabilities for quoting and manufacturing workflows.

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ELECTRONINKS EI-1169 CONDUCTIVE INK

EI-1169 UV-curable silver conductive ink supports inkjet deposition for printed electronics, semiconductor packaging and additive manufacturing applications. Polymer-free metal-organic decomposition (MOD) formulation provides adhesion on copper, epoxy and polyimide substrates while supporting low-temperature processing and stable jetting performance across industry-standard printheads. Supports UV curing at 365nm and 395nm wavelengths and is lead-free and halogen-free. Combines long shelf stability, repeatable print performance and scalable processing for digitally manufactured electronics, EMI shielding and advanced interconnect applications.

Electroninks

electroninks.com

IGNYS RAPIDJIG PCB TEST FIXTURE DESIGN TOOL

RapidJig PCB test fixture design tool automates creation of bed-of-nails test fixtures from Gerber design files. Generates CNC-ready manufacturing packages including Excellon drill files, G-code, STL models and engineering documentation. Supports common spring probe types and automatically configures drill dimensions based on probe selection. Provides live cost estimation, bill-of-materials generation and local file processing to keep design data on the user’s machine. Compatible with RS-274X, X2 and X3 Gerber formats and operates directly in a web browser without installation.

Ignys

ignys.com

KEYSIGHT PRO XA6 SA6320A AND EXPERT XA5 SA6210A SIGNAL ANALYZERS

Pro XA6 SA6320A and Expert XA5 SA6210A signal analyzers support wideband wireless, 5G NR, WLAN, radar and millimeter-wave design validation. Pro XA6 SA6320A provides up to 8GHz analysis bandwidth, frequency coverage to 67GHz, full preselection and GPU-accelerated 5G NR demodulation. Expert XA5 SA6210A offers swept measurements to 32GHz, up to 2GHz analysis bandwidth and dual-channel RF analysis for MIMO, ultra-wideband and radar applications. Feature advanced error vector magnitude measurements, wide-resolution bandwidth support, dual-receiver architecture and compatibility with legacy X-Series SCPI command sets.

Keysight Technologies
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AG16xFNxx Series 80V automotive Mosfets support 48V vehicle power systems, including inverter control circuits, electric motors and electric water pumps. Come in compact HPLF5060 and DFN3333 packages to reduce board space requirements compared with conventional automotive MOSFET packages. Copper clip junctions are said to enhance heat dissipation and high-current operation. HPLF5060 devices feature gull-wing leads, while DFN3333 devices incorporate wettable flank technology for solder joint inspection and reliability. AEC-Q101 qualified.

Rohm Semiconductor
rohm.com

STACKPOLE TNC SERIES NTC THERMISTORS

TNC Series thick-film NTC thermistors provide temperature sensing and monitoring for automotive, industrial, battery management and medical electronics applications. Come in 0402, 0603 and 0805 case sizes with resistance values from 50Ω to 500kΩ, B values from 2410K to 4700K and operating temperatures to 150°C. Utilize thick-film technology to improve mechanical strength, maintain consistent thickness across resistance values and increase resistance to cracking compared with multilayer thermistors. Feature thermal response, solderability, heat resistance and AEC-Q200 qualification.

Stackpole Electronics

seielect.com

VISHAY IHDV SERIES POWER INDUCTORS

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Vishay Intertechnology

vishay.com

CA

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Vision LUXO benchtop magnifiers provide magnification and task lighting for assembly, inspection, rework and production applications. Combine precision optics with Luxo's K-arm positioning mechanism for distortion-free viewing, smooth adjustment and stable positioning during detailed manufacturing tasks. Five-year warranty. Intended for electronics manufacturing environments requiring enhanced visual inspection, operator comfort and workstation flexibility.

CE3S

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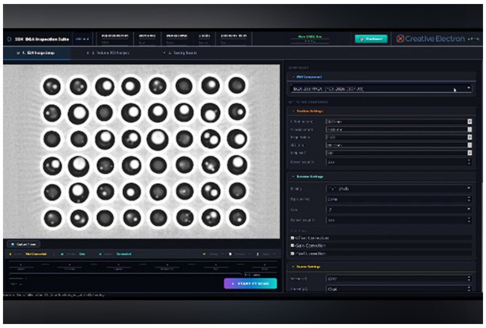
COLLECTIVE MIND VISION AI LABEL READER

Vision AI label reader automates label inspection, identification and data capture for goods-in and logistics operations. Uses AI-based image analysis to extract and interpret printed text, 1D and 2-D codes, and handwritten information across varying label formats, languages and code types. Powered by an IDS uEye CP industrial camera and engineered to handle reflective packaging, damaged codes and changing lighting conditions. Supports ERP integration, automated validation, traceability and inventory management workflows.

Collective Mind

comi.de



CREATIVE ELECTRON TRUVIEW PRIME SDX X-RAY

TruView Prime SDX benchtop x-ray inspection system combines 2-D x-ray, 2.5D imaging and SDX Planar CT capabilities in a compact platform for electronics manufacturing inspection. Features a 20" × 20" inspection area for large BGAs, stacked packages, bottom-terminated components and complex assemblies. AI-powered analysis tools automatically measure solder quality metrics including BGA and pad voiding. Supports quality control, process development and failure analysis with repeatable planar CT workflows and saved inspection parameters.

Creative Electron

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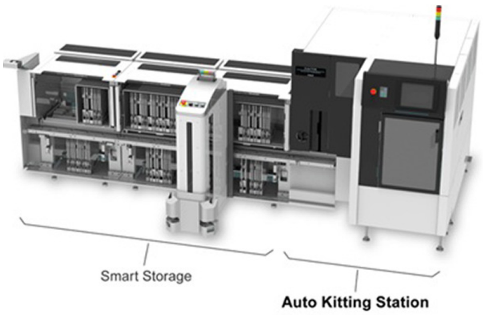
DOW DOWSIL TC-3120 THERMAL GEL

Dowsil TC-3120 thermal gel is a silicone-based thermal interface material for optical modules, dense electronics and high-speed data applications. Provides thermal conductivity of approximately 12W/m·K while minimizing oil bleeding and condensed outgassing to maintain optical-grade cleanliness. Flowable one-part material supports bondline thicknesses as low as 200µm, fills large gaps and can be reworked after curing. Intended for 800G and 1.6T optical modules, telecommunications equipment, autonomous vehicles and electronic control systems.

Dow

dow.com



FUJI AUTO KITTING STATION

Auto Kitting Station automates tape reel loading for SMT feeder preparation and integrates with Fuji NXTR A placement machines, Smart Storage systems, AMRs and automated warehouses. Automates reel removal, reel identification, tape preprocessing and feeder loading for 8mm tape components. Intended for high-mix, low-volume manufacturing environments where frequent product changeovers impact labor and efficiency. Supports integration of storage, transport, kitting and placement operations to advance automated SMT production workflows.

Fuji Corp.

smt.fuji.co.jp

MAGNALYTIX OE IN A BOX PROCESS QUALIFICATION KITS

OE in a Box Full Process Kit and OE in a Box High Density Kit support IPC J-STD-001 objective evidence generation and assembly process qualification for electrochemical reliability. Include test cards, taped-and-reeled components, SIR testing services and certificates of compliance upon successful completion. Support qualification of top- and bottom-side SMT assemblies, multiple soldering processes and conformal coating applications.

Magnalytix

magnalytix.com

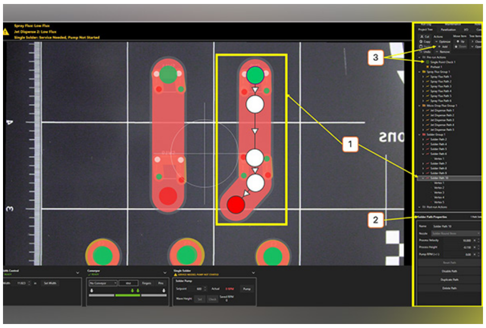
MASTER BOND MASTERSIL 981-LO LOW-OUTGASSING SILICONE

MasterSil 981-LO low-outgassing silicone supports bonding, sealing, coating and encapsulation applications requiring optical clarity and flexibility. Two-component addition-cured system meets NASA low-outgassing specifications and is for aerospace, satellite, optical and optoelectronic applications. Features Shore A hardness of

20-30, elongation of 200-300%, operating temperatures from -65° to +400°F, dielectric strength of 450V/mil and volume resistivity greater than 10^{14} ohm-cm. Bonds to metals, glass, plastics, ceramics and silicone rubbers.

Master Bond

masterbond.com



TM SOLDERING EMBERX SELECTIVE SOLDERING CONTROL SOFTWARE

EmberX selective soldering control software supports programming, process control and monitoring for PHOENIX selective soldering platforms. Provides visual programming, onboard PCB image capture, HD video monitoring, customizable data collection and automated process validation tools. Supports wave height verification, nitrogen quality analysis, closed-loop preheating, maintenance tracking, fiducial correction and panelized board processing. Intended to reduce setup time and improve production consistency in manual and inline selective soldering environments.

TM Soldering Solutions

tmssolutions.us

In Case You Missed It

PCB Materials

"A Molecular Pathway to Corrosion-Resistant Printable Copper"

Authors: Jun Zhang, *et al.*

Abstract: Copper's exceptional electrical and thermal conductivities make it essential for electronics and energy systems. Oxidation and corrosion, however, limit its long-term reliability, and existing protection strategies often involve high-temperature or multistep processing. The authors report a molecularly reactive strategy that converts copper precursors to metallic copper at <150°C, while generating an ultrathin carbonaceous and copper(I) surface passivation. Catechol-based ligands mediate copper reduction, enable low-temperature interparticle fusion, and impart surface passivation, yielding flexible copper with low resistivity and exceptional stability (>1000 hr. in acid, >200 hr. in sulfide, >240 hr. at 140°C). This strategy resolves the long-standing tradeoff among conductivity, corrosion resistance and processability for next-generation flexible electronics and energy systems. (*Science,* May 14, 2026, vol. 392, no. 6,799, https://www.science.org/doi/10.1126/science.aed4488*)*

Printed Electronics

"On-Demand Additive Nanomanufacturing of Electronics in Microgravity: Towards In-Space Manufacturing of Electronics and Functional Devices"

Authors: Colton Bevel, *et al.*

Abstract: On-demand manufacturing of electronics in space is critical not only to enable the availability of essential devices for long-duration missions but also to reduce spare parts inventory, decrease resupply missions, accelerate repairs, and use recycled materials to produce custom electronics. Existing ink-based printing methods remain reliant on gravity and complex ink logistics, however. Here, the authors present the first successful demonstration of an inkless, dry-additive nanomanufacturing (Dry-ANM) platform for printed electronics under microgravity conditions. A custom payload was developed and analyzed to generate, deposit, and sinter silver and copper nanoparticles during 50 25-sec. microgravity intervals over a two-day parabolic flight campaign. Terrestrial control samples were printed with identical parameters to ensure that any observed differences reflect only the effects of microgravity. In general, the microgravity-printed samples performed better or retained comparable electrical performance to terrestrial samples, with printed silver and copper achieving resistivities of 13.8μΩ·cm and 160.8μΩ·cm, respectively. By tailoring print parameters to compensate for increased particle flow under the influence of microgravity, these resistivities are expected to be driven even lower. This achievement marks a paradigm shift for in-space additive manufacturing of electronics and a significant step toward sustainable long-term space missions. *(npj Advanced Manufacturing,* vol. 3, no. 23, 2026; https://www.nature.com/articles/s44334-026-00085-w*)*

Solder Materials

"Low-Temp Solders Are Suddenly Critical for Chiplets and Photonics"

Author: Laura Peters

Abstract: Low-temperature solders are becoming increasingly attractive in the chiplet era because they promise substantially reduced package warpage while enabling the use of temperature-sensitive components such as silicon photonics, LED modules, and flex circuits. These solders are mostly used today in mobile devices, wearables, camera modules, and for thin printed circuit boards, where warpage is a significant problem. Leading-edge HPC/AI applications that must withstand high current densities and significant thermal gradients are likely to stick with the tried-and-true SAC305 solder. Nonetheless, SAC305's high thermal budget (235° to 250°C reflow) is becoming increasingly incompatible with large, thin, heterogeneous packages with complex stackups. *(Semiconductor Engineering,* May 21, 2026, https://semiengineering.com/low-temp-solders-are-suddenly-critical-for-chiplets-and-photonics*)*

Stretchable Electronics

"Stretchable Neuromorphic Electronics for Future Human-Integrated Intelligence"

Authors: Tianda Fu, *et al.*

Abstract: Neuromorphic electronics emulate the computational principles of biological neural systems, offering low-power, adaptive, and parallel signal processing capabilities for next-generation intelligent systems. When integrated with stretchable platforms, neuromorphic devices gain the mechanical compliance necessary to interface seamlessly with soft, dynamic biological environments, enabling applications in wearable computing, bioelectronic skins, and implantable artificial intelligence. This review provides a comprehensive overview of recent progress in stretchable neuromorphic electronics, covering device architectures, material design strategies, underlying neuromorphic mechanisms, and novel applications. The authors discuss key challenges and outline future research directions toward advancing the performance, integration, and translational potential of stretchable neuromorphic systems. The aim is to provide a foundational resource to guide the co-design of materials, devices, and systems toward autonomous, skin-conformal neuromorphic intelligence. *(International Journal of Extreme Manufacturing,* vol. 8, no. 4, Mar. 23, 2026, https://iopscience.iop.org/article/10.1088/2631-7990/ae5004*)*