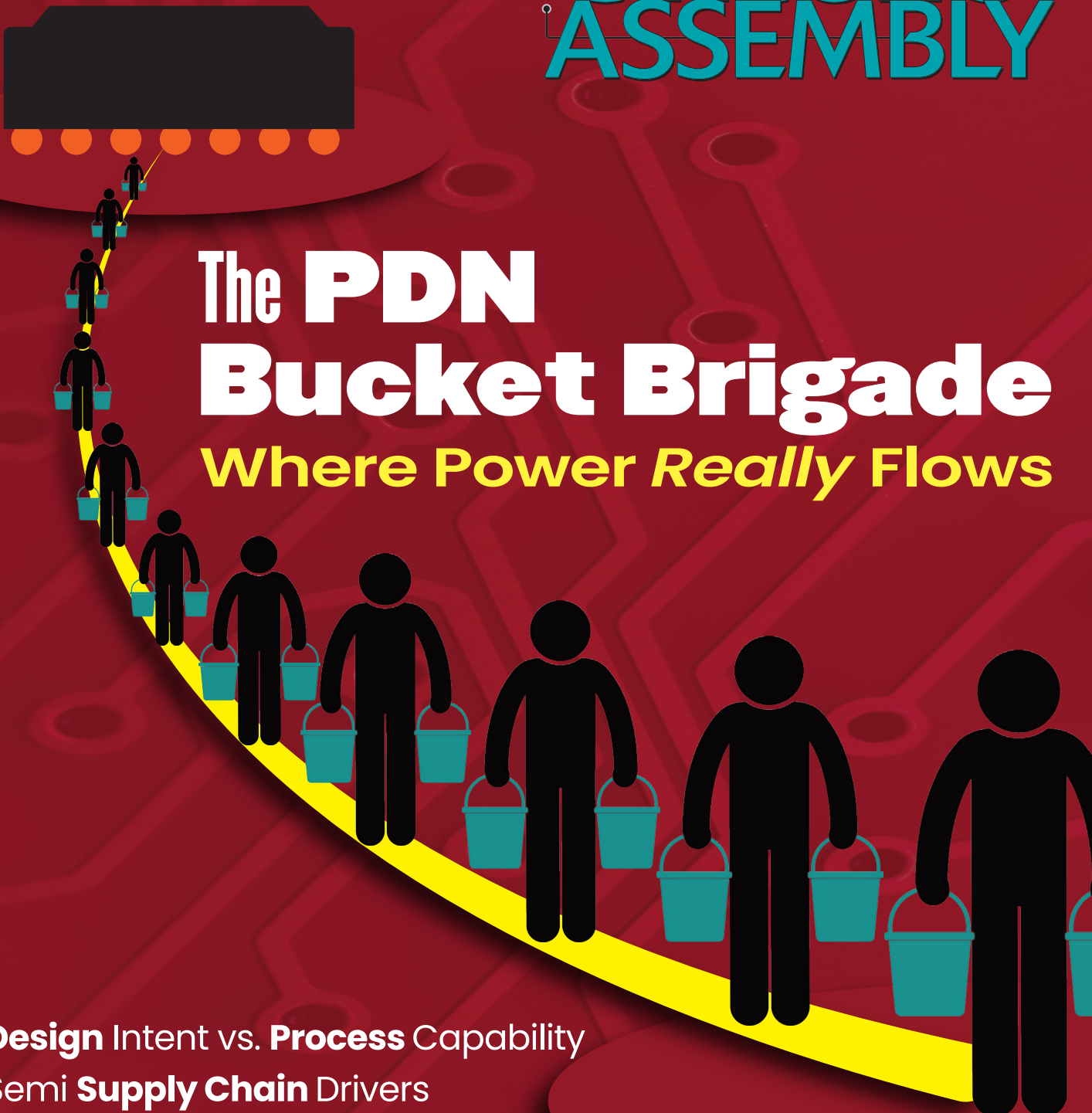


pcdandf.com
circuitsassembly.com
August 2026

PRINTED CIRCUIT DESIGN & FAB

CIRCUITS ASSEMBLY

An illustration of a bucket brigade on a red background with a circuit pattern. A yellow path curves from the top left towards the bottom right. Along this path, a line of black silhouettes of people is shown. The first person at the top left is carrying a bucket and is positioned under a black rectangular object with seven orange circles below it, representing a power source. As the path curves, more people are added, each carrying a bucket. The path ends with a single person at the bottom right. The title 'The PDN Bucket Brigade' is written in large white letters, and 'Where Power Really Flows' is written in yellow italicized letters below it.

The PDN Bucket Brigade

Where Power Really Flows

Design Intent vs. **Process** Capability

Semi **Supply Chain** Drivers

Mastering **AI** in the **Manufacturing** Environment

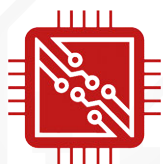
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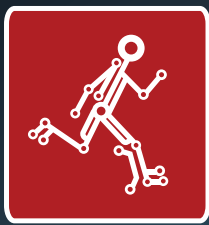
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PCB TRACE

20 YEARS OF MANUFACTURING
EXPERIENCE WITH BLIND AND BURIED
VIAS, RIGID FLEX & FLEX PCB

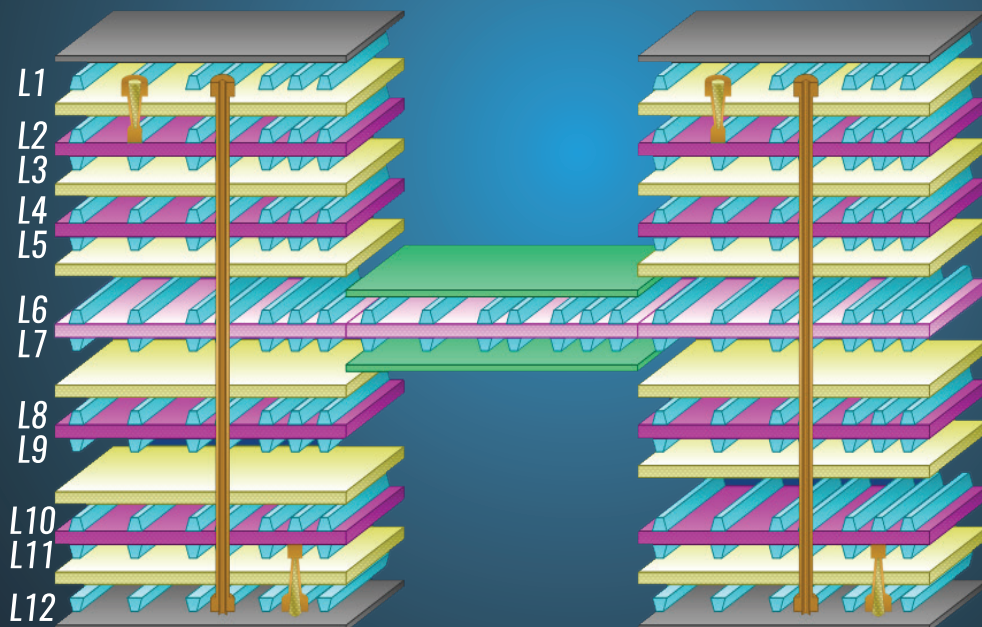


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BOARDS, ASSEMBLY & FULL TURNKEY

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Blind Via L1-L2 & L11-L12, 0.003" Hole, Resin Filled,
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CAVEAT LECTOR

Some things never change.

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MONEY MATTERS

ROI

Standards must keep pace.

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BOARD BUYING

Location isn't the strategy.

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FOCUS ON BUSINESS

Hold your horses.

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Making reshoring a reality.

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DESIGNER'S NOTEBOOK

Power starts the signal.

John Burkhardt, Jr.

ECAD TIPS & TRICKS

Geometry shapes power integrity.

Kirsch Mackey

MATERIAL GAINS

Building AI's backbone.

Alun Morgan

THE FLEXPERTS

Mind the bend.

Mark Finstad

TECHNICAL ABSTRACTS

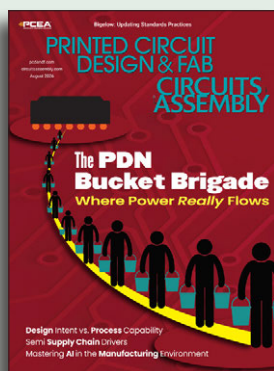
DEPARTMENTS

AROUND THE WORLD

PCEA CURRENT EVENTS

MARKET WATCH

OFF THE SHELF



PRINTED CIRCUIT DESIGN & FAB CIRCUITS ASSEMBLY

FEATURES

POWER DELIVERY (COVER STORY)

The Charge of the Bucket Brigade

Reflections on distributed electromagnetics.

by DANIEL BEEKER

FLEX DFM

Flex DfM Guidelines, Part 1

Learn how following key flex DfM guidelines can boost manufacturing yields, minimize production risks and improve long-term product reliability.

by AKBER ROY

PROCESS WINDOWS

Why Don't UHDI Capability Charts Tell the Whole Story?

Understanding the distinction between process capability and design intent can help engineers optimize UHDI performance while improving manufacturability and production yield.

by ANAYA VARDYA

INDUSTRY PERSPECTIVE

Seeing Electronics Manufacturing Through New Eyes

Continuous learning, quality and process improvement are at the heart of electronics manufacturing, influencing both personal development and the technologies that power today's world.

by WILL O'NEIL

DOCUMENTATION AUTOMATION

The Workday You Lose to Documentation, and How to Get It Back

Discover how AI can transform routine reports, meeting notes and work instructions into editable first drafts, enabling engineering teams to save time and focus on higher-value work.

by SEAN PATTERSON

SUPPLY SHIFT

AI Is Reshaping the Semiconductor Supply Chain

AI-driven demand is reshaping semiconductor supply chains, driving manufacturers to prioritize capacity, adjust pricing and tighten availability for mature-node devices.

by MARC SCHWANBECK

AI SECURITY

Claude Mythos and Project Glasswing: What OEMs Need to Know Now

Embedded product security is entering a new era as AI reshapes the cybersecurity landscape and introduces increasingly sophisticated threats.

by RAJESHPAL SINGH

ON PCB CHAT (PCBCHAT.COM)



MAKING AI USEFUL IN MANUFACTURING

with SEAN PATTERSON

RETIRING THE PCB RESPIN

with AJ COOPER

THE LATEST ECAD MARKET DATA

with WALLY RHINES

CLOSING THE GAP BETWEEN
VALIDATION AND REALITY

with DR. NISHITH KUMAR REDDY
GORLA

RESPONSIBLE TECHNOLOGY
ADOPTION

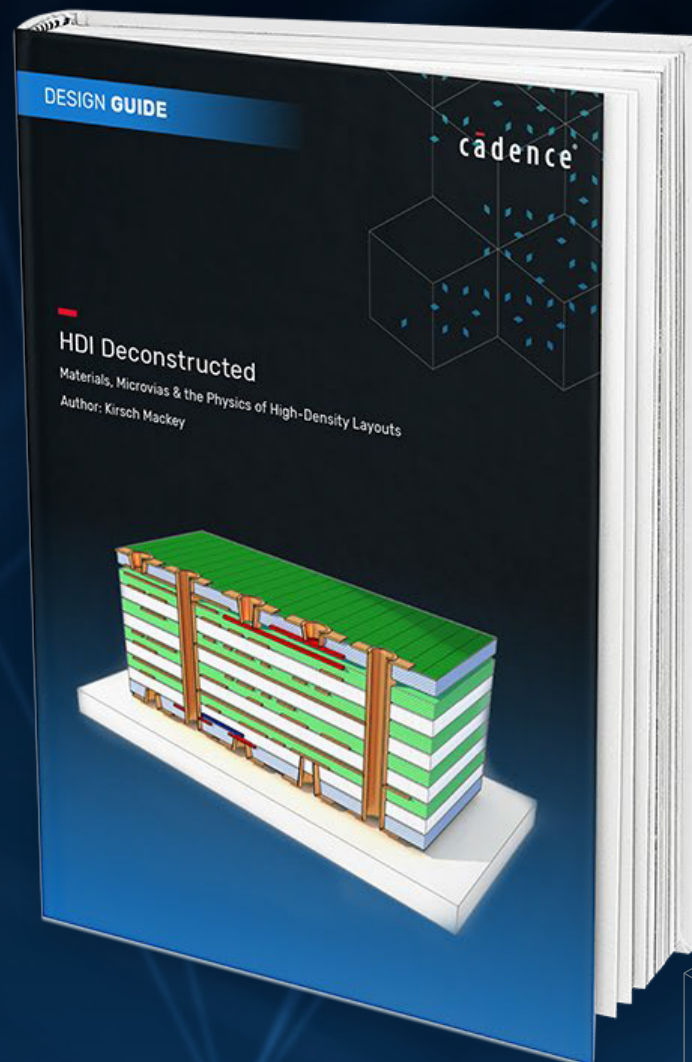
with DR. JAMES MAISIRI

HDI Deconstructed

Materials, Microvias & the Physics
of High-Density Layouts

Get the “why” behind HDI design challenges.
Learn the critical tradeoffs that influence
reliability, performance, yield, and
production success.

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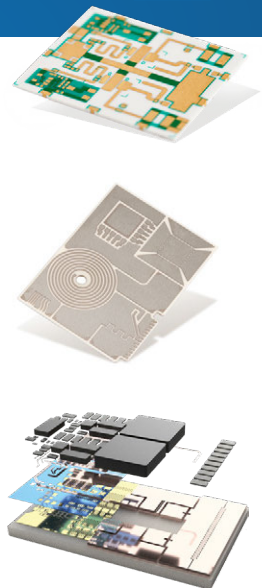
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Back in the Saddle

“Just when I thought I was out, they pull me back in.” – *Al Pacino*

SO LET ME start where Mike Buetow left off in our last issue: Thanks. And let’s hear a round of applause for Mike. He’s spent 26 years writing this column, longer than both of my marriages combined.

But I see why he’s stuck around for so long. PCEA’s magazines, newsletters and trade shows provide vital information for technologists in the PCB design, fabrication and assembly segments. People rely on our products to do their jobs better and more productively. Readers tell us how important our content is.

Plus, PCEA is a great place to work. I’m fortunate to be part of a group of wonderful people, from the staff to the board members, some of whom I’ve known since the ‘90s. They’re a lot of fun, especially at trade shows. But I can’t tell too many stories about the old trade show days because of the statute of limitations.

I started out at *Printed Circuit Design* in 1999 as an assistant editor, still a wee lad in my 30s. (According to our 1998 PCB Designer Salary Survey, the average PCB designer was around my age.) On my first day, I inherited a Rolodex and a desk full of hanging folders. I opened snail mail every day, because that’s how most companies sent out product announcements and press releases.

At the time, HDI had just begun to proliferate, thanks to cellphones and the new GPS devices. Flexible circuits, especially rigid-flex, were considered too expensive for most applications.

On the design side, every design was output in Gerber. EDA tools featured autorouters, but designers didn’t like to use them. Signal integrity was a growing concern, but most PCB designers didn’t have to worry about SI yet, and power integrity was rarely mentioned at all. Signal integrity analysis tools were expensive add-ons, not part of your typical mainstream EDA platform.

Speaking of which, there were nearly a dozen mainstream EDA companies back then, including VeriBest, DDE, PADS, Intercept Technology, Protel and Accel, in addition to the bigger players Mentor Graphics, Cadence and Zuken. Cadence acquired OrCAD that year.

At the time, the industry was riding high. The US was still the electronics manufacturing powerhouse of the world. The dotcom boom was in full swing, and North American fabricators still numbered in the thousands. But change was coming.

Many of the EDA startups I encountered were dotcoms, and they were completely virtual. They often called

themselves something like “a portal for the PCB design and design engineering community.” Perhaps even an e-portal! They were showered with Silicon Valley e-cash, but almost all of them were e-gone within a few years, as were many American fabricators.

A lot has changed since 1999. We’ve gone through a laundry list of disruptions: three downturns, implementation of the Restriction of Hazardous Substances directive, Covid, the post-pandemic supply chain debacle, the continued consolidation of EDA companies and PCB manufacturers, and the steady flow of PCB manufacturing from North America to Asia. We’re now down to about 180 North American fabricators, but these companies are stronger than ever.

Along the way, we’ve witnessed a number of manufacturing innovations, such as UHDI, SAP and mSAP, and the meteoric rise in the use of flexible and rigid-flex circuits. Rigid-flex has gone from niche to mainstream in a little over a decade.

On the EDA side, we have the “Big Four” PCB design software companies and a slew of companies making free and inexpensive CAD tools. Almost every PCB design tool contains some type of signal and power integrity analysis capability, as well as thermal management. Autorouters now feature a variety of capabilities that were unheard of years ago, but designers still don’t like to use them. And despite the availability of IPC-2581 and ODB++ intelligent data transfer standards, Gerber is still used to output over 90% of PCB designs.

Some things never change.

In the last few years, AI has become part of our lives, at work and play. AI-assisted software is now used throughout our industry. On the shop floor, process engineering managers see AI as a means for simplifying their daily reports. But some designers believe AI is going to replace them, not assist them.

Do you see AI as a disruption or an innovation?

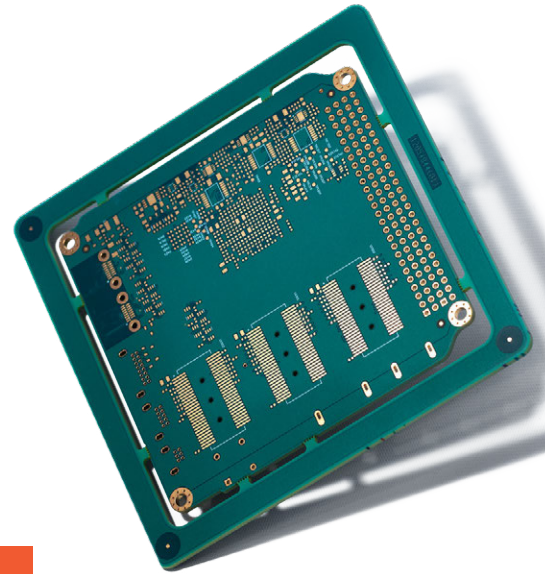
Well, I’ve been given the keys to the car, and I promise I won’t wreck it. I’m going to keep covering this crazy industry that’s been so good to so many of us. I’m glad to be back working with Mike, Frances Stewart and Brooke Downey, and my new coworkers Ryann Howard, Will Bruwer and Leah Spinks. What a great team.

See you next month!



ANDY SHAUGHNESSY is content architect of PCD&F/Circuits Assembly; andy@pcea.net.

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Foxlink Opens First US AI Factory in Texas

FORT WORTH, TX – Foxlink Group has opened its first US AI Factory, launching an advanced manufacturing facility in Fort Worth as part of its strategy to integrate artificial intelligence into electronics manufacturing.



Leaders from Taiwan's Foxlink Group celebrate the opening of the company's first "AI Factory" at Hillwood's AllianceTexas in Fort Worth.

The facility combines large-scale GPU computing infrastructure with AI-driven robotics and automation, supporting Foxlink's transition from a traditional electronics manufacturing services (EMS) provider to an AI-enabled manufacturing model.

The company plans to deploy the AI Factory concept across surface mount technology (SMT) and final assembly, testing and packaging (FATP) operations. Foxlink said the Texas site will support growing North American demand for localized manufacturing and more resilient supply chains. 

Keiron Raises \$24M to Scale LiFT Solder Paste Printing

EINDHOVEN, THE NETHERLANDS – Keiron Printing Technologies has raised \$24 million to accelerate commercialization of its laser-induced forward transfer (LiFT) solder paste printing technology for electronics assembly.

The funding will support production scale-up, global commercial expansion across Europe, North America and Asia-Pacific, and continued development of the company's next-generation printing platforms.

Keiron's HF2 LiFT printer replaces conventional stencil printing, jet printing and solder paste inspection (SPI) with a digital, non-contact process designed for high-mix, low- to medium-volume manufacturing and high-reliability electronics applications. 

SEL Breaks Ground on Idaho Electronics Manufacturing Facility

MOSCOW, ID – Schweitzer Engineering Laboratories (SEL) has begun site preparation for a new \$50 million electronics manufacturing facility in Moscow, ID, that will expand the company's production capacity.

The facility will be constructed adjacent to SEL's existing printed circuit board factory on the company's Schwartz Campus. Production is expected to begin in summer 2027, with the completed site employing approximately 1,000 workers.

Construction is scheduled to begin later this summer, with completion anticipated in late 2027. SEL manufactures electronic devices at facilities in Washington, Indiana and Illinois. 

East West Expands with Vexos Acquisition

ATLANTA – East West Manufacturing has acquired electronics manufacturing services provider Vexos, expanding its engineering, manufacturing and supply chain capabilities across the Americas and Asia.

The acquisition adds Vexos' operations in the United States, Canada, Mexico, China and Vietnam to East West's global manufacturing network.

Vexos specializes in high-mix, high-complexity manufacturing for medical, aerospace, AI data center and other regulated markets. East West said the acquisition strengthens its product lifecycle capabilities from design and industrialization through manufacturing, fulfillment and global delivery. 

Solstice Makes \$14B Play for Element Solutions

HOUSTON – Solstice Advanced Materials has agreed to acquire Element Solutions in a \$14 billion transaction that expands its portfolio of advanced materials for electronics, AI infrastructure and data center applications.

The combined company is expected to generate approximately \$6.8 billion in 2025 net sales. Solstice said the

acquisition will add Element Solutions' formulation technologies, technical services and customer relationships.

The company expects the transaction to generate approximately \$180 million in annual net synergies by the third year following closing. 

Kimball Electronics Acquires Helvoet

JASPER, IN – Kimball Electronics has acquired Helvoet Polymer Technologies, a Netherlands-based contract development and manufacturing organization specializing in highly automated micro-molding and precision injection molding for medical applications.

The \$103 million acquisition expands Kimball's medical manufacturing footprint in Europe and adds production facilities in India. Helvoet generated approximately \$56 million in revenue in 2025 and serves customers in the microfluidics, diagnostics and drug delivery markets.

Kimball said the acquisition strengthens its global medical manufacturing platform, creates opportunities for vertical integration and is expected to be accretive to fiscal 2027 adjusted earnings. 

Dymax Opens Mexico Distribution, Technical Center

QUERÉTARO, MEXICO – Dymax has opened a distribution and technical center in Querétaro, expanding support for customers throughout Mexico and Latin America.



Ribbon cutting ceremony celebrating the opening of the Dymax sales and distribution center in Querétaro, Mexico.

Located in Parque Terra Park Centenario in El Marqués, the facility provides local inventory, application testing, product development resources and technical support for regional manufacturers.

Dymax said the site will improve product availability, shorten lead times and strengthen support for customers in the medical device, automotive electronics and aerospace markets. 

Compeq Acquires Taiwan Site for HDI PCB Expansion

TAOYUAN, TAIWAN – Compeq Manufacturing has acquired a manufacturing site in Taoyuan's Guanyin Industrial Park for approximately \$64 million to expand production of advanced printed circuit boards.

The facility will support growing demand for high-density interconnect (HDI) PCBs used in optical networking, AI infrastructure, cloud computing and high-performance data center applications.

Compeq said the investment will increase manufacturing capacity and strengthen its ability to supply next-generation PCB technologies for high-speed communications markets. 

TTM Expands into Europe with Swiss, German PCB Acquisitions

SANTA ANA, CA – TTM Technologies is expanding its PCB manufacturing footprint into Europe through the acquisitions of Swiss Technology Group AG (STG) and Germany-based ILFA GmbH.

Expected to close in the third quarter, the transactions add PCB fabrication capabilities serving the aerospace, defense, medical and industrial markets. STG specializes in PCB technologies for surgical robotics, hearing aids, medical imaging and implantable devices, while ILFA manufactures complex printed circuit boards for high-reliability applications.

Separately, TTM is completing a \$130 million manufacturing facility in DeWitt, NY, that will produce ultra-high-density interconnect (UHDI) PCBs for US defense applications. 

FTG Opens Aerospace Manufacturing Facility in India

HYDERABAD, INDIA – Firan Technology Group (FTG) has opened a new aerospace manufacturing facility in Hyderabad, expanding production of high-technology printed circuit boards and electronic assemblies.

Operating as FTG Aerospace Hyderabad, the facility will manufacture PCBs and assemblies for aerospace applications, complementing the company's existing North American manufacturing operations.

FTG said the investment expands its global manufacturing footprint and provides additional capacity to support aerospace customers worldwide. 

MKS Atotech Expands Guangzhou Equipment Plant

GUANGZHOU, CHINA – MKS Instruments will invest \$25 million to expand the manufacturing facility of its MKS Atotech business in Guangzhou, doubling production capacity by late 2027.

The expansion will increase manufacturing, final assembly, logistics, testing and validation capabilities while supporting research and development and technical collaboration with customers.

MKS said the investment will strengthen support for semiconductor, advanced packaging and printed circuit board customers across Asia while incorporating solar power generation to improve energy efficiency at the site. 

PCD&F

Asahi Kasei expanded dry film photoresist production in Taiwan with a new slitting facility.

Schweizer Electronic and **Ascent Circuits** plan a strategic partnership to supply automotive and industrial PCBs.

SEMI and **TechSearch International** expanded the Worldwide Assembly & Test Facility Database to more than 820 back-end manufacturing sites. 

CA

Datalink Electronics installed a **Kolb** PSE LH5 cleaner.

Federal Electronics added automation, production space and testing resources.

Foxconn plans to anchor a new US-backed technology hub in the Philippines.

Incap Electronics Slovakia invested in manufacturing expansion.

Javad EMS installed a **Seho** PowerWave 3.0 wave soldering system.

Omron expanded its collaboration with **Nvidia** by integrating **Omniverse** and **Metropolis** technologies.

Parmi appointed **Cope Assembly Products** manufacturers' representative for Delaware, Maryland, West Virginia, Virginia, North Carolina and South Carolina.

Pillarhouse USA named **BarTron** manufacturers' representative in Indiana.

SmarTsol Technologies partnered with **iRayple** to expand autonomous mobile robot and machine vision solutions.

Test Research (TRI) appointed **Forwessun** exclusive UK distributor.

Vinyas Innovative Technologies secured an \$8 million order to manufacture and supply printed circuit board assemblies (PCBAs).

YJ Link reported a record \$25 million order backlog driven by AI data center demand. 

SIEMENS

AI-enabled electronic systems design

Xpedition

Harness one integrated flow from schematic to manufacturing-ready

HyperLynx

Ensure a first pass success with high-speed signal and power integrity analysis

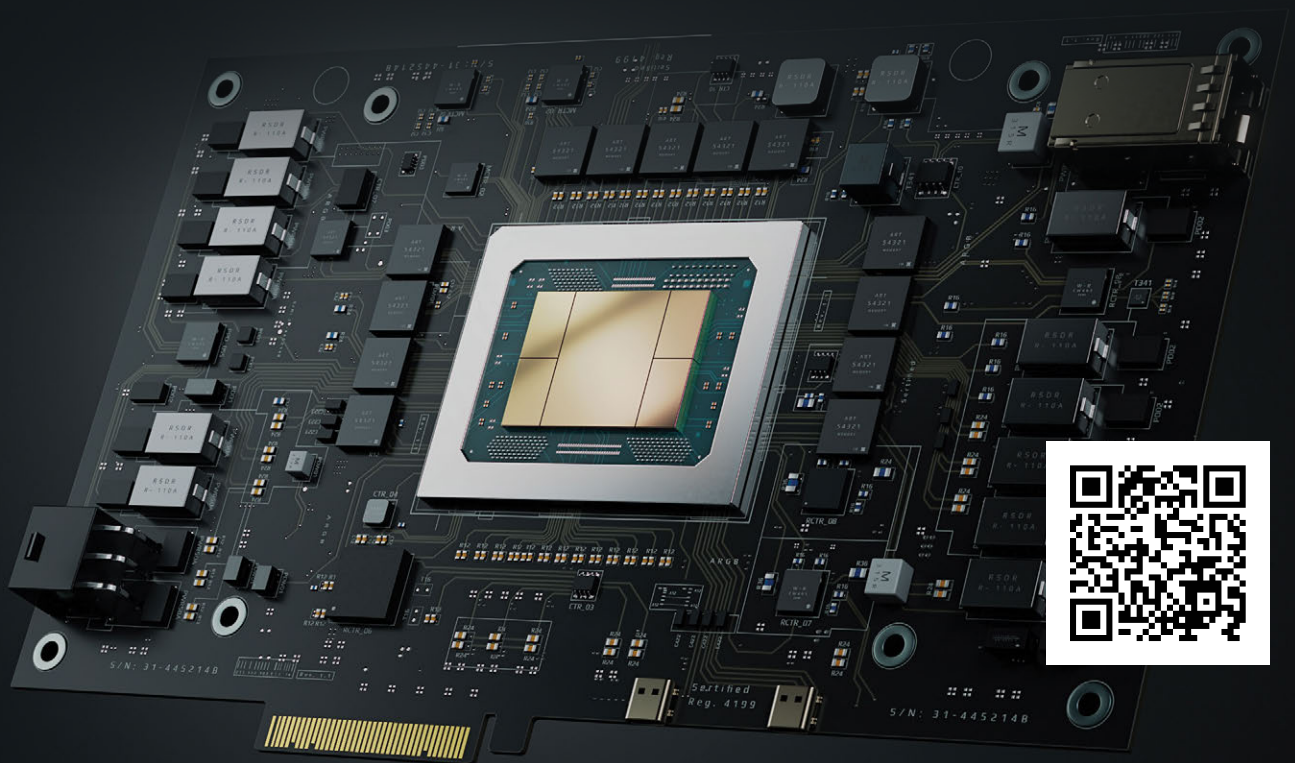
Valor

Bridge the gap with a digital thread from design to manufacturing

The #1 solutions provider for your most complex designs*

* Figure P 1, Pedestal Research, Feb 2025

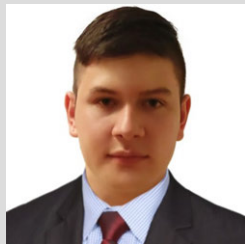
Come see us at
booth #405 at PCB West.



PCDF



Patrick York



Nicolás Arcila Potosí



Colin Warren



Dan Chirpich

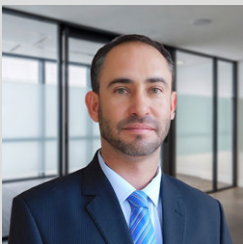
AdvancedPCB promoted **Patrick York** to general manager of its Chandler, AZ, manufacturing facility.

Joonik named **Nicolás Arcila Potosí** senior hardware design engineer.

Millennium Circuits promoted **Colin Warren** to director of quality following the retirement of **John Waite**.

Oxide Computer named **Dan Chirpich** electrical engineer – signal integrity. 

CA



David Solis

James Langan, Mike
Todd & Brian Andrews

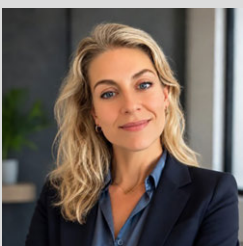
Steven Dorwart



Patrick Prondzinski



Mike DePauw



Laura Bouman



Heriberto Cuevas



Ramiro Mora



David Glagow



Kevin Castonguay



Brooke (Anglin) Downey



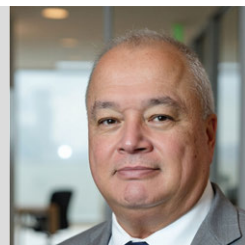
Shawn Myers



Huy Pham



Raul Jorge Lopez Jr.



Steve Dutton

AIM Solder has promoted **David Solis** to senior technical applications and laboratory support engineer.

Altus Group names **Brian Andrews** and **James Langham** field service engineers.

Celestica has appointed **Steven Dorwart** president of its connectivity and cloud solutions.

East West Manufacturing named **Patrick Prondzinski** vice president of sales.

Heller Industries named **Mike DePauw** senior key account manager.

Keiron Printing Technologies promoted **Laura Bouman** to head of people and culture.

Koh Young America has promoted **Heriberto Cuevas** to country manager for Mexico and South America.

Koh Young America promoted **Ramiro Mora** to service and applications manager for Mexico and South America.

Luminovo has promoted **David Glasgow** to customer success lead.

MicroCare has appointed **Kevin Castonguay** senior director of marketing.

MRS appointed **Peter Andries** as a business leader for its die bonding operations.

PCEA has named **Brooke (Anglin) Downey** vice president of sales to lead sales for its events, publications and digital media.

RBB appointed **Shawn Myers** engineering project manager.

ViTrox Americas appointed **Huy Pham** technical support engineer.

XLR8 EMS appointed **Raul Jorge Lopez Jr.** director of program management and procurement.

XLR8 EMS appointed **Steve Dutton** chief sales officer. 



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To learn more about our manufacturing processes download our latest whitepaper, "Key Areas to Audit When Selecting a Contract Manufacturer" at **www.axiomelectronics.com/ads**.

PCB West 2026 Show Floor Almost Sold Out

PEACHTREE CITY, GA – The exhibition floor space is almost sold out for this year's [PCB West](#), the largest exhibition and conference for printed circuit board design, fabrication and assembly in Silicon Valley.

Fewer than 5% of booths remain for the annual event. Last year marked the eleventh time in 12 years that all booths have been sold for the popular exhibition.

"We had a fantastic PCB West in 2025, and booth sales for our 2026 event have been strong," said Brooke Downey, vice president of sales, PCEA. "We're looking forward to another great event."



The show will be held Sept. 29 – Oct. 2, at the Santa Clara (CA) Convention Center. The event includes a one-day exhibition on Sept. 30.

This year's show will feature more than 110 exhibitors showcasing the leading companies in the PCB industry, including the top CAD and CAM vendors and top names in printed circuit fabrication and electronics assembly. Attendees will be treated to a free lunch on the exhibit floor during the exhibition on Sept. 30. 

Annual Designer Salary Survey Deadline Approaching

PEACHTREE CITY, GA – How are PCB designer salaries changing? Which ECAD tools are gaining ground? Are engineers happier in their roles than they were a year ago?

PCD&F's annual salary survey is now open, and we'd love to hear from you.

The survey covers salaries, job responsibilities, experience, education, job satisfaction and much more. The more responses received, the more meaningful the results are for the entire industry.

Take the survey here: <https://lnkd.in/gedBiUij>

Responses must be submitted by Aug. 7 to be included in this year's report. Individual responses are confidential. Only aggregated industry data are published. 

CIRCUITS ASSEMBLY Opens Entries for 2026 NPI Awards

PEACHTREE CITY, GA – CIRCUITS ASSEMBLY is accepting entries for its 2026 New Product Introduction Awards for electronics assembly equipment, materials and software suppliers.

Colloquially referred to as the Engineer's Choice Awards – a nod to the background and independence of the judges – the 20th annual NPI Awards recognize the leading new products for electronics assembly during the past 12 months. Recipients are selected by an independent panel of practicing industry engineers and are presented by CIRCUITS ASSEMBLY.



Registrations must be received at this link: pcea.net/npi-awards.

The categories include equipment, materials, software, training materials, and process innovation. To be eligible, entries must have been introduced to market (any region) no earlier than Jan. 1, 2026.

Entrants must submit a single registration form for each product and category entered. All entries must include a 250- to 1,000-word statement describing the product in the following terms:

- Creativity and innovation
- Compatibility with existing technology
- Cost-effectiveness
- Design
- Expected reliability
- Flexibility
- Expected maintainability/reparability
- Performance
- User-friendliness
- Speed/throughput.

The entry fee is \$500 per product. The deadline for entries is Dec. 4, 2026. For more information and to register, visit pcea.net/npi-awards.

The 2026 winners included: Adaptsys, Arch Systems, Austin American Technology, CalcuQuote, Data I/O, Fuji America, ITW EAE, Keiron Printing Technologies, KIC, Kurtz Ersä, Kyzen, SAKI, Seika Machinery, Sierra

PCB East 2027 Booth Sales Open for Returning Exhibitors

PEACHTREE CITY, GA – PCB East 2027 booth sales are now open for returning exhibitors and PCEA Gold and Platinum corporate members. The one-day exhibition will take place Apr. 28, while the four-day technical conference will take place Apr. 27 – 30.

All events will be held at the DCU Center in Worcester, MA.

Attendance at the PCB East 2026 conference and exhibition rose nearly 48% year-over-year. In all, more than 85 companies, including the top [CAD](#) and CAM vendors and leading names in component design, printed circuit fabrication and electronics assembly, exhibited at the show.



PCB East 2027 booth sales will be open on the following schedule:

- July 15: Booths open for 2026 exhibitors and [PCEA](#) Gold and Platinum members
- July 29: Booths open for 2026 exhibitors and [PCEA](#) Silver, Gold, and Platinum members
- August 12: PCB East booths open for all companies

“Today, the PCB East 2027 show floor is open to 2026 show exhibitors and [PCEA](#) Gold, Platinum and Silver corporate members for this exclusive period,” said Brooke Downey, vice president of sales, PCEA. “Then we will open it to any companies that want to exhibit at the electronics industry’s largest exhibition and conference in New England.”

Contact Brooke Downey at brooke@pcea.net for details or visit pcbeast.com. 

PCEA Names Brooke (Anglin) Downey VP of Sales

PEACHTREE CITY, GA – The Printed Circuit Engineering Association in July named Brooke (Anglin) Downey vice president of sales, responsible for sales of all the association’s events, magazines, newsletters, and related products.

Downey has a long history in event and advertising sales, as well as customer service, with PCEA and its predecessor, UP Media Group.

Downey served as exhibits sales manager with UP Media Group from 2004-08, responsible for exhibit and sponsorship sales for PCB East and PCB West. She later stepped into the role of senior sales executive for UP Media Group and PCEA from 2019-23, managing all print, digital and online advertising.



Brooke Downey

“Brooke’s personality and approach is customer-first through and through,” said Mike Buetow, president, PCEA. “She is exactly the person to drive our organization’s commitment to best-in-class trade shows and marketing content by listening to the customer and developing lasting relationships.”

“I’m thrilled to be back with the PCEA team,” said Downey. “I’ve missed the energy, the collaboration, and most of all, our customers! I’m excited to jump back in and keep delivering great work together.” 🧩

PCEA CURRENT EVENTS

ASSOCIATION NEWS

PCB West 2026 features over 50 classes and more than 120 hours of in-depth electronics engineering training on circuit board design and assembly. Rick Hartley, Karen Burnham, Susy Webb, Stephen Chavez, and Tomas Chester are among the headliners of this year’s conference. Those who sign up by Aug. 21 can take advantage of the early bird special discounts for the conference.

Certification. The following recently passed the PCEA [Certified Printed Circuit Designer](#) exam:

- Cori Nicholson

New Corporate Members

- [Weidmuller USA](#)

Networking. The PCEA Discord server brings together engineers and designers from around the world on a private channel to discuss technical questions and career opportunities. To join, contact [PCEA](#). Recent conversations covered standard operating procedures for ECAD, resume writing, and SMT wire to board connectors. 🧩

CHAPTER NEWS

National. Upcoming PCEA Training Certified Professional Circuit Designer (CPCD) training and

certification classes will be held:

- Sept. 4, 11, 18, 25, Oct. 9
- Sept. 28 – Oct. 2 (live abridged class, taught in-person in conjunction with PCB West)
- Oct. 16, 23, 30, Nov. 6, 13

Orange County, CA. We plan to hold a meeting the third week of August. The guest speaker is Juston Fleming of Livewire, and the topic is implementing accurate and standards-compliant footprints.

Portland, OR. The next meeting is tentatively scheduled for Aug. 20, from 12 – 1 p.m. Pacific. Speaker and meeting link to be announced. 

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TPCA: Forecast PCB Market by Following the CapEx

TAIPEI – Want to know where the PCB industry thinks it's headed? Watch where the money goes. Trace the capital spending of Taiwan's listed PCB fabricators over the past few years and the story writes itself: capex and industry health move in lockstep.

That's according to a new report from the Taiwan Printed Circuit Industry Association. From 2020 through 2022, pandemic-driven shortages and a run on electronics pushed output and capital spending up together. That was the last peak. Then came the hangover. In 2023 and 2024, with the channel choking on inventory and end demand limp, fabricators pulled in their horns and spending slowed hard.

Now the pendulum has swung back. Starting in 2025, AI demand lit the fuse, and capex is climbing again. The projection for 2026 is NT\$203 billion (\$6.2 trillion), an all-time high, according to TPCA.

Look at where that money is going and the shift is unmistakable. High-layer-count boards still take the biggest slice, riding demand for AI servers and advanced networking gear. ABF substrate lines are next, pulled along by AI chips. And HDI is getting its own push from AI servers and low-Earth-orbit satellites, sending manufacturers scrambling to stand up high-end lines and tighten their fine-line processes.

Here's the difference that matters. The 2020-era buildout was about capacity; more square footage, more panels. This wave isn't. It's about technology and high-end capability. In other words, the industry has stopped competing on scale and started competing on precision.

The map is changing too. The old playbook – R&D in Taiwan, mass production in China – is giving way to a three-legged strategy spanning Taiwan, China, and points abroad.

Overseas now commands the largest share of 2026 spending, roughly 44%, with Thailand the single biggest destination. China's slice has shrunk but still sits near 30%, and fabricators there keep pouring money into the high-layer-count and HDI capacity AI server demand. For all the talk of diversification, China remains Taiwan's production backbone. Taiwan itself takes about 26%, concentrated on substrate and high-layer-count capacity. Tellingly, Taiwan remains where the advanced R&D, leading-edge processes, and key technology upgrades live.

May Showers

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	MAR.	APR. ^r	MAY ^p	YTD
Computers and electronics products	0.7	0.6	0.6	6.8
Computers	2.0	-0.3	-1.6	17.6
Storage devices	0.3	1.5	2.6	12.9
Other peripheral equipment	4.1	9.1	-1.7	50.7
Nondefense communications equipment	1.8	1.1	3.5	23.7
Defense communications equipment	3.6	5.1	-3.2	0.7
A/V equipment	0.7	-1.4	-0.7	-9.5
Components ¹	0.9	0.7	-0.4	4.8
Nondefense search and navigation equipment	-0.4	3.2	-1.2	5.7
Defense search and navigation equipment	0.0	-0.2	2.5	13.1
Electromedical, measurement and control	0.3	0.6	-0.1	0.3

^rRevised. ^pPreliminary. ¹Includes semiconductors. Seasonally adjusted.

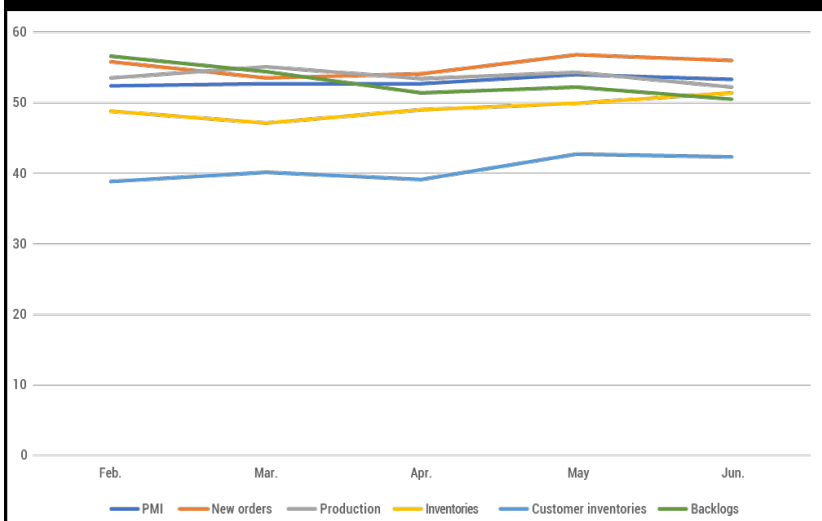
Source: US Department of Commerce Census Bureau, Jul. 6, 2026

Key Components

	FEB.	MAR.	APR.	MAY	JUN.
Semiconductors ^{1,3}	61.8%	79.2%	93.9%	104.1%	TBA
PCBs ^{2,3}	1.08	1.08	1.24	1.60	1.49
EMS ^{2,3}	1.32	1.29	1.36	1.36	1.33
Electronics mfg. orders ²	122.0	120.0	118.0	115.0	118.0
Electronics shipments ²	117.0	117.0	115.0	117.0	117.0
Component sales sentiment ⁴	139.7%	149.2%	146.6%	146.6%	154.1%

Sources: ¹SIA, ²GEA, ³3-month moving average, ⁴ECIA

US Manufacturing Indices



Source: Institute for Supply Management, Jul. 6, 2026

Quick Hits

Global **semiconductor sales** reached a record \$120 billion in May, rising 9% month-over-month and 104% year-over-year. (SIA)

The European Commission in July approved \$771 million in German state aid to support four **semiconductor manufacturing projects** under the European Chips Act.

The **global smartphone market** shrank 6.7% year-on-year to 277.5 million units in the second quarter. (IDC)

The **NAND flash market** has remained undersupplied throughout 2026, driven by surging AI-related demand and limited capacity expansion. In 2027, server demand is anticipated to stay strong. However, ongoing process migrations by suppliers, steady growth in bit output, and persistent weak demand in consumer electronics are likely to gradually restore market balance. Consequently, the current supply tightness is expected to diminish in the latter half of 2027. (TrendForce)

Global **smartphone shipments** will decrease 11% year-on-year in the second quarter, falling to their lowest second quarter level since 2013. (Counterpoint Research)

Global **semiconductor manufacturing equipment sales** will reach a record \$229 billion by 2028, up 23% year-over-year. (SEMI)

MLCC capacity utilization is forecast to remain heavily occupied by AI-related orders, extending lead times and increasing prices for high-end MLCCs in the second half of the year. (TrendForce)

The **global robotaxi market** will reach \$1 trillion by 2040. (Morgan Stanley)

India has eliminated import duties on a range of electronics manufacturing equipment and components in an effort to lower production costs and strengthen domestic electronics manufacturing through 2029. (The Next Web)

Worldwide **PC shipments** fell 4.9% year-over-year in the June quarter to 68.2 million units. (IDC)

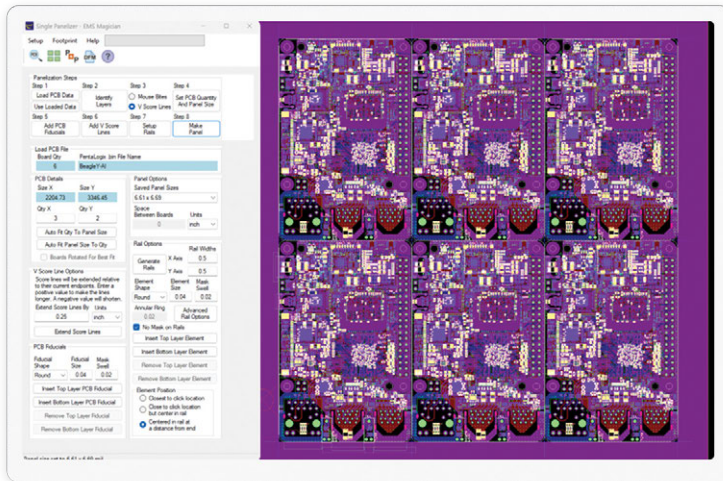
June **North American PCB shipments** rose 12% year-over-year but fell 18.5% from May. Year-to-date shipments are up 12.7%. Bookings climbed 31.5% from a year ago and fell 35.9% from May. Bookings are up 29% for the year. (GEA)

North American **EMS shipments** rose 6.7% in June from last year and 15.1% from May. For the year, shipments are up 7.4%. Bookings jumped 29.3% year-over-year and 6.6% from the previous month, and are up 5% for the year. (GEA) 



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Can Standards Keep Pace with Technology?

Standards organizations face growing pressure to develop reliable guidance quickly enough to support emerging technologies without compromising quality.

AS TECHNOLOGY CONTINUES to advance at an accelerating pace – turning what once seemed impossible into widely adopted reality almost overnight – it raises questions about how quickly future innovations will emerge. It also prompts consideration of whether this rapid development could eventually make standards impossible to develop in time for implementation or render them obsolete altogether.

It took decades for interconnections to evolve from wire-to-wire assemblies into printed circuits, then another decade to move from 12mil lines and spaces to 7mil. It took only about five years to advance from 7mil to 5mil, and then to 3mil. Clearly, the pace of technological development has accelerated, just as Gordon Moore's "Moore's Law" predicted. Today, technologies such as ultra-high-density substrates – so small they can barely be seen and unimaginable just a few years ago – are now commonplace in electronics. Along the way, organizations adopting these technologies sought assurance that they had been properly verified to perform as intended and validated to be manufactured consistently, even by different suppliers. This need gave rise to the development of industry standards, however.

The challenge is that developing a high-quality standard takes time. The process involves identifying critical failure modes, creating test vehicles, and determining the appropriate number of tests or cycles needed to verify the materials and processes used in the technology. It also requires assembling the right experts, conducting testing and analyzing the results. Standards can be developed more quickly today than in the past, however. The key question remains whether the process can be shortened enough to keep pace with the increasingly rapid development of new technologies.

Another complication is that, as technology advances more rapidly, companies increasingly view the technologies themselves – along with the materials and processes used to produce them – as proprietary information or intellectual property they are unwilling to share with standards organizations or competitors. In the past, collaboration was generally viewed as serving everyone's best interests. Today, many companies see new technology as a competitive advantage instead. As a result, the industry is often left to rely on a company's assurance that its technology will perform as claimed and will not negatively affect related technologies upstream or downstream.

Which brings us to the question: Why have standards in the first place? The answer is simple and important: to mitigate risk.

Risk takes many forms. The most important is safety. Products must not harm the people who use them, whether that

means preventing an appliance from causing a fire, ensuring a vehicle's brakes function reliably, or having confidence that an aircraft will take off, fly and land safely. Safety also includes ensuring the materials used in products do not pose health risks. Reducing these risks is one of the primary reasons strong industry standards are essential.

Financial risk is another important consideration. No manufacturer wants to face legal liability because a technology or component incorporated into its product failed. Using technologies produced to recognized standards significantly reduces that risk.

Risk also increases when a product or technology is available from only one source. Multiple qualified suppliers capable of producing the same technology with consistent quality and reliability reduce the likelihood of production disruptions for products that depend on those technologies.

Standards also create a level playing field, reducing risk for both customers and suppliers. Increased competition lowers costs, encourages innovation and expands adoption by making technology more affordable and delivering greater value.

As advanced technologies move from concept to production in ever-shorter timeframes, standards developers must find ways to reduce the time required to bring new standards to market. Risk again becomes the central issue. If creating a standard takes significantly longer than developing and widely adopting the technology it is intended to support, standards organizations must evaluate the efficiency of their own processes. Which steps are essential? Which add little or no value? Which consume the most time, and how can they be improved while still generating the information and data needed to produce effective standards?

Companies operating at the cutting edge – or even the bleeding edge – of technology development should have a strong interest in accelerating the standards process. These organizations, along with employees who contribute to standards development, should actively support efforts to shorten development timelines and work with standards bodies to create more efficient processes without compromising quality. Doing so benefits the entire industry, while providing the greatest advantage to the companies introducing the next generation of technologies. 



PETER BIGELOW has more than 30 years' experience as a PCB executive, most recently as president of FTG Circuits Haverhill; peterbigelow@msn.com.

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The “China Plus One” Reality Check for High-Mix, Low-Volume PCBs

For high-mix, low-to-medium volume PCB production, supply chain resilience depends as much on manufacturing ecosystems and engineering expertise as it does on geography.

IF ANYONE SITS in on enough supply chain meetings, it won't take long before the phrase “China Plus One” comes up. It has become the prevailing corporate mantra.

Driven by tariffs, geopolitical tensions and the lingering scars of pandemic-era supply chain disruptions, OEMs and EMS providers across North America and Europe are desperately looking for the exits. Many are pointing to Vietnam, Thailand, India and Malaysia and declaring a new era of diversified printed circuit board procurement.

On paper, it sounds good. But as someone who has spent decades navigating the bare printed circuit board market and connecting Western buyers with Asian manufacturing, I need to deliver a heavy dose of reality.

The truth is, PCB demand consisting of high-mix, low-to-medium volume parts often turns a move to a “Plus One” country into a one-way ticket to longer quote times and crippling lead times.

For commodity, high-volume manufacturing, the shift makes sense. When building millions of identical consumer devices, setting up a highly automated, low-mix facility in Southeast Asia is a viable strategy.

But the North American and European OEM landscapes are largely defined by industrial, medical, aerospace (non-ITAR) and specialized tech sectors. These industries thrive on high-mix, low-to-medium volume (HMLV) orders.

And for HMLV bare boards, China still reigns supreme. It isn't just about the factories; it's about the ecosystem. Understanding this distinction is the difference between a resilient supply chain and a localized catastrophe.

To understand why China Plus One struggles with HMLV, it's important to understand why China succeeds.

In regions like Shenzhen and the broader Guangdong province, manufacturers aren't just dealing with a solitary PCB fabricator. They are plugged into the densest, most highly evolved electronics manufacturing ecosystem on the planet. If a Chinese PCB factory runs out of a specific Rogers material or specialized solder mask, the supplier is literally down the street. If a drill bit breaks, the replacement is an hour away.

This localized infrastructure allows for unprecedented speed and agility. In the HMLV world, agility is everything. Manufacturers deal with frequent revisions, unique stackups and short production runs. Chinese manufacturers have

spent the last 30 years optimizing their front-end engineering (CAM) departments to process dozens, sometimes hundreds, of new part numbers every single day. Their engineers are adept at catching design flaws and issuing Engineering Questions (EQs) with lightning speed.

Now let's look at the Plus One destinations. Moving an HMLV portfolio to an emerging PCB region immediately sacrifices that infrastructure. A factory in Thailand or Vietnam might have brand-new presses and plating lines, but where do its raw materials come from? China. Where does its chemistry come from? China.

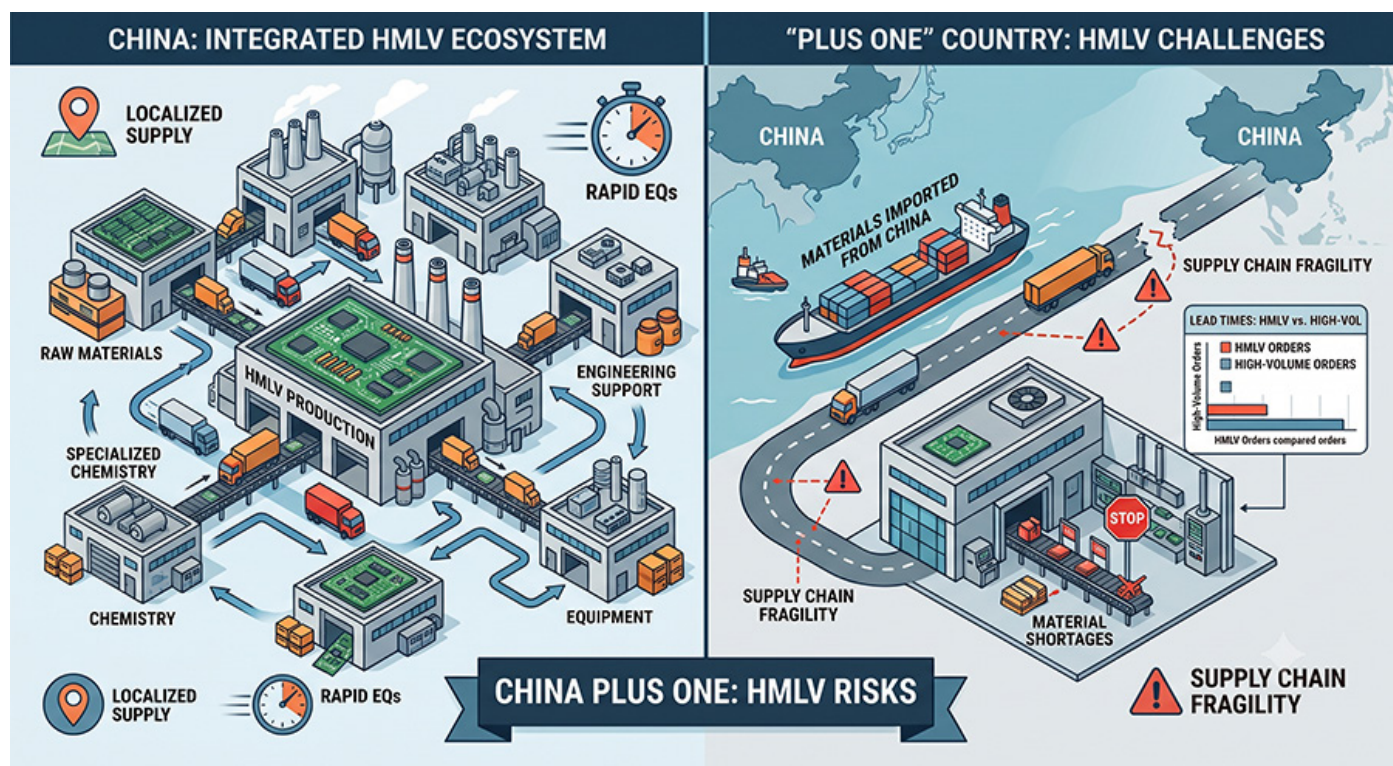


Figure 1. China's unmatched PCB manufacturing ecosystem continues to give it a significant advantage for high-mix, low-to-medium volume production despite growing interest in "China Plus One" sourcing strategies.

If a factory in a Plus One country experiences a localized shortage of a specific laminate required for a low-volume medical board, it cannot simply call a supplier down the street. It has to wait for a shipment from Shenzhen. Suddenly, a standard three-week lead time stretches to six or eight weeks.

And the infrastructure gap isn't just about material logistics; it deeply impacts quality and problem-solving.

In a high-mix environment, mistakes happen. Boards fail testing, yields drop or a plating issue ruins a panel. In China, if a batch of 50 boards is scrapped on a Tuesday, the factory can pull new material from local stock, expedite it through the line and still make the Friday shipment.

In a newly established Plus One factory, a scrapped batch is a full-blown crisis. If buffer stock of a specific material isn't available—which is rarely the case for low-volume mix—the factory has to reorder from overseas suppliers. A simple manufacturing hiccup cascades into a month-long delay.

Furthermore, the CAM and front-end engineering talent in these emerging regions is often geared toward high-

volume, low-mix production. These operations are built to set up one job perfectly and run it for a month. Present them with 20 different part numbers requiring rapid tooling, and their front-end departments choke. EQs are missed, assumptions are made and the result is bare boards arriving on the dock with glaring defects.

As a broker, I have watched EMS companies pull their high-mix spend out of China to avoid a 25% tariff, only to lose far more money dealing with scrapped boards, missed OEM delivery dates and idle assembly lines because their new Plus One supplier couldn't handle the mix.

And then there are freight issues. The transportation systems in many of those nations are not as mature or seamless as they are in China.

Funny story: On one of my recent visits to Thailand, I visited several EMS companies hoping to discover board houses producing HMLV locally. When I asked where they sourced those bare boards, the unanimous response was, "Oh, from China."

So if fleeing to a new geography isn't the silver bullet for HMLV boards, what is the solution? The answer is to stay in China (or established hubs like Taiwan) while managing the supply chain with far greater sophistication.

Instead of fleeing tariffs, consolidate and negotiate existing spend more strategically. By consolidating HMLV spending with a specialized broker or directly with a carefully vetted factory, companies can negotiate better base pricing that often offsets the cost of tariffs.

There's no need to cross borders to diversify. China is massive, making internal diversification entirely possible. If regional lockdowns or localized power grid issues are a concern, qualify factories in different provinces. Maintain a primary supplier in Guangdong and a qualified backup in Jiangsu.

Don't just audit a factory for its equipment; look deeper into its supply chain. Ask Chinese suppliers where their materials come from and how much local buffer stock they maintain. Ensure they are financially stable enough to survive economic headwinds.

The desire to mitigate risk is understandable, but true risk management requires looking past the buzzwords. Moving high-mix, low-to-medium volume bare PCB production out of China today often means trading a manageable geopolitical risk for guaranteed operational failure.

Until the Plus One countries build out the dense, localized infrastructure and deep CAM engineering talent pools that China has spent decades perfecting, they will remain ill-equipped to deliver the agility HMLV products require. Rather than chasing the latest trend, the smarter strategy is to embrace the realities of the PCB ecosystem and build stronger, more direct relationships where the infrastructure already exists. 



GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as the founder of a leading distributor. He is cofounder of DirectPCB (directpcb.com); greg@directpcb.com.

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Leadership Lessons from the Horse's Mouth

Leadership, mentorship and continuous improvement go hand in hand, both in the dressage arena and on the electronics manufacturing floor.

ONE OF MY [most popular articles](#) last year was focused on leadership lessons my mare was teaching me. Prim is still delivering teaching moments, so I thought it was time for another column.

The journey we've had this past year is distinctly different from last year because we've moved from the forming, storming and norming stages of team formation into a well-functioning team. That point really got driven home at our last show in Scottsdale, when a judge who scored us at 47 last year at the same show gave us two 66s on more difficult tests. In the warm-up ring before those tests, I was thinking about how different the warm-up ride felt because the dynamics that had been sabotaging our previous show weren't present. What changed? There were several things:

We practice precision. Precise, repeatable geometry is important in dressage just as repeatable processes are important in the EMS. Last year, we were like a production team that does stuff on the fly and course corrects when the test department sees a spike in defects. This year, we focused on eliminating all variation from our process, studying video to make sure we hit the correct marks every time. This analysis showed me that my memory of the test was faulty and we were transitioning late at two points in tests. Now, instead of assuming my memory is good enough, I review my test geometry before every test. The parallel in the EMS world is DfX and NPI checklists.

I pay attention to team quality of work life. Prim is an integral part of my team, and while she can't talk, watching her behavior tells me what is and isn't working. She worked better on the simpler bit my trainer was using with her than on the bit I'd chosen, so we switched bits and had better connection. She also was pawing more at competitions as we were tacking up, so I switched supplements to improve her gut health while traveling. The pawing stopped. The parallel in team building is listening to the team's preferences for meeting process design, tracking system integration and frequency. Creating a stress-free environment goes a long way in developing a well-functioning team.

We respect each other. I've had Prim for two years now. She has tested me, and most of the time I've passed. I've also set expectations on appropriate work behavior and reward good behavior. The result is that we both know our roles in the dressage court, and we work well together. Work teams need the same elements: mutual respect, boundaries, goals and rewards.



Figure 1. Experiences with dressage horse Prim highlight leadership lessons that translate directly to building stronger EMS teams.

There is one other lesson I learned in my journey this year that I think is worth sharing. Last year, I was the only person riding Prim. This year, I've been mentoring a junior rider who was cleaning stalls to afford lessons at our barn. This process paid two dividends.

First, I got the joy of watching a really talented and hard-working equestrian live her dream at regional competitions on Prim. Second, the exposure to a second rider was great for Prim. It gave her variety and broadened the disciplines we are working on, because both the junior and Prim enjoy hunter classes, as well as dressage. Sadly, I no longer bounce well enough to do much jumping.

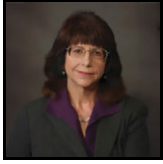
These lessons didn't stop at the barn. The junior wanted to shadow me at work as she starts college in the fall (with a four-year equestrian team scholarship) and is exploring majors. We spent a day discussing my consulting business and the EMS industry. One of her biggest concerns was choosing a career that AI wouldn't negatively impact. One of the career fields we discussed was EMS program management.

While I believe we will see AI and automation increase significantly in the EMS industry, including in program management, I also think the customer-facing role of most EMS program managers will remain necessary.

A few weeks after our shadowing session, she came up to me in the barn and told me she'd been studying program management roles in more detail. She'd decided she needed to get a Scrum Master certification because Scrum Masters made more than program managers, and if she was going to afford a horse later in life, she was going to need to make a lot of money. I love seeing a young person think through career strategy at that level.

She also plans to seek out summer internships and work-study opportunities to both test whether her career plans

make sense in terms of work-life quality and build the relationships she needs to be employable once she gets a degree. She'll be a success in whatever she decides to do because she has the intelligence, focus and work ethic to succeed. In many ways, being her mentor this year was the most fulfilling part of my journey with Prim. I highly recommend finding a young person to mentor. The EMS industry needs to be recruiting the next generation before they go to college. 



SUSAN MUCHA is president of Powell-Mucha Consulting Inc. (powell-muchaconsulting.com), a consulting firm providing strategic planning, training and market positioning support to EMS companies and author of *Find It. Book It. Grow It. A Robust Process for Account Acquisition in Electronics Manufacturing Services*. She can be reached at smucha@powell-muchaconsulting.com.

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-Peter Lynch

*successful trader
also really rich,
fluffy white hair*



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PCBAA at 5: Bigger, Better and Facing a Deadline

Why shouldn't "China Plus One" include the US?

THE PRINTED CIRCUIT Board Association of America is celebrating its fifth anniversary this year, having grown from five founding fabricators to more than 90 members spanning the full ecosystem – raw materials, fabrication, assembly, design and OEMs – including recent additions Neros, Trace and Zenode.

Executive Director David Schild credits the growth with expanding PCBAA's footprint on Capitol Hill from five congressional relationships to a presence across 36 states.

The group's most pressing near-term priority is Section 851, the five-year-old mandate to purge Russian, Iranian, North Korean and Chinese PCBs from dual-use and COTS applications in Pentagon supply chains. With implementation set for January 1, 2027, the public comment period runs through August 31, and PCBAA is pushing members to weigh in against any delay or dilution.

Schild points to the Department of War's new "Rebuilding the Arsenal of Freedom" [investment map](#), which highlights DPA-funded HDI/UHDI facilities in Calumet, MI; Charleston, SC; and Eau Claire, WI. Longer-term, he's framing the fight in market-share terms: US PCB share of global market value has fallen from 30% to 4%, and PCBAA believes that sound policy can reverse it.

Schild also warns against complacency about "China Plus One" diversification, noting that Malaysia, Thailand and Vietnam are courting manufacturers relocating from China more aggressively than the US. Why shouldn't Santa Ana, CA, or Camden, SC, become the Plus One?

A Domestic-Facing Mission

Indeed, domestic supply chain resiliency is fundamental to the PCBAA's mission, which includes rebuilding US PCB and PCBA capacity, restoring capability, and returning strategic independence.

PCBAA is pursuing this through policy advocacy, industry messaging, and support for domestic investments and partnerships. The organization is bending the curve of the North American electronics manufacturing trajectory.

Those interested in learning more should visit pcbbaa.org. 



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RF PCB Layout: Transmission Lines, Impedance and PDN Design

Analog PCB design demands careful attention to power delivery, bypass capacitor placement and impedance control to ensure accurate sensor performance in increasingly compact electronic systems.

THE WORD “ANALOG” has a special connotation in the PCB design world. One of the things that comes to mind is that we measure performance on a linear scale. A specification may call for 100dB of isolation, but achieving even greater isolation is always desirable. The Internet of Things (IoT) could just as easily be called the Internet of Analog Things.

This article will discuss the following:

- How the power delivery network affects analog circuits
- Bypass capacitor placement and routing
- Managing impedance requirements against manufacturability concerns

Sensors come in every flavor under the sun. Measuring heat, light, pressure and anything else in the spectrum falls under the analog umbrella. The smart watch that takes your pulse while sending and receiving radio transmissions from your phone is a good example. The tiny volume of a watch makes it an RF Thunderdome.

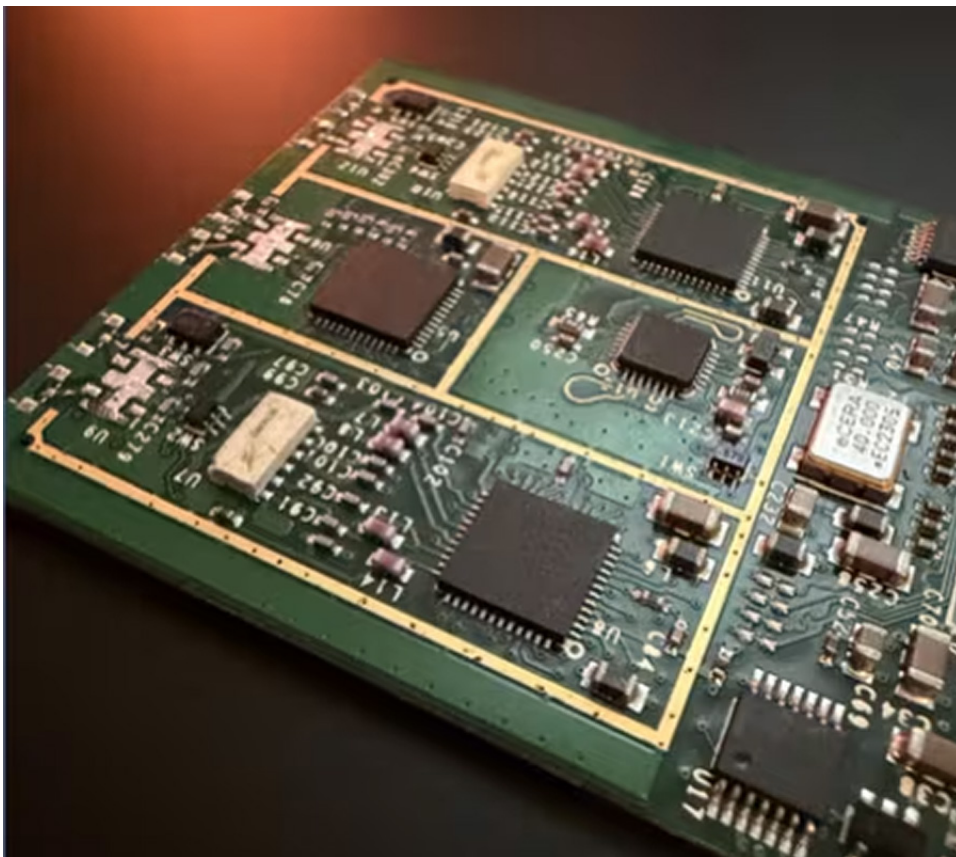


Figure 1. Shields within a shield provide for signal integrity for analog blocks. (All images courtesy of author)

One of the greatest challenges in these compact devices is supplying power to the integrated circuits. The process is highly iterative, reducing the power delivery network (PDN) to only what is necessary. Even when additional space is available, excess copper in the power planes can act as an antenna. The design process becomes an exercise in trimming away unnecessary copper to lower the noise floor on transmission lines. Precise power delivery is a hallmark of successful analog design.

A humorous sign once displayed outside a test engineer's cubicle read, "Relax, it's all just a bunch of ones and zeroes." The irony was that the work centered on analog integrated circuits. Board bring-up in the test lab often provided valuable insight into layout decisions, highlighting both successful design choices and areas requiring improvement.

Star routing for the power delivery network. Well-documented schematics play an essential role in analog PCB layout. Detailed notes from the electrical engineer help guide placement and routing decisions. Identifying which components belong within specific shielded areas simplifies placement, while assigning individual bypass capacitors to specific power pins instead of only identifying voltage rails improves routing accuracy.

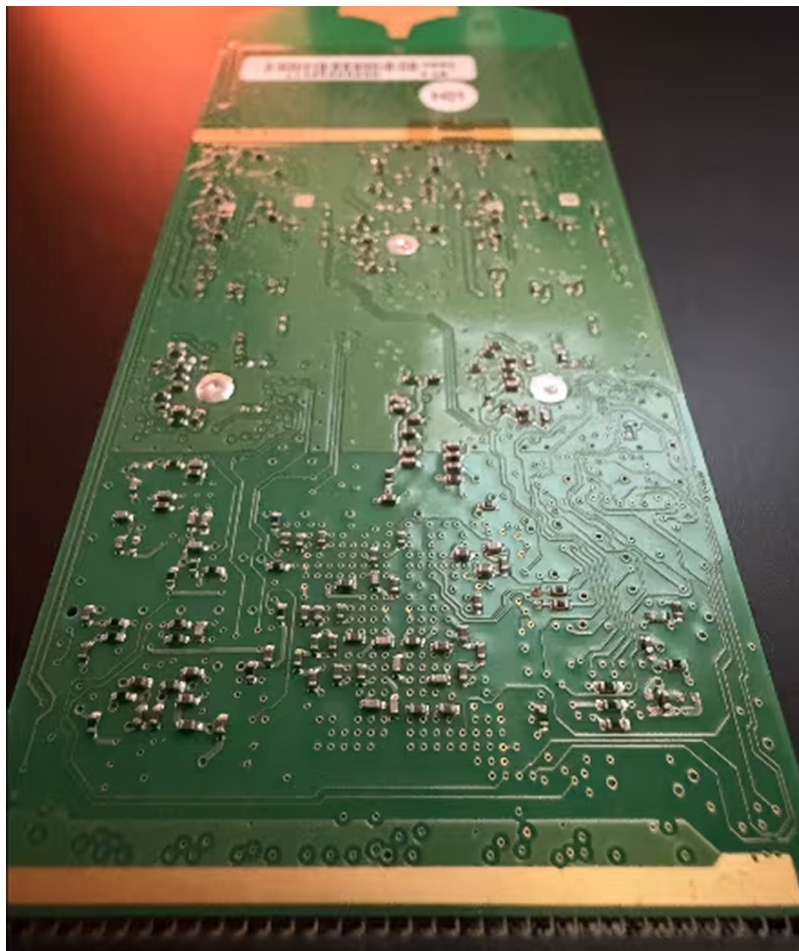


Figure 2. Capacitor placement lends itself to short inductive loops ahead of uniformity of rotation angle.

In some cases, proximity alone is not sufficient. A wide trace may be required to feed the capacitor, followed by a short, narrow connection from the capacitor to its assigned power pin. Multiple pins may share a single capacitor, or several capacitors may be assigned to one pin. Highlighting individual capacitor-to-pin assignments is often more effective than simply color-coding voltage nets.

Although not originally intended for this purpose, the Net Schedule function can also be used to associate bypass capacitors with specific voltage pins. Its primary application is routing emitter coupled logic (ECL), where termination resistors must connect to designated locations. The same approach ensures that moving a capacitor maintains its connection to the intended power pin rather than automatically snapping to the nearest one.

Impedance control – the crux of analog design. Much of analog PCB design revolves around maintaining controlled impedance. A 50Ω transmission line remains the industry standard for many RF applications. Stripline geometry is commonly implemented on the outer layers, where impedance depends primarily on trace width, dielectric thickness and the dielectric constant (Dk) of the laminate material. As a rule of thumb, selecting a trace width approximately equal to the dielectric thickness provides a reasonable starting point before refining the design through calculation.

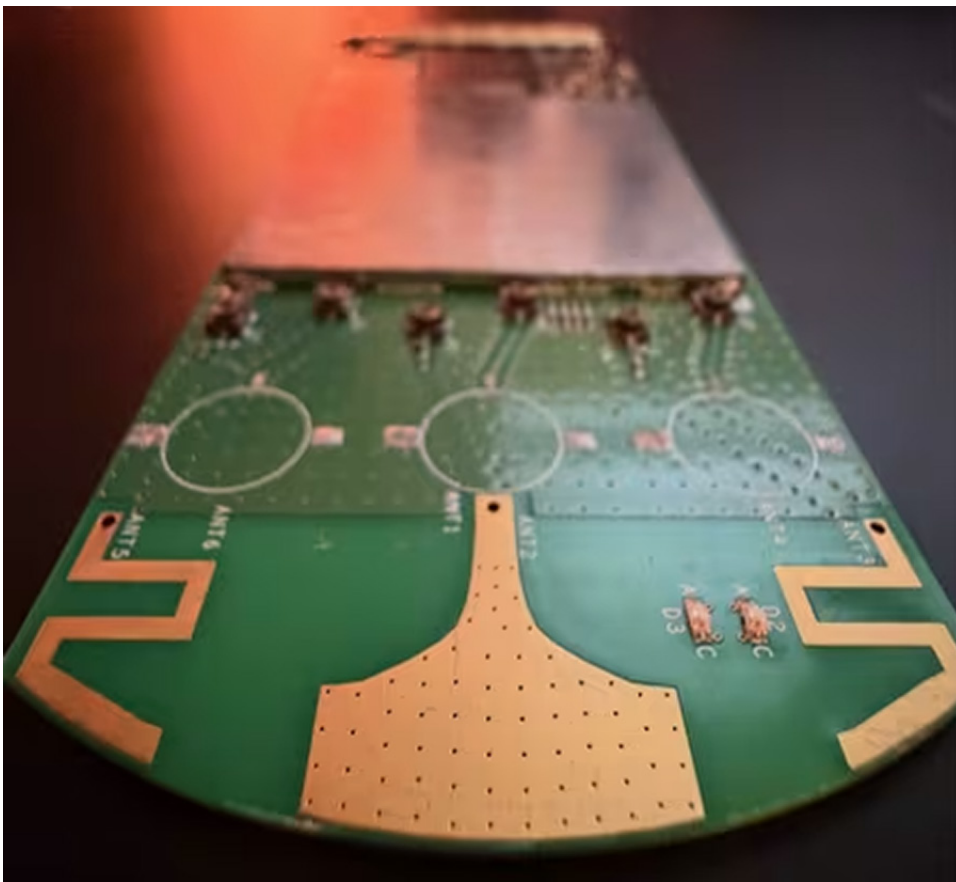


Figure 3. WiFi MIMO printed antennas. The silkscreen circles once had little metal antennas installed.

According to IPC-4101/21, FR-4 has a nominal dielectric constant of approximately 5.4, although the actual value varies by manufacturer and changes with temperature, copper roughness and operating frequency. Standard FR-4 performs well into the 5GHz range in many applications. Beyond that point, lower-loss materials generally become necessary because FR-4 exhibits increasing dielectric loss at higher frequencies.

Impedance mismatch – the bane of signal integrity. Any discontinuity along an RF signal path deserves careful attention. While outer-layer routing is generally preferred for analog signals, placement always dictates the routing strategy. Wherever possible, routing length should be minimized through thoughtful component placement.

The ideal layout places the RF input connector immediately adjacent to the DC blocking capacitor, followed closely by the matching network, typically implemented as a pi network. The amplifier, coupler or subsequent circuit should then connect using the shortest, straightest possible trace with minimal spacing between components.

When additional transmission-line length cannot be avoided, every effort should be made to minimize it through improved placement. Ideally, the components themselves occupy most of the signal path. Excess routing should be avoided because every exposed trace has the potential to radiate energy at the operating frequency and its harmonics.

Considering the trace versus pad width. The PCB stackup can be engineered to support wider controlled-impedance traces. Ideally, trace width closely matches the pad width of common RF components. For example, a pi network constructed with 0201 resistors is best served by a trace width of approximately 0.35mm to match the

component pads. Boards using plated through-hole vias typically require a dielectric thickness between 0.3 and 0.4mm from the outer layer to Layer 2.

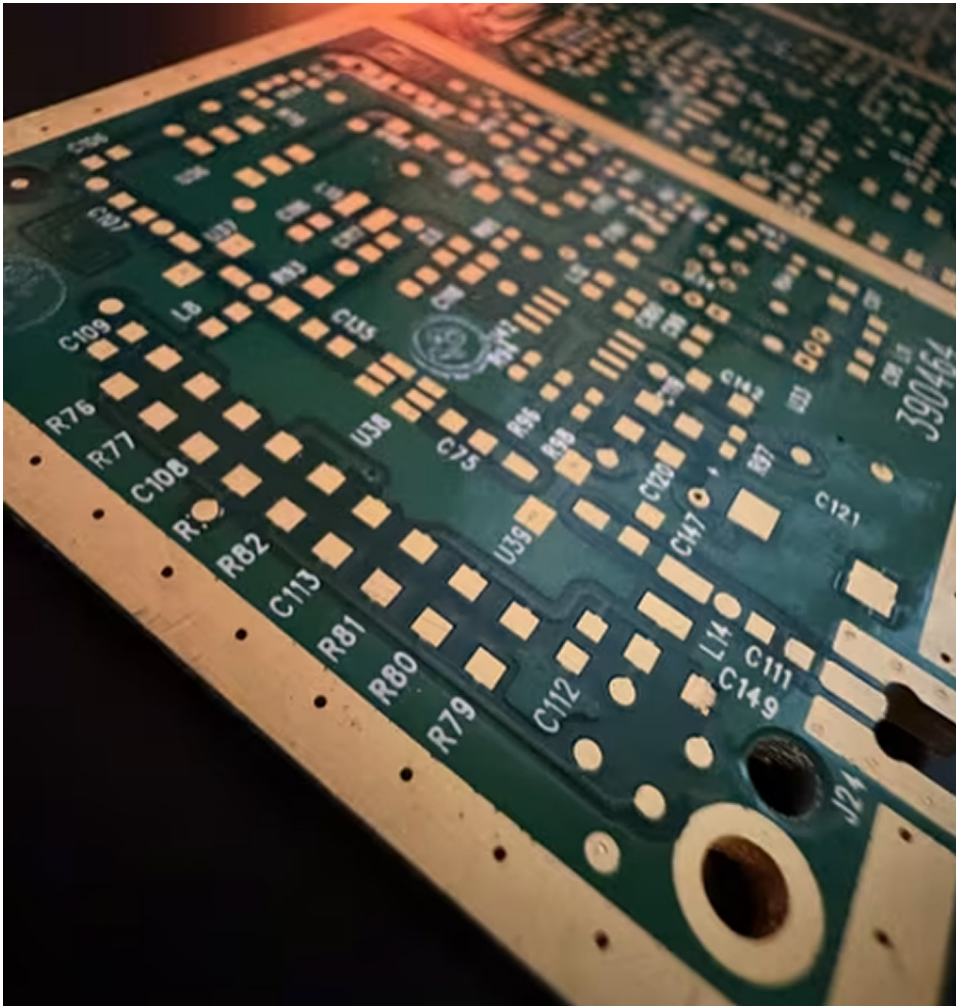


Figure 4. The RF transmission line from J24 (lower right) flows straight and is only stretched enough to allow for in-circuit test points. Line width matches the component pads.

HDI designs introduce additional complexity. Microvia dimensions dictate dielectric thickness because of laser-drilled via aspect-ratio limitations. If Layer 2 lies only 50µm below Layer 1, maintaining manufacturable trace widths may require clearing Layer 2 beneath the RF trace and instead using Layer 3 as the reference plane.

This routing strategy has been successfully applied in several high-density consumer electronics designs. If Layer 2 remains the reference plane, the resulting trace width may become too narrow for conventional PCB fabrication. Manufacturing would then require extremely thin starting copper and minimal via plating, reducing overall manufacturing robustness and long-term reliability.

Where coplanar waveguides are used. At some point, the transmission line may need to transition into the PCB as a microstrip. Every via introduces an impedance discontinuity that must be carefully managed. One proven approach transitions from stripline to a coplanar waveguide immediately before the signal via.

A coplanar waveguide helps maintain impedance through the transition region surrounding the via, particularly where the reference plane has been cleared around the plated hole. Instead of relying solely on the reference plane beneath the trace, the coplanar waveguide uses grounded copper adjacent to the signal trace to maintain field containment.

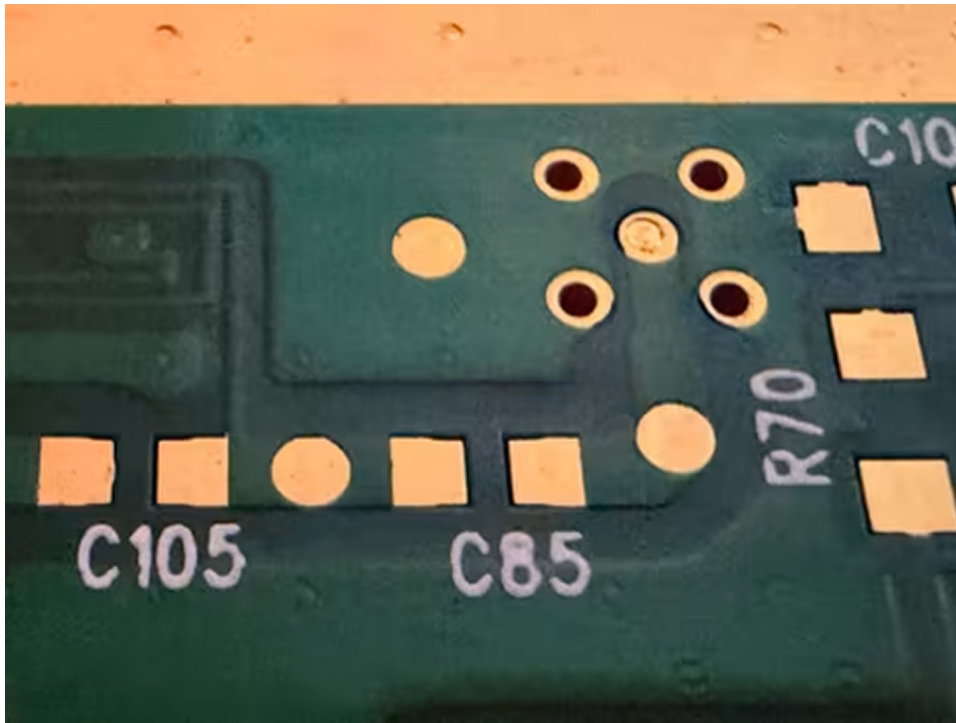


Figure 5. On the right-hand side, the stripline narrows while the ground plane closes in to create a CPWG before transitioning to an inner layer so as to cross under the shield. The left shows a printed inductor from RF to GND.

Integrating an antenna directly onto the PCB introduces another level of complexity. All copper beneath the antenna should be removed, while multiple rows of stitching vias should surround the antenna region. Staggered rows of interstitial vias, typically three or four rows deep, provide effective isolation. Analog circuits present unique design challenges, but careful layout practices can successfully control their performance. 



JOHN BURKHART, JR. is a principle PCB designer in retirement. For the past several years, he has been sharing what he has learned for the sake of helping fresh and ambitious PCB designers. The knowledge is passed along through stories and lessons learned from three decades of design, including the most basic one-layer board up to the high-reliability rigid-flex HDI designs for aerospace and military applications. John's well-earned free time is spent on a bike, or with a mic doing a karaoke jam.



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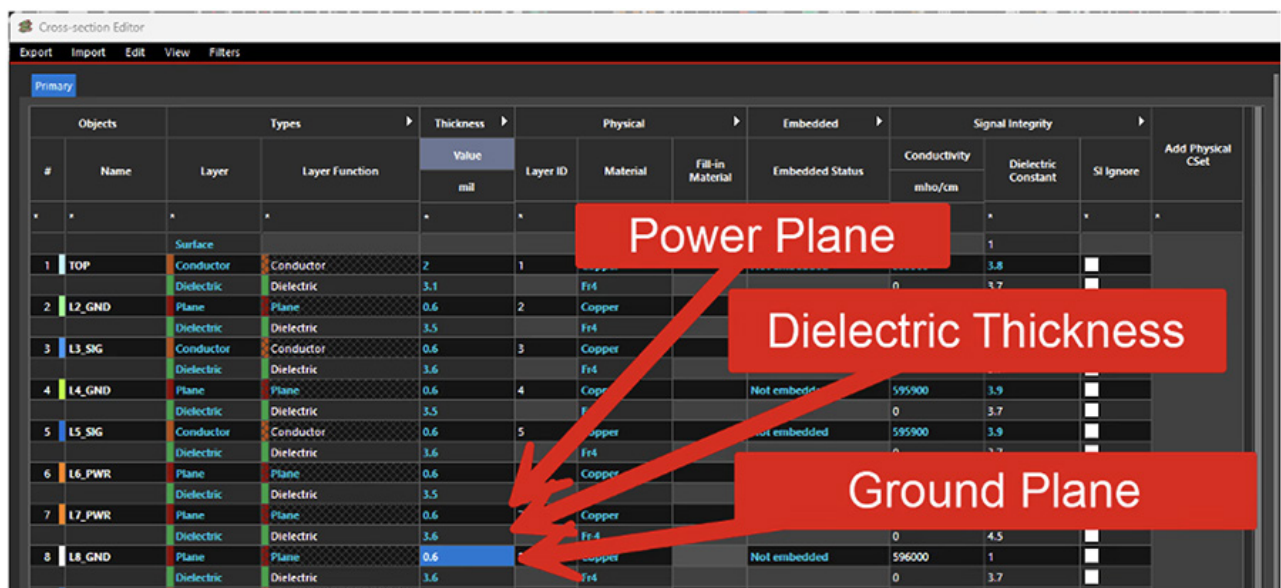
PCB Power Integrity Analysis: Why PDN Behavior is a Geometry Problem

Designing a reliable power delivery network takes great layout skills, as well as a solid understanding of geometry.

A **VOLTAGE REGULATOR** outputs 1.0V. The integrated circuit (IC) needs 1.0V within 3 percent. Somewhere between them, the voltage drops, or worse, the voltage rings.

The question is not whether the regulator works. The question is what the copper does to the power delivery path between the regulator and the IC.

Plane pair capacitance. When a power plane sits close to a ground plane, the two form a capacitor. The capacitance depends on three things: the area of overlap, the dielectric constant of the material between them, and the thickness of that dielectric.



Cross-section Editor												
Export Import Edit View Filters												
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Objects		Types		Thickness	Physical			Embedded	Signal Integrity			Add Physical CSet
#	Name	Layer	Layer Function	Value mil	Layer ID	Material	Fill-in Material	Embedded Status	Conductivity mho/cm	Dielectric Constant	SI Ignore	
		Surface										
1	TOP	Conductor	Conductor	2	1	Copper				3.8		
2	L2_GND	Plane	Plane	0.6	2	Copper				3.7		
		Dielectric	Dielectric	3.5		Fr4						
3	L3_SIG	Conductor	Conductor	0.6	3	Copper						
		Dielectric	Dielectric	3.6		Fr4						
4	L4_GND	Plane	Plane	0.6	4	Copper		Not embedded	595900	3.9		
		Dielectric	Dielectric	3.5		Fr4			0	3.7		
5	L5_SIG	Conductor	Conductor	0.6	5	Copper		Not embedded	595900	3.9		
		Dielectric	Dielectric	3.6		Fr4			0	3.7		
6	L6_PWR	Plane	Plane	0.6		Copper						
		Dielectric	Dielectric	3.5		Fr4						
7	L7_PWR	Plane	Plane	0.6		Copper						
		Dielectric	Dielectric	3.6		Fr4			0	4.5		
8	L8_GND	Plane	Plane	0.6		Copper		Not embedded	596000	1		
		Dielectric	Dielectric	3.6		Fr4			0	3.7		

Figure 1. Adjacent power and ground planes form a distributed capacitor. Reducing dielectric thickness increases capacitance per unit area, extending PDN effectiveness into higher frequencies.

A thin dielectric means more capacitance per unit area. That capacitance works at frequencies where discrete decoupling capacitors run out of usefulness. A typical ceramic capacitor becomes inductive above a few hundred megahertz. Plane pair capacitance keeps working well past that point because the current path is short and wide instead of long and narrow.

The cross-section editor in [Allegro X PCB Layout](#) sets this spacing for you. Place your power plane and ground plane on adjacent layers. Specify the dielectric thickness. That single decision, made early in the design, sets the distributed capacitance for the entire board.

Cavity resonance and plane geometry. Parallel plane pairs do not just store charge. They behave as cavity resonators. The plane edges reflect electromagnetic energy back toward the center. At specific frequencies, the reflections add in phase and the cavity rings.



Figure 2. PDN impedance vs. frequency showing multiple cavity resonances. These peaks are driven by plane dimensions, dielectric spacing, and via distribution. Not regulator performance.

The first resonance frequency is approximately the speed of light divided by twice the longest plane dimension times the square root of the dielectric constant. For a 4-inch plane dimension with a dielectric constant near 4, the first resonance falls near 740MHz. At that frequency, the plane impedance spikes. Any via that penetrates the plane pair at a resonance hotspot couples that noise into whatever signal the via carries.

Complex high-speed PCBs often have several power rails with large plane areas. Each one has its own set of resonance frequencies set by its shape. At this stage of the PCB design, power integrity is no longer just a component-level concern; it becomes a system-level interaction between geometry and frequency behavior.

Sigrity X Aurora can compute those resonances and show you a heat map of where they peak on the board. The following results are generated from a representative demonstration layout to illustrate how plane geometry shapes PDN behavior.

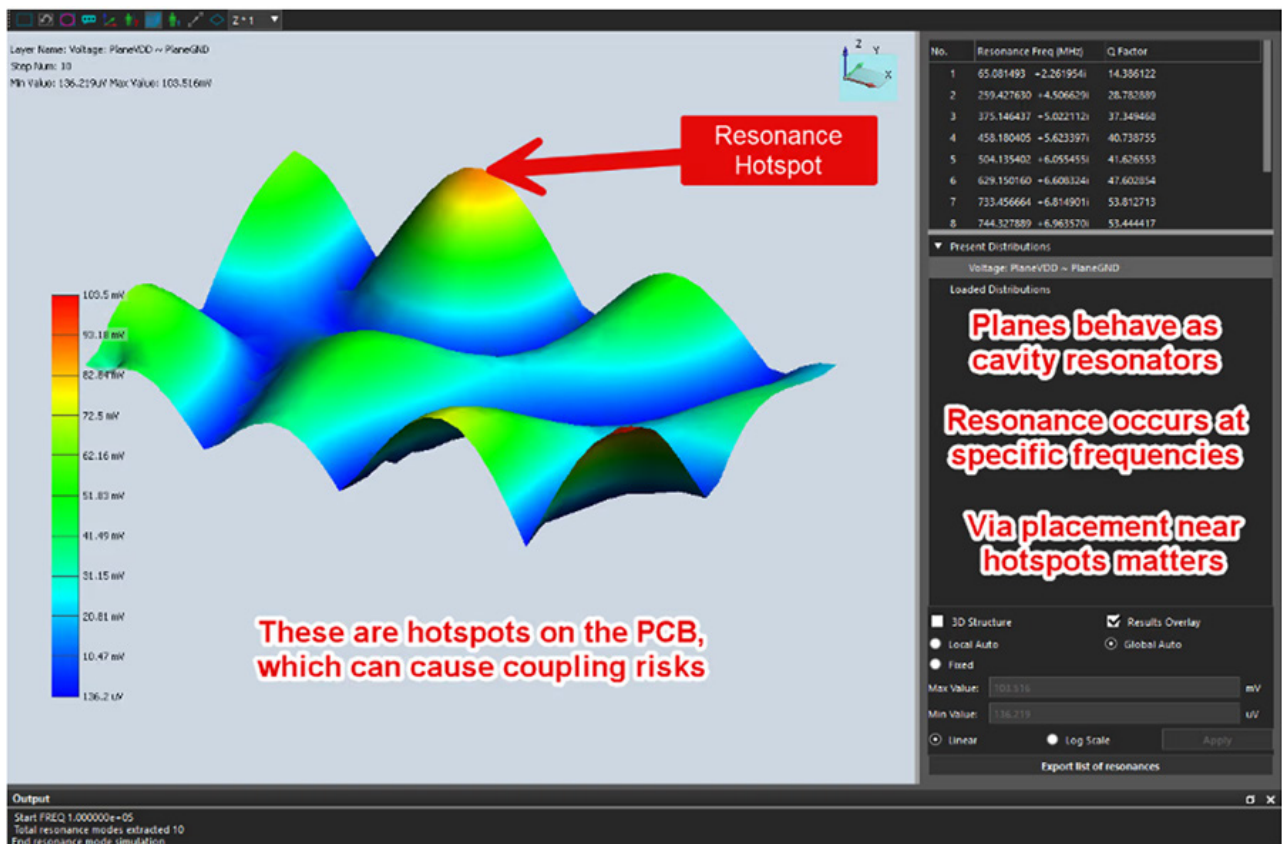


Figure 3. Resonance mode of a power-ground plane pair at a specific frequency. The spatial distribution reveals geometry-driven hotspots where noise coupling is strongest.

Those hotspots are where you do not want to place sensitive analog lines or high-speed serializers.

Stitching vias break the cavity. A stitching via ties a power plane to its ground plane reference. Each stitching via locally reduces the impedance between the power and ground structures, altering the cavity current distribution and suppressing resonant behavior. Many stitching vias, distributed across the plane, suppress cavity resonances by lowering the structure's Q factor and reducing the size of uninterrupted resonant regions.

This is geometry, not component selection. You do not buy low-resonance vias. You place more of them in the right locations. The locations that matter most are near every signal via that transitions between layers. When a signal via penetrates the power and ground planes, the electromagnetic wave has to make the same transition. The nearest stitching via is where that wave's other half couples to its nearest lowest impedance conductor and voltage reference.

If the nearest stitching via is far away, the electromagnetic waves traverse any and all PCB surfaces and dielectric material it needs to, to find its reference voltage. All conductive materials along that path have their electrons excited, thereby forming an incident current path. A large path has more inductance. More inductance means more voltage drop at the return transition. That voltage drop is the noise on your PDN.

Putting it together on any complex high-speed board. On a typical multilayer PCB, the highest-current rails span large plane areas. Without sufficient stitching, these planes can resonate in the hundreds of megahertz range, well within the spectral content of modern switching loads.

Run PDN impedance analysis on the layout database. Look at the impedance as a function of frequency. Look for peaks. Peaks are resonance. The goal is to keep PDN impedance below the target across the load's operating frequency range. When impedance exceeds the target, transient current demand converts directly into voltage ripple on the power rail. Correlate the peak frequencies to plane dimensions. Then place stitching vias to break up the largest cavities.

The visual payoff is immediate. Before: impedance peaks near the resonance frequencies. After: the peaks flatten. The PDN maintains lower impedance and reduced voltage ripple across the frequency band your signals care about, improving overall power distribution.

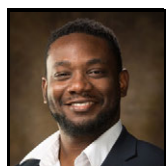
The geometric controls in order. Power integrity comes from three geometric choices, in this order of influence:

First, the PCB stackup. Closer plane pairs, thinner dielectric, more distributed capacitance. The cross-section editor sets this once, and it affects the whole board, making it one of the most critical steps in the design process.

Second, the plane shape. Long, narrow planes resonate at lower frequencies than short, compact planes. Cutouts and voids change the cavity dimensions in ways that can surprise you. Look at your planes the way an antenna designer looks at a patch.

Third, the stitching via pattern. Enough stitching vias, placed where signal transitions happen, break up the cavities and complete the electromagnetic field wave guidance and subsequently the induced current paths.

Change the geometry, and you change the power delivery. The schematic defines the voltage target, but it is the copper that ultimately determines what the IC receives. 



KIRSCH MACKEY is a freelance writer with TechEdKirsch and a frequent Cadence blog contributor. He is an electrical engineer, educator, and content creator with over 15 years of experience spanning power systems, control systems, electrical systems, embedded programming, PCB design, power electronics, and high-speed digital systems.



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The PCB Podcast

AI's Next Manufacturing Challenge

The AI server boom is creating significant opportunities for the PCB industry, provided manufacturing capacity can scale to meet growing demand.

THE RELENTLESS AND ongoing surge in demand for AI servers continues to drive a huge call for materials and components. The effects within the PCB industry are well known, and supply challenges are affecting components of all types from high-end processors and memory modules to commodity items like multi-layer ceramic capacitors (MLCCs). Tens of thousands of these tiny but essential devices are needed on every server to perform power-supply decoupling, and equipment manufacturers need to be smart and decisive to secure the supplies they require.

And while investors celebrate the market performance of premium semiconductor stocks, excitement is building around related technologies like high-speed optical modules; the only devices capable of feeding cutting-edge GPUs with data quickly enough to keep them properly busy. Optical modules represent a huge growth opportunity as AI compute hardware seeks ever-faster interconnects between GPU clusters to continue boosting performance. Sales are expected to more than double in the next two years, particularly among the fastest modules, as server makers upgrade their interconnects from 400Gbit/s to 1.6Tbit/s and even 3.2Tbit/s.

What's interesting here, for the PCB industry, is that the substrates for these modules are becoming vastly more complex and expensive with each speed upgrade, now requiring as many as 50 layers featuring ultra-fine trace widths and very low-profile copper. While per-port data speeds are rising, and per-bit power efficiency is 30-40% greater, the overall power dissipation is increasing. In fact, 400Gbit/s modules typically dissipate 10-12W per unit, which scales to 320-384W for a fully loaded 32-port data center switch; dissipation is even greater at higher speeds. Realizing this is forcing thermal management back onto the table in high-speed board design.

In revenue terms, the market for optical module PCBs could potentially exceed \$3.75 billion in the next couple of years, according to Morgan Stanley. However, manufacturing these PCBs depends on advanced modified semi-additive process (mSAP) technology, which currently happens at scale only in Asia. This is consistent with the widespread loss of large-volume PCB manufacturing in numerous important technologies, which has happened over the last three decades in the West.

During that time, much of the Western electronics sector has moved out of manufacturing as technology businesses have directed their energies towards IP creation, design and conceptualizing. The strategy has been to concentrate on these high-value, high-margin activities, regarding manufacturing as low-margin, less profitable, and economical to outsource. Moreover, globalization made supply chains cheaper, so scaling production was faster and easier in Asia. Those of us who were in the industry in the late 1990s and early 2000s can probably remember thought leadership

comments from the time, confidently asserting that aspects like system architecture, chip design, software, standards and IP licensing would be directed from the West, while activities like chip fabrication, product assembly, and packaging would move to the East.

But the weakness in this model is that making things accumulates knowledge that provides the foundation for innovation. Making things teaches engineers how to improve them. Innovating only in aspects like design and intellectual property, but not in manufacturing, loses the feedback loops that sustain long-term competitiveness. Being close to where the manufacturing happens means being close to where the problems are. Solving these builds expertise and supports greater capability and capacity. It's important for driving investment and sustaining the high-tech sector as a whole.

It's now clear that outsourcing manufacturing has relinquished the power to generate wealth and shape the future of technology. Initiatives like the CHIPS Act, the EU Chips Act, onshoring incentives, and the drama over import tariffs and strategic export controls acknowledge this and are all part of the effort to rebuild high-tech manufacturing. Strong manufacturing depends on a diverse ecosystem that includes elements such as suppliers, sub-suppliers, logistics, and skills, which have also eroded with the loss of manufacturing. These cannot be legislated into existence and will take time to rebuild. Until that is achieved, reshored manufacturing will remain dependent on specialized materials, components and other services and supplies from abroad to deliver finished products.

The dominance historically held in the West is unlikely to return during this cycle. But there are opportunities to establish niches of excellence, perhaps in areas like photonics at the heart of the high-speed optical modules needed for AI servers. Success would depend on establishing a means to manufacture these technologies at scale, and the window for this opportunity is narrowing quickly.

I have commented on the importance of advanced technology for defense-related projects in previous columns here, and this remains topical amid prevailing conflicts and tensions worldwide. In this context, those initiatives to recapture high-tech manufacturing are also important to establish sovereignty of supply. There is a strong appetite for this in North America, including a recent significant investment in ultra HDI printed circuit board manufacturing in Syracuse. The partly government-funded initiative is among the first to establish purpose-built UHDI capabilities in the US and is expected to create up to 400 new jobs. The same company is also investing in PCB manufacturing in Europe by acquiring two existing SME board producers based in Switzerland and Germany. Europe, it must be said, is generally far behind in re-establishing large-scale indigenous high-tech electronics manufacturing.

Reshoring for any purposes, defense-related or commercial, needs to be viewed in the context of the current serious supply-chain squeeze driving basic materials into allocation. The main investments in new capacity to alleviate these shortages are happening in Asia. While conditions for doing business – prices, margins and payment terms – are simply more favorable there, the current cycle looks set to continue.  **P**



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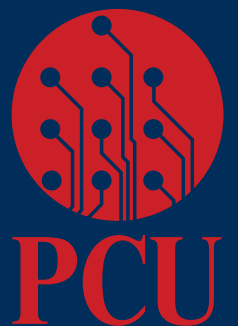
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Flexpert Bending with Attached Structure

Dynamic flex applications require careful consideration of bend geometry, material selection and stackup design to minimize mechanical stress and improve long-term reliability.

WHEN POSED WITH the question of bonding a flex circuit to a thin piece of plastic in an application where the bonded area will flex dynamically, much like a diving board secured at one end, the answer is that there are many variables that affect long-term reliability.

Below, I'll examine the factors with the greatest impact on performance and discuss how they interact in the final assembly.

Bend radius and bend angle. These are the first factors to evaluate. How tight is the bend? Is the dynamic flexing from zero to X degrees, or from zero to the same angle in both directions? These two variables, and how they interact, will have the single biggest impact on how the flex performs during service.

Right from the start, violating the IPC-2223 bend ratio guidelines for the bare flex is not a good sign. While exceeding the IPC-2223 bend ratio guidelines does not, by itself, guarantee failure, it is rare for the situation to improve as additional materials are added.

Flex circuit construction. The number of flex circuit layers and the overall thickness are both critical to the evaluation, both independently and in conjunction with bend radius and bend angle. The analysis becomes even more complex once the flex is bonded to a flexible plastic support.

Mechanical support type and thickness. The type and thickness of the mechanical support material are also important considerations. A softer-durometer thermoplastic with some elasticity will behave differently than a more rigid material such as ABS.

Mechanical support bonding method. The bonding method also plays a role. For example, a pressure-sensitive adhesive will affect the assembly differently than a thermosetting adhesive.

Interactions between variables. Whenever a material is bonded to a flex circuit, whether a thick FR-4 stiffener, a thin piece of plastic or a piece of stainless steel, the bonded area behaves differently when flexed. The change extends beyond the obvious increase in stiffness caused by the additional thickness. The same principle applies to areas with overmolded plastic on one or both sides of the flex.

Once additional materials are incorporated, flex circuit reliability can no longer be evaluated solely on the bend ratio of the bare flex. Instead, the entire stackup must be considered to predict how the assembly will perform during

dynamic flexing.

The first illustration below shows a cross-section of a single-layer flex and the approximate location of the neutral bend axis. Depending on the construction, the neutral axis generally falls within the middle third of the cross-sectional area. The second illustration shows the flex bonded to a mechanical support. In this configuration, the neutral axis shifts completely out of the flex circuit and into the mechanical support.

The amount of this shift depends on the thickness and material properties of the mechanical support. A support made from a softer, more elastic material, such as rubber or a soft thermoplastic, has less effect on the neutral axis than a rigid material such as FR-4. The location of the shifted neutral axis significantly influences the forces applied to the flex circuit as the assembly bends.



Figure 1. Bonding a flex circuit to a mechanical support shifts the neutral bend axis into the support material, increasing mechanical stress on the flex during dynamic bending.

The illustrations below show how shifting the neutral bend axis (blue line) into the mechanical support exposes the entire flex circuit to either tensile or compressive forces during bending. On a bare flex circuit, the outer portion of the bend experiences tension, while the inner portion experiences compression. The middle region of the flex experiences relatively little of either force.

Once additional material is bonded to the flex, these forces can increase rapidly, leading to failure. Excessive compression can create wrinkles that lead to delamination, while excessive tension can stretch the materials, resulting in tears and conductor cracks.

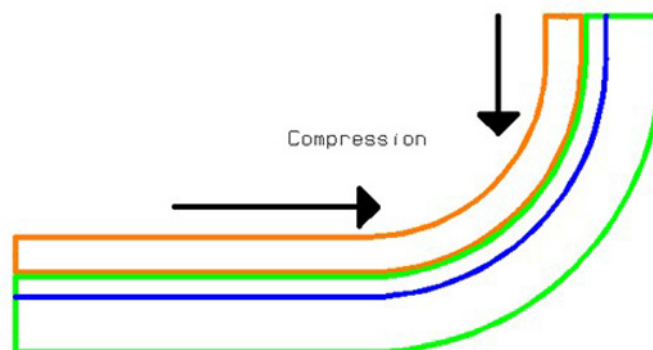


Figure 2. When the assembly bends in one direction, the shifted neutral axis subjects the flex circuit to increased tensile forces that can lead to stretching and conductor cracking.

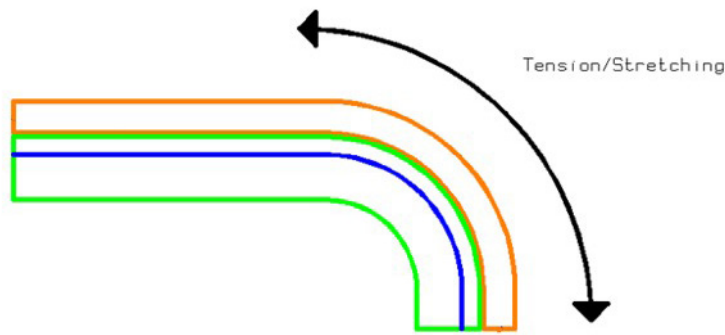


Figure 3. Bending in the opposite direction places the flex circuit under compression, increasing the risk of wrinkling and delamination.

Design recommendations. Revisiting the original design considerations, bend radius and bend angle have the greatest influence on long-term reliability. As bend radius decreases and bend angle increases, the forces acting on the flex rise dramatically. Any design changes that increase the bend radius or reduce the bend angle will improve reliability.

Using a thinner or softer mechanical support material can reduce the shift in the neutral axis. Another option is to use two mechanical supports, each half the required thickness, with one placed on each side of the flex. This configuration positions the flex closer to the center of the stackup and shifts the neutral axis back toward the flex circuit.

All these variables interact and can influence the performance of a dynamic flex circuit application in ways that are not always predictable. For that reason, it is important to have an in-depth discussion with the flex circuit supplier early in the design process. Experienced suppliers have seen thousands of applications and can provide valuable guidance on what works and, perhaps more importantly, what does not. 



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The Charge of the Bucket Brigade

An exploration of the PDN bucket brigade concept as a practical way to understand time-domain energy delivery in high-speed PCB design.

by DANIEL BEEKER

Why do otherwise good PCB designs still fail EMC testing, exhibit excessive jitter or require multiple redesign cycles? The answer often begins with a misunderstanding of how electromagnetic field energy moves through a power delivery network (PDN).

Every switching event in a modern electronic system creates a request for electromagnetic field energy. The question is not whether the energy exists – the question is whether the PDN can deliver it fast enough.

For decades, PCB design has often been taught from a conductor-centric perspective, where electrical current is viewed primarily as electrons moving through copper traces.

While circuit theory remains important, modern high-speed electronic systems increasingly require designers to think differently.

Electronic systems are fundamentally electromagnetic field management systems. As switching speeds continue to increase and semiconductor geometries continue to shrink, understanding how electromagnetic field energy behaves in the spaces surrounding conductors becomes critical to achieving signal integrity, power integrity, electromagnetic compatibility (EMC) and overall system reliability.

This is the foundation of what I often summarize as “All About That Space.” So far, Meghan Trainor has not objected to my repurposing of her 2014 hit song.

The Traditional View Versus the Physical Reality

Traditional circuit theory teaches that electrical energy flows inside conductors and that switches instantly cause current to flow through a loop. In reality, electromagnetic field energy propagates through the dielectric spaces between the conductors.

Switches do not simply connect wires; they create new spaces into which electromagnetic field energy must propagate, and that propagation takes time. The movement of electromagnetic field energy through space is what is observed as current flow. As signal rise times shrink into the nanosecond and picosecond range, understanding this distinction becomes increasingly important.

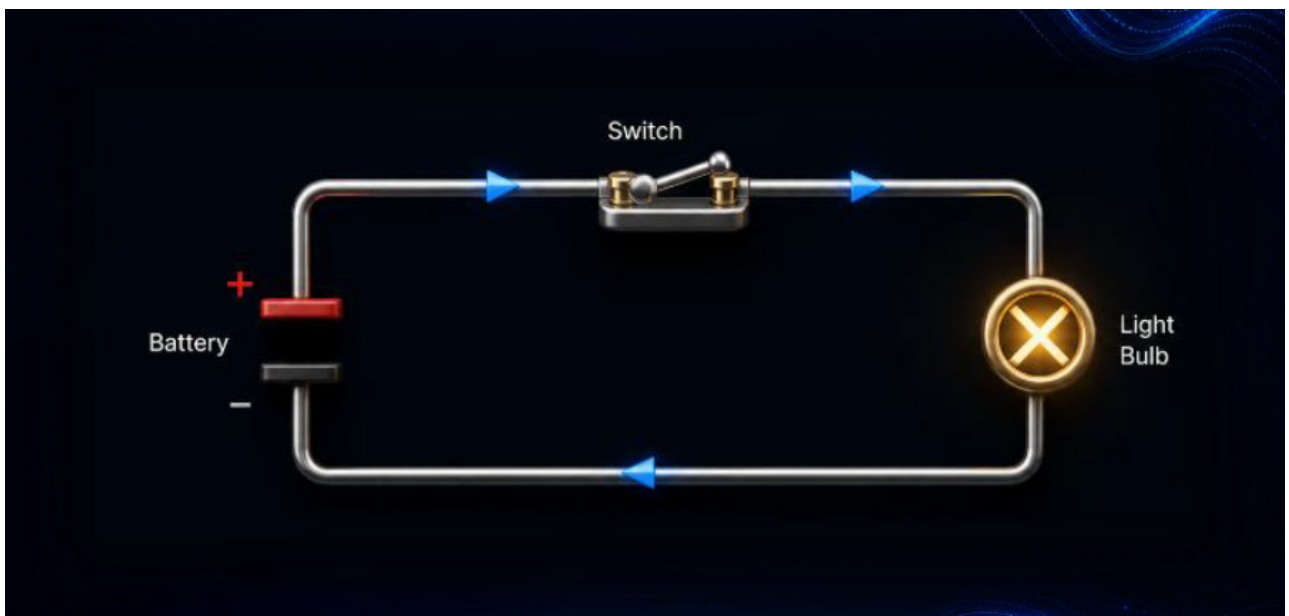


Figure 1. Illustration of the traditional view of power delivery. *(All images courtesy of Cadence Design Systems.)*

The rules of triplets. Modern electronic systems can be understood through three fundamental concepts. Electromagnetic field energy requires only three elements for containment: a conductor, a dielectric space and another conductor. Likewise, electronic systems are built from just three basic components: conductors, dielectric spaces and switches. Electromagnetic field energy can perform only three functions: it can be stored, moved or converted into kinetic energy. Together, these principles provide a simplified framework for understanding complex PCB behavior.

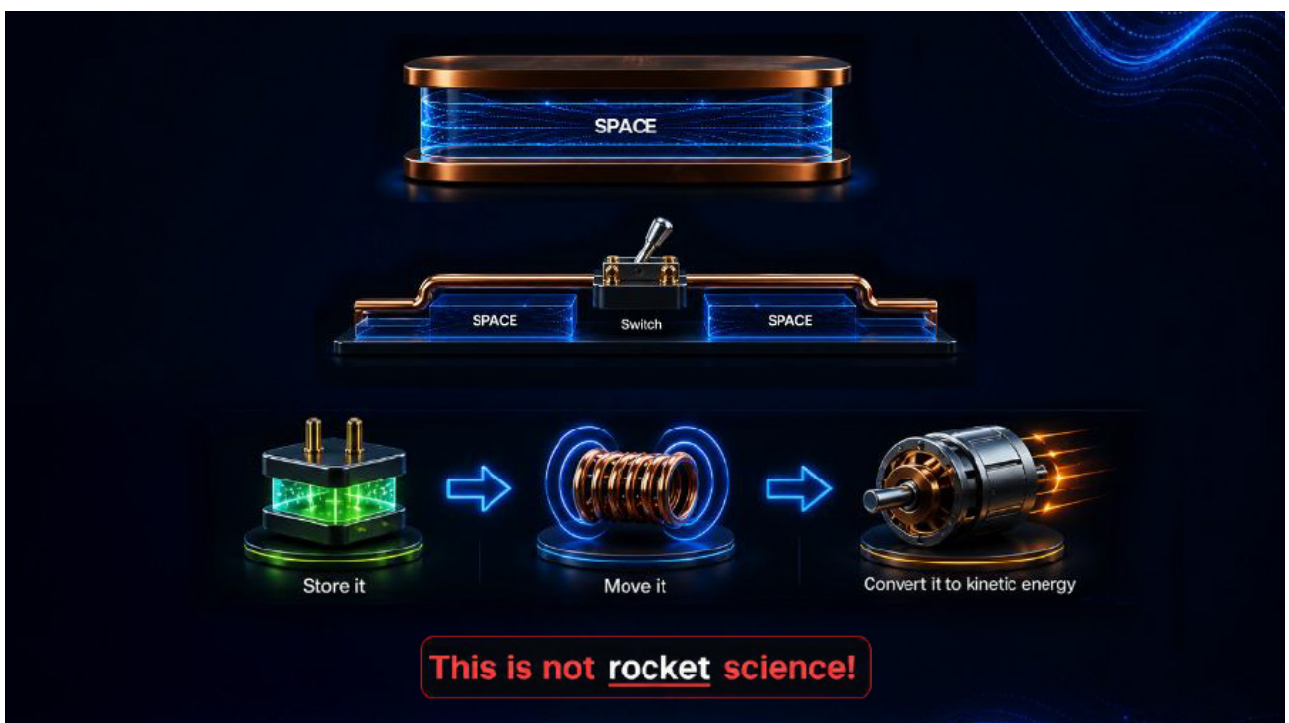


Figure 2. Illustration of the Rules of Triplets concept.

Signal integrity starts with power integrity. One of the most misunderstood aspects of high-speed PCB design is that signal integrity depends directly on power integrity. A poorly designed power delivery network cannot support

clean signal behavior.

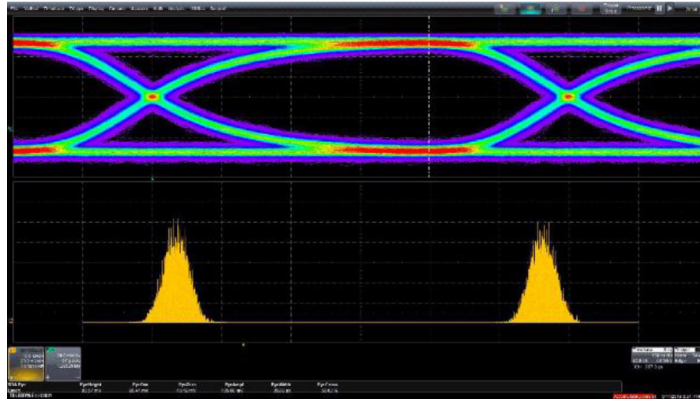


Figure 3. Signal integrity begins with power integrity.

Every switching event creates a demand for electromagnetic field energy. That demand propagates as a wave through the power delivery structure until energy is delivered from nearby storage structures. The critical issue is time. Field energy does not arrive instantaneously. The request for energy must travel to the storage device and return to the switching device.

This creates a hierarchy of energy delivery systems:

- On-die capacitance
- Package capacitance
- PCB planar capacitance
- Local bypass capacitors
- Bulk capacitors
- Power supplies

The farther away the energy source is from the switching device, the longer it takes to respond. As semiconductor switching speeds increase, the effective energy-delivery distance becomes extremely short.

At picosecond edge rates, the depletion waves requesting energy may not even travel outside the footprint of the BGA package before multiple switching cycles have already occurred. This is why low-impedance transmission line structures, tightly coupled power/ground systems, and small-package capacitors located close to the switching device become essential.

The PCB designer's job is no longer simply routing traces. Now, the PCB designers must control electromagnetic field movement in three-dimensional spaces.

Well-defined transmission lines. Signal traces must remain one dielectric away from their return path along their entire length, including vertical transitions. This requirement applies to adjacent reference planes, coplanar structures, vias and layer transitions to maintain signal integrity and consistent electromagnetic field behavior.

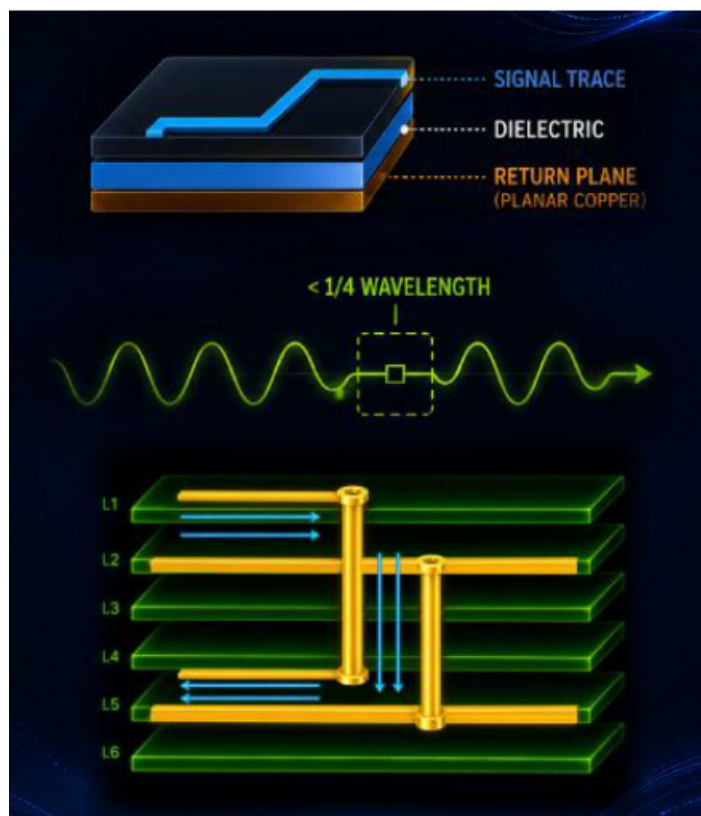


Figure 4. Characteristics of well-defined transmission lines.

One of the most common design mistakes in otherwise good PCB layouts is failing to maintain proper field containment through vertical transitions. The fields do not magically find their way between layers. They fill the space between the signal via and the nearest ground via. If it is not done by design, the results can be devastating, causing SI issues and EMC failures. The electromagnetic fields continue to propagate through the surrounding spaces and must remain properly controlled.

The PDN Bucket Brigade: The Eureka Moment



Figure 5. Energy delivery from power supplies is a one-way path.

Each node in the power supply should be considered a discrete electromagnetic energy domain, with field energy traveling downstream from the power source to the switching device. The farther away from the switch, the longer it

takes for the request for energy to be answered. Do not ask for fast energy from a large package capacitor far away, and you will avoid disappointment. The supply system must be designed so that different portions of the electromagnetic energy spectrum are delivered from matching structures.

Imagine a network of water barrels connected by pipes of different diameters and lengths. The large barrels farther away hold substantial amounts of water, but they do not respond quickly to changes in demand. Smaller, closer barrels respond much faster but cannot supply large volumes of water.

The capacitors behave like these reservoirs distributed throughout the system. Before energy can move farther downstream, those reservoirs must first fill.

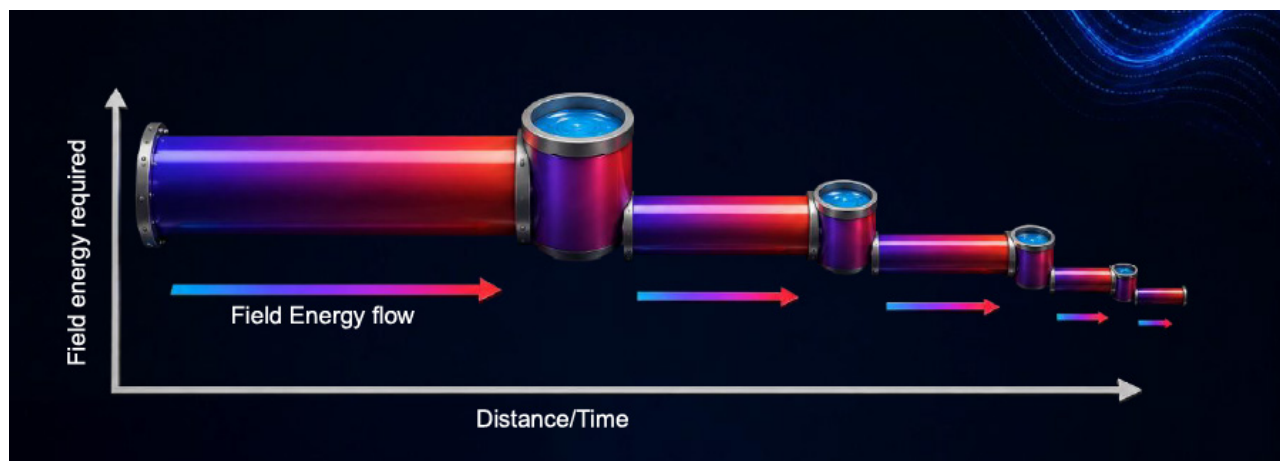


Figure 6. The overall behavior is less like the source pushing energy forward and more like the loads pulling electromagnetic field energy toward themselves.

When a switch closes, field energy moves into a newly connected space. That movement creates a localized drop in field density, which launches a depletion wave back upstream through the PDN.

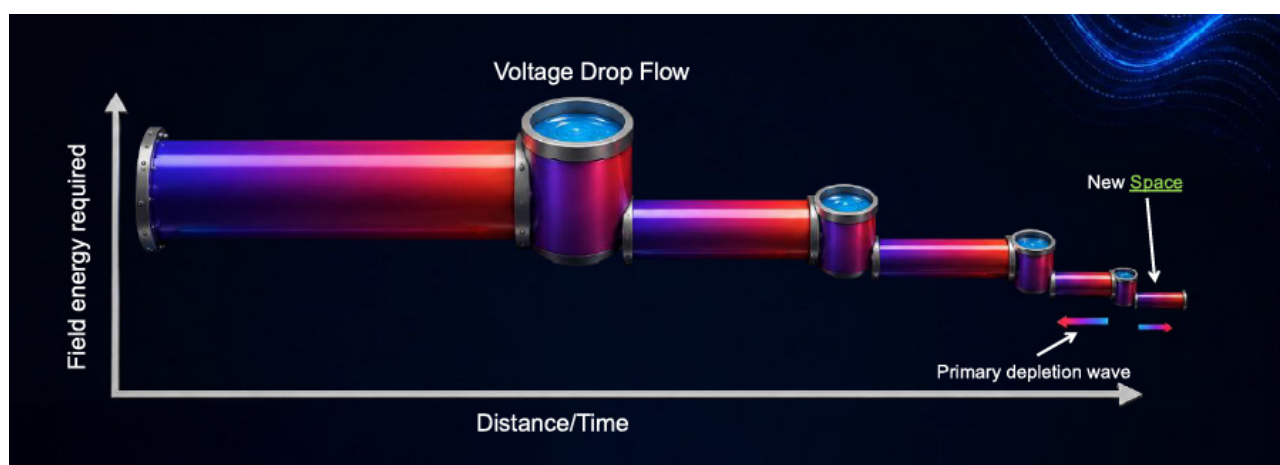


Figure 7. The switch turns on.

This depletion wave travels outward requesting additional electromagnetic field energy. When the wave encounters a nearby energy storage structure, such as on-chip capacitance, package capacitance, plane capacitance or local bypass capacitors, energy begins returning toward the switching device.

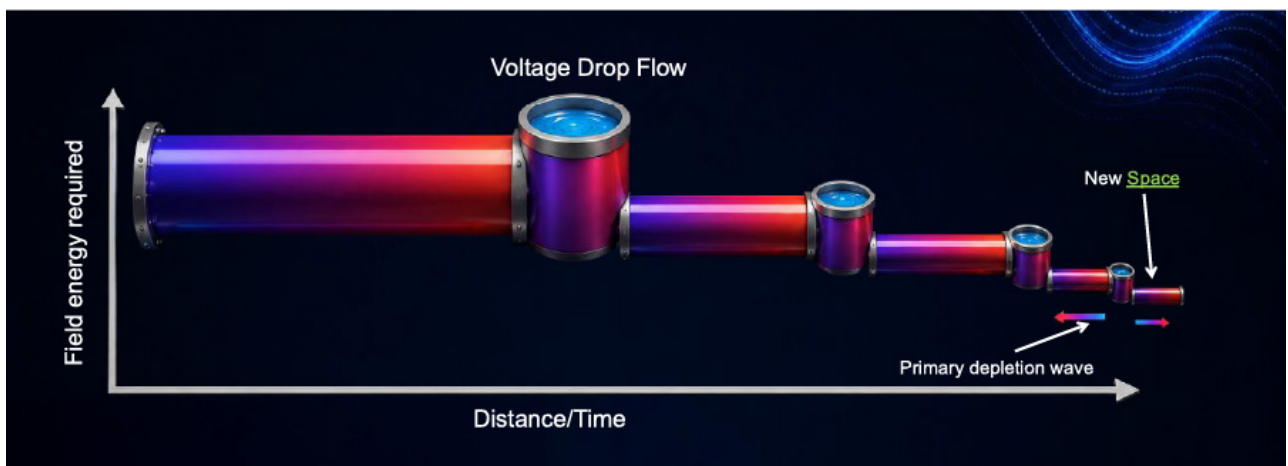


Figure 8. The bucket brigade begins.

Each reflection creates a new reduction in field density at the discontinuity, launching additional waves farther upstream to request more energy. The closest energy storage structures respond first because their round-trip propagation delay is shortest. More distant structures respond later.

This process continues in a cascading hierarchy:

- On-chip capacitance
- Package capacitance
- PCB planes
- Local capacitors
- Bulk capacitors
- Eventually the power supply itself

The result is a distributed electromagnetic “bucket brigade” in which energy is progressively transferred from smaller, faster-switching structures and replenished by larger, slower-switching storage domains farther away. At the speeds electromagnetic waves travel, this process happens astonishingly fast. Electromagnetic waves on a standard PCB move approximately one-sixteenth of an inch in 10 picoseconds. Eight round-trip depletion and replenishment cycles may occur in only 160 picoseconds.

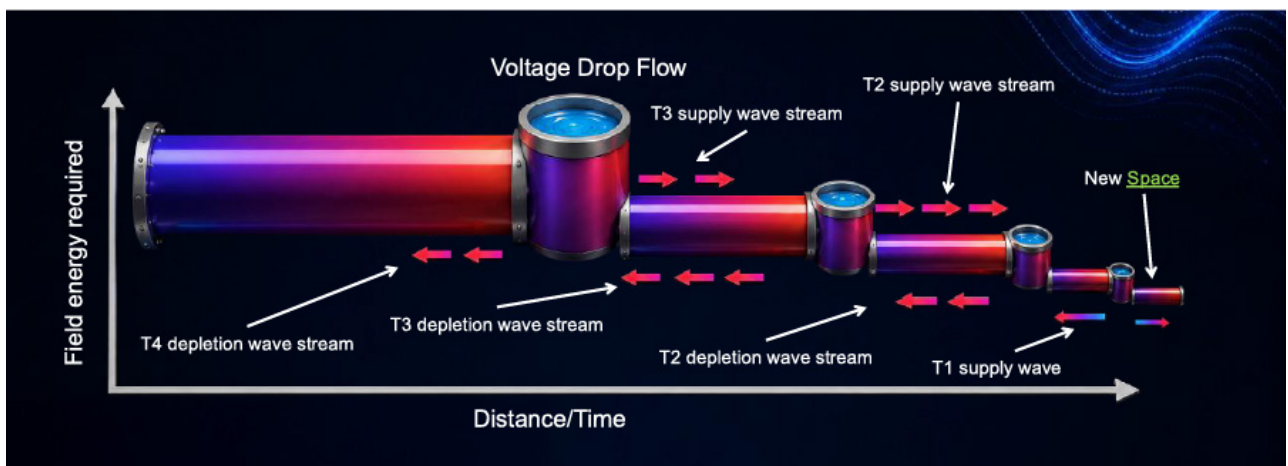


Figure 9. Illustration of the distributed electromagnetic “bucket brigade,” in which energy is rapidly transferred between local and remote storage structures to maintain stable power delivery.

During that time, the energy travels only one inch, and the electromagnetic field energy may not even propagate in the planar structure beyond the footprint of a typical BGA package.

Perspective

- 1/16 inch in 10pS
- 8 cycles in 160pS
- Energy has moved only 1 inch



Figure 10. The energy has only traveled one inch in any direction during this time.

The power management IC still has no idea. At modern switching speeds, multiple depletion-and-replenishment cycles can occur before electromagnetic field energy has propagated beyond the footprint of a typical BGA package. The power management IC (PMIC) has no idea that the switching event has occurred. The switching device is initially supported by nearby energy storage structures rather than the distant power supply.

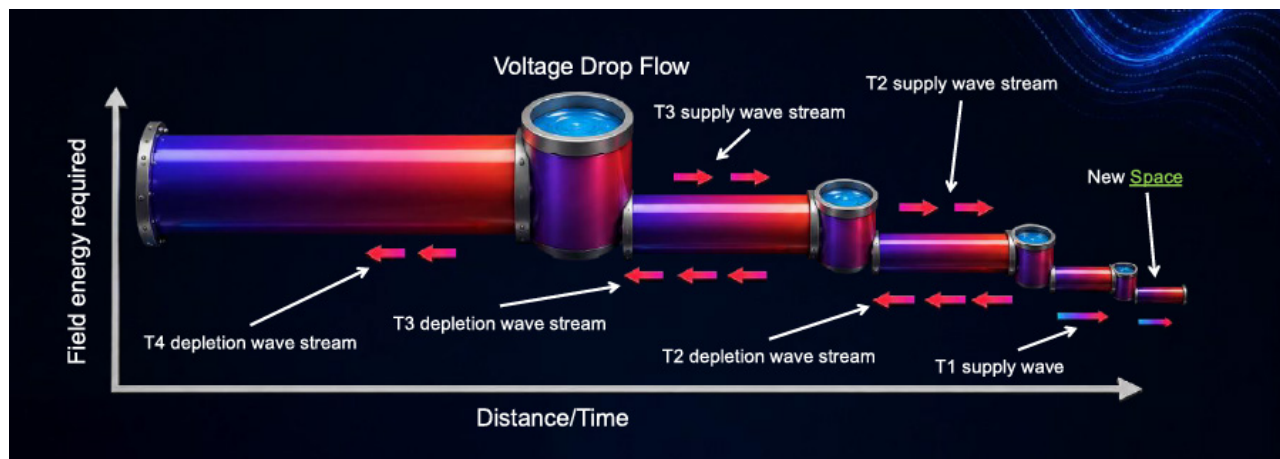


Figure 11. Eighth T1 cycle, and the PMIC still has no clue.

In a good design, there is enough energy available in the first two domains to supply the device with energy until the bucket brigade makes its way to the PMIC and back again. In a world where picoseconds matter, travel times in the nanosecond range and beyond make delivering energy from the power supply a critical consideration in PDN design, and the local storage capacity must be up to the challenge. This simple concept can spell the difference between success and failure.

As stated earlier, the PCB designer's job is no longer simply routing traces. The challenge is managing and controlling electromagnetic energy movement through three-dimensional space. It's "All About That Space."

The New Reality

Modern PCB designers are not simply connecting circuits. We are designing three-dimensional structures that guide, contain, store and deliver electromagnetic field energy.

Or stated another way: "We are all just plumbers using very leaky water pipes."

One final thought: if the Bucket Brigade did not exist, modern electronics simply would not work. This is a simplified perspective of the time domain, wave-based power supply behavior. There are, in fact, thousands of buckets traveling in search of energy. Because the distances depletion waves must travel across the die and package differ, each switching event creates a unique set of wave cycles. All of these requests for energy working in concert form the foundation of power supply behavior.

The conductors define the boundaries. The spaces determine the behavior. The length determines the time. This is a four-dimensional concept.

And ultimately, it's "All About That Space." 

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Flex DfM Guidelines, Part 1

Understanding key flex DfM guidelines can improve yields, reduce production risks and enhance long-term product reliability.

by AKBER ROY

Design for manufacturability (DfM) is critical in ensuring high yield, reduced production risks, controlled costs and long-term product reliability. This guideline outlines essential DfM principles to help flexible circuit designers optimize performance, durability and production efficiency while meeting the demands of the modern electronics industry.



Figure 1. Flexible circuit fabrication is similar to the process for manufacturing rigid PCBs, but with a few key differences.

Because of the breadth of the topic, this guideline is presented in two parts. Part 1 focuses on internal layout and drilling considerations, while Part 2 will address design outline requirements and other design-related features.

Material selection (thickness). Material thickness directly affects flexibility, bend life and mechanical reliability of the flex PCB. The selection of the base polyimide, copper foil thickness, adhesive and coverlay must align with the product's bending requirements and electrical performance. Thinner constructions improve dynamic flexibility, while thicker builds offer mechanical strength and dimensional stability. Proper stackup planning ensures manufacturability and long-term reliability.

Table 1. Standard Flexible PCB Material Thicknesses

Material Selection	Material Type	Standard Thickness (μm)		
Base Material	Polyimide	12.5	20/25	50
	Cu (RA and ED)	12	18	35
	Adhesive	13	20	
Bonding Sheet	Epoxy / Acrylic	12	20/25/40	50
Cover Lay	Polyimide	7.5	12.5	25
	Adhesive	10	15/20/25/30	35
Covercoat	Photo Imageable S/M	5 to 30 (over conductive surface)		
Stiffener	PI with adhesive	25 to 200		
	FR4 W/O adhesive	0.1mm to 1.6mm		
	Others (SUS, Aluminum)	As per customer specification		
	Shielding Film	8	10	15

Holes (Drilling & Plating)

In flex PCBs, the drilling and plating process is a delicate balance between electrical precision and physical toughness. Since these boards are built to bend, every hole (from standard mechanical vias to tiny laser-drilled holes) needs to be placed with plenty of material support to stay stable. Proper spacing is the key to keeping signals isolated and making sure the copper plating doesn't crack or merge under pressure. It is also vital to keep holes away from transition zones to prevent mechanical failure when the board is folded or twisted. Ultimately, following these steps ensures that the circuit remains reliable even in the most demanding, high-flex environments.

Hole size. For flexible circuits, the standard minimum mechanical hole size is 0.15mm, ensuring stable drilling and reliable plating during regular production. With specialized technological capabilities, we can ensure the use of a minimum hole size of 0.1mm, which is typically used for high-density designs requiring finer interconnections and tighter layout constraints.

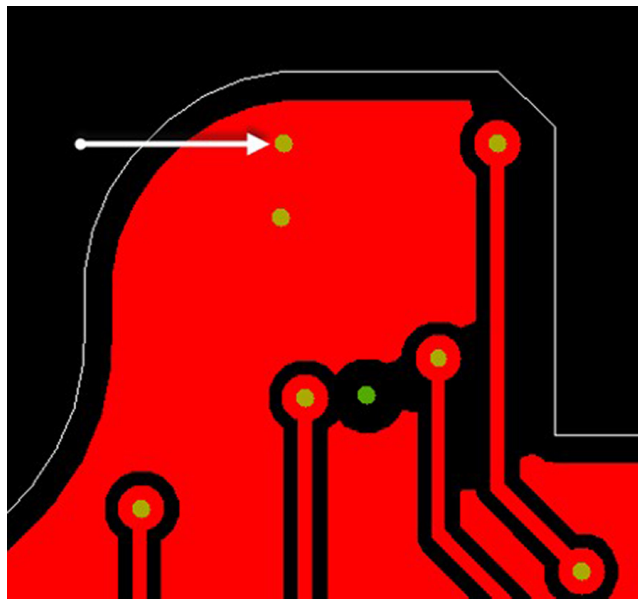


Figure 2. Minimum mechanical hole sizes for standard and advanced flex PCB manufacturing capabilities.

Hole spacing (same net holes). For holes belonging to the same net, spacing can be reduced to 0.2mm (standard) and 0.15mm (special) as no electrical isolation is required between them. CAM must still ensure that adequate material remains between holes to maintain drill integrity, registration accuracy and structural reliability, however. If spacing is reduced below the defined limits, it can lead to drill breakouts, hole merging, weakened webbing and poor plating quality, potentially causing reliability issues such as mechanical failure or intermittent connectivity.

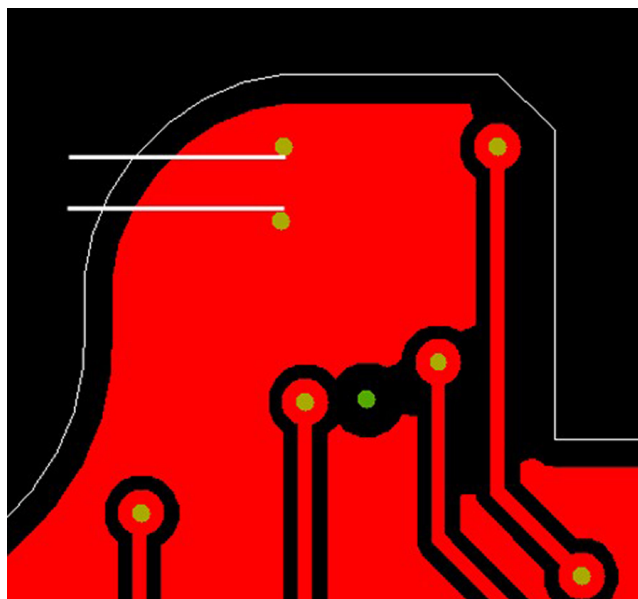


Figure 3. Minimum spacing requirements between plated holes on the same electrical net.

Hole spacing (different net holes). For different nets, the minimum hole-to-hole edge spacing is 0.36mm (standard) and may be reduced to 0.275mm with special technology to maintain required electrical isolation. If the applied design does not follow the DfM specification, it may introduce the risk of insufficient clearance and potential

electrical isolation issues.

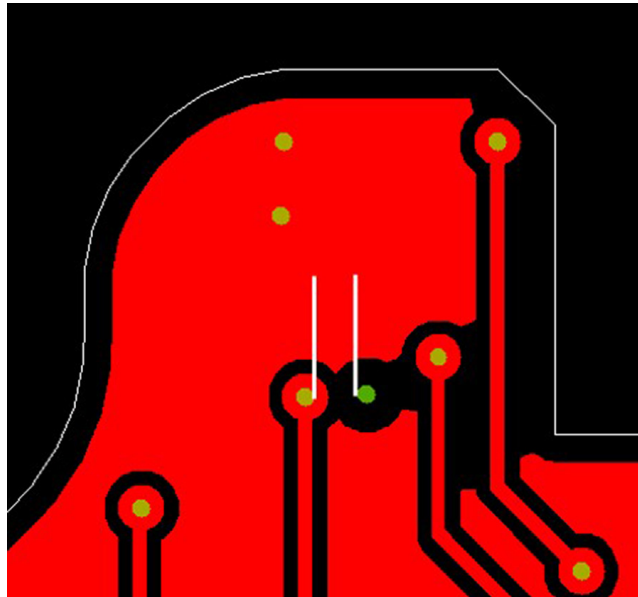


Figure 4. Minimum spacing requirements between plated holes on different electrical nets to maintain electrical isolation.

The minimum spacing between a plated through hole (PTH) edge and non-plated through hole (NPTH) edge in a flex PCB is 0.275mm (standard) and can be reduced to 0.20mm under special process capability, ensuring adequate material support and plating reliability. If this requirement is not maintained, it can result in plating cracks, dielectric separation or hole wall breakout, especially under bending stress, leading to long-term mechanical and electrical failure.

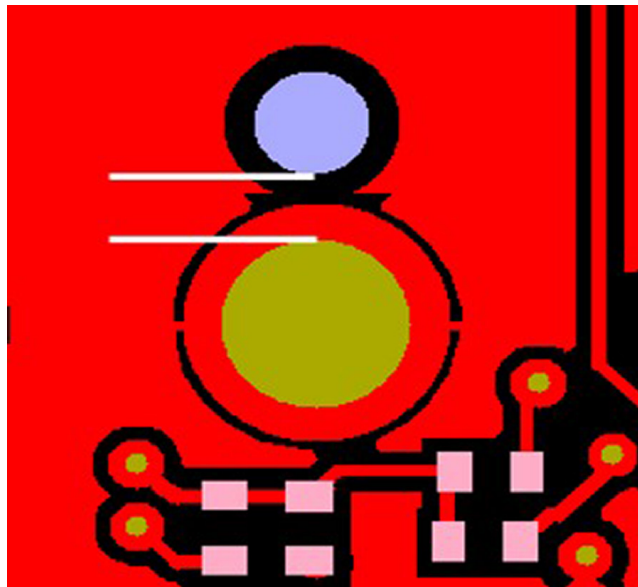


Figure 5. Minimum spacing requirements between PTHs and NPTHs.

To maintain mechanical reliability and avoid edge breakout, consider a minimum PTH-to-outline clearance of

0.275mm (standard build) or 0.2mm (advanced build). Not meeting these limits may cause barrel cracking, plating damage, delamination or electrical opens, thereby reducing long-term reliability.

Slot hole size. Our flex process supports slot widths of 0.5–2.5mm and lengths of 1–10.7mm ($L/W > 2$) to ensure stable fabrication. Exceeding these limits may cause deformation, tearing, plating defects or reduced mechanical reliability during assembly and flexing.

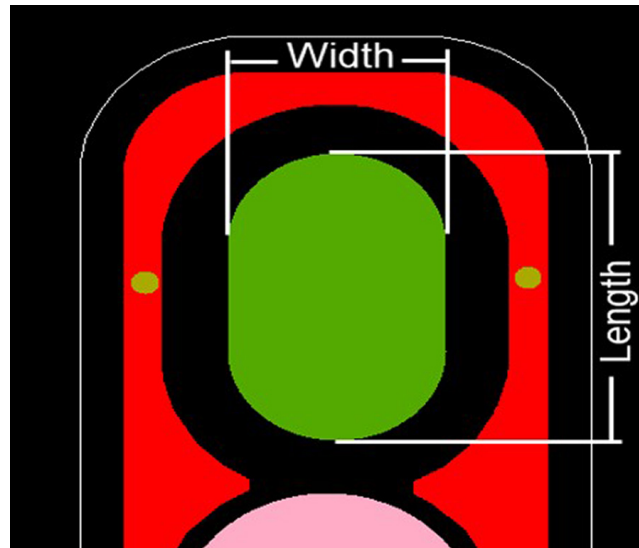


Figure 6. Recommended slot dimensions for reliable flex fabrication and long-term mechanical performance.

Minimum laser hole size. Our flex capability supports minimum laser-drilled hole sizes of 0.10mm (standard) and 0.075mm (advanced). Smaller diameters may lead to incomplete drilling, poor plating, weak interconnects and reduced reliability.

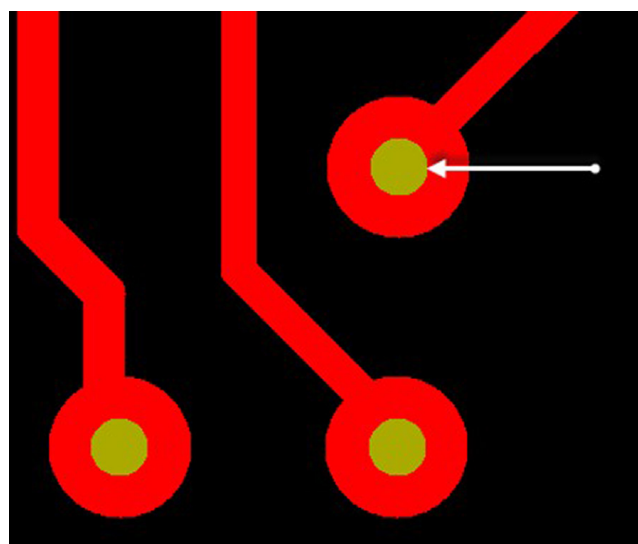


Figure 7. Minimum laser-drilled via sizes supported by standard and advanced flex manufacturing processes.

Minimum hole-to-bend area distance. A minimum hole-to-bend distance of 1mm is recommended to prevent

mechanical stress damage during forming. Advanced constructions may support reduced spacing, but ignoring this guideline can lead to barrel cracking, pad lifting, delamination and long-term reliability failures.

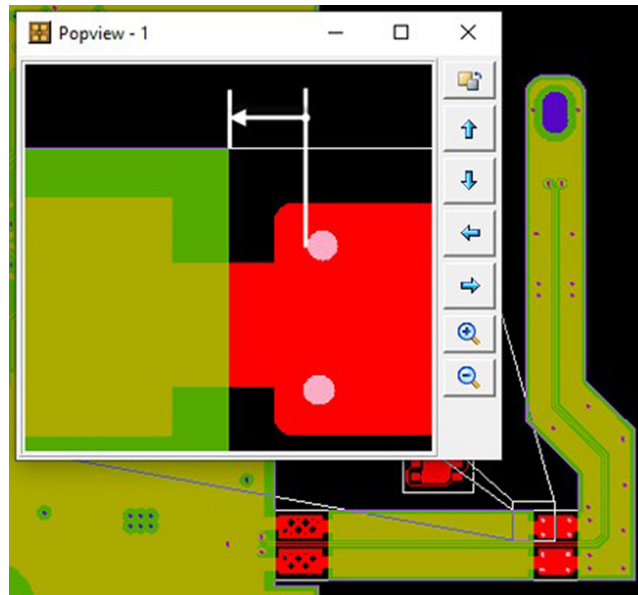


Figure 8. Minimum clearance between drilled holes and bend areas to reduce mechanical stress and improve reliability.

Minimum Line Width/Space

The ability to achieve fine trace geometries and tight copper spacing is primarily influenced by the layer's base copper thickness and the manufacturing technology used. Based on these factors, here are recommendations for different base copper weights:

Minimum line width/spacing for 0.33oz base copper. For 0.33oz base copper, fine trace geometries are achievable due to the lower copper thickness. Without additional copper plating, line width and spacing can reach 0.045mm under standard capability and 0.035mm with advanced processing. A PCB involving button plating requires higher values of 0.0635mm (standard) and 0.050mm (special), while panel plating further increases them to 0.075mm and 0.0635mm, respectively. The added copper buildup from plating reduces etching precision, requiring wider trace spacing to ensure reliable manufacturability.

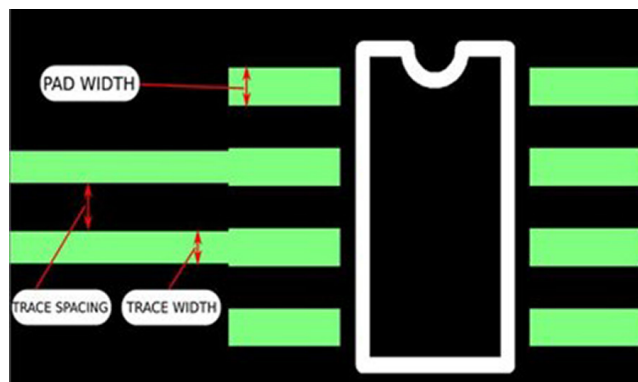


Figure 9. Minimum line width and spacing guidelines for 0.33oz base copper under standard and advanced manufacturing conditions.

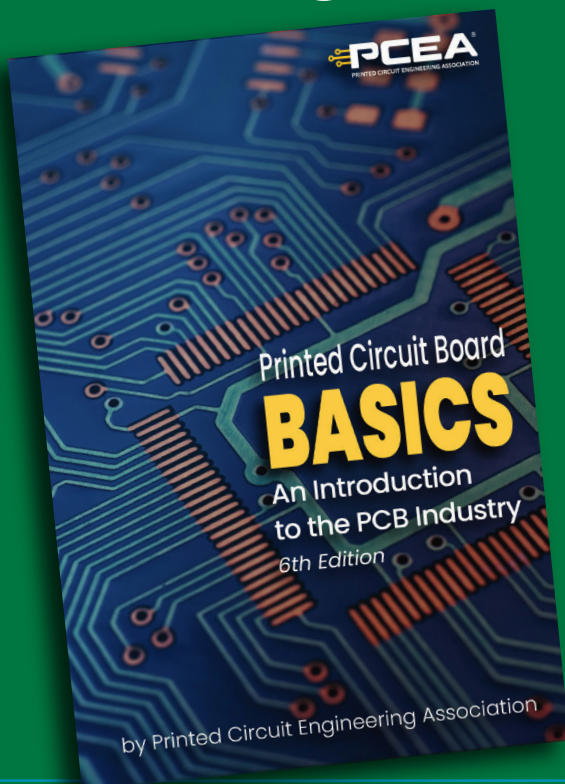
Minimum line width/spacing for 0.5oz base copper. With 0.5oz base copper, the increased copper thickness requires slightly larger trace widths and spacing compared to 0.33oz copper. For non-plated designs, the minimum achievable line width and spacing are 0.050mm (standard) and 0.045mm (special). When button plating is introduced, these values increase to 0.0635mm and 0.050mm, respectively. Panel plating imposes the most restrictive limits, requiring a minimum of 0.075mm (standard) and 0.0635mm (special). These constraints are necessary to compensate for the added copper thickness and to maintain reliable etching and electrical isolation between traces.

Minimum line width/spacing for 1oz base copper. Designs incorporating 1oz base copper demand significantly wider traces and spacing due to the higher copper thickness and reduced etching tolerance. For configurations without copper plating, the minimum line width and spacing are typically 0.1mm under standard manufacturing conditions and 0.075mm for special capabilities. The thicker copper not only limits fine feature fabrication but also impacts the mechanical flexibility of the circuit, making it especially critical in rigid-flex applications to balance electrical performance with mechanical reliability. 🛠️

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Why Don't UHDI Capability Charts Tell the Whole Story?

Understanding the difference between process capability and design intent enables engineers to maximize UHDI performance while improving manufacturability and yield.

by ANAYA VARDYA

Ultra high-density interconnect (UHDI) is a PCB fabrication technology that achieves trace and space geometries of $75\mu\text{m}$ or smaller, as defined by IPC-2226 Class C. These finer geometries enable higher routing density within a smaller board footprint.

A UHDI capability chart defines the minimum feature sizes a fabrication process can achieve, including trace and space, microvia diameter and layer-to-layer registration. What it does not define is which of those minimums are repeatable in production or appropriate for a particular design. Using capability data effectively requires understanding the difference between what is possible, what is repeatable and what is best suited to the application. IPC-2226 defines density levels A, B and C that correspond to these capability tiers, with Class C covering the sub- $75\mu\text{m}$ geometries characteristic of UHDI.

One question comes up early in almost every UHDI discussion: "What is the minimum trace and space that can be used?"

It is a logical place to start. It is also where UHDI design begins to move beyond familiar design practices. In UHDI, those minimum values matter, but they do not tell the whole story.

Capability charts are valuable tools. They define what a fabrication process can achieve and help designers understand where new possibilities exist. UHDI expands those possibilities with finer traces, smaller microvias and higher routing density than traditional PCB technologies.

The challenge is that those values can easily be interpreted as design targets rather than process capabilities. A capability chart defines what is possible. Successful UHDI design comes from understanding what is also repeatable and appropriate for the design.

Learning from a capability chart. When a fabricator publishes values for trace and space, microvia size or outer-layer spacing, it is easy to view those numbers as design rules. In reality, they are better understood as process boundaries.

In reality, they are better understood as boundaries. They represent what the process can achieve under the right conditions: specific materials, specific stackups, specific layer structures. They don't automatically define the most stable or efficient choice for every part of every design.

That distinction becomes more important as geometries shrink. In UHDI, a single number rarely tells the full story. The effectiveness of any feature depends on its context within the design, including where it sits in the stackup, the routing density around it, the other design constraints nearby and, ultimately, what the design is trying to accomplish. When those factors are considered together, UHDI becomes much easier to understand and apply successfully.

Geometry precision matters more in UHDI. UHDI does more than shrink features. It makes the design space more precise. As geometries become smaller, there is less unused margin, which means design decisions carry greater weight and there is less room to accommodate errors.

That added precision enables cleaner breakouts from fine-pitch BGAs, often reduces layer counts, improves electrical performance and makes more efficient use of available board space. At the same time, it requires a more deliberate approach to layout because there is less flexibility built into the design.

This represents an important shift in design philosophy. A 25 μ m trace may be achievable. A 50 μ m microvia may also be achievable. Tight outer-layer spacing may be well within a fabricator's capabilities. The real question is where those features provide meaningful value and where more relaxed geometries can achieve the same result with greater manufacturing margin.

That is where UHDI design becomes strategic.

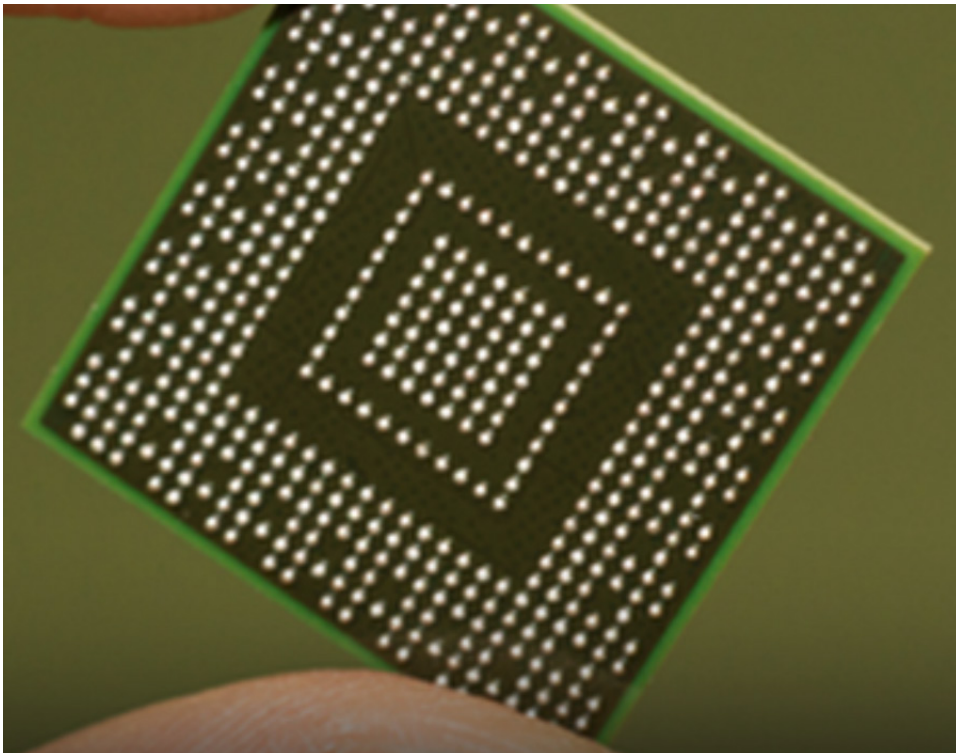


Figure 1. UHDI enables finer traces and smaller features, but successful designs rely on using those capabilities where they add the most value.

The most common UHDI design errors. Most UHDI fabrication challenges do not come from pushing the limits of the technology. They result from applying those limits everywhere without a clear design purpose.

One of the most common mistakes is using minimum trace and space across the entire board. Once a design team knows a fabrication process can support very fine geometries, it is tempting to use them throughout the layout. In reality, most designs do not require that level of density everywhere. Areas such as fine-pitch BGA breakouts or other highly constrained regions often benefit from aggressive routing, while more open areas can use relaxed geometries that improve manufacturability without affecting performance.

Another common misconception is assuming the same design rules should apply across the entire PCB. Different layers, routing regions and structures have different requirements. A dense breakout area may justify one set of design choices, while a less constrained routing region may not. Treating the entire board as though it must meet the most demanding conditions can add unnecessary complexity. Thinking in terms of design zones, rather than one global rule, often produces better results.

It is also important to avoid evaluating individual features in isolation. Capability charts typically list values such as minimum trace and space, minimum microvia size and minimum spacing, but a PCB is built from combinations of these features. Trace width affects pad definition, pad definition influences solder mask requirements, and vias interact with dielectric thickness and layer-to-layer alignment. IPC-2315 provides additional guidance for microvia design. In the highest-density areas of a layout, all of these relationships come together.

Understanding how these features interact, rather than evaluating each one independently, is what distinguishes a well-executed UHDI design from one that simply pushes minimum dimensions.

Another misconception is assuming all UHDI fabrication processes perform the same way. Capability depends on the fabricator's equipment, materials and manufacturing experience. Two suppliers may publish similar capability charts but achieve those results using different processes and process windows. That does not make one approach better than another, but it does mean those published values should not be viewed as interchangeable.

This is why early collaboration with the fabricator is so important. Working together early in the design process ensures the layout is aligned with a proven manufacturing process rather than a generic assumption.

How to think about UHDI capability. One useful way to think about UHDI capability is in three stages. First, determine what is possible, meaning the feature can be produced under controlled conditions. Next, consider what is repeatable, or what can be manufactured consistently. Finally, evaluate whether that feature is well suited to the design by supporting manufacturability, reliability and yield.

That final step is where the strongest UHDI designs are developed. The goal is not to avoid the edge of process capability, but to understand when operating at that edge is necessary and when a more forgiving geometry will achieve the same result.

Using capability data more effectively. Capability charts become far more valuable when they are treated as

design tools rather than rigid rules. The smallest trace widths, microvias and spacing should be reserved for the areas that truly require them, such as fine-pitch BGA breakouts, dense escape routing and other localized high-density regions. Elsewhere, allowing a little more design margin can improve manufacturability without sacrificing performance.

It is equally important to ask questions early in the design process. Rather than concentrating only on minimum feature sizes, discuss which geometries are most comfortable for the selected stackup, where the process becomes more sensitive and which areas of the board would benefit from additional design margin. These conversations help shape a design that is aligned with the manufacturing process.

Designers should also think in terms of zones rather than applying one set of rules across the entire board. Different regions often have different requirements, and UHDI provides the flexibility to apply tighter geometries only where they provide meaningful value.

Ultimately, successful UHDI designs are developed within a proven process window rather than at the limits of capability simply because those limits exist. Designing within that process window typically results in more predictable fabrication, improved yields and a smoother transition from design to manufacturing.

UHDI is not higher risk than traditional PCB design; it offers more control. Tighter geometries enable more efficient routing, reduced layer counts, and improved electrical performance when applied with intent. It's easy to look at fine geometry and assume higher risk; in practice, the opposite is true when the design is aligned to a real process window.

It gives designers the ability to:

- route more efficiently
- reduce layer counts
- improve electrical performance
- and solve problems that were difficult or impractical with traditional approaches.

Like any advanced technology, it rewards understanding. But it does not require perfection.

Designers don't need to memorize every process detail. They need to understand how to interpret the information they already use. Capability charts are still part of that picture and they work best when paired with intent. Because in UHDI, the advantage doesn't come from using the smallest number everywhere. It comes from knowing where that number matters, and where it doesn't.

The most important thing to remember is that capability charts define what is possible under controlled manufacturing conditions, not what is optimal for every design. Successful UHDI designs apply the smallest geometries only where higher routing density is truly needed and use more relaxed dimensions where they provide the same electrical performance with greater manufacturing margin.

Understanding the difference between the limits of a fabrication process and the right geometry for a specific application is what transforms UHDI from a collection of capability numbers into a practical manufacturing advantage.

Key Takeaways

Capability charts establish process boundaries, but they should not be treated as universal design rules. Minimum feature sizes describe what a fabrication process can achieve, not necessarily what can be manufactured most consistently or what is best suited to every design.

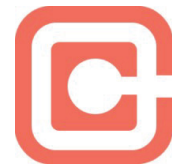
Applying the smallest geometries only where they add value, such as fine-pitch BGA breakouts and other localized high-density routing areas, improves manufacturability without compromising performance. Likewise, treating different areas of the board according to their individual requirements, rather than applying one aggressive rule set everywhere, creates a more balanced design.

Early collaboration with the fabricator ensures the layout is matched to a proven process window instead of relying on generic capability data. When approached this way, UHDI provides designers with greater flexibility and control, enabling higher-density designs while maintaining reliable, repeatable manufacturing. 

ANAYA VARDYA is CEO of American Standard Circuits and ASC Sunstone Circuits. ASC works closely with customers and design teams on advanced PCB technologies, including RF, HDI, rigid-flex and ultra HDI, with a focus on turning complex fabrication realities into practical design guidance.

Thank You!

TO OUR PCEA CORPORATE MEMBERS

The logo for ACCURIS features a stylized blue icon resembling a circuit board or a stylized 'A' to the left of the word "ACCURIS" in a blue, sans-serif font.The logo for all flex SOLUTIONS features a stylized orange 'A' with a circuit board pattern inside, above the text "all flex" in a blue, sans-serif font, with "SOLUTIONS" in a smaller, orange, sans-serif font below it.The logo for AllSpice.io features a stylized blue circuit board icon to the left of the text "AllSpice.io" in a blue, sans-serif font.The logo for ASC features a stylized blue circuit board icon to the left of the letters "ASC" in a bold, black, sans-serif font.The logo for BEST Technology features the word "BEST" in a large, bold, blue, sans-serif font, with "Technology" in a smaller, blue, sans-serif font below it.The logo for BOARDERA features the word "BOARDERA" in a grey, sans-serif font, with the letter 'E' stylized in green.The logo for CED features the letters "CED" in a bold, black, sans-serif font, with "CHESTER ELECTRONIC DESIGN" in a smaller, black, sans-serif font below it.The logo for cofactr features a green circuit board icon to the left of the word "cofactr" in a green, sans-serif font.The logo for Cybord features the word "Cybord" in a blue, sans-serif font, with a stylized blue circuit board icon to the right.The logo for DirectPCB features a stylized green circuit board icon to the left of the text "DirectPCB" in a green, sans-serif font.The logo for ep ELECTRONIC INTERCONNECT features a stylized blue 'ep' logo to the left of the text "ELECTRONIC INTERCONNECT" in a blue, sans-serif font, with "THE PCB EXPERTS" in a smaller, blue, sans-serif font below it.The logo for elSYCA features a stylized blue circuit board icon to the left of the text "elSYCA" in a blue, sans-serif font.The logo for EMA Design Automation features the word "EMA" in a bold, red, sans-serif font, with "Design Automation" in a smaller, blue, sans-serif font to the right.The logo for ESPEC features the word "ESPEC" in a stylized, orange, sans-serif font.The logo for FINELINE features the word "FINELINE" in a bold, black, sans-serif font, with "EXCELLENCE IN PCB" in a smaller, black, sans-serif font below it.The logo for FREEDOMCAD features a stylized blue circuit board icon to the left of the text "FREEDOMCAD" in a blue, sans-serif font, with "ELECTRONIC PRODUCT DEVELOPMENT" in a smaller, blue, sans-serif font below it.The logo for GFE features the letters "GFE" in a stylized, green, sans-serif font.The logo for luminovo features a stylized blue circuit board icon to the left of the word "luminovo" in a blue, sans-serif font.The logo for McL features the letters "McL" in a stylized, blue and yellow, sans-serif font, with "Millennium Circuits Limited" in a smaller, black, sans-serif font below it.The logo for NCAB GROUP features a stylized green circuit board icon to the left of the text "NCAB GROUP" in a bold, black, sans-serif font.The logo for the 25th anniversary features the number "25" in a large, blue, sans-serif font, with "Newgrange Design" in a smaller, blue, sans-serif font to the right, and "Celebrating 25 years" in a smaller, blue, sans-serif font below it.

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Seeing Electronics Manufacturing Through New Eyes

A new perspective on electronics manufacturing reveals how continuous learning, quality and process improvement shape both personal growth and the products that power modern technology.

by WILL O'NEIL

WHEN I ENTERED electronics manufacturing earlier this year, I quickly realized I was stepping into a field unlike anything I had experienced before. I came in with a strong interest in technology and a background that had already exposed me to electronics, troubleshooting and repair, but this industry opened my eyes to a much larger and more complex world. It was not just about understanding individual components or fixing a single piece of equipment. It was about seeing how people, processes, standards, customers, materials and technology all come together to build products that serve real-world purposes.

My background has always involved technology and electronics in one way or another. Growing up, I was fortunate to take computer classes through the Boys & Girls Club, and that's where my fascination with technology really began. I still remember how exciting it was to use computers not just as tools, but as systems I could explore, learn about and eventually improve. Before long, I was helping repair and upgrade computers. I learned how to replace parts, diagnose problems and think through issues step by step. That interest eventually led me into robotics and later into careers involving electronics repair, from biomedical robotics and fire alarm systems to other electronic equipment. Each experience gave me another piece of knowledge and helped me become more comfortable working with technology in practical, hands-on ways.

Throughout those experiences, I was always curious about how things worked. I wanted to understand what was happening behind the scenes and why circuits behaved the way they did. If something failed, I wanted to know what caused the failure. That curiosity led me to spend a lot of time researching electronics on my own and learning as much as I could. I developed a habit of looking beyond the surface level of a problem and trying to understand the process behind it. That mindset has helped me throughout my career, and it continues to help me now.

Even with that background, joining RBB challenged me in ways I didn't expect. I thought my experience with troubleshooting and repair would prepare me for most of what I would encounter, and in some ways it did; It gave me a foundation to build on. I quickly learned that electronics manufacturing requires a different kind of thinking, however.

Instead of focusing only on a single device or repair, I had to think about the full process: how a product is built, how

it is tested, how information is documented and how each step affects the final result.

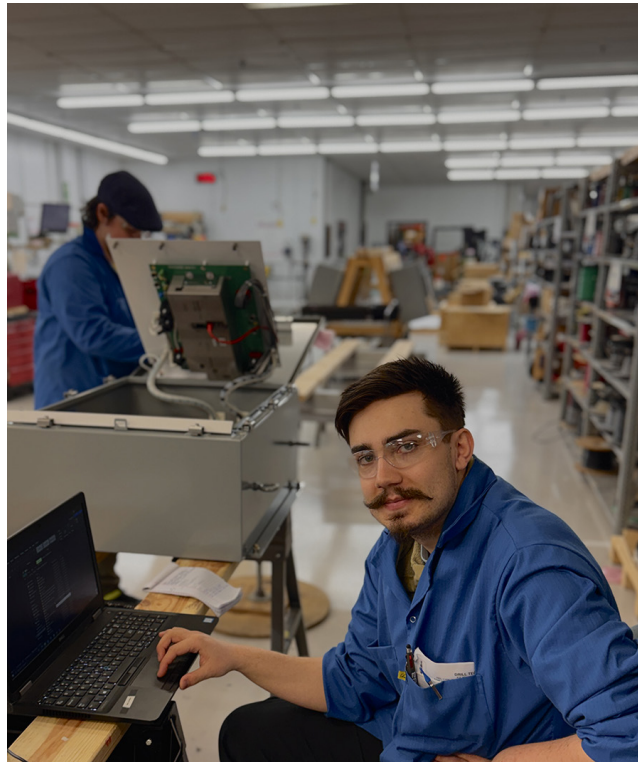


Figure 1. Joining a new team provided a firsthand look at the people, processes and collaboration behind electronics manufacturing.

I was used to working with a small number of products that were built the same way every time. Now, that's rarely the case. When I first started, it took some time to grasp the complexity of a manufacturing environment where different products move through the facility every day. What we're working on changes constantly. One day I'm troubleshooting a particular assembly, the next day I'm learning a new process, using different test equipment or supporting an entirely different product.

The environment can feel a bit overwhelming at first because there is so much information to absorb. There are drawings to interpret, procedures to follow, customer requirements to understand, and quality expectations that cannot be ignored. Over time, I began to see that this variety is one of the things that makes the work valuable. It forces me to keep learning and prevents me from becoming too comfortable with only one way of doing things.

What surprised me most is how much I've come to enjoy that variety.

No two days are the same, and that's what keeps the job interesting. Every new project gives me an opportunity to learn something different. It's fun to see both the similarities and the differences among products, processes, and customer requirements. There is always a new challenge waiting around the corner. Sometimes that challenge is technical, such as identifying why a unit is not performing as expected. Other times it is procedural, such as learning the correct documentation or understanding the reasoning behind a specific requirement. Either way, every challenge has pushed me to become more adaptable and more aware of the bigger picture.

The industry itself has also been eye-opening.

Before joining RBB, I knew PCB manufacturing existed, but it was one of those industries that quietly operated in the background of everyday life. I never really stopped to think about it. Now I see it everywhere. Nearly every device we touch, use, or rely on contains a printed circuit board. Whether it's medical equipment, industrial controls, communications systems, transportation technology or consumer electronics, PCB manufacturing plays a role.

Even products that seem simple on the outside often rely on electronic assemblies inside. That realization changed the way I look at the world around me. Instead of seeing only the finished device, I now think about the people and processes that make it function.

Working in this industry has felt like getting a glimpse behind the curtain and finally seeing how so much of modern technology becomes reality.

Another thing that immediately stood out to me is the emphasis placed on quality, standards and documentation. Electronics manufacturing may be constantly evolving, but it's built on a foundation of consistency and accountability. Between AS9100, ISO 9001, IPC standards, military requirements, traceability and customer-specific expectations, every detail matters. These standards are not just paperwork or formalities. They exist because the products being built may be used in environments where reliability is critical. A small mistake in handling, assembly or testing can have consequences far beyond the production floor. That level of responsibility has made me look at quality in a more serious and practical way.

I've learned very quickly that success in this industry isn't just about technical skill. It's about precision, discipline and making sure every process is documented and followed correctly. The details matter because the products we build matter. It takes patience to slow down, verify information, and ensure the work is done the right way rather than simply the fastest way. Good manufacturing depends on people who care enough to pay attention to the small things.

As I continue growing in my role, I've become increasingly interested in operational excellence, process improvement, and automation. I enjoy figuring out how systems work, but I also enjoy understanding how to make them work better. Manufacturing is full of opportunities for improvement because every process has steps, handoffs, decisions and potential delays. Sometimes improvement means simplifying documentation. Sometimes it means finding a better way to organize information, reduce repeated work, or make a process easier for the next person to follow. I like the idea that small improvements can build on one another and eventually create a much stronger system.

Looking ahead, I believe the future of manufacturing will be heavily influenced by Industry 4.0 technologies and artificial intelligence. In many ways, we're already there. AI is finding applications throughout the manufacturing process, from PCB design and inspection to scheduling, documentation, quoting, and process management. Industry 4.0 is not only about adding new technology for its own sake. It is about connecting information, improving quality, and helping people make better decisions faster. In a manufacturing environment where priorities can change quickly, having accurate information available at the right time can make a major difference.

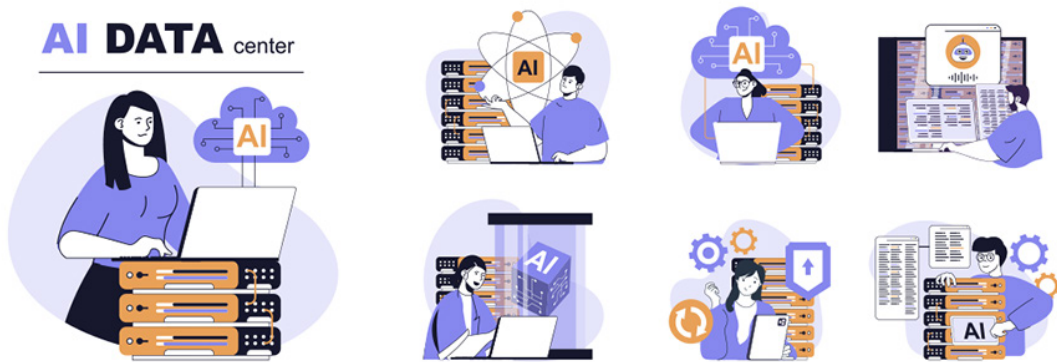


Figure 2. Artificial intelligence is becoming an increasingly important tool in electronics manufacturing, helping streamline design, inspection, documentation, scheduling and other production workflows while keeping people at the center of decision-making.

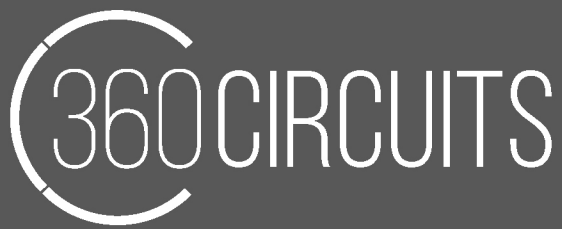
I don't see AI replacing the people who make this industry successful. Instead, I see it as a tool that can help eliminate repetitive work, improve efficiency, and allow skilled employees to focus on solving bigger problems. Companies that learn how to effectively integrate these technologies will be positioned to accomplish even more. Humans will still be essential to understanding context, making judgment calls, solving unusual problems, and bringing practical experience to the process. AI can support that work, but it cannot replace the value of people who understand the products, the customers, and the realities of the production floor.

What excites me most is that RBB is already moving in that direction. We're exploring new systems, new technologies and new ways of improving how we work. Our workflow may be anything but typical, but if there's one thing I've learned during my time here, it's that this team embraces challenges. In a field where products, requirements and technologies continue to evolve, standing still is not really an option. The ability to learn and improve is what allows a company to stay competitive and continue meeting customer needs.

Electronics manufacturing may not always be visible, but it is one of the pillars of modern society. Without it, many of the innovations we rely on every day simply wouldn't exist. It supports other industries, enables new ideas, and helps turn designs into functioning products. The work can be detailed, demanding and sometimes difficult, but it is also meaningful because the result often supports something much larger than the assembly itself.

As someone new to the industry, that's probably been my biggest takeaway; electronics manufacturing doesn't just support technological advancement, it helps make it possible. My time at RBB has shown me that this field combines technical skill, problem-solving, quality, teamwork, and continuous learning in a way that is both challenging and rewarding. I still have a lot to learn, but that is part of what makes the opportunity exciting. Every day gives me another chance to build my knowledge, contribute to the team and better understand the role this industry plays in the world around us. 

WILL O'NEIL is a test technician at RBB (rbbsystems.com), where he supports the testing and validation of electronic assemblies while continually expanding his knowledge of electronics manufacturing; woneil@rbbsystems.com.



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The Workday You Lose to Documentation, and How to Get It Back

AI can turn routine reports, meeting notes and work instructions into editable first drafts, helping engineering teams reclaim hours each week for higher-value work.

by SEAN PATTERSON

It's 5:15 p.m. on a Friday, the floor has gone quiet, the last shift has clocked out, and you are still at your desk. You are not solving a yield problem; you are writing the weekly production summary from a legal pad covered in notes you scribbled between meetings.

Maybe it is not the production summary for you. Maybe it is the meeting recap nobody will read, the work instruction you have rewritten four times, or the customer email you have started and deleted twice. The real work, the engineering and the problem solving, ended hours ago, and what is left is the writing about the work.

I spent the better part of my career in operations across submarines, PCB shops and high-volume logistics, and for a lot of that time my real job was paperwork. Travelers, status reports, corrective actions, shift handoffs. I was strong on the technical side, but I lost evenings to documentation that any clear-thinking assistant could have drafted for me. The tools to fix it did not exist yet. Now they do, and most of us still are not using them.

Here is the promise of this article, and I mean it literally. You can get back three to five hours every week, starting Monday, without buying a single new system. Not by working faster, but by handing the first draft of your documentation and reporting to AI, then doing what you are actually good at, which is reviewing and deciding.

This is the easiest, highest-return place to start. Let's get your evenings back.

A Full Workday, Every Week

For most people in design and manufacturing, documentation and reporting take about an hour a day, if not more. That is five hours a week, and it is the part of the job that never shows up in your title or your performance review.

Put a real number on it: that's five hours a week, which is 250 hours a year. It is one person spending a full month of work, every year, just typing. If you run it across a team, 10 people at a fully loaded rate of \$60 an hour comes to roughly \$150,000 a year. That is real money, and you are spending it on the lowest-value thing your skilled people do.

And this is the work that hides in plain sight. It never shows up on a traveler or a production schedule, so nobody

manages it, and it quietly grows year over year. In a shop with thin margins and open positions you cannot fill, it is the most expensive problem nobody puts on a report.

Much of that time disappears into routine documentation: preparing status and production reports such as weekly summaries, shift handoffs and management updates; writing meeting recaps and tracking action items; creating technical documentation and work instructions from rough notes; drafting customer emails, supplier follow-ups and cross-functional communications; and completing corrective actions and quality records that must be clear, accurate and well documented.

Every one of these is a first draft AI can produce, leaving you to do the part that actually requires your judgment.

Stop Writing and Start Editing

Here is the mental shift that makes all of this work, and it is bigger than any single prompt. Most of us were taught that writing a report means starting with a blank page. You stare at it, organize your thoughts, hunt for the words, and an hour later, you have a document. The blank page is the expensive part, since it is where time goes and where dread lives.

AI removes the blank page and gives you your raw material, the notes, the numbers and the bullet points you already have, and it hands you a complete first draft in seconds. Your job changes from author to editor as you edit where your expertise actually lives. You can look at a draft and know in 10 seconds that the scrap number looks wrong, that the tone is off for this customer, or that it buried the one issue that mattered. That judgment is the part no AI has, and it is also the part that was never the bottleneck.

This reframe answers the question every careful engineer asks first: if you can trust it. You do not have to, since you are not directly publishing what the AI writes. You are reviewing it, the same way you would review a draft from a new hire. You still own every word that leaves your desk, and the accountability never moves.

A status report or a meeting recap is low risk, so it is a safe place to start. If the draft is wrong, you catch it and fix it, and you have lost nothing. You are building the habit and the trust on tasks where a mistake costs you a few minutes, not a board.

Context and your own raw notes are the two things that make a draft worth editing. The more you tell AI about the situation, who it is for, what format you need, and what the constraints are, the less editing you do. Here is where you put it to work by feeding it your messy notes, telling it exactly what you want back, and letting it carry the blank page so you never have to again.

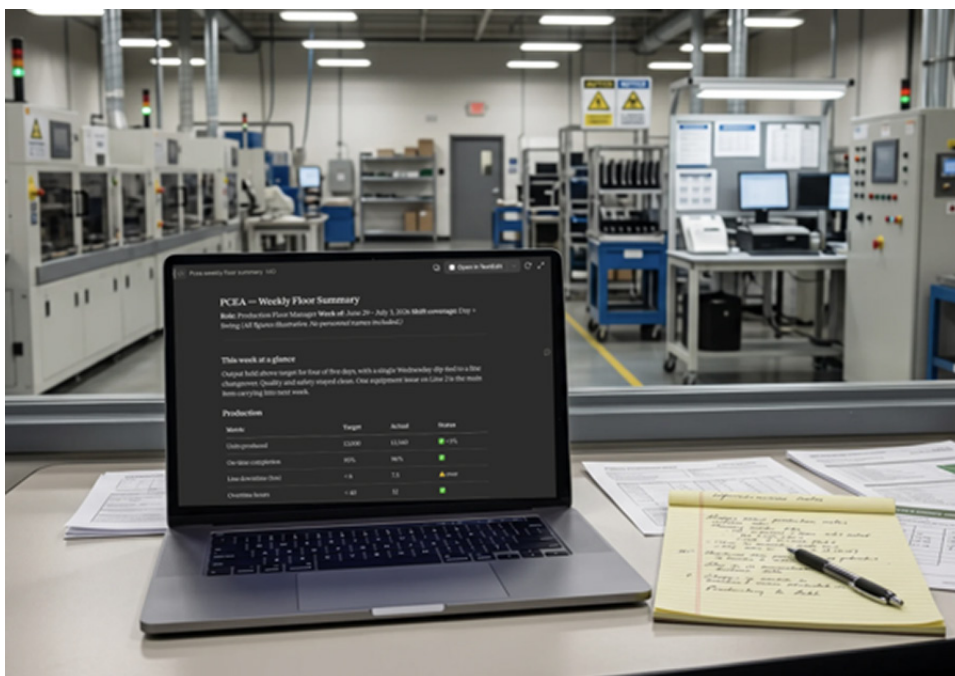


Figure 1. A structured AI prompt converts raw production notes into a standardized weekly report, allowing engineers to spend less time drafting documentation and more time reviewing and making decisions.

A Worked Example: The Friday Report That Writes Itself

Let's go back to that 5:15 p.m. Friday. [The last article](#) was about turning one-off prompts into repeatable workflows, and the weekly report is the clearest place to begin. You have a legal pad of notes from the week, which you would normally spend an hour turning into the production summary your plant manager expects. Instead, open an AI chat tool and set up this prompt once. It becomes your reusable template, and the only things that change week to week are the notes you drop at the bottom and occasional edits to the prompt as you get familiar with AI's capabilities.

Here's a prompt to try:

You are helping me, the operations manager of a PCB fabrication shop, write my weekly production report for the plant manager. The report goes to leadership, so keep it clear, factual, and brief. No hype.

Use exactly these sections:

- 1. Summary (three sentences: output versus plan, biggest win, biggest issue)**
- 2. Output and Yield (key numbers, plan versus actual)**
- 3. Quality and Scrap (top issues, status, owner)**
- 4. Downtime and Maintenance**
- 5. Staffing**
- 6. Risks and What I Need From Leadership**

Rules:

- Use only the information in my notes below. Do not invent numbers.
- If something important for a section is missing, list it under “Missing info to confirm” instead of guessing.
- Keep the whole report under one page. Use short bullets, not paragraphs.

Here are my raw notes for this week:

[paste your notes here, however messy]

The two rules about numbers are the most important lines in that prompt. “Do not invent numbers” and “list what is missing instead of guessing” keep the AI honest and turn your review into a 30-second checklist rather than a trust exercise.

As a result, you get a clean, one-page report in your exact format, your numbers in the right places, and a short list of anything you forgot to mention. Now you do the part you are good at: reading it. Fix the line where the scrap cause is only half right. Delete the risk that already resolved itself and any other minor tweaks you may have. The hour became five minutes, and those five minutes were judgment, not typing.

This is a standing habit you should continually work on. Keep the prompt in a note and run it every Friday without deciding to. As we said back in [Article 1](#), a gym membership only works if you show up. So, pick the one recurring report you dread most and run through this every single time it is due. Once that feels automatic, add a second one. That is how three to five hours a week come back, one habit at a time.

Same Recipe, Any Document

The Friday report is just one use. The same structure works for anything on that earlier list because the recipe never really changes. You give AI your role and context, hand it your raw notes, and tell it the exact format you want back. Right after a production meeting, paste your notes in and ask:

Turn my rough meeting notes below into two things: a short summary of five bullets or fewer, and an action-item table with columns for Owner, Task, and Due Date. Use only what is in my notes. If an action has no clear owner or date, mark it as TBD rather than guessing.

Notes: [paste your notes here]

You get a clean recap and a table you can forward in under a minute, with the gaps flagged so you know exactly what to chase down. Swap a few lines and the same recipe drafts a work instruction from rough steps, a customer email from a handful of facts, or a corrective action from your findings.

Now Multiply It: From Your Desk to Your Team

Everything so far saves one person, you, a few hours a week. The real return shows up when you refuse to stop there and ask a different question. What if everyone on your team got those hours back?

This is where managers get it wrong, since the instinct is to treat AI as a way to automate a role away. Stop having a person write the reports, let the software do it, and cut the headcount. That is the old technology-as-replacement playbook, and in my experience, it fails every single time. You lose the judgment, you lose trust, and you usually end up with a worse report and a more nervous team.

The better move is the one this whole series is built on. Don't automate your team, teach your team to automate. The win is not removing the person who writes the production report. It is teaching that person, the next one, and the new hire who starts in three months to hand the first draft to AI and spend their time on the work they are best at.

Do the math again, this time across the floor. Five hours a week per person, ten people, and you have recovered most of a full-time-position-worth of capacity without losing a single person or their hard-won knowledge. That is the difference between buying automation and building capability.

The part you cannot delegate is that you have to go first. Run your own Friday report through AI for a month. Once you have felt the hour disappear, share the exact prompt at your next team meeting and show the before-and-after. Let people copy what already works for you. Adoption spreads by demonstration, not by memo.

The Habit Is the Whole Game

Knowing AI can write your reports changes nothing, but doing it every week changes everything. Be honest about that, because the people who actually get their evenings back are not the ones who found this article interesting. They are the ones who built a routine and kept it.

So make it small and make it fixed by picking the one document you dread most- the weekly report, the shift handoff, the meeting recap- and give it a standing appointment. Same prompt, same time, every week, until you stop noticing you are doing it. Do not add a second task until the first one is automatic because a habit you keep beats five you abandon.

The hours you save here are not the prize; they are the budget. Once your team has some time back and more confidence, you can aim that recovered time at things the vendors said you could not afford to build, like real monitoring for the plating line or simple sensors on machines that were running long before anyone said the word internet. 

SEAN PATTERSON is an accomplished executive with extensive C-suite experience across CRO, COO, and CTO roles who now specializes in humanizing artificial intelligence implementation in business environments, particularly manufacturing; sean@crossgen-ai.com.

Patterson's unique approach to AI implementation stems from his multifaceted leadership experience in the PCB industry, including serving as COO and CTO & head of AI at Summit Interconnect, various senior positions at TTM

Technologies, and CRO of Nano Dimension. He built Amazon's tractor trailer division and healthcare platforms. He currently serves as COO of StartGuides, providing military technology working backwards from the soldier. He is also on several nonprofit AI advisory boards in education.

Patteson brings practical insights into how PCB manufacturers can approach AI adoption strategically. His methodology emphasizes cultural adoption from the top, employee empowerment, and then automation. His approach to AI implementation is captured in his often-quoted principle: "AI adoption is not something a leader can delegate."

Patterson holds a master's in nuclear science and engineering from MIT and a bachelor's in systems engineering with a focus on robotics from the United States Naval Academy.

AI Is Reshaping the Semiconductor Supply Chain

AI-driven demand is reshaping semiconductor supply chains, prompting manufacturers to prioritize capacity, adjust pricing and tighten availability for mature-node devices.

by MARC SCHWANBECK

The second quarter of 2026 made one thing clear: AI's influence on the semiconductor market has moved well beyond processors.

What started as surging demand for advanced computers is now reshaping manufacturing priorities, capital allocation and supplier behavior across the entire industry. That includes the analog, power management, automotive and industrial categories that customers depend on every day.

Supply hasn't tightened to 2021–2022 levels. But the easy, oversupplied market of 2024 and early 2025 is fading. Pricing discipline is returning, lead times are shifting and the sourcing strategies that worked 18 months ago deserve a second look.

Demand: AI Is Setting the Pace

AI infrastructure investment was again the defining force in the second quarter. Hyperscale cloud providers accelerated data center deployments, continued driving demand for accelerated computing platforms, networking equipment and advanced power systems.

The ripple effects are reaching further down the supply chain than many expected. Reuters reported that [STMicroelectronics raised its 2026 data center revenue target](#) on the strength of AI-related demand, a signal that industrial and power semiconductor technologies are increasingly tied to next-generation computing buildouts.

Beyond AI, industrial *automation*, medical electronics, networking infrastructure and transportation markets continued a steady recovery as excess inventory normalized.

The story isn't broad shortages; it's one of selective tightening in product families where manufacturers are choosing to prioritize AI-related applications.



AI-driven demand is reshaping semiconductor manufacturing priorities, influencing capacity allocation across the supply chain.

Supply: Pricing Actions Are Back

Supplier price increases were seen across multiple categories, driven by higher production costs, ongoing investment in advanced manufacturing capacity and improving demand in industrial and automotive markets.

Infineon Technologies announced its [second price increase of 2026](#), effective July 1, and raised its outlook amid stronger AI-driven demand for data center power solutions. Memory markets stayed firm as suppliers continued shifting capacity toward higher-value AI server products, with [TrendForce's June spot market update](#) flagging tightening DDR4 availability and strengthening DDR3 pricing as a direct result.

The pattern is consistent: Manufacturers are emphasizing higher-margin technologies and disciplined capacity management. Procurement teams sourcing analog devices, embedded controllers, industrial semiconductors, and power management products should expect this pressure to continue.

What to Watch by Market

Commercial and industrial. Investment in factory automation, industrial controls and edge computing strengthened throughout the quarter. Inventory levels have largely normalized, but AI-driven capacity allocation is beginning to tighten availability for select analog, power management and embedded control devices. I recommend monitoring lead times closely for mature-node components supporting long-life equipment.

Automotive and transportation. Demand remained stable, supported by vehicle electrification, the proliferation of

advanced driver assistance systems (ADAS) and rising electronic content per vehicle. Power semiconductors, microcontrollers, sensors and connectivity solutions should stay resilient through the second half of 2026, but selective supplier pricing actions could complicate sourcing strategies for automotive manufacturers and Tier 1 suppliers.

Medical manufacturing. Medical device procurement teams have always prioritized supply continuity over price. That instinct is well-placed right now. As semiconductor manufacturers allocate more capacity toward AI applications, we believe diversified sourcing strategies for analog, power, and embedded processing technologies with extended lifecycles are more important than ever.

Aerospace and defense. Defense modernization and aerospace electronics investment support stable demand for high-reliability components across avionics, radar, communications and mission-critical systems. Long qualification cycles make strategic sourcing partnerships essential as manufacturers continue to optimize capacity for advanced computing.

The Bottom Line for Procurement Teams

The market is stable, but it's not static. AI-driven manufacturing priorities and returning supplier pricing actions are creating pockets of tighter supply in the mature semiconductor technologies that industrial, automotive, networking and embedded applications depend on.

The organizations best positioned heading into the second half of 2026 will be those that maintain diversified sourcing across qualified supply partners, stay ahead of supplier pricing actions rather than reacting to them, and secure critical components before availability windows tighten.

This isn't a crisis, but it isn't a comfortable market either. Navigating it successfully requires flexible sourcing options and a proactive approach to supply chain management. 

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Claude Mythos and Project Glasswing: What OEMs Need to Know Now

As AI transforms cybersecurity, OEMs must rethink embedded product security before tomorrow's threats become today's vulnerabilities.

by RAJESHPAL SINGH

In April, Anthropic announced Claude Mythos – its most capable AI model to date – but chose not to release it publicly due to unprecedented cybersecurity risk. Instead, Anthropic launched Project Glasswing, a defensive coalition of over 50 major technology organizations tasked with finding and fixing critical software vulnerabilities before similar capabilities proliferate.

For OEMs building connected EMS products, Project Glasswing signals an accelerating shift in the threat landscape, reinforces growing regulatory expectations around secure-by-design engineering, and creates practical opportunities to strengthen product security across the design, manufacturing and field-service lifecycle. Action taken now will compound in value.

Claude Mythos, Anthropic's publicly confirmed but unreleased frontier AI model, has demonstrated the ability to autonomously discover software vulnerabilities, prompting the launch of Project Glasswing, a defensive initiative that gives select technology partners early access to identify and remediate critical flaws. As AI accelerates vulnerability discovery, OEMs with long-lifecycle embedded products face increased exposure from software weaknesses that can persist long after certification. At the same time, cybersecurity regulations are becoming more closely aligned with product safety requirements, raising compliance expectations for manufacturers. While the challenge is growing, OEMs can reduce risk through practical, phased security improvements without undertaking a complete product redesign.

What is Claude Mythos?

Like previous Claude models, Anthropic's newest frontier AI model, Mythos, is a general-purpose large language model (LLM) capable of reasoning, writing code and solving complex problems. What distinguishes Mythos from its predecessors is a step-change improvement in autonomous cybersecurity tasks.

According to [Anthropic's official system card](#) and the Frontier Red Team blog, Mythos Preview demonstrated the ability to independently discover thousands of previously unknown software vulnerabilities across every major operating system and web browser, and to develop working exploits without human guidance.

Critically, Anthropic assessed that these capabilities exceeded those of previous models by a significant margin and were advanced enough to pose a dual-use risk: the same skills that accelerate the discovery of defensive vulnerabilities could, in the wrong hands, dramatically lower the barrier to large-scale cyberattacks.

On that basis, Anthropic decided not to make Claude Mythos Preview generally available.

What is Project Glasswing?

Rather than withholding its new model entirely, Anthropic launched [Project Glasswing](#) on the same day as the Mythos Preview announcement. Project Glasswing is a defensive cybersecurity initiative that provides controlled access to Claude Mythos Preview to a curated set of organizations responsible for globally critical software infrastructure.

Project Glasswing's launch partners include many of the world's largest technology organizations, including Amazon Web Services, Apple, Broadcom, Cisco, CrowdStrike, Google, JPMorganChase, The Linux Foundation, Microsoft, Nvidia and Palo Alto Networks.

More than 40 additional organizations with roles in critical software infrastructure have also received access. Anthropic has committed \$100 million in usage credits to support participants, alongside direct funding for open-source security work.

Project Glasswing's stated purpose is to use Mythos Preview's capabilities to find and remediate critical vulnerabilities before similar AI capabilities become widely accessible, effectively creating a window for defenders to reduce the global software attack surface ahead of broader proliferation.

Anthropic has stated that it does not plan to make Mythos Preview generally available but intends to develop safeguards over time that will allow Mythos-class capabilities to be deployed safely at scale.

Why Project Glasswing Matters

AI can accelerate vulnerability discovery and exploitation. Traditional security research relies on skilled human analysts manually working through large code bases, or on specialized tooling that scans for known vulnerability patterns. Both approaches are time-intensive and produce incomplete coverage of complex, real-world codebases.

Advanced AI models like Claude Mythos Preview represent a different class of capability. These systems can read and reason about large volumes of code, identify subtle logical flaws and, in documented cases, autonomously develop working exploits. At a conceptual level, this shifts the economics of vulnerability discovery. Tasks that previously required months of expert effort may become achievable in hours or minutes.

Connected products can potentially be impacted. For OEMs whose products contain embedded software – whether in smart appliances, industrial controllers, medical devices or transportation systems – the relevant concern

is not today's adversarial capability, but the trajectory.

Two characteristics of embedded products make them particularly worth examining in this context:

- **Long deployment lifetimes.** Many embedded systems operate for 10–30 years after manufacture. Software that was considered secure at certification may contain latent vulnerabilities that were never identified due to prior tooling limitations, but could, in principle, be discovered by more capable systems in the future.
- **Constrained update pathways.** Unlike enterprise software, many embedded products lack reliable over-the-air update mechanisms, particularly in regulated environments. This can mean that even a known vulnerability remains unpatched in the field for extended periods.

Neither of these characteristics is new. What Project Glasswing signals is that the speed and breadth of vulnerability discovery may increase, and that the window between discovery and exploitation could shorten.

The extent to which these dynamics translate into actual attacks on specific embedded product categories within a defined timeframe is not precisely predictable, so OEM teams should treat this as a risk-planning horizon rather than a fixed outcome.

Implications for the EMS Product Lifecycle

Design and architecture. Secure-by-design principles are the most efficient point of intervention. Products architected with minimal attack surface, hardware-enforced trust boundaries, and defense-in-depth are more resilient to both current and future vulnerability discoveries, regardless of the discovery method. Threat modeling during early design stages, rather than as a late-stage audit, is increasingly the expected baseline under frameworks such as IEC 62443, ETSI EN 303 645 and the EU Cyber Resilience Act.

Component selection decisions made at the design stage, including the choice of third-party open-source libraries, connectivity stacks, and SoC firmware, determine much of the downstream surface of vulnerabilities. Proactive assessment of a component's security posture, including the history of known vulnerabilities and the vendor patch cadence, should be part of the standard design review process.

Verification and validation. Secure firmware practices, including code signing, boot chain integrity verification, and separation of privileged execution contexts, reduce the exploitability of vulnerabilities even when they are present. These practices are well-established; where they are not already implemented in a product line, prioritization is warranted.

Software Bill of Materials (SBOM) and Vulnerability Exploitability eXchange (VEX) documentation are increasingly required by regulation and customer procurement in sectors including medical and defense. Maintaining a current SBOM enables faster triage when new vulnerability disclosures affect components used in a product.

Fuzz testing at scale – the automated generation of malformed inputs to identify unexpected software behavior – is a well-supported technique for finding vulnerabilities earlier in the development cycle. AI-assisted tooling is beginning

to improve coverage and efficiency here, offering OEM teams access to previously scarce capabilities.



Figure 1. As AI accelerates software vulnerability discovery, OEMs are being urged to strengthen secure-by-design practices, SBOM management and product lifecycle cybersecurity.

Manufacturing and supply chain. The manufacturing phase is a critical control point for device identity and cryptographic credential provisioning. Products shipped without unique device identities or with default credentials that are not changed at commissioning represent preventable exposure.

Secure provisioning, such as the controlled injection of unique keys, certificates and configuration at the time of manufacture, establishes a verifiable root of trust that supports lifecycle management.

Supply chain integrity, ensuring that components and firmware are authentic and have not been tampered with between manufacture and field deployment, is a related concern. Trusted component sourcing, chain-of-custody documentation and bill-of-materials verification are all relevant controls.

Field operations and lifecycle management. Over-the-air (OTA) update capability is increasingly a product design requirement rather than an optional feature. Products that can receive authenticated, integrity-checked firmware updates retain the ability to respond to newly discovered vulnerabilities throughout their deployed lifetime. Where OTA is not feasible – for example, in certain safety-certified environments – defined patch delivery and service processes, including field update procedures, provide a fallback.

Patch SLA policies with defined commitments to assess and respond to disclosed vulnerabilities within a stated timeframe are becoming standard in regulated sectors and are expected by sophisticated OEM customers. End-of-life strategies that define the point at which security support ceases and communicate this clearly to customers are equally

important for long-lifecycle products.

What OEMs Should Do Now

1. **Understand current exposure.** The first step is understanding where an organization may be vulnerable. A cross-functional review involving engineering, cybersecurity, product management and other relevant teams can help assess what Claude Mythos and Project Glasswing could mean for the product portfolio. Products that rely on major operating systems, browsers or open-source libraries, such as the Linux kernel, common RTOS variants or networking stacks, should be identified and evaluated, as these technologies may have been analyzed through Project Glasswing. Key software suppliers should also be consulted to determine whether they are participating in the initiative or have received vulnerability disclosures through it, as well as to understand their expected patch release timelines. Finally, responsibility for tracking vulnerability disclosures should be assigned to a designated internal owner so critical updates can be evaluated and addressed as they emerge.
2. **Strengthen the baseline.** Strengthening the cybersecurity baseline begins with establishing a current Software Bill of Materials (SBOM) across the active product portfolio. Products without an SBOM should have one created, with third-party open-source components identified and their patch status documented. Existing update and patch policies should also be evaluated to identify products that lack over-the-air (OTA) update capabilities and to confirm that field update procedures are documented and can be executed when needed. Conducting a structured threat-modeling exercise on a flagship or high-revenue product using methodologies such as STRIDE or TARA can help identify design risks early, while a review of supplier security questionnaires and procurement criteria can ensure they address SBOM availability, patch cadence and secure provisioning capabilities.
3. **Build systematic capability.** Building long-term cybersecurity resilience requires security practices to become part of the product development and manufacturing process. Integrating fuzz testing or other forms of dynamic analysis into the firmware development pipeline can improve the ability to identify vulnerabilities early in development. Manufacturing processes should also incorporate secure provisioning, including the injection of unique device identities and cryptographic credentials on new or updated products. Organizations can further strengthen preparedness by conducting tabletop incident response exercises that simulate a publicly disclosed zero-day vulnerability affecting deployed products, helping uncover gaps in detection, triage and customer communication. Finally, existing cybersecurity practices should be benchmarked against the regulatory requirements of target markets to identify compliance gaps and prioritize future improvements.
4. **Establish a durable posture.** Creating a lasting cybersecurity strategy requires planning beyond immediate threats. A product security roadmap should outline priorities for architecture updates, secure-by-design requirements for next-generation products and plans for addressing technical debt in existing product lines. Patch service-level agreements (SLAs) should define response timelines for critical, high- and medium-severity vulnerabilities and be clearly communicated to customers. Regular third-party security assessments, including penetration testing, component vulnerability scanning and supply chain reviews, can help validate security controls and support regulatory compliance. In addition, close collaboration with EMS partners can strengthen secure provisioning, SBOM management and manufacturing-phase security practices as products move into

new design cycles or production refreshes.

The emergence of AI-driven vulnerability discovery reinforces something we have observed building across our customer base over recent years: cybersecurity is no longer a separate workstream appended to a hardware project. It is a foundational quality dimension that affects design choices, supplier selection, manufacturing processes and field service expectations.

Taking a secure-by-design approach, we support OEM engineering teams in assessing product architectures for security risk early in the design cycle, including component selection, connectivity surface and debug/update interface exposure. We also offer SBOM and VEX support, helping customers develop and maintain software bill of materials documentation for products we manufacture, supporting traceability and vulnerability triage.

Our secure provisioning practices ensure manufacturing-phase provisioning processes that inject unique device credentials, cryptographic keys and configuration in controlled, auditable conditions, while our trusted supply chain practices include authorized channel procurement and component authenticity controls relevant to embedded product integrity.

When it comes to compliance-readiness, we assist customers in documenting manufacturing-phase evidence for cybersecurity regulatory submissions, including IEC 62443, ETSI EN 303 645, and the EU Cyber Resilience Act.

[Post-production](#), we also offer lifecycle patch and field support by providing post-market logistics and field service options relevant to products requiring firmware update delivery or managed EOL transitions.

A Balanced Perspective

Claude Mythos and Project Glasswing represent a genuine inflexion point in the security landscape; what is unclear is the rate at which comparable capabilities will proliferate to other actors, the extent to which embedded product categories in OEM markets will be specifically targeted, and whether the defensive window created by Glasswing will close before widespread exposure occurs.

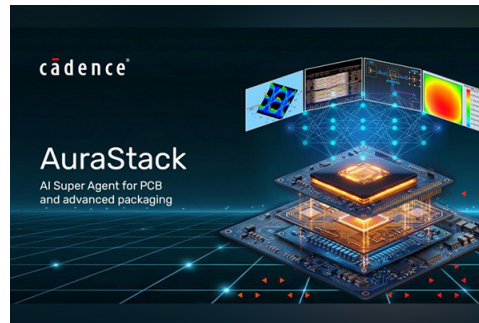
The responsible response is to treat AI-accelerated vulnerability discovery as a directionally established trend likely to intensify, without forecasting specific failure modes or timelines that cannot currently be substantiated. Overreaction – such as product recalls unsupported by specific evidence of vulnerability – is as counterproductive as inaction.

Anthropic's decision to restrict Mythos and invest in defensive infrastructure reflects a considered judgment about dual-use risk. The EMS and OEM community can play a complementary role by building products that are harder to exploit, more transparent in their software composition, and more capable of receiving security updates throughout their operational life. 

Ed.: This article is first published in the [Escatec blog](#) and is republished with permission.

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PCD&F



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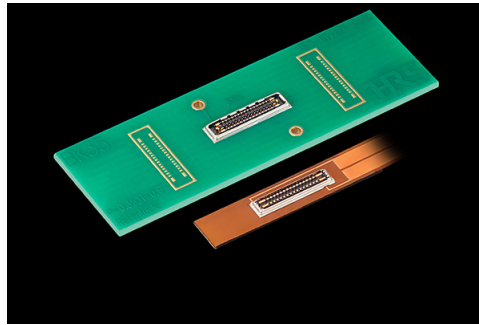


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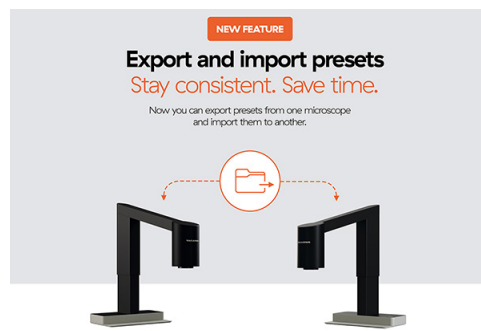


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Assembly Reliability

“Reliability Analysis and Parameter Optimization of Board-Level BGA Packaging Structures under Thermal-Drop Impact Load”

Authors: Yanxi Sun, *et al.*

Abstract: This study investigates the reliability of a board-level BGA package structure when subjected to simultaneous thermal and drop impact loads. The investigation encompasses the effects of dimensional parameters on the stress and fatigue life of solder balls. The findings of this study provide a theoretical foundation for enhancing the reliability of BGA package structures under the sequential coupling of thermal-drop impact loads. In this work, a three-dimensional finite element model of a board-level BGA package structure is established, and numerical calculations are performed based on thermal-drop impact load sequence coupling. The effects of chip thickness, solder ball height, diameter and array on its temperature field distribution, solder ball stress and average impact life are investigated. Optimization schemes were designed using Taguchi quadrature and surface response method. The optimal combination of structural parameters to minimize solder ball peeling stress was obtained by mathematical-statistical analysis and regression analysis. (*Soldering & Surface Mount Technology*, vol. 37, no. 4, June 2026; <https://www.emerald.com/ssmt/article-abstract/37/4/308/1256208/Reliability-analysis-and-parameter-optimisation-of>)

Chip Stacking

“Die-to-Wafer Hybrid Bonding Technology Down to 1 μ m Pitch for Multi-Die Stacking Integration”

Authors: Melissa Najem, *et al.*

As Moore's Law reaches physical limits, the semiconductor industry is increasingly relying on 3D stacking to enhance performance and energy efficiency. Die-to-wafer (D2W) technology addresses a critical bottleneck in AI accelerator design: interconnect density and bandwidth. Here, the authors demonstrate a functional test vehicle utilizing D2W hybrid bonding with pitches down to 1 μ m. By vertically stacking device layers with ultra-fine pitches, the technology shortens interconnect paths, significantly increasing data transfer speeds while reducing power consumption. Achieving a 1 μ m pitch requires engineering very precise alignment accuracy, the primary challenge for the D2W building block. Additionally, the wafer reconstruction process involving inter-die gap filling (IDGF) demanded optimized chemical mechanical planarization (CMP) to ensure compatibility with subsequent vertical interconnects. Electrical characterization of daisy-chain structures confirmed expected performance and yields for pitches ranging

from 5µm down to 2µm. While the yield at 1µm is limited by the alignment accuracy of existing bonding tools, the team anticipates significant improvements with the introduction of next-generation tools featuring 0.5µm (3σ) alignment capabilities. This demonstration serves as a transitional proof of concept, laying the groundwork for a second-generation test vehicle. The immediate next steps include integrating the D2W technology with vertical interconnections – specifically high-density through-silicon vias (HD TSV) and through-oxide vias (TOV) – facilitated by the intermediate inter-die gap filling (IDGF) process step. (IEEE Electronic Components and Technology Conference, April 2026; <https://www.leti-cea.com/cea-tech/leti/english/Pages/What's-On/Press%20release/Die-to-Wafer-Hybrid-Bonding-Press-Release.aspx>)

Circularity

“From Biotechnological Residues to Biodegradable Printed Circuit Boards: *Aspergillus Niger* Mycelium as a Structural Support Material”

Authors: Nina Oehlsen, *et al.*

Abstract: The electronics industry urgently seeks sustainable, biodegradable alternatives to conventional substrates for printed circuit boards (PCBs) to reduce the environmental impact of electronic waste and CO₂ emissions. Here, the authors introduce a biobased, plastic-like material derived from *Aspergillus niger* mycelium, Animat_{RT}. This material is produced from residual biomass generated in industrial citric acid production, offering a circular-economy approach. The raw mycelial biomass, consisting of spherical pellets, is processed via mold casting and air-drying, consolidating the pellets into a dense, plastic-like monolith (1.23g cm⁻³).

When formed into sheets, Animat_{RT} serves as a viable substrate for low-complexity PCB fabrication, permitting direct ink writing and manual soldering of electronic components. Although its electrical properties are lower than those of FR-2, a common, low-cost PCB laminate made of paper bonded with a phenolic resin, it remains suitable for low-frequency and proof-of-concept applications and, on average, has 56% lower embodied carbon. The mycelium boards disintegrate in water, allowing recovery of operative electronic components, whose functionality was demonstrated by resoldering them onto a conventional PCB. The material exhibits high mechanical performance, with compressive strengths of up to 121MPa, a flexural modulus of 2.3GPa, and a flexural strength of 30 MPa. It is fully biodegradable (ISO 20200), redispersible in water, has low flammability, and favorable thermal insulation properties (0.21W (mK)⁻¹). Heat treatment at 120°C enhances the mechanical properties, improves water resistance, and slows biodegradation. This study demonstrates the first use of biotechnology-derived *A. niger* mycelium as a biodegradable substrate for PCBs, addressing circularity and end-of-life challenges in electronics. (*Cleaner Materials*, vol. 21, no. 100416, September 2026, <https://www.sciencedirect.com/science/article/pii/S2772397626000511>)

Sensors

“Tactile Perception through Fluid–Solid Interaction”

Authors: Arman Goshtasbi, *et al.*

Abstract: Soft tactile sensors elevate robotic touch through enhanced flexibility and adaptability, yet most existing designs depend on embedded electronics that are susceptible to interference and environmental limitations. In this work, the authors leverage fluid–solid interactions to develop a class of soft tactile sensors that operate entirely without electronics at the sensing site. The sensor comprises a fluid-filled elastomeric channel connected to only two external pressure sensors. Touching different regions of the elastomeric surface displaces the viscous fluid, producing distinct pressure patterns that encode both touch position and force. These signals are decoded through a machine learning framework that integrates feature extraction, soft clustering, and adaptive neuro-fuzzy inference to achieve accurate localization and force estimation. We validate this concept through single-point touch localization and force estimation in a linear (1D) sensor and extend the same sensing principle to 2D tactile mapping by routing the channel across the surface using space-filling curves, while maintaining the same minimal hardware setup. This simple approach remains effective in environments where conventional electronic sensors often fail, such as underwater or in the presence of magnetic interference. (*Nature Communications*, Apr. 29, 2026, vol. 17, no. 5784, <https://www.nature.com/articles/s41467-026-72497-3>) 



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