

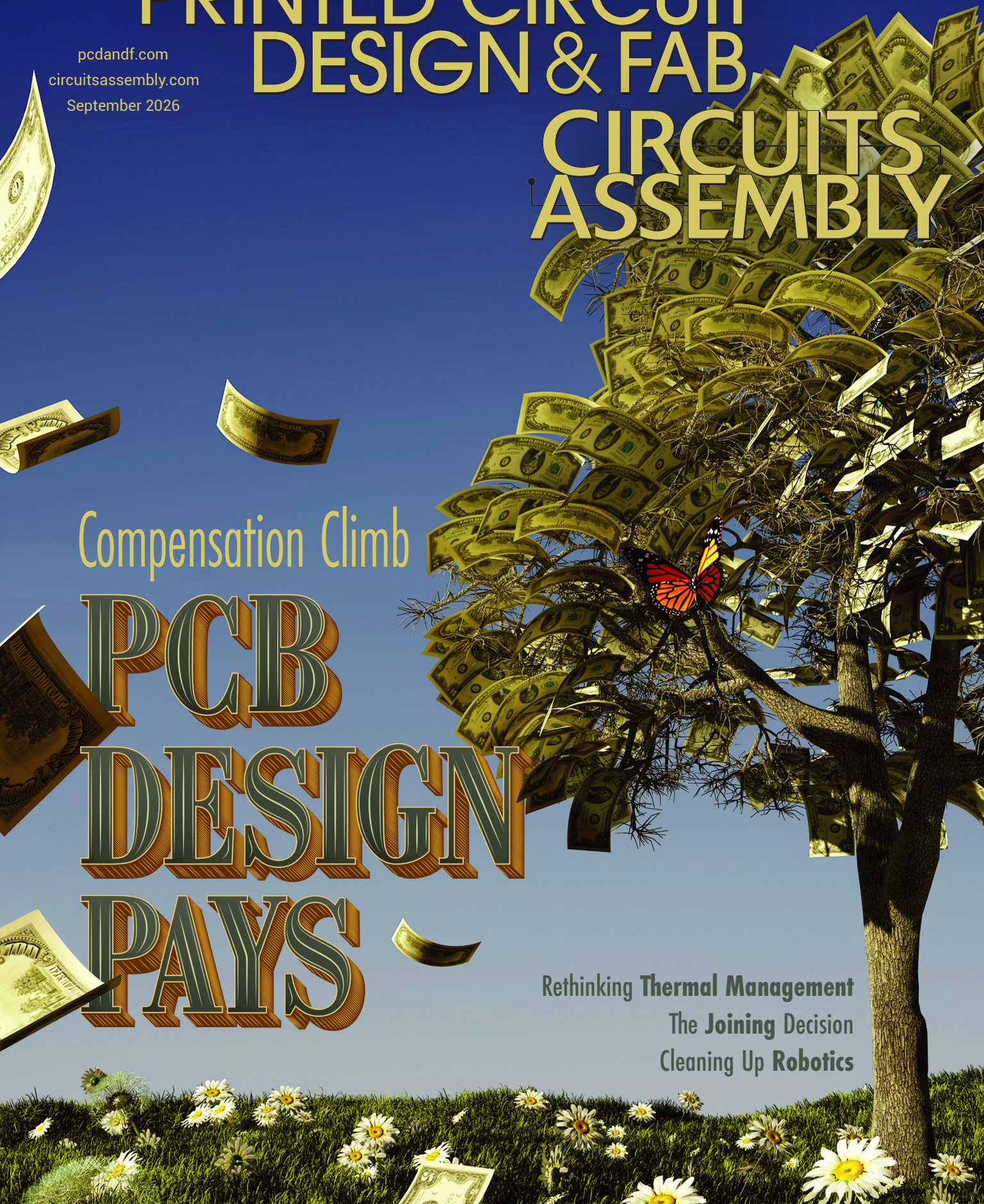
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September 2026

PRINTED CIRCUIT DESIGN & FAB. CIRCUITS ASSEMBLY

Compensation Climb

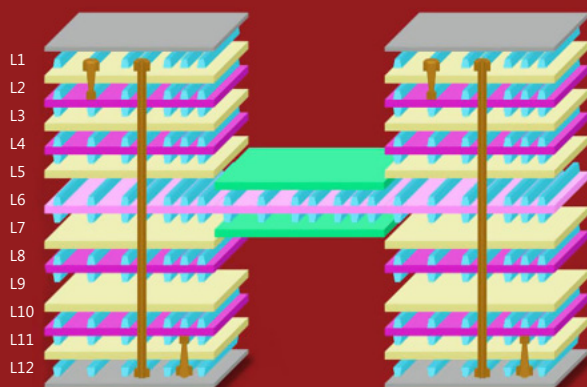
PCB
DESIGN
PAYS

Rethinking Thermal Management
The Joining Decision
Cleaning Up Robotics



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Leaders in HDI Manufacturing

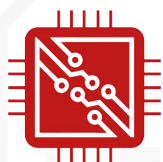


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FIRST PERSON

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The show must go on.

Andy Shaughnessy

MONEY MATTERS

ROI

Who's checking the checkers?

Peter Bigelow

BOARD BUYING

Breakups require a backup.

Greg Papandrew

FOCUS ON BUSINESS

Leadership leaves a mark.

Jake Kulp

REBUILDING THE BASE

The work continues year-round.

Dan Beaulieu

TECH TALK

DESIGNER'S NOTEBOOK

Give every pin room.

John Burkhert, Jr.

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Close the gap early.

Stephen V. Chavez

ECAD TIPS & TRICKS

Resistance adds up quickly.

Brian Gilman

MATERIAL GAINS

AI is raising barriers.

Alun Morgan

BOARD TALK

Availability isn't qualification.

Jeffrey Beauchamp

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Stop drawing conclusions.

Hemant Shah

GETTING LEAN

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Matt Cline and Mike Stanley

SEEING IS BELIEVING

Experience knows when to ask.

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OFF THE SHELF

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THERMAL MANAGEMENT

High-Power Thermal Management: Two-Layer IMS Design Considerations

As power electronics become more compact and power-dense, two-layer IMS PCB designs are helping improve thermal management, reliability and EMI performance in high-power applications.

by CHRIS PARKER

FLEX FINISHING

Based on FPC Board Design for Manufacture Rules Part II

Proper flex PCB outline design, shielding and stiffener placement help improve manufacturability, durability and long-term reliability in demanding applications.

by AKBER ROY

ENERGY MATTERS

Heat Staking vs. Ultrasonic Welding for PCB Assemblies

Both processes form a permanent thermoplastic joint without fasteners or adhesives. For a populated board, the deciding factor is usually not which forms a stronger head – it is where the process energy ends up.

by ALEX SPURGEON

COMPENSATION (COVER STORY)

PCB Designers Earn More, Do More: The 2026

Compensation Picture

The 2026 PCD&F Salary Survey examines compensation, workloads, career satisfaction and the evolving role of PCB designers across the electronics industry.

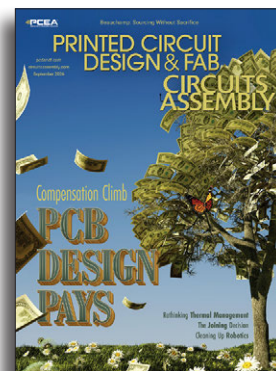
by RYANN HOWARD

PRECISION CLEANING

Contamination Control in Robotic Electronics Manufacturing

As robotic systems become more advanced, effective cleaning and contamination control are increasingly important for ensuring long-term reliability and manufacturing consistency.

by ELIZABETH NORWOOD



ON PCB CHAT (PCBCHAT.COM)



GOOD ADHESIVE, BAD BOND

with DAVID DWORAK

DIELECTRICS AND THERMAL MANAGEMENT

with CHRIS PARKER

M&A TRENDS AND GLOBAL MANUFACTURING

with TOM KASTNER

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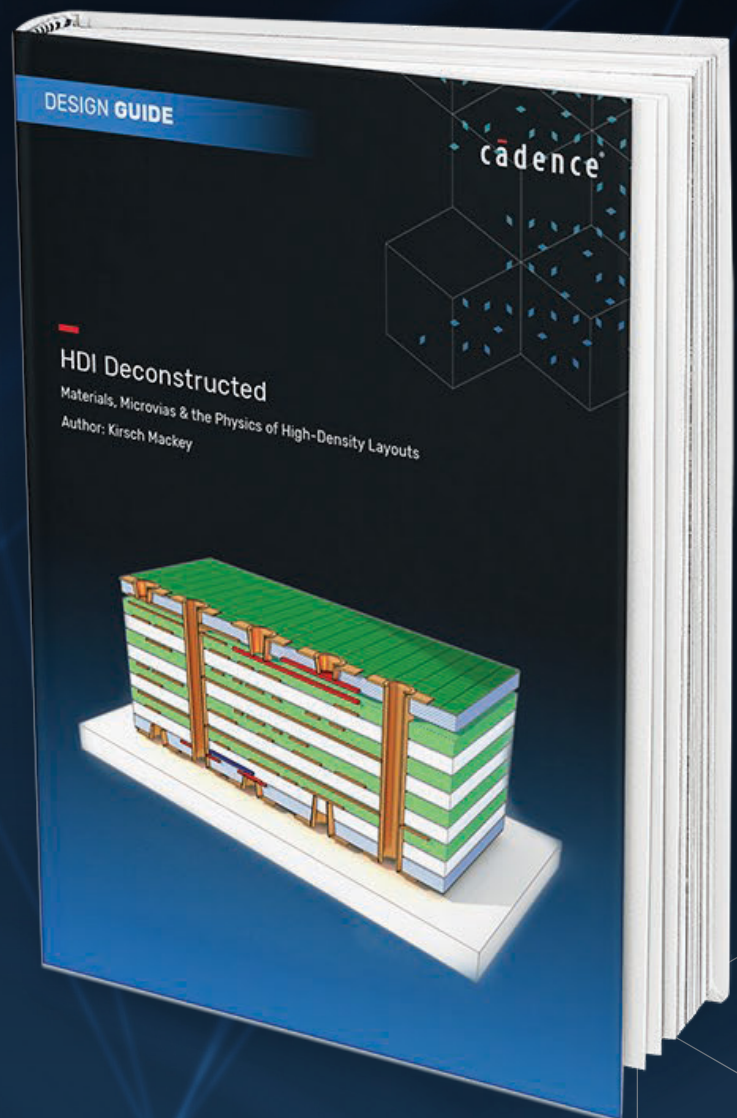
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MANAGEMENT

PRESIDENT

Mike Buetow 617-327-4702 | mike@pcea.net

VICE PRESIDENT, SALES

Brooke Downey 404-316-9018 | brooke@pcea.net

SENIOR DIRECTOR, STRATEGIC ACCOUNTS

Frances Stewart

PCD&F/CIRCUITS ASSEMBLY EDITORIAL

MANAGING EDITOR

Ryann Howard 912-803-9780 | ryann@pcea.net

CONTENT ARCHITECT

Andy Shaughnessy 770-315-9901 | andy@pcea.net

COLUMNISTS AND ADVISORS

Jeffrey Beauchamp, Dan Beaulieu, Peter Bigelow, Robert Boguski, John Burkert, Jr., Stephen V. Chavez, Mark Finstad, Nick Koop, Jake Kulp, Alun Morgan, Susan Mucha, Greg Papandrew, Hemant Shah, Chrys Shea, Jan Vardaman, Gene Weiner

PRODUCTION

ART DIRECTOR & PRODUCTION

blueprint4MARKETING, Inc. | production@pcea.net

Nathan Hoeller | nathan@pcea.net

SALES

VICE PRESIDENT, SALES

Brooke Downey 404-316-9018 | brooke@pcea.net

SENIOR SALES EXECUTIVE

Will Bruwer 404-313-1539 | will@pcea.net

EVENTS/TRADE SHOWS

EXHIBIT SALES

Brooke Downey 404-316-9018 | brooke@pcea.net

TECHNICAL CONFERENCE

Mike Buetow 617-327-4702 | mike@pcea.net

WEBINARS

Andy Shaughnessy 770-315-9901 | andy@pcea.net

EVENTS MANAGEMENT

Leah Spinks 912-239-7730 | leah@pcea.net

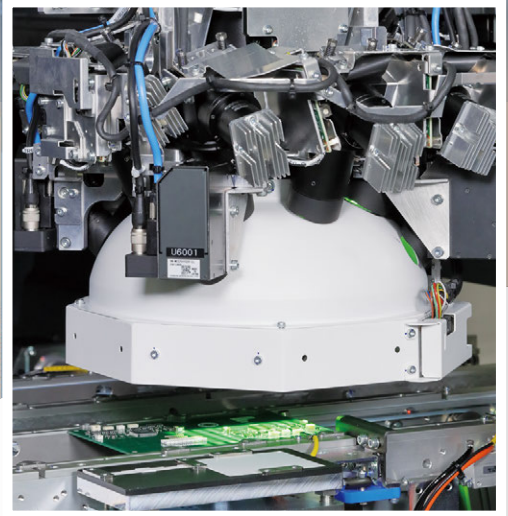
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It's Show Time

A LOT OF us travel for work; it's part of the job. It recently dawned on me that I've spent over a year of my life in California. (I'm surprised I don't have a surfer accent and purple hair by now.) California has its share of issues, natural and manmade, but the Golden State remains the high-tech capital of the US.

That's why we're heading to Silicon Valley for PCB West 2026. The conference kicks off Sept. 29 at the Santa Clara Convention Center, running through Oct. 2, with a trade show on Sept. 30.

I'm slightly biased, but it's no exaggeration to say that the instructors teaching at this year's technical conference are the top experts in PCB design and manufacturing today. Classes will address topics such as controlling noise and EMI, RF and mixed-signal design, signal integrity in UHDI boards, thermal management, stackup design, copper pour, and – of course – AI.

And the show floor continues to expand, with over 100 companies exhibiting this year. An exhibit pass gets you onto the show floor, plus free food and drinks and access to the Free Wednesday classes.

Retire the Respin

This year's keynote speech bears the audacious title "It's Time to Retire the Respin." Keynote speaker AJ Cooper is the CEO of Itera, and he believes his company's liquid metal processes could make respins a thing of the past. Itera's patented process, built on an electrowetting platform, replaces copper traces with reconfigurable liquid metal.

Cooper says this technology can iterate hardware 1,000 times faster than the traditional design process. In his speech, he'll explain how this process works, how it could eliminate the PCB respin cycle, and why he believes hardware updates will eventually be as simple as software updates. This will be an interesting keynote.

Designer Career Day

PCEA is launching a new program at PCB West this year: Designer Career Day. This daylong event takes place on Sept. 30 and is targeted at students, recent grads, and anyone interested in a career in PCB design.

Chaired by Matthew McBride and John Burkert, Jr., the program will feature speakers and a moderated panel. The topics include education, training, technology, job-seeking skills, social media, the realities of being a PCB designer, and more.

Bring some smart, young, tech-minded students to the show so they can get first-hand knowledge about what a career in PCB design is really like. We need to spread the word about PCB design, because most high school and college counselors are still unaware that this career even exists.

The Future of PCB Design

What's next for PCB design? That's what the panel discussion "The Future of PCB Design" will address on Sept. 29. Moderated by Matt Leary of Newgrange Design, the panel will examine the role of AI in PCB design, interposer boards, the latest in high-speed and high-current design, and the integration of optical interconnects. These issues will be affecting mainstream PCB designers sooner rather than later.

The PCB Market Outlook

Dr. Hayao Nakahara will share his thoughts on the past, present and future of the PCB market, the forces driving the industry, and the effects of AI. "Naka" has been compiling his NTI-100 ranking of the top PCB makers since 1999, and his discussions are always informative and entertaining. The class takes place Sept. 30.

The Assembly Track Returns

We also have classes for those on the assembly side. Chaired by consultant Chrys Shea, the assembly track takes place September 29-30, with 11 presentations on circuit assembly processes. Classes run the gamut from fundamentals of assembly to advanced processes, with a half-day workshop on solder paste qualification.

The "Aha" Moment

For design instructors, nothing is more satisfying than an "aha" moment, especially when attendees realize that they've been doing something wrong for decades, and then learn a better, faster way to perform that task.

At PCB West a few years ago, I witnessed an "aha" moment in a roomful of senior designers and design engineers attending a DfM class led by Mike Tucker and Ray Fugitt. (This class is part of Free Wednesday on Sept. 30.) Many of them had no idea what happened to their design package after they hit "send." One designer spoke for the crowd: "I didn't know that's what happened in CAM, and I've been a designer since the 1980s."

If you haven't attended PCB West in the past, what are you waiting for? Visit pcbwest.com and register today. You just might have your own "aha" moment.

See you at the show!



ANDY SHAUGHNESSY is content architect of PCD&F/Circuits Assembly; andy@pcea.net.

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TTM Technologies to Acquire Epiq Solutions for \$1.1B

SANTA ANA, CA – TTM Technologies has entered into a definitive agreement to acquire Epiq Solutions from an affiliate of Veritas Capital for \$1.1 billion. The transaction is expected to close by the end of 2026, subject to regulatory approvals.

Epiq provides software-defined radios, embedded computing and other specialized radio technologies for commercial, government and defense customers. Its technologies serve signal intelligence, electronic warfare, unmanned systems and space applications.

Veritas acquired Epiq in 2022 and subsequently expanded the company through product development and the acquisitions of Xiphos Systems and Cyber Radio Solutions, adding space-based computing and high-performance RF capabilities. 

Victory Giant Plans \$444M PCB Plant for AI Demand

HUIZHOU, CHINA – Victory Giant Technology plans to invest at least \$444 million in a new PCB manufacturing facility in Huizhou as the company expands capacity for AI computing applications.



Victory Giant Technology plans to invest \$444 million in a new PCB manufacturing facility in Huizhou, China, to expand capacity for AI computing applications.

The company acquired a 100,000-square-meter industrial site for the facility, with at least \$296 million of the planned investment expected to go toward fixed assets. Victory Giant has expanded its presence in GPU and AI accelerator supply chains in recent years, including through its HDI business.

The investment comes amid broader PCB capacity growth tied to AI servers and computing infrastructure, with Chinese manufacturers including Shengyi Technology, WUS Printed Circuit and Shennan Circuits also benefiting from increased demand. 

NXP Breaks Ground on Malaysia Assembly and Test Factory

PETALING JAYA, MALAYSIA – NXP Semiconductors has broken ground on a 500,000-sq.-ft. assembly and test factory that will more than double the output of its Malaysian operations once fully operational.



NXP Semiconductors breaks ground on a 500,000-sq.-ft. assembly and test factory in Petaling Jaya, Malaysia.

The facility will increase NXP's existing Petaling Jaya site to approximately 900,000 sq. ft., with production expected to begin ramping in the first quarter of 2028. The additional capacity will provide assembly and testing across NXP's semiconductor portfolio.

NXP plans to operate the facility as a highly automated smart factory incorporating automated material handling systems and advanced quality management technologies. The investment will complement the company's existing assembly and test operations in Greater China and Thailand. 

DRAM Shortage Could Force Nvidia to Rethink Rubin Ultra Memory

TAIPEI – Tight DRAM supplies expected to persist through 2027 could lead Nvidia to reduce the HBM configuration of its next-generation Rubin Ultra AI platform, according to TrendForce.

Nvidia is evaluating 8-Hi and 12-Hi configurations using HBM4 and HBM4e as uncertainty surrounding DRAM wafer capacity and production yields complicates the originally planned 12-Hi HBM4e configuration. Other AI hardware developers are also reconsidering memory configurations as supply constraints persist.

TrendForce forecasts HBM bit shipments will rise 50% to 60% year-over-year in 2027 but remain insufficient to meet demand, maintaining availability and cost pressures for AI chip developers. 

NEOTech Acquires Virtex, Adds Five US Manufacturing Sites

STAMFORD, CT – NEOTech has acquired electronics manufacturing services provider Virtex, expanding its US manufacturing footprint and high-reliability electronics capabilities for defense applications. Financial terms were not disclosed.

Virtex operates five US facilities and provides PCB assembly, engineering and testing, cable and harness assembly, system integration, supply chain management and aftermarket services. The combined organization will operate 11 facilities and employ more than 2,500 people.

The acquisition also expands NEOTech's capacity for complex, low- to medium-volume, high-mix electronics manufacturing and adds to its ITAR-registered domestic manufacturing footprint. 

RRP Electronics Moves to Acquire Vital Electronics

INDIA – RRP Electronics has signed a memorandum of understanding and term sheet to acquire electronics manufacturing services provider Vital Electronics as it looks to expand beyond semiconductor packaging into complete electronic system manufacturing.

RRP plans to acquire 100% of Vital Electronics in four tranches, reaching 50% ownership by March 2027 and completing the transaction by March 2028, subject to milestones and regulatory approvals.

Vital Electronics provides PCB assembly, SMT, electromechanical assembly, engineering, sourcing, testing and box-build services. RRP said combining those capabilities with its semiconductor packaging operations would create an integrated manufacturing chain from semiconductor packaging through PCB assembly and finished systems. 

CACI Opens Defense Electronics Manufacturing Center in New York

PITTSFORD, NY – CACI International has opened a 61,000-sq.-ft. Manufacturing Center of Excellence for Defense Electronics, increasing its manufacturing space by more than 300%.



CACI International's 61,000-sq.-ft. Manufacturing Center of Excellence for Defense Electronics in Pittsford, NY.

The facility will support development, testing, assembly and delivery of electronic warfare technologies for the US military. It will also support CACI's Terrestrial Layer System Brigade Combat Team Manpack program with the US Army, for which the company received a nearly \$400 million contract modification in 2025.

The center is one of CACI's largest manufacturing sites and includes additional space for future expansion. It will also work with more than two dozen small-business suppliers across Upstate New York. 

Velocity Group Triples Capacity with Ohio Manufacturing Plant

CAMBRIDGE, OH – Velocity Group has opened an 80,000-sq.-ft. manufacturing facility in Cambridge, consolidating three previous facilities and tripling its production capacity.

The plant adds more than 25,000 sq. ft. of production space for high-mix, low- to mid-volume manufacturing of electronic and electromechanical products. New capabilities include insert molding, overmolding, large-part injection molding and precision machining.

Velocity Group said the facility will also more than double its subassembly and assembly capacity and includes injection molding capabilities within an FDA Class 7 clean room for medical device manufacturing. 

Norautron Acquires Jaltek to Expand UK Manufacturing

HORTEN, NORWAY – Norautron has acquired UK-based electronics manufacturing services (EMS) provider Jaltek, expanding its manufacturing footprint into the United Kingdom.

Jaltek has more than 35 years of experience in electronics design and manufacturing for aerospace, defense, medical technology and industrial electronics. Its capabilities include new product introduction, PCB assembly layout, manufacturing, testing and final system assembly.

Jaltek will continue operating from its existing facilities under its current management team while gaining access to Norautron's international manufacturing network and technical resources. 

Foxconn Unit Acquires Mexico Land for \$20M

TAIPEI – Foxconn subsidiary FII AMC Mexico has acquired approximately 2.6 million sq. ft. of land in El Salto, Jalisco, Mexico, for approximately \$20 million.

The property, purchased from FARUBA, was appraised at approximately \$20.6 million. Foxconn said its board approved the transaction Aug. 18 for operational needs.

The acquisition adds to Foxconn's existing manufacturing presence in Mexico as the electronics manufacturing services provider maintains significant production operations in the country. 

Dixon Technologies Forms Smartphone Manufacturing Venture

NOIDA, INDIA – Dixon Technologies is establishing a subsidiary to support its electronic device manufacturing business, including smartphones, through a joint venture with Vivo Mobile India.

Dixon will hold a 51% stake in Advistor Electronics India through an initial investment of approximately \$295,000. India's Ministry of Electronics and Information Technology has approved Vivo Mobile India's proposed investment in the venture.

The joint venture will expand Dixon's smartphone manufacturing capacity, with revenue from the business expected to begin contributing during the October-December quarter. 

Quectel Opens Brazil R&D Center for PCB Design, IoT Engineering

MANAUS, BRAZIL – Quectel Solutions has opened its first South American R&D center in Manaus, expanding its engineering presence in Latin America.



Quectel Solutions' first South American R&D center in Manaus, Brazil.

The facility, Quectel's ninth global R&D center, will focus on smart modules, cellular and short-range communication modules, PCB design and ODM customization services. Engineering teams will support industrial IoT, utilities and asset-tracking applications.

Located in one of Brazil's largest electronics manufacturing hubs, the center will provide localized engineering resources while supporting product development for customers throughout Latin America. 

Unichem Moves to Acquire Loomia Technologies

BROOKLYN, NY – Unichem has signed a term sheet to acquire flexible electronics company Loomia Technologies for up to \$6 million, with plans to extend its technology into robotics, automotive, medical and other applications.

Loomia develops an ultra-thin flexible electronic circuit structure that integrates into materials such as leather and textiles to provide heating and pressure and temperature sensing. Unichem plans to combine the technology with its materials manufacturing capabilities to develop large-area electronic skin for humanoid robots.

Potential applications also include medical devices, wearables, automotive interiors and thermal sensing in AI data centers. Unichem plans to retain Loomia founder Madison Maxey and key R&D personnel, with its Brooklyn operation serving as a North American R&D and market development hub. 

GSI Group Acquires Aven Tools

MAHWAH, NJ – GSI Group Holdings has acquired Aven Tools, adding the precision tool and microscopy equipment provider to its portfolio of laboratory and industrial workflow brands.

Aven supplies digital and stereo microscopes, LED illumination systems, cameras, tweezers, magnifiers and other precision tools used in industrial electronics, medical device and research applications.

GSI said the acquisition expands its presence in industrial electronics and medical device workflows while adding Aven's dealer network and customer base of more than 1,000 customers. Aven joins GSI brands Globe Scientific, AmScope, Euromex and GenesisBPS. 

PCD&F

Anthropic is building an in-house chip design team to develop custom AI processors, complementing its use of hardware from **AWS**, **Google**, **Nvidia** and **AMD**.

Eiso Enterprise opened a second-phase expansion at its Guishan plant, doubling PCB capacity for AI and aerospace demand.

Molex invested in **CAEPlus** to advance active liquid-cooling technology for AI data centers.

Syrma SGS and **Kaga Electronics India** formed a joint venture to manufacture bare PCBs in Haryana.

ZenaDrone began flight testing custom-designed printed circuit boards manufactured in-house. 

CA

EMPEL Systems selected **Altus Group** to supply an advanced power electronics manufacturing line.

Keiron raised \$21 million in a Series A round for its digital printed circuit board printing technology.

Komatsu Midori-Kai named **Matric** grand partner.

LG Electronics is expanding its Latin American footprint with a smart-factory production hub in Paraná, Brazil.

Pegatron is expanding operations in Ciudad Juárez, Mexico, with a \$330 million investment.

Sanmina-SCI India was approved to establish a manufacturing unit in Oragadam, Sriperumbudur, expected to generate 1,350 jobs.

StenTech is expanding its North American manufacturing capacity.

Surrey Satellite Technology installed a **Sciencscope** Smart Rack system.

Sypris Electronics won a manufacturing deal to produce complex electronic power assemblies for a new LEO satellite constellation.

Velocity Group opened an electronic and electromechanical products manufacturing plant in Ohio.

Zero Defects International more than doubled its flying-probe ICT testing capacity with new equipment.

Zollner Elektronik is building Phase 2 of its project in Cartago, Costa Rica, including a nearly 10,000-sq.-m. production, office and logistics facility. 

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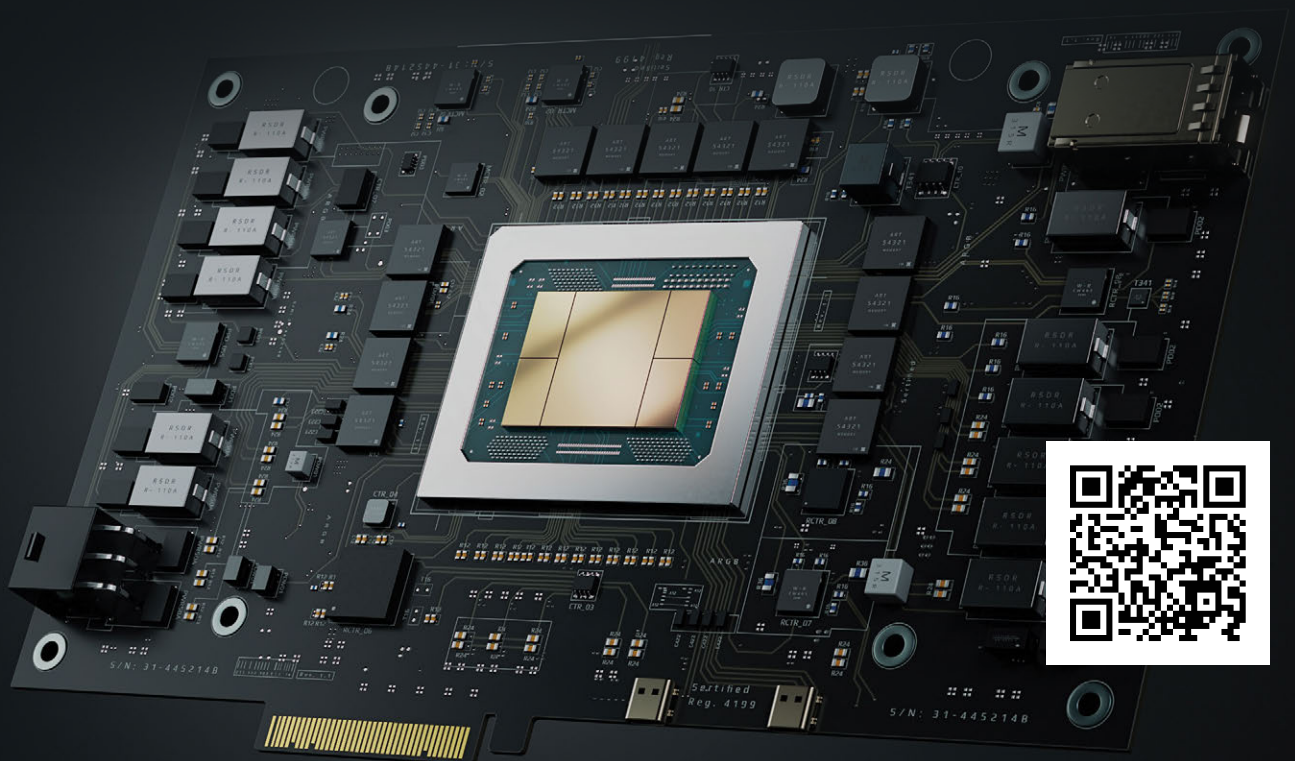
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* Figure P 1, Pedestal Research, Feb 2025

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Guy Schechter



Charles Wert



Mark Duarte



Michael Robbins

Amtech Systems named **Guy Schechter** president and CEO.

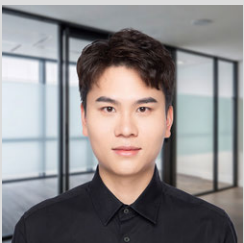
ASC Sunstone Circuits appointed **Charles Wert** president.

Flexible Circuit Technologies named **Mark Duarte** director of global business development.

Michael Robbins was named president and CEO of the Semiconductor Industry Association.

PNE PCB named **Kua Khai Loon** group CEO. 

CA



Bruce Gao



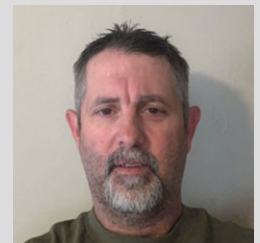
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Bassel Haddad



Jos Timmermans



Jody Saultz



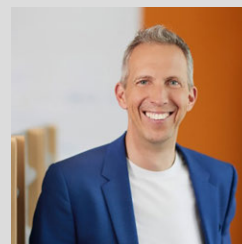
Sean Gallimore



Rob Guthrie



Pascal Delloue



Rainer Brehm



Glenn Farris

AIM Solder appointed **Bruce Gao** sales manager for South China.

AIM Solder appointed **Jake Vlacich** senior product manager.

ASMPT named **Bassel Haddad** group chief executive officer and executive director.

KIC appointed **Jos Timmermans** research and development manager.

Kurtz Ersä named **Jody Saultz** service manager.

MicroCare appointed **Sean Gallimore** chief operating officer.

Neros named **David DiDomenico** vice president of operations.

Parmi appointed **Rob Guthrie** sales manager for the Central Region.

Pica Manufacturing Services named **Pascal Delloue** COO.

Rexel USA named **Mike Hanna** CRO.

Siemens named **Rainer Brehm** to lead its newly restructured automation business.

Teradyne named **Glenn Farris** vice president of sales, product test group. 

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PCB West Announces Free Technical Sessions

PEACHTREE CITY, GA – Registrants for the PCB West exhibition in September will gain access to 11 free technical sessions (plus a keynote presentation) ranging from printed circuit design to fabrication and assembly, [PCEA](#) announced.



The free sessions take place on Sept. 30 at the Santa Clara (CA) Convention Center, and cover topics including AI and PCB design, flex design, simulation, UHDI, and more. “Free Wednesday” kicks off with “Career Day,” an all-day event featuring classes and a moderated panel aimed at students and graduates interested in a career as a PCB designer.

Signal integrity instructor Rick Hartley will discuss the pros and cons of “Copper Pours on PCB Signal Layers.” Next, Ed Dodd, VP of government and defense for Cofactr, will present “The Prototype Trap: Bridging the Sourcing Gap to Volume Production.”

Matt Leary, founder of Newgrange Design, will delve into “Changing PCB Design Software: No Big Deal, Right?” Longtime industry analyst Dr. Hayao Nakahara will share “The PCB Market Outlook,” and AI Block of DirectPCB will present “The Hidden Failure Mode Using Mixed VIPPO in BGA Structures.”

The morning sessions will conclude with Itera CEO AJ Cooper’s keynote presentation “It’s Time to Retire the Respin,” followed by lunch on the exhibit floor, which is free to all show registrants.

Free sessions resume in the afternoon with five sessions:

- The Most Common Issues Seen in Incoming Designs for PCB Fabrication
- Designing High Thermal PCBs with Advanced Dielectrics
- Lessons Learned from Installing AI in an EMS NPI Environment
- The Journey of a Material Disruptor
- Cutting Edge PCB Technologies

Following the free sessions is a reception on the exhibition floor sponsored by Cofactr.

Anyone who registers for the exhibition and free sessions by Sept. 28 will receive free admission. Day of show

registration for the exhibition and free sessions is \$25. 

PCEA Launches Designer Career Day at PCB West

PEACHTREE CITY, GA – PCB West this year will debut Designer Career Day, a free program targeted at students, graduates, and anyone interested in careers in PCB design and design engineering, PCEA announced.

The daylong event will be held on Sept. 30 at the Santa Clara (CA) Convention Center, and is chaired by Matthew McBride and John Burkhardt, Jr. Designer Career Day will feature sessions by industry experts including Stephen V. Chavez, Tomas Chester and Dan Beeker, as well as a panel discussion. Speakers will cover everything from interview skills, networking, and compensation to technology, CAD tools, and the reality of working as a PCB design professional today.



John Burkhardt, Jr.

Attendees will learn about securing industry internships, certifications, fine-tuning a resume and utilizing social media, plus “soft” skills such as communication and problem-solving. Career pathways, education, and training opportunities will also be discussed.

“Designer Career Day could end up being a pivotal moment in a young engineer’s future,” said Burkhardt. “I can still recall the first time I was shown a CAD workstation. From that point onward, I knew what kind of work I wanted to do.”

This year’s show will feature more than 100 exhibitors showcasing the leading companies in the PCB industry, including the top CAD and CAM vendors and top names in printed circuit fabrication and electronics assembly. 

PCEA Announces Fall Webinar Schedule

PEACHTREE CITY, GA – The PCEA fall webinar schedule includes a pair of online sessions aimed squarely at the working printed circuit board designer.

On Oct. 21, veteran PCB designer Judi Emerson will present “How to Be a GREAT Designer,” from 1 to 2:30 p.m. EDT. To register, [click here](#).

Putting down copper traces properly is only part of the job. As Emerson points out, a great PCB designer also has to be an expert on the product, an expert with the ECAD tool, an expert on fabrication and assembly processes, an advocate for the needs of the board, a time bender and, on occasion, a miracle worker. Those demands are sharper still for the solo designer with no team or established process to lean on.

This session covers the “other” work a designer does beyond the board itself, including time management, change control, and building the processes that protect a designer’s schedule and sanity. Where other presentations explain how to do great PCB design, this one explains how to be a great PCB designer.

Emerson has been a PCB designer for 30 years, working primarily for Tier 1 automotive suppliers. She holds a bachelor’s in electrical engineering from Lawrence Technological University and is CID+ certified. Apart from a short stint at Visteon and a brief spell with a PCB supplier during the 2001 electronics downturn, she has been the first or only PCB designer at every job she has held, delivering designs for a range of products while learning on the job how to manage everything that surrounds the design process.

Late in October, Keven Dial of ASC Sunstone will speak on copper coins, including design for manufacturing and RF considerations.

On Nov. 4, senior PCB design engineer and instructor Susy Webb will present “Designing the Signal Routing to Control Energy in Digital PCBs,” a 3.5-hour webinar running from 11 a.m. to 2:30 p.m. EST. To register, [click here](#).



Susy Webb

Great care is often given to the way signals are routed, but the full energy path is frequently not considered or even understood. As signal energy travels around a layer or moves layer to layer through the stackup, a range of complications can lead to poor signal integrity or EMI performance.

The webinar examines what signal energy is and where it is actually located, along with its ability to spread out and the containment measures that may be needed; the physics of rise time, signal flow and impedance control, plus EMI mechanisms and control measures; transmission lines, crosstalk and reference planes; and the way signals fanout, route, return and change layers, with a detailed look at routing order, location and spacing. Webb will also cover stackup design and quality planes, which provide a path for energy to travel from layer to layer while minimizing potential antennas. Attendees will come away understanding why certain routing scenarios are more effective than others.

Webb is a senior PCB design engineer and design instructor with more than 45 years of experience spanning oceanographic exploration and monitoring equipment, point-to-point microwave network systems, and CPCI and ATX computer motherboards. She is CID certified, a regular speaker at PCB West and PCB East, a former columnist for *PCD&F*, a chapter writer for Clyde Coombs’ *Printed Circuits Handbook*, and coauthor of the PCEA CPCD program. She is an active member of the PCEA board and education committees.

For more information on PCEA webinars, visit pcea.net. 

PCB West Panel to Take on What’s Next for PCB Design

PEACHTREE CITY, GA – A panel discussion on the technologies reshaping printed circuit board design over the next two to five years will take place at PCB West this month.

“The Future of PCB Design” (session 10) will be moderated by Matt Leary, founder and president of Newgrange Design. The 90-minute session takes place Sept. 29 from 3:30 to 5 p.m. at the Santa Clara Convention Center in Santa Clara, CA. It is included with conference registration.



Matt Leary

The panel will examine four developments designers are likely to encounter before the end of the decade: the current – and realistic – role of AI in PCB design; interposer boards that sit between the PCB and the semiconductor; advances in high-speed and high-current design; and the integration of optical interconnects. The emphasis is on exposure to what is coming, and on what designers should be doing now to prepare, rather than a deep technical dive into any single topic.

Panelists include Joe Dickson of WUS Printed Circuits, Takuro Sakamoto of Elephantech, Steven Clark, Ph.D., of Stanford University (retired), David Fromm, Ph.D., of Promex, and Mohammad Matin of Celus.

Leary founded Newgrange Design, a Wakefield, MA-based PCB design and engineering services firm, in 1996. The company marks its 30th year in 2026 and today fields a staff of more than 30 designers and engineers working across the major ECAD platforms, along with library development, signal integrity simulation and cable documentation. Leary began his career as a full-time PCB designer and is a frequent speaker at PCEA events.

“These four topics are not academic exercises – they are going to land on designers’ desks, and sooner than most people think,” said Mike Buetow, president, PCEA. “Designers who understand where AI actually helps today, what interposers mean for their stackups, and how optical integration changes the rules will be the ones companies turn to. Matt has built a business by staying in front of exactly these shifts, and he has assembled a panel that spans fabrication, materials, research and design automation. This is the kind of session that pays for itself.” 

Nakahara to Deliver Latest PCB Markets Report at PCB West

PEACHTREE CITY, GA – Dr. Hayao Nakahara, president of N.T. Information Ltd. and author of the annual NTI-100 ranking of the world’s largest printed circuit board manufacturers, will present “The PCB Market Outlook” at PCB West 2026.

His session, “The PCB Market Outlook,” takes place Sept. 30 from 10 to 11 a.m. at the Santa Clara (CA) Convention Center.

Dr. Nakahara will examine the past, present and future of the PCB market, the forces pushing the industry, and the effects of AI – not only on demand, but on the technology changes fabricators and designers will be asked to absorb.

The class is open to all experience levels and is intended for designers, hardware and test engineers, fabrication and assembly personnel, and business leaders.

Dr. Nakahara has compiled the NTI-100, the definitive ranking of printed circuit board manufacturers with annual PCB revenues above \$100 million, every year since 1999.

[The list is published each fall](#) in PCD&F/CIRCUITS ASSEMBLY.



Hayao Nakahara

His most recent ranking found a record 159 fabricators topped the \$100 million mark in 2024, up from 134 the year prior, and put worldwide PCB production at approximately \$96 billion, with China accounting for roughly 59% of global output.

The 2024 data also tracked an accelerating buildout in Southeast Asia, where more than 60 fabricators are constructing plants in Thailand, Malaysia and Vietnam.

Dr. Nakahara founded N.T. Information in 1986 and has toured more than 600 PCB manufacturing plants in 67 countries over a career spanning six decades. He began in the industry at Photocircuits Corp. in 1965 and spent 15 years with the PCK Technology division of Kollmorgen Corp. He holds a master's in electrical engineering from the University of Washington and a doctorate in electrical engineering from Columbia University.

“Dr. Nakahara’s data are the backbone of how this industry understands itself,” said Mike Buetow, president, PCEA. “When an OEM decides where to source, or a fabricator decides where to put its next dollar of capital equipment, the NTI-100 is the reference they reach for. No one else has spent six decades walking the factory floors in 67 countries and then done the arithmetic. For anyone making a sourcing, capacity or investment decision, this hour is the best market intelligence in the industry.” 

A Day of Assembly Classes at PCB West 2026

PEACHTREE CITY, GA – PCB West 2026 offers 11 presentations on circuit assembly processes across two days in September at the Santa Clara (CA) Convention Center.

The two-day event on Sept. 29-30 features a half-day workshop on solder paste qualification, coupled with 10 presentations spanning the spectrum on electronics assembly, from basic fundamentals of circuit assembly processes to more advanced topics.

The program “Introduction to Circuit Assembly Processes” covers the fundamentals: Chrys Shea of Shea Engineering’s class on the SMT printing process, pick-and-place fundamentals with Daniel Stanphill of Aurora Boardworks, the basic components of solder paste with Anna Lifton of MacDermid Alpha, and the basics of cleaning with Doug Pauls of ItDepends.

“Advanced CA Processes” picks up in the afternoon: X-ray imaging resolution misconceptions, Type 5 solder pastes and beyond, stencil design and manufacturing, placement for high-reliability applications, formic acid reflow soldering, and cleanliness measurement with conformal coatings.

Shea will also present “A Data-Driven Solder Paste Qualification Process,” a half-day course on building a qualification protocol that produces defensible data instead of opinions. 



Chrys Shea

PCEA CURRENT EVENTS

ASSOCIATION NEWS

PCB East 2027 booth sales are open. The one-day exhibition will take place Apr. 28, while the four-day technical conference will take place Apr. 27 – 30. All events will be held at the DCU Center in Worcester, MA. Attendance at the PCB East 2026 conference and exhibition rose nearly 48% year-over-year. Contact Brooke Downey at brooke@pcea.net for details or visit pcbeast.com.

New Corporate Members

- Cybord

Recent Discord Chatter

Overheard on the PCEA Discord server:

- Transition via placement
- Applying standards as reference documents
- Pressfit connectors

Want to join? Send a note to membership@pcea.net. 

CHAPTER NEWS

National. Upcoming PCEA Training Certified Professional Circuit Designer (CPCD) training and certification classes will be held:

- Sept. 28 – Oct. 2 (live abridged class, taught in-person in conjunction with PCB West)
- Oct. 16, 23, 30, Nov. 6, 13

Orange County, CA. Our next meeting is Sept. 3. The guest speaker is Justin Fleming, and the topic is implementing accurate and standards-compliant footprints. In modern electronic design, the accuracy and consistency of PCB library components are critical to both product reliability and manufacturing efficiency. By implementing accurate and standards-compliant footprints design teams can ensure consistency, reduce errors and streamline the fabrication process. Fleming is a degreed engineer with over a decade in PCB design with Harley-Davidson/Livewire, Curtiss-Wright and Biamp. He has held positions in circuit design, layout and librarian work, while also having worked in manufacturing of semiconductor tools and functional unit assemblies. 



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Components, Electronics Production Surging in Taiwan

TAIPEI – Taiwan's Ministry of Economic Affairs announced the domestic electronic components production index hit a new high in July, ahead of the coming peak season for consumer electronics.

The electronic components production index was 154, up 23% year-over-year. The IC production index was 175, up 27%, while the computer, electronic products, and optical products production index was 458, up 96%.

The second half is the peak season for consumer electronics production, but July's manufacturing data showed no significant order buying surge yet. AI servers continue to drive manufacturing growth.

Machinery equipment sales grew 19.8% year-over-year in July and basic metals sales rose 13.2%. Chemical materials and automotive and parts segments were hit by weak market demand momentum and inventory reduction, falling 5.9% and 5%, respectively.

The August production index is expected to rise sequentially, and the manufacturing production index is projected to range between 149.5 and 153.5, a year-over-year increase of 26% to 29%. (Source: Central News Agency).

Hot Talk

Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	APR.	MAY ^r	JUN. ^p	YTD
Computers and electronics products	0.6	1.0	2.5	7.5
Computers	-0.3	1.6	-0.1	16.2
Storage devices	1.5	0.2	-1.8	13.9
Other peripheral equipment	9.1	2.0	-10.4	43.3
Nondefense communications equipment	1.1	2.1	2.0	24.4
Defense communications equipment	5.1	4.4	6.4	2.4
A/V equipment	-1.4	0.2	-2.4	-9.9
Components ¹	0.7	2.2	1.7	5.6
Nondefense search and navigation equipment	3.2	-0.5	-0.9	5.5
Defense search and navigation equipment	-0.2	0.1	3.7	13.7
Electromedical, measurement and control	0.6	0.5	5.1	1.3

^rRevised. ^pPreliminary. ¹Includes semiconductors. Seasonally adjusted.

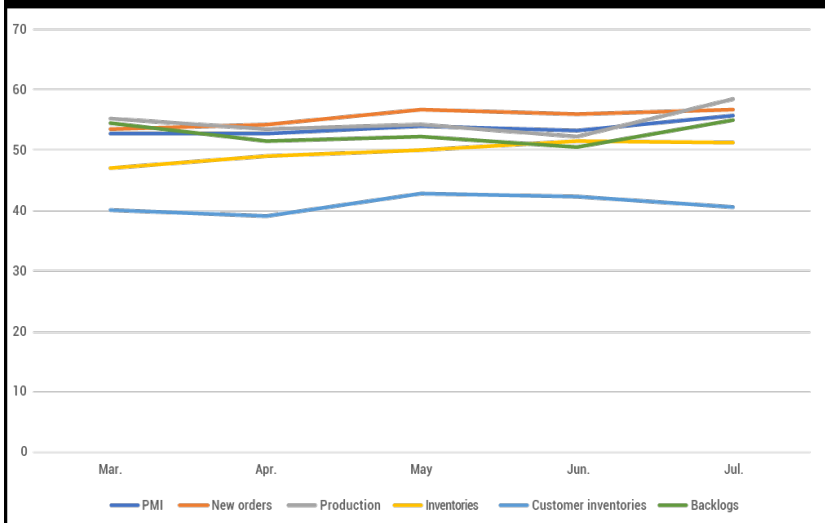
Source: US Department of Commerce Census Bureau, Aug. 4, 2026

Key Components

	MAR.	APR.	MAY	JUN.	JUL.
Semiconductors ^{1,3}	79.2%	93.9%	104.1%	123.6%	TBA
PCBs ^{2,3}	1.08	1.24	1.60	1.49	1.46
EMS ^{2,3}	1.29	1.36	1.36	1.33	1.29
Electronics mfg. orders ²	120.0	118.0	115.0	118.0	119.0
Electronics shipments ²	117.0	115.0	117.0	117.0	119.0
Component sales sentiment ⁴	149.2%	146.6%	146.6%	154.1%	141.6%

Sources: ¹SIA, ²GEA, ³3-month moving average, ⁴ECIA

US Manufacturing Indices



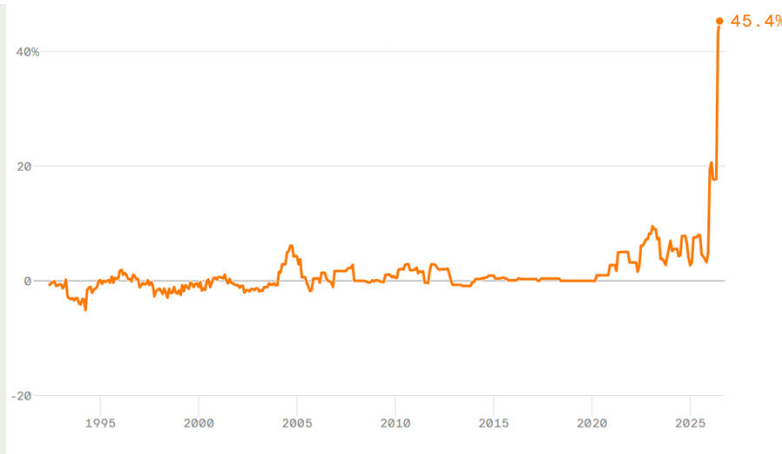
Source: Institute for Supply Management, Aug. 3, 2026

Quick Hits

North American **PCB bookings** jumped 62% year-over-year in July and rose 28% sequentially, bringing year-to-date bookings up 33%. Shipments increased from a year ago and 19.8% sequentially, while year-to-date shipments climbed 13%. (GEA)

India approved 106 new **electronics parts manufacturing projects** under its Electronics Components Manufacturing Scheme (ECMS) program, projected to create 75,000 jobs. (India Union Electronics and Information Technology)

Bare PCB prices are climbing as AI-driven chip demand collides with fallout from the Iran war. (Bureau of Labor Statistics)



Source: Bureau of Labor Statistics, Axios

Major global cloud service providers (CSPs) are accelerating **AI infrastructure investment**, with total CapEx projected to surge 98% year-over-year in 2026 and rise another 50% in 2027. (TrendForce)

North American **electronics manufacturing services** bookings surged 44% year-over-year in July and jumped 76% from June. Year-to-date bookings are up 11%. Shipments declined 0.3% year-over-year and fell 5.8% sequentially. Despite the July decline, year-to-date shipments remained 6.2% above the prior-year period. (GEA)

Global IT spending is forecast to reach \$6.4 trillion this year, a 14 percent increase over 2025. (Gartner)

First half shipments of **flexible OLED panels** for smartphones increased 16% year-over-year to 350 million units, an increase of about 47 million units. (Sigmaintell)

Chinese smartphone vendors reported second quarter shipments fell to 130.5 million units, down 13 percent from the prior quarter and 26 percent from a year earlier. (DigiTimes)

Global authorized distribution grew 12.6% in 2025, with Asia expanding its share 240 basis points to 76%, while Americas companies grew 6% and European companies fell 4.9%. (ECIA)

ECIA released its annual Top 50 Worldwide Authorized Distributors study. (ECIA)

Taiwanese tech suppliers are increasingly targeting satellites, space computing, and optical technologies as potential growth markets. (Nikkei Asia)

PCB prices will rise as much as 50% in Q3. (Board Channels)

The Department of Commerce will provide \$874 million in Chips Act funding to seven US companies developing semiconductor technologies for AI and advanced computing systems. (Department of Commerce) 



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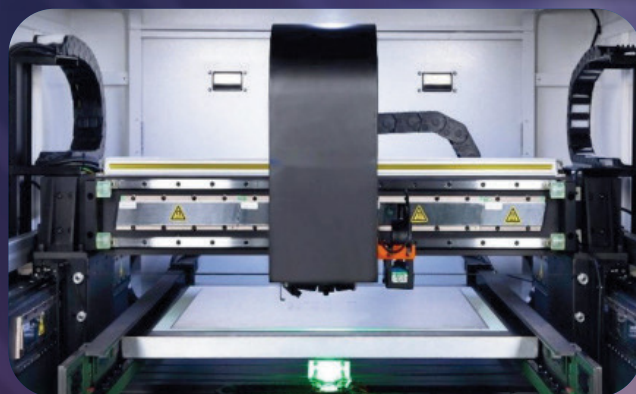
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When the Government Stops Checking

As the US government stresses the importance of quality and cybersecurity, changes to independent certification and auditing requirements raise questions about whether its actions match its warnings.

SOMETIMES I JUST shake my head and say, “Really?” In recent years, I seem to be doing that a lot more often.

Product quality, particularly in high-reliability products, has long ranked among the most important goals for manufacturing companies. W. Edwards Deming helped establish modern thinking about manufacturing quality by emphasizing statistical methods, process improvement and the use of data to improve manufacturing outcomes.

That thinking helped drive the concept of certifying processes, products and quality systems so customers could have confidence that manufacturers had verified and validated the products they delivered.

Today, virtually every industry uses certification programs to verify product quality and demonstrate that products will consistently perform their intended functions. Manufacturing companies encounter many of these programs, including ISO, AS, IATF and Nadcap certifications.

The defense electronics industry has also historically relied on military specifications and qualification programs to demonstrate that products supplied to the US military meet demanding requirements. Standards tailored to specific industries, manufacturing processes and end markets underpin all these programs.

More recently, growing concerns about data security in an increasingly competitive world have driven additional requirements. In the United States, the NIST SP 800 series has played an important role in establishing cybersecurity requirements and guidance. Companies and governments understandably do not want their intellectual property to end up in the hands of competitors, whether those competitors are businesses or foreign governments.

Certification programs certainly create challenges, particularly for smaller companies. Compliance costs money, consumes resources and creates plenty of complaints. But the benefits can justify that effort and expense. Strong certification systems can provide assurance that manufacturers maintain product quality, manage processes properly, improve safety, protect the environment and secure sensitive data.

One of the strongest proponents of quality and security requirements has historically been the US government.

Over decades, the government has established requirements including the FAR, DFARS, military specifications and, more recently, the Cybersecurity Maturity Model Certification (CMMC). These requirements seek to address product

quality, business practices, supply chain integrity and data security.

Some rely on companies to assess and attest to their own compliance. Others require independent audits, which provide a much stronger level of assurance. Historically, government qualification programs have included outside oversight, while CMMC introduced independent assessments for companies handling certain sensitive Department of Defense information.

For the past decade, and particularly during the past several years, the US government has repeatedly emphasized the critical importance of ensuring that military equipment and supplies come from reliable sources and meet demanding standards.

At the same time, federal officials have repeatedly warned businesses about the threat of cyberattacks and stressed the need for stronger cybersecurity and demonstrable compliance with requirements such as NIST SP 800-171.

All of which leads me to another moment when I shake my head and ask, “Really?”

Recent changes to longstanding military qualification programs have reduced some of the government’s direct auditing and qualification activities, shifting more responsibility toward manufacturers. That represents a significant change from a system in which independent oversight provided additional assurance that suppliers met the government’s requirements.

If independent verification mattered enough to require it before, why should self-assessment provide the same confidence now?

That question becomes even more important when we look at cybersecurity.

CMMC has already gone through multiple rounds of revision, review and delayed implementation as the government has tried to balance cybersecurity requirements against the compliance burden placed on the defense industrial base. Each additional review may have legitimate reasons behind it, particularly when smaller manufacturers face significant costs. But every delay also pushes back the day when the government can consistently verify whether contractors have implemented the protections it says are critical.

That creates a contradiction that the government needs to address.

On one hand, federal officials tell the defense industrial base that product quality, supply chain integrity and cybersecurity have never mattered more. On the other, changes that reduce independent verification or delay certification requirements can send the opposite message.

Manufacturers notice that contradiction.

I understand the argument for reducing unnecessary compliance burdens. No company wants to spend money satisfying requirements that add paperwork without improving products or security. Small manufacturers in particular cannot absorb endless compliance costs without consequences.

But if a requirement protects something important enough to mandate in the first place, the government should think carefully before weakening the mechanism that verifies compliance.

Otherwise, I find myself shaking my head again and asking, “Really?”

If government rhetoric continually warns industry about serious quality and cybersecurity threats while government actions appear to reduce the mechanisms intended to address those threats, companies may eventually stop treating the warnings with the urgency they deserve.

That is what worries me most.

We all know the story of the boy who cried wolf. If we hear the warning often enough without seeing actions that match it, eventually people stop responding. And when the wolf finally does show up, we may discover that no one prepared for it. 🗨️



PETER BIGELOW has more than 30 years' experience as a PCB executive, most recently as president of FTG Circuits Haverhill; peterbigelow@msn.com.



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Your PCB Vendor Is Dropping You. What Do You Do Next?

Congratulations. You've been dumped by a supplier.

THE *IT'S NOT YOU*, *It's Us* email may sound polite, but the message is unmistakable: The printed circuit board supplier no longer wants your business.

Maybe the factory is discontinuing a technology, raising its minimum order requirements or exiting the market. Maybe volumes have declined, the product mix has become too complicated or the orders no longer fit the vendor's preferred manufacturing profile. Whatever the reason, active part numbers, customer commitments and production schedules now depend on a supplier that is moving on.

Before searching for a replacement, determine exactly why the supplier made the decision.

Does the decision apply specifically to the company, or is the supplier leaving an entire market or technology segment? Does low volume, excessive quoting, payment history, engineering revisions, quality disputes or an unfavorable product mix drive the decision? Has the factory changed ownership, equipment or strategic direction? Is it eliminating certain materials, surface finishes, layer counts or compliance requirements?

The answer matters because the same problem may follow the business to the next supplier.

If the orders are too small for a high-volume factory, another high-volume factory will probably reach the same conclusion. If frequent revisions and incomplete documentation create excessive engineering work, changing suppliers will not fix the underlying issue. If the board has quietly moved beyond the vendor's comfortable capability range, the company needs a supplier suited to the board as it exists today – not as it appeared when first quoted.

A direct call to the sales representative offers the best way to find out. Skip the email and make the call. Ask what specifically drove the decision. A candid explanation provides useful intelligence, even if it is uncomfortable, and will help determine the criteria for potential suppliers.

Establish how much transition time remains. Request information covering every affected part number, open order, work-in-process lot and forecast requirement.

Then ask the departing supplier about transition options:

- Will it accept a final purchase order or last-time buy?
- Will it complete current work in process?
- Can it accelerate open releases?
- Can it provide the approved production stackup, material list and relevant quality records?
- Can it provide a short extension while the company qualifies a replacement source?

PURCHASE ORDER

PO NUMBER: 4500987
DATE: AUG 12, 2020

VENDOR: PRC DROXX, JNXXXN PRC DROXX, JNXXXN		BUYER: ACME ELECTRONICS INC.	
ITEM LIST	QUANTITY	UNIT PRICE	TOTAL
CUSTOMER MULTI-LAYER PCB REV 3	6,000		38.00
		QUANTITY:	5,000
		UNIT PRICE:	\$4.50
		TOTAL:	\$22,500.00

STANDARD TERMS APPLY TO ALL ORDERS. NO EXCEPTIONS.
PREPARED BY: J. DODANE AND GIPAN FOR REMBYT: ACME ELECTRONICS.
NO IN A HOT PRICE OF HANTHOT DISCOURSE.

126040130, 0020

A supplier exit can expose gaps in sourcing strategy, manufacturing documentation and PCB supply chain resilience.

Do *not* assume that tooling, test fixtures or manufacturing data can simply transfer to another supplier. Establish exactly what is available and what the replacement supplier must recreate.

A last-time buy can provide breathing room. But avoid ordering blindly. Consider product shelf life, forecast reliability, design revisions and the storage requirements of the selected surface finish. Emergency inventory only provides value if it remains usable.

Unfortunately, many companies discover during a supplier transition that they lack a complete, current PCB manufacturing package.

The departing vendor may have built the boards from a collection of Gerber files, email approvals, engineering notes and undocumented exceptions accumulated over several years. The drawing may specify a laminate that the supplier no longer uses. The impedance table may not match the production stackup. An engineer may have approved a material substitution in an email that no one can find.

The outgoing supplier should provide as much detailed information and assistance as possible to facilitate a smooth transition of work to another vendor, especially when the supplier initiated the business change that requires the company to find a new source for its boards.

Ideally, the company already uses more than one supplier. However, resist the temptation to simply move the business to another supplier on the approved vendor list (AVL) and consider the problem solved. As the departing vendor sends the data packages, distribute them for quotes not only to existing vendors but also to other suppliers seeking the business. The company should leverage its vendor base rather than allow vendors to gain disproportionate control.

Quoting only incumbent suppliers gives them greater confidence to raise prices. Every serious PCB buyer needs a robust vendor bench. For example, two qualified production sources could handle 60% of the volume, while two “quote-ready” vendors remain active with the remaining 40% of spend.

Quoting is not betrayal. Quoting is governance. Even when an incumbent supplier steps up after another supplier exits, competing suppliers should remain part of the quoting process. Here’s why:

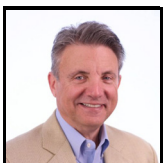
- It validates current market pricing (Governance).
- It keeps the incumbent sharp (Strategy).
- It identifies a better fit in price, lead time or technology without forcing the outcome (Discovery).

Do not use a challenger’s quote simply to drive down an incumbent’s price. That approach creates a “Last Look” culture in which suppliers have little incentive to provide their best price first. If the challenger wins on merit, award the purchase order accordingly. Then explain to the incumbent exactly why it lost the business. Few lessons carry more weight than a missed opportunity. Build a strong PCB supplier bench and use it to its fullest extent.

In today’s volatile market, with continually rising material costs, longer lead times and the real possibility of a supplier ending the relationship, relying on only one or two factories for a PCB portfolio creates unacceptable risk.

A vendor disengagement can serve as the catalyst for building a more innovative and resilient supply chain.

Suppliers do not drop customers out of malice. They do so because commercial considerations drive portfolio decisions, and a company may land in a column labeled “low margin.” Bitterness offers no useful lesson. Supply relationships are commercial arrangements that both parties continually reevaluate. Companies that emerge from a supplier exit intact do not rely on better luck. They already know what comes next. 



GREG PAPANDREW has more than 25 years’ experience selling PCBs directly for various fabricators and as the founder of a leading distributor. He is cofounder of DirectPCB (directpcb.com); greg@directpcb.com.

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EMS Leaders, Please Don't Be This Person

In a 47-year EMS career, the author has encountered leadership styles that can undermine companies, from micromanagement and indecision to poor accountability and siloed thinking.

I'M PRETTY SURE this will stir some emotions in the EMS crowd. Some will think, "I've been through similar circumstances." Others might think, "He can't be talking about me."

Over 47 years in the EMS industry, including the past seven as a consultant, I've worked with many great leaders. I've also encountered my share of poor leadership. Certain behaviors show up again and again, and none of them do a company any favors.

Some leaders operate in silos. Many leaders in our business come from operations or finance backgrounds, and sometimes they concentrate so heavily on those areas that they neglect sales, marketing, HR, IT or other critical functions. A successful business needs attention across what I call the "four-legged stool of success": stakeholders, shareholders, customers and vendors. Ignore one leg long enough and the stool gets pretty unstable.

Then there is the "title bully." I don't need to explain this one because we have all seen leaders use their titles to make up for, or mask, their own self-doubt. I spent much of my career battling these types. Constantly operating at DEFCON 4 makes for a hard path, and I don't recommend following the one I walked. Sometimes the best decision is to leave and find a company that doesn't treat every disagreement like combat.

Narcissistic leaders create a different problem. They believe they sit at the center of the universe, spew hubris at everyone around them and take little direction from people who know more than they do. They often treat everyone below them like menial workers while behaving very differently toward those above them.

Believe it or not, I've also encountered leaders who seem to hate their customers. Yes, they are out there. They forget that EMS is a service business and convince themselves that OEMs must do business with them to survive. They approach every customer as though that customer is trying to "get one over on their business." Eventually, that attitude becomes a self-fulfilling prophecy, and the business disappears.

A lack of accountability can cause just as much damage. Some leaders refuse to recognize their own mistakes, let alone fix them. When they finally acknowledge a problem, they find someone else to blame. We used to call this "walking point," with direct reports taking turns absorbing the blame for the leader's mistakes.

Micromanagers create another kind of dysfunction. Remember a simple thought: "If everything is important, then

nothing is important.” When leaders micromanage every detail, workers feel undervalued and start treating their careers like jobs instead of adventures. Everyone arrives just before 8 a.m. and stands ready to leave by 4:55 p.m., regardless of the critical work still sitting on the table.

Indecisive leaders create the opposite problem. The EMS industry moves at a speed rarely seen on the OEM side of the business. Time kills deals, loses business and costs companies customers. Endless meetings and studying an issue ad nauseam create stagnation. Get the details and make a decision. If you make the wrong call, you’ll learn that faster and can change direction toward the right path.

Some leaders surround themselves with friends instead of people who will make the company better. You have to hire “players” who contribute to the company’s success. You can’t fill the organization with “bootlickers” who spend their days complimenting you instead of proposing solutions or challenging bad decisions. But I bet they have pretty overhead slides.

Dishonest leadership needs little explanation. Leaders who rely on half-truths or believe they can achieve success through lying, cheating and stealing eventually fail.

Low emotional EQ also makes leadership incredibly difficult. Leaders who act on impulse, lack empathy, dismiss others and struggle to think strategically can make an organization miserable. I once worked with an incompetent “owner/president” of a turnaround who thought he could price a complex PCBA by simply looking at it for 15 seconds. He refused to let facts interfere with his flawed judgment. I still wake up remembering dismissive comments like, “Don’t worry about it slick; I got this.”

Then there are leaders who manage from dashboards rather than out in front. These “CRM Masters” let high-level CRM details drive company decisions. They expect everyone else to arrive early and stay late while doing neither themselves. They rarely acknowledge the employees who actually get the work done. Instead of spending time on the manufacturing floor, you find them in spacious offices surrounded by administrative staff who answer only to them. They ask CRM-based questions whose answers generate three more questions, often with zero effect on the business, yet they convince themselves that this activity constitutes hard work.

I’ve also worked under leaders struggling with alcoholism. They weren’t necessarily bad people, but their illness created an environment where we needed to make critical decisions before lunch because afterward they could no longer effectively run the business, much less drive an automobile. We used to try to become the last person to make our case before our director left for lunch. If we secured the last sober agreement from him, our plan won. God help them, please.

I’ve encountered plenty of other characters throughout my career, but these behaviors account for much of the poor leadership I’ve witnessed. One beauty of working as a 1099 consultant is that I no longer have to suffer leaders who consistently demonstrate them.

I should also admit that I have displayed some of these crappy behaviors myself at times. Ignorance played a role, as did receiving more responsibility than I was probably prepared to handle. Experience taught me a lot. I hope those of

you whose careers have crossed mine feel that, over time, I did more good than harm.

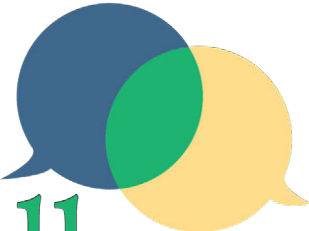
Fortunately, the poor examples don't define my 47 years in EMS. I've also had the privilege of working with many great leaders whom I highly respect – the kind of people I would happily have as my next-door neighbors. 🧑🏻🔧



JAKE KULP is founder of JHK Technical Solutions; jkulp@cox.net. He assists OEMs and EMS companies with optimizing demand creation offerings and deciding when and where to outsource manufacturing. He previously spent nearly 40 years in executive roles in sales and business development at MC Assembly, Suntron, FlexTek, EMS, and AMP Inc.

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PCBAA at Work While Congress is on Vacation

Reviving the domestic electronics manufacturing infrastructure is a round-the-clock job.

WHILE CONGRESS SPENT August in recess, PCBAA executive director David Schild never quite made it to Ocean City. He said that the association's work in Washington never slowed down.

"A lot of people take a vacation in August," Schild laughs. "I'm just not one of them."

PCBAA has been actively engaging federal agencies – including the FCC, Department of Transportation, National Security Council, and Department of Commerce – on issues ranging from tariff impacts to advancing an executive order supporting American-made PCB purchasing.

Schild points to a few results from this lobbying, including the Defense Production Act funding that helped support facility investments at companies like Calumet Electronics (Michigan), GreenSource Fabrication (New Hampshire), and TTM Technologies (Wisconsin). He says bringing lawmakers directly into PCB facilities is a core educational tactic, citing a recent visit with Rep. Joe Courtney to TTM's Stafford Springs facility, tied to Connecticut's submarine supply chain.

On the legislative side, Schild has been busy with the Protecting Circuit Boards and Substrates Act (H.R. 3597 / S. 4569), which requires coordination across multiple committees because the bill includes tax provisions. He notes that PCBAA has bills active in the US House and Senate and is working to build co-sponsor support.

A major near-term focus is Section 851 rulemaking, which would prohibit dual-use and commercial off-the-shelf technologies from containing PCBs from Russia, Iran, North Korea or China in defense supply chains starting January 1, 2027. PCBAA and its member companies have submitted public comments urging the Pentagon to implement the rule on schedule without dilution or delay. The public comment period closed August 31.

Looking ahead, Schild sees the defense budget, the National Defense Authorization Act, and potential future tax legislation (a possible "Reconciliation 3.0") as key items to watch this fall, alongside the November elections and subsequent lame-duck session. He believes that PCBAA's bipartisan support base means the association's priorities will remain stable regardless of which party controls Congress.

He notes growing interest from AI design firms, and draws a comparison to the Chips Act, arguing the PCB industry needs similar critical-technology recognition and federal investment.

“If we didn’t go to Washington and plead our case, we were never going to get what the semiconductor companies got with the Chips Act. Federal policies that level the playing field and make us globally competitive,” says Schild.

He also highlights PCBAA’s membership growth, which has climbed to 92 members from five in the past five years.

“But I’d like to be at 192, or 292,” says Schild.

He explains how PCBAA membership literally puts each company on the map in Washington, DC.

“When you join PCBAA, you’re a dot on the map for one member of the House and two US senators,” Schild says.

“And you now have a communications and advocacy shop in Washington working for you, so you can focus on P&L and production.”

Building that domestic supply chain is at the core of what PCBAA is working toward: growing printed circuit board and PCB assembly capacity in the US, restoring capabilities that have eroded, and reclaiming strategic independence in the electronics hardware space.

PCBAA is driving this forward through policy advocacy, industry engagement, and by backing domestic investment and partnership efforts.

To learn more, visit pcbbaa.org. 



DAN BEAULIEU is a longtime management consultant to the printed circuit industry and a member of the PCBAA; danbbeaulieu@aol.com.



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PCB Design Strategies: Designing for High-Pin Count Devices

Routing and fanout strategies for high-pin-count devices, from managing dense BGA escapes to maximizing available routing layers.

AS DEVICES SHRINK in pitch and increase in pin count, current density becomes a concern. The outer rows of the devices typically have many signal pins, while the pins in the center focus on power and ground. At the edges, the first few layers of the board must be used specifically for fanout.

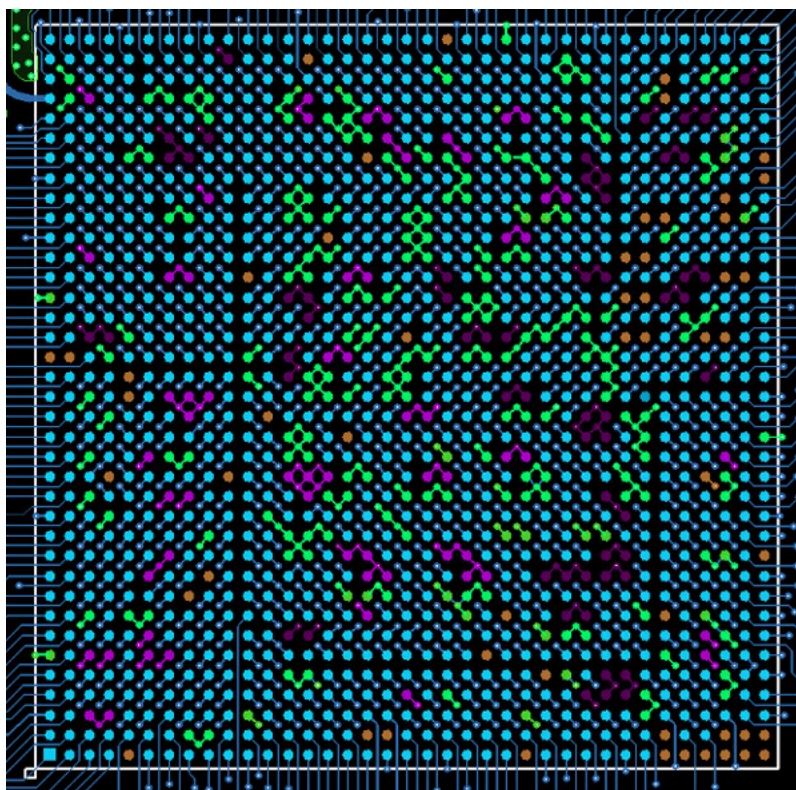


Figure 1. Just an average 1,369-pin FPGA using a 1.27mm (0.05") pitch.

In terms of colors, green is the primary ground domain. Deep purple represents where heavy metal is needed for high current. The lighter magenta is a lower-wattage, more spacey kind of metal, like Pink Floyd, and the orange? Well, orange you glad those are the no-connect pins?

One of the worst approaches when faced with a BGA of 1,000 pins is to drop a via deep into the board for pins on the edge of the device. Every routing channel on the first three layers may be needed, with layer 2 routed in the air gaps of the other two.

The point is to get away from the device until the trace has a chance to join the normal flow of the routing channels. There are two distinct areas. One is the fanout zone, followed by everything else, where up, down, left and right make sense.

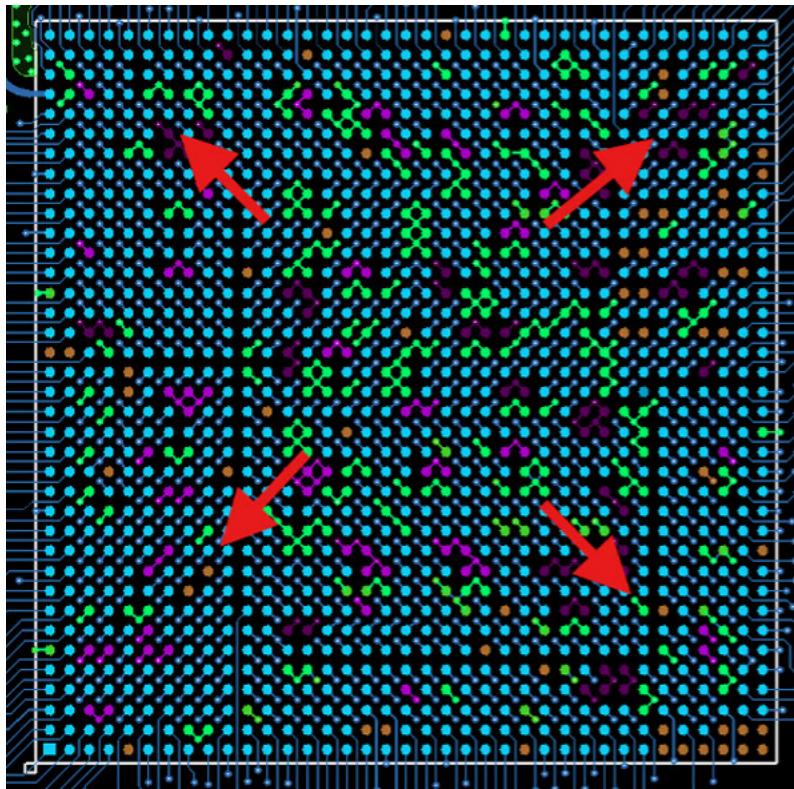


Figure 2. The first step is to address the outer ring(s), using the top layer to escape to a via for an internal routing layer or to a nearby component placed there for that reason. The arrows indicate the fanout flow: always away from the core. For the sake of rework, as well as room for the fanout, a component-free area around the device makes desoldering easier if the device needs to be replaced. Otherwise, the technician has to remove the nearby components first. (Figures 2-7 credit: Author)

Find the beach and drop a via that reaches a level where the current is going the right way. Until the vast majority of the connections are handled in that manner, it makes no sense to route between component clusters. Fanout occurs early in the timeline, and updates to the schematic are probably still on the table. It is much easier to move or edit a group while it remains isolated from the rest of the board.

The outer ring of pins should be routed to “anywhere but here” using the outer layer of the board. If there is room to route between the pins, the second ring of pins should escape on the outer layer as well. If there is no room for that, as with a 0.4mm pitch, the next layer down is best, even if that is the traditional ground layer.

Conventional wisdom calls for routing orthogonal to the traces on adjacent layers. In reality, that is a nonstarter on the edges of a pin field. The routing direction should radiate away from the center of the device far enough to reach a component conveniently placed around the device or a via where the regular routing scheme can begin according to each layer’s purpose.

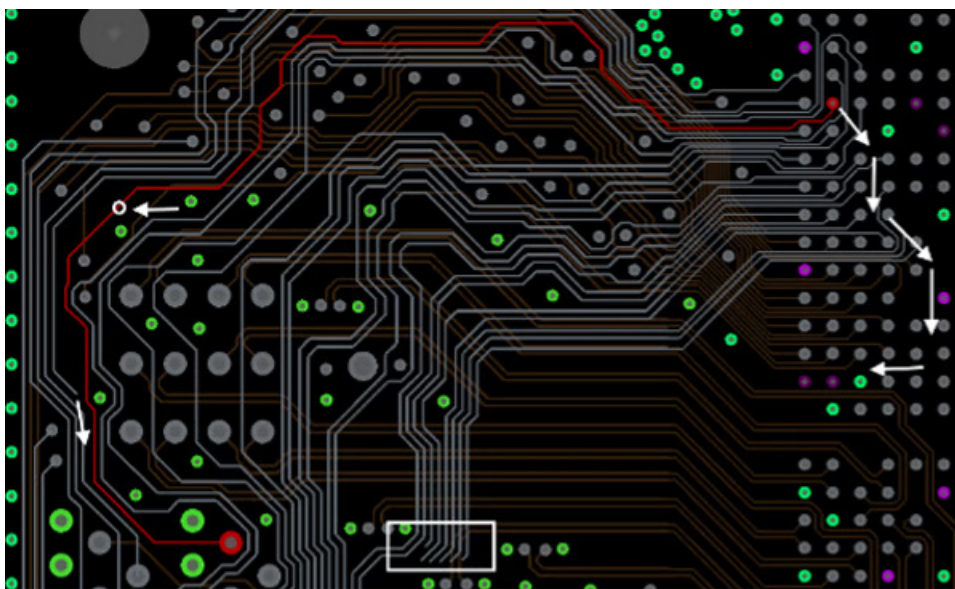


Figure 3. This trace in red is consuming too many vertical routing channels. One option is to drop a via in the upper-left corner and wrap around the differential pairs on the horizontal routing layer. The other option is to use the same brown layer throughout and follow the arrows on the right side, routing under the FPGA to the point where only two traces pass through the fanout vias. From there, the routing goes all the way around the high-speed lanes. The first option seems like less work.

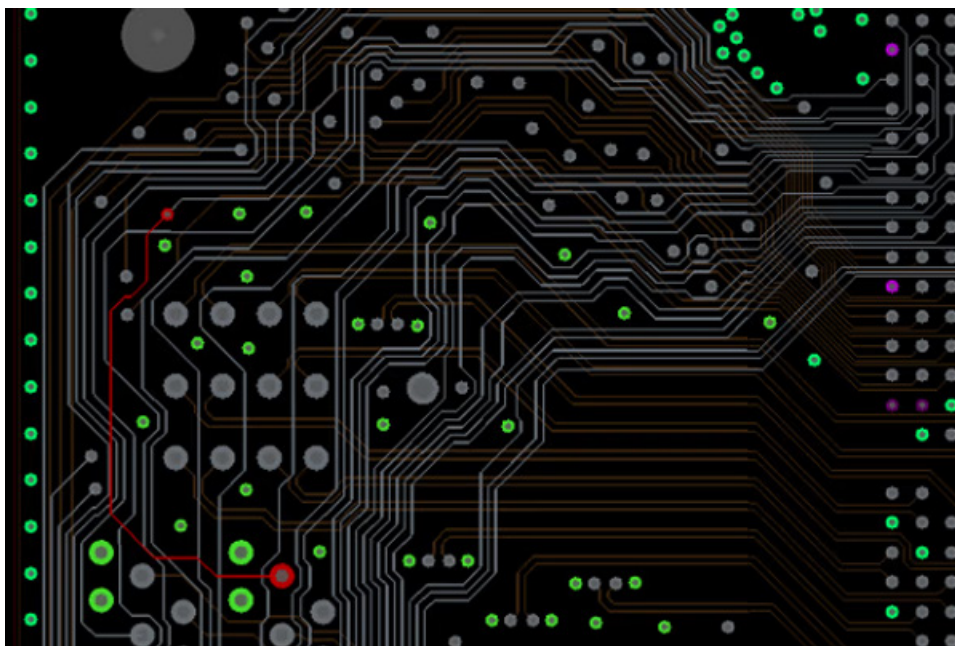


Figure 4. The strategy around horizontal and vertical routing layers involves knowing when to break away from the trend. The little box full of dangling lines has enough lanes to proceed with a minor revision to the trace. Obstacles such as shields, slots and board edges can provide places to route counter to the prevailing directions as a matter of necessity.

If a PMIC device has external oscillator pins, they are likely buried deep inside the BGA pin field rather than out on the perimeter where they would be preferable. There may not be enough headroom for a crystal on the opposite side

of the board, requiring some internal routing to reach the crystal.

If that is the case, a guard band around those traces is appropriate. Like almost every other component, there is a good reason to place the PMIC near the SoC. It is the same reason a single regulator is placed near the pins that use the power it provides to a chip. It is a source of signal degradation that should be minimized. In the case of a PMIC, there are a number of such concerns.

With the power domains and essential routing complete, the schematic can finally be closed and the remaining connections routed using the two inner layers for up/down and side-to-side routing channels. There are no length or width requirements left for the unrouted segments. The average person might assume this is the nature of most, if not all, routing solutions. This has become less common as the percentage of constrained nets has grown over time.

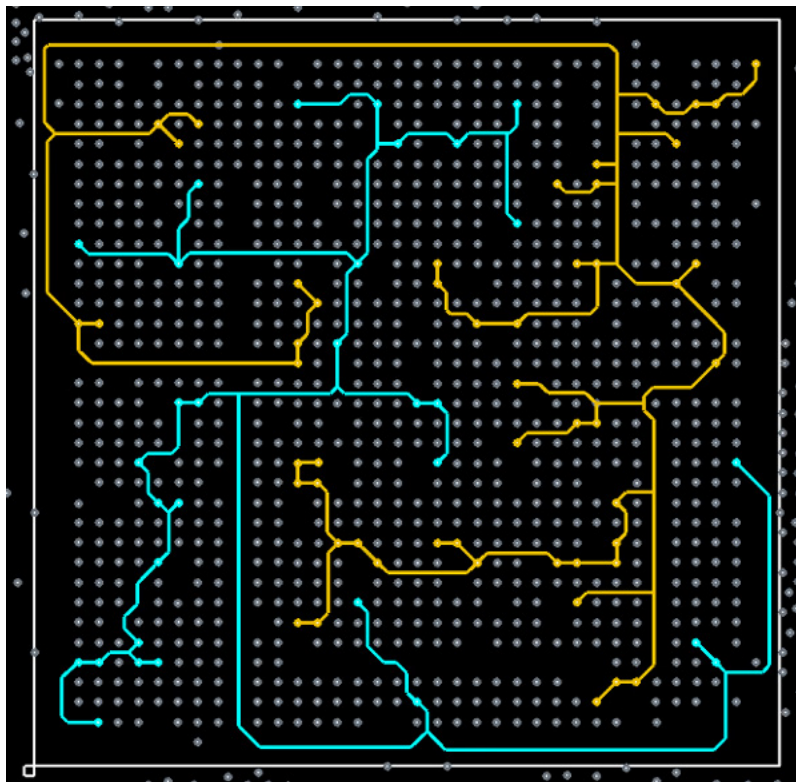


Figure 5. Both power domains can be connected without overlap. If it was not obvious before, it is now clear that the two main power domains can be supplied with shapes on this layer based on the routing study. The shapes will fill in to distribute the voltages with minimal neck-down. (As dynamic copper would most likely be used for the power planes, the traces would remain as a backbone. Though they are not even close to sufficient in terms of width, they will prevent a future trace from splitting the plane entirely in case additional routing ends up on this layer.)

Closing those last traces can be a chore, as all the good routing channels seem to be taken. There are times when the routing goal is “anywhere but here.” Routing can begin at both ends, with a meander extending as far as possible in any direction. Along the way, it may be necessary to be “impolite” with the existing work. If the two ends can cross at some point, the routing solution is only a via away. On a 95% routed board, that still may be a problem. I remember

spending 20 minutes clearing space to add one ground via. Such is life under an NFC chip in a phone.

The fanout provides a chance to make minor adjustments to the placement. This effort continues throughout the fanout and routing steps. There is always some guesswork involved in making design decisions. The decisions are not always right, but adjustments can always be made when new information comes to light.

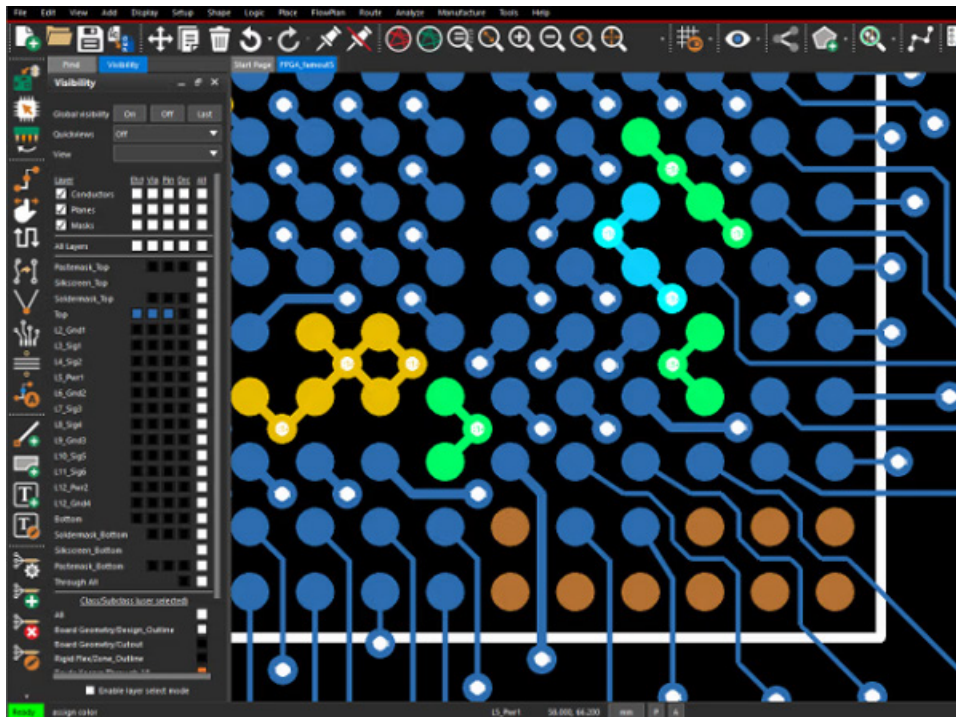


Figure 6. Re-examining this unused MIPI corner gets two more vias out of the grid. If only one trace can be routed between pins/vias, that space should be used. Routing a trace through every gap can depressurize the inner layers in the same way. This applies to pin-grid connectors as well as BGA devices. Maximizing the number of connections on each layer helps reduce the layer count to something more feasible.

Let's Talk About Preliminary Routing

Cross-probing and selectively displaying or colorizing nets provide insight into what is to come. Even after checking off on the placement gate, it is a good idea to maintain elasticity for as long as possible. Modularity is useful when the inevitable update makes it necessary to relocate or rotate a device and its constituent parts.

That said, the various devices have to be connected at some point. The heaviest-hitting device on the board is a good place to start. It could be key because it uses the most power or has the most interconnects. It may also be the main amplifier or whatever motivates the product. Some device lies at the heart of every board, so that is where risk management begins. The process has to start somewhere.

Step one is the highest-priority net on the highest-priority chip. It is all downhill from there, working toward the least significant connections. Operationally, pull-up resistors may not even need to be placed until the pin escape from the device is complete. Once the trace is fanned out and routed to a clear spot for the via, the low-priority part can

land. The same applies to test points. The goal is to get away from the dense area and find a home for the test point.

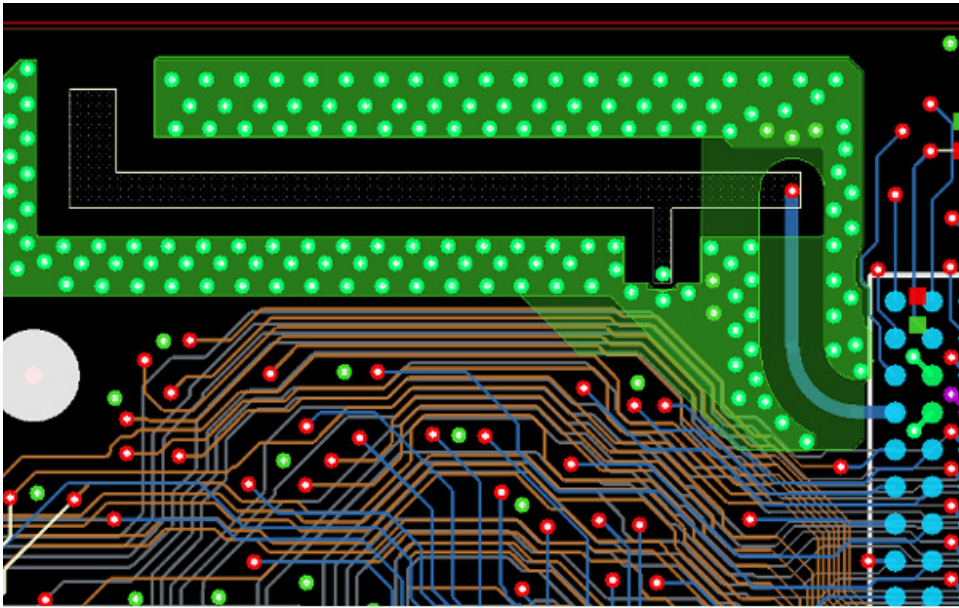


Figure 7. There are times when everything else must step aside and clear all layers for a printed antenna. A net short property can tie the antenna shape and the ground via so the two can coexist at DC and at the antenna's frequency. Like most of these slides, this one is made up entirely from scratch. The takeaway is that ground vias are always in demand around features like this one.

Like going back to the good old days, this process uses the organic, free-range kind of intelligence that comes straight from the brain. Sometimes it helps to flip the bit. Mirror the board's image. Soften the color palette. Make the process easier. Working from home, when possible, can also help.

Either way, via stubs are one consideration during fanout. If the chip is on layer 1, the higher layer numbers are the best choice for differential pairs and similar routing. If the route is on layer 3, there will be a stub from layer 3 to the bottom. Backdrilling should be avoided when possible. Via stubs can become a signal integrity concern as the layer count increases. With that advice, the remaining studies will move on to high density interconnect (HDI) implementation. 



JOHN BURKHART, JR. is a principle PCB designer in retirement. For the past several years, he has been sharing what he has learned for the sake of helping fresh and ambitious PCB designers. The knowledge is passed along through stories and lessons learned from three decades of design, including the most basic one-layer board up to the high-reliability rigid-flex HDI designs for aerospace and military applications. John's well-earned free time is spent on a bike, or with a mic doing a karaoke jam.

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pays the best interest.”*

-Benjamin Franklin

*noted entrepreneur,
yep, rich too...*

hippie hair. hmm--

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Why PCB Manufacturing Still Feels Disconnected from PCB Design, and How Leading Teams Are Closing the Gap

Bringing manufacturing intelligence upstream can reduce costly iterations and create a more continuous path from PCB design through production.

FOR ALL THE advances in PCB design technology, one part of the development process still feels surprisingly disconnected: the transition from design to manufacturing. PCB designers have always worked with fabricators and assemblers to resolve questions and address issues as a design moves toward production. What has changed is the complexity of today's products, the speed at which organizations must deliver them, and the number of people involved. In many companies, manufacturing knowledge still enters the process primarily through a handoff. The PCB designer completes, verifies, documents and releases the design. Manufacturing engineering then determines whether the organization can build it efficiently, reliably, and at an acceptable cost.

That process appears logical, but it often creates unnecessary friction. A fabricator questions a via structure or tolerance, a stackup requires reconsideration, or a feature that meets design requirements introduces unnecessary manufacturing complexity or cost. These issues do not necessarily indicate a mistake. More often, they expose a gap between the information available during design and the knowledge required for successful fabrication and assembly.

The handoff model is reaching its limits. For years, PCB development followed a straightforward sequence: engineering defined the requirements, the PCB designer completed and verified the design, and the team generated manufacturing data. The release package represented a clear boundary between design and manufacturing. That approach made sense when boards had lower densities and technologies followed more standardized processes.

Today's products are different. HDI and UHDI structures, rigid-flex designs, complex stackups, high-speed and high-frequency interfaces, advanced component packages, and tighter geometries have increased the interaction between design decisions and manufacturing capabilities.

A decision involving a via structure, material, stackup, conductor geometry or tolerance can affect far more than fabrication feasibility. It can influence yield, reliability, cost and schedule. Yet designers do not always have manufacturing knowledge available when making those decisions.

A PCB designer may select materials, stackups or fabrication technologies that provide the desired electrical performance without complete visibility into the cost implications. The resulting board may meet every performance objective but cost more than necessary to manufacture. Conversely, a fabricator may identify a manufacturing concern

and modify the data to address it. If engineering does not understand the implications of that change, a modification intended to improve manufacturability could introduce an electrical or performance issue outside the original design intent.

The data used to communicate the design can create another layer of disconnect. Intelligent manufacturing data formats such as ODB++ and IPC-2581 can preserve considerably more design information and context than traditional Gerber-based deliverables. When manufacturing receives only Gerber data, the fabricator may need to reconstruct or reengineer portions of the design before manufacturing preparation can begin. That additional interpretation takes time and creates more opportunities for assumptions or errors to enter the process.

A PCB designer may understand the product requirements but have limited visibility into a fabricator's capabilities or preferred processes. At the same time, the fabricator may understand how to build the board efficiently without knowing which requirements are critical to system performance and which allow flexibility.

When those perspectives and the underlying design intent do not come together until after release, manufacturing teams must reconstruct the reasoning behind decisions made weeks or months earlier. The resulting questions, iterations, engineering changes, and delays may seem normal, but they also indicate that important knowledge entered the process too late. More importantly, they can introduce unnecessary cost or, in the worst case, changes that compromise the intended performance.

The real issue is fragmented knowledge. It is easy to describe this as a communication problem, but the deeper issue is fragmented knowledge. Some information exists in the PCB design database; other requirements reside in drawings, specifications, PLM systems, supplier documentation or email exchanges. Still more may exist only in individual experience.

This fragmentation becomes particularly significant in larger organizations, where multiple design teams may work with different manufacturing partners and processes. Without an effective method for capturing and sharing existing knowledge, teams can repeat conversations and solve the same problems project after project.

Late manufacturing questions can disrupt prototype schedules, redirect engineering resources, delay suppliers and consume time across the organization. As development cycles compress, organizations have less opportunity to absorb that disruption. Reducing the process's dependence on the handoff itself creates an opportunity for improvement.

Moving beyond DfM as a final check. Design for manufacturability remains an essential part of PCB development, but the way organizations apply it can make a significant difference. In many organizations, the first meaningful manufacturing review occurs after engineering releases the design. At that point, issues that the fabricator or assembly provider identifies often trigger another cycle of questions, changes, and revised data.

A practical first step involves incorporating formal DfM sign-off into the engineering release process. Before releasing the design to manufacturing, the design team can perform a final manufacturability review and resolve issues while retaining control of the design. This approach does not eliminate the need for manufacturing involvement, but it can prevent many problems from becoming downstream iterations that consume additional time

and introduce unnecessary schedule risk.

The effectiveness of that review, however, depends on the information behind it. A generic DfM rule deck can identify common manufacturing concerns and provide a valuable baseline, but generic rules cannot account for the specific capabilities, processes, and limitations of every fabricator. A design that passes a general set of DfM checks may still present challenges for the selected manufacturer.

Manufacturer-specific DfM provides greater value in these cases. When teams tune design rules and manufacturing checks to the capabilities of the intended fabricator, engineers can evaluate decisions against the actual processes that the fabricator will use to build the product. A complex via structure, material selection, conductor geometry or spacing requirement may satisfy a generic rule set while still creating unnecessary cost, yield concerns or manufacturing risk for a particular supplier.

A DfM sign-off review based on manufacturer-specific knowledge represents an important improvement over discovering issues only after release. Moving that same intelligence further upstream creates an even greater opportunity, however. Catching a problem before release is better than discovering it during manufacturing preparation, but avoiding the problem while the design is still taking shape gives engineering more flexibility and reduces the cost of change.

The more effective approach, therefore, does not simply add another checkpoint at the end of the process. Instead, organizations can progressively bring manufacturing knowledge into the design environment, beginning with DfM sign-off and manufacturer-specific rules and making that information available earlier as their processes and digital capabilities mature.

This approach does not require every PCB designer to become a fabrication expert, nor does it require manufacturing engineers to participate in every design decision. The objective is to provide relevant manufacturing intelligence while it can still influence the outcome. Most engineers do not need more data. They need useful context that clarifies the consequences of a design decision before changing that decision becomes difficult, expensive, or disruptive.

Technology can enable this shift, but technology alone will not eliminate the disconnect. Organizations also need to reconsider how they define the relationship between design and manufacturing. In a traditional workflow, collaboration often intensifies when the design reaches a release milestone or when someone discovers a problem. A more connected process introduces manufacturing perspectives earlier and maintains that connection as the design evolves. This matters as PCB development becomes more distributed across design teams, fabricators, assembly providers, component engineers, and supply chain organizations.

Organizations need better methods for capturing useful knowledge, making it accessible, and connecting it to the engineering workflow. Manufacturing partners play an important role in that equation. Fabricators and assembly providers possess practical knowledge that can influence design decisions long before engineering releases a manufacturing package. Moving that expertise upstream and capturing it for reuse can turn individual experience into shared engineering intelligence.

Connecting design intent with manufacturing reality. A manufacturing package can communicate what the

manufacturer needs to build, but released files do not always preserve the context surrounding the design. That context explains why engineering selected a particular requirement, which constraints are critical, where flexibility exists and what changed during development.

When product data lacks that context, downstream teams must recreate it through documents, meetings, and questions. That approach depends heavily on individual experience and does not scale well as organizations and supply chains become more complex. A more connected digital environment can maintain relationships among design data, engineering intent, manufacturing requirements, component information, and change history. The PCB then becomes part of a broader information flow that supports decisions throughout development.

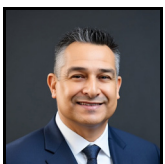
The value extends beyond design efficiency. Reducing iterations can improve schedule predictability and reduce engineering costs. Capturing manufacturing knowledge makes experience available across teams, while connecting changes to design intent can identify consequences before a small decision becomes a larger production problem.

From handoff to continuity. Perhaps the most important shift involves reconsidering where PCB design ends and manufacturing begins. Traditionally, engineering considers design complete when it releases the manufacturing package. In reality, the product is not ready until the organization responsible for building it understands the requirements, prepares the process, and executes manufacturing with confidence.

That perspective expands the definition of successful design. A PCB must not only meet electrical requirements and pass design-rule checks; it must also move through fabrication and assembly without unnecessary questions, rework, cost, or schedule disruptions. For leadership, this means viewing development as a connected system rather than a series of departmental milestones. Organizations should measure the process by how predictably the design moves into production and how much unnecessary iteration occurs along the way.

PCB manufacturing feels disconnected from PCB design because the industry has historically organized the process around data transfer rather than continuity of knowledge. As products become more complex, the cost of discovering manufacturing knowledge late continues to grow. Teams making progress bring manufacturing intelligence into the design process earlier, collaborate continuously with fabrication and assembly partners, and capture knowledge for reuse across projects.

Ultimately, the opportunity is to move beyond the manufacturing handoff altogether. Manufacturing cannot remain an activity that begins after design is complete. It needs to become an integral part of the engineering process itself. Organizations that make that shift will be better positioned to reduce unnecessary iterations, improve development predictability, and create a more resilient path from design intent to manufactured product. 



STEPHEN V. CHAVEZ is a senior printed circuit engineer with three decades' experience. In his current role as a senior product marketing manager with Siemens EDA, his focus is on developing methodologies that assist customers in adopting a strategy for resilience. He is an IPC Certified Master Instructor Trainer (MIT) for PCB design, IPC CID+, and a Certified Printed Circuit Designer (CPCD). He is chairman of the Printed Circuit Engineering Association (PCEA); stephen.chavez@siemens.com.

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Check PCB Trace Resistance with Ohmic Distance in CR-8000

Running trace resistance checks early in the design cycle can help ensure design intent.

PCB TRACES ARE not perfect conductors. As current moves through a routed copper path, PCB trace resistance is affected by the trace's length, copper thickness and temperature. In critical circuits, excessive resistance harms performance through voltage drops, signal integrity issues and measurement errors.

CR-8000 Design Force helps PCB designers evaluate these risks with the Ohmic Distance tool. Designers can measure resistance directly on the PCB layout or define resistance limits for multiple pin pairs to check critical connections during design updates.

PCB design is not complete when every component is connected. The physical layout of each route can influence how the circuit behaves in the real world. For critical connections, designers need to confirm that the routed path supports the design's electrical intent.

Why PCB Trace Resistance Matters

Trace resistance is the electrical resistance along a copper path on a PCB. Every trace has some resistance, although the value is often small. For critical circuits, too much resistance can affect voltage delivery, heat generation, signal quality, and measurement accuracy.

The trace resistance equation is as follows:

$$R = \rho \times \frac{L}{H \times W} \times [1 + \alpha \times (T_{amb} - 25)]$$

Variables

L = trace length

H = trace height

W = trace width

T_{amb} = ambient temperature

Constants (copper)

ρ = 1.7 x 10⁻⁶ Ω-cm

α = 3.9 x 10⁻³ Ω/Ω/C

Eq 1: This trace resistance equation reveals how geometry and temperature impact performance.

In simple terms, resistance increases when the trace gets longer, narrower, thinner or hotter. If trace resistance is too high, it can create several power distribution issues:

Voltage drop. Small resistance values can cause meaningful voltage loss when the current is high. For example, a 10mΩ trace carrying 5A creates a 50mV drop, which can be significant for low-voltage rails with limited operating margin.

Power delivery instability. Devices with tight supply requirements need voltage to stay within a narrow range. Excess trace resistance can reduce the voltage delivered to the load and make the circuit more sensitive to current changes.

Thermal stress. Power dissipation is calculated as P = I²R. High current through excessive trace resistance can generate localized heat, contributing to copper degradation, solder joint stress and long-term reliability risks.

Excess trace resistance can also lead to signal integrity issues, including:

- **Signal loss.** Excess trace resistance can attenuate signals as they travel across the board. Signal loss is especially important for high-speed digital buses, RF paths, and other circuits where signal strength affects reliable operation.
- **Controlled impedance.** Some high-frequency PCB signals require the trace to maintain a consistent controlled impedance. Excess trace resistance can change the impedance characteristics of the transmission line, causing reflections that superimpose on the primary signal and create distortion.
- **Measurement and control errors.** In sense lines or feedback loops, trace resistance can add unintended series resistance. This additional resistance can affect measured values and contribute to regulation drift.

Calculating Trace Resistance with the Ohmic Distance Tool

CR-8000 Design Force contains the layout data needed to evaluate PCB trace resistance, including the routed path, cross-sectional area and copper properties. The Ohmic Distance tool uses this data to calculate resistance directly

between two selected points on the canvas.

Designers can also select the trace temperature before running the calculation. Selecting the trace temperature matters because copper resistance increases as temperature rises. Temperature-aware analysis helps the result better reflect real operating conditions. Instead of estimating resistance outside the PCB design environment, designers can utilize CR-8000 to calculate resistance from the actual routed copper path.

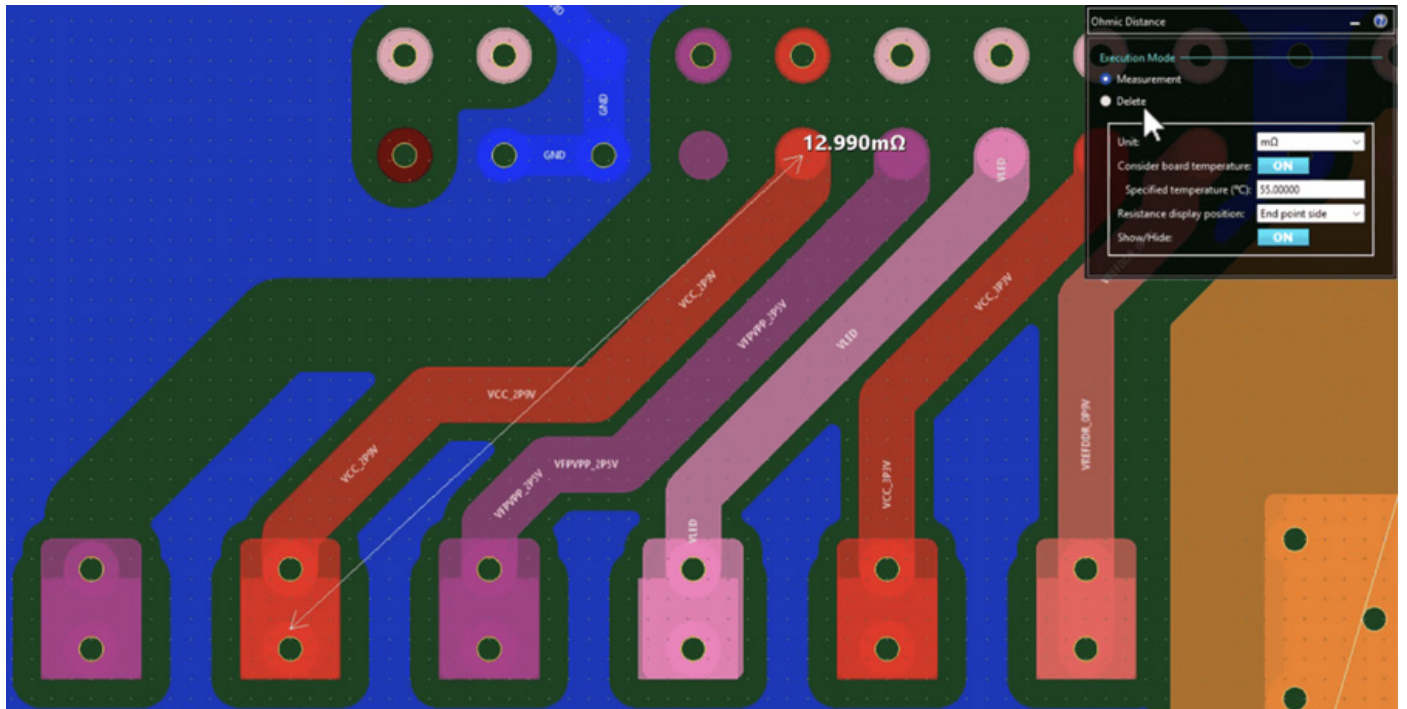


Figure 1: Calculate trace resistance between endpoints directly on routed PCB paths.

Checking Multiple Trace Resistance Limits at Once

Ohmic Distance can also be used through the Constraint Browser for a more systematic design check. Designers define pin pairs for critical connections and the minimum and maximum trace resistance allowed for each pair. The table automatically evaluates compliance during design updates.

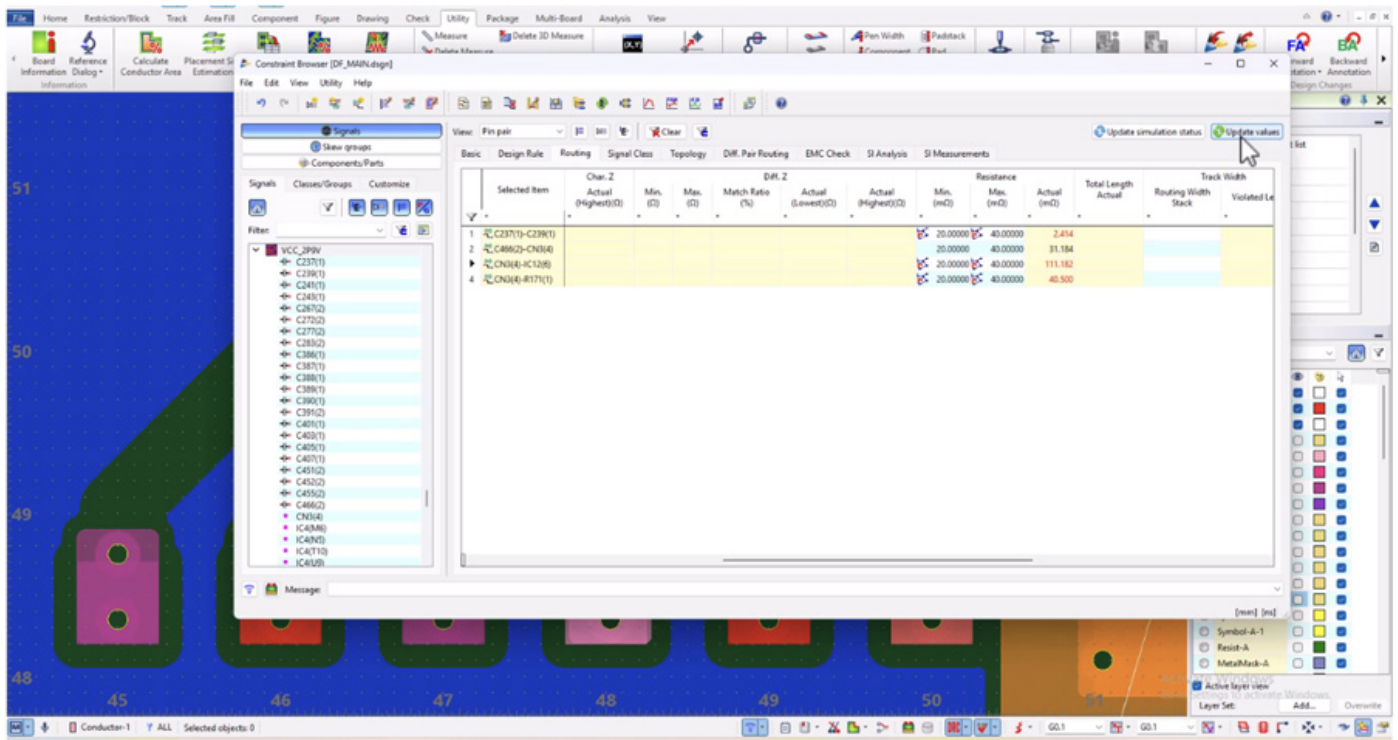


Figure 2: Red markings in the Constraint Browser clearly identify resistance violations in critical connections.

Teams can move from one-by-one manual checks to constraint-driven validation. Resistance violations are clearly flagged (e.g., highlighted in red) in the constraint system. Clear violation markers enable rapid identification and correction of power delivery weaknesses and signal integrity risks.

By integrating Ohmic Distance analysis and resistance constraints into the design workflow, CR-8000 Design Force enables:

- Proactive issue prevention instead of reactive debugging
- Faster design iterations with built-in validation
- Improved product reliability and performance
- Reduced risk of costly redesigns or field failures

Resistance targets are enforced systematically, not dependent on manual checks.

PCB layout designers can use Ohmic Distance to measure trace resistance directly on the board layout. Direct measurement helps them adjust trace width, routing length, copper usage or layer choices before the design moves further downstream.

Electrical engineers use Ohmic Distance to confirm that critical circuits meet performance expectations. Ohmic Distance is especially useful for power rails, high-current connections, precision measurement circuits, and other nets where resistance can affect circuit behavior.

Design review teams use resistance constraints to verify that important pin pairs meet defined limits. Constraint-

based verification creates a more consistent approval process and helps teams identify potential issues before fabrication.

Summary

PCB trace resistance is easy to overlook, but it can affect voltage drop, heat, signal quality, measurement accuracy, and long-term reliability. CR-8000 Design Force helps designers check resistance directly from the PCB layout and apply resistance limits to critical pin pairs through the Constraint Browser.

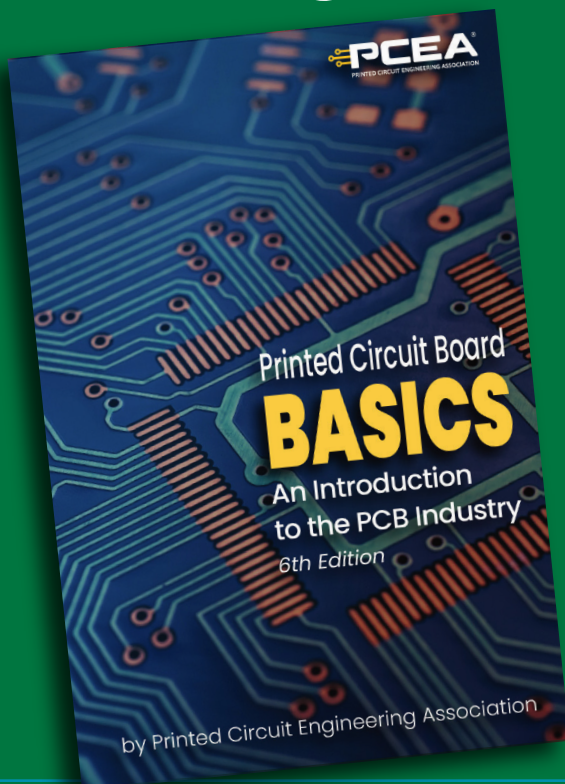
By adding trace resistance checks to the design workflow, teams can find issues earlier and improve confidence before board approval. 



BRIAN GILMAN is an applications engineer with Zuken, supporting customers with CR-8000/CR-5000 training and consulting.

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This Time It Is Different

The future depends on data-center computers that we cannot build today. We are all under pressure to find a way.

INVESTMENT EXPERTS CITE the “This time it’s different” fallacy as a warning against ignoring historical patterns and the power of human psychology when analyzing market behavior. We might have reached a technological “This time it’s different” moment as we consider the next steps in AI computing.

Nvidia is shipping its latest-generation Rubin multi-chip GPUs for cutting-edge AI compute performance and efficiency, and the company has already published its roadmap to subsequent Rubin Ultra and 3D-stacking Feynman devices. What we don’t know is how to handle the thermal issues and data throughput challenges at the packaging and interconnect levels to access the silicon’s performance in the real world.

Historically, engineers treated interconnect design as secondary to the challenges presented by chip lithography. Creating the processor presented the hurdle; connecting it came relatively easily. But this time it’s different.

The Rubin GPU, which contains 336 billion transistors, already stretches the limits of today’s connectivity technologies. Its multi-chip module (MCM) comprises two compute dies and two I/O dies. Nvidia refers to the PCB laminate specification “M9” as an internal performance standard for high-bandwidth AI interconnects that moves beyond the maximum performance of most manufacturers’ standard product ranges. M9 specifies Df in the order of 0.0007 at 10GHz to ensure suitable signal integrity and minimize thermal problems. It dictates specific combinations of resin, copper and glass fiber that only a very small number of materials suppliers can fulfill.

Rubin Ultra servers will demand PCBs with Df in the 0.00035 range, calling for another upgrade in substrate materials performance. As the industry works out how to respond, higher-grade Q-glass can deliver low Df and Dk at high frequency, but its rigidity creates manufacturability challenges. New hyper very-low-profile (HVLP) copper foils also promise performance beyond today’s typical maximum limits.

PTFE could offer another way forward, but engineers must contend with processing difficulties, CTE mismatch and pending legislation restricting the use of PFAS chemicals. Current resin systems will likely adopt evolved blends that meet Rubin Ultra requirements, but this technology is approaching its performance limits.

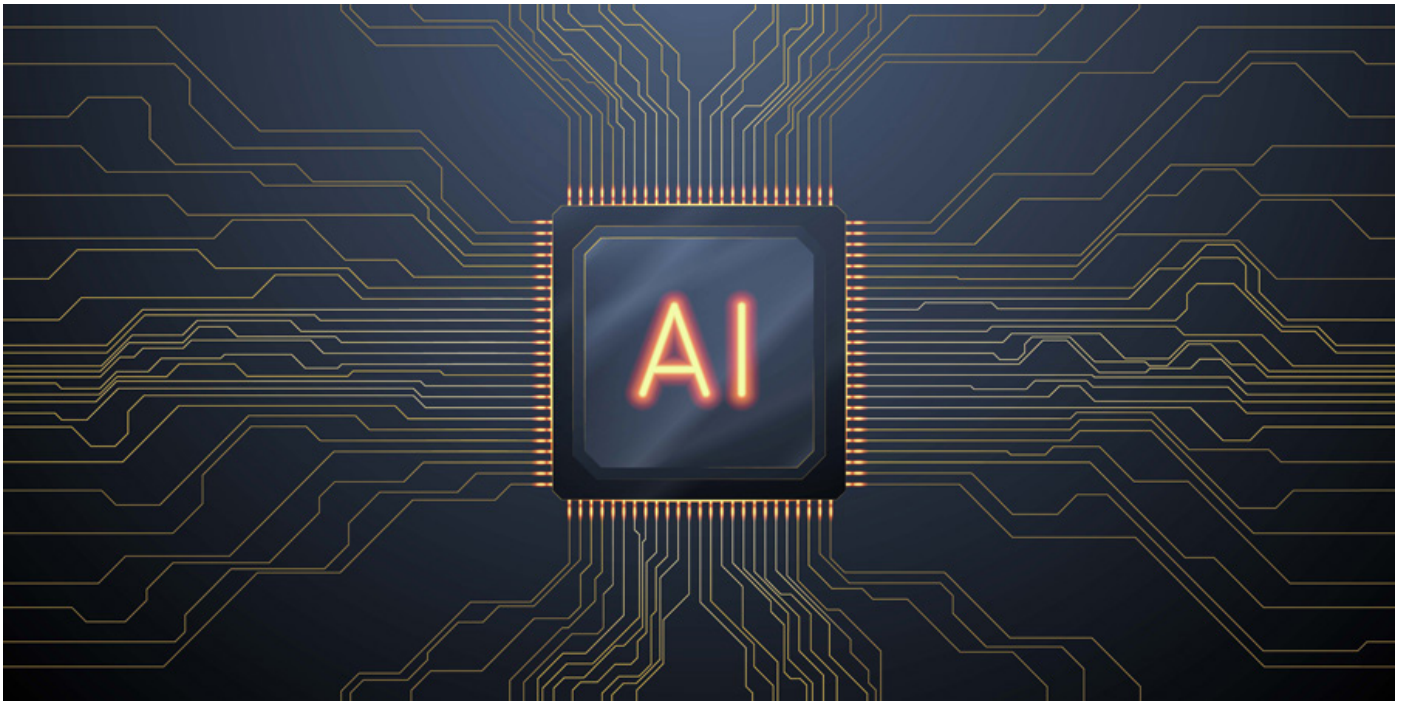


Figure 1. As AI processors push computing performance higher, PCB materials and interconnect technologies are approaching physical limits that could determine how quickly next-generation systems advance.

The intended Feynman architecture proposes co-packaged optical interconnects through scale-up and scale-out interconnects, improving efficiency and eliminating external electro-optical connector losses. Interestingly, I have an old board on my desk from before the dotcom crunch of 2000 that contains embedded optical interconnects, although obviously built with technology more than two decades older.

Optics can bypass some board requirements, but pushing current copper foil grades and resin chemistries to their limits restricts the number of materials suppliers capable of delivering in volume. It also introduces manufacturability challenges that only a small number of board producers can handle.

That shrinking supplier pool creates two problems. It makes resilient supply chains harder to establish as protection against geopolitical uncertainty, and, more importantly, it creates a serious capacity constraint. AI server demand already compromises supply and manufacturing throughout the global PCB business and fundamentally reshapes the market. An even more rarefied supplier base would likely struggle to sustain the pace of investment required for new AI data centers.

As a species, humans have a strong record of overcoming technological obstacles that once appeared insurmountable. When we saw the end of Moore's Law and the potential threat it posed to continued economic development, we engineered our way into the More than Moore era. When transistor geometries approached their minimum limits, we created the FinFET as a three-dimensional solution.

But this time it *is* different because we are pushing against the physical limits of materials, and no obvious solution sits on the horizon.

Scientific research almost guarantees that somebody, somewhere, is working on something that could deliver the

breakthrough we need. Our built-in human insecurities make us sensitive to the possibility that we have reached the end of the road, despite our track record as problem solvers.

Today's research communities connect more closely than at any time in the past, thanks to the communication technologies and channels now available. Sharing knowledge and experimental results may create the conditions for a breakthrough by focusing multiple minds on the same problem.

On the other hand, history provides plenty of examples of parallel invention, including calculus, the telephone and the computer mouse, while also reminding us that sometimes a singular mind sees patterns invisible to everyone else. Charles Darwin had the same instruments available to him as anyone else in his field. The way he thought about what he saw produced the breakthrough.

As we look for a way to overcome the connectivity challenges in our path right now, I'll take the liberty of adapting another phrase to express the faith we must have in our ability to eventually produce a solution: "Cometh the hour, cometh the tech."

It is said that technological progress leads us to know more and more about less and less. Over time, we gain increasingly specialized insights into the technologies we develop. We need those insights, but our future success will also depend on a coordinated, cross-disciplinary approach that brings together chipmaking, multi-chip packaging and PCB design to achieve the data throughput and signal integrity needed to realize Rubin Ultra and Feynman servers.

And, of course, because we are human, the even faster and more powerful generations that inevitably come next. 



ALUN MORGAN is technology ambassador at Ventec International Group (ventecclaminates.com); alun.morgan@ventec-europe.com. His column runs monthly.



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The PCB Podcast

How to Safeguard PCB Quality in a Seller's Market

PCB buyers can safeguard quality by maintaining rigorous factory qualification, engineering review and material controls despite growing market pressures.

THE PCB MARKET has changed quickly.

Demand tied to AI infrastructure and advanced electronics is placing significant pressure on glass yarn, epoxy resin, copper foil, prepreg and copper-clad laminate. In some areas, material availability has become a greater constraint than factory capacity itself. At the same time, many of the strongest PCB factories face heavy workloads and have become more selective about the business they accept.

This creates a difficult environment for PCB buyers. When lead times extend and preferred factories reach capacity, buyers naturally feel pressure to move quickly, approve alternatives or accept assurances that might receive greater scrutiny under normal conditions. This is where quality risk begins to creep up.

A seller's market does not automatically mean lower quality, but it does require customers to exercise greater discipline. The focus must remain on using the right factory, materials and controls for the product, even when availability is limited.

Do Not Let Availability Become the Main Qualification Requirement

When delivery pressure increases, the first question often becomes: Who can build it fastest? That should never be the only question.

A factory may have open capacity, but that does not mean it is the right source for the product. A factory that performs well on standard two- to four-layer industrial boards may not have the experience or processes necessary for complex HDI or rigid-flex designs.

Factory selection should still reflect the PCB's actual requirements, including the factory's experience with the specified technologies and materials and the applications in which customers will use the boards. A general capability chart can be useful, but it does not tell the full story. A factory may claim the ability to manufacture a certain technology while having very limited experience running it consistently in production. In today's market, the safest

decision remains placing the product with a factory that has proven experience with that technology, not simply the first factory that says yes.

A proven factory regularly supports similar technologies as a core competency. If a factory builds one rigid-flex project annually, it has not demonstrated that it can manufacture the technology reliably, consistently or at scale. Companies should also prove factory capabilities through sample builds rather than live projects. Doing so establishes the risk threshold upfront, before a customer invests significant time and resources only to have boards fail quality testing or, worse, experience field failures because a factory took on more than it could reliably handle in an effort to win the business.

The market is full of quick-turn prototype suppliers and online marketplaces offering small quantities of PCBs for extremely low prices, sometimes advertising 10 boards for less than \$10 with delivery in only a few working days.

These services have a place. They can prove useful for early design validation, bench testing, educational projects and prototypes that will remain within a controlled laboratory environment. They can help an engineer confirm fit, function or basic electrical performance before moving into a more controlled production process. However, buyers should not confuse available prototype capacity with production capability.

A factory optimized for extremely low-cost, small-quantity online orders builds its model around speed, automation and standardized processing. That differs considerably from a production factory selected for long-term consistency, controlled materials, formal change management, detailed engineering review and repeatable quality across many production lots.

The issue is not that every low-cost prototype board will fail. Many will work perfectly well for their intended purposes. The question is whether the sourcing model provides the level of process control, material traceability and repeatability required for a product that will enter the field and remain in service for years.

A prototype that powers up on the bench has not demonstrated long-term reliability. It has not necessarily proven plated-through-hole robustness, material consistency, thermal endurance, solder mask durability or stable performance from lot to lot.

An old saying applies well here: you get what you pay for. Low-cost online prototype services can serve as valuable engineering tools, but companies should not automatically use them as production sources for medical, automotive, aerospace, defense, industrial or other reliability-driven products simply because they have available capacity.

Protect against unapproved material changes. Material substitution represents one of the biggest quality risks during a shortage. When the specified laminate becomes difficult to obtain, companies may feel pressure to quickly approve another brand or allow the factory to use an “equivalent” material. In some cases, the proposed alternative may be suitable. In others, it may only appear similar based on a few values taken from the datasheet.

Companies should never approve an alternate laminate based on Tg alone. The review should consider the full range of properties that matter to the product, UL recognition, and compatibility with both the PCB construction and

assembly process.

For high-speed or impedance-controlled designs, changing the selected laminate may also affect trace geometry and electrical performance. Engineers may need to rework the stackup and recalculate impedance structures rather than simply replace one material name with another. With today's constrained material supply chain, smaller factories may consider materials outside their normal approved selections when standard materials become unavailable. Materials that lack UL approval may remain readily available because of lower demand, tempting some fabricators to use these non-recognized materials and potentially compromise end-product quality and reliability. These conditions make material traceability and change control more important than ever.

Customers should confirm the laminate manufacturer, material family, construction and UL status before production. They should document, technically review and approve any substitution before the factory proceeds. As always, delivery of completed PCBs should include certificates from the base material manufacturers.

Be careful when moving an existing product. Moving a PCB from one factory to another involves more than a purchasing change. Each factory uses slightly different processes that can introduce subtle nuances into finished PCBs. No two factories are identical, and while two factories may both build to the same drawing, they can still produce boards with visible differences.

Before transferring an existing product, the new factory should complete a full engineering review rather than treat the build as a copy-and-paste exercise based solely on the previous supplier's stackup or finished-board data.

For critical post-production products, the transfer should include first-article inspection, microsection review, impedance verification, solderability testing, thermal-stress testing, assembly validation or additional reliability testing as appropriate. The amount of validation should match the product's risk. A simple commercial board may require a different level of qualification than a medical, aerospace, defense or high-reliability industrial PCB. The important point is to control and intentionally manage the change.

Maintain the normal engineering review. One of the easiest ways for quality to slip is for urgent orders to bypass the normal engineering process. During a constrained market, companies may feel pressure to reduce front-end review, leave open questions for later or move into production before resolving all engineering queries. That approach creates more risk, not less.

The factory should still properly review the stackup, material, copper weights, minimum spacing, annular ring, hole tolerances, aspect ratio, solder mask clearances, impedance requirements, via structures, surface finish, finished thickness and any special acceptance criteria.



Figure 1. Careful factory selection helps PCB buyers protect quality and reliability as material constraints and capacity pressures increase.

The customer and factory should resolve engineering questions before production begins. If a factory avoids asking questions because it wants to move the order quickly, customers should not automatically view that as good service. It may actually signal a problem. A lack of engineering questions may indicate that the product has not received sufficient review. The same principle applies to repeat orders transferred from another factory. The receiving factory must review the design against its own processes and controls rather than assume it can duplicate another fabricator's tooling decisions without evaluation.

A thorough PCB design review allows the factory to evaluate requirements and address potential engineering questions before production.

Keep quality controls in place on expedited orders. A fast build still requires the same level of process control, electrical testing, final inspection and documentation specified by the drawing and purchase order. When a supplier offers a lead time significantly shorter than the rest of the market, customers should ask how the supplier plans to achieve it.

The supplier should confirm that it physically has the correct material available, will keep the order at the approved factory, will complete the normal CAM review, and will maintain electrical testing, microsectioning, final inspection and required documentation. The supplier should also clearly disclose whether it plans to subcontract any portion of the work.

A legitimate expedite may involve priority scheduling, overtime or premium material purchasing. It should never involve skipping controls.

Use the right factory for the right product. Unprecedented demand driven by the buildup of AI infrastructure has stretched many of the industry's flagship factories far beyond their normal capacity. Under these conditions,

companies may feel tempted to send products to whichever source has room, particularly when delivery schedules begin to slip.

A better approach protects the most capable factories for the products that truly need them. Companies can place simple boards with qualified factories well suited to standard technology, while keeping complex HDI, rigid-flex, high-layer-count, low-loss and high-reliability products with factories that have the process control and experience necessary to manufacture them consistently.

Matching the product to the right factory reduces the likelihood of process exceptions, engineering misunderstandings and unstable production performance. It also reduces the risk of moving a complex product to an unproven source simply because the preferred factory is full. Although waiting for the right source may extend a delivery schedule, choosing the wrong factory can ultimately cost far more. Quality problems can require rework or replacement, disrupt downstream assembly and, in the worst cases, result in field failures, recalls or shortened product life cycles.

Understanding factory capabilities helps ensure each PCB comes from a factory with the appropriate experience and processes.

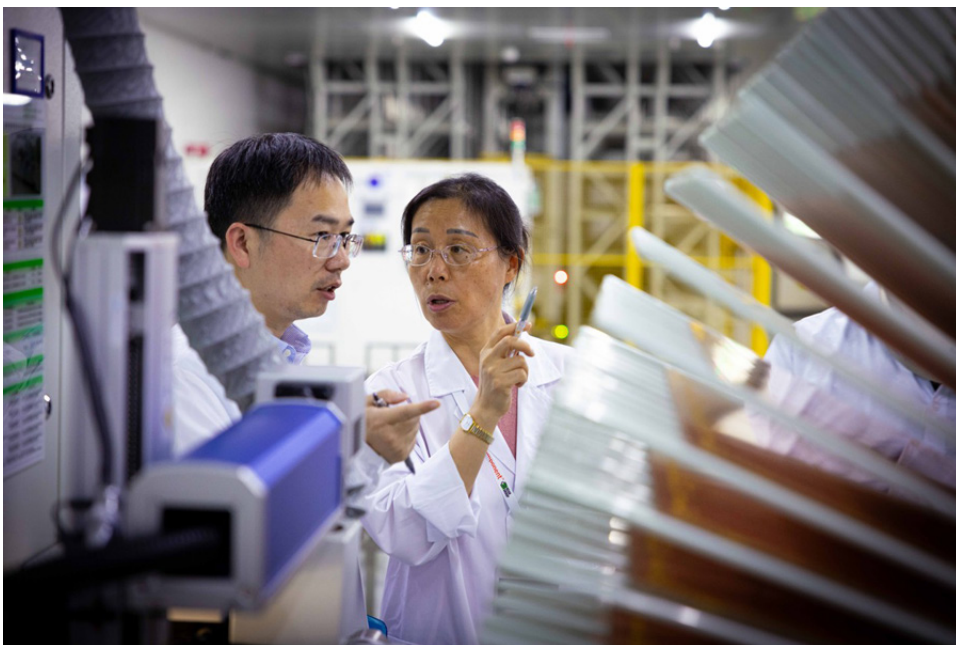


Figure 2. Strong engineering review, material controls and supplier qualification can reduce PCB quality risks in a seller's market.

Maintain strong change control. In a seller's market, factories may propose more changes than usual.

A factory may request an alternate laminate, revised stackup, different production site, alternate surface finish, adjusted copper weight or modified delivery plan. Customers should review each change through a formal process and understand exactly what is changing, why it is changing, and whether the change requires qualification or validation.

Verbal approval or informal email comments can create confusion later, particularly when several changes are under discussion at the same time. A change that appears commercially minor may carry significant technical or regulatory implications. Strong change control protects both the customer and supplier while ensuring the factory clearly understands the approved condition and properly reflects it in the manufacturing data.

Quality must remain the first filter. The current PCB market presents real challenges. Material supply remains tight, commercial pressure continues to increase, and many of the strongest factories have more business opportunities than they can accommodate. AI infrastructure demand has intensified those constraints, increasing the pressure on buyers to accept different materials, sources or manufacturing arrangements to keep products moving.

Those conditions make planning more important, but they also make technical discipline essential. A short-term delay caused by properly qualifying a factory or material can prove far less costly than a quality problem discovered after assembly or deployment. Once a PCB reaches the field, failures can lead to troubleshooting, replacement, recalls, lost production and shortened product life cycles, quickly outweighing any time saved during sourcing.

In a seller's market, the most important strategy for maintaining PCB quality remains simple: do not trade product quality for speed. Faster delivery is never worth introducing risks that could compromise product integrity, reliability or service life. 



JEFFREY BEAUCHAMP is director of technology & engineering at NCAB Group USA (ncabgroup.com); jeffreybeauchamp@ncabgroup.com. He started his career in the PCB industry in 2003 at P.D. Circuits, now part of NCAB Group, and works with PCB customers to provide optimal solutions. His column runs quarterly.

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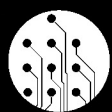
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Get Rid of Your Fab Drawing: IPC-2581 Already Has the Data

IPC-2581 can streamline PCB handoffs by keeping manufacturing requirements connected to intelligent design data.

A **SURPRISINGLY LARGE** number of technical queries (TQs) generated by a manufacturing partner after PCB design handoff have nothing to do with the design itself. They concern the documentation accompanying the design.

In fact, some manufacturers report that documentation-related issues can account for as much as 50% of the TQs generated after handoff.

Consider how much engineering effort goes into verifying a PCB design: running design rule checks, checking signal integrity, reviewing the stackup, verifying impedance requirements and confirming the design is ready for manufacturing. Then additional metadata and manufacturing instructions are manually entered as text in a fabrication drawing, disconnected from the design objects to which they refer. Every additional representation of the same information creates another opportunity for inconsistency.

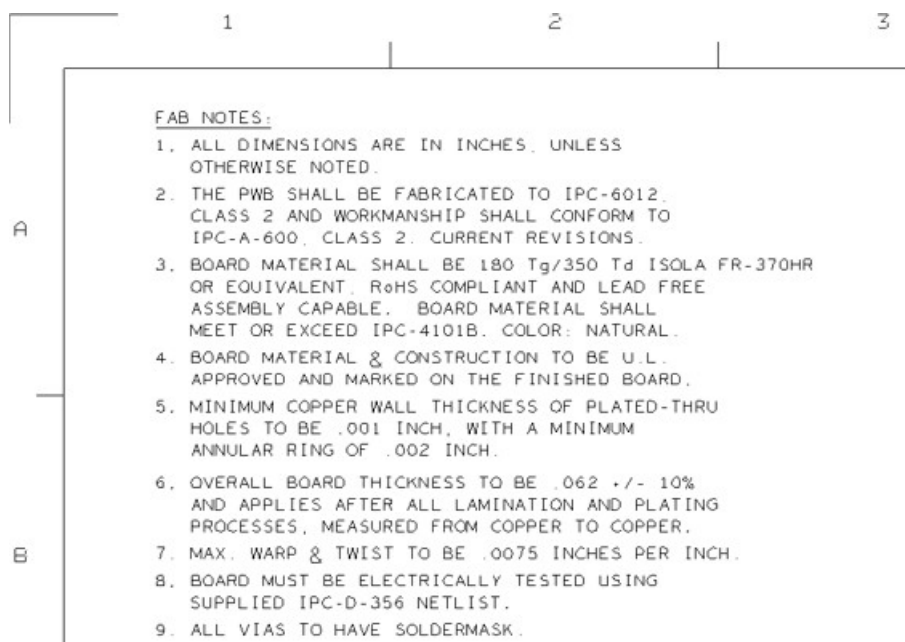


Figure 1. Sample fabrication drawing notes illustrate how manufacturing requirements are traditionally communicated separately from the intelligent PCB design data.

Traditional PCB manufacturing handoff packages require designers to create fabrication and assembly drawings. Although greater automation is available for generating these drawings today, they remain another representation of information that often already exists elsewhere in the design. Whenever the same information exists in two or three places, there is a possibility those sources will disagree. That is where many unnecessary TQs begin.

A dimension on the fabrication drawing may not match the actual board outline. The documented stackup may differ from the stackup data. A note may specify one copper weight while another document specifies something else. The number of holes listed in the documentation may not agree with the manufacturing data. The manufacturer then has to determine which information is correct.

Interestingly, when manufacturers find discrepancies between fabrication documentation and Gerber data, one response they sometimes receive from the design organization is, “Use the Gerber data.” In other words, ignore the documentation because the graphical manufacturing data is the master.

That raises a basic question: In the age of AI, why are we still spending engineering time creating documentation that may ultimately be ignored? Why not provide intelligent manufacturing data containing the information the manufacturing partner needs and eliminate as much duplicate documentation as possible? That is one of the less-discussed, but very practical, benefits of IPC-2581.

Where the discrepancies begin. A typical fabrication drawing contains a significant amount of information beyond the graphical representation of the PCB, including dimensions, tolerances, stackup references, material requirements, plating requirements, impedance information, fabrication instructions, test requirements and other manufacturing notes. All this information must remain synchronized with the actual design.

Manufacturers report discrepancies involving dimensions or tolerances that do not match the board outline, incorrect hole or via counts, differences between the documented and actual stackup, conflicting impedance or loss requirements, netlist differences, conflicting material or plating requirements, and fabrication notes that reference obsolete or incorrect documents.

In a traditional manufacturing package, drawings contain instructions while Gerber, drill, netlist and other files contain different portions of the manufacturing data. When these representations disagree, the manufacturer has little choice but to generate a TQ.

Someone at the design organization must then research the question, determine which information is correct, respond to the manufacturer and, in some cases, issue updated documentation. Multiply that process across several questions, boards and manufacturing partners, and a seemingly minor documentation problem can consume a significant amount of engineering time. More importantly, every TQ can delay manufacturing.

Netlist limitations. Netlist information in traditional manufacturing packages is commonly transferred using IPC-D-356 or IPC-D-356A. These formats have limitations and do not adequately represent certain aspects of design intent, including intentional shorts and intentional opens.

As a result, some manufacturers report that designer-supplied netlists cannot always be used in production exactly as received. Additional interpretation or processing may be required. Again, the design itself is not necessarily wrong. The manufacturing package simply does not completely communicate design intent.

Using IPC-2581 to reduce documentation. IPC-2581 has been in production use across the industry for approximately a decade. One capability introduced into the standard several revisions ago permits specifications and notes to be associated directly with the design and individual design objects. IPC-2581 provides this capability through the SPEC element.

A SPEC element may not sound particularly exciting, but it can eliminate a surprising amount of traditional documentation. Instead of placing manufacturing instructions only on a separate fabrication drawing, that information can become part of the intelligent PCB design data.

Companies using IPC-2581 can therefore reduce – and in some cases eliminate – traditional fabrication and assembly notes when transferring PCB data to manufacturing partners.

The SPEC element. An IPC-2581 SPEC element is created by the PCB design tool based on information entered during design. When the IPC-2581 file is generated, the information is included directly in the data file. Technically, SPEC is an XML element within the IPC-2581 file transferred to the manufacturing partner.

The important point, however, is not the XML structure. It is the manufacturing information the element can communicate.

A SPEC can be associated with the PCB itself or with specific objects within the design. Board-level fabrication information, for example, can identify the applicable IPC class, board type, material, copper weight, surface finish, plating requirements, panelization, panel orientation, markings and test requirements. These are the same types of instructions traditionally placed on a fabrication drawing. With IPC-2581, they can travel with the intelligent design data.

Making fabrication notes part of the design. Defining fabrication requirements through SPEC elements makes those requirements part of the design and includes them in the IPC-2581 manufacturing data. An IPC-2581 viewing or manufacturing tool can read the information directly from the file.

This eliminates the need to locate the correct drawing revision and manually correlate a note on that drawing with information contained in several other files. The information instead travels with the design, reducing one of the most common problems associated with document-based handoffs: ensuring everyone is working from the correct revision.

Spec Definition

Name:

Data Elements

☒ Design ☐ Nets ☐ Comps ☐ Shapes ☐ Lines ☐ Clines

Spec Type: Sub Type:

Spec Type	Sub Type	Property
General	INSTRUCTION	All Dimensions are in Inches unless otherwise specified
General	STANDARD	Fabricate PCB per IPC-6012, Class 2 and conform to
General	MATERIAL	Board material and construction to be U.L. Approve

Figure 2. Fabrication notes entered within the PCB design can be incorporated directly into IPC-2581 data and maintained with the design revision.

Associating specifications with design objects. SPEC information becomes even more useful when associated with individual design objects.

Consider the plating requirements for a connector. Instead of placing a generic note on the fabrication drawing and requiring the manufacturer to determine which feature it applies to, the specification can be associated directly with the appropriate object.

The same concept applies to controlled-impedance traces. Manufacturers need more than a general note stating that certain traces require impedance control. They need to know which traces require impedance control and the applicable requirements.

The image shows a software dialog box titled "Spec Property Def...". At the top, it says "Spec Type: Impedance / IMPEDANCE". Below that, "Data Type:" has two radio buttons: "Text" and "Number", with "Number" selected. A red circle labeled 'a' points to the "Text" radio button. The "Text" section has a large empty text box. Below it are "Import..." and "View..." buttons. The "Number" section has a "Value:" field with "50" (callout 'b'), a "Unit:" dropdown menu showing "OHMS" (callout 'c'), and "Tol. By:" radio buttons for "Value" and "Percentage" (callout 'd'), with "Percentage" selected. Below these are "Tol. Plus:" and "Tol. Minus:" fields, both containing "3" and followed by a "%" symbol. A red circle labeled 'e' points to the "Tol. Minus" field. At the bottom of the "Number" section is a "Comment" text box (callout 'f'). At the very bottom of the dialog are "OK", "Cancel", and "Help" buttons.

Figure 3. IPC-2581 SPEC information can be associated directly with individual design objects to communicate specific manufacturing requirements.

Associating SPEC information with the relevant design objects provides a more precise representation of design intent than a note placed separately on a drawing.

Including assembly instructions. The same approach applies to assembly requirements. Suppose a component requires a heat sink installed using a specific process. The assembly instructions may require application of a particular thermal epoxy before heat sink installation.

Rather than placing those instructions in an assembly drawing or separate manufacturing document, they can be associated with the appropriate component. The instruction and the object to which it applies then travel together as part of the intelligent manufacturing data.

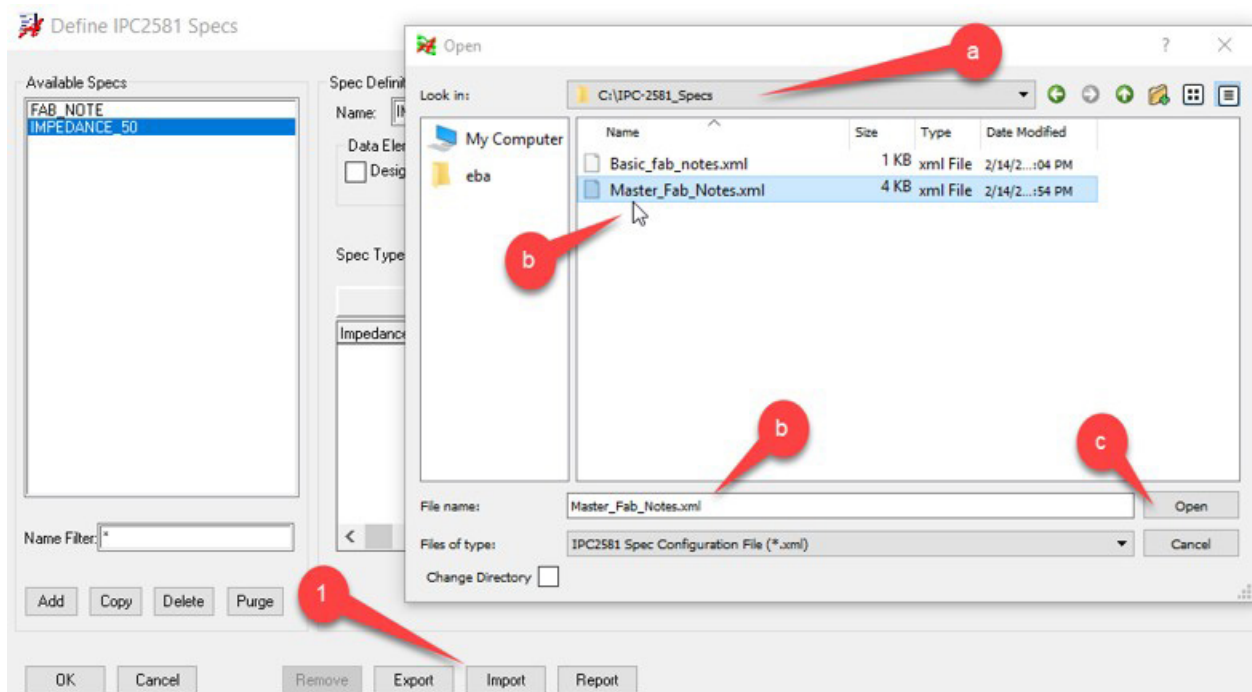


Figure 4. Assembly requirements can be associated with specific components so the instructions and corresponding design objects remain linked in the manufacturing data.

Reducing references to separate documents. Fabrication notes frequently direct manufacturers to separate documents for information already available within the PCB design data. A typical note might instruct the manufacturer to refer to a stackup document for board thickness and impedance requirements. That approach introduces another document that must be included in the manufacturing package, located by the manufacturer, maintained at the correct revision and checked against the rest of the manufacturing data.

IPC-2581 can communicate stackup information as intelligent data. Creating a separate document simply to direct the manufacturer to information that can already reside in the manufacturing data adds another potential source of inconsistency. Reducing the number of separate representations of the same information reduces the opportunity for conflicts among those sources.

Communicating intentional shorts and opens. The same principle can be applied to electrical intent. For intentionally shorted or intentionally open nets, a SPEC element can be associated with the appropriate nets to communicate that condition to the manufacturing partner. Instead of discovering what appears to be an inconsistency and generating a TQ, the manufacturer receives information explaining the condition with the design. An intelligent manufacturing handoff should communicate more than the geometry that exists. It should also communicate the designer's intent.

Reusing manufacturing specifications. Entering manufacturing specifications individually for every PCB could become time-consuming, but many requirements repeat across designs. Engineering organizations already maintain libraries for components, footprints, design rules and other reusable design information. The same approach can be applied to commonly used manufacturing specifications.

PCB design tools can store these specifications for reuse according to the requirements of a particular design. An

organization might maintain approved specifications for different IPC classes, fabrication technologies, copper weights, surface finishes, materials, via structures, test requirements and assembly processes. Instead of recreating fabrication notes for every PCB, the designer can begin with an approved set of specifications and modify only the requirements unique to that design.

Standardized templates can also improve consistency among design teams and PCB projects, reducing variability before the manufacturing package is generated.

From drawings to intelligent data. The objective is not simply to eliminate a drawing. It is to eliminate duplicate, manually maintained representations of information when that information can instead be communicated as intelligent data.

Traditional PCB handoff practices developed when drawings were one of the primary means of communicating manufacturing intent. Modern PCB design systems contain considerably more information about the design, including board geometry, stackup, nets, vias, components, materials and constraints. IPC-2581 SPEC elements extend that information to manufacturing requirements that historically resided only in drawings.

A fabrication drawing may still be appropriate for certain company-specific or manufacturing requirements, and eliminating drawings entirely may not be practical for every organization or PCB. But drawings should not be generated simply because that has historically been the handoff process. The better question is what information the manufacturing partner actually requires and whether IPC-2581 can communicate it directly. In many cases, it can.

Fewer documents, fewer TQs. The primary benefit of incorporating fabrication and assembly information into IPC-2581 is not simply the time saved by eliminating a drawing. More important is reducing the number of independent sources of manufacturing information that must remain synchronized throughout the life of the design.

With IPC-2581, manufacturing notes and specifications can become part of the intelligent design data rather than being manually duplicated across separate documents. Specifications can be associated with the PCB or directly with the objects to which they apply. Stackup information can travel as stackup data, impedance requirements can be associated with the relevant design information, and intentional shorts and opens can be identified before they generate questions during manufacturing.

The result is fewer opportunities for conflicts among drawings, stackup documents, netlists and manufacturing files. It can also reduce documentation-related TQs, simplify revision control and limit the engineering time spent resolving avoidable questions after design release.

Reusable libraries and templates add another benefit by providing a consistent set of approved fabrication, assembly and test requirements across multiple designs.

IPC-2581 is sometimes described simply as a replacement for Gerber or other PCB manufacturing data exchange formats. That description understates its potential. The larger benefit is the transition from a collection of drawings and loosely connected files to an intelligent manufacturing handoff capable of communicating both the PCB design

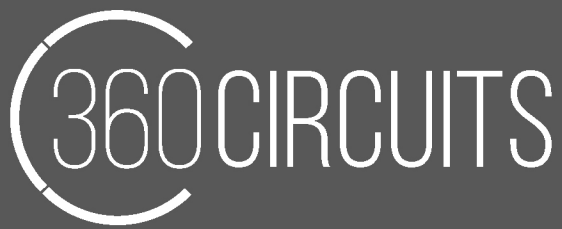
and its intent.

Before generating the fabrication drawing for the next PCB, consider how much of the information on that drawing already exists – or could exist – within the IPC-2581 data. The drawing may contain far less unique information than it appears. 



HEMANT SHAH is an EDA veteran and chair of the IPC-2581 Consortium (ipc2581.com). Shah led the effort to create an industry-wide consortium of design and supply chain companies to get IPC-2581 – the standard for transferring PCB design data to manufacturing – adopted.

He spent 20 years at Cadence as product manager for various PCB design products. Shah also led the industry adoption of the IBIS-AMI algorithmic modeling standard. Prior to joining Cadence, Shah worked at Xynetix and Intergraph. He is passionate about developing and marketing leading-edge software products for PCB design.



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High-Power Thermal Management: Two-Layer IMS Design Considerations

As power electronics become more compact and power-dense, two-layer IMS PCB designs are helping improve thermal management, reliability and EMI performance in high-power applications.

by CHRIS PARKER

As electronic systems become more compact and power-dense, effective thermal management has emerged as a primary bottleneck to performance, efficiency, and long-term reliability. These increasing thermal demands are exposing the limitations of conventional FR-4 materials and accelerating the adoption of advanced substrate constructions, such as two-layer insulated metal substrates (IMS), in high-power applications.

Although FR-4 remains a cost-effective and widely used solution for low-power designs, its inherently low thermal conductivity and reliance on dense thermal via networks limit its suitability for advanced power systems based on gallium nitride (GaN) and silicon carbide (SiC) semiconductors. While GaN and SiC power transistors can withstand higher junction temperatures than traditional silicon devices, this capability offers little benefit unless the rest of the PCB assembly can reliably operate under the same conditions.

In contrast, two-layer IMS PCB constructions integrate a thin, thermally conductive dielectric with a metal baseplate, enabling efficient heat transfer directly beneath power components. This architecture lowers junction temperatures, enhances mechanical stability, and supports electromagnetic shielding and space-efficient routing strategies.

This article examines the growing adoption of IMS constructions in high-power, mission-critical applications and analyzes the structural and material properties that lead to measurable advantages in performance and reliability. Key design considerations unique to IMS technology are also discussed. Finally, a Texas Instruments case study illustrates how switching to an IMS board construction can reduce junction-to-ambient thermal resistance by up to 45% compared to an equivalent FR-4 design operating under similar conditions. Together, these insights provide a practical framework to support informed material and design decisions in high-power circuit applications.

Evolution and Adoption of IMS in High-Power Module Design

IMS technology gained widespread adoption in the 1990s as telecommunications rapidly expanded. DC-DC converters – particularly quarter-brick and half-brick power modules – became standardized around fixed mechanical footprints (2.28×1.45 inches and 2.28×2.20 inches, respectively), enabling compact, board-mounted, isolated power conversion across a wide operating range, from approximately 50 watts to over 600 watts. The combination of

standardized external footprints and flexible internal architectures made IMS a natural fit for brick converters, enabling substantial increases in power density and reliability without altering established system-level form factors.

Internally, these converters rely on high-current copper planes, dense thermal via arrays and increasingly, IMS substrates. By enabling MOSFETs, GaN and SiC switches, magnetic components and rectifiers to transfer heat directly into a metal baseplate, IMS eliminates the thermal bottlenecks inherent in conventional FR-4 constructions. The metal base acts as an efficient heat spreader, provides improved mechanical stability under shock and vibration, and supports the stringent thermal performance requirements of the telecom and datacom sectors.

By the early 2000s, IMS board constructions had expanded into the defense and aerospace sectors to address the more demanding requirements of radar and RF power systems. These applications emphasized electromagnetic interference (EMI) containment, long-term reliability, and resistance to wide-range thermal cycling. Over the past two decades, IMS adoption has continued to expand across a wide range of high-power applications, including:

- **Defense and radar power supplies.** Where large, continuous copper ground planes on IMS substrates provide inherent RF shielding and predictable EMI performance.
- **Directed-energy and avionics platforms.** These require high breakdown voltages, mechanical rigidity, and stable operation across extreme temperature swings.
- **Industrial power converters (DC-DC, AC-DC, DC-AC).** Often implemented with an IMS power stage paired to an FR-4 control board for optimal thermal and routing performance.
- **Motor drives and inverters.** Where direct attachment of power semiconductors to the metal base enables efficient heat extraction and improved long-term reliability.

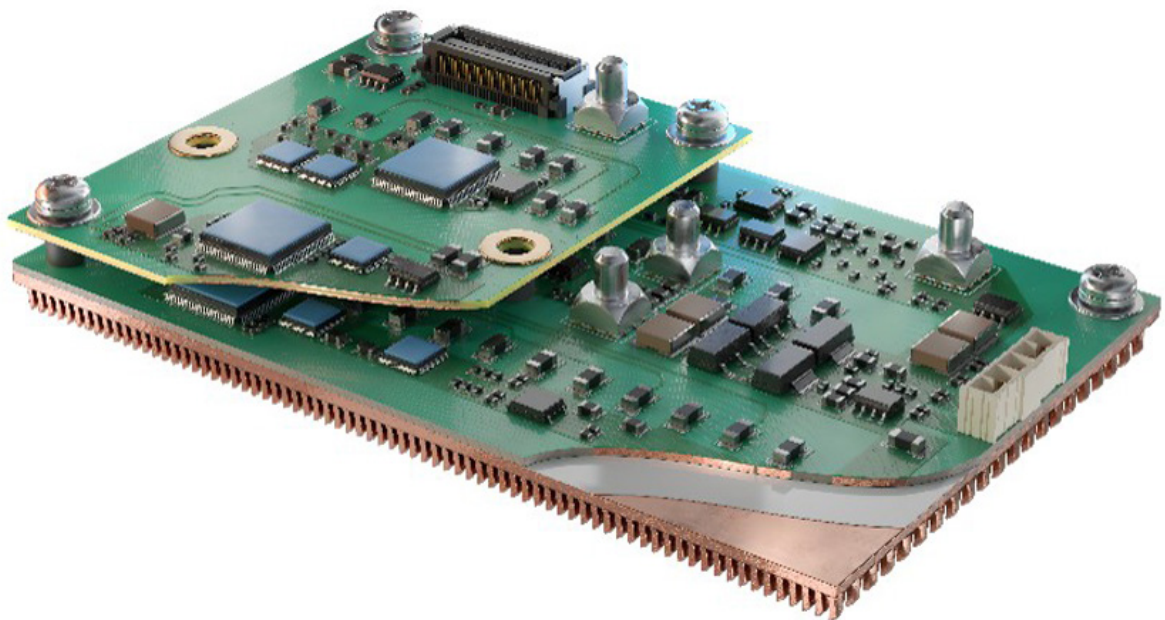


Figure 1: An insulated metal substrate (IMS) printed circuit board assembly provides efficient heat dissipation for high-power electronic applications.

How the Choice of Metal Shapes IMS Performance

Approximately 80% of IMS applications employ aluminum baseplates, valued for their favorable cost, light weight, ease of machining, and effective thermal spreading capability. Aluminum's coefficient of thermal expansion (CTE), typically around 22–24ppm/°C, is acceptable for most power electronics and is generally well accommodated by compliant dielectric layers and typical semiconductor packages. In high-stress, high-reliability environments, however, roughly 20% of IMS constructions utilize copper baseplates.

Typically, aluminum is selected when the combined copper thickness is less than 10% of the aluminum base plate thickness. When copper foil thickness exceeds 10% of the aluminum base plate thickness and includes large internal ground planes, copper is selected to maintain part flatness and reduce internal stress caused by the relatively high CTE of aluminum.

Copper baseplates offer two key advantages.

- **Superior CTE Matching.** Copper's CTE (~16–17ppm/°C) closely matches that of copper circuitry, plated vias, and many package leadframes. This tighter CTE alignment significantly reduces thermomechanical shear stress at the copper-dielectric-metal interfaces during thermal cycling. The benefit is particularly pronounced in heavy-copper constructions, designs subjected to rapid thermal transients (such as GaN and SiC switching), embedded-die architectures, and aerospace or defense modules that must withstand thousands of thermal cycles over decades of service.
- **Higher Thermal Conductivity.** With a thermal conductivity of approximately 400W/m·K – roughly twice that of aluminum (~200W/m·K) – copper enables faster heat spreading and more uniform temperature gradients beneath power devices. The superior thermal performance of copper is essential for high-density converters and mission-critical systems where localized hot spots can degrade reliability.

While copper baseplates introduce higher material cost and weight, the resulting gains in mechanical stability, resistance to warpage, and long-term solder joint reliability often outweigh these trade-offs in demanding applications. For this reason, copper remains the substrate of choice when maximum reliability, controlled thermal expansion, and robust thermal cycling performance are non-negotiable.

Why the Second Layer Matters

Two-layer IMS boards represent more than an incremental improvement over single-layer substrates; they directly address several fundamental challenges inherent in high-power, high-frequency and high-density electronics. Engineers typically introduce a second layer to improve EMI resistance, enhance circuit routing flexibility and boost thermal performance in compact power systems.

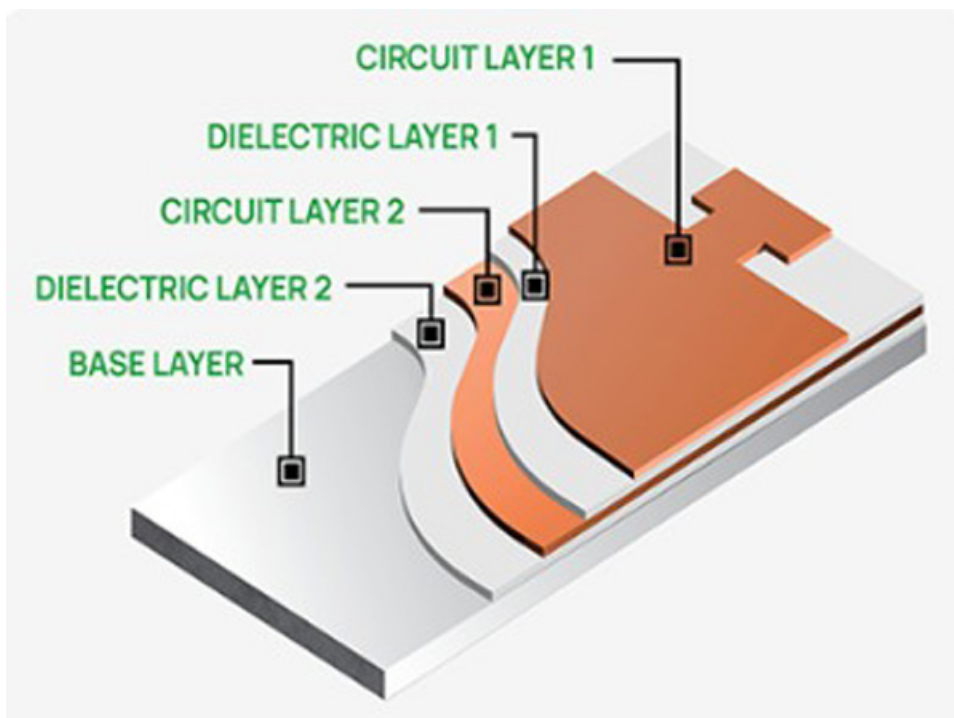


Figure 2: A two-layer IMS construction uses an internal layer to improve RF shielding, EMI control and high-frequency signal stability in high-power electronic designs.

In military, aerospace, and radar applications, the second layer in a two-layer IMS stackup is often implemented as a continuous internal ground plane. This buried copper layer serves as an effective RF shield, providing significant electromagnetic performance benefits. This also establishes a low-impedance, low-inductance reference plane that suppresses switching noise from fast GaN and SiC power devices, reducing both radiated and conducted EMI. It also improves signal integrity by providing well-controlled return paths for high-frequency and high-speed signals.

In addition, the internal ground plane enhances the system's immunity to noise by electrically isolating sensitive control and signal circuitry from high-energy power stages, supporting compliance with stringent military and aerospace electromagnetic compatibility (EMC) requirements.

Radar and directed-energy platforms frequently combine this internal ground plane with dense via stitching around electrically noisy regions. These vias electrically connect the top copper layer to the internal ground plane, forming a vertical Faraday barrier that confines electromagnetic fields within defined boundaries. The result is a cleaner, more controlled RF environment that remains stable across temperature extremes, load variations, and switching conditions.

For systems characterized by rapid voltage transitions (high dv/dt), RF sensitivity or space constraints, the inclusion of an internal ground plane offers a highly effective method of EMI control and high-frequency stabilization, without introducing significant complexity to the overall system design.

In applications such as industrial power supplies, motor drives, telecom brick converters and high-density power modules, the benefits of a second IMS layer extend beyond EMI containment. A buried copper layer enables functional separation of circuitry within constrained footprints while simultaneously improving thermal

performance.

The second layer allows designers to physically separate power and signal functions within the board. Low-current, noise-sensitive control and signal traces can be routed on the internal layer, while high-power traces remain on the top layer, where thicker copper and wider traces are easier to implement. This approach supports space-efficient layouts, enabling increased routing density while maintaining creepage, clearance and thermal conduction path requirements.

In more advanced constructions, portions of the top dielectric can be selectively removed to expose copper features on the second layer. These localized “copper wells” allow power components, such as MOSFETs, diodes, LEDs or bare die, to be mounted nearer to the metal baseplate. Reducing the thermal path length lowers effective thermal resistance, decreases steady-state operating temperatures and improves long-term reliability.

In these architectures, the second layer serves as a multifunctional element in both the electrical and thermal strategies. Depending on system requirements, it may serve as a shield, a low-current routing layer, a heat spreader, or a component mounting surface. This flexibility is particularly valuable in applications that must balance high power density, EMI compliance and mechanical robustness within a compact, space-constrained PCB assembly.

Design Considerations: Copper Weight, CTE Constraints and Baseplate Selection

Selecting copper weight in a two-layer IMS design requires careful balancing of thermal performance, manufacturability and mechanical reliability. While heavier copper improves current-carrying capacity and heat spreading, it also increases mechanical stress within the dielectric and metal stackup, particularly when paired with aluminum substrates.

Copper weight limitations. In most two-layer IMS constructions, the internal copper layer is limited to 4oz using standard processes. Designs exceeding 4oz are technically feasible but become more design-dependent and may require additional operations.

Heavy copper effectively stiffens the copper-dielectric stack, reducing the dielectric’s ability to accommodate differences in thermal expansion between layers. The use of thick copper layers may require a transition to a copper base plate to minimize internal stress.

When higher copper weights are required. Applications such as motor drives, high-current DC-DC converters, and pulsed-power systems may require copper thicknesses greater than 4oz. on one or both layers. In these cases, maintaining reliability often requires changes to the IMS’s mechanical structure.

Copper baseplates are particularly advantageous for thick-copper designs because their CTE ($\sim 16\text{--}17\text{ppm}/^\circ\text{C}$) closely matches that of copper foil. This alignment significantly reduces shear stress during thermal cycling compared to aluminum baseplates, which have higher CTE values ($\sim 22\text{--}24\text{ppm}/^\circ\text{C}$) and expand more aggressively, increasing the

risk of distortion in heavy-copper constructions.

Copper thickness rule of thumb. A practical engineering guideline is to limit the total copper thickness on any layer to roughly 10% of the metal baseplate thickness. When the copper thickness exceeds this ratio, internal stresses become difficult to manage, the risk of warpage increases and dielectric integrity may be compromised.

Dielectric Selection: Thickness, Via Structure and Thermal Design Principles

Dielectric selection is central to IMS performance, directly influencing thermal behavior, electrical isolation, and mechanical stability. Two-layer IMS designs typically employ one of three dielectric classes: high-temperature (HT), high-performance (SFL), and standard-performance (SPL).

Among these, HT dielectrics are the variety most commonly used in two-layer IMS constructions due to their high breakdown voltage, good thermal capability and excellent reliability in harsh operating environments.

Selecting dielectric thickness requires balancing thermal performance against voltage-isolation requirements. Thinner dielectrics reduce thermal resistance and improve heat transfer to the metal baseplate, while thicker dielectrics increase breakdown voltage and provide additional margin during high-potential (HIPOT) testing. Standard thickness ranges are typically 3-12mils for HT dielectrics, with custom thicknesses reserved for high-volume or highly specialized applications.

Table 1: Relationship Between Dielectric Thickness and Dielectric Strength

Dielectric	120VAC	240VAC	480VAC	960VAC	1200VAC
HT 75µm	*	*			
HT 150µm	*	*	*	*	
HT 225µm	*	*	*	*	*

Designers typically qualify thicknesses using test voltages on the order of twice the maximum operating voltage, plus a safety margin, while avoiding operation near the material’s intrinsic breakdown strength to preserve long-term reliability.

Via structure. Via structures are another critical element in IMS design. Plated through-hole vias provide vertical heat transfer, carry current between layers, and enable stitched shielding for EMI control. Filled vias improve planarity and enhance thermal conduction, while arrays of parallel vias increase current-carrying capacity and reduce localized heating.

Thermal design principles. From a thermal standpoint, IMS substrates significantly outperform FR-4 laminates because heat is rapidly conducted through the dielectric into the metal baseplate. This efficient heat-spreading

capability enables higher current densities and more compact routing. Conventional FR-4 trace current calculators often underestimate the current-carrying capacity of IMS constructions because they don't account for enhanced heat dissipation through the metal core and adjacent copper planes. As a result, IMS designs can often use narrower traces or thinner copper to achieve equivalent current ratings, an important advantage in space-constrained power modules.

Compared with FR-4 constructions that rely on dense thermal via arrays to move heat toward the baseplate, TCLAD thermally conductive dielectrics spread heat across the full metal baseplate area. The result is lower, more uniform junction temperatures, rather than the localized conduction paths that via arrays provide. This approach also eliminates the incremental drilling, plating, and via-fill operations that dense-via FR-4 boards require, reducing fabrication cost and shortening lead time at production volumes.

System-Level Considerations: When the Entire Thermal Stack Matters

Overall heat dissipation is governed by the entire thermal stack, not just the IMS baseplate and dielectric. Cooling strategies, interface materials, package design, mechanical clamping and heat sink geometry all influence system-level thermal performance. Accurate thermal modeling must account for every interface in the thermal path, including copper layers, dielectrics, solder joints, thermal interface materials (TIMs) and mounting hardware, to avoid overly optimistic temperature predictions.

Some IMS designs use selective dielectric removal to expose copper features on the second layer, creating localized "copper wells." These structures shorten the thermal path to the metal baseplate, reduce parasitic loop inductance, and improve heat dissipation for power semiconductors or LEDs, while simultaneously freeing routing area on the top layer. This approach improves performance by incorporating features commonly associated with embedded-die techniques, blurring the boundary between IMS construction and advanced packaging technology.

In many practical systems, an IMS-based power board is paired with a separate FR-4 control or logic board, interconnected through press-fit pins, board-to-board connectors, or soldered headers. This architectural separation keeps temperature-sensitive electronics away from high heat flux regions while allowing the board to fully leverage the thermal advantages of IMS construction.

In high-voltage applications, partial discharge inception voltage (PDIV) becomes a critical design consideration. Partial discharges can initiate within voids, interfaces or material imperfections in the dielectric when localized electric fields exceed a critical threshold. Although these discharges may not cause immediate failure, repeated partial discharge activity accelerates dielectric aging. To ensure long-term dielectric reliability, designers evaluate PDIV under combined electrical and thermal stress conditions representative of real operating environments. Elevated temperatures reduce dielectric strength and increase discharge activity, making PDIV testing especially important for wide-bandgap power systems that operate at higher voltages, switching speeds, and junction temperatures. Proper control of dielectric thickness, material selection, and void-free processing is therefore essential to maintaining sufficient PDIV margin throughout the life of the IMS assembly.

Together, these system-level considerations enable engineers to optimize IMS-based designs for thermal performance, electrical isolation and long-term reliability in demanding power electronics applications.

IMS vs. FR-4. To quantify the thermal performance differences between conventional FR-4 and IMS PCB constructions, Texas Instruments conducted a comparative study. The evaluation used two-layer FR-4 and two-layer IMS PCBs with similar layouts, as illustrated in the cross-sectional views in **Figure 3**.

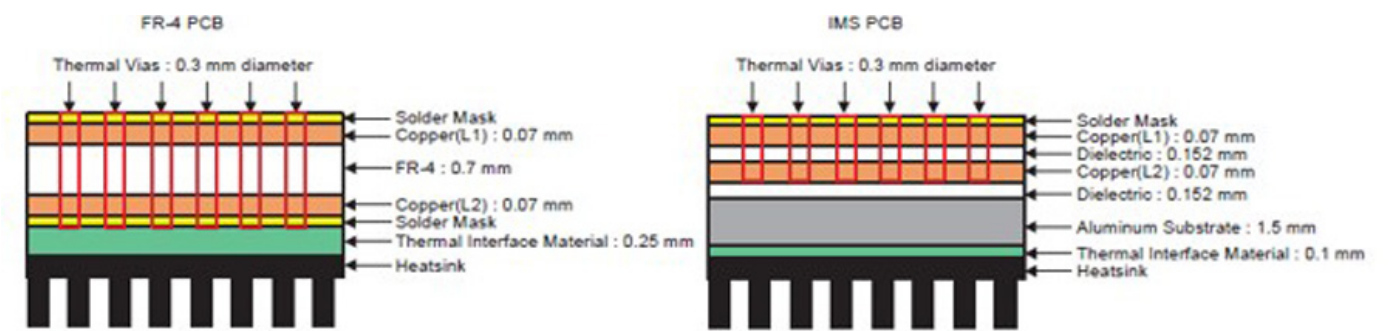


Figure 3. This comparison illustrates how an IMS PCB construction can provide improved thermal performance over a conventional FR-4 design in high-power applications.

The thermal performance of each board was evaluated using six Texas Instruments three-phase GaN inverters (LMG3410R050) driving a motor in a high-power, high-switching-frequency operating environment.

In both cases, a thermal interface material (TIM) was applied between the PCB and an anodized aluminum heat sink to ensure consistent contact and minimize thermal resistance. All testing was performed under natural convection conditions.

Both the FR-4 and IMS boards delivered a continuous RMS current of 3 amps to drive a 200-volt, three-phase motor. Operating conditions were maintained until steady-state temperatures were reached.

Table 2 summarizes the thermal resistance contributions along the heat-dissipation path for both FR-4 and IMS implementations, including vias, dielectrics, interface materials and the heat sink.

Table 2: Thermal Resistances Across the Heat-Dissipation Path (FR-4 vs. IMS)

Thermal Resistance (°C/W)	FR-4 PCB		IMS PCB	
	Top-Side FET	Bottom-Side FET	Top-Side FET	Bottom-Side FET
Junction to case (R_{JC})	0.5	0.5	0.5	0.5
PCB thermal vias (R_{VIAS})	3.76	2.03	0.83	0.76
Dielectric ($R_{dielectric}$)	N/A	N/A	3.1	2.08
Aluminum (R_{AL})	N/A	N/A	0.3	0.3
TIM (R_{TIM})	25.5	17.13	2.57	2.57
Heat Sink ($R_{Heat\ Sink}$)	31.8	31.8	31.8	31.8
Junction to ambient (R_{JA})	61.56	51.46	39.1	38.01

Conclusion

This study demonstrates the significant thermal performance advantages of TCLAD IMS technology over conventional FR-4 PCB constructions. Experimental results show that the FR-4 PCB exhibits approximately 45% higher average junction-to-ambient thermal resistance than the IMS PCB, confirming the superior heat dissipation capability of IMS for high-power, high-density electronic applications. These findings highlight IMS as an effective solution for improving thermal management, enhancing system reliability and extending the operational life of power electronic devices.

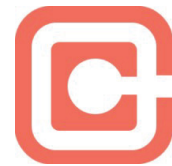
As power electronics continue to evolve toward higher voltages, faster switching frequencies, and increased power density, the inherent thermal, electrical, and mechanical limitations of FR-4 substrates become increasingly restrictive. Two-layer IMS architectures provide a compelling alternative by offering enhanced thermal management, robust electrical isolation, improved EMI containment and greater mechanical stability, attributes that are particularly critical for GaN- and SiC-based power systems operating near their performance limits.

Nevertheless, achieving optimal IMS performance depends on careful material selection and design optimization. Dielectric properties, copper layer configuration, thermal interfaces and system-level constraints must be considered holistically to balance thermal efficiency, electrical reliability and manufacturability. Leveraging application-specific expertise in these areas is essential to fully realize the benefits of IMS technology in real-world power electronics designs. 

CHRIS PARKER is product engineering manager at TCLAD (tclad.com); chris.parker@tclad.com.

Thank You!

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The logo for ACCURIS features a stylized blue icon resembling a circuit board or a stylized 'A' to the left of the word "ACCURIS" in a blue, sans-serif font.The logo for all flex SOLUTIONS features a stylized orange 'A' with a circuit board pattern inside, above the text "all flex" in a blue, sans-serif font, with "SOLUTIONS" in a smaller, orange, sans-serif font below it.The logo for AllSpice.io features a stylized blue circuit board icon to the left of the text "AllSpice.io" in a blue, sans-serif font.The logo for ASC features a stylized blue circuit board icon to the left of the letters "ASC" in a bold, black, sans-serif font.The logo for BEST Technology features the word "BEST" in a large, bold, blue, sans-serif font, with "Technology" in a smaller, blue, sans-serif font below it.The logo for BOARDERA features the word "BOARDERA" in a grey, sans-serif font, with the letter 'E' stylized in green.The logo for CED features the letters "CED" in a bold, black, sans-serif font, with "CHESTER ELECTRONIC DESIGN" in a smaller, black, sans-serif font below it.The logo for cofactr features a green circuit board icon to the left of the word "cofactr" in a green, sans-serif font.The logo for Cybord features the word "Cybord" in a blue, sans-serif font, with a stylized blue circuit board icon to the right.The logo for DirectPCB features a stylized green circuit board icon to the left of the text "DirectPCB" in a green, sans-serif font.The logo for ep ELECTRONIC INTERCONNECT features a stylized blue 'ep' logo to the left of the text "ELECTRONIC INTERCONNECT" in a blue, sans-serif font, with "THE PCB EXPERTS" in a smaller, blue, sans-serif font below it.The logo for elSYCA features a blue circuit board icon to the left of the text "elSYCA" in a blue, sans-serif font.The logo for EMA Design Automation features the word "EMA" in a bold, red, sans-serif font, with "Design Automation" in a smaller, blue, sans-serif font to the right.The logo for ESPEC features the word "ESPEC" in a stylized, orange, sans-serif font.The logo for FINELINE features the word "FINELINE" in a bold, black, sans-serif font, with "EXCELLENCE IN PCB" in a smaller, black, sans-serif font below it.The logo for FREEDOMCAD features a stylized blue circuit board icon to the left of the text "FREEDOMCAD" in a blue, sans-serif font, with "ELECTRONIC PRODUCT DEVELOPMENT" in a smaller, blue, sans-serif font below it.The logo for GFE features the letters "GFE" in a green, sans-serif font, with a stylized green circuit board icon to the right.The logo for luminovo features a stylized blue circuit board icon to the left of the word "luminovo" in a blue, sans-serif font.The logo for McL features the letters "McL" in a blue, sans-serif font, with "Millennium Circuits Limited" in a smaller, black, sans-serif font below it.The logo for NCAB GROUP features a stylized green circuit board icon to the left of the text "NCAB GROUP" in a bold, black, sans-serif font.The logo for the 25th anniversary features the number "25" in a blue, sans-serif font, with "Celebrating 25 years" in a smaller, blue, sans-serif font below it.

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Flex DfM Guidelines, Part 2

Proper flex PCB outline design, shielding and stiffener placement help improve manufacturability, durability and long-term reliability in demanding applications.

by AKBER ROY

Following [Part 1](#)'s discussion of internal layout and drilling, this section covers the final design considerations needed to prepare a flex PCB for production. It explains how boards are separated from their panels using either high-volume punching or high-precision laser cutting, then examines the use of shielding films, stiffeners and other protective layers. It also outlines key spacing and alignment guidelines that help prevent edge tearing, reduce electromagnetic interference and improve connector durability.

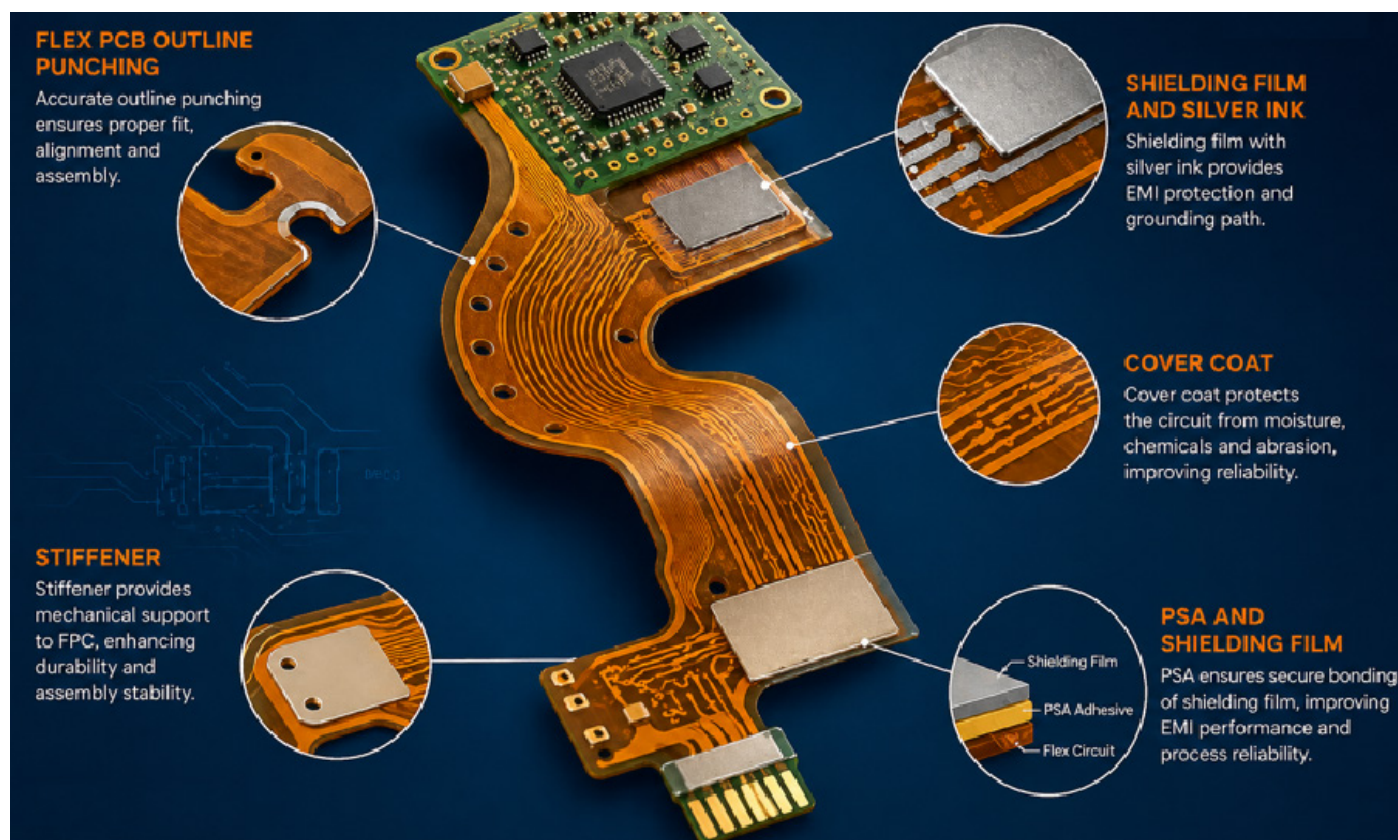


Figure 1. Die punching provides accurate, high-volume separation of flex PCBs when proper tooling hole placement and edge clearances are maintained.

Outline punch. Die punching is typically used in high-volume FPC production. Accurate tooling hole placement ensures alignment during punching and improves dimensional precision. Board features must maintain safe clearance from board edges to prevent damage during die punching.

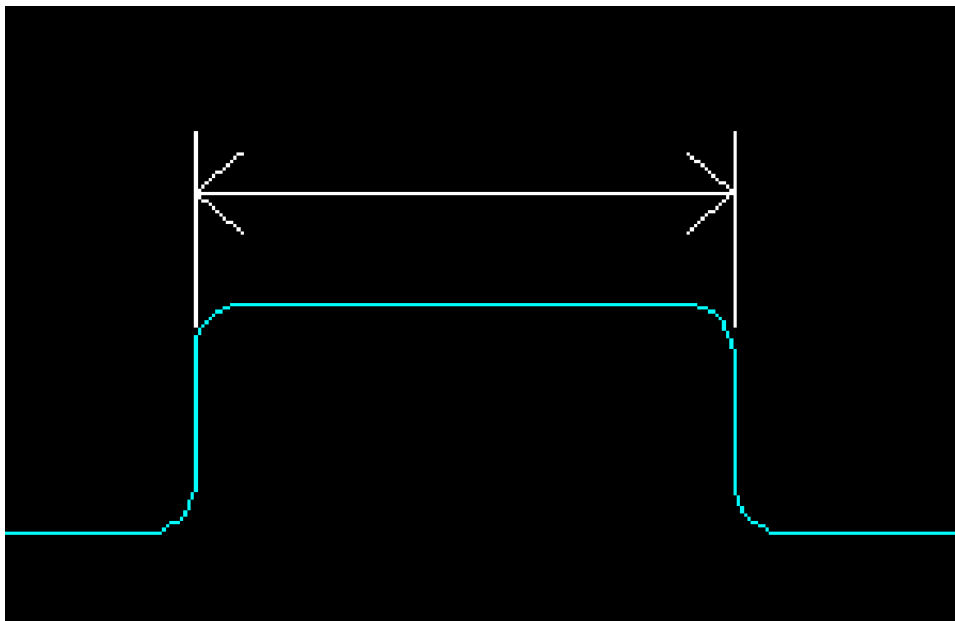


Figure 2. Board outline tolerances help ensure dimensional accuracy and proper fit for punched flex PCBs.

Outline tolerance. For flex PCBs manufactured by punching, the board outline tolerance is $\pm 0.10\text{mm}$ (standard) and can be improved to $\pm 0.075\text{mm}$ with special process control, ensuring accurate dimensional conformity.

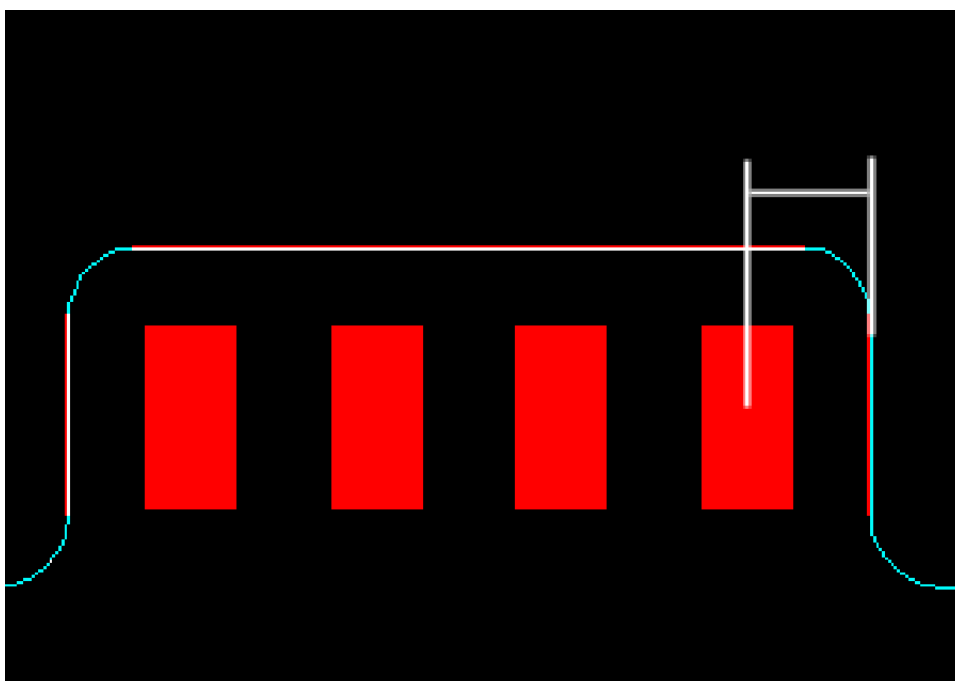


Figure 3. Maintaining ZIF pad-to-outline tolerance is critical for reliable connector alignment and electrical performance.

ZIF pad-to-outline tolerance. The tolerance from the ZIF pad center to the board edge in a punched flex PCB is $\pm 0.1\text{mm}$ (standard) and can be tightened to $\pm 0.075\text{mm}$ with special process control to ensure proper connector alignment. If this tolerance is not maintained, the ZIF contacts may not align properly with the connector terminals, resulting in poor electrical contact, intermittent signals or assembly failure.

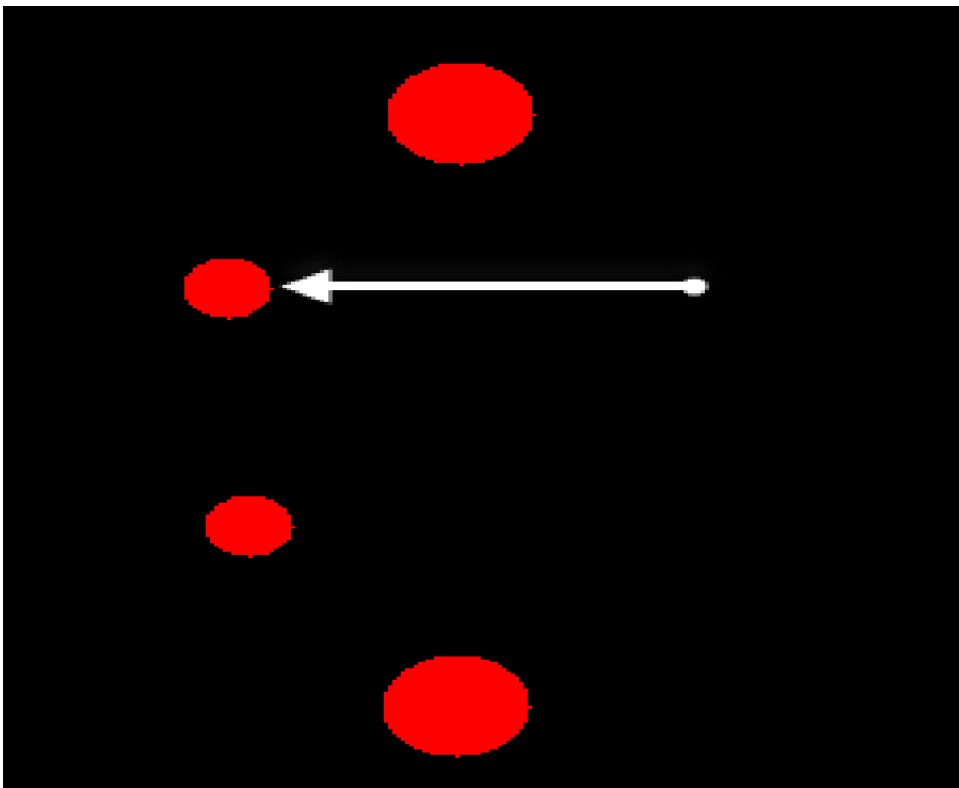


Figure 4. Minimum punch hole diameters help prevent material tearing and dimensional defects during fabrication.

Min cut-out (punch hole diameter). In the punching process for flex PCBs, the minimum cut-out or hole diameter is 0.55mm (standard) and can be reduced to 0.4mm with special tooling capability.

If the hole size is smaller than the specified limit, it may result in incomplete punching, material tearing, or deformation of the flexible substrate, which can affect dimensional accuracy and mechanical reliability.

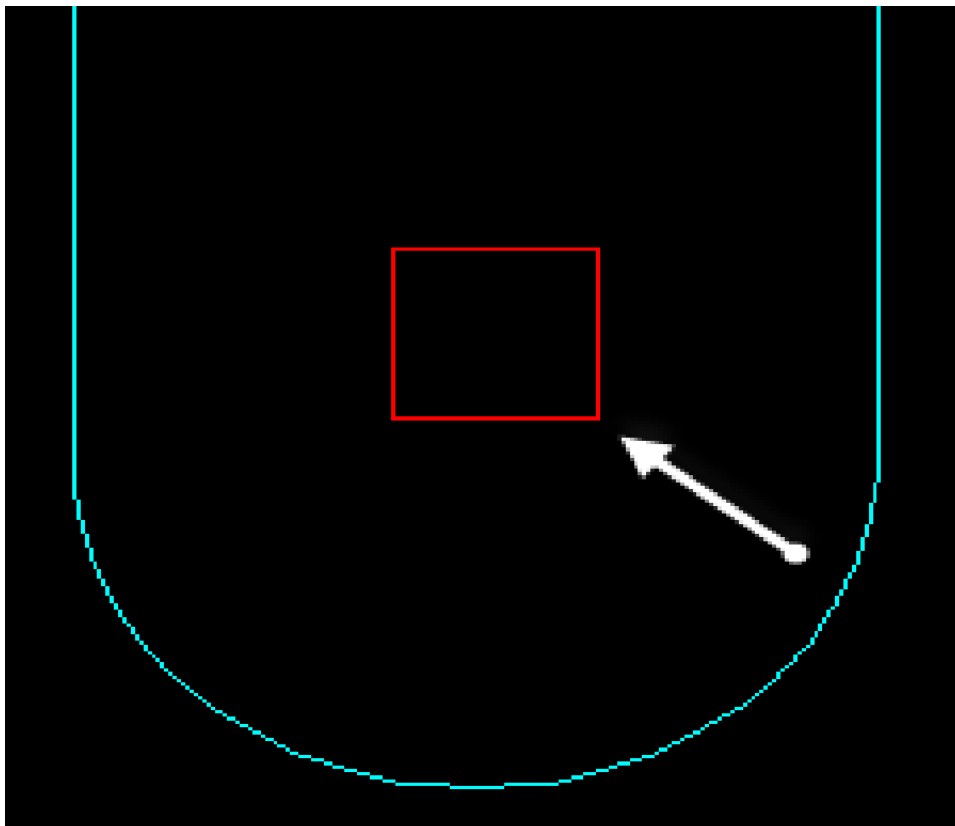


Figure 5. Square cut-out dimensions should meet manufacturing limits to ensure clean punching and reliable board quality.

Minimum cut-out (square). For flex PCBs manufactured by punching, the minimum punch cut-out size is $0.7 \times 0.7\text{mm}$ under standard capability, and special process control allows it to be reduced to $0.6 \times 0.6\text{mm}$. Designing cut-outs smaller than these limits may lead to incomplete punching or material deformation, which can compromise dimensional accuracy and overall reliability of the flexible circuit.

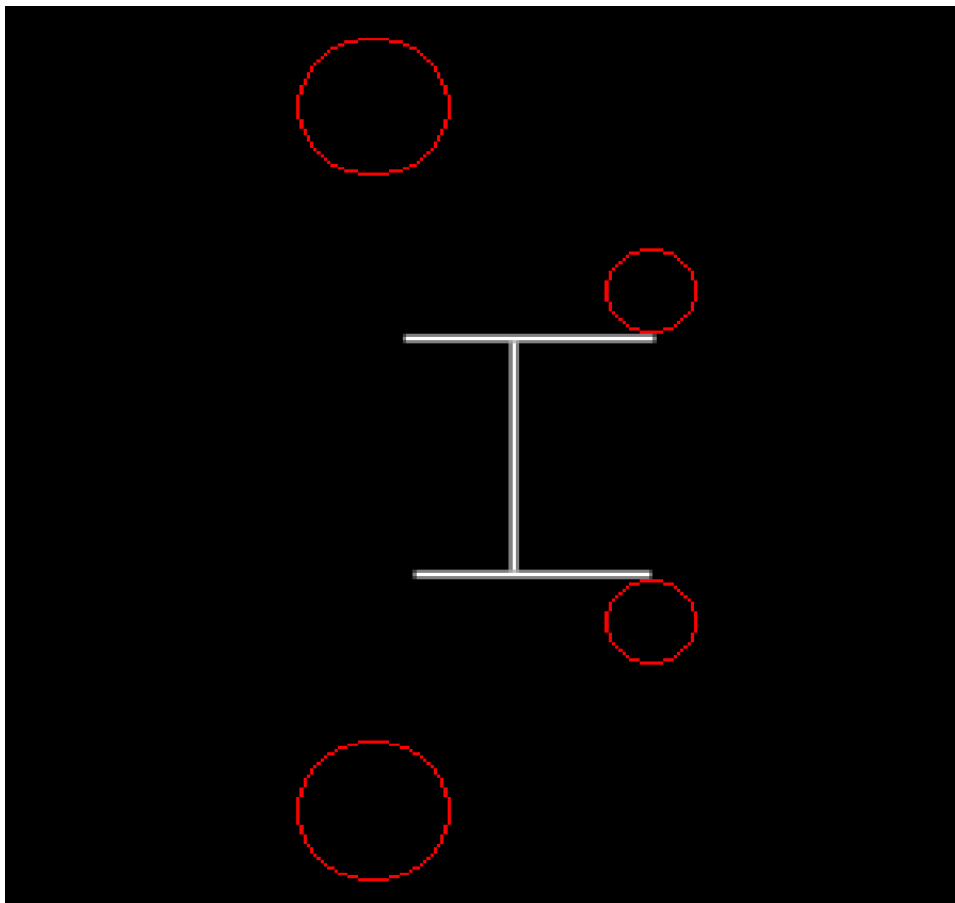


Figure 6. Proper spacing between punched holes reduces the risk of deformation and improves manufacturing stability.

Min punch hole edge to hole edge. For flex PCBs manufactured by punching, the minimum punch cut-out size is $0.7 \times 0.7\text{mm}$ under standard manufacturing capability, while special process control allows it to be reduced to $0.6 \times 0.6\text{mm}$.

However, the current design does not comply with the specified DfM specification, posing a risk of manufacturing instability and potential deformation or edge-quality issues during punching.

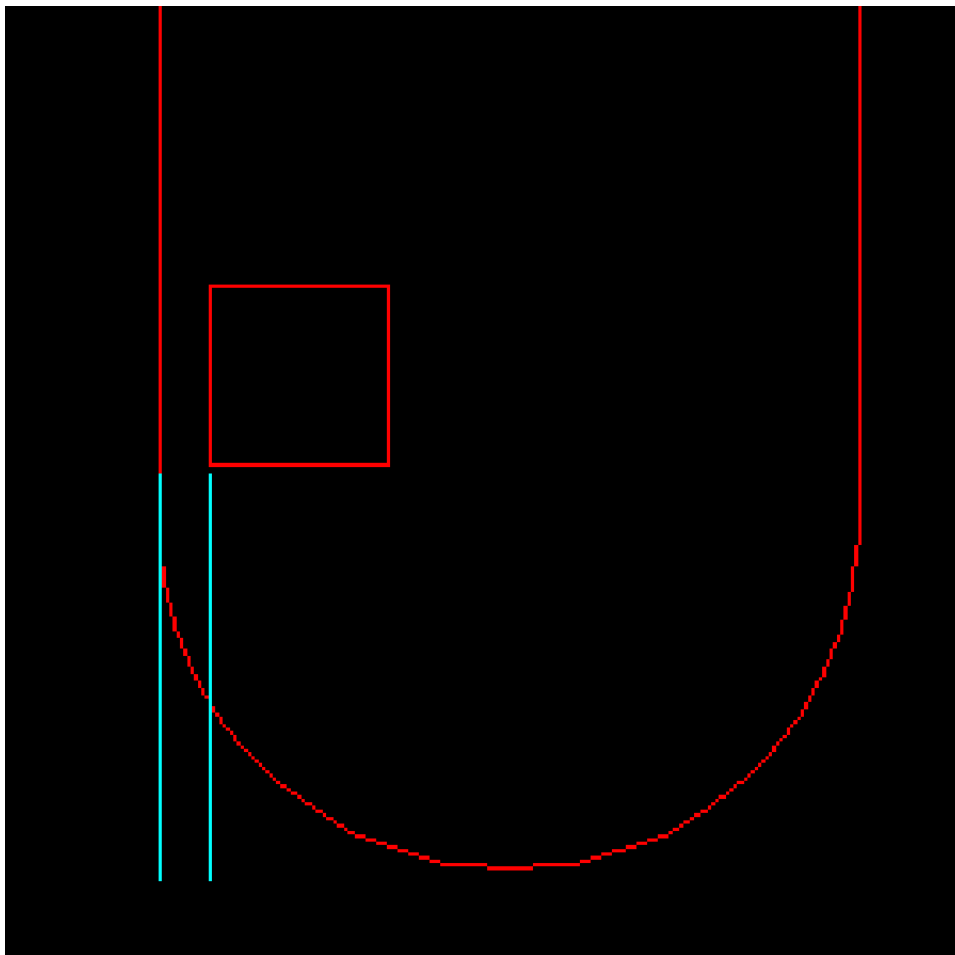


Figure 7. Adequate clearance between punched holes and the board edge helps prevent cracking and delamination.

Punch hole edge to outline distance. The minimum distance from the punched hole edge to the PCB outline must be $0.4 \text{ mm} \pm 0.1 \text{ mm}$ (standard) or $0.3 \text{ mm} \pm 0.05 \text{ mm}$ (special) to ensure adequate mechanical strength of the flex PCB during punching and handling.

If the hole is placed too close to the outline, it may cause edge tearing, cracking, or delamination of the flex material during punching.

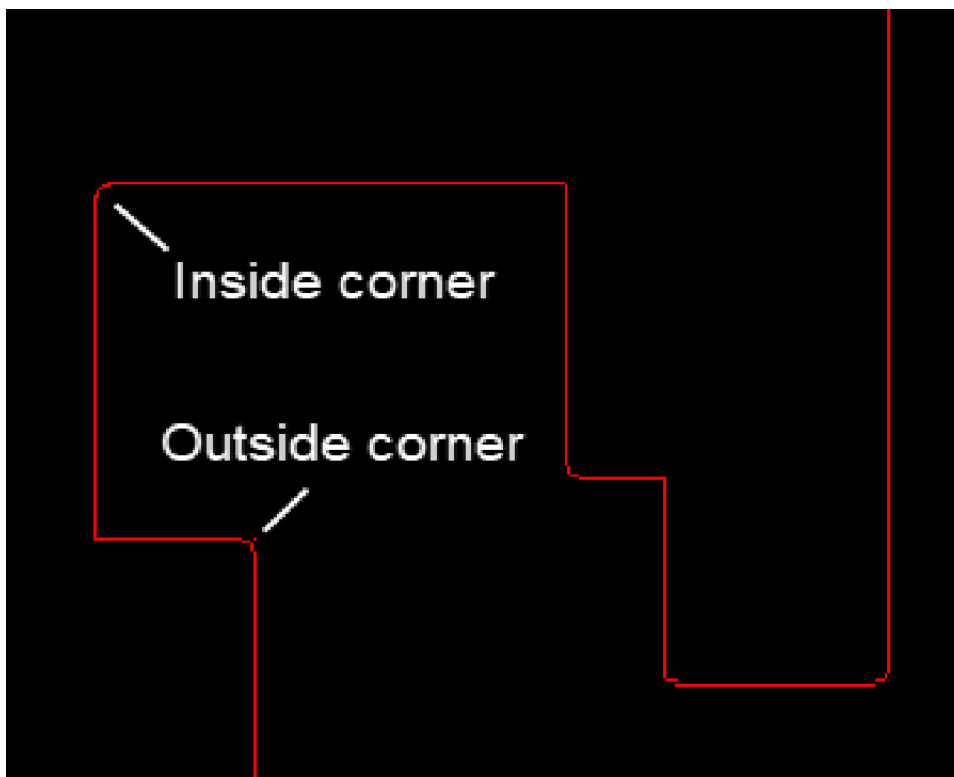


Figure 8. Minimum inside and outside corner radii reduce stress concentrations and improve flex PCB durability.

Minimum inside and outside corner radius. The minimum inside and outside corner radius should be 0.2mm (standard) or 0.1mm (special) to support reliable punching and reduce stress concentration in the flex PCB outline. This radius helps maintain manufacturability and mechanical stability during handling and flexing. If the corner radius is smaller than the specified 0.2mm / 0.1mm, sharp corners may form, increasing stress in the material. This can lead to tearing, cracking, dimensional inaccuracies, or reduced durability of the flex PCB during manufacturing and use.

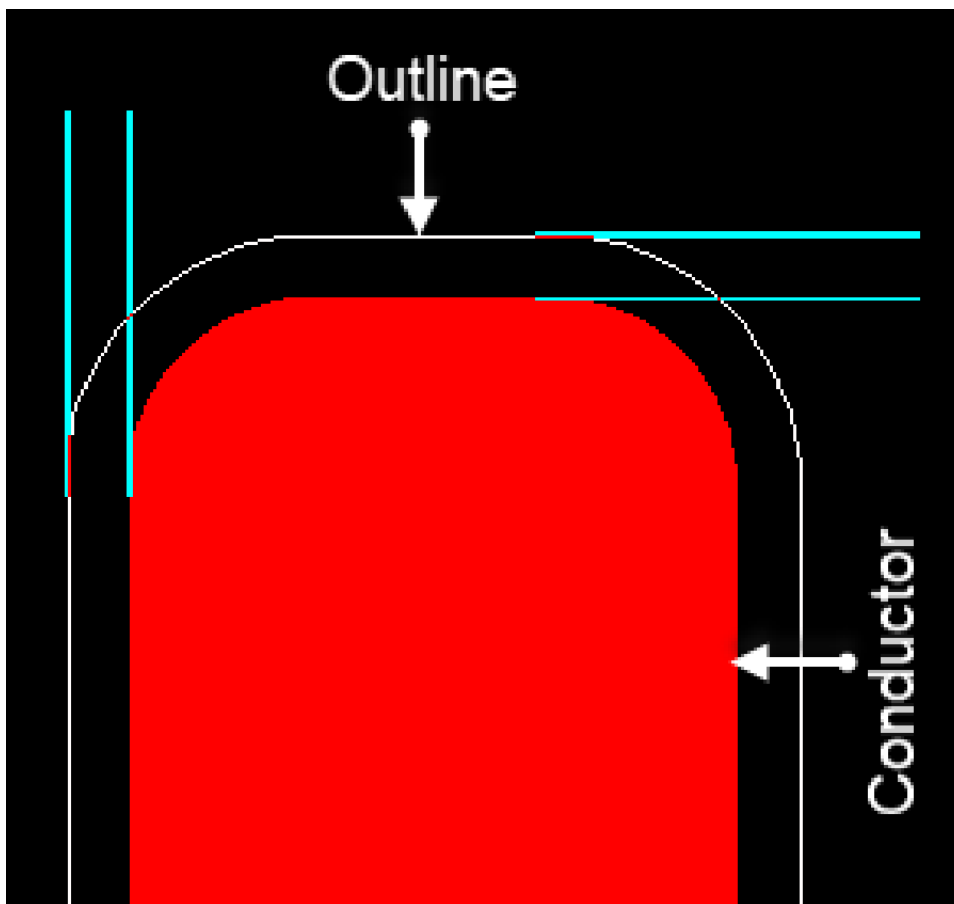


Figure 9. Keeping copper features away from the board outline protects conductive traces during punching.

Outline to all conductive surfaces. The minimum distance from the punch outline to any conductive (copper) surface should be 0.2mm (standard) or 0.15mm (special) to ensure safe separation during punching. This clearance protects copper traces from mechanical damage and maintains electrical integrity.

If the copper features are placed closer than 0.2mm / 0.15mm to the outline, punching may damage or expose the copper traces. This can result in trace breakage, shorts, or reliability failures during manufacturing or product operation.

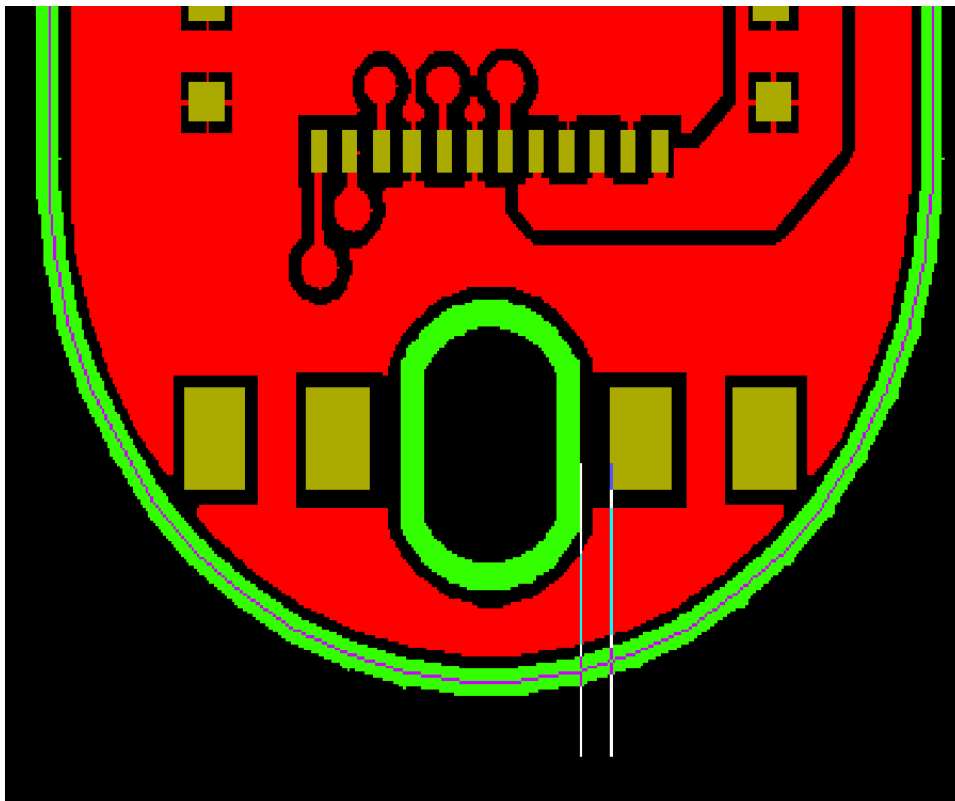


Figure 10. Minimum spacing between punch holes and nearby copper features helps preserve electrical integrity.

Minimum punch hole edge to copper feature spacing. The minimum spacing from the punch hole edge to conductive features should be 0.3mm (standard) or 0.25mm (special) to protect nearby copper during punching and maintain electrical integrity.

If this spacing is not maintained, punching may damage or deform traces, leading to opens, shorts or reliability issues.

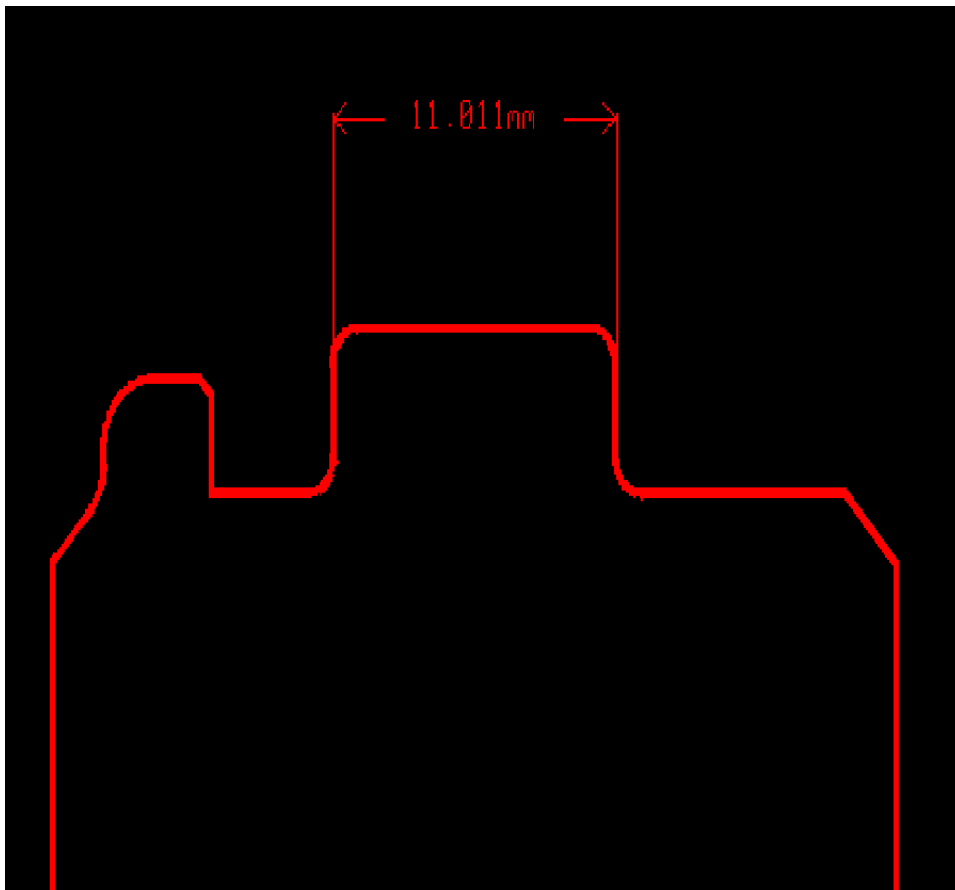


Figure 11. Laser cutting provides tight outline tolerances for complex flex PCB geometries and low-volume production.

Outline Tolerance (Laser). Laser cutting is well-suited to complex geometries and low-volume production, offering high precision and easy design adjustments. Like any process, however, it introduces some dimensional variation. Outline tolerance specifies the acceptable difference between the designed and actual cut profile of a flex PCB to ensure proper assembly fit. We offer a standard $\pm 0.05\text{mm}$ tolerance, which suits most designs, while a $\pm 0.025\text{mm}$ tolerance is used for high-precision needs. Maintaining tight control is essential in flex PCBs to ensure alignment, minimize mechanical stress and achieve reliable performance in compact, flexible designs.

Shielding Film and Silver Ink

Shielding films and silver ink are used in flex PCBs for EMI protection, grounding and signal shielding in high-density circuits.

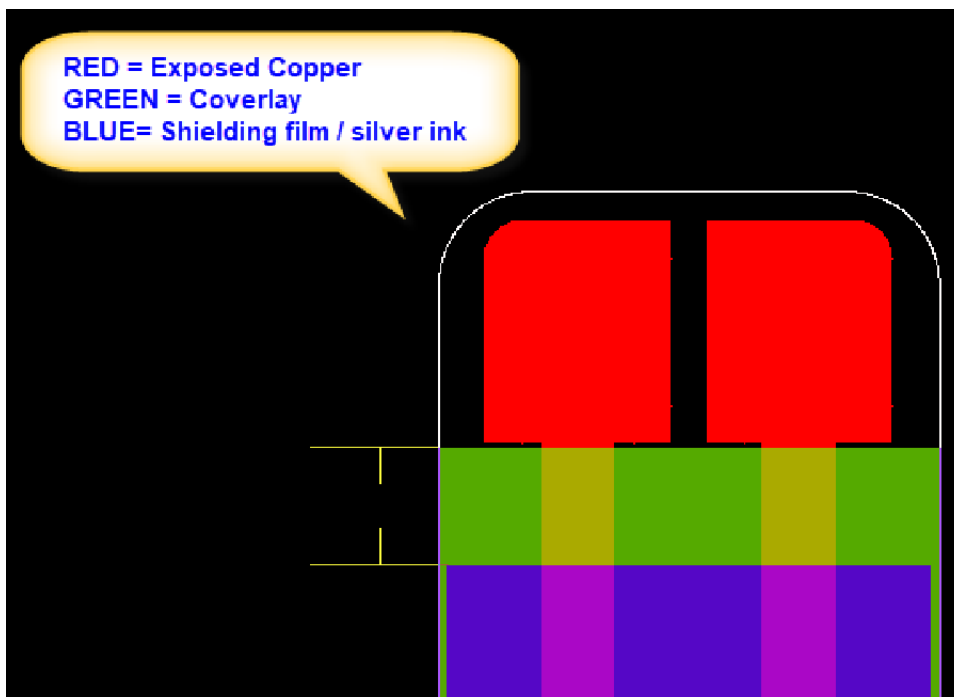


Figure 12. Proper clearance between shielding film or silver ink and exposed surfaces helps prevent shorts and signal leakage.

Minimum shielding film / silver ink to exposed surface. From a CAM perspective, maintaining a minimum clearance of 0.5mm (standard) or 0.4mm (special) from exposed surfaces is essential to prevent conductive overlap. If this spacing is violated, silver ink may bleed or migrate onto exposed pads, causing shorts or signal leakage. To control this risk, designs must account for material spread, registration tolerance and flex-induced movement, especially in dynamic bend regions.

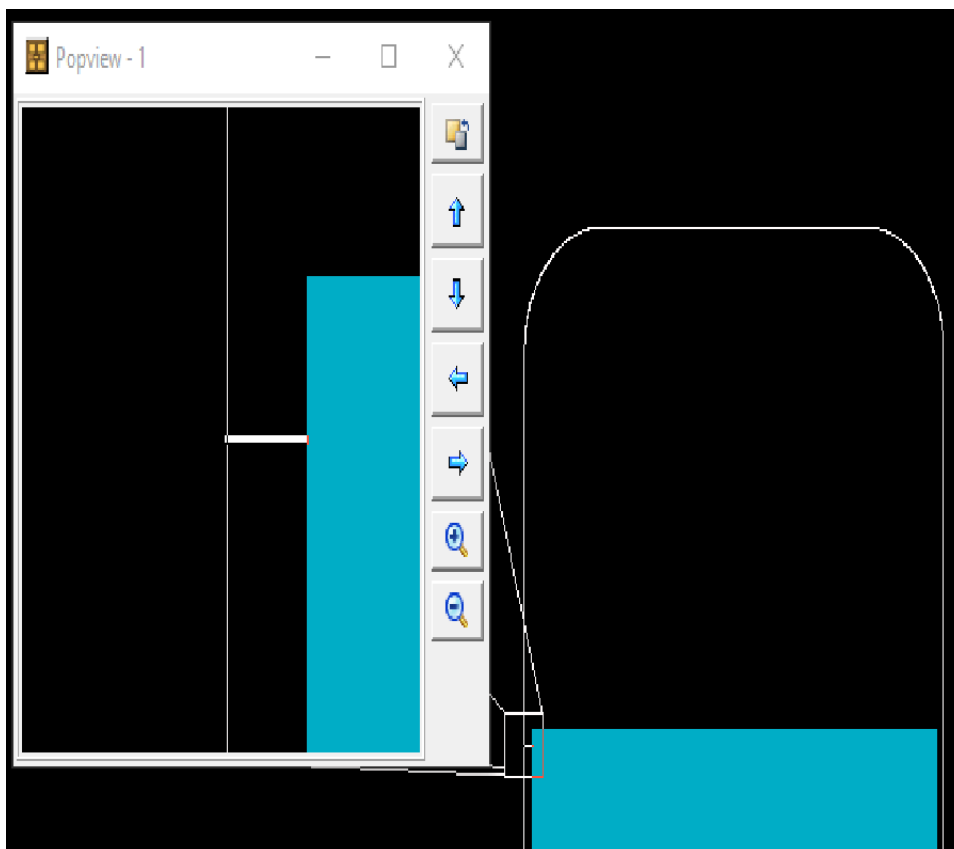


Figure 13. Maintaining adequate setback between silver ink and the board edge improves long-term mechanical and electrical reliability.

Minimum distance between silver ink and outline. Silver ink is commonly applied for shielding and grounding, but it must be kept at a safe distance from the PCB outline to ensure structural and electrical reliability. A minimum spacing of 0.5mm (standard) or 0.4mm (special) helps prevent exposure of conductive ink after laser cutting. If placed too close, edge cracking, peeling or delamination can occur due to mechanical stress during cutting or flexing. The solution is to maintain proper setback in design and include process tolerances to protect the ink layer and ensure long-term performance.

Cover Coat, Stiffener, PSA and Shielding Film

Cover coat, stiffener, PSA (pressure-sensitive adhesive) and shielding film are essential materials used in PCB and flexible circuit assemblies. They enhance mechanical strength, provide insulation, enable secure bonding, and protect circuits from electromagnetic interference (EMI). Together, these layers improve durability, reliability and overall performance of electronic components in demanding applications.

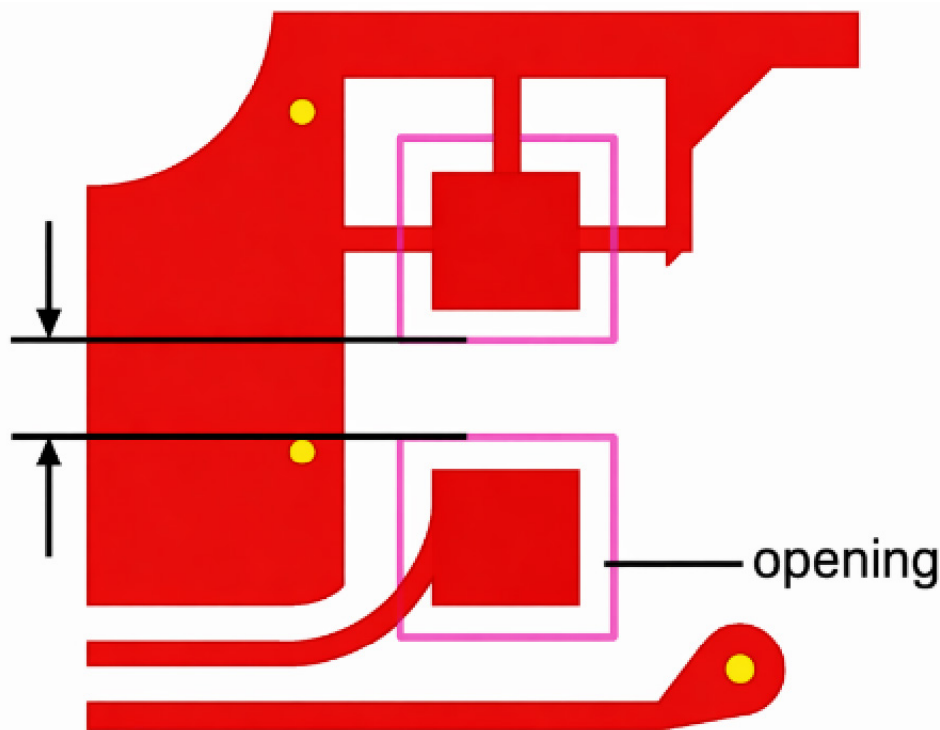


Figure 14. Coverlay dam widths and layer registration tolerances are essential for solderability, insulation and manufacturing yield.

Minimum coverlay dam. From a CAM perspective, maintaining the dam width of 0.3mm (standard) or 0.25 mm (special) for coverlay and 0.075mm (standard) or 0.0635mm (special) for LPI solder mask helps ensure proper isolation between pads and prevents solder bridging during assembly. It also allows stable registration between copper and protective layers during fabrication. Insufficient dam can lead to solder bridging, short circuits, mask/coverlay misregistration, and reduced yield due to open/short defects.

Minimum tolerance of registration. This defines the allowable misalignment between layers (coverlay, solder mask, stiffener, PSA, shielding film) and copper features. CAM accounts for process shifts and material movement to keep features within tolerance. Misregistration can expose copper, partially cover pads, cause poor solderability, or misplace stiffeners, leading to assembly failures and functional defects. The following is what we suggest and consider during analysis and processes:

- **Coverlay:** $\pm 0.2\text{mm}$ (standard) or $\pm 0.15\text{mm}$ (special)
- **Solder mask:** $\pm 0.05\text{mm}$ (standard) or $\pm 0.038\text{mm}$ (special)
- **Stiffener/PSA/Shielding film:** $\pm 0.2\text{mm}$ (standard) or $\pm 0.15\text{mm}$ (special)

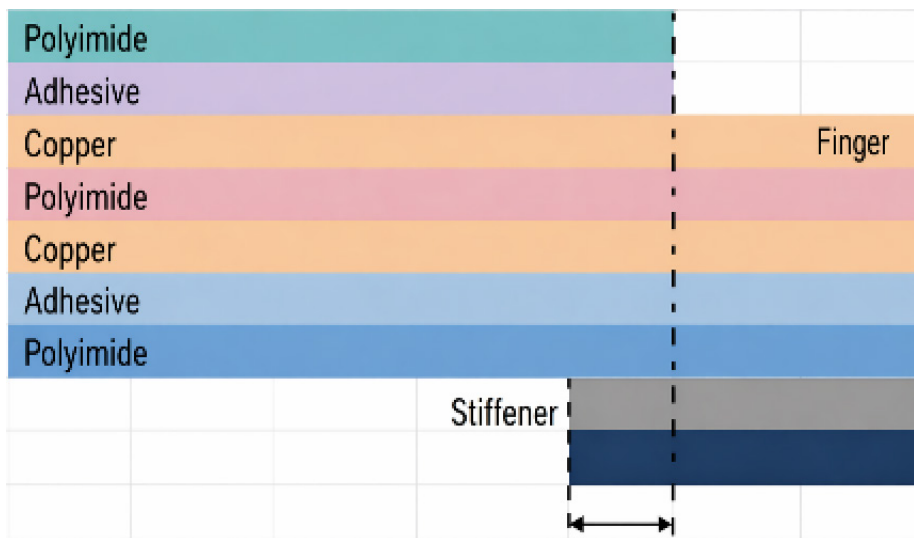


Figure 15. Proper stiffener overlap with the ZIF finger region reinforces the connector area and reduces flex-induced failures.

Distance between stiffener and finger. The requirement to ensure a minimum overlap of 0.5mm between the stiffener and the ZIF finger region on opposite sides of the flex PCB is critical for providing mechanical reinforcement at the transition zone where the flexible circuit interfaces with the connector, thereby reducing localized bending stress. Proper overlap helps to distribute stress more evenly during insertion, removal, and repeated flexing. If sufficient overlap is not maintained, a stress concentration can form at the stiffener edge, leading to crack initiation in the copper or base material. Over time, this can result in trace fractures, intermittent electrical failure, or complete open circuits, especially in dynamic or high-cycle flex applications. 

AKBER ROY is CEO and founder of Rush PCB in Silicon Valley (Milpitas), California, www.RushPCB.com. Contact the author at sales@rushpcb.com.



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PCB Designers Earn More, Do More: The 2026 Compensation Picture

The 2026 PCD&F Salary Survey examines compensation, workloads, career satisfaction and the evolving role of PCB designers across the electronics industry.

by RYANN HOWARD

If your paycheck reflects how your employer sees you, printed circuit board designers are looking pretty good right now.

A decade ago, the percentage of designers who made six figure salaries was low; those who pulled in \$150,000 or more were basically nil. Fast forward to today, however, and compensation once reserved for certain engineers is now becoming widespread among layout personnel.

That's according to the 2026 *PCD&F* Salary Survey, which found many respondents earning salaries well into six figures. A notable share now earns more than \$150,000 annually, reflecting the value employers continue to place on experienced design talent.

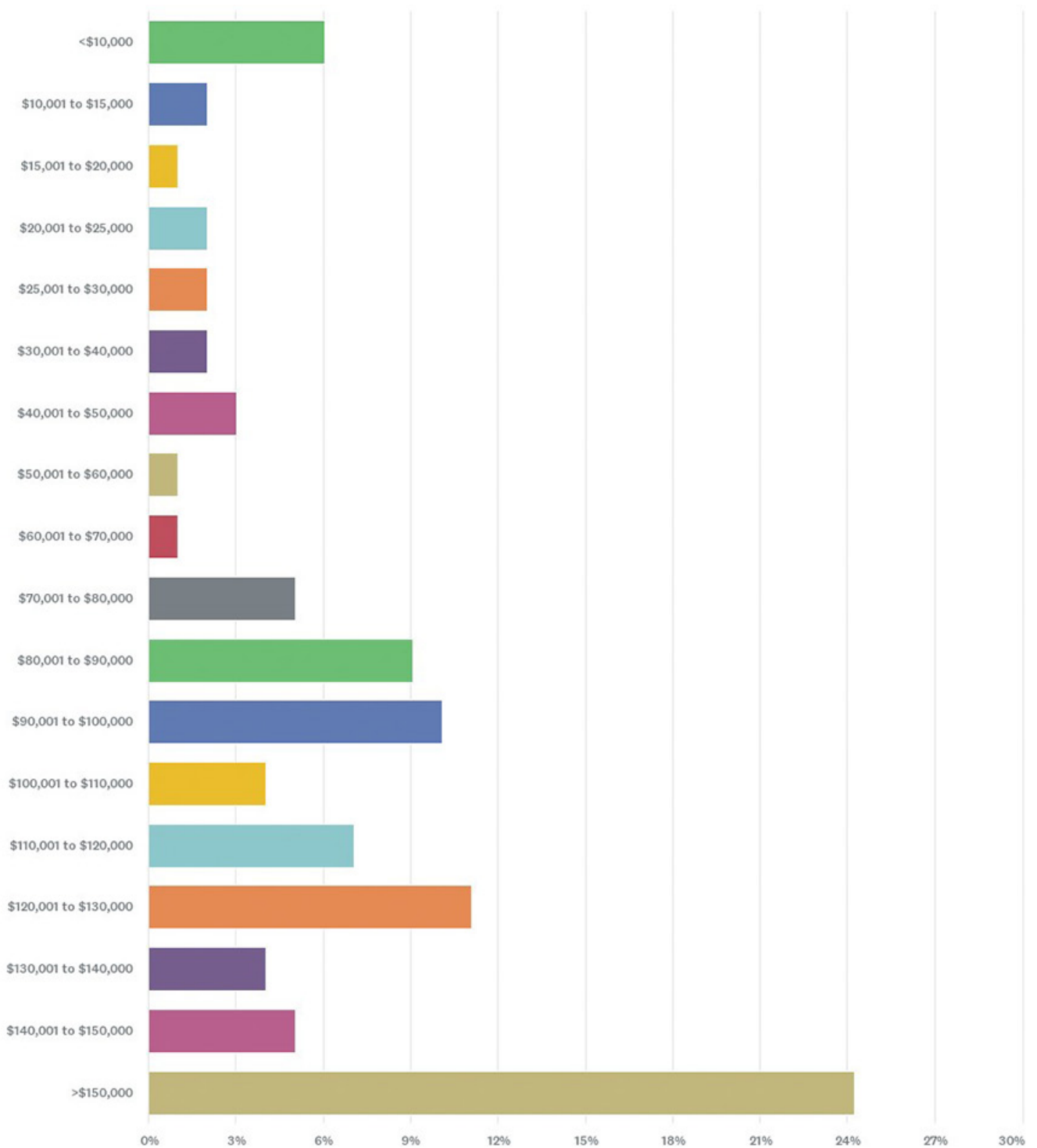


Figure 1. Respondents by annual salary.

And salaries continued to climb in the past year. The overwhelming majority of respondents received a salary increase, with raises most commonly falling in the 1% to 6% range, but a select number saw raises exceeding 10%. Only a handful experienced salary reductions. (The survey does not account for job changes, which may explain some of the changes.)

How has your salary changed in the past year?

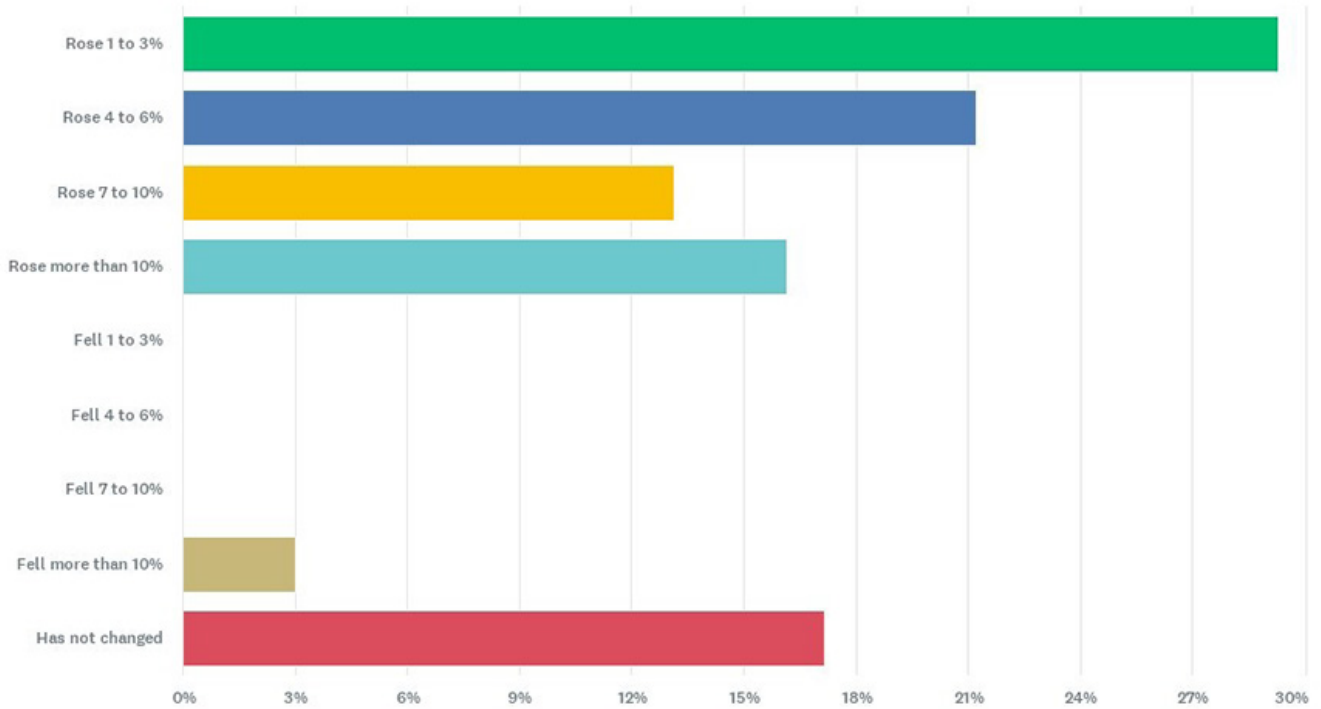


Figure 2. Respondents by salary change over the past year.

The longer-term change is even more striking. In 2016, the median salary for PCB designers fell in the \$80,000 to \$90,000 range, with about one in five respondents earning more than \$110,000. Ten years later, the median has moved into the \$110,000 to \$120,000 range.

Based on the midpoint of those ranges, that represents an increase to \$115,000 from roughly \$85,000, or about 35%, since 2017. And the upper end has become far less exceptional: in 2026, 24% of respondents earn more than \$150,000, compared with just 4% in 2016. The shift reinforces just how dramatically compensation for experienced PCB design talent has moved upward over the past decade.

The data are derived from a survey conducted by PCEA during summer 2026, in which a questionnaire was distributed to a self-selected population. Respondents were directed to answer questions related to job titles and functions, ages, years of experience, education, location, types of projects, annual salaries and sales, job satisfaction and challenges, ECAD tools used, and years left in the field. In these types of surveys, respondents are not necessarily representative of the entire population, and the findings may not accurately reflect the broader population.

PCB Designer Median Salary Range, 2017 vs. 2026

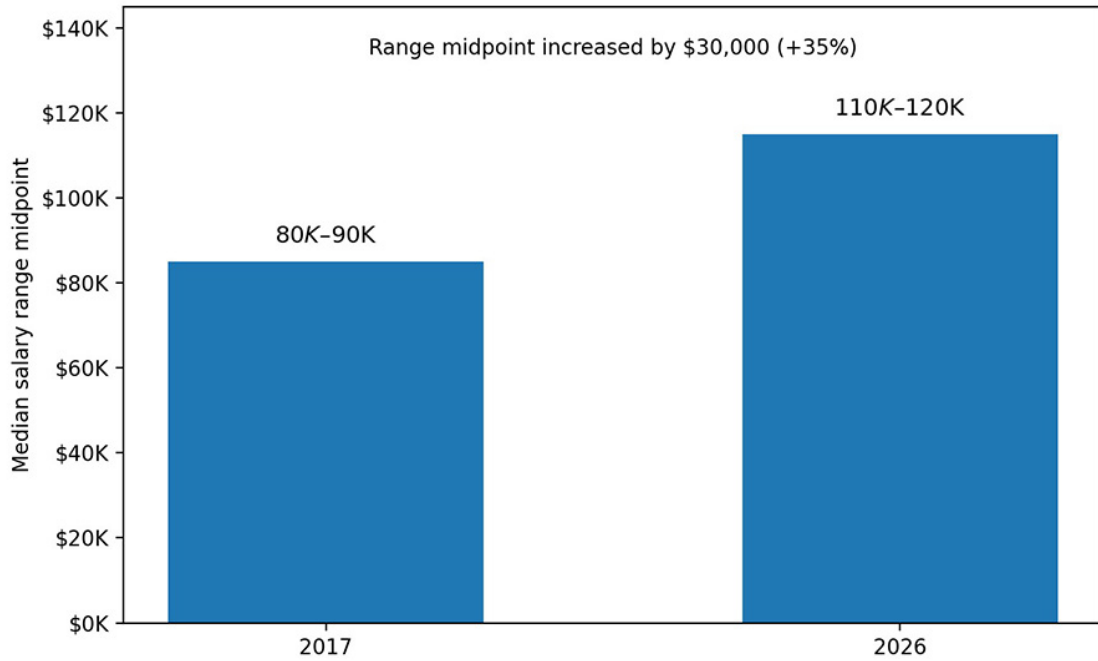


Figure 3. Salary data comparison between 2017 and 2026.

But salary figures alone tell only part of the compensation story. The type of work designers perform, the technologies they handle and the experience they bring to the job provide important context for what employers are willing to pay.

Experience pays. Survey respondents represent every stage of a design career, but seasoned professionals continue to make up the largest share of participants. Many hold senior-level titles, including senior PCB designer, senior PCB design engineer, principal engineer and PCB design manager. Most also continue to spend the majority of their time performing hands-on engineering and layout work rather than managing others.

Which best describes your job title?

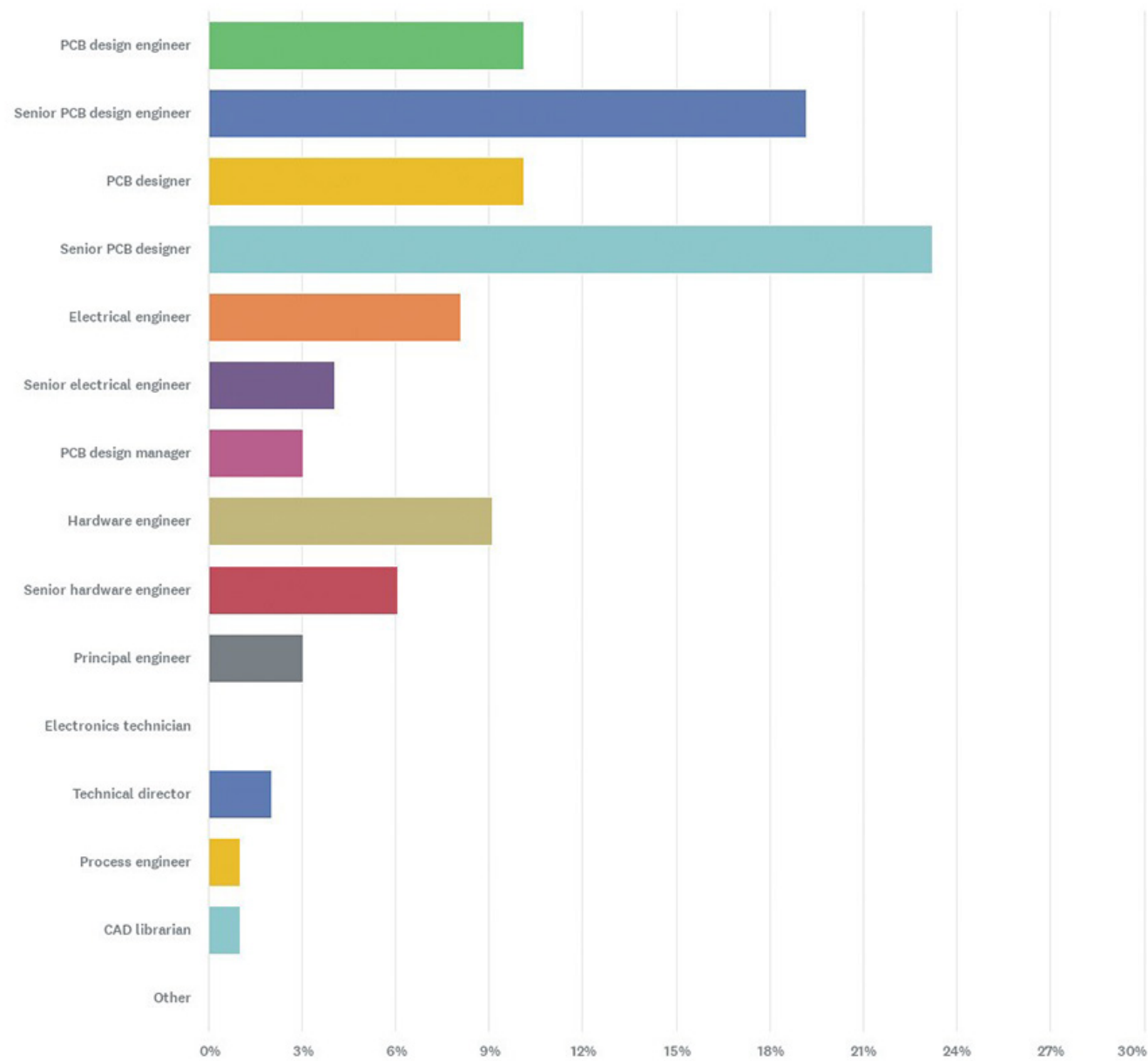


Figure 4. Respondents by job title.

That experience accompanies increasingly sophisticated design work. High-speed designs are now commonplace among respondents, along with HDI structures, RF and microwave circuitry and flex and rigid-flex boards. More than half work on designs containing 12 or more layers, while advanced packaging technologies, embedded systems and optoelectronics further broaden the technical demands placed on today’s designers.

What types of projects and/or technologies do you directly engineer, design or lay out? (Check all that apply.)

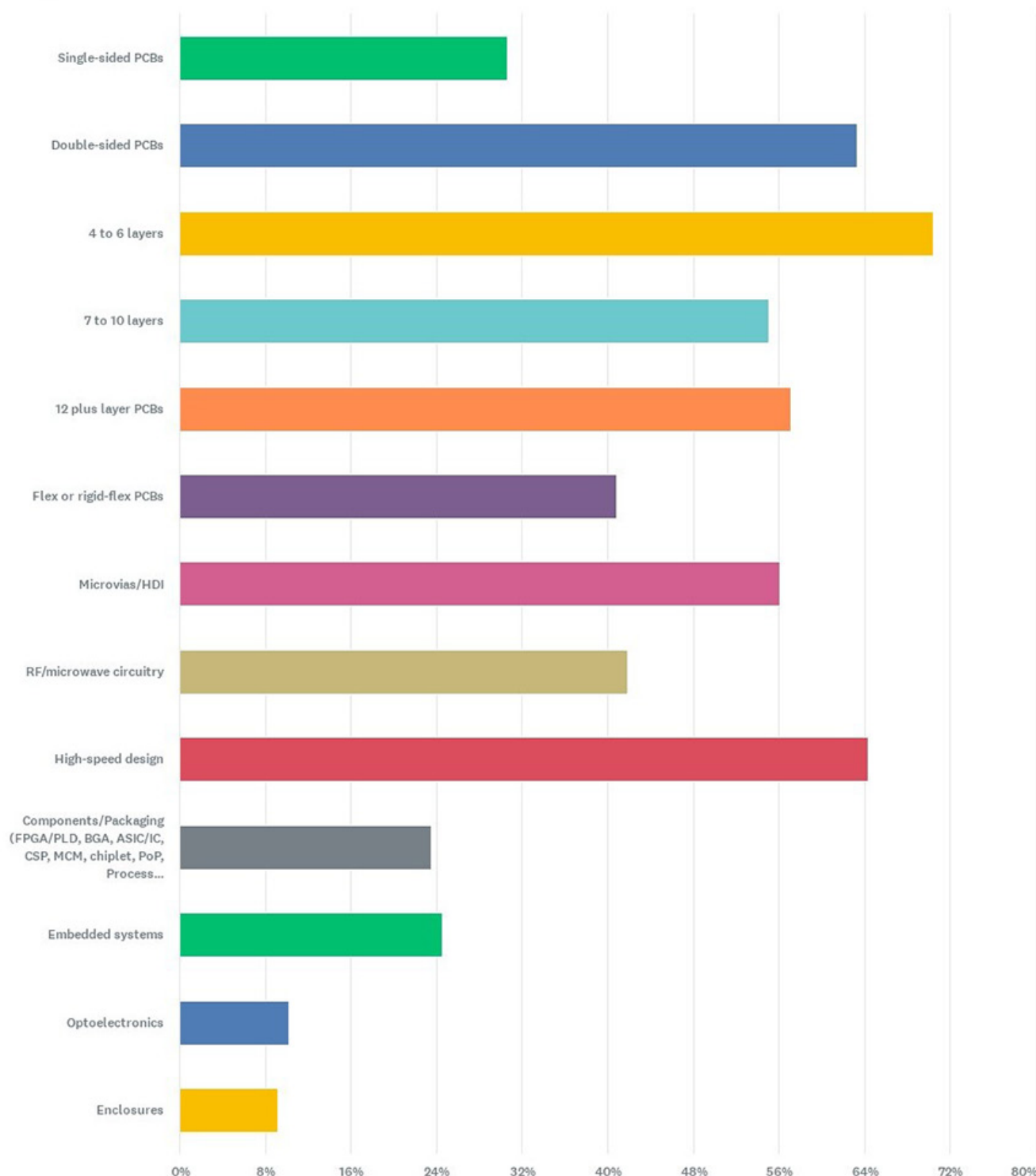


Figure 5. Respondents by type of project.

Those findings provide useful context for the salary numbers. PCB designers aren't simply earning more while doing the same work. Many of the professionals commanding higher compensation bring decades of experience to jobs that require them to manage increasingly complex technologies and design requirements.

Design quality offers another measure of that expertise. Most respondents report relatively few board respins each year, and the majority indicate those numbers have remained steady over the past 12 to 18 months. Experienced designers appear to be managing tighter constraints without a corresponding increase in costly redesign cycles.

On average, how many board revisions (respins) do you produce each year?

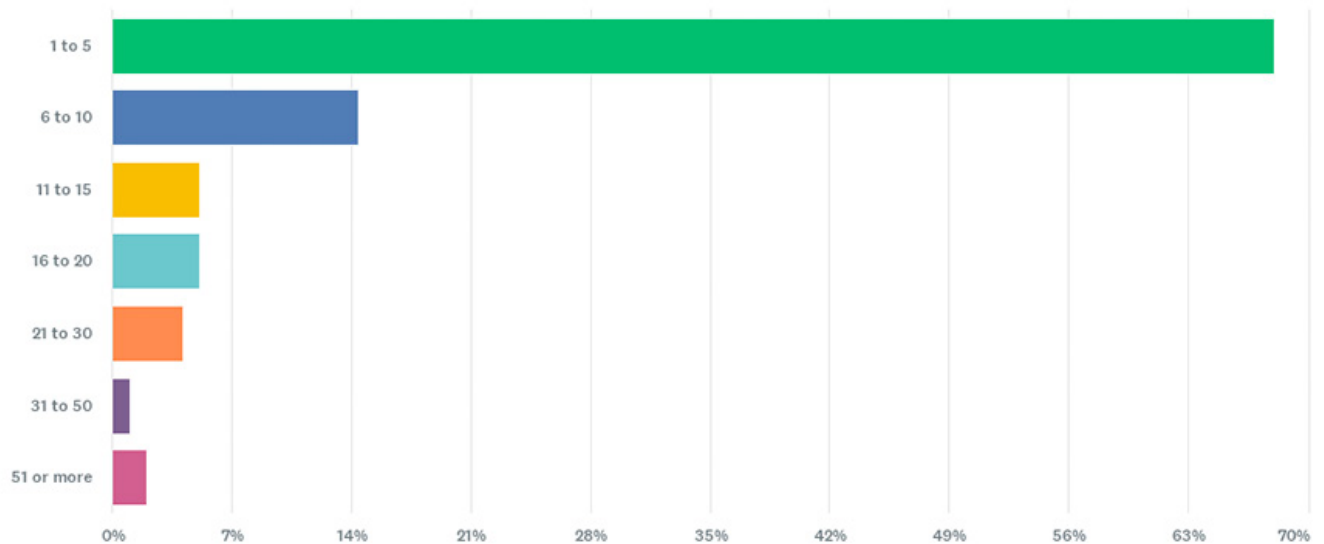


Figure 6. Respondents by respins produced per year.

The job isn't getting easier, however. When asked about their biggest challenges heading into 2026, respondents pointed first to workload, followed closely by keeping pace with rapidly changing technology. Professional development funding ranked well behind those concerns.

What do you think will be the biggest challenge(s) you will face as a designer in 2026? (Check all that apply.)

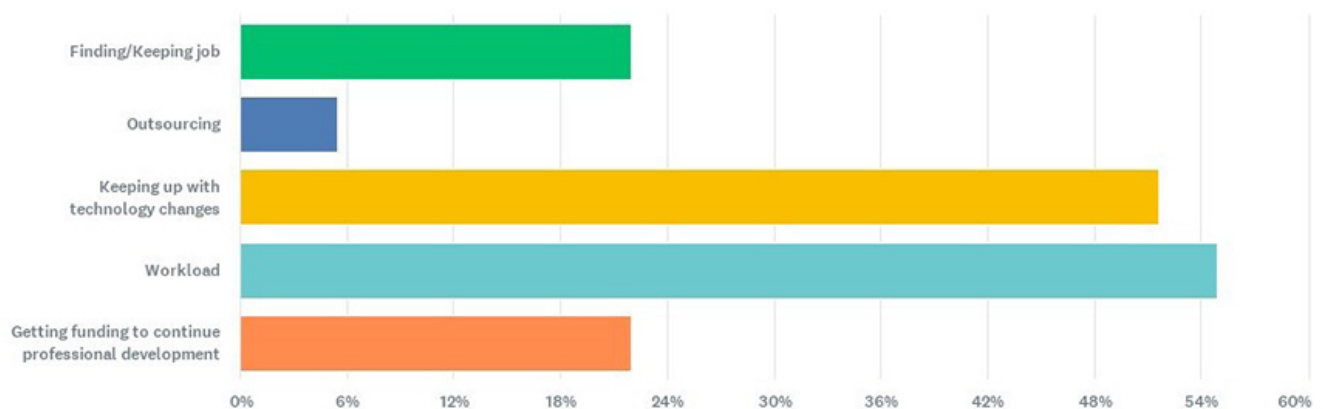


Figure 7. Respondents by biggest challenge(s).

Taken together, the results help explain the compensation picture. Employers are paying for a mature workforce that combines extensive experience with the ability to handle sophisticated designs, maintain quality and keep pace with rapidly evolving technology.

Bonuses remain an important part of total compensation as well. Nearly 70% of respondents indicated they receive an annual bonus, with most falling within the lower single-digit percentage of base salary, while others reported bonus programs exceeding 7%.

If so, what percentage of your current salary is your average annual bonus?

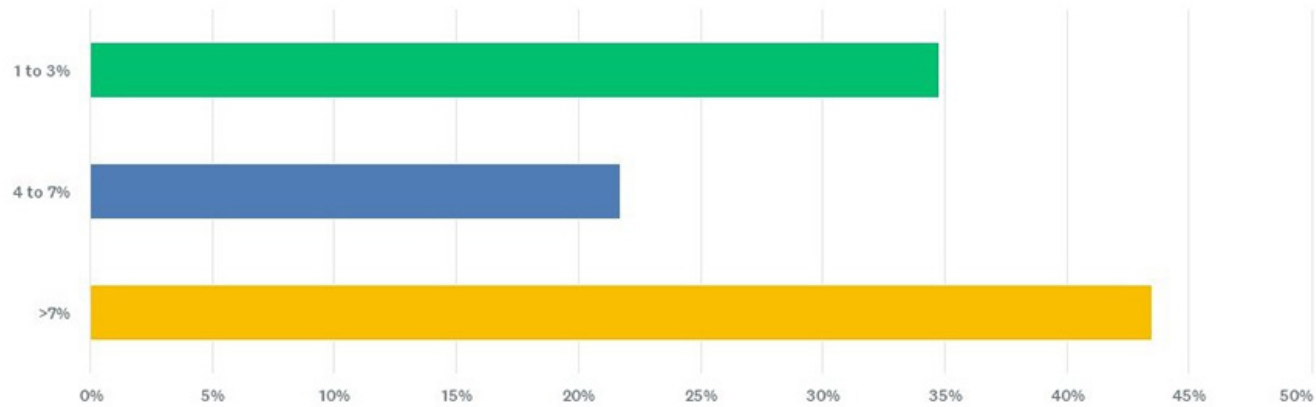


Figure 8. Respondents by percentage of annual bonus.

Education still matters. Education continues to play an important role in the profession, although respondents suggest experience ultimately carries the greatest weight over the course of a career.

Engineering degrees remain the dominant educational background among survey participants, with 51% of respondents holding a bachelor’s in engineering or a related field. Electrical engineering accounts for the largest share of four-year degrees. Another 18% reported holding a master’s degree, while no respondents reported a doctoral degree. When asked how education affects compensation, more than half said it plays either a major or moderate role in determining their salary, including 18% who called it a major factor and 35% who described it as a moderate factor.

What is your highest level of education?

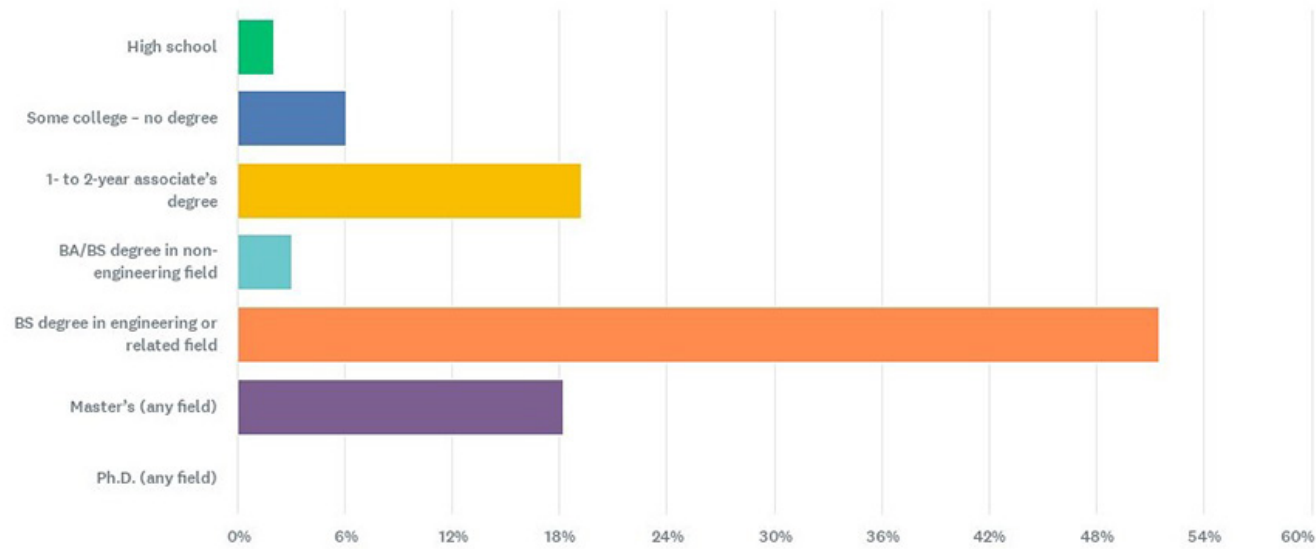


Figure 9. Respondents by highest level of education.

Professional certifications remain another avenue for career development. About 44% of respondents reported holding a design certification. Among certified designers, IPC's CID remains the most common credential, as 35% reported holding CID+ and 18% holding the [PCEA Certified Printed Circuit Designer \(CPCD\)](#) certification.

Asked what has helped them advance professionally, respondents pointed primarily to formal education and networking, followed by personal design portfolios and certifications. The responses suggest career growth depends less on a single credential than on combining technical knowledge with industry relationships and demonstrated design experience.

Investing in growth. Many employers continue to support professional development, although the types of assistance vary considerably.

On-the-job training, conference attendance, mentoring and company-sponsored classes remain among the most common forms of educational support. Tuition reimbursement, industry certification programs and college coursework are also available at some organizations. Many respondents also believe attending conferences and technical classes has had a positive impact on their compensation, reinforcing the value of continued education in an industry where design tools and technologies evolve rapidly.

What educational opportunities are supported by your company? (Check all that apply.)

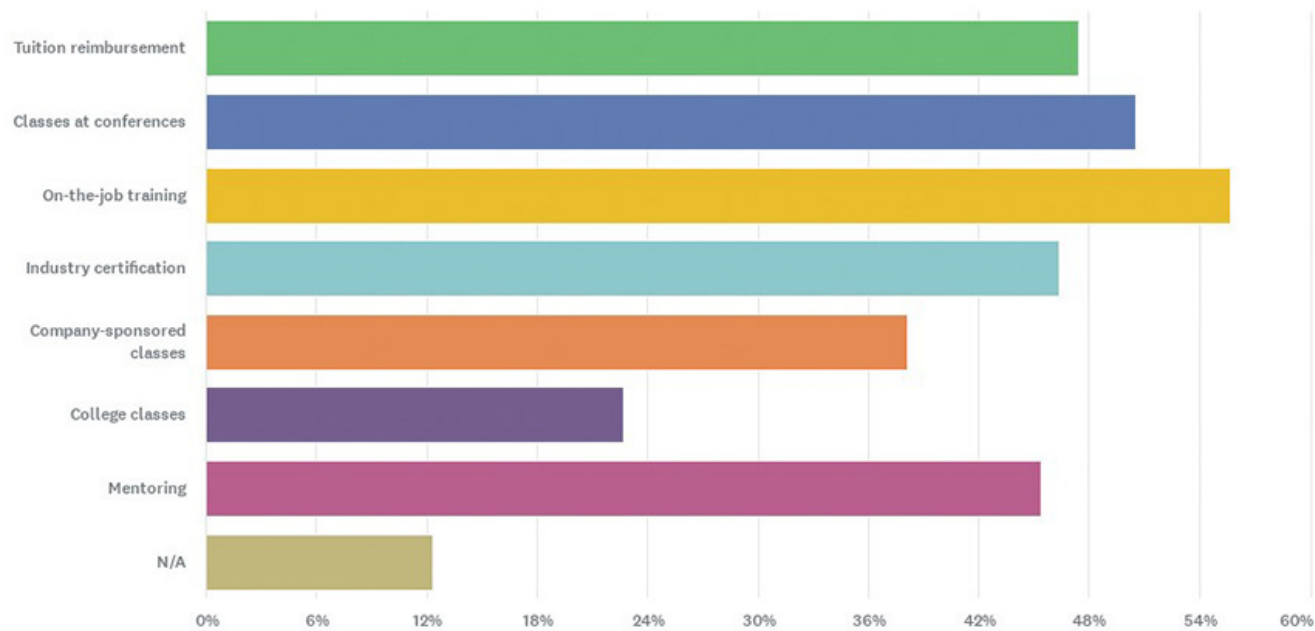


Figure 10. Respondents by educational opportunities.

Where designers work. The survey continues to show PCB design concentrated within large organizations. OEMs remain the dominant employer, followed by design service bureaus, PCB fabricators, EMS providers and consultants. Nearly half of respondents work for companies with more than 1,000 employees worldwide, while many are employed by organizations generating hundreds of millions, or even billions, of dollars in annual revenue.

How many total employees does your company have worldwide?

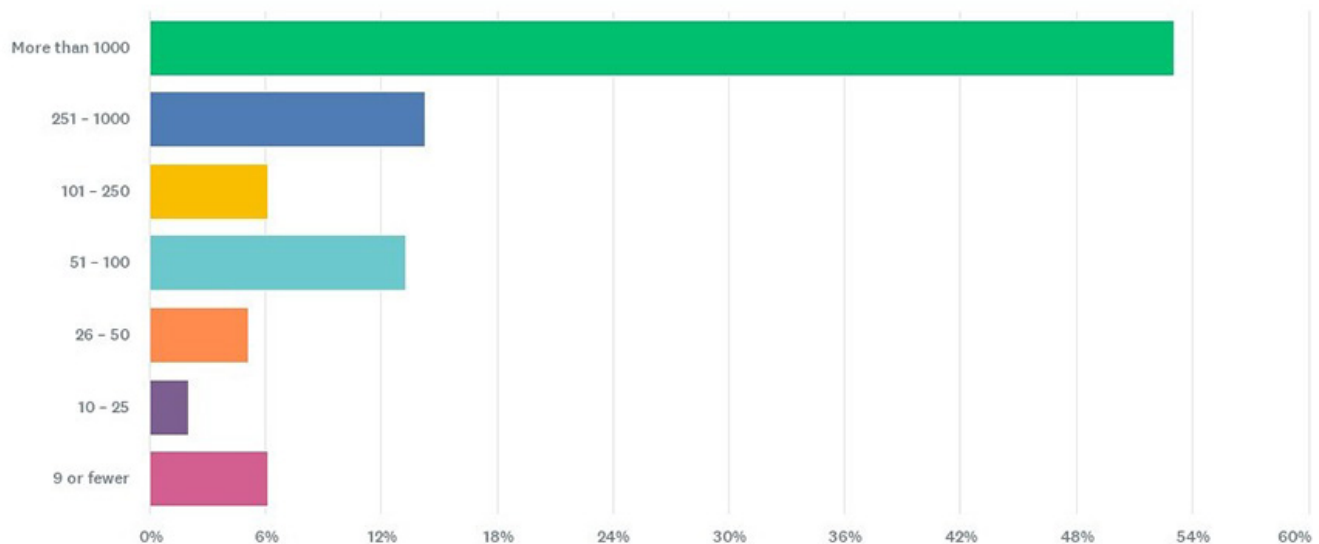


Figure 11. Respondents by total employees at company worldwide.

Government, military, aerospace, avionics and space remain the largest end-market represented in the survey, accounting for nearly one-third of respondents. Consumer electronics, automotive and industrial controls also maintain a significant presence, with communications, medical electronics and semiconductor-related applications rounding out a diverse customer base.

Benefits beyond the paycheck. While salaries remain healthy, benefits continue to play an important role in attracting and retaining talent.

Health insurance, dental coverage and 401(k) plans remain among the most common benefits offered, with many employers also providing life insurance, pension or retirement plans, telecommuting options and profit-sharing programs. Yet not all respondents saw improvements over the past year. Many indicated their benefits either remained unchanged or became more expensive, highlighting the ongoing pressure rising healthcare and benefit costs continue to place on employers and employees alike.

What benefits are offered by your company? (Check all that apply.)

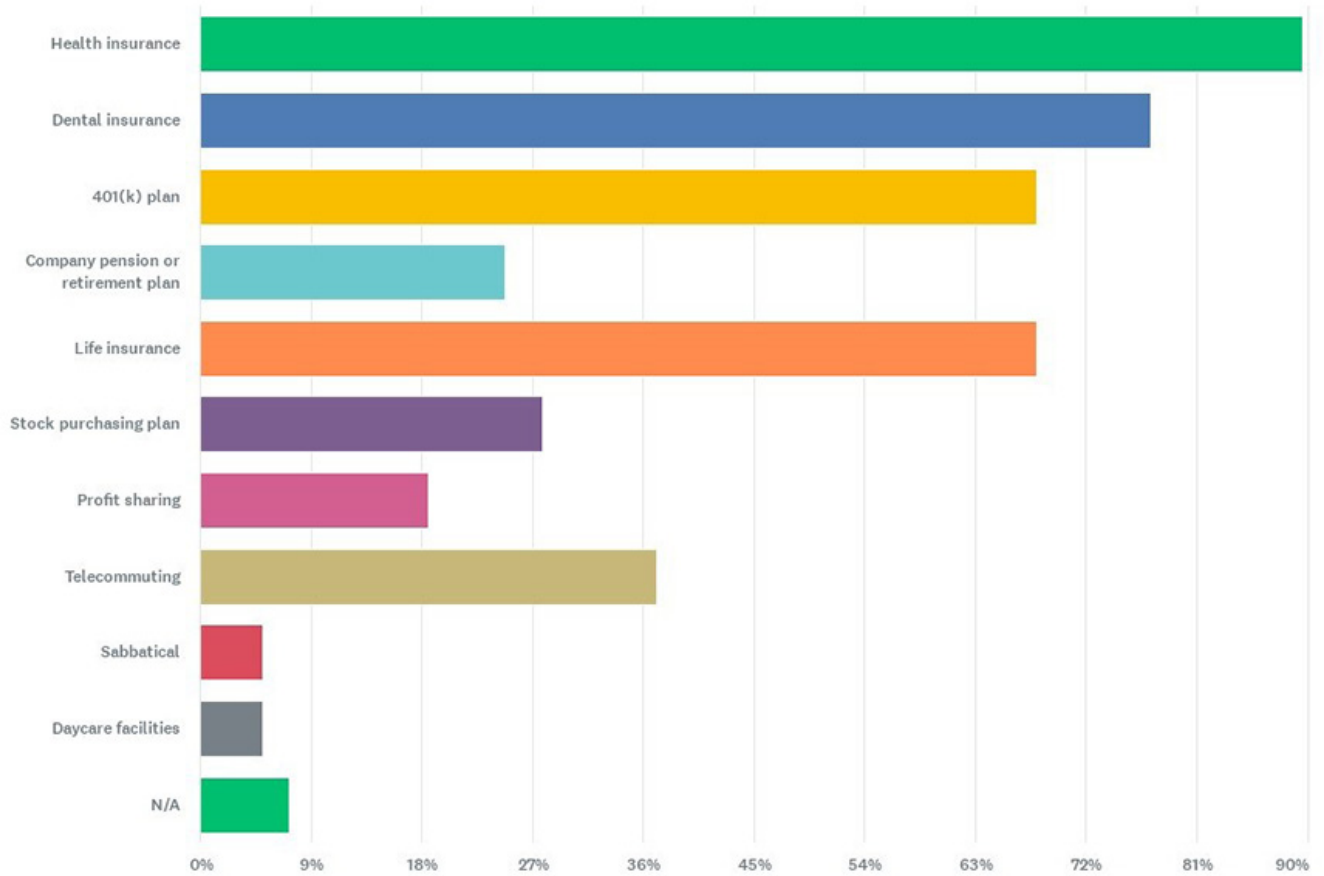


Figure 12. Respondents by benefits.

The tools keep evolving. PCB designers continue to rely on a broad range of ECAD platforms, but a handful account for much of their regular design work. About half of respondents use Altium Designer at least weekly, making it the most widely used platform among survey respondents, followed by Cadence Allegro at roughly 35%. Siemens Xpedition and Cadence OrCAD each draw weekly use from about 18% of respondents, while roughly 16% use KiCad. Designers also report working with Siemens HyperLynx and Pads, Cadence Sigrity and several Zuken platforms, among others.

Which ECAD tools do you use on at least a weekly basis?

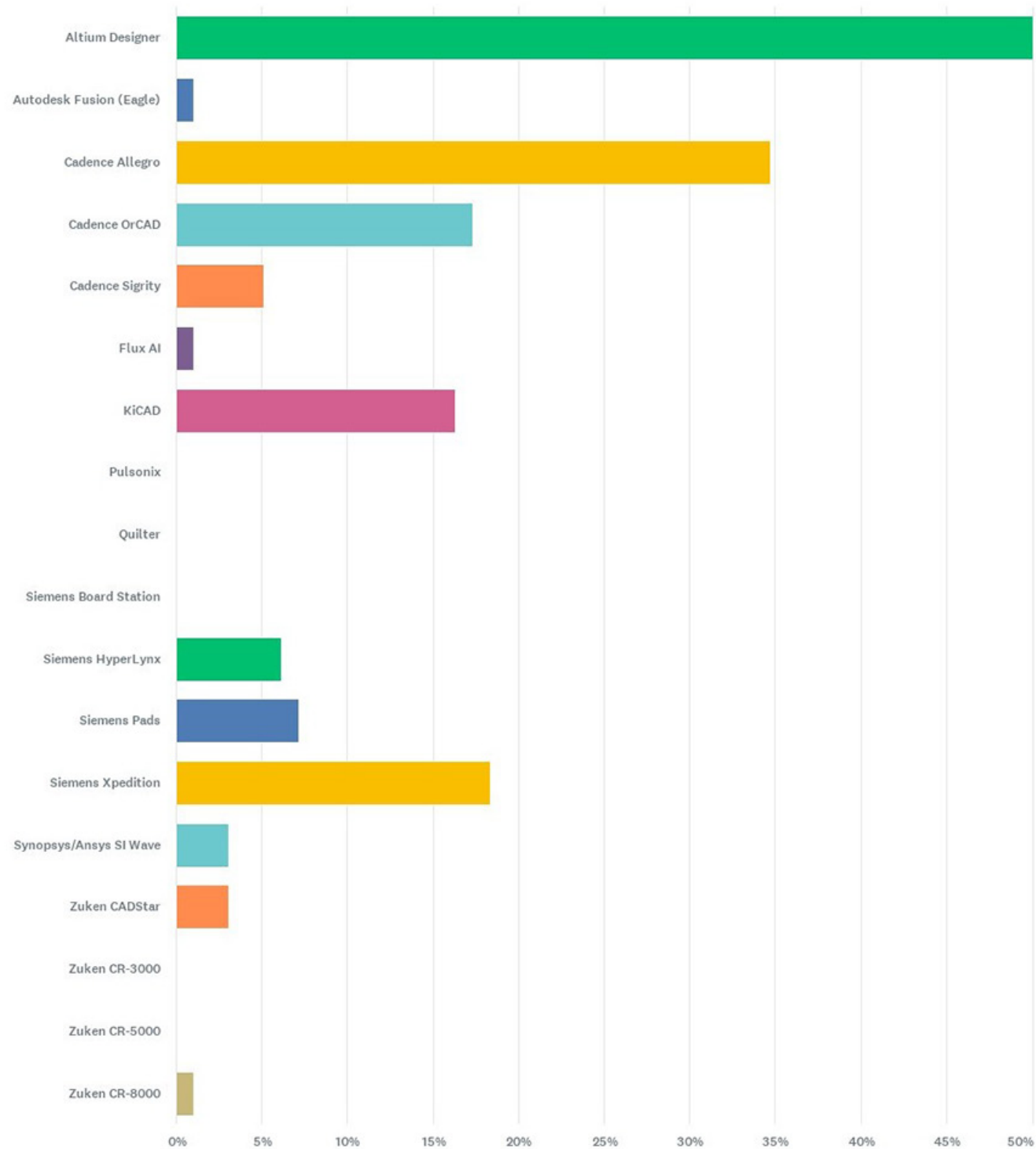


Figure 13. Respondents by ECAD tools used weekly.

Beyond software selection, respondents also wield considerable purchasing influence. Many evaluate, recommend or specify products ranging from ECAD and simulation software to PCB fabrication, assembly services, connectors, components and test equipment, reinforcing the PCB designer’s role in broader engineering and procurement decisions.

Looking Ahead

The survey also highlights the profession's continuing gender imbalance, with men accounting for the overwhelming majority of respondents and women representing a much smaller share of the workforce. As the industry works to strengthen its talent pipeline, attracting and retaining more [women in PCB design](#) will be an important part of building the next generation of engineering talent.

Despite the increasing technical demands of the profession, designers remain optimistic about their careers. Overall job satisfaction continues to trend positive, with most respondents placing themselves toward the upper end of the satisfaction scale. At the same time, many anticipate remaining in their current positions for another five to 10 years, while others see even longer careers ahead.

Taken together, the 2026 survey paints the picture of a profession in good health. PCB designers continue to earn competitive salaries, enjoy stable employment and work on some of the electronics industry's most technically challenging products. At the same time, the survey underscores the growing demands placed on experienced designers as board complexity, technology adoption and development schedules continue to accelerate.

The profession has never stood still. Neither have the people designing the boards that make modern electronics possible. If the survey is any indication, PCB designers remain well positioned to meet whatever challenges come next, provided they continue receiving the tools, training and organizational support needed to keep pace with an increasingly demanding industry.

RYANN HOWARD is managing editor of PCD&F/Circuits Assembly; ryann@pcea.net. Prior to joining PCEA, she helped train the AI for a major US-based company.

Heat Staking vs. Ultrasonic Welding for PCB Assemblies

Both processes form a permanent thermoplastic joint without fasteners or adhesives. For a populated board, the deciding factor is usually not which forms a stronger head – it is where the process energy ends up.

by ALEX SPURGEON

Mechanically fastening plastic to a printed circuit assembly is a routine but consequential step. Boards are retained in plastic housings, light pipes and bezels are located to displays, EMI shields and connectors are captured, and standoffs are formed in a single operation. When designers want to avoid screws, snap fits and adhesives, two thermoplastic joining methods dominate the conversation: heat staking and ultrasonic welding. Both melt and reform plastic to lock parts together, and both are fast and free of consumables. They are not, however, interchangeable on a populated board.

This article compares the two processes specifically for PCB assembly work. The thesis is stated up front, because it should drive the decision: the most important difference for a board is not joint strength but how each process delivers energy. Heat staking conducts heat into a localized boss; ultrasonic welding couples high-frequency mechanical vibration through the assembly. On a board carrying vibration-sensitive components and mixed materials, that distinction usually decides the process before throughput or cost enter the discussion.

How each process forms a joint. A heat-staked joint is formed by an external heat source. A temperature-controlled tool, a stream of hot air, or an impulse-heated thermode raises a plastic boss above its softening point. The softened boss is reformed into a head that captures the mating part, then cooled – ideally under pressure – so it solidifies in the formed shape before the tool retracts. The heat is conductive and stays largely within the boss. Thermoplastic staking can be performed with thermal tooling, a hot punch, hot-air/cold-upset tooling or cold forming, and the process readily joins plastics to dissimilar materials, including metal and PCBs¹.

Ultrasonic welding forms a joint by a different physical mechanism. A transducer converts high-frequency electrical energy into mechanical vibration, typically at 20 to 40kHz, which a horn (sonotrode) delivers to the part under pressure. The vibration produces intermolecular and surface friction at a designed contact point, melting the plastic in a fraction of a second; the melt then solidifies under a hold force². When two thermoplastics are joined, the melt is concentrated at a small triangular feature called an energy director. When a single stud is reformed over a board – the closer analog to staking – the operation is often called ultrasonic staking. The defining characteristic is that the energy arrives as vibration, and that vibration does not stop at the joint.

Figure 1 contrasts the two mechanisms on the same task: a plastic boss retaining a PCB in a housing.

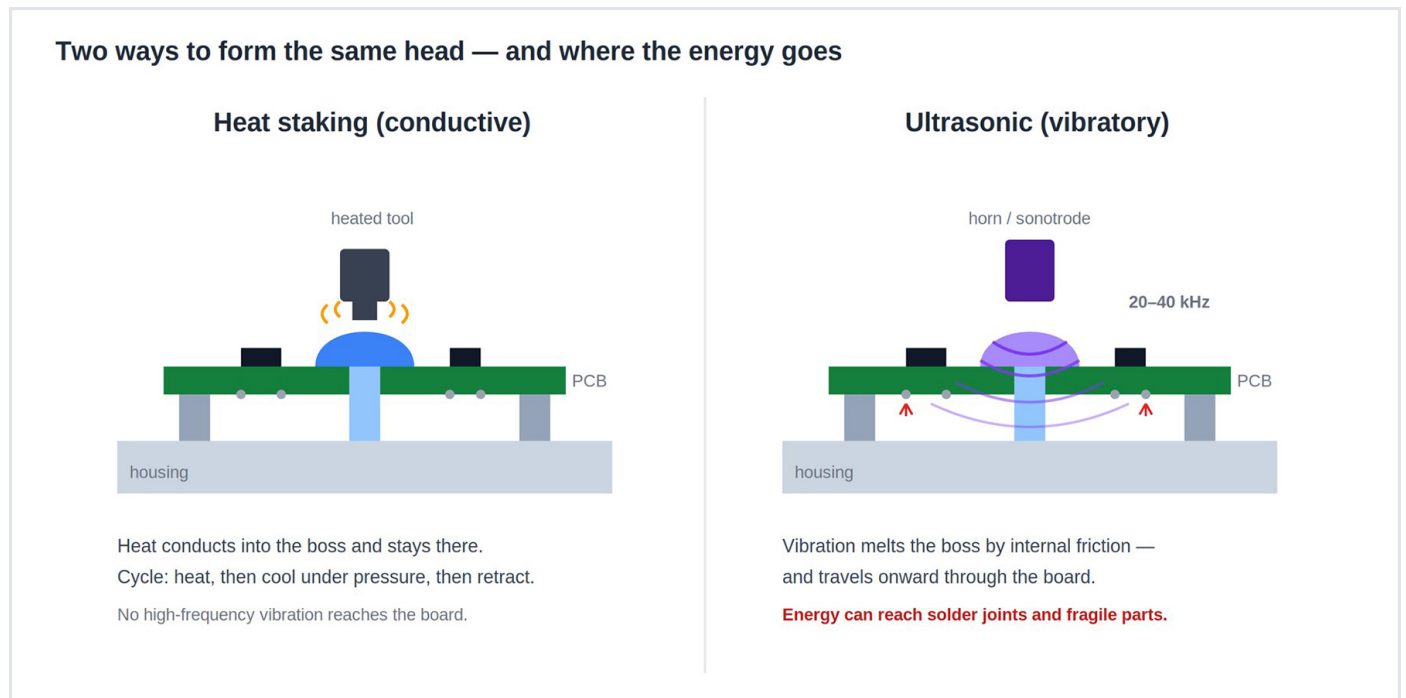


Figure 1. Heat staking conducts localized heat into the boss; ultrasonic welding couples 20–40kHz vibration through the boss into the board and its solder joints.

The practical consequence is visible in the figure. In heat staking, the energy is conductive and localized. In ultrasonic welding, the energy is vibratory and travels through the boss into the board, its solder joints, and any components in the acoustic path.

The crux for populated boards: vibration coupling. A printed circuit assembly is a mechanical structure with its own stiffness, resonances, and fragile features. When ultrasonic energy passes through it, those features are loaded. Solder joints, in particular, are brittle interconnects that do not tolerate repeated high-frequency strain well, and ceramic capacitors, crystals, MEMS devices and fine-pitch packages can be sensitive to vibratory input.

This is not a theoretical concern. A finite-element study of ultrasonic plastic assembly modeled the vibration that reaches the solder joints of a cell phone assembly during welding and identified solder-joint failure driven by the process itself. The analysis showed the failures depended on three structural factors – the location of the chip, the shape of the PCB, and the structure of the housing – rather than on the weld joint in isolation. After the design was revised based on the simulation, the reported reject ratio in mass production fell by roughly 90 percent³.

Two conclusions follow, and both matter for process selection. First, ultrasonic energy can damage a board even when the weld itself is sound, and the location of the damage is governed by the board and housing structure, not by weld parameters alone. Second, the risk is manageable: with the horn kept away from sensitive devices, the board supported and fixtured, amplitude controlled, and energy directors used to localize the melt, ultrasonic welding runs reliably on many electronic assemblies. The point is that the risk has to be engineered out, and that engineering is specific to each board.

Heat staking sidesteps this class of risk. Because the energy is conductive rather than vibratory, there is no high-frequency input to couple into solder joints or fragile parts. The thermal load is real and must be managed – standoff height, clearance from traces and components, and clamp force that does not flex the board all require attention – but the failure mode of vibration-stressed interconnects is largely absent. This is a primary reason heat staking is frequently specified when bosses are located close to populated areas on a board.

Materials and joint design. Material behavior separates the two processes as much as energy delivery does.

Heat staking is tolerant of a wide range of thermoplastics – ABS, polycarbonate, nylon and polypropylene among them – and the tool temperature is dictated by the polymer rather than by a single universal setpoint. Amorphous resins such as ABS and polycarbonate soften over a broad range and are forgiving; semicrystalline resins such as nylon and polypropylene have sharper melt transitions and a narrower process window. As rough heated-tip starting points, ABS forms at roughly 200 to 230°C and polycarbonate at roughly 260 to 300°C, with the exact window set by the grade. Nylon should be dried before staking because absorbed moisture flashes to steam in the molten head, leaving a porous, weak stake; acetal has a narrow window and degrades if overheated. Because there is no vibration, heat staking is also comparatively forgiving of glass- and mineral-filled grades and of higher-temperature resins, which can be prone to micro-cracking under vibratory input. It also joins dissimilar materials and mechanically secures metal to plastic, which is useful when a board is captured between a plastic boss and a metal chassis¹.

Ultrasonic welding is more sensitive to material selection and joint design. Welding is most reliable between identical or closely compatible resins, and amorphous polymers generally transmit and weld more predictably than semicrystalline ones, which absorb and redistribute vibratory energy differently. Fillers and additives alter how the material conducts ultrasonic energy, and the joint must be designed with an appropriate energy director or shear geometry to concentrate the melt. For stud reforming specifically, melt that flows freely under vibration can yield heads of varying diameter and shape unless the tooling and parameters are well controlled, whereas a thermally formed head cooled under pressure tends to be geometrically consistent.

Throughput, cost and process control. Speed is ultrasonic welding's signature advantage. A weld or stake is typically made in well under a second, which makes the process attractive on high-volume lines where a single joint sets the cycle time². The trade-offs are a higher equipment investment – a generator, converter, booster, and a horn tuned to the operating frequency – a more involved setup, and a narrower process window that is sensitive to part and material variation.

Heat staking inverts several of those terms. A single cycle is longer because it includes both a heat phase and a cooling phase, often a few seconds in total. But multi-point thermal tooling forms many bosses in one stroke, so per-board throughput can be competitive even when per-joint time is longer. Equipment costs are generally lower, maintenance is simpler and modern systems use distance- or energy-based control with position feedback to hold head geometry within tolerance. Two process details carry most of the quality on a board: cooling the head under pressure so it does not relax back and a clamp-and-standoff scheme that locates the board without flexing it. On the ultrasonic side, the equivalent variables are amplitude – set by the booster and horn gain – trigger and weld force, weld and hold time, and rigid support of the part; these govern both joint quality and the amount of energy reaching the board. **Figure 2**

summarizes the qualitative comparison across the attributes that most often determine a PCB assembly application.

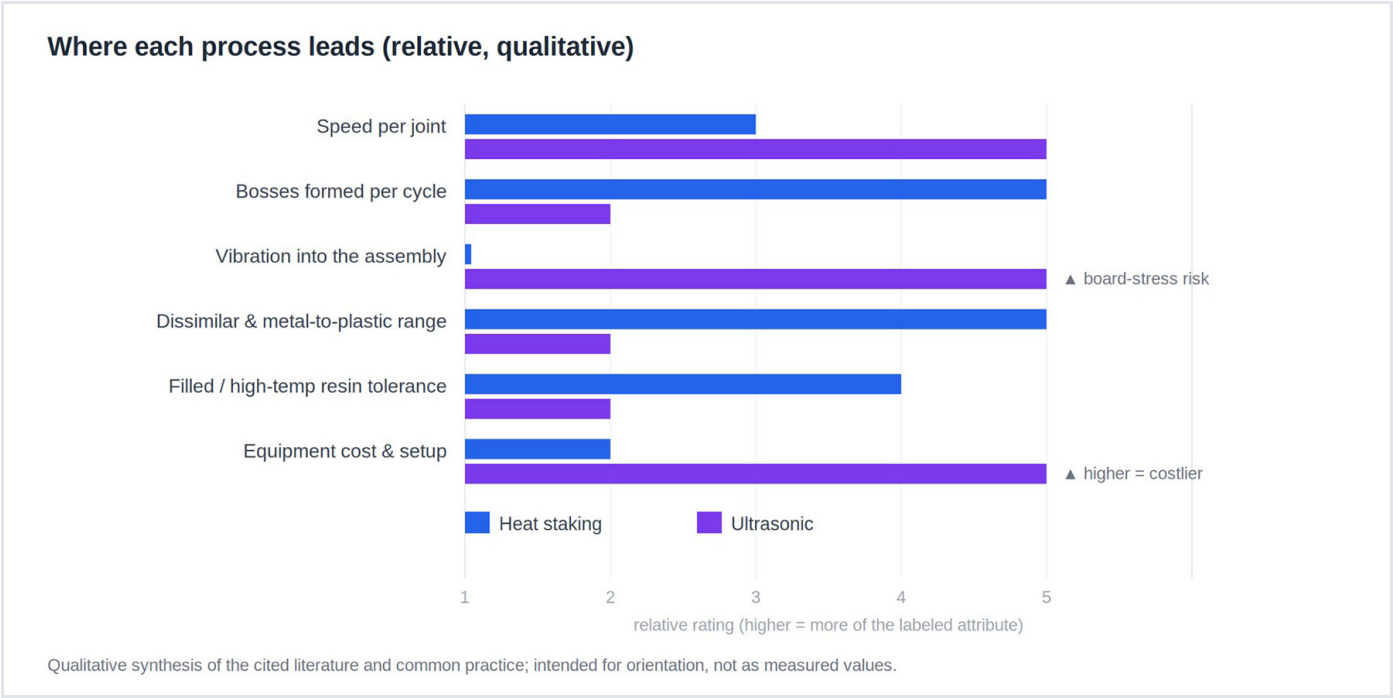


Figure 2. Qualitative comparison of heat staking and ultrasonic welding across attributes that commonly decide a PCB-assembly application. Higher indicates more of the labeled attribute; values are for orientation, not measurement.

The figure is a qualitative synthesis intended for orientation rather than a set of measured values; the right answer for a specific assembly depends on its components, materials, geometry and volume.

A selection framework. For PCB assemblies, the decision can be reduced to a short sequence of questions, shown in **Figure 3**.

Choosing a process for a PCB assembly

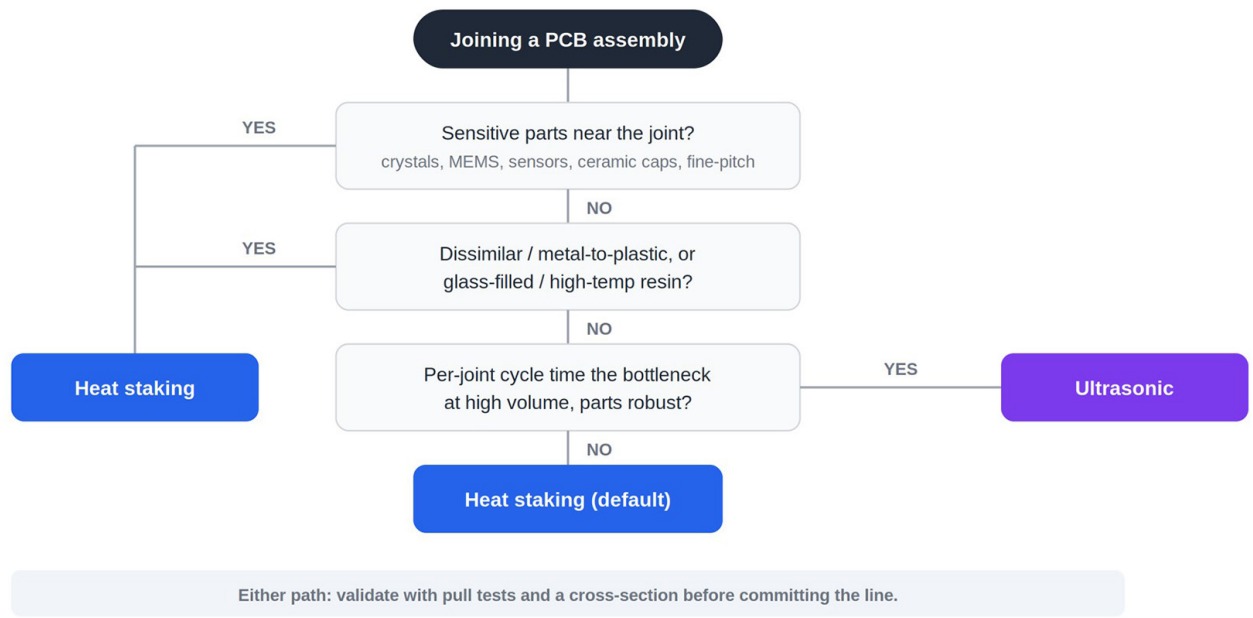


Figure 3. A process-selection flow for PCB assemblies. Sensitive components or mixed and filled materials favor heat staking; a per-joint cycle-time bottleneck at high volume on a robust board favors ultrasonic.

Work through it in order. If vibration-sensitive components are near the joint, heat staking avoids the energy path that would put them at risk. If the assembly joins dissimilar materials or metals to plastics, or uses glass-filled or high-temperature resins, heat staking is the more tolerant process. If neither of those applies and per-joint cycle time is the genuine bottleneck at high volume on a mechanically robust assembly, ultrasonic welding's speed becomes the deciding advantage. Absent a strong cycle-time argument, heat staking is a reasonable default on cost and simplicity grounds. Whichever process is chosen, the joint should be validated with pull tests and at least one cross-section before it is committed to a production line; neither a hollow head, a cracked boss base, nor a vibration-stressed solder joint is visible from the outside.

Validation and the defects each process hides. Neither process should be released on appearance alone, because the failures that matter are internal. A heat-staked head can look complete while hiding a cold, unfused core that fails a pull test, an over-formed head that has cracked the boss base, or thermal exposure to a component that sat too close to the tool. An ultrasonic joint can look clean while concealing a partially welded interface, a marked or diaphragmed area beneath the horn, or – as the finite-element work showed – solder-joint damage at a location remote from the weld itself³. A short validation routine catches all of these. Pull-test a sample of joints to failure, cross-section at least one to inspect head fill and the boss base, and, where the assembly is vibration-sensitive, functionally test or inspect the solder joints nearest the tool after ultrasonic processing. Building that routine into first-article approval is inexpensive relative to a field return.

Conclusion

Heat staking and ultrasonic welding both produce strong, fastener-free thermoplastic joints and belong in a PCB assembly engineer's toolbox. The choice between them for a populated board should be based on energy delivery first.

Ultrasonic welding is faster per joint and well suited to high-volume work, but its vibration couples into the assembly and can stress solder joints and fragile components unless the board, housing, and horn placement are engineered to prevent it – a risk demonstrated in finite-element analysis and resolved only by structural redesign³. Heat staking delivers localized, conductive heat that avoids the input, tolerates dissimilar and filled materials, and reduces cycle time through multi-point tooling, at the cost of a longer individual cycle. Match the process to the assembly: choose ultrasonic when per-joint speed on a robust board dominates, and heat staking when the board carries sensitive components, mixes materials, or runs filled or high-temperature resins. In every case, validate the joint before the line depends on it. 

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ALEX SPURGEON is the founder of U.S. HeatStake (usheatstake.com), a U.S. manufacturer of precision impulse heat-staking and brass-insert installation systems based in Roanoke, Indiana. He works with assembly teams on thermoplastic joining process development. He can be reached at info@usheatstake.com or (614) 549-0627.

Contamination Control in Robotic Electronics Manufacturing

As robotic systems become more advanced, effective cleaning and contamination control are increasingly important for ensuring long-term reliability and manufacturing consistency.

by ELIZABETH NORWOOD

Robotic systems are becoming increasingly common across industrial automation, logistics, healthcare and manufacturing environments. Whether used for assembly operations, materials handling, inspection or collaborative applications, today's robotic platforms rely on sophisticated electronic assemblies to process information, control movement and communicate with other systems.

The rapid expansion of the robotics sector is creating demand for more advanced electronic assemblies. According to the [State of Robotics 2026](#) report, the global robotics market reached \$38 billion in 2026, growing 34% year-on-year. As manufacturers continue to develop more capable robotic systems and deploy them across a wider range of applications, greater emphasis is being placed on the quality and consistency of the electronics used within them.

At the heart of these machines are printed circuit board assemblies (PCBAs) responsible for power management, sensor interfaces, communications and control functions. To deliver greater functionality, designers are incorporating more components into smaller spaces, resulting in higher-density assemblies and increasingly challenging board layouts.

While advances in electronics design have enabled significant improvements in robotic capability, they have also increased the importance of contamination control during manufacturing. Residual fluxes, particulates and other manufacturing and assembly contaminants can affect assembly quality and create conditions that contribute to electrical failures over time.

For manufacturers producing electronics used in robotic systems, effective cleaning has become an important part of achieving consistent manufacturing quality and helping ensure assemblies perform as intended throughout their operational life.

Why Cleanliness Matters

Contamination remains one of the most common causes of electronic assembly problems. During PCBA production, boards are exposed to a variety of materials and processes, including solder pastes, fluxes, marking inks, handling

residues and environmental particulates. While many contaminants may be invisible after manufacture, they can remain on the assembly surface or become trapped beneath components.

If not removed effectively, these residues can contribute to a range of problems including electrochemical migration, dendritic growth, parasitic leakage and corrosion. In some cases, contamination may also interfere with conformal coating adhesion or affect the performance of subsequent manufacturing processes.

The challenge is that contamination-related issues are not always immediately apparent. Assemblies may successfully pass inspection and functional testing before problems develop later in service. For this reason, many manufacturers view cleanliness as a process-control issue rather than simply a cosmetic concern.

As electronic assemblies become smaller and more densely populated, ensuring that contamination has been removed effectively becomes increasingly important.

Sources of contamination during production. Electronic assemblies can be exposed to numerous contaminants throughout the manufacturing process. One of the most common sources is soldering flux residue. Flux plays an essential role during soldering by removing oxides and promoting proper wetting. However, flux residues left after soldering can pose challenges if not properly managed.

Additional contaminants may include solder paste residues, handling oils, adhesive residues, marking inks, dust, fibers and other particulate matter introduced during production.

These contaminants generally fall into several broad categories:

Particulate contamination includes dust, cloth fibers and small fragments of manufacturing debris. These contaminants may settle on assemblies during production and can be difficult to remove from densely populated boards.

Organic contamination includes oils, greases, flux residues and other carbon-based materials. These residues are commonly encountered during electronics assembly and often require specialized cleaning fluids for effective removal.

Inorganic contamination can include ionic residues originating from soldering materials and process chemicals. These contaminants are often regarded as particularly important because of their potential to contribute to electrochemical migration and other electrical failures.

Water contamination can also present challenges. Moisture trapped beneath components or within complex assembly structures may affect downstream manufacturing processes and can contribute to corrosion-related issues if not properly removed.

Understanding the type of contamination present is often the first step in selecting an appropriate cleaning process.



Figure 1. Many contaminants are invisible to the naked eye, making effective cleaning and verification increasingly important for today's complex electronic assemblies

Cleaning Challenges in Modern Robotic Electronics

The electronic assemblies used in robotic systems present many of the same cleaning challenges found throughout modern electronics manufacturing.

Today's PCBAs frequently incorporate fine-pitch components, bottom-termination devices, low-standoff packages, and densely populated layouts. Components such as QFNs, BGAs and power devices create narrow gaps where contaminants can become trapped during manufacturing.

As assemblies become more compact, these areas become increasingly difficult to access using conventional cleaning methods.

Flux residues and particulates can accumulate beneath components, around solder joints and within small spaces that may be inaccessible to visual inspection. Although contamination in these areas may not be visible, it can remain on the assembly after production.

The challenge is further complicated by the variety of materials used within modern electronic assemblies. PCBAs may incorporate advanced laminates, plastics, elastomers, ceramics and other materials that require careful consideration when selecting cleaning processes and cleaning fluids.

Manufacturers must therefore balance cleaning effectiveness with material compatibility to ensure contamination is removed without damaging sensitive components or assembly materials.

Cleaning before conformal coating. Many electronic assemblies used in robotic environments are protected with conformal coatings. These coatings help shield PCBAs from moisture, dust, chemicals and other environmental contaminants that may be encountered during operation. For robotic systems operating in manufacturing environments, conformal coating often plays an important role in the overall protection strategy. However, conformal coatings perform best when applied to thoroughly cleaned surfaces.

If residues remain on the assembly before coating, they may interfere with adhesion and affect coating performance. Contaminants trapped beneath the coating can also become more difficult to identify and remove after the coating process is complete.

For this reason, cleaning is often regarded as a critical preparation step before coating operations. By removing residues before coating, manufacturers can help ensure the coating adheres correctly and provides the intended level of environmental protection.

Achieving cleanliness is only part of the challenge. Manufacturers must also be confident that cleaning processes are delivering consistent results.

As assemblies become more complex, visual inspection alone is often insufficient to determine whether contamination has been removed successfully. Residues can remain beneath components or within areas that are difficult to inspect directly. This has increased interest in cleaning validation and cleanliness testing.

A variety of techniques may be used to evaluate cleaning effectiveness, including ionic contamination testing, SIR (surface insulation resistance testing) and other analytical methods designed to identify residual contamination.

These techniques help manufacturers establish whether cleaning processes are performing as intended and whether contamination levels remain within acceptable limits.

Process consistency is equally important. Cleaning performance can be influenced by factors such as contamination loading, equipment parameters, cleaning fluid condition and process control. Establishing repeatable cleaning procedures helps ensure that cleanliness standards are maintained from one production batch to the next.

For manufacturers producing electronics assemblies in volume, consistency is often just as important as cleaning performance itself.

Precision Cleaning Approaches

A variety of cleaning methods are available to electronics manufacturers, ranging from manual cleaning techniques and benchtop processes through to fully automated cleaning systems. As robotic PCBAs become smaller and more densely populated, many manufacturers are reassessing whether traditional cleaning approaches can effectively remove contamination from increasingly challenging board geometries.

One precision-cleaning method widely used throughout electronics manufacturing is vapor degreasing. The process uses engineered cleaning fluids within a controlled cleaning system to remove contamination from PCBAs. Unlike many conventional solvents, modern cleaning fluids are formulated for precision cleaning and designed to remove a broad range of contaminants while remaining compatible with sensitive electronic assemblies.

The physical properties of the cleaning fluid play a significant role in cleaning performance. Modern engineered fluids typically exhibit very low surface tension and low viscosity, allowing them to penetrate narrow spaces and reach contamination that may be inaccessible to less effective cleaning methods. This is particularly important as robotic electronic assemblies continue to become more compact, creating areas where residues can remain trapped after soldering and be difficult to remove consistently.

Different contaminants often require different cleaning approaches. Organic residues such as fluxes, solder pastes, oils and greases may require one type of cleaning chemistry, while ionic contamination and particulate matter can present entirely different cleaning challenges. Selecting the appropriate cleaning fluid is therefore an important part of the process. The fluid must be capable of dissolving or displacing the contamination present while remaining compatible with the materials used throughout the assembly.

Another advantage of modern engineered cleaning fluids is their rapid evaporation rate. After cleaning, the fluid evaporates quickly from the assembly surface, leaving PCBAs clean and dry without the lengthy drying stages associated with some alternative cleaning methods. This characteristic is particularly beneficial for densely populated assemblies where moisture or cleaning media may otherwise become trapped beneath components or within complex structures.

The controlled nature of vapor degreasing also helps improve process consistency. Cleaning conditions remain stable throughout production, helping manufacturers achieve repeatable cleaning results across different assembly types and production volumes. Combined with the cleaning performance of modern engineered fluids, this enables effective removal of contamination while supporting the process control and repeatability required in modern electronics manufacturing.

Robotic systems depend on electronic assemblies that are expected to operate consistently in demanding environments. As PCBAs become more complex and manufacturing tolerances continue to tighten, contamination control is becoming an increasingly important part of the production process.

Achieving the required level of cleanliness involves more than simply removing visible residues. Manufacturers must understand the types of contamination present, select cleaning processes capable of addressing those contaminants and verify that cleaning results remain consistent over time. Cleaning validation, process control, and material compatibility all play key roles in ensuring that assemblies are prepared for subsequent manufacturing stages and

long-term operation.

For robotics manufacturers, PCBA cleanliness is no longer simply a finishing step. It is an integral part of the overall manufacturing process and a key contributor to the production of high-quality assemblies for today's robotic applications. 

ELIZABETH NORWOOD is a senior chemist at MicroCare, LLC, which offers precision cleaning solutions. She has been in the industry for more than 25 years and holds a bachelor's in chemistry from the University of St. Joseph. Norwood researches, develops and tests cleaning-related products. She currently has one patent issued and two pending for her work.

Improving Productivity in a High-Mix Environment Utilizing Lean Manufacturing Principles

Applying Lean manufacturing principles to streamline higher-level assembly, reduce wait times and improve throughput.

THE ELECTRONICS MANUFACTURING services (EMS) industry is a form of controlled chaos. EMS factories often have 30 or more customers with completely different products, varying levels of assembly complexity and highly variable demand patterns. To control this chaos, EMS providers implement systems to standardize production processes and streamline production flow. While manufacturers can often significantly automate high-volume production, higher-mix production typically involves a greater human element, particularly in higher-level assembly. Consequently, production team members must also standardize their approach to manual assembly activities. This article looks at the strategy EDM used to introduce Lean manufacturing principles to its production team and the initial results that training delivered.

Integrating Lean Principles Into Higher-Level Assembly

EDM is a full-service, employee-owned EMS provider with a facility in Lynchburg, VA. Its surface mount technology (SMT) printed circuit board assembly (PCBA) and test processes use highly automated, continuous-flow manufacturing. However, its higher-level, or box-build, assembly processes have traditionally used batch-flow work cells. Increasing product mix and volumes have necessitated a transition to continuous-flow processes in higher-level assembly.

As a result, the team has been implementing Lean manufacturing principles in conjunction with GENEDGE, a Virginia-based NIST Manufacturing Extension Partnership (MEP) center. The team has held kaizen workshops that introduced core concepts and tools, including value stream mapping and Deming's Plan-Do-Check-Act (PDCA) cycle. The goal is to encourage team members to continually consider ways to apply Lean principles day-to-day to improve efficiency and throughput.

Team exercises reinforced these concepts. For example, teams started by analyzing a current-state process map of a mock company with significant inefficiencies against a limited set of improvement options. A subsequent exercise allowed the team to develop a future-state map with no constraints on improvement options. Combining these exercises helped team members better understand the impact of their improvement choices.

The team subsequently held kaizen events on the production floor. The first event analyzed a project for which the customer's volumes had more than doubled in both required lot size and frequency of production builds compared with the prior year. The kaizen event aimed to optimize the process and improve throughput.

The team mapped the current state and then used the PDCA process to identify potential improvements and determine which would likely have the greatest impact. At lower volumes, one operator could produce 32-40 pieces per hour. When the team scaled the product to a one-piece-flow model, three operators produced a total of 120-140 pieces per hour. This improvement in throughput aligned with the customer's increased volume requirements.

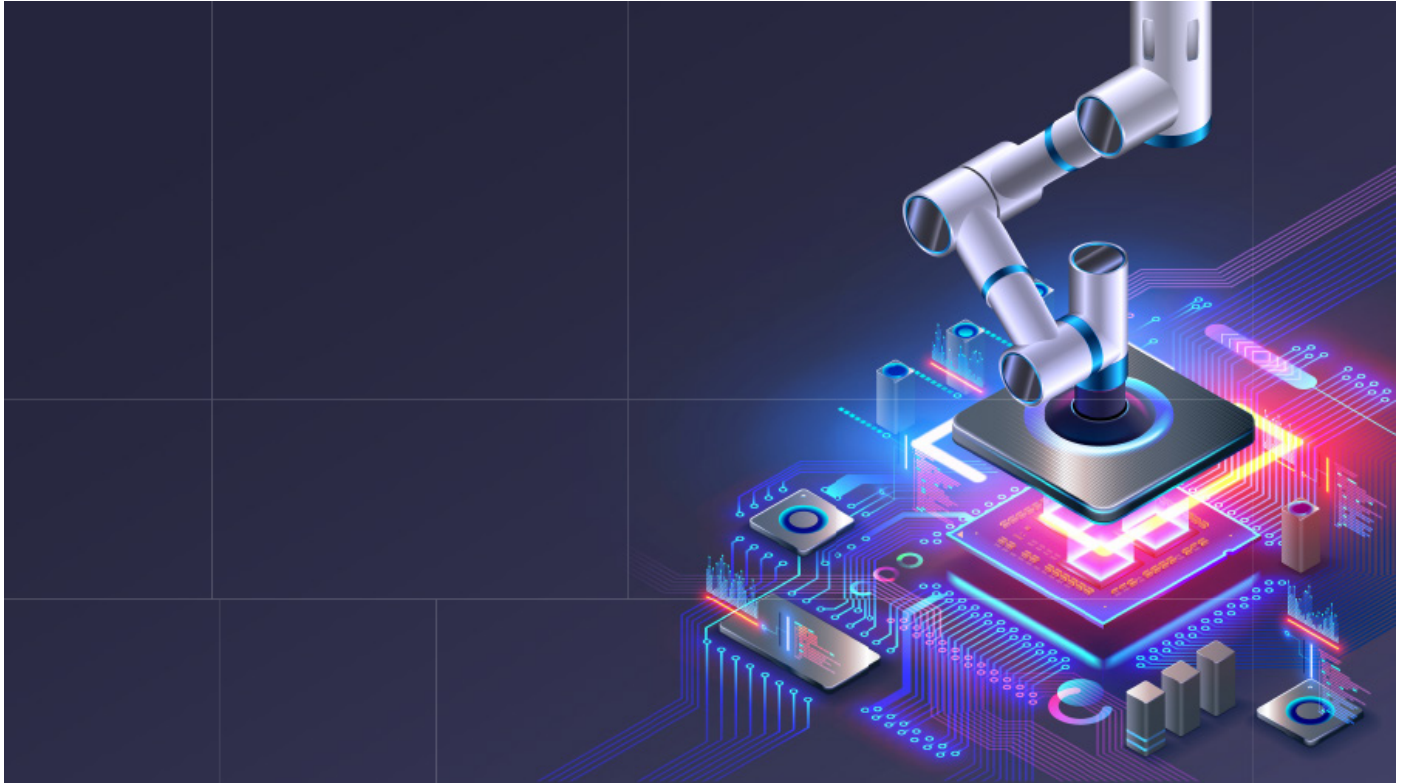


Figure 1. Lean manufacturing principles can help high-mix EMS operations streamline workflows, reduce wait times and improve throughput.

The team identified a list of improvements for the future-state map, including:

- Consolidating workspace from one workbench per operator to two operators per workbench. This change reduced the distance operators needed to transfer material.
- Changing the tool used to clean dust from a plastic overlay from a can of air to a benchtop-mounted air gun.
- Replacing regular screwdrivers with a screwdriver mounted on a tool balancer over the product. The team also replaced bins holding screws with screw presenters, enabling the operator to grab a screw with the screwdriver's magnetic tip instead of reaching into a bin.

EDM's Lean integration continued to focus on the wastes of waiting and transportation. Three cross-functional teams of eight people, including production operators, engineers and purchasing personnel, analyzed existing inventory levels, material flow and production flow product by product.

The teams initially analyzed two products. In one case, a spaghetti diagram of the complete flow showed that material and product traveled 73 miles over a six-week period. Moving to continuous-flow cells reduced the total wait time to 1.5 weeks. Converting the second product to continuous flow reduced four weeks of wait states to 3.5 days. The teams continued analyzing products adaptable to continuous flow until they had transferred all likely candidates. In conjunction with this analysis and the transition to continuous-flow processes, EDM also educated employees on 6S processes designed to improve workspace and workplace organization and safety.

The second kaizen workshop focused on a new product final assembly operation. The product had 33 part numbers and 70 parts total. During the initial production run, the team measured assembly time at 44 minutes of labor per unit. Team members then went through several improvement iterations, including changing the workstation setup and dividing the assembly work differently. They timed each operation to enable a line-balancing exercise.

The final configuration eliminated bottlenecks by dividing work among operators into equal blocks of time. Each operator became responsible for checking the material in their bins for accuracy and checking the prior operator's work. The team also modified the toolkits. Historically, common tools were available in a work-cell toolset, while product-specific tools remained with the product kit. Now, EDM issues each workstation a common toolkit for the product. As a result of these improvement efforts, assembly time for the product dropped from 44 to 24 minutes.

Leveraging outside resources such as GENEDGE offers an effective way to introduce Lean concepts to production teams. Training exercises that encourage teams to apply continuous improvement processes beyond workshop activities can also help create a Lean culture. 🧩



MATT CLINE is EDM's quality manager and can be reached at mccline@edmva.com.

MIKE STANLEY is EDM's manufacturing manager and can be reached at mstanley@edmva.com.

Old Man, Round Two, Not Half Bad

Eternal vigilance is the price we pay for catching others' screw-ups.

MY FATHER OWNED a printed circuit fabrication company. I apprenticed at that company as a teenager, learning a trade I could always fall back on should more glamorous options vaporize. As an apprentice, I attended many meetings. My job was to listen and learn. My father used to employ an old management trick in those meetings. He would feign confusion when he wanted subordinates to focus on an important subject, or drive home a valuable lesson. Often during a sales review, some hotshot salesperson, in the full-bore naïve flower of heedless youth, would describe a new opportunity in the brightest, glowing-est, most opportunistic, can't-miss, counting-my-commissions-before-they-hatch terms. If you didn't know better, you'd visualize the sales hotshot already forking over a down payment on a beachfront condo before the ink had hardened on a meaningless letter of intent. This is referred to in the trade as a triumph of hope over experience.

My father's scrutiny was agonizing for all concerned, except my father. He would slow everything down. Way down. Down to earth. Delighting in the tension he imposed upon the room. He would methodically regurgitate, word for word, the salesperson's pitch; except much slower than a young man's patience or attention span (or ego) would permit. Which was the point. He would often transpose words from the presentation intentionally, forcing the original presenter to be on alert for misinterpretations and be prepared to intervene and correct, where necessary. He would speak in an affected, seemingly confused tone of voice as if to signify he wasn't fully comprehending – and, by extension, accepting – the nervous young man's attempt at persuading (in those days, the early 80s, the salespersons were invariably male) all present that he had the inside line on the Next Big Thing. He would force the young man to make corrections to my father's recapitulation of the opportunity, down to the last syllable. You could almost hear the sound of deflation as the proceedings dragged on mercilessly.

This weekly excursion into verbal water torture was usually held on a Friday afternoon (another old management trick my father delighted in performing regularly), when young men's thoughts while in captivity tended in the direction of the weekend, and more appealing pleasures commencing with the letter W. Woe betides the poorly prepared salesman: many were dispatched to the weekend in a dark mood with disrupted plans and dents in their personal cashflow projections. My father reveled in these moments; he did not take kindly to pretentious young men.

The ordeal served a worthy purpose, searing into facile brains an unforgettable lesson: by the time the interrogation was finished, the substance of the opportunity was largely eviscerated. By then we often wondered what the original fuss was in the first place. The salesperson, forced to be on the defensive, ejected from the Friday cross-examination, metaphorical tail between legs, learned to make a stronger case, do his homework, and come back thoroughly prepared before attempting another swan dive from the diving board of Can't-Miss Land.

I took it all in. Being the Boss's Son, I was not immune to my father's rhetorical proctology. Indeed, I got more subjective scrutiny than any salesman (or woman, as the benighted 80s transitioned to the enlightened 90s). And, lucky me, I got them at home *and* at work. My dates got them too. (The woman who eventually became my wife stormed out of a restaurant family dinner one time, after a notably intrusive interrogation. It was a scene. I'm sure daughter-in-law and father-in-law laugh about the episode now, during Happy Hour in Heaven. It was not amusing at the time. I hated every minute of every hour of every day being dragged through those sessions.)

But I listened. And remembered. And took notes. And grew older. And began to see the wisdom in such techniques. I started applying them, in my own way; first tentatively, then frequently. Because they worked.

Forty-five years later, I employ a variant of the same technique.

Call it "I'm confused." Plant that elementary sentence at the end of an email, and watch consternation spread like waves on water.

Like my father (curiously, the older I become, the wiser he sounds), I employ those two words to sharpen slipshod thought, regroup disjointed or scattered attention, and achieve clarity of purpose, and thus agreement, on some previously muddled subject. That's the theory.

In our business, we deal with many muddled subjects. This is because of customers; you know, the ones we are drilled to believe are always right. (They are not.) Companies are populated by many muddled individuals, some with agendas, others merely slow movers. They've been schooled in euphemism, or acceptance euphemism, as the norm, or as a survival skill. Clear, direct thinking is viewed in some corporate quarters as a threat.

Not to me.

There's the customer who declares that they want to hire us for a flying probe test of 10,000 boards, starting immediately and ending in a period of 90 days. Such declarations gain prompt attention. Quotes are sent. Credit references are sent back. Indications are that something's happening. Then nothing. After several weeks of silence, we inquire repeatedly. The answer, after several attempts: the customer's customer is having second thoughts about "expanded capacity" and wishes to examine several production scenarios before mapping out and making a decision.

Second thoughts? Expanded capacity? Several production scenarios?

Experience tells you what's going on here.

This is doublespeak for "I don't like your price, I'm getting other quotes, and will not make a decision until one of those quotes fits my predetermined model."

I reply to the customer with a simple, "I'm confused."

Then, in a second email, I elaborate. "You asked for immediate service. We can put two machines on your project immediately, just like you asked. If your customer is fantasizing (Mapping out? Sounds like wargaming.) about nine

machines sitting idle and collecting dust, waiting for you to traipse through their door with boards to be tested, you will seek in vain.” The subtext: management had no clue about the cost of this project. More plausible: the price they plugged unilaterally into their cost model bore no relationship to reality. Somebody needs adult supervision.

They don’t reply. I interpret this as tacit acceptance of my argument. Words matter.

Or the customer who had us test a job to revision B, then asked us to quote to revision A.

Huh?

Wait a minute. Doc Control 101 says that B follows A, not the reverse. What’s going on?

“I’m confused.”

Spluttering justifications by the customer, reminiscent of cockroaches bathed in unwelcome sunlight. *The customer made some changes, and we mistakenly thought they rolled the revision, but they really haven’t. It’s merely a minor update, and we’re still at revision A. Sorry.*

None of the aforementioned changes were documented. We were supposed to find them, forensically, on the boards, once received. Whatever happened to ECOs?

Why not simply admit the truth? Somebody screwed up and got caught. Why the rhetorical contortions?

Or the customer who hired us to perform AXI services on a very large board, only to balk at our price.

Our machine is the only AXI system capable of processing their board. Even so, we have to perform special modifications to the conveyor to admit it inside the machine for scanning. We’re talking void-the-warranty-style actions. The customer took nearly three months to justify paying us, then gave us a go-ahead, then took an additional month to modify board documentation to somehow make it easier for us to process their board. All sorts of big company excuses to obfuscate, push responsibility, and delay, without ever once consulting those of us who actually do the work.

All of their “helpful” pre-engineering was no help at all. In fact, the CAD file they provided was useless. Missing X and Y and netlist information. Also missing was a purchase order. Yet in their minds, we are expected to proceed. They dream.

Only one thing left to do.

Class, let us, as a chorus, join together as one voice, in our now-familiar refrain:

“I’m confused.”

We received the PO the next day, and the correct CAD the following day, after threatening additional charges for manual data entry. People often respond well to threats.

I use the same method in the office, hopefully more in a spirit of benevolence than belligerence. Customers deserve the latter; trusted employees do not. Still, situations arise requiring a sorting, with some guidance that only experience allows. Incantation of the magic words can often cut the chaos and retrieve focus.

The list is long: banking instructions gone wrong; customer files mislabeled; the requested test method misunderstood; shipment instructions misinterpreted; customer details overlooked; order status not clearly communicated to the customer; customer requests being responded to less than promptly; emails misconstrued. Lots of mis-s. Stuff happens.

Some figure it out on their own. Others need to have misalignment pointed out, gently, in the form of a question. Like my father did 45 years ago.

“I’m confused.”

It’s not because I’m confused. Because I’m not. 🧩P



ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.

PCD&F



APOLLO AUTOMATION ESPHOME STARTER KIT

ESPHome Starter Kit simplifies embedded hardware development with ESPHome. Includes the ESPHome C6 board based on the ESP32-C6-MINI-1 wireless module and four snap-off sensor and notification modules connected through flexible printed circuit (FPC) cables. Supports Wi-Fi 6, Bluetooth LE, Thread and Zigbee and enables configuration through the ESPHome device builder application. Includes access to hardware documentation, schematics and Gerber files.

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PANASONIC INDUSTRY ECWFJ METALLIZED POLYPROPYLENE FILM CAPACITORS

ECWFJ Series metallized polypropylene film capacitors feature AEC-Q200 qualification for industrial and automotive power electronics applications. Offer voltage ratings from 600V to 1,100VDC and capacitance values from 1µF to 12µF. Operate from -40°C to 110°C, with the 1,000V version rated to 105°C, and maintain stable operation at 40°C

and 95% relative humidity for up to 1,000hr. Feature patterned metallization with an integrated fuse mechanism, flame-retardant plastic enclosure and nonconductive resin. For DC/DC converters, onboard chargers, e-compressors, solar inverters, EV charging infrastructure, industrial power supplies, LED lighting, smart meters and embedded power systems.

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PEWCB ONE DESKTOP PCB PROTOTYPING SYSTEM

PewCB One desktop PCB prototyping system produces double-sided printed circuit boards in-house using laser ablation. Processes ceramic PCB blanks with preformed vias, automatically creates solder paste stencils and supports trace widths down to 0.1mm. Compatible with Windows and Linux software for PCB prototyping and hardware development.

PewCB

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POLAR INSTRUMENTS SPEEDSTACK SOFTWARE UPDATE

Speedstack PCB stackup design software adds Ventec glass-free materials, including pro-bond and thermal-bond Bondply dielectrics, to its online material libraries. Adds visualization of multi-material families within PCB stackups and customizable display colors in stackup documentation to improve communication of complex material and stackup requirements from design through fabrication.

Polar Instruments

polarinstruments.com

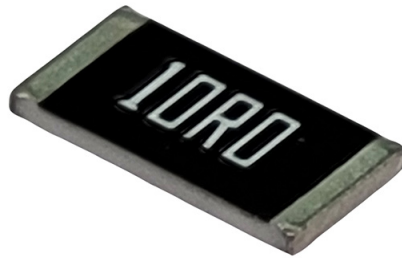


STACKPOLE RMHT HIGH-TEMPERATURE CHIP RESISTORS

RMHT Series AEC-qualified thick-film chip resistors maintain full-rated power up to 105°C for high-temperature automotive, aerospace and industrial applications. Available in 0402, 0603 and 0805 package sizes with resistance values from 1Ω to 300kΩ, tolerances of 0.5%, 1% and 5% and TCR options of 100ppm/°C or 200ppm/°C. Include anti-sulfur protection and 100% automated optical inspection.

Stackpole Electronics

seielect.com



STACKPOLE RNCQ HIGH-FREQUENCY THIN-FILM RESISTORS

RNCQ Series high-frequency thin-film chip resistors support RF and microwave applications operating above 1GHz. Built on high-purity alumina substrates, support frequencies up to 70GHz in the 0201 package and 50GHz in 0402 and 0603 sizes while maintaining stable impedance at higher frequencies. Available in sizes from 0201 through 1206 and include impedance-versus-frequency curves and S-parameter data for high-frequency circuit modeling and optimization.

Stackpole Electronics

seielect.com



YAMAICHI Y-CIRC P T-SERIES RIGHT-ANGLED PCB SOCKET

Y-Circ P T-Series 90° PCB socket provides direct board mounting for space-constrained industrial applications. Features IP68 protection when mated and supports harpoon pins, screw mounting and solder pins. Available in sizes

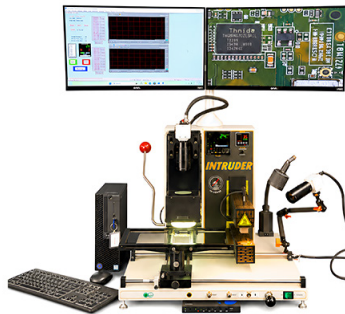
09, 12, 15 and 18 with multiple pin counts for industrial, automation and test and measurement applications requiring compact PCB integration.

Yamaichi Electronics

yamaichi.de



CA



A.P.E. TRIDENT AND INTRUDER REWORK STATION CAMERA OPTIONS

Trident benchtop rework station adds optional top-mounted monitor and freestanding camera configurations to improve visibility during SMT and BGA rework. Intruder hot-air BGA rework station adds a monitor capable of switching between split-vision and side-angle camera views and features a repositioned top-mounted computer monitor. Both systems support component removal and replacement in precision rework applications.

A.P.E.

ape.com



BTU AURORA VACUUM REFLOW OVEN

Aurora Vacuum reflow oven supports high-volume, low-void electronics assembly with a 24-inch vacuum chamber accommodating PCBs up to 24.4 × 28 inches and dual-lane production. Features soft-start vacuum control, an

independently heated vacuum chamber, low-vibration conveyor and vacuum systems and three independent conveyors. 125N50 configuration includes 10 heated zones before the vacuum chamber, three heated chamber zones, two internal panel heaters and four controlled cooling zones.

BTU

btu.com



COUNT ON TOOLS 2026-5679 CUSTOM DX S1 BASE

2026-5679 custom DX S1 base supports specialized Fuji pick-and-place applications. Features a spring-loaded nozzle shaft, 8mm bellow suction cup, 16.05mm center spacing and ID dome clearance. Precision-machined to customer specifications for component handling and placement requirements not served by standard tooling.

Count On Tools

cotinc.com

DYMAX 9310 LIGHT-CURING ADHESIVE

9310 light-curing adhesive reinforces fine-pitch, leadless components on printed circuit boards, providing additional mechanical strength for assemblies exposed to vibration, thermal stress and other demanding conditions. Supports rapid curing for automated production and reduces component movement in automotive, industrial, medical, communications and consumer electronics applications.

Dymax

dymax.com



FUJI NXTR AND AIMEXR SMT PLACEMENT

NXTR and AIMEXR pick-and-place machines support large, heavy components for AI server and data center equipment. Handle components measuring up to 200 × 200mm and weighing 2.0kg in standard configurations. Support placement requirements for larger GPU, ASIC and HBM packages and co-packaged optics applications.

Fuji

fuji.co.jp



HAKKO FX-310 WAVE SOLDERING POT

FX-310 wave soldering pot features a two-piece architecture with a separate control module and flat-top design to accommodate larger printed circuit boards. Supports operating temperatures up to 380°C and includes NP01 Series nozzles, nitrogen input, leak detection, five programmable process presets and Ethernet connectivity. Enclosed solder pot reduces oxidation, while adjustable temperature, solder flow rate, flow duration and descent speed provide process control and repeatability.

American Hakko Products

hakkousa.com

SBF AUTOMATIC LABEL FEEDER

Automatic Label Feeder provides automated labeling of printed circuit boards and electronic components. Adapts to different production processes, with an enhancement adding automated labeling of glass vials for pharmaceutical,

laboratory diagnostics and fine chemical applications.

SBF AG

[sbf-ag.com](https://www.sbf-ag.com)

SBF INSPECT OPTICAL INSPECTION SYSTEM

INSPECT optical inspection system automates quality inspection following SMD assembly. Uses a high-resolution camera to capture assembled printed circuit boards and automatically identify fiducial marks and component positions and orientations. Reads standard barcode and 2-D code formats, automatically documents inspection results, retains calibration and operating data during updates and supports setup within minutes.

SBF AG

[sbf-ag.com](https://www.sbf-ag.com)



In Case You Missed It

Microwave Communication

“A Room-Temperature Cavity-Magnonic Source of Correlated Microwave Magnon Polariton Pairs”

Authors: Qiuyuan Wang, Aravind Karthigeyan, Chung-Tao Chou and Luqiao Li

Abstract: Correlated microwave photon sources are required for the development of quantum-limited sensing, signal amplification and communication. The devices typically have a millikelvin operating temperature, which limits their broader application. Here, the authors report a hybrid magnon–photon platform that is based on a printed-circuit-board microstrip resonator coupled to a yttrium iron garnet film and emits strongly correlated microwave signals at room temperature. The authors’ approach achieves non-degenerate excitations by coupling magnon modes simultaneously with two cavity photon modes. Through the magnon–photon interactions in the corresponding linear and nonlinear regimes, one input microwave photon splits into a pair of magnon polaritons that have distinct frequencies and maintain strong intermode correlations. The nonlinear magnon polariton dynamics exhibit true randomness and robust multichannel correlations, and the authors use the system to demonstrate microwave communication with reliable signal transmission through two noisy channels. (*Nature Electronics*, Aug. 19, 2026, <https://www.nature.com/articles/s41928-026-01689-y>)

PCB Recycling

“Kinetically Inert Covalent Adaptable Networks Enable Holistic Resource Recovery from High-Performance Printed Circuit Boards”

Authors: H. Hu, T. Song, X. Chen, *et al.*

Abstract: The massive accumulation of electronic waste (e-waste) globally demands sustainable strategies for printed circuit boards (PCBs), a goal currently hindered by the pervasive use of irreversibly cured epoxy resins. Here, a kinetically inert covalent adaptable network (CAN) is designed for recyclable high-performance PCB based on *gem*-dimethyl dithioketal (gTK) epoxy resins. The *gem*-dimethyl effect significantly enhances the stability of gTK bonds through steric hindrance, kinetically blocking undesirable acidolysis and heat-induced exchange reactions. The fabricated gTKPCB satisfies the demanding commercial specifications, exhibiting robust thermomechanical stability ($\sim 220^{\circ}\text{C}$), chemical resistance, and highly reliable electrical interconnection under long-term thermal conditions (105°C , 90 d). Crucially, gTKPCBs undergo oxidation-specific degradation in H_2O_2 solution, enabling the direct, nondestructive recovery of high-purity copper (99.5%) and glass fibers, and the degraded resins as adhesives. Life

cycle assessment confirms that this valorization approach significantly mitigates environmental impact compared to traditional metallurgical recovery processes. This work provides a powerful blueprint for sustainable transitions in the electronics industry and offers a holistic solution for e-waste recycling. (*Nature Communications*, Aug. 27, 2026, <https://www.nature.com/articles/s41467-026-77223-7>)

Surface Finishes

“Interfacial Reactions of Sn-19Bi-19In Solder on OSP and ENIG Surface Finishes During Thermal Aging”

Authors: Ju-Hyeon Kim, *et al.*

Abstract: This study investigates the interfacial reactions and mechanical properties of Sn-19Bi-19In (SBI) solder on OSP and ENIG finishes under isothermal aging at 85 °C for up to 500 h. The microstructure analysis of the SBI solders on the two surface finishes (OSP and ENIG) reveals that the intermetallic compound (IMC) morphologies of these SBI/OSP and SBI/ENIG joints are fundamentally distinct from those of conventional SAC solder joints. Our findings indicate that the high In concentration of SBI solder induces the formation of In-containing ternary IMCs [Cu₆(Sn,In)₅ for OSP and Ni(In_{0.3}Sn_{0.7})₂ for ENIG], which strongly contribute to the IMC morphologies. For the SBI/OSP joints, Cu₆(Sn,In)₅ IMCs form a rod-type structure, deviating from the typical scallop-type growth of SAC/OSP joints. Similarly, for the SBI/ENIG joints, Ni(In_{0.3}Sn_{0.7})₂ IMCs develop a stacked cuboid morphology, which is also different from that of conventional SAC/ENIG joints. The IMC thickness of the SBI joints on both finishes follows the parabolic relationship, indicating that the IMC growth proceeds through a diffusion-controlled reaction. The ball shear tests reveal that the SBI/OSP joints undergo a ductile-to-brittle transition of the fracture mode with aging, whereas the SBI/ENIG joints exhibit brittle fracture for all aging conditions and their maximum shear strength decreases after prolonged aging. The fracture analysis of the sheared SBI/ENIG joints reveals that this strength decrease appears closely related to the shift of the fracture location toward the IMC/Ni₃P interface. These findings provide a basis for understanding the interfacial reliability of Sn-Bi-In solder joints on different surface finishes. (*Journal of Electronic Materials*, vol. 37, no. 1905, Aug. 27, 2026, <https://link.springer.com/article/10.1007/s10854-026-18298-2>)

Thermal Management

“Spatiotemporal Mapping of Anisotropic Thermal Transport in Gan Thin Films Via Ultrafast X-ray Diffraction”

Authors: Thanh Nguyen, *et al.*

Abstract: Efficient thermal management is essential for the reliability of modern power electronics, where increasing device density leads to severe heat dissipation challenges. In thin-film systems, however, thermal transport is often compromised by interfacial resistance and microscale defects introduced during synthesis or transfer, which are difficult to characterize using conventional techniques. Here the authors present a noncontact, spatiotemporal-resolved ultrafast x-ray diffraction method to extract in-plane thermal conductivity and thermal boundary conductance, using GaN thin films on silicon as a model system. By tracking the pump-induced lattice strain, they

reconstruct the lateral heat flow dynamics and quantitatively probe thermal transport near a wrinkle defect. This study uncovers pronounced asymmetric heat dissipation across the wrinkle, with a four-fold reduction in the local thermal conductivity near the wrinkle and a 25% drop in interfacial conductance. The work demonstrates that ultrafast x-ray diffraction can serve as a precise thermal metrology tool for characterizing heat transport in multilayered thin-film structures for next-generation microelectronic devices. (*Nature Communications*, Jul. 29, 2026, <https://www.nature.com/articles/s41467-026-75414-w>)

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