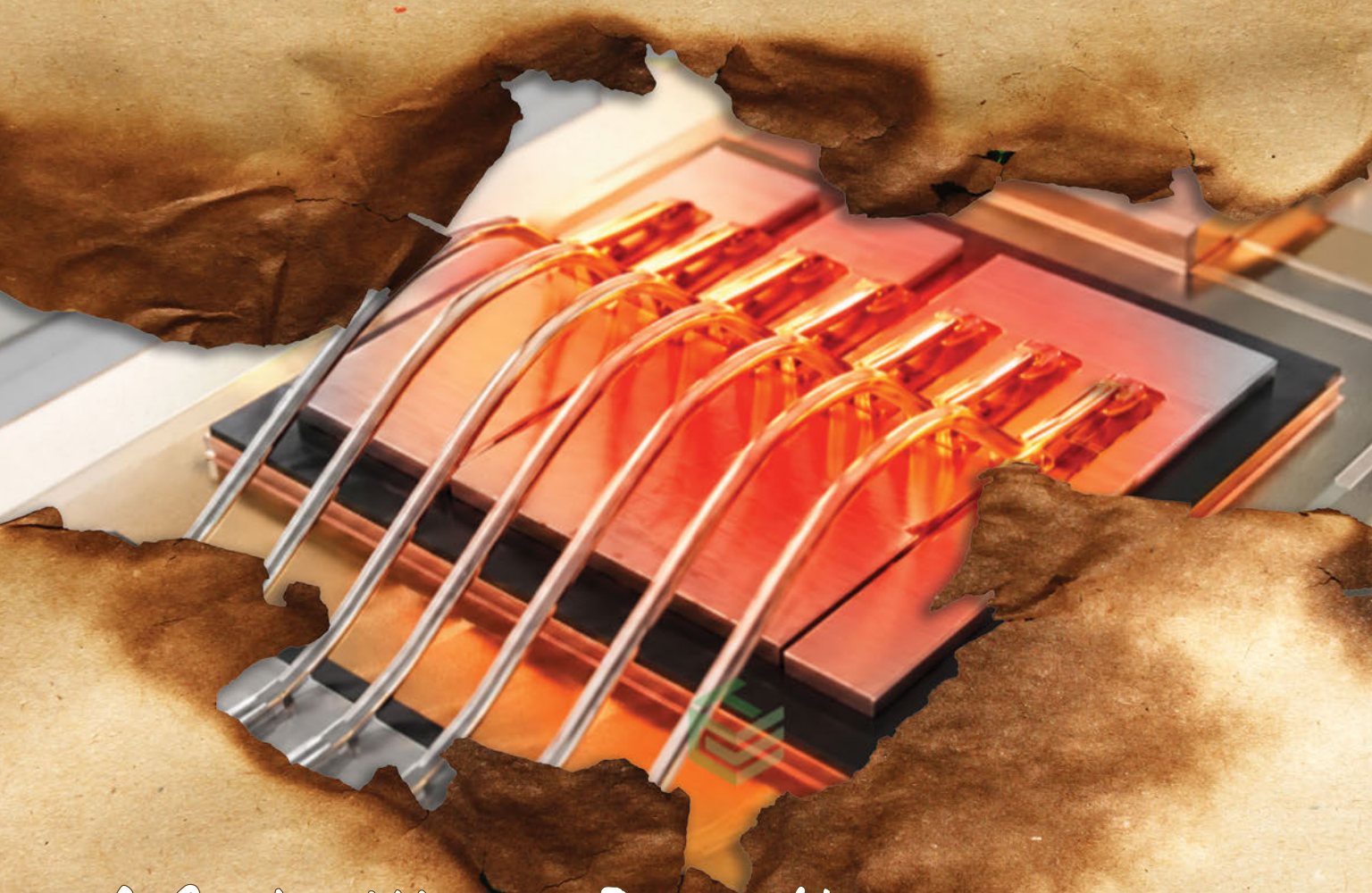
PCEA
PRINTED CIRCUIT ENGINEERING ASSOCIATION

Bigelow: Bringing Manufacturing Back to the Future

PRINTED CIRCUIT DESIGN & FAB

CIRCUITS ASSEMBLY

pcdandf.com
circuitsassembly.com
November 2026



A Cooler Way to Power Up

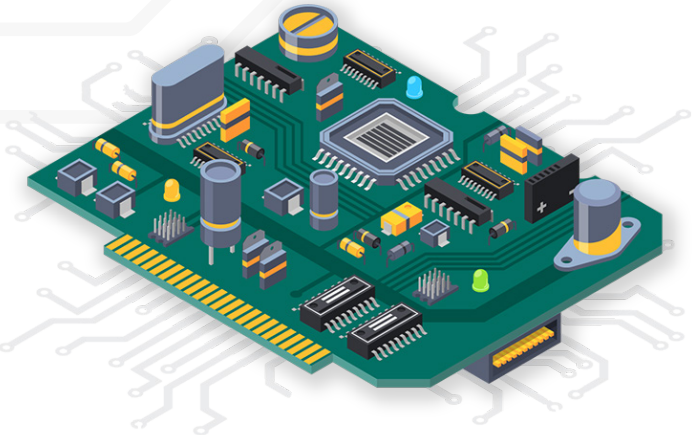
Spreading the Heat

Strengthening Connector Integrity

Tracing Hidden Interference

This issue of PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is brought to you by:

Instant FULL TURNKEY PCB Quote



PCB Trace provides instant quotes on multiple sets of quantities within minutes.

Visit pcbtrace.com and get a **$1500** discount.

Click to learn more

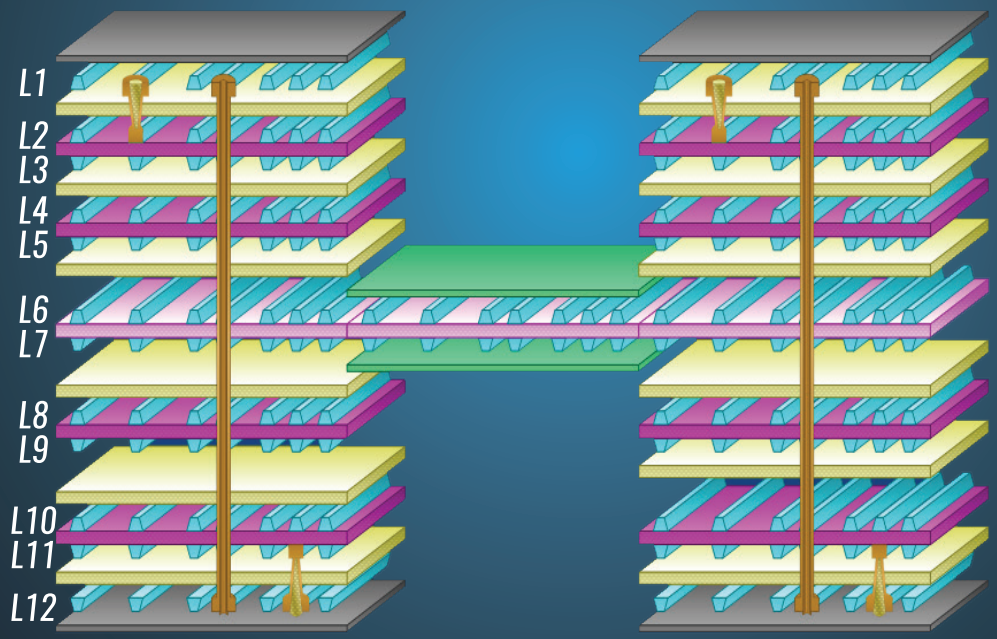
PCB TRACE
20 YEARS OF MANUFACTURING EXPERIENCE WITH BLIND AND BURIED VIAS, RIGID FLEX & FLEX PCB

RUSHPCB

20 YEARS OF MANUFACTURING EXPERIENCE WITH BLIND AND BURIED VIAS, RIGID FLEX & FLEX PCB ELECTRONIC DESIGN, & QUICK TURN CIRCUIT BOARDS, ASSEMBLY & FULL TURNKEY

Multilayer PCB Stackup

12 Layer Flex Rigid, 0.030" Thick Rigid, 0.008" Thick Flex
Blind Via L1-L2 & L11-L12, 0.003" Hole, Resin Filled,
0.002"/0.002" Trace/Space, Controlled Impedance



Manufactured on August 2016

When you're in a rush call RUSH PCB

Affordable Pricing ★ Satisfaction Guarantee ★ Fast Response ★ Free Quote ★ Fast Shipping
HDI Boards ★ Stacked Micro Vias ★ 2 mil line & Space ★ Flex & Rigid Flex

Located in the Silicon Valley
PCB up to 12 Layers in 3 days
PCB Assembly Same Day Turn
Full Turnkey Service

Certified: ISO9001/ITAR/UL

www.rushpcb.com | Sales@rushpcb.com | 1 408 496 6013
Rush PCB Inc, 2149-20 O'Toole Ave, San Jose, CA 95131, U.S.A

NOVEMBER 2026 • VOL. 43 • NO. 11

PRINTED CIRCUIT DESIGN & FAB CIRCUITS ASSEMBLY

FIRST PERSON

CAVEAT LECTOR
Hyperscalers are eating our laminate.
Andy Shaughnessy

MONEY MATTERS

ROI
A mission plan for reshoring.
Peter Bigelow

BOARD BUYING
Plan now for Chinese New Year.
Greg Papandrew

FOCUS ON BUSINESS
Say what you mean by NPI.
Jake Kulp

TECH TALK

DESIGNER'S NOTEBOOK
It pays to be nice.
John Burkhert, Jr.

ECAD TIPS & TRICKS
De-embed DC resistance.
Martyn Gaudion

DESIGN BEST PRACTICES
Good habits make design scalable.
Stephen V. Chavez

MATERIAL GAINS
Reindustrializing for the age of AI.
Alun Morgan

DATA TRANSFER
By the industry, for the industry.
Hermant Shah

GETTING LEAN
Lean works in high-mix, too.
Rob Rowland

SEEING IS BELIEVING
Don't blame the test engineer.
Robert Boguski

TECHNICAL ABSTRACTS

DEPARTMENTS

AROUND THE WORLD

PCEA CURRENT EVENTS

MARKET WATCH

OFF THE SHELF

FEATURES

PROTECTION DECISIONS

Selecting Via Protection for PCB Design and Manufacturing
Selecting the right via protection method requires balancing design requirements, material properties, assembly reliability and manufacturing costs.
by AKBER ROY

CONNECTOR INTEGRITY

Layout and Connector Footprint Strategies for Industrial EMC and Signal Integrity
Connector footprint design plays a critical role in electromagnetic compatibility and signal integrity, with return paths, shielding and grounding strategies helping ensure reliable performance in industrial electronics.
by DENNIS CHIANG

HIDDEN INTERFERENCE

Stackup Decisions That Prevent EMI Problems Later
A seemingly harmless low-speed feedback trace caused an 18dB emissions failure, demonstrating why stackup reviews must account for high-impedance nets and return paths.
by UJJWAL DATT SHARMA



EMBEDDED POWER (COVER STORY)

Embedded Die Substrate Technology
Embedded die substrate technology combines thick copper heat spreaders, sintered silver die attach and copper microvias to improve thermal management, reduce parasitic inductance and increase switching performance in wide-bandgap power electronics.
by CHRIS PARKER

MANUFACTURING INTELLIGENCE

Manufacturing's Next AI Wave: Notes from the Frontier
See how the emerging AI manufacturing landscape could transform electronics manufacturing operations through intelligent automation, data integration, and decision-making tools.
by SHIRIN KHANNA

ELECTRONIC EVOLUTION

The Electron: A Biography, Part 2: From the Vacuum Tube to the Data Center
From early radio and television assembly to surface mount technology and AI data centers, the evolution of electronics manufacturing reveals how innovation, miniaturization and automation have transformed the industry.
by RONALD C. LASKY, PH.D.

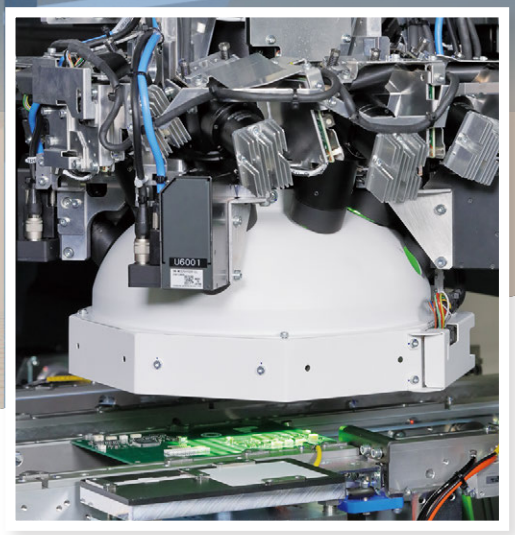
ON PCB CHAT (PCBCHAT.COM)

PCB Chat

FINDING YOUR PLACE IN PCB DESIGN with MIROSLAVA VELASCO

A Printed Circuit Engineering Association, Inc. publication. All rights reserved.

REDUCE PROGRAMMING TIME AND DEFECTS WITH YAMAHA'S AI ENHANCED AOI





- Fastest 3D Automated optical inspection on the market today!
- Resolution for narrow pitch 0201mm devices.
- New co-axial lighting system for finding defects on reflective surfaces.
- AI Automatic Secondary Inspection reduces false call rates and operator interaction
- AI Based **Automatic Data Generation and Auto Component Programming** dramatically reduces the time to create new inspection tasks.

SCAN THE QR CODE® FOR MORE INFO
Messaging and data rates may apply.



Yamaha can meet the challenges of almost any product that is on the market today.

DON'T MISS THE OPPORTUNITIES FOR THESE NEW TECHNOLOGIES!

Learn more at www.yamaha-motor-im.com
For inquiries: y-sales@yamaha-motor.com

YAMAHA
Revs Your Heart

PCEA®
Printed Circuit Engineering Association

PCEA
PO BOX 237
PORTSMOUTH, NH 03802

PRINTED CIRCUIT DESIGN & FAB
pcdandf.com
circuitsassembly.com
CIRCUITS ASSEMBLY

PCEA BOARD OF DIRECTORS
ANAYA VARDYA, CHAIRMAN
MATTHEW LEARY, VICE CHAIRMAN
JUSTIN FLEMING, SECRETARY
DOUG DIXON, TREASURER

MEMBERS
Jim Barnes
Michael Buetow
Stephen V. Chavez
Tomas Chester
Juan Frias
Richard Hartley
Charlene McCauley
Susy Webb
Eriko Yamato

PCEA.NET

THE PRINTED CIRCUIT ENGINEERING ASSOCIATION, INC. BRANDS:

PUBLICATION
PCD&F/Circuits Assembly ..... digital.pcea.net

WEBSITES
PCD&F ..... pcdandf.com
Circuits Assembly ..... circuitsassembly.com

NEWSLETTER
PCB Update ..... pcbupdate.com

PODCASTS
PCB Chat ..... pcbchat.com

EVENTS
PCB West ..... pcbwest.com
PCB East ..... pcbeast.com

EDUCATION
PCEA Training ..... pceatraining.net
Printed Circuit University ..... pcea.net/pcu

AWARDS PROGRAMS
Service Excellence Awards ..... pcea.net/sea-awards
NPI Awards ..... pcea.net/npi-awards

MANAGEMENT
PRESIDENT
Mike Buetow 617-327-4702 | mike@pcea.net
VICE PRESIDENT, SALES
Brooke Downey 404-316-9018 | brooke@pcea.net
SENIOR DIRECTOR, STRATEGIC ACCOUNTS
Frances Stewart

PCD&F/CIRCUITS ASSEMBLY EDITORIAL
MANAGING EDITOR
Ryann Howard 912-803-9780 | ryann@pcea.net
CONTENT ARCHITECT
Andy Shaughnessy 770-315-9901 | andy@pcea.net

COLUMNISTS AND ADVISORS
Jeffrey Beauchamp, Dan Beaulieu, Peter Bigelow, Robert Boguski, John Burkhert, Jr., Stephen V. Chavez, Mark Finstad, Nick Koop, Jake Kulp, Alun Morgan, Susan Mucha, Greg Papandrew, Hemant Shah, Chrys Shea, Jan Vardaman, Gene Weiner

PRODUCTION
ART DIRECTOR & PRODUCTION
blueprint4MARKETING, Inc. | production@pcea.net
Nathan Hoeller | nathan@pcea.net

SALES
VICE PRESIDENT, SALES
Brooke Downey 404-316-9018 | brooke@pcea.net
SENIOR SALES EXECUTIVE
Will Bruwer 404-313-1539 | will@pcea.net

EVENTS/TRADE SHOWS
EXHIBIT SALES
Brooke Downey 404-316-9018 | brooke@pcea.net
TECHNICAL CONFERENCE
Mike Buetow 617-327-4702 | mike@pcea.net
WEBINARS
Andy Shaughnessy 770-315-9901 | andy@pcea.net
EVENTS MANAGEMENT
Leah Spinks 912-239-7730 | leah@pcea.net

PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is distributed without charge to qualified subscribers. To subscribe, visit pcdandf.com or circuitsassembly.com and click on Subscribe. For changes or cancellations to existing subscriptions: subscriptions@pcea.net

PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is published monthly by Printed Circuit Engineering Association, Inc., PO Box 237, Portsmouth, NH 03802. ISSN 1939-5442. GST 124513185/ Agreement #1419617.

© 2026, Printed Circuit Engineering Association, Inc. All rights reserved. Reproduction of material appearing in PRINTED CIRCUIT DESIGN & FAB/ CIRCUITS ASSEMBLY is forbidden without written permission.

Built for change.



The world is constantly changing. Now faster than ever. From rapid tech shifts to climate pressure. From geopolitical uncertainty to new production methods. Today, stability comes from agility. That means having a supply chain that can adapt to your needs – fast. And PCB production is no exception.

NCAB is built for change. For over 30 years, we have been producing PCBs and taking full responsibility – without owning any factories. Instead, we constantly source, qualify and develop the most optimal ones across three continents. And we only use them where they excel.

In other words – you will always have more than one option for your PCB production. So when things change, you can too. Fast.

Reliable PCBs. Resilient supply chain.

Read more here:
www.ncabgroup.com

NCAB GROUP

Honey, the Hyperscalers Ate My Laminate

AS DR. HAYAO NAKAHARA reported in his NTI-100 rankings last month, the 10 largest fabricators are focusing primarily on creating products for data centers. Data center PCBs are monopolizing more and more of the industry's advanced materials and components that readers like you need.

Now, Nittobo, the weaver that makes most of the world's T-glass specialty cloth, plans to triple its capacity to meet this demand, and laminate maker Kingboard has a six-month wait time for some high-end products after raising prices eight times this year.

TPCA believes there will be a tight market for these advanced materials and memory through at least 2027. But, as Naka pointed out, some cynical analysts believe we will see overcapacity in a few years, followed by a glut.

Our entire industry seems to have been caught flat-footed here. But consider this: Even five years ago, data centers were barely on our radar screen.

I first encountered the data center donnybrook in 2024, when I was dating a teacher who lived near the QTS data center in Fayetteville, GA, in metro Atlanta.

She had a bee in her bonnet regarding QTS. She said the project was pushed through by city and county officials in closed-door sessions in violation of state laws (it wasn't), and that it would cause everyone around to get cancer or have deformed children (pretty unlikely).

To its credit, some elements of this facility are environmentally enviable. The site's closed-loop cooling system, for instance, recycles water continuously, and the only water consumption is from restrooms and break rooms. It has almost no effect on the water grid.

But the power grid is another story. Leased by Microsoft and OpenAI for model training, the site is custom-built for ultra-high-density AI compute clusters, and it uses more power per square foot than a typical cloud data center.

When it's fully operational, the 6.2 million square-foot facility will consume 5 to 6 terawatt-hours of electricity per year, enough to power half a million average US homes for a year. The maximum power draw is 700 megawatts.

One day we drove to the data center so I could see what the fuss was about. It's a sprawling complex of 13 buildings on 600 acres. And you can hear the humming a half mile away. I think it would be great for sleeping.

But my girlfriend acted like we were standing outside the factory in *Soylent Green*. Her fears didn't ease when I

mentioned that QTS had to follow FCC emissions regulations and that standing in front of a data center wouldn't take years off our lives.

Still, she and her neighbors remain hyperfocused on hyperscalers. In response, Fayette County points to the economic upside: Once the QTS site is fully built out, it will bring in about $350 million annually in real estate and sales tax revenue.

County commissioners believe this data center will help the county offset the economic loss from Marvel's movie production, which recently moved from Fayetteville to the UK.

Hundreds of movies and TV shows, including *The Walking Dead* and *Ozark*, have been filmed in the business-friendly Peach State, which actors have dubbed "Y'allywood."

Likewise, we've seen this movie before. Today's data centers are what we called server farms during the dot-com boom of the late 1990s and early 2000s. That episode ended with reams of unneeded equipment being scrapped and physically destroyed or salvaged via brokers. It took years for many suppliers to dig out from the capacity glut.

Data centers are here to stay. We live in a data-collection world, and we are still in the early stages of tapping into how to understand and utilize all that information.

Perhaps this time we will unlock enough of the supply chain secrets to turn off the capacity builds just before the inevitable peak is crested.



ANDY SHAUGHNESSY is content architect of PCD&F/Circuits Assembly; andy@pcea.net.

HELLER INDUSTRIES

Low Void Soldering
Maximized Throughput



Short Cycle Vacuum Reflow

Smooth Profile
Heated Vacuum Chamber
for Flexible Manufacturing

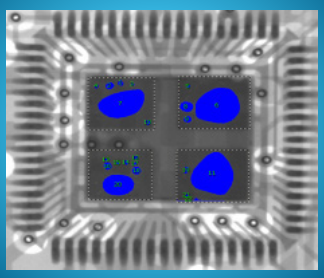
Low Void
Vacuum Closed-Loop
Stepped Control for Improved Quality

Exclusive Patent
Innovative Multi-Stage
Speed-Adjustable Conveyor System

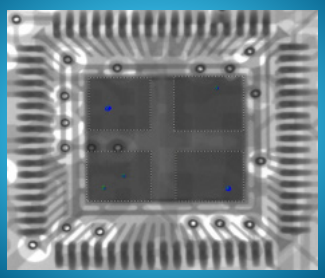
Doubled Throughput
Achieve the Shortest Cycle
Time to Up Your Production

Reliable Vacuum Design, Achieve < 1% Void

Normal Reflow



Vacuum Reflow



HELLER INDUSTRIES

4 Vreeland Road, Florham Park, New Jersey 07932, USA
Tel: +1-973-377-6800
E-mail: info@hellerindustries.com
More products can be found on our website: www.hellerindustries.com

Amphenol to Acquire AdvancedPCB

WALLINGFORD, CT – Amphenol has signed a definitive agreement to acquire AdvancedPCB, a leading US manufacturer of printed circuit boards for the defense and industrial markets.

Colorado-based AdvancedPCB is expected to have full-year 2026 sales of approximately $270 million and will be included in the company's Harsh Environment Solutions segment post-closing. Amphenol and AdvancedPCB combined will have estimated printed circuit board sales of about $500 million.

The acquisition is expected to close in the fourth quarter, subject to customary regulatory approvals and other closing conditions. Amphenol, which is also buying Dexgreen, Empire Electronics and Humanetics Sensors, said the aggregate price paid for all the companies will be $1.6 billion.

PCB Technologies to Acquire Gorilla Circuits for $120M

SAN JOSE, CA – PCB Technologies Ltd. has signed a definitive agreement to acquire Gorilla Circuits for an enterprise value of $120 million, financed by credit facilities from two Israeli banks.



Gorilla Circuits' facility in San Jose, CA.

Gorilla has operated in San Jose for more than 20 years and employs more than 320 people. It provides high-mix, low-volume PCB fabrication and assembly to more than 700 active customers, mainly in semiconductor test, technology and aerospace and defense.

The deal will give PCB Technologies its first US manufacturing base and let it bid on contracts that require onshore fabrication. It requires regulatory approval, including from CFIUS, and is expected to close within eight months of the Oct. 8 announcement.

TTM Technologies Completes $1.1B Acquisition of Epiq

SANTA ANA, CA – TTM Technologies has completed its acquisition of Epiq Design Solutions LLC for $1.1 billion in cash, subject to customary closing adjustments.

Epiq supplies open-architecture, AI-enabled software-defined radios, high-performance RF products and radiation-tolerant space compute products for signals intelligence and electronic warfare. The business complements TTM's RF and mission systems portfolio and supports its vertical integration strategy across land, air, sea and space applications in the aerospace and defense market.

Kyzen Opens Southeast Asian Headquarters in Penang

PENANG, MALAYSIA – Kyzen has opened a Southeast Asian headquarters and production facility in Penang.



Kyzen executives and Malaysian government officials at the grand opening of Kyzen's new Southeast Asian headquarters in Penang.

The site is designed to increase production capacity, improve delivery times and expand technical support for customers in Malaysia and the wider Asia-Pacific region. It also adds administrative space and strengthens the

company's regional supply chain.

The cleaning chemistries supplier has operated in Penang for more than 16 years and will continue to offer its chemistries and lab services from the new facility.

Toppan Opens First Overseas FC-BGA Substrate Plant

SINGAPORE – Toppan has established its first FC-BGA substrate production site outside Japan at Advanced Substrate Technologies Pte. Ltd. (AST) in Singapore, with support from the Singapore Economic Development Board and Broadcom. An opening ceremony was held on Sept. 29.

The plant has about 95,000 sq. m. of total floor area, with about 70,000 sq. m. in phase 1. It will focus on large, high-layer-count substrates for generative AI, machine learning and large-scale network switches. Operations are set to start in December, and the site had 315 employees as of the end of September.

Toppan previously concentrated FC-BGA production at its Niigata plant in Japan. The company aims to raise its FC-BGA production capacity to at least 2.5 times its fiscal 2022 level by the end of fiscal 2027.

Rapidise to Invest $22M to Quadruple Manesar Capacity

MANESAR, INDIA – Rapidise will invest about $22 million over three years to quadruple its electronics manufacturing capacity in Manesar.

The expansion adds a 120,000-sq.-ft. facility in Sector 8 to the company's existing 40,000-sq.-ft. site in Sector 3. The plan includes 10 SMT lines along with automated manufacturing systems and digital production tools. A newly commissioned dual-lane SMT line brings total placement capacity to about 800,000 components per hour.

The company serves automotive, consumer electronics, telecom, security, networking, healthcare and agriculture customers. It plans to expand into server and AI hardware, defense and railways, and expects the expansion to create about 1,000 direct and indirect jobs during fiscal 2027.

Amazon to Invest Nearly $50M in Gold Circuit Electronics

TAIPEI, TAIWAN – Amazon.com will invest about $50 million in Taiwanese PCB manufacturer Gold Circuit

Electronics through a private placement approved by the Gold Circuit board on Sept. 29.

Amazon, already a Gold Circuit customer, will buy about 1.86 million newly issued common shares at NT$856 each. Gold Circuit makes high-end multilayer PCBs for servers and counts Amazon Web Services, Microsoft and Google among its customers.

Gold Circuit's board also approved a $7.9 billion budget for land and a new plant, to be invested in stages starting in the fourth quarter and funded by convertible bonds.

CSI Sud-Ouest Inaugurates Rebuilt Toulouse PCB Plant

TOULOUSE, FRANCE – CSI Sud-Ouest, a subsidiary of Cimulec, inaugurated its rebuilt PCB plant in Toulouse on Sept. 29, two years after an arson fire destroyed much of the site.



The inauguration of CSI Sud-Ouest's rebuilt PCB plant in Toulouse.

The July 2024 fire destroyed 2,000 sq. m. of the site along with its production equipment. Reconstruction cost €25 million ($28 million), with the French government and the Occitanie region covering about €5 million left uncovered by insurance through the France 2030 program.

CSI kept all 57 employees through short-time work, remote work and temporary assignments, and it regained its 300 customers.

Wistron Approves $150M Investment in US Subsidiary

TAIPEI, TAIWAN – Wistron's board of directors has approved an additional $150 million capital injection into its wholly owned subsidiary Wistron InfoComm (USA) Corp.

The funds will cover facility improvements, machinery and equipment at the company's Westport (D2) plant in Texas, with capital expenditure capped at $146 million.

The board also approved up to $59.1 million for facility upgrades and equipment at Wistron InfoComm (Vietnam) to support its server business, plus a Dallas facility lease for subsidiary SMS Infocomm to support after-sales service.

ICTC Acquires Trinity Manufacturing

BROOKSVILLE, FL – Interconnect Cable Technologies Corp. has acquired Trinity Manufacturing Corp., a cable and wire harness manufacturer based in Bradenton, FL.

The acquisition expands ICTC's domestic manufacturing footprint and US production capacity. It also strengthens its ground support wire harness and electronic box-build capabilities. ICTC is a global contract manufacturer of cable and wire harnesses, PCB assemblies and electronic box builds. Terms were not disclosed.

Draper Breaks Ground on Microelectronics Center

LOWELL, MA – Draper broke ground Oct. 6 on a 111,000-sq.-ft. building that will house its Integrated Microelectronics Production & Advanced Chip Technology (IMPACT) Center.

The center is in the Hamilton Canal Innovation District, part of the Lowell Innovation Network Corridor (LINC) linking the UMass Lowell campus with downtown. It will provide high-mix, low-volume manufacturing, including advanced chip packaging and precision navigation and timing systems.

The project is expected to create more than 100 jobs and is supported in part by state and local funding. Wexford Science & Technology is the developer.

Xi Electronics Acquires C.J. Rogers Electronics

ORANGE, CA – Xi Electronics LLC has acquired C.J. Rogers Electronics, a Southern California contract electronics manufacturer.

C.J. Rogers operated for more than 50 years under founder Carol Rogers, who is retiring. The company will operate as Xi Electronics, and the C.J. Rogers team will remain.

Xi Electronics provides SMT and through-hole PCB assembly, mixed-technology assembly, prototyping, NPI support and production manufacturing. The company plans to invest in advanced equipment, automation, quality systems and expanded manufacturing capabilities.

SEL Invests $25M to Expand West Lafayette Operations

WEST LAFAYETTE, IN – Schweitzer Engineering Laboratories will invest $25 million to expand manufacturing at its West Lafayette facility in the Purdue Discovery Park District, with completion expected in March 2027.

SEL will add SMT, electronic assembly and conformal coat production lines, bringing PCB assembly capabilities to the site. The expansion will raise recloser control production capacity by more than 35% and create about 130 jobs.

The project is part of more than $500 million SEL plans to invest in US manufacturing from 2026 to 2028, including more than $70 million for a new 305,000-sq.-ft. electronic device manufacturing facility in Moscow, ID.

Samsung to Invest $4B in Vietnam Chip Testing

THAI NGUYEN, VIETNAM – Samsung Electronics plans to invest about $4 billion in memory chip testing facilities at Yen Binh Industrial Park in northern Vietnam. The first production line is set to start in the fourth quarter of 2027, with another planned for 2028.

The facilities will perform final testing of DRAM and NAND chips packaged at Samsung's Cheonan plant in Korea and will not make wafers. About 63% of the funding will come from reinvested profits of Samsung's Vietnamese operations.

Separately, Samsung Electro-Mechanics plans to invest $4.7 billion in FC-BGA substrates. That total includes $2.9 billion in Sejong, Korea, targeting mass production in September 2028, and $1.7 billion in Vietnam, targeting June 2030.

Amber Subsidiary Takes Full Ownership of

Ascent Circuits

BANGALORE, INDIA – IL JIN Electronics (India), a subsidiary of Amber Enterprises India, has agreed to acquire the remaining 1.5% stake in PCB maker Ascent Circuits, making Ascent a wholly owned subsidiary.

Founded in 1999, Ascent makes single-sided, double-sided, multilayer and RF PCBs for aerospace and defense, medical, automotive, telecom and data center markets. IL JIN raised its Ascent stake from 60% to 98.5% in June.

Microart Consolidates Markham Operations in Expanded Facility

MARKHAM, ON – Microart Services has consolidated its Markham operations into an expanded 100,000-sq.-ft. facility. As part of the move, Microart added SMT buffers and an additional wave-soldering system.

Microart provides electronics manufacturing services. It previously operated a 42,000-sq.-ft. main facility and a 20,000-sq.-ft. support building in Markham.

Microscreen Opens Baltimore Manufacturing Facility

BALTIMORE, MD – Microscreen has opened a manufacturing facility in Baltimore, its third US manufacturing site and its second new location this year.



Microscreen's new manufacturing facility in Baltimore.

The facility will produce laser-cut production and step stencils and offer MicroGlide and MicroGlide Platinum nanocoatings. Equipment includes Watt Laser Nevis and SE12 systems and a proprietary robotic nanocoating system.

The Baltimore site joins Microscreen's longtime headquarters in South Bend, IN, and a recently opened facility in Oxford, CT. Founded in 1981, Microscreen makes SMT solder stencils and custom tooling.

Amber Takes Full Control of Power-One Micro Systems

BANGALORE, INDIA – IL JIN Electronics (India), a subsidiary of Amber Enterprises India, has agreed to acquire the remaining 40% stake in Power-One Micro Systems, making it a wholly owned subsidiary.

Power-One makes solar inverters, UPS systems, battery energy storage systems and EV chargers. It joins PCB assembly and bare-board operations in Amber's electronics business as the group moves beyond air conditioner boards into higher-value electronics.



Reliability Is Engineered. . . Not Assumed!

Reliable electronics begin with understanding where designs are vulnerable. From accelerated stress testing to environmental qualification and electrical measurement, ESPEC helps engineers uncover weaknesses, evaluate performance, and improve product robustness.







DESIGN

Design for Reliability
Find Weaknesses Early

HALT

QUALIFY

Validate Reliability
Environmental Testing
+ Real Time Electrical
Measurement

(AMI • AMR • AEM)

PRODUCE

Screen for Consistency,
Identify Manufacturing
Defects and Variation

HASS

Scan to explore reliability testing solutions for PCB, electronics, and semiconductor applications.

Quality is more than a word

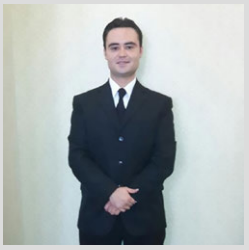
ESPEC

PCDF


Dr. Meredith LaBeau


Robert Toohey


Jeff Mason


Nicolas Martinez


Keven Coates


Elias Wheatfall

Calumet Electronics named **Dr. Meredith LaBeau** president and CTO.

Celestica named **Robert Toohey** printed circuit board design engineer.

Fabric8Labs named **Jeff Mason** vice president of manufacturing.

Motion Applied named **Nicolas Martinez** senior PCB designer.

Siemens named **Keven Coates** technical marketing engineer.

SpaceX named **Elias Wheatfall** lead supplier development engineer.

CA



Hytham Gadallah



Kevin Kendrick



Dave Barnett

Gradian named **Hari Prasad** India managing director.

Microboard promoted **Hytham Gadallah** to operations manager.

Micro-Precision Technologies appointed **Kevin Kendrick** vice president of sales.

Vergent Products promoted **Chris Johnson** to associate quality engineer.

ZTest Electronics named **Dave Barnett** president and CEO.



WHEN IT HAS TO WORK, THINK AXIOM ELECTRONICS

Quality isn't just a metric at Axiom Electronics. For many of the complex PCBAs and subassemblies we work on, failure is not an option. We provide customers with a complete electronics manufacturing services solution which includes:

- Robust NPI process ensuring all requirements are identified before project start
- DFX recommendations
- Support for prototype, pilot and production builds
- In-house automated conformal coating
- Supply chain management
- Automated traceability
- Industry-leading process control
- Comprehensive inspection and test

We are able to build to virtually any standards and specifications you choose. From Earth to Mars, our manufacturing expertise is helping our customers deploy mission critical products.

If you are looking for an EMS supplier expert in supporting the rigorous quality and device history recordkeeping requirements found in medical device manufacturing, give us a call at **503-643-6600** or visit our website at **www.axiomelectronics.com.**

Axiom Electronics

To learn more about our manufacturing processes download our latest whitepaper, *"Key Areas to Audit When Selecting a Contract Manufacturer"* at **www.axiomelectronics.com/ads.**

PCB West 2026 Conference Registration Grows 60%

PEACHTREE CITY, GA – Registration for the technical conference at the PCB West conference and exhibition held in the Silicon Valley last month grew 60% year-over-year. Overall attendance for the sold-out exhibition rose 15% from 2025.

The annual event was held Sept. 28 to Oct. 2 at the Santa Clara (CA) Convention Center. The audience of engineers and other professionals from a range of printed circuit and electronics design, fabrication, assembly and advanced packaging companies represented almost the entire US and more than 30 countries.

“This was likely the best PCB West in more than 20 years,” said Mike Buetow, president, PCEA. “We heard great reports from exhibitors about the number and quality of leads, and the energy among the conference attendees was off the charts.

“A special thanks to our sponsors, including Allspice, ASC Sunstone, Cofactr, Cadence/EMA Design Automation, NextPCB, Polar Instruments, Screaming Circuits, and Zenode,” he added.

Conference registrants and exhibitors were effusive in their praise of the access to experts and attendance on the show floor.

“The material shared during PCB West was truly exceptional,” said Joaquin Martinez, electrical system design engineer at Spectrolab. “The speakers were highly knowledgeable and genuinely enthusiastic.”

“PCB West was phenomenal. Our booth was bustling, and I could barely leave it all day,” added Kenneth Chang, chief of staff, JITX.

“As always, we learned a ton, got a pulse on the industry, met great new people, and had a great time. It was everything you are looking for in a show,” said Matt Leary, cofounder, Newgrange Design.

The exhibition featured more than 110 leading suppliers to the electronics design and manufacturing industry.

The 2027 show will be held Sept. 14-17 in Santa Clara.

CIRCUITS ASSEMBLY Announced 2026 Service Excellence Winners

PEACHTREE CITY, GA – CIRCUITS ASSEMBLY last month announced the winners of its 34th annual Service Excellence Awards (SEA). The awards, presented during a ceremony at PCB West in Santa Clara, CA, recognize electronics manufacturing services (EMS) providers and their equipment, materials, software and service suppliers for outstanding customer service.



Unlike most industry honors, the SEA program is based entirely on direct, verified feedback from each entrant's own customers rather than editorial judging. Respondents rate participating companies across seven service dimensions: Dependability/Timely Delivery, Manufacturing Quality, Responsiveness, Technology, Value for the Price, Flexibility and Overall Satisfaction. Every entrant, whether it wins or not, receives a confidential report detailing how its customers rated it.

Four EMS providers earned the highest overall customer rating in their respective revenue category, the program's top overall distinction:

- Creation Technologies (EMS revenues over $500 million)
- Mack Technologies (EMS revenues from $100 million to $500 million)
- Electronic Systems, Inc. (EMS revenues from $20 million to $100 million)
- Surf-Tech Manufacturing (EMS revenues under $20 million).



2026 Service Excellence Award winners – EMS category.

Kimball Solutions earned the highest customer rating in all seven service categories among EMS providers with revenues over $500 million: Dependability/Timely Delivery, Manufacturing Quality, Responsiveness, Technology, Value for the Price, Flexibility and Overall Satisfaction.

In the $100 million to $500 million tier, Emerald Technologies was rated highest in Dependability/Timely Delivery, Manufacturing Quality, Technology and Value for the Price, while Vexos took top honors in Responsiveness, Flexibility and Overall Satisfaction.

In the $20 million to $100 million tier, Absolute EMS swept all seven categories, and Microboard earned the highest rating in Flexibility.

Among EMS providers with revenues under $20 million, RBB earned the highest customer rating in all seven categories.

Twelve suppliers to the electronics assembly industry were also honored with the highest customer rating in their category:

- Anda Technologies USA – Coatings/Encapsulants
- Europlacer Americas – Screen Printing Equipment

- Europlacer Americas – Pick-and-Place Equipment
- KIC Thermal – Soldering Equipment
- Koki Solder America – Materials
- Kyzen – Cleaning
- Koh Young – Test and Inspection Equipment
- Optimum Design Associates (an Emerald Technologies company) – PCB Design Services
- PVA – Automation and Handling Equipment
- PVA – Dispensing
- The Test Connection – Test Laboratories
- Win-Source – Distributors



2026 Service Excellence Award winners – supplier categories.

“Every year the Service Excellence Awards reaffirm what our customers already know – that this industry’s best companies earn their reputations one satisfied customer at a time,” said Mike Buetow, president, Printed Circuit Engineering Association. “Congratulations to all of this year’s winners for the consistency and care that shows up in their own customers’ ratings. Just as important, I want to recognize every company that entered. Putting your

business in front of your own customers for an unfiltered verdict takes real confidence, and that willingness to be judged is itself a mark of service excellence. We're grateful to every entrant, and to the customers who took the time to respond."

Now in its 34th year, the CIRCUITS ASSEMBLY Service Excellence Awards is the electronics assembly industry's only awards program based solely on direct, verified customer feedback rather than editorial or judged criteria. EMS providers and suppliers of equipment, materials, software and services are rated by their own customers on dependability, manufacturing quality, responsiveness, technology, value, and flexibility. All entrants receive a confidential customer satisfaction report regardless of outcome.

Upcoming PCEA PCB Design Training Classes for 2027

PEACHTREE CITY, GA – PCEA Training announced its winter and spring 2027 schedule for the Certified Professional Circuit Designer (CPCD) training and certification program.

The instructor-led classes cover the gamut of printed circuit design engineering, from layout, place and route to specifications and materials to manufacturing methods. Schematic capture, signal integrity and EMI/EMC are also part of the comprehensive program.

Classes will be held on the dates below:

- Jan. 15, 22, 29, Feb. 5, 12 (online)
- Mar. 19, Apr. 2, 9, 16, 23 (online)
- Apr. 26-30 (in person in the Boston suburbs, at PCB East)

Each class is 40 hours long and includes a copy of *Printed Circuit Engineering Professional,* a 400-page handbook on circuit board design, and the optional certification exam.

There are no prerequisite requirements to enroll. The January and March classes will be held online via Zoom; the April class will be held in person in conjunction with PCB East. All courses are led by experienced instructors. Private corporate classes are also available on request, subject to instructor availability.

The course handbook, *Printed Circuit Engineering Professional,* was authored by Michael Creeden, Stephen Chavez, Rick Hartley, Susy Webb and Gary Ferrari, industry veterans who combined have more than 200 years' experience designing and building PCBs for all types of applications.

The course includes an optional certification exam recognized by the Printed Circuit Engineering Association (PCEA).

For information about the course overview, class format, and materials to prepare in advance for the class, visit pceatraining.net/course-overview.

To enroll, visit pceatraining.net/registration for the next available class or email pceatraining@pcea.net for additional information.

PCEA Announces 2027-28 Board of Directors

PEACHTREE CITY, GA – PCEA in late October announced its board of directors for the 2027-28 term. Anaya Vardya, CEO of ASC Sunstone, will serve as chairman, with Matthew Leary, president of Newgrange Design, becoming vice chairman.

Doug Dixon, chief marketing officer of 360 BC Group, is now treasurer. Returning as secretary is Justin Fleming.

The board sets the strategic direction of the association, which serves the printed circuit board design, fabrication and assembly community through its publications, conferences, and training and certification programs.

Also elected to the PCEA board for 2027-28 are:

- Jim Barnes, executive vice president – Global Supply Chain, Generac
- Stephen V. Chavez, principal technical product marketing manager, Siemens
- Tomas Chester, founder and hardware designer, Chester Electronic Design
- Juan C. Frias, staff PC board designer, Rivian
- Rick Hartley, founder, RHartley Enterprises
- Charlene McCauley, president, McCauley Design Group
- Susy Webb, senior PCB designer, DesignScience
- Eriko Yamato, OEM business development manager, Panasonic

“The board has done a phenomenal job of defining PCEA’s mission and path to collaborate, educate and inspire the current and next generation of printed circuit board designers and engineers,” said Mike Buetow, president, PCEA. “I am excited for the chance to continue working with them over the next two years.

“I am also grateful to Steph Chavez, our founding chairman, without whom the impressive strides we’ve made over the past five-plus years would not have been possible.”

“PCEA has built something valuable: a place where engineers across the full PCB lifecycle learn from each other,” said Vardya. “As incoming chair, my goal is to build on that foundation by bringing designers and fabricators closer together, supporting the next generation of engineers, and keeping our members ready for what’s coming next in electronics.”

PCEA Issues Call for Abstracts for PCB West 2027

PEACHTREE CITY, GA – Abstracts are now being accepted for the PCB West 2027 technical conference. The conference, the largest of its kind in Silicon Valley, focuses on training and best practices for printed circuit board designers and design engineers, electronics hardware engineers, fabricators and assemblers.

The four-day technical conference will take place September 14–17, 2027 at the Santa Clara (CA) Convention Center. The event includes a one-day exhibition on September 15.

Papers and presentations of the following durations are sought for the technical conference: one-hour lectures and presentations; two-hour workshops; and half-day (3.5-hour) and full-day seminars.

Preference is given to presentations of two hours in length or more, and no presentations of less than one hour will be considered.

Abstracts of 150-750 words and speaker biographies should be submitted to PCEA. Papers and presentations must be noncommercial in nature and should focus on technology, techniques or methodologies related to printed circuit board design, fabrication, assembly, test, components or packaging, and additive manufacturing.

Submit abstracts at pcbwest.com by January 8, 2027. No emailed abstracts will be accepted. Submitters will be notified by early April if their abstract has been accepted. Presentations are due August 13, 2027.

Speaker Benefits: Presenters of accepted abstract(s) for the 2027 program receive the following event benefits:

- Complimentary access to the online proceedings
- Complimentary pass to the technical conference
- Invitation to the Speaker/Exhibitor Reception.

PCEA **CURRENT EVENTS**

ASSOCIATION NEWS

PCB East 2027 booth sales are open. The one-day exhibition will take place Apr. 28, while the four-day

technical conference will take place Apr. 27 – 30. All events will be held at the DCU Center in Worcester, MA. Attendance at the PCB East 2026 conference and exhibition rose nearly 48% year-over-year. Contact Brooke Downey at brooke@pcea.net for details or visit pcbeast.com.

On Nov. 4, senior PCB design engineer and instructor Susy Webb will present "Designing the Signal Routing to Control Energy in Digital PCBs," a 3.5-hour webinar running from 11 a.m. to 2:30 p.m. EST. To register, click here.

New Corporate Members

- Cybord

Recent Discord Chatter

Overheard on the PCEA Discord server:

- Managing net names
- Non-revision changes in Altium
- When to switch to a new UI

Want to join? Send a note to membership@pcea.net.

CHAPTER NEWS

National.

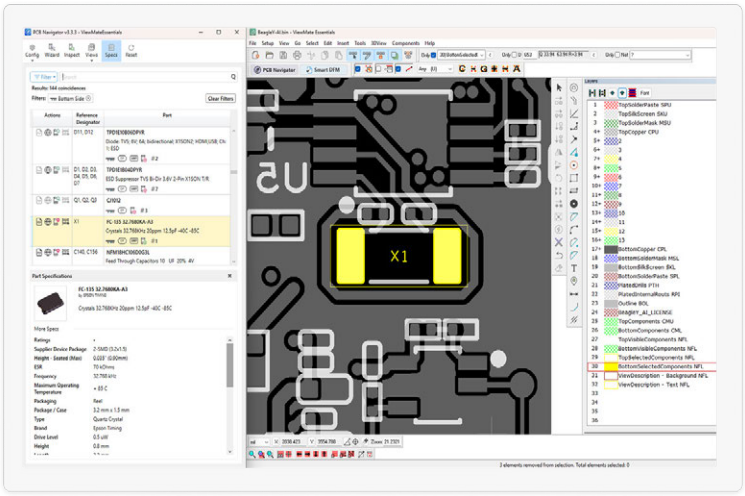
Upcoming webinars:

- Nov. 4 – "Designing the Signal Routing to Control Energy in Digital PCBs," with Susy Webb (register here).
- Nov. 17 – Printed Circuit Board Supply Constraints: A Complete Review of the Supply Chain, with Yash Sutariya, Saturn Electronics (register here).
- Dec. 8 – "From Design to Production Reality: How AI Optimizes Your Entire BOM, Not Just One Part at a Time," with Asaf Israelit (register here).

ViewMate Essentials

The Designer's Edge – CAM Made Simple, Smart





Get your CAD data ready for PCB Fabrication and PCB Assembly

- CAM Editor for Gerber Files & Drill Data
- SmartDFM with Custom Rule Checks
- PCB Navigator with Views and Reports

Integrating ViewMate Essentials into the PCB workflow catches errors early, optimizes files for manufacturing, reduces costly rework, and improves collaboration with standardized outputs.

→ **Download a free trial or book a custom demo!**

ViewMate is the industry standard CAM software, trusted by PCB Designers worldwide for decades.

+1 (800) 238-1920

pentalogix.com

AI's PCB Boom is Running Into a Capacity Wall

TAIPEI – The PCB industry's biggest problem right now is that it can't build fast enough. At the TPCA Show on Oct. 20, Unimicron chairman S.C. Chien gave numbers that should worry anyone planning 2027 builds. Lead times for some key equipment have stretched to as long as 30 months. More than 80% of equipment now takes longer to arrive, and over 20% is running at more than double the original lead time. Low-CTE glass cloth, copper-clad laminate and ABF are all tight, and critical materials could fall 20% short of demand in 2027.

Unimicron also warns that the scramble for AI capacity is leading customers to double-book orders. Anyone who lived through the 2021 component crunch knows how that ends. Order books look stronger than real demand, until they suddenly don't. Zhen Ding, the world's largest PCB maker, says it expects no near-term relief.

The demand side isn't in doubt. AI servers, larger substrates and higher layer counts are real, and they're profitable. The risk is in reading the signals. When lead times run longer than product cycles, and buyers order twice to be sure of getting served once, bookings stop being a clean measure of demand. Fabricators, EMS providers and OEMs will spend 2027 figuring out how much of the current backlog is real.

D-Day
Trends in the US electronics equipment market (shipments only)

	% CHANGE			
	JUN.	JUL.[r]	AUG.[p]	YTD
Computers and electronics products	2.5	-1.3	0.0	7.8
Computers	0.3	-0.9	-1.1	16.2
Storage devices	-1.8	3.6	4.6	15.7
Other peripheral equipment	-11.2	0.4	-0.7	35.7
Nondefense communications equipment	2.1	0.9	1.6	25.9
Defense communications equipment	6.8	4.8	-7.2	6.5
A/V equipment	-1.4	3.2	-1.4	-9.8
Components[1]	2.4	0.1	1.0	6.5
Nondefense search and navigation equipment	-1.4	-1.2	-0.1	5.0
Defense search and navigation equipment	3.5	-1.7	0.4	14.5
Electromedical, measurement and control	5.0	-3.6	-1.0	1.4

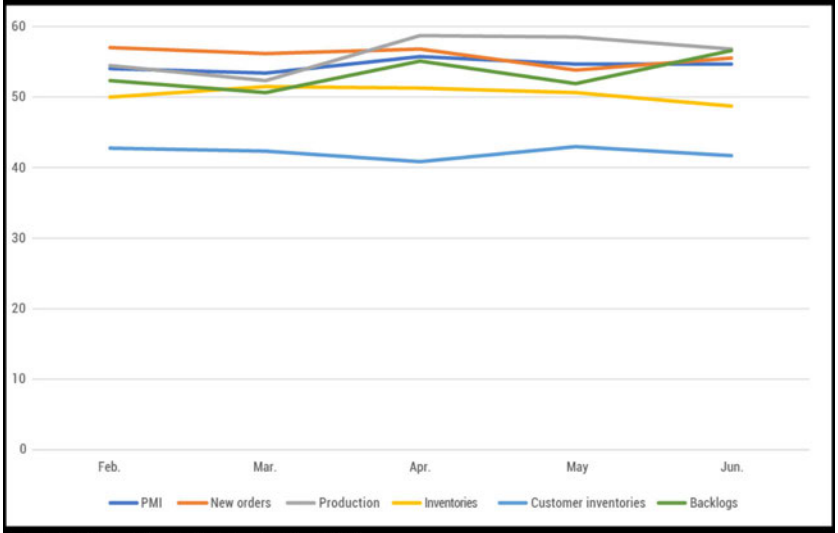
[r]Revised. [p]Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: US Department of Commerce Census Bureau, Oct. 2, 2026

Key Components

	MAY	JUN.	JUL.	AUG.	SEPT.
Semiconductors[1,3]	104.1%	123.6%	135.0%	144.3%	TBA
PCBs[2,3]	1.60	1.49	1.46	1.29	1.77
EMS[2,3]	1.36	1.33	1.29	1.39	1.68
Electronics mfg. orders[2]	115.0	118.0	119.0	117.0	123.0
Electronics shipments[2]	117.0	117.0	119.0	117.0	119.0
Component sales sentiment[4]	146.6%	154.1%	141.6%	136.7%	142.0%

Sources: [1]SIA, [2]GEA, [3]3-month moving average, [4]ECIA

US Manufacturing Indices



Source: Institute for Supply Management, Oct. 1, 2026

Quick Hits

Global silicon wafer shipments are forecast to increase 11.8% to 14.4 billion square inches in 2026, with record highs expected each year through 2029, when shipments are projected to reach 17 billion square inches. (SEMI)

Global **smartphone shipments** fell 22% year-over-year to 255.3 million units in the third quarter, as escalating memory costs curbed consumer spending. (IDC)

EMS M&A activity rebounded to seven transactions in the third quarter following a slower second quarter, with consolidations accounting for roughly 57% of deals. (Lincoln International)

The **PCB etching equipment market** is projected to grow from $1.88 billion in 2026 to $2.58 billion in 2030, a CAGR of 8.2%. (The Business Research Company)

North American **EMS shipments** fell 10.8% in September versus the same month last year and dropped down 10.4% sequentially. Year-to-date shipments are up 3.6%. Bookings increased 41.7% year-over-year and rose 9.4% sequentially, brining the YTD increase to 19.3%. (GEA)

The global **electronic chemicals and materials market** is projected to grow from $79.8 billion in 2026 to $109.4

billion by 2031, a CAGR of 6.5%. (BCC Research)

The **AR microLED display engine market** is forecast to reach about $2.5 billion by 2031, while co-packaged optics engine revenue for AI data centers is projected to exceed $112 billion that year. (Yole Group)

September North American **PCB shipments** fell 6.4% year-over-year and dropped 33.9% sequentially Year-to-date shipments are up 13.3%. Bookings rose 229.4% from last year and 336% from August, and are up 56.1% for the year. (GEA)

the *Best* in Electronics Assembly

CIRCUITS ASSEMBLY'S SERVICE EXCELLENCE AWARDS 2026 WINNER

RBB

HIGHEST RATING

EMS Revenues from $20M to $100M

Dependability/Timely Delivery, Manufacturing Quality, Responsiveness, Technology, Value for the Price, Flexibility, Overall Satisfaction

RBB



CIRCUITS ASSEMBLY

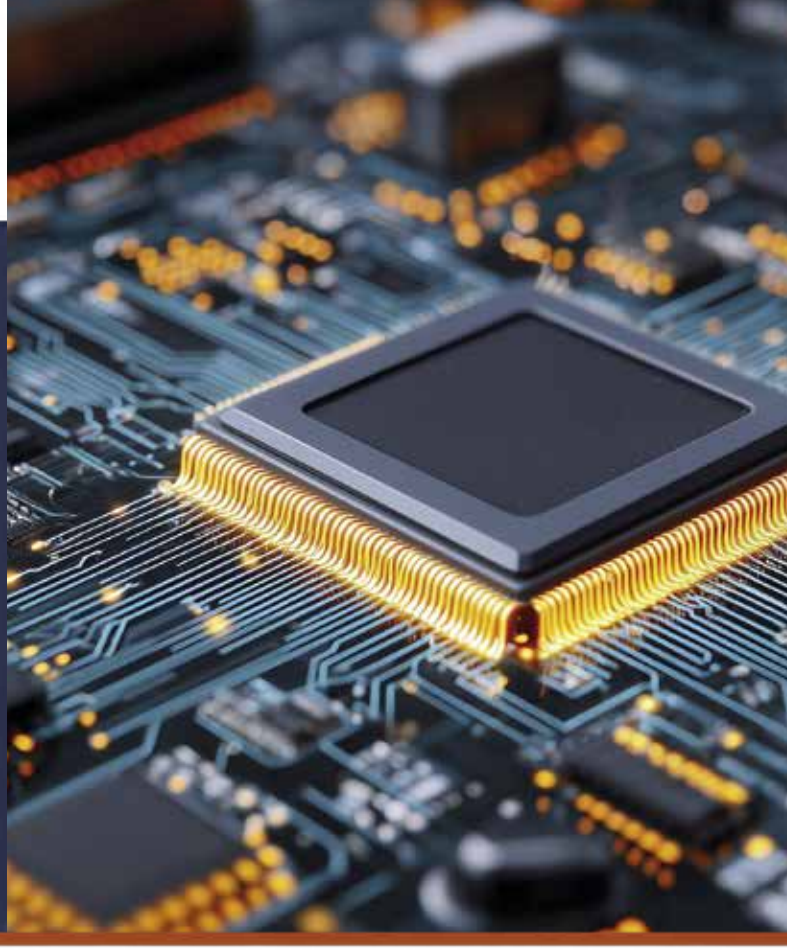
PCEA
Printed Circuit Engineering Association

RBB

Built For Partnership

RBB moves heaven and earth to get our clients what they need when they need it.

RBB is a privately-owned, full-service Electronic Manufacturing Services (EMS) provider that can handle the whole lifecycle: prototype, production, and end of life. RBB has been serving clients since 1973.



Services

RBB specializes in Printed Circuit Board Assembly, Industrial Control Panel Assembly, Box Builds, and Wire Harnesses.

Capabilities

RBB supports small and medium jobs of turnkey and labor-only projects for clients in Aerospace, Medical, Energy, Nuclear, Industrial, and More.

Certifications

RBB is AS9100:2016; ISO9001:2015 certified; ITAR registered. RBB builds to IPC standards.

Service Excellence Winner: 5 Years!

- 2022 — Technology
- 2023 — Overall Winner
- 2024 — Responsiveness
- 2025 — Overall Winner
- 2026 — All Categories

Contact us today!
330-567-2906

www.rbbsystems.com
sales@rbbsystems.com

1909 Old Mansfield Road,
Suite A; Wooster, Ohio 44691

ROI

Mission Back to the Future: A Plan to Revive North American Manufacturing

Revitalizing North American manufacturing will take more than rhetoric, requiring a clear mission, skilled workforce, reliable supply chains, significant investment, and decisive action.

FOR ABOUT A decade now, people have talked, chatted and pontificated about "reshoring." This conversation seems to have started in the electronics industry, where companies producing the critical technologies that support virtually everything, from complex national defense systems to simple consumer devices, were becoming increasingly scarce. Soon, virtually every industry, along with government officials, began discussing the need to bring manufacturing back to North America. Yet here we are, roughly a decade later, with little real progress despite all the rhetoric.

Whatever you call it, "reshoring," bringing manufacturing back, or something else, it requires a plan. Not just words, but a real, sustainable action plan. So, while I am not a politician, financier or multibillionaire, I have a recommendation. I call it "Mission Back to the Future."

Briefly, my plan draws on the life experiences of a baby boomer who spent his entire career manufacturing everything from paper to the most advanced electronics. Those experiences have taught me more than a few things, often the hard way. So here goes.

1. **Define your mission and stick to it.** In this case, the mission is to increase and expand manufacturing in North America. All activities must align with the national interest and the goal of creating a highly competitive manufacturing environment that rivals any in the world. Define the mission and stick to it.
2. **You cannot manufacture without people, period.** Yes, automation, AI, and other technologies must play a part, but without people, you are dead in the water. That means investing in vocational and technical education at the high school and postsecondary levels. From the 1950s through the 1970s, North America had many schools that successfully educated and trained young and not-so-young people, equipping them with the skills they needed to enter and thrive in manufacturing. Regrettably, too many of those educational opportunities no longer exist. One of our first priorities must be to commit to and invest in the training necessary to develop a plentiful, manufacturing-competent workforce. Achieving the mission of expanding North American manufacturing demands educating and training people in the skills the industry requires.
3. **Ensure a robust supply chain exists to support the manufacturing base.** While the long-term goal is to establish a local supply base (read: North America), we must utilize existing supply chains in the short term. This means eliminating senseless tariffs that negatively affect the availability of materials and supplies, at least

until we establish a robust local supply base. Manufacturing will never rebound or thrive if supply-chain shortages starve factories of essential materials. In particular, government officials must understand that tinkering with tariffs before completing the mission of expanding manufacturing will only choke the supply chain and jeopardize its success.



Figure 1. Great Scott! Bringing manufacturing back to the future will take more than a DeLorean and 1.21 gigawatts.

4. **Without adequate and appropriate funding, the mission will never get off the ground.** Expanding manufacturing requires significant investment to build facilities and equip them with the capital equipment, inventories, and personnel necessary to produce products. The operative term here is "appropriate." Tax incentives are great, but only if recipients actually have money to invest. However, expanding manufacturing in North America at the massive scale required will force governments to raise the bar and write some checks, and I mean BIG checks! Governments have dabbled in this approach through initiatives such as the CHIPS Act in the United States. However, if we take this mission seriously, we need a Herculean effort comparable to World War II mobilization. Put another way, we must take actions similar to those of many Asian countries that have committed significant investments to achieving strategic initiatives. That level of commitment is essential to accomplishing the mission of expanding manufacturing.
5. **Finally, stop talking and start taking action.** Every day, week, year, or decade spent debating "how" to accomplish the mission or "who" should take the initiative represents wasted time. When you are on a mission, time is often the most critical and valuable resource. Talk without action assures mission failure!

So, there you have it. "Mission Back to the Future" requires following the five points above. However, simple does not necessarily mean easy. Accomplishing each objective requires everyone involved in the mission, including business executives, educators and government officials, to demonstrate commitment, tenacity and patience, and to repeat

those efforts over and over. Put another way, everyone involved must walk the walk, not just talk the talk.

However difficult or unlikely "Mission Back to the Future" may appear to some, history provides ample precedent for what people can accomplish when all parties commit to a common mission. Consider the United States. Without that commitment, the country might never have built a transcontinental railroad, electrified such a vast nation, or sent a man to the moon and brought him back safely within a decade. In each case, those involved supported the stated mission by following the five principles outlined above.

We can do it. Manufacturing in North America can once again become abundant and globally competitive, but only if everyone commits to the mission.



PETER BIGELOW has more than 30 years' experience as a PCB executive, most recently as president of FTG Circuits Haverhill; peterbigelow@msn.com.

the *Best* in Electronics Assembly

CIRCUITS ASSEMBLY'S SERVICE EXCELLENCE AWARDS 2026 WINNER

VEXOS

HIGHEST RATING

EMS Revenues
from $100M to $500M

Responsiveness, Flexibility,
Overall Satisfaction

VEXOS



CIRCUITS ASSEMBLY

PCEA
Printed Circuit Engineering Association

Award-winning electronics manufacturing services & integration solutions

East West | VEXOS
An East West Company



CIRCUITS ASSEMBLY'S SERVICE EXCELLENCE 2026

FLEXIBILITY ▪ RESPONSIVENESS ▪ OVERALL SATISFACTION

East West + Vexos is a trusted Integrated Manufacturing Solutions (IMS) company partnering with some of the world's most recognizable brands and new disruptive players. As an IMS company, East West + Vexos **provides full lifecycle management, from custom design and proprietary products to advanced manufacturing and global supply chain solutions.** From concept to scale, East West + Vexos engineers, makes, and delivers complex electronic and electro-mechanical products leveraging more than 3,800 employees at 14 facilities in 7 countries. East West + Vexos' global team serves a broad spectrum of dedicated end markets knowing that the quality products made today can truly make a difference for all of us.

For more information visit: **ewmfg.com**

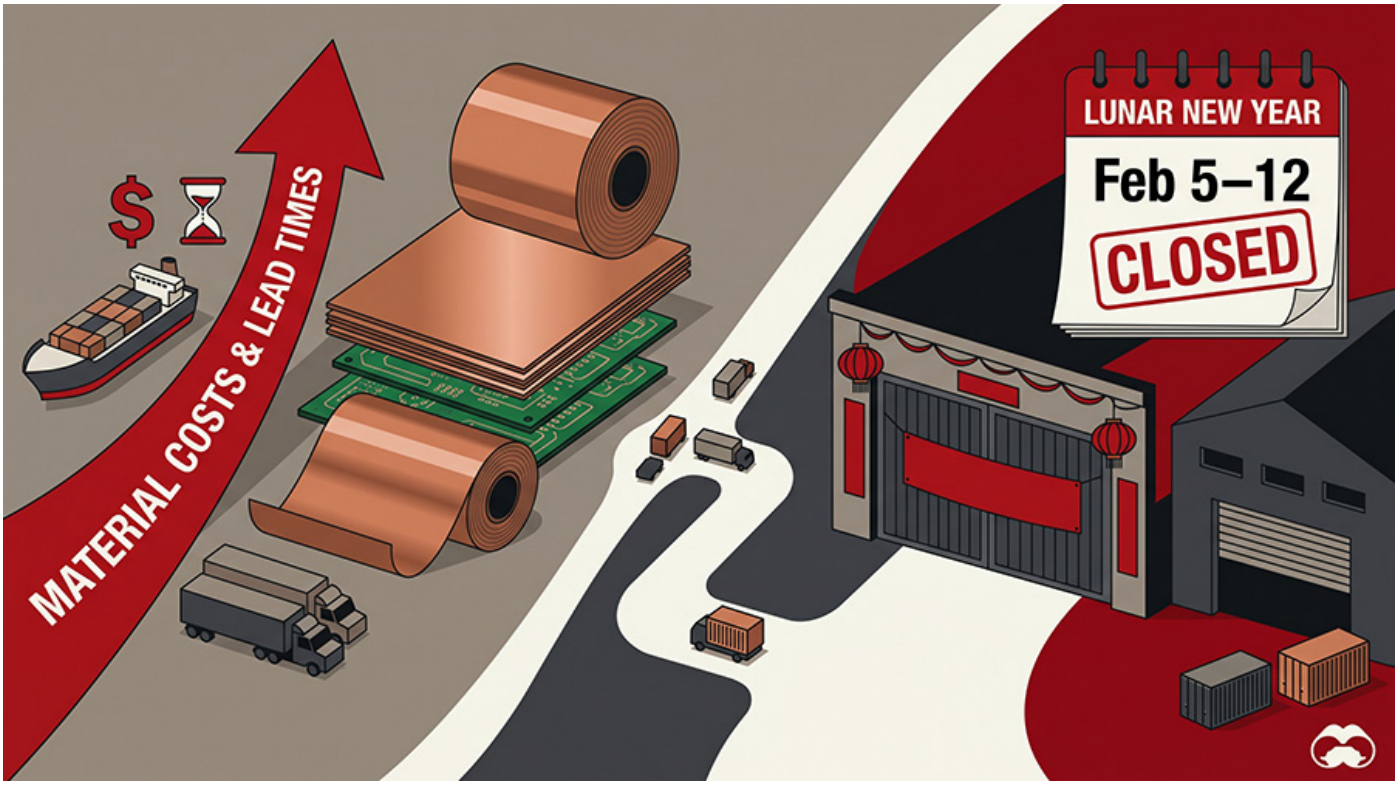
BOARD **BUYING**

Material Shortages Compound CNY Manufacturing Challenges

Chinese New Year celebrations take place a month after the ball drops in Times Square. And if you don't plan beforehand with your Asian suppliers, your hangover might last until spring.

DURING THE FIRST few months of the year, China shuts down for 7 to 10 days for its Spring Festival. Also known as Chinese New Year (CNY), the holiday's timing is determined by the traditional Chinese calendar, which tracks both the phases of the moon and the sun's position.

For 2027, standard closures will run from Feb. 5 through Feb. 12. PCB buyers who fail to plan for it will find their production schedules disrupted.



Rising material costs, supply shortages and Chinese New Year factory closures threaten to extend PCB manufacturing lead times into March 2027.

Most buyers who work with Asian suppliers know about the annual holiday, yet many still view it as a simple weeklong break that is easy to plan around. Few printed circuit board buyers seem to realize that CNY actually stalls

production and logistics for nearly a month. And in 2027, that disruption will be significantly worse.

Although the holiday is still about 90 days away, buyers must prepare now. Rising raw material prices and tightening supply are already extending lead times across the electronics supply chain, which will magnify the annual shutdown's effects.

The biggest difference going into the 2027 holiday season is the volatility of the foundational materials required to build bare boards. Prices for copper foil, electronic-grade fiberglass yarn (E-glass), epoxy resins and precious metals used in surface finishes – such as gold for ENIG and silver for immersion silver – have been climbing steadily. At the same time, laminate manufacturers are shifting capacity to high-margin infrastructure projects, tightening supply of standard copper-clad laminates (CCL) and specialized high-speed materials.

Many high-demand laminates now carry delivery lead times of six to eight weeks just to reach the board house. Because we are already in the final quarter of the year, an eight-week material lead time leaves less than a month for board fabrication before factories begin powering down for the holidays. Unfortunately, material shortages will push many orders placed within the next several weeks directly into March 2027, requiring buyers to plan well beyond February.

This material crunch also creates an immediate commercial trap: quote expiration. When copper and laminate mills hike prices ahead of the holiday rush, PCB fabricators shorten quote validity windows, often to seven or 15 days. Buyers holding open quotes from two weeks ago may find those prices no longer valid when they try to release a purchase order for January shipment, or worse, that the quoted delivery date is no longer achievable because competitors have already claimed the raw stock.

To understand why a one-week holiday causes a month of delays, buyers have to look at the timeline on the factory floor. Manufacturing begins to slow one to two weeks before the official holiday, when an estimated 40% of the workforce starts traveling home to be with family. As line staffing drops, factories will not start complex jobs. They will focus entirely on finishing in-process boards, creating a hectic January push to ship products.

In the rush to get goods out the door, severe freight queues are common. Freight forwarders and customs brokers become overwhelmed as thousands of factories attempt to clear shipments simultaneously. A buyer may receive a valid tracking number in late January even though the package sits in a congested warehouse and does not move for days. If that shipment does not physically clear the port or airport before the festivities begin, the buyer must wait until shipping operations resume after the holiday.

Furthermore, orders received in the three to five days before the shutdown are unlikely to begin production until afterward. During the holiday week itself, factories, freight companies, customs offices, banks and domestic material sub-suppliers close completely. Buyers should not expect factory communications, engineering reviews or shipping updates. Meanwhile, new orders continue to arrive from Western buyers while the factories are dark, leaving sales and engineering teams with a massive administrative backlog. An order placed shortly before or during the holiday may not even be reviewed for several days after employees return.

When the holiday officially ends on Feb. 12, factories do not restart immediately or at the same pace. Full production rarely stabilizes until after the Lantern Festival on Feb. 20. Factories must wait for migrant workers to return from inland provinces, and many employees use the holiday break – after collecting their annual bonuses – to change jobs or remain in their hometowns. Double-digit workforce turnover is common across Asian manufacturing hubs in late February, causing acute labor shortages and sluggish production ramp-ups.

This post-holiday period introduces two major risks that buyers frequently overlook:

The expedite and scrap trap. Buyers who miss the December ordering window often pay steep expedite fees in January to force their boards onto a plane before CNY. However, if a complex multilayer board encounters a manufacturing defect during lamination, drilling or electrical testing in the final days before the shutdown, there is zero time for a remake. If a lot is scrapped on Jan. 28, that expedited shipment automatically slips into late February or March.

The March quality dip. High workforce turnover means factories spend late February and March training new line operators while simultaneously rushing to clear the post-holiday backlog. At the same time, wet-process chemical lines – including copper plating baths, etching lines and surface finish tanks – have been drained or powered down for two weeks and require careful titration and recalibration upon restart. The combination of green operators, freshly restarted chemical baths and schedule pressure creates a notorious spike in quality escapes. Buyers receiving boards from the first two weeks of post-CNY production should increase their incoming quality control (IQC) inspections accordingly.

Meanwhile, products that missed the pre-holiday shipping cutoff are rushed to freight forwarders who are already buried under similar demand, driving up air freight spot rates and causing shipping delays for several days after operations resume.

Buyers cannot simply sidestep CNY by shifting orders to neighboring Asian countries at the last minute. The effects extend well beyond mainland China. Taiwan observes the exact same holiday schedule, and Vietnam celebrates Tet on matching dates with similar workforce migrations.

While alternative manufacturing hubs like Malaysia and Thailand observe CNY for only a few days – meaning they do not experience factory closures or worker departures on the same scale – both countries remain heavily dependent on mainland China and Taiwan for raw laminates, copper foil, dry film and specialized chemistry. When Chinese material mills shut down and freight corridors freeze, Southeast Asian board shops face the exact same raw-material bottlenecks.

While CNY dates vary each year, buyers can find out the specifics months in advance. The holiday does not suddenly disrupt production. But it may expose how many buyers lack inventory.

To protect Q1 production lines, PCB buyers should immediately execute a four-part strategy:

Lock in orders and audit open quotes. Work with internal stakeholders, customers and management to review

order histories and place purchase orders at least two months before the holiday. If you are holding open quotes from earlier in the quarter, verify with your supplier today that the pricing and material lead times still hold.

Use blanket orders to bypass inventory restrictions. Buyers who are restricted by just-in-time (JIT) mandates or cash-flow targets can use scheduled blanket purchase orders. Placing a six-month blanket PO now, with staggered monthly delivery releases through April, gives the fabricator the firm commitment needed to order and allocate scarce laminates today without forcing you to take delivery and pay for all the inventory in January.

Pre-approve alternate materials to prevent EQ holds. Prompt, clear communication between buyers and suppliers is critical when resolving engineering questions (EQs). If your fabrication drawing specifies a single-source laminate that currently has an eight-week lead time, your order will stall before it ever hits the shop floor. Work with your engineering team now to pre-approve functional equivalents (such as listing approved Shengyi, ITEQ, TUC or Ventec alternates alongside primary materials) directly on the fabrication notes so the factory can pull from available stock without pausing for an EQ review.

Build a post-holiday buffer. Do not just order enough inventory to survive the second week of February. Order enough stock to cover the holiday plus six to eight weeks afterward. This buffer is essential to sustain your assembly operations during the slow, backlog-heavy factory ramp-up into March.

February is the shortest month on the calendar, but without proper planning right now, it could easily feel like the longest.



GREG PAPANDREW has more than 25 years' experience selling PCBs directly for various fabricators and as the founder of a leading distributor. He is cofounder of DirectPCB (directpcb.com); greg@directpcb.com.

the Best in Electronics Assembly

CIRCUITS ASSEMBLY'S SERVICE EXCELLENCE AWARDS 2026 WINNER

ANDA TECHNOLOGIES

HIGHEST RATING

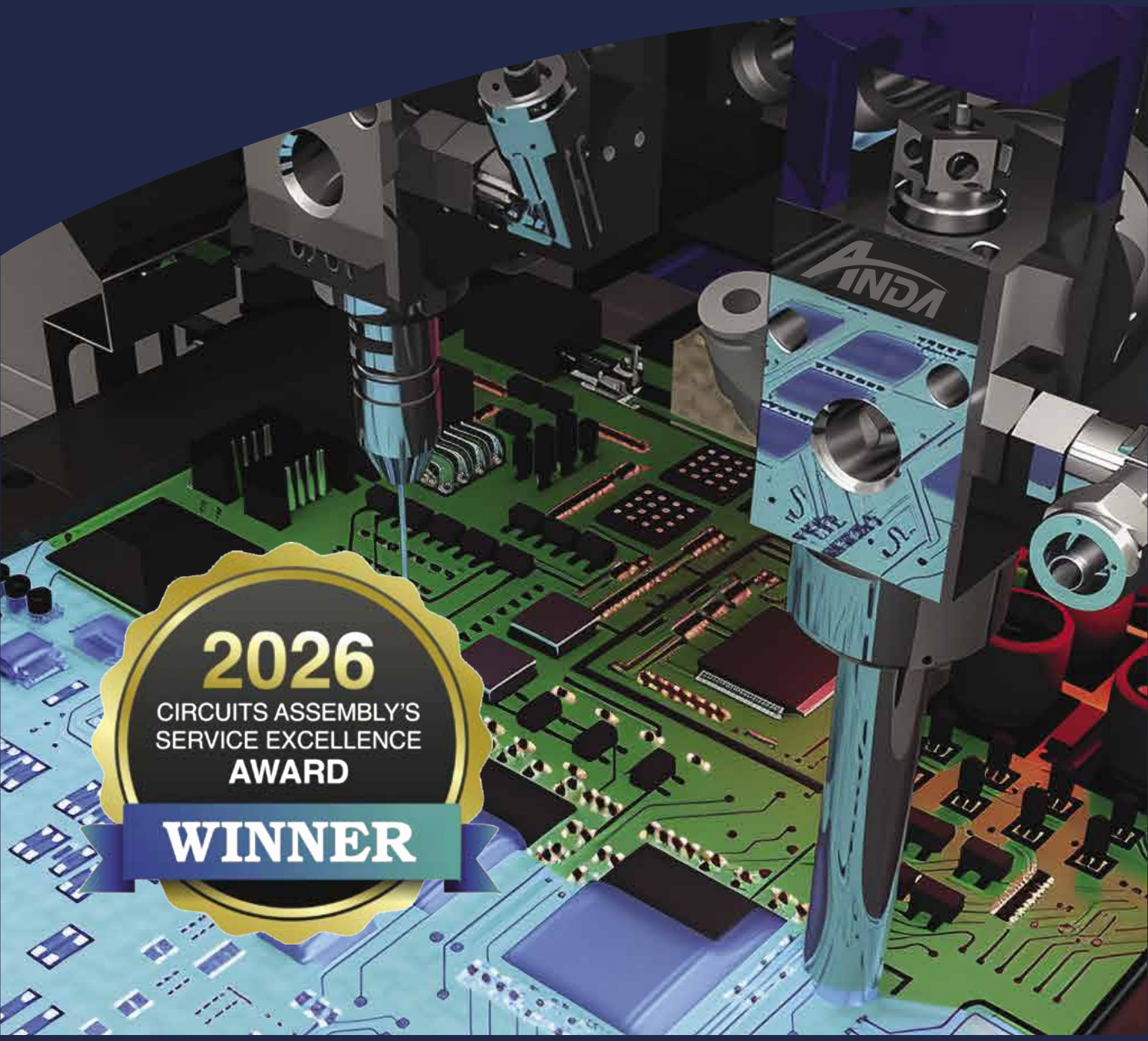
Coatings/Encapsulants



CIRCUITS ASSEMBLY

PCEA
Printed Circuit Engineering Association

ANDA



SMART MANUFACTURING SOLUTIONS
for Fluid Dispensing, Plasma and more....

www.anda.us

Terminology in the EMS World

One company's first article may be another company's NPI.

WE HAVE A bit of a communication issue in the EMS-OEM relationship, and possibly even within our own companies, particularly in the area of new product development

You may not be aware of this unless you have conducted a deep dive into the daily exchanges between your employees and customers, or taken the initiative to clarify what language (terms) you'll use to describe the various stages of a new product and the actions that need to be taken.

Communication, or a lack thereof, is at the root of much of the dysfunction between the EMS provider and the customer. I have seen these issues throughout my time in the industry.

Terms and definitions related to early-stage product development and launch can confuse customers and suppliers, and even people within the same company.

For example, here are just a few of the terms I have seen used interchangeably by technologists within the same company:

1. New product introduction (NPI)
2. First article
3. Prototype
4. Incubation
5. Quick turn
6. Product commercialization
7. New product launch
8. Product realization

These terms are not synonymous. If an engineer or purchasing manager wants to communicate specific elements of a new product's life-cycle stage, each term carries different meanings and requires different actions.

It isn't my intent to tell you how to define these terms. I simply want to draw your attention to a potential communication breakdown, both inward (within your own company) and outward (to customers).

If this is a problem in your factory, it should be easy to clarify which terms you use, both internally and externally, and what actions accompany each definition.

Review communications between your company and your customers, as well as your company's interoffice communications regarding NPI.

You may find yourself agreeing with Mandy Patinkin's character in *The Princess Bride*: "You keep using that word. I do not think it means what you think it means."



JAKE KULP is founder of JHK Technical Solutions; jkulp@cox.net. He assists OEMs and EMS companies with optimizing demand creation offerings and deciding when and where to outsource manufacturing. He previously spent nearly 40 years in executive roles in sales and business development at MC Assembly, Suntron, FlexTek, EMS, and AMP Inc.

the *Best* in Electronics Assembly

CIRCUITS ASSEMBLY'S SERVICE EXCELLENCE AWARDS 2026 WINNER

KOH YOUNG

HIGHEST RATING

Test and Inspection Equipment



KOH YOUNG AMERICA

CIRCUITS ASSEMBLY

PCEA Printed Circuit Engineering Association

KOH YOUNG TECHNOLOGY

Measure Everything, AI Everywhere

FIVE WINS. ONE UNWAVERING COMMITMENT TO SERVICE.

Five Circuits Assembly Service Excellence Awards since 2021, including three consecutive wins, reflect our commitment to keeping production moving. Our dedicated team delivers technical support, onsite service, and focused training, backed by the largest and most experienced network across the Americas. Expert help. Proven commitment. Wherever you need us.

27,000+ MACHINES SOLD

4,200+ SATISFIED USERS

AWARD WINNING COMPANY

EXPERT STAFF



5** x Circuits Assembly Service Excellence* ***Award Winner

kohyoungamerica.com
america@kohyoung.com

When Parts Run Out, Make a Friend and Make Your Quarter

> When the parts you need are unavailable, reach out to your close friends and associates in the electronics industry. They just might have a contact who can take care of you.

THE CLICHÉ ABOUT borrowing a cup of sugar to start a relationship holds true in business too. If you found a company representative who was especially accommodating, they might be the one you turn to when you need a lot of options again, even if they didn't get the job the first time. If they were quick to provide the cost breakdown, quantities, and turn-around times within budget, it may be time to use that second source. Critical items may need three vendors to manage inventory risks. Let's look at an example of whatever it takes to keep the assembly line moving.

Distributors and Brokers

A few well-known electronics catalog vendors seem to set the market on commodities as they grow scarcer. Big players can tie up key components. They don't get them all, but their order size gives industry leaders a leg up when parts are on allocation. Supply and demand according to big data. That is what the DigiKeys of the world have become.

Logistics is a huge business; nothing new about that. The evolution is towards transparency. They not only tell us whether a component is in stock, but also how many they have. We also get the lead time for parts that are currently unavailable.

Of course, "unavailable" has become a relative word. In a world with eBay and Amazon, just about anything that isn't specifically prohibited can be dropped off at your doorstep by the next delivery truck. Shop wisely. Component surfing has eaten its share of engineering hours. Services are filling in with the send us your bill of materials approach. Once engaged, the plan is committed to action. Here comes the inventory, whether it was the right stuff or not.

Knowing when to spend is harder than it sounds. Waiting for those precious commodities is a drain on the factory. Overbuying risks obsolescence before the inventory can be drawn down. Sometimes, the buyer is walking a tightrope between too little and too much.

Office Politics

Back when I was an electronics assembler, I tried to do a good job before putting my little ASSY-68 stamp on the units. Failing Quality Control inspection was not an option. You're as good as your workmanship. Management thought I'd make a good supervisor, so there I was overseeing a team that was trying to build fuse/alarm panels with no PCBs.

As you know, the PCB is an important part, so I went across the hall to ask the nice lady in charge when we could expect some alarm boards. She didn't know when they would be done, but she had a bunch of them in racks. They were waiting for that one big diode that most boards use to keep current flowing in the right direction. One part short!

Back to my desk and the primitive material resource planning (MRP) software of the day. It revealed a division in the company that had about a two-year supply, given their low run-rate. Half of their stash would have been perfect for my quarterly revenue target. It pays to be nice. The planner for that group was willing to sign off on a material transfer ticket (MTT) to move stock from one stockroom to another. I got the reel of diodes to my team's stockroom and told them I'd wait while they entered the transaction and filled the shortages in the PCB kits in that other person's department. They kept me waiting, so I waited.



Figure 1. When designers need diodes like these, it pays to be nice. (Image courtesy of Fairchild)

My patience paid off, and I was able to hand-carry the diodes over to the nice lady who got them soldered in, tested

the boards, and submitted them to quality control (QC) for a nice QC stamp of approval. The next day, I had boards for the half-assembled units and some more for the incoming kit. All of these were built up and tested in the panels. The panels went through another round of QC and then racked up for a quality assurance (QA) audit of a random sample, getting a lovely QA stamp. Passed and submitted to an on-site source inspector from AT&T with another lot right on the heels, that was two quality weeks for the fuse/alarm panel team.

Sorry, Not Sorry

The next week, my planner tells me a shipment of diodes has arrived in the Receiving Inspection department. She was not so nice about me helping the nice lady on the PCB side of the factory. Ms. Not-So-Nice suggested that my efforts were stepping on toes. I was young and couldn't let a witty remark go to waste. I answered with "Only toes that were dragging." I shouldn't have engaged that way.

It turns out that there was some rivalry among the planners and ours was the big selling product. Maybe she felt taken down a notch with some help from the puny, little 60-channel team. All of the assemblers were productive over those weeks, and we're close to shipping the racks that were missing their crowning piece: the fuse panels.

The moral of the story is that addressing the shortage report may take some footwork in the form of solving someone else's problems. Those tariff notices give pause to the supply chain manager. Buying and hoarding the remains of an end-of-life (EOL) part only lasts so long. In the board design community, we need to be ready to accommodate the fixes that keep the wheels turning in today's hyper-competitive procurement world. Proactively managing inventory risk is, simply put, good business.



JOHN BURKHERT, JR. is a principle PCB designer in retirement. For the past several years, he has been sharing what he has learned for the sake of helping fresh and ambitious PCB designers. The knowledge is passed along through stories and lessons learned from three decades of design, including the most basic one-layer board up to the high-reliability rigid-flex HDI designs for aerospace and military applications. John's well-earned free time is spent on a bike, or with a mic doing a karaoke jam.

the *Best* in Electronics Assembly

CIRCUITS ASSEMBLY'S SERVICE EXCELLENCE AWARDS 2026 WINNER

PVA

HIGHEST RATING

Dispensing

HIGHEST RATING

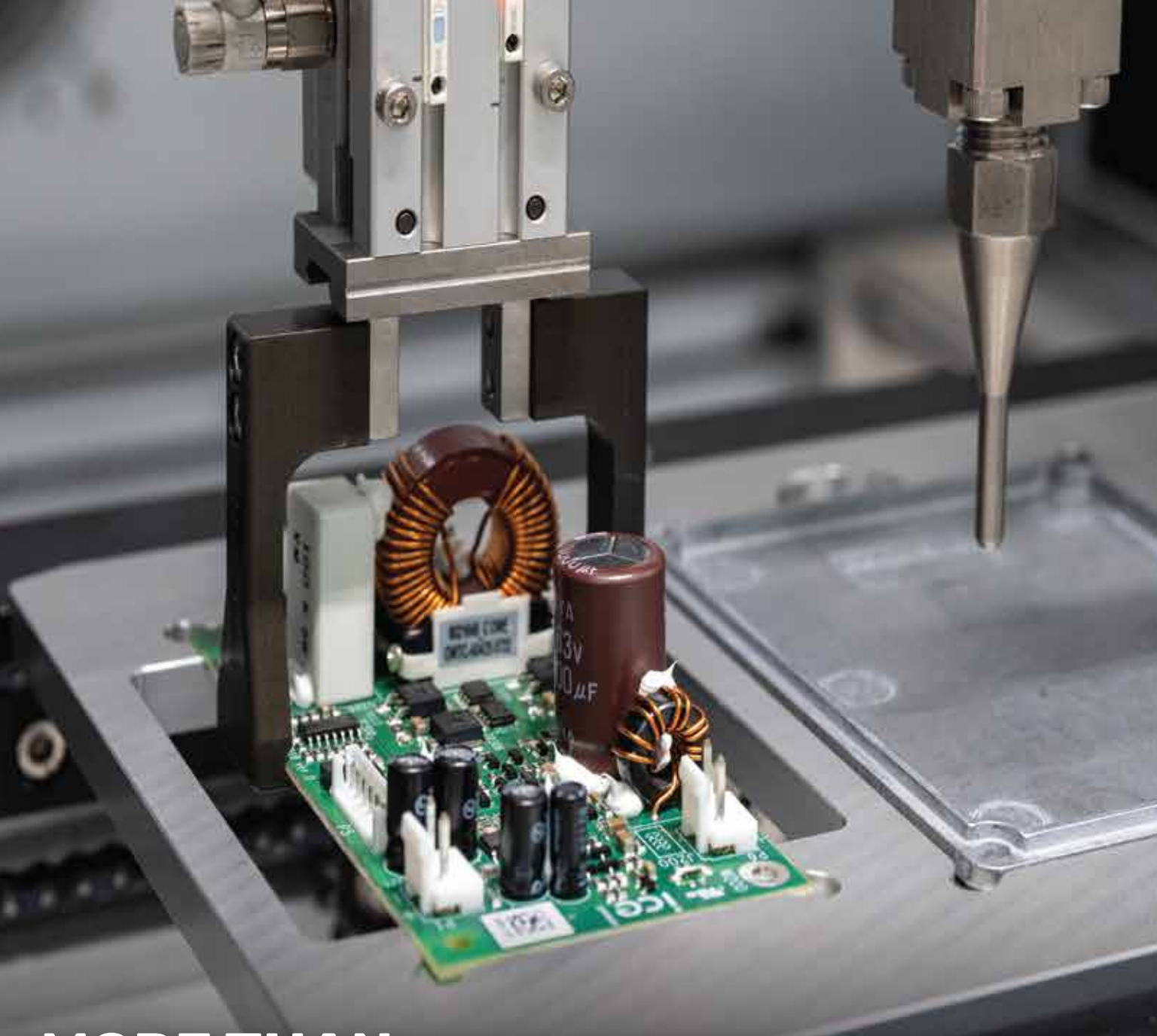
Automation and Handling Equipment

PVA



CIRCUITS ASSEMBLY

PCEA Printed Circuit Engineering Association



MORE THAN CONFORMAL COATING

PVA delivers custom automation solutions built around your dispensing application.

Protect your most sensitive components and perfect your production process with support from our team of experts.

ASSEMBLED IN THE US. SUPPORTED GLOBALLY.

PVA

Learn more

CIRCUITS ASSEMBLY'S
SERVICE EXCELLENCE
AWARDS
2026 DUAL WINNER
DISPENSING & AUTOMATION CATEGORIES

DESIGN **BEST PRACTICES**

Scalable PCB Design: From Independent Designer to Global Enterprise

Design best practices for building engineering workflows that grow with complexity, connect disciplines, and deliver measurable business value.

WE HEAR SCALABILITY often in engineering, usually in connection with increasing production capacity, expanding infrastructure, or supporting more users. In PCB design, however, scalability means something more fundamental: the ability to manage increasing design complexity, support more people and disciplines, preserve engineering intent, and deliver reliable products without letting the process become a bottleneck.

The challenge is that PCB design organizations rarely grow in a perfectly structured way. An independent contractor may begin with a laptop, an EDA tool, and a few trusted manufacturing partners. A small engineering business may add designers, introduce formal design reviews, and begin supporting multiple customers simultaneously. A larger organization may need to coordinate electrical, mechanical, thermal, signal integrity (SI), power integrity (PI), manufacturing, and supply chain teams across multiple locations and time zones.

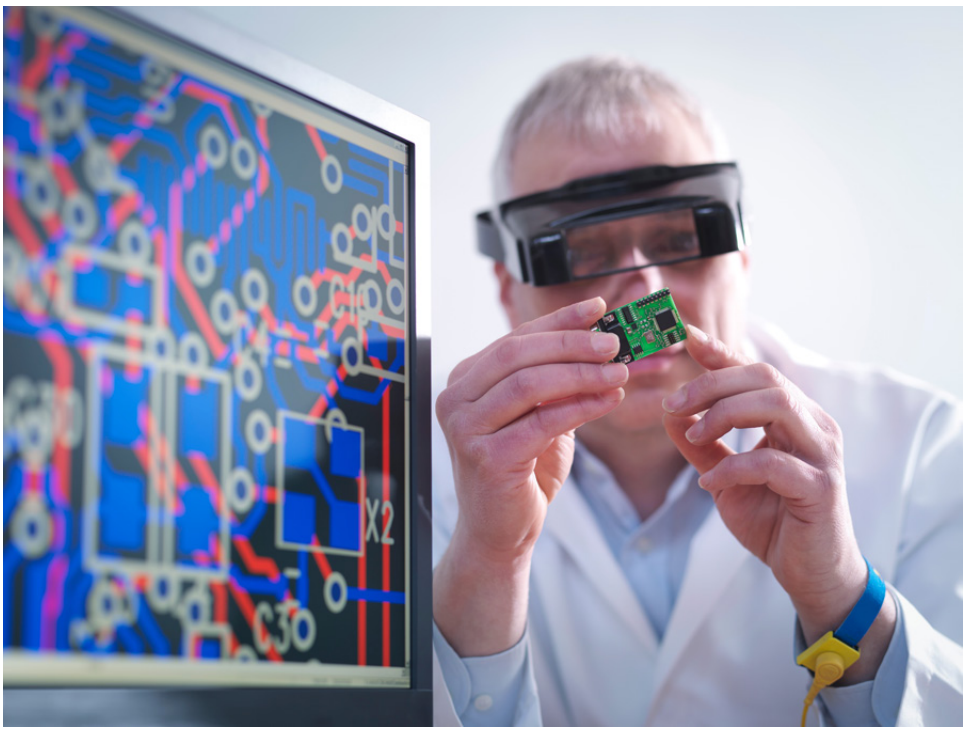


Figure 1. Scalable PCB design workflows connect engineering disciplines, streamline collaboration and help teams manage increasing complexity without sacrificing design quality.

Although these organizations differ considerably in size, their fundamental engineering objectives remain remarkably consistent: produce a design that meets its requirements, supports reliable manufacturing, and advances the product's long-term business objectives. What changes is the complexity of achieving those outcomes consistently.

The best scalability strategy, therefore, is not to introduce enterprise-level overhead into every organization. It is to establish sound engineering practices early, then evolve the tools, workflows, and collaboration models as business needs demand.

Build good habits before adding complexity. An independent PCB designer or contractor may have limited resources, but that does not mean scalability is irrelevant. In fact, this is where some of the most important habits should begin.

When one person owns the entire design process, information often resides in that individual's experience, working files, spreadsheets, emails, and memory. This approach can be remarkably effective for a straightforward project. Problems emerge when a customer requests a revision six months later, another designer must take over, or the original designer is unavailable when a manufacturing issue surfaces.

The first step toward scalability is making design information understandable, traceable and transferable. That includes establishing consistent library practices, documenting design constraints, maintaining revision control, recording critical engineering decisions and organizing manufacturing deliverables so that another qualified person can understand the final release and the decisions behind it.

This does not require an elaborate product lifecycle management (PLM) system or a large IT investment. The appropriate level of process depends on the work at hand. What matters is that the designer establishes a reliable source of truth and avoids treating the latest file on a local drive as the definitive record of engineering intent.

EDA tools should support these practices through reusable constraints, managed libraries, design-rule checking, and controlled release procedures. Even a contractor working alone benefits from separating reusable intellectual property from customer-specific project data and protecting both appropriately.

There is also a business advantage. Well-organized design data reduces time spent searching for information, reconstructing previous decisions, and correcting avoidable errors. It makes customer handoffs more professional and helps protect the value of the designer's expertise. When the workload increases, those habits provide the foundation for bringing in additional resources without starting over.

Small businesses. As a small PCB design business grows, the challenge shifts from individual productivity to repeatable execution. Multiple designers may work on different projects, share libraries, support several customers, or coordinate with external engineering and manufacturing partners. The owner can no longer rely on personal oversight of every design decision. This is where standardized workflows, managed design data, and design reuse become business necessities rather than administrative conveniences.

A small organization should establish common practices for project setup, constraint definition, library qualification,

design reviews, verification, and manufacturing release. Reusable circuit blocks, validated design elements, approved land pattern libraries, and documented design rules can reduce repetitive work while improving consistency across projects. Reuse, however, requires careful management: a proven circuit or layout from one product is not automatically suitable for another application with different electrical, thermal, mechanical, or regulatory requirements.

Collaboration also needs structure. If two designers modify different aspects of the same design, the organization needs a reliable way to identify changes, resolve conflicts, and maintain configuration integrity. If an external signal integrity specialist recommends a routing change, the team must communicate that recommendation in a way that preserves the relationship between the analysis, the design revision, and the final implementation.

Modern EDA environments can help by connecting design data, constraints, verification, and review processes. Depending on the organization's needs, cloud-connected collaboration, managed libraries and centralized project data can improve access and reduce the administrative burden of coordinating work. The goal is not to adopt every available capability; it is to remove the friction that prevents a small team from delivering consistent results.

The business case becomes clearer through utilization, margin, and risk. If experienced designers spend too much time rebuilding known functionality, resolving preventable library problems, or preparing and correcting manufacturing packages, the business pays for work that does not differentiate its engineering services. Standardization and automation can recover that time for higher-value engineering.

Just as importantly, repeatable processes reduce dependence on a few individuals as a business grows. A small business becomes more resilient when controlled data and workflows preserve project knowledge rather than leaving it in the memory of its most experienced designer.

Integrate the engineering disciplines. As electronic products become more complex, PCB design increasingly sits at the intersection of multiple engineering disciplines. Electrical performance often depends on mechanical packaging, thermal behavior, component selection, power delivery and manufacturing capability. A layout decision that appears acceptable within the PCB layout tool may create a problem elsewhere in the system.

For growing engineering teams, scalability therefore requires more than adding designers or increasing the number of EDA licenses. It requires connecting the disciplines that influence the design.

Consider a high-speed electronic assembly in which the electrical engineer defines interface requirements, the PCB designer establishes the stackup and routing strategy, the mechanical engineer controls the enclosure and the thermal engineer evaluates heat removal. If these activities occur in isolated environments with disconnected data, conflicts may not surface until late in development. A mechanical change can affect component placement; a component substitution can alter electrical performance; and a stackup change can affect impedance, loss, fabrication cost and schedule.

Multidiscipline integration helps teams evaluate these relationships earlier. Connected design environments, shared constraints, simulation, and coordinated change management allow engineers to review decisions in context rather

than as isolated tasks. Signal and power integrity analysis, thermal simulation and mechanical verification become more valuable when teams connect their results to the same design configuration and incorporate them into the engineering workflow.

This is also where the digital thread becomes important. The digital thread is the connected flow of information linking requirements, engineering decisions, design data, verification results and downstream manufacturing. It provides traceability across the product lifecycle, helping teams understand not only what changed, but why it changed and what else may be affected.

A digital thread does not require every discipline to use the same software. It requires meaningful interoperability, governed data, and clear ownership of information. Appropriate integration between EDA, mechanical CAD, simulation, PLM, component data and manufacturing systems can reduce duplicated effort and help ensure that teams work from consistent product information.

For management, the benefit is improved decision-making. Earlier visibility into design conflicts can reduce expensive late-stage changes, avoid schedule disruptions and make engineering trade-offs more transparent. Organizations should judge the investment not by the number of systems they connect, but by whether the integration improves product outcomes and reduces avoidable business risk.

Global enterprises. At enterprise scale, the challenge becomes coordinating people, processes and data across business units, geographic regions, suppliers and manufacturing partners. Different teams may use different tools, follow different local procedures and operate under different regulatory or customer requirements. Without deliberate governance, growth can create disconnected engineering environments that undermine the benefits of scale.

Enterprise scalability requires a balance between standardization and flexibility. Common design methodologies, approved libraries, constraint templates, verification practices, and release procedures help establish consistency. At the same time, local teams need the flexibility to address product-specific requirements, customer commitments and regional manufacturing capabilities.

The digital thread provides a framework for connecting these activities, while the digital twin extends the value of engineering data by representing a product or system for analysis, validation, and lifecycle decision-making. In PCB and electronic systems engineering, a digital twin may incorporate the board's physical design, material and stackup information, electrical and thermal models, simulation results and manufacturing or operational data, depending on the use case.

The distinction matters. A collection of disconnected CAD files and simulation reports does not, by itself, constitute a useful digital twin. The value comes from linking relevant product data to analytical models so engineers can evaluate behavior, investigate changes and make better-informed decisions. The scope and fidelity of that representation should match the questions the business needs to answer.

For example, when a component becomes unavailable, the impact extends beyond procurement. An alternate

component may introduce different electrical characteristics, package dimensions, thermal behavior, or qualification requirements. A connected engineering workflow can help teams identify affected designs, evaluate the technical implications, perform the necessary verification, and coordinate approved changes with manufacturing. That is a meaningful business application of connected product data: improving supply chain resilience without compromising engineering integrity.

Manufacturing integration is equally important. A design release should communicate more than the geometric definition of copper features. It should preserve the information manufacturers need to fabricate and inspect the product, including relevant layer structures, materials, tolerances, constraints and other applicable product data. Intelligent product-model exchange formats such as ODB++ and IPC-2581 can support richer data transfer than a collection of Gerber files alone, provided the receiving systems and manufacturing partners support the required information.

The objective is not to eliminate Gerber, which enjoys widespread support. It is to avoid unnecessary reconstruction of engineering intent and to establish a controlled, verifiable handoff appropriate to the product and manufacturing process. Enterprise teams should also document and review supplier feedback, approved fabrication changes and nonstandard requirements rather than allow them to become undocumented exceptions.

At this scale, engineering data governance, access controls, configuration management, and cybersecurity are essential. Organizations must protect reusable intellectual property, control supplier access, and maintain traceability of released product information. These controls protect not only engineering quality but also customer commitments, intellectual property and business continuity.

Measure outcomes, not software adoption. Across all organizational sizes, the business principles remain consistent. Technology should solve a defined problem, support a repeatable process and deliver measurable value. The mistake is to assume that a larger organization automatically needs more tools, or that a smaller organization can postpone sound engineering practices until it reaches a certain size.

A practical scalability strategy begins with identifying the organization's biggest sources of friction. Does repetitive manual work consume too much engineering time? Do teams struggle to trace design changes? Do verification activities occur too late? Do manufacturing partners repeatedly request clarification? Do engineers rebuild validated functionality or struggle to coordinate across disciplines?

Once the organization understands the problem, it should establish a baseline and measure improvement. Useful indicators include engineering rework, design-cycle time, first-pass verification results, release-package defects, time required to qualify design changes, reuse of validated IP and the frequency of manufacturing-related design escapes. Organizations should select these measures carefully; no single metric tells the whole story, and improvements in speed must never come at the expense of reliability or product quality.

Investment should follow the same principle. An independent designer may need disciplined file management and a well-maintained EDA environment. A small business may benefit from managed libraries, standardized workflows, and selective automation. A multidisciplinary organization may need connected analysis and collaboration. A global

enterprise may require governed product data, integrated lifecycle workflows and a more comprehensive digital thread.

Each stage builds on the previous one. Organizations should adopt capabilities when their complexity, risk, workload, and business objectives justify them…not simply because the technology is available.

Scalability Is an Engineering Discipline

After more than three decades in PCB engineering, one lesson remains clear: successful design is not just about producing a board that passes electrical checks. It is about making informed engineering decisions, validating those decisions against the requirements, and ensuring that the resulting product supports reliable manufacturing and long-term service throughout its lifecycle.

The same principle applies to scaling an engineering organization. A single contractor, a small design business and a global enterprise may operate very differently, but each benefits from reliable design data, controlled changes, appropriate verification and effective collaboration. The tools and processes should evolve as the work becomes more complex, while the fundamental discipline remains consistent.

Digital threads, digital twins, multidiscipline integration and automation are not ends in themselves. Their value lies in connecting engineering intent to execution, reducing avoidable rework, improving visibility, and enabling people to make better decisions with greater confidence.

The real measure of scalability is not how many engineers an organization can add or how many systems it can connect. It is whether the organization can take on greater complexity, deliver higher-value products, and grow its business without sacrificing engineering integrity. That is the foundation of a scalable PCB design practice, and a competitive advantage at every stage of growth.



STEPHEN V. CHAVEZ is a senior printed circuit engineer with three decades' experience. In his current role as a senior product marketing manager with Siemens EDA, his focus is on developing methodologies that assist customers in adopting a strategy for resilience. He is an IPC Certified Master Instructor Trainer (MIT) for PCB design, IPC CID+, and a Certified Printed Circuit Designer (CPCD). He is a past chairman of the Printed Circuit Engineering Association (PCEA); stephen.chavez@siemens.com.

the *Best* in Electronics Assembly

CIRCUITS ASSEMBLY'S SERVICE EXCELLENCE AWARDS 2026 WINNER

THE TEST CONNECTION

HIGHEST RATING

Test Laboratories

THE TEST CONNECTION, INC. 45TH ANNIVERSARY 1980-2025



CIRCUITS ASSEMBLY

PCEA Printed Circuit Engineering Association

The Test Connection, Inc.

LEADING-EDGE TEST SYSTEMS

Test Solutions & Services for Test Programming, Board Test, In-Circuit Test, Functional and Boundary Scan



IPC

CORPORATE MEMBER

SMTA MEMBER

410-205-7300
112 Lakefront Drive
Hunt Valley, MD 21030-2225

ITAR Registered and NIST 800-171 Compliant

ECAD TIPS & TRICKS

De-Embedding DC: Removing Resistance Effects in Impedance Measurements

Measuring characteristic impedance on PCBs with line widths over 75 microns is fairly simple. But below 20 microns, things begin to get a little dicey.

IN PCBS WITH traces of 75 microns or above, measuring characteristic impedance is a straightforward affair. But as dimensions drop to 20 microns or less, PCB fabricators and designers must de-embed the effect of DC resistance, which shows up as a rising reflection from the TDR measurement.

Solver and impedance measurements do correlate. Characteristic impedance is an inherent property of a transmission line, and it does not vary with length. When traces measure 75 microns and above, time-domain reflectometers (TDR) and vector network analyzers (VNA) operating in the time domain return a flat reflection over the length of the tested line, as shown in **Figure 1**.

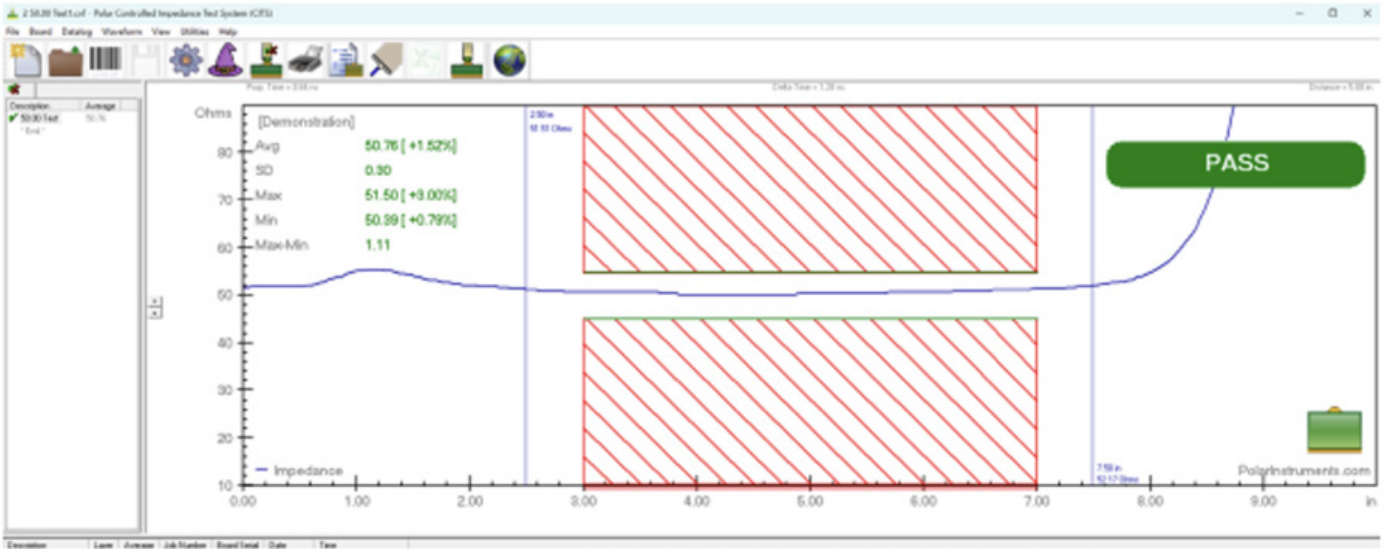


Figure 1. A typical 100-micron line-width TDR trace.

So, what changes at 20 microns? At line widths above 50 to 75 microns, the DC resistance of a PCB transmission line is small compared with the characteristic. But as line width reduces, the resistance appears to "pile up" on the TDR reflection. This is not the characteristic impedance changing: If you cut the line at any point and measure with a TDR, it will always start at the characteristic impedance. The only problem is that the reflection is disturbed by interconnect aberrations at the launch. **Figure 2** illustrates a trace with a sub-50-micron line width, and it illustrates the rise on the reflected trace:

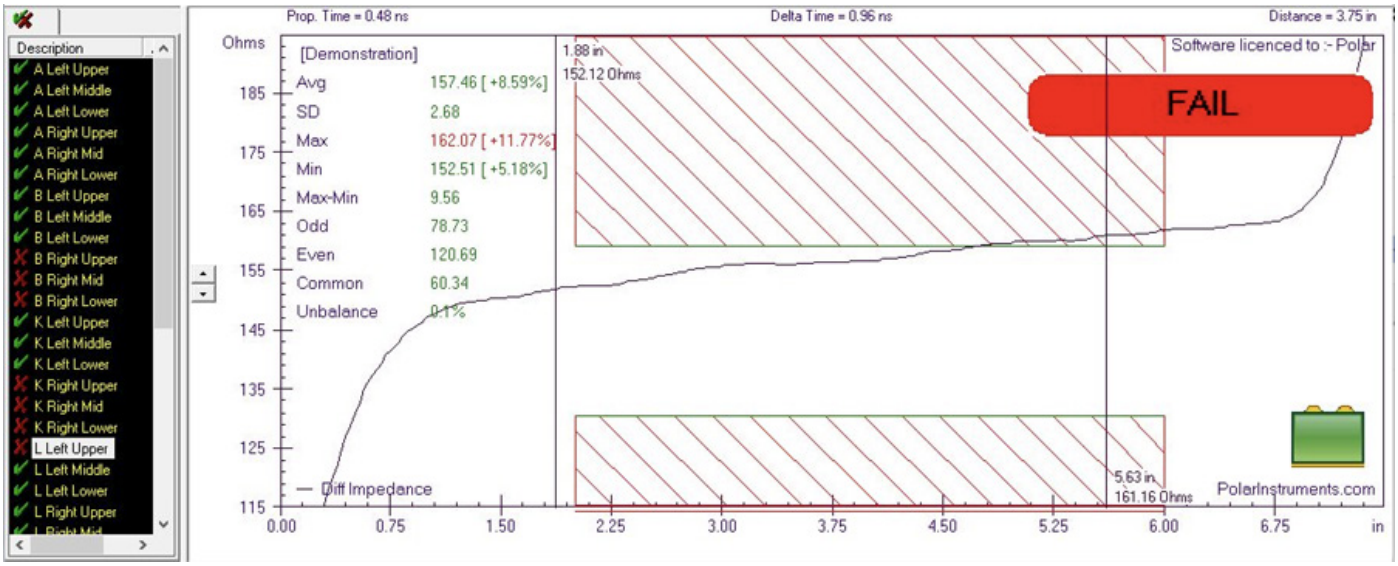


Figure 2. A sub-50-micron trace showing the effect of DC resistance.

What not to do. If you are unaware of the "why," and this has happened from time to time when fabricators take a chance on it, some imaginative people suspect the Dk is incorrect and use a field solver to "goal seek the Dk." This is an incorrect approach. The correct approach is to remove the effect of the DC resistance component on the reflection. So, how to achieve that?

Launch point extrapolation. Because the DC resistance superimposes a steady rise on the trace, it is possible to fit a regression line on the TDR trace and project back to the physical start of the trace. (Recall the earlier example – on the TDR trace, the actual point is masked by launch aberration.) Applying launch point extrapolation (LPE) simply draws a line back to the hidden point at the start of the trace. This gives us the characteristic impedance. Note that we are not ignoring the DC resistance – this is a characteristic of the line. But it is not the characteristic impedance. **Figure 3** shows the line from Figure 2 with LPE regression used to de-embed DC resistance.

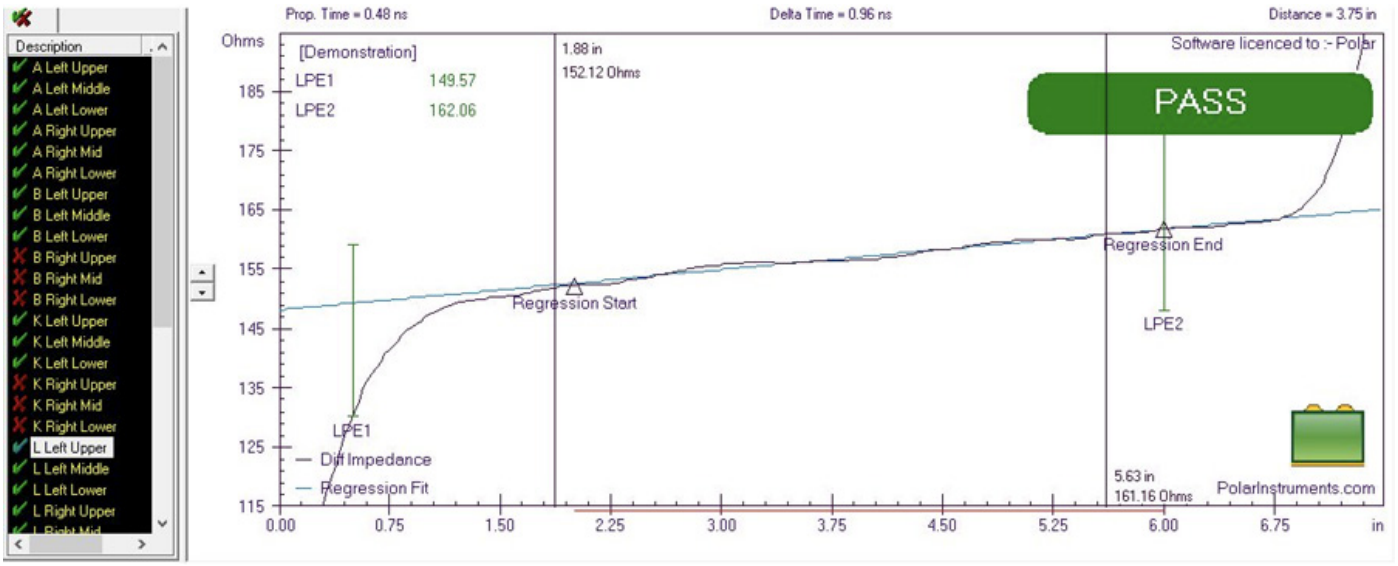


Figure 3. Applying LPE shows the characteristic impedance after removal of DC resistance from the TDR trace. It measures 10 ohms less than it would have without compensation.

Measuring at the Lower Limits of Subtractive Manufacture

Figure 4 illustrates the measurement of a differential pair at the lower limits of subtractive fabrication.

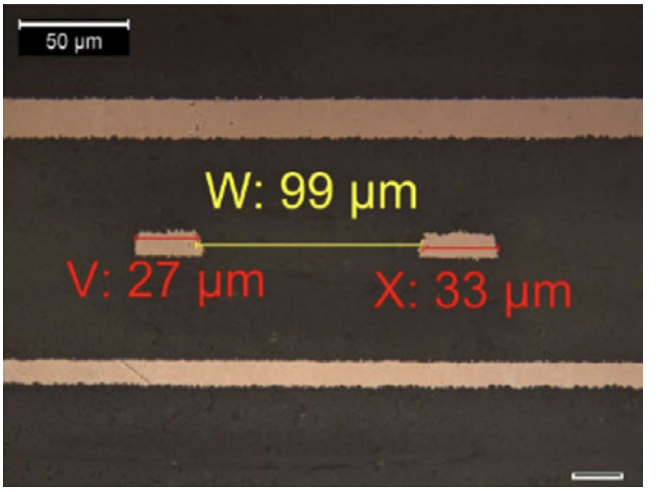


Figure 4. This differential pair shows significant DC resistance under test and will only correlate if DC resistance is removed from the measurement.

At these dimensions, the DC resistance of the trace is significant, and using a raw reflection from TDR or VNA with the time-domain option will lead to the impression that the measured and modeled impedances do not correlate. The simple action of removing the DC resistance component from the reflection will lead to the correct correlation.

Figure 5 depicts an easy way to predict the impact of DC resistance on TDR traces.

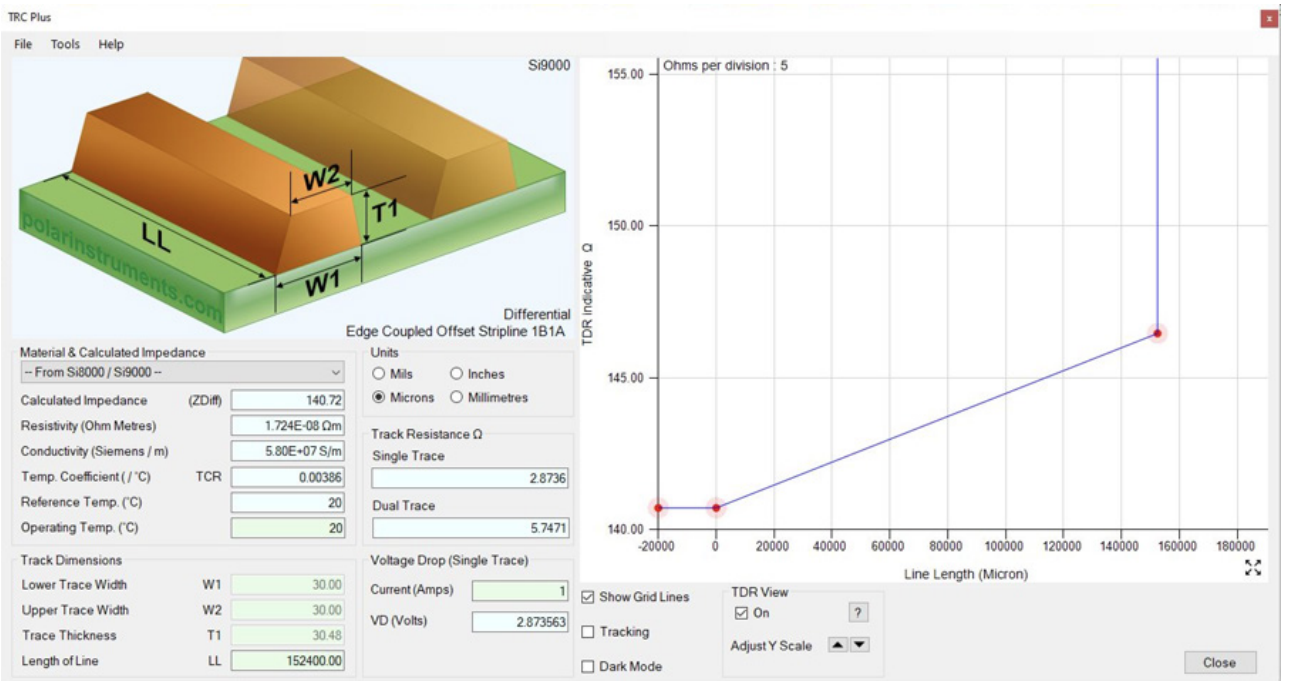


Figure 5. Prediction of the impact of DC resistance on the TDR impedance measurements.

By feeding the copper geometry and resistivity into the Polar TRC Plus, you can predict whether you need to ask your fabricator to use LPE in order to achieve correlation between solver and measured results for controlled (characteristic) impedance.

When traces get below 20 microns, measuring characteristic impedance really starts to get interesting.

REFERENCES

1. James A. Strickland, *Time Domain Reflectometry Measurements*, published by Tektronix, 1970. An invaluable resource, now out of print but available online and occasionally in print used.

2. Polarinstruments.com application notes and youtube.com/@polarinc.



MARTYN GAUDION is managing director of Polar Instruments.

PCEA®
PRINTED CIRCUIT ENGINEERING ASSOCIATION

Thank You!

TO OUR PCEA CORPORATE MEMBERS

ACCURIS

all flex SOLUTIONS

AllSpice.io

ASC

BEST Technology

BOARDERA

CHESTER ELECTRONIC DESIGN

cofactr

Cybord

DirectPCB®

electronic interconnect
THE PCB EXPERTS

elyca

EMA Design Automation™

ESPEC

FINELINE
EXCELLENCE IN PCB

FREEDOMCAD
ELECTRONIC PRODUCT DEVELOPMENT

GFE

luminovo

Millennium Circuits Limited

NCAB GROUP

25 Newgrange Design
Celebrating 25 years

Collaborate • Educate • Inspire

PCEA CORPORATE MEMBERS

Nordson ELECTRONICS SOLUTIONS

Panasonic INDUSTRY

PARMI

Parter

Pcbcart

PCB Libraries

PCB TECHNOLOGIES USA

pentalogix

Polar

POLYONICS

PRECISION CIRCUIT TECHNOLOGIES
Every micron matters.

Quantic Ohmega Ticer

REMTEC

SCREAMING CIRCUITS
a division of Milwaukee Electronics

SIEMENS

SVT
SVTRONICS, INC.

SYNTRONIC

TCLAD INC.

THE TEST CONNECTION, INC.
45TH ANNIVERSARY
1980-2025

ventec
INTERNATIONAL GROUP
騰輝電子

VISCOM
vision technology

Weidmüller

WINONICS

JOVE

Learn more: **Will Bruwer** Senior Sales Executive • 404-313-1539 **will@pcea.net**

Reindustrializing for the Age of AI

AI, supply chain constraints and evolving manufacturing technologies are reshaping reindustrialization efforts, highlighting the need for a forward-looking approach to rebuilding industry.

PEOPLE OFTEN SAY that the biggest problem with computers is that they do exactly what we tell them to do, even when the result isn't what we really want. Agentic AI now inverts that dilemma by allowing users to describe the desired result and leave the agent to calculate the best way to achieve it. Moreover, these agents can draw not only on resources within, say, a factory, but also on information from additional sources to evaluate and adapt their strategies over time as external factors change. This represents continuous improvement – a principle already deeply rooted in industrial quality-management strategies – that now operates autonomously and in real time.

AI processing can take place in the cloud or at the edge, on small, resource-constrained platforms. As factories incorporate more sensors, edge devices provide an ideal way to measure sensor readings and determine immediate responses. Processing, packaging and sending data to the cloud then provides the basis for longer-term analysis, helping identify trends and build the information sources AI agents need to optimize manufacturing and business processes.

The rapid adoption of AI in industrial edge devices such as smart sensors, PLCs, computing modules, and gateways puts the sector in competition with AI data center operators for access to resources such as high-end components, PCBs, and substrate materials. Explosive growth in the server market is diverting these resources from other sectors, and we should remember that industrial automation products account for about 20% of the global PCB market. While the sector currently represents only about 12% of the US PCB market, industrial applications account for more than 30% of European PCB production. Industrial PCBs account for about 6% of China's total PCB production, as the country produces enormous volumes of boards, primarily for communication and computing equipment.

As AI server demand continues to consume high-end resources, limited access to advanced technologies could significantly hinder the West's urgent drive to reindustrialize. Factories must adopt cutting-edge technology to deliver competitive quality and productivity. The offshoring boom has transformed manufacturing over the past two to three decades, and companies must establish new factories with full awareness of these changes.

While manufacturers initially pursued offshoring mainly to reduce costs, today's push for reshoring aims to strengthen supply chain resilience and geopolitical independence. New approaches include split-sharing, which divides manufacturing operations across multiple locations worldwide to avoid geographical concentration. At the same time, China's manufacturing landscape is changing as producers increasingly serve healthy and rapidly growing

domestic markets profitably.

The current situation has evolved over more than a quarter of a century and will take more than a couple of years to rebalance. Although the West has no shortage of determination or financing, money always moves faster than people. Companies must hire and train suitable workers, and workforce development could become a bottleneck. We are approaching a time when humanoid robots could help address this challenge, and at least one company in Europe is currently planning a new factory that will incorporate AI-based principles and processes from the ground up. This strikes me as a bold and exciting move that highlights a direction Western industry could pursue as it strives to meet its objectives in the coming years. On the other hand, the hardware shortages we currently face will limit how quickly we can adopt advanced AI technologies, including humanoid robots, in new factories.

"Time is what keeps everything from happening all at once," wrote author Ray Cummings in the short story *The Girl in the Golden Atom*. There is an undeniable truth at the heart of the joke. While we can implement small changes relatively easily and quickly, the major changes we now need are much more complex and will demand proper planning, a long-term perspective, and perseverance.

We must also consider the current circumstances: supply chain bottlenecks persist, new capacity takes time to come online, and establishing a new factory realistically takes two to three years. Meanwhile, technological change continues to accelerate.

Analyzing the origins of the current situation is unlikely to help guide the future. I remember participating in a working group after the dotcom crash of the early 2000s, tasked with identifying the causes and developing a way to anticipate similar events in the future. The crash had left the company with excessive inventory, and management wanted to avoid a repeat. We concluded that we could not have reliably predicted the situation, much less prevented it. I believe today's circumstances are similar. Companies pursued offshoring for understandable and defensible reasons: technology made it possible, competitive pressures made it necessary, and the shift democratized high-tech manufacturing while sharing its benefits with emerging economies.

The next era of advanced manufacturing could begin here, and incorporating AI into every activity, from the factory floor to the front office, could unlock greater efficiency, delivery performance, profitability, and adaptability. It will be fascinating to watch this transformation take shape and a privilege for those of us here today to witness it and play a role in it.



ALUN MORGAN is technology ambassador at Ventec International Group (venteclaminates.com); alun.morgan@ventec-europe.com. His column runs monthly.

DATA TRANSFER

IPC-2581 Adoption Summit 2026: Intelligent Data Exchange Between Design Houses and Manufacturing Partners

The third annual summit at PCB West highlighted real-world adoption, industry collaboration and the next generation of intelligent PCB data exchange.

THE THIRD ANNUAL IPC-2581 Adoption Summit took place Oct. 1, 2026, at PCB West in Santa Clara, CA. It brought together OEMs, PCB fabricators, contract manufacturers and software suppliers to discuss an important question: How can the industry accelerate its transition from traditional PCB manufacturing data packages to intelligent, digital data exchange?

The discussions did not question whether IPC-2581 works. Companies already use IPC-2581 in production. Instead, participants shared experiences, discussed how to overcome adoption challenges and collaborated on innovations that can benefit the entire PCB design and manufacturing supply chain.

Representatives from leading OEMs, VGT, WUS, Dynamic Electronics, IFOUND PCB, Cadence, Aegis, Polar Instruments, Vayo and others participated. Some have used IPC-2581 for years, while others are just beginning their journey. IPC-2581 no longer serves simply as a replacement for Gerber. It is changing how the industry communicates design and manufacturing intent.

By the industry, for the industry. Twelve founding members established the IPC-2581 Consortium in 2011. Today, it includes more than 140 member companies representing the PCB design and manufacturing ecosystem: OEMs, EDA/DFM/CAM software suppliers, PCB fabricators, electronics assemblers and test companies. Its mission is to accelerate adoption of IPC-2581 as an open, neutrally maintained global standard that encourages innovation, improves efficiency and reduces costs. What's not to like?

The Consortium does much more than promote a data format. Its greatest strength is collaboration. Members identify problems affecting the industry, develop solutions, incorporate those solutions into the standard and help companies implement them, including companies that do not belong to the Consortium.

With a proprietary format, innovation depends on the format owner's priorities, resources and release schedules. Even when users identify an important requirement, changing the format can be difficult at best, and rolling the change out across the ecosystem and into end users' hands can take considerably longer. The IPC-2581 Consortium gives the industry a forum to identify needs, propose enhancements, review them through an open standards process

and help drive implementation. Changes still require work, but industry needs, rather than a single proprietary-format owner, set their direction.

IPC-2581 is by the industry, for the industry.

Three years of adoption summits and growing momentum. The Consortium held its first IPC-2581 Adoption Summit right after PCB West in 2024. The objective was to bring companies across the PCB ecosystem together to share adoption experiences, identify obstacles and collaboratively develop solutions. The 2026 meeting marked the third summit at PCB West.

The Consortium holds the annual Adoption Summit the day after the PCB West exhibit day. This year, at the request of members who attended the summit, the Consortium also held an IPC-2581 update meeting at IPC APEX EXPO 2026 to share progress and engage more of the industry.

These meetings go beyond presentations about a standard. They are working sessions in which members discuss what works, what doesn't and what needs to improve. This year's summit included show-and-tell sessions that showed participants how easily they can use IPC-2581 to, for example, eliminate the fabrication and assembly drawings that often cause 25% to 50% of (unnecessary) technical questions (TQs).

The Consortium maintains a Top 10 list of priorities for accelerating adoption and reviews progress against those priorities. Table 1 highlights in yellow the items on which the Consortium has made progress.

Table 1. IPC-2581 Consortium Top 10 Adoption Priorities: Progress Report

Rank	Issue
1*	DfX exchange tool for both contract manufacturers and fabricators
2*	Validation: generation and consumption of the standard
3*	Address issues with stackup-only exchange
4	OEMs should require their suppliers to accept IPC-2581
5*	Simplify and reduce IPC-2581 file size
6*	Transfer DFM rules from manufacturer to customer (OEMs)
7	Bidirectional transfer of materials libraries between manufacturer and customer (OEMs)
8	Get Altium to the table to support the latest IPC-2581 revision and stackup exchange
9	OEMs stop sending defective data
10*	Promote IPC-2581 in the industry

* Indicates priorities on which the Consortium has made progress.

Table 1 shows how the Consortium translates industry feedback into concrete activities, and where it needs additional collaboration and participation.

Adoption is happening: the numbers tell the story. One of the most encouraging parts of the summit was hearing about actual deployments, not just plans.

- One OEM reported that it has fabricated and assembled more than 150 different PCB designs using IPC-2581 over the past 12 months.
- Aegis reported that more than 33 of its EMS and contract manufacturing customers worldwide have used IPC-2581 over the past decade.
- A large, influential OEM uses IPC-2581 internally and is working toward bidirectional data exchange with manufacturing partners.
- Polar Instruments implemented IPC-2581 Revision C import/export for stackup exchange in response to OEM requirements.
- Cadence continues to enhance its IPC-2581 implementation based on customer needs and collaboration with other Consortium members.

These examples demonstrate that adoption extends beyond one supplier or manufacturing process. Companies can start with stackup-only exchange, move to fabrication data, expand into assembly and eventually use bidirectional DFM exchange. There's no need to change everything at once.

Why Move to IPC-2581?

Protect your intellectual property. One of IPC-2581's most valuable capabilities is protecting intellectual property through function modes. Traditional manufacturing handoff packages contain considerably more information than a particular partner needs. Why should an assembly house receive all the information a fabricator needs? Why should a stencil manufacturer receive unrelated design details?

IPC-2581 allows users to generate packages appropriate to a particular operation, including fabrication, assembly, test, stencil, BOM, DfX and other user-defined modes. Send partners the information they need to do the job, not everything in the design.

Eliminate unnecessary fabrication and assembly drawings. Traditional manufacturing packages rely heavily on drawings to communicate requirements the artwork does not capture. A drawing may lag behind a design change, a note may be ambiguous, or a manufacturer may need clarification about which objects a requirement applies to.

Vince DiLello of Cadence demonstrated how designers can electronically attach manufacturing specifications to design objects and export them in IPC-2581. For example, a designer can attach a via-plugging requirement directly to the applicable vias. Other examples include impedance, tolerances, fabrication instructions and assembly specifications.

Cadence has supported this capability since 2021 and recently enhanced it to allow multiple specification definition files and sharing among designers. Many users remain unaware of it. Rather than automate the creation of potentially inconsistent drawings, why not eliminate the need for many of them?

Reduce manufacturing data preparation time and avoid errors. Dana Korf offered a fabricator's perspective. Gerber originated more than 70 years ago, and conventional handoff still requires significant interpretation and reconstruction. Fabricators receive artwork, drawings, drill files, netlists, spreadsheets and other documents that may conflict or omit important information.

Korf described IPC-2581 imports that take less than one minute, compared with 20 minutes to more than eight hours for some traditional packages. These figures reflect participants' experience rather than industry-wide benchmark averages, but they illustrate the opportunity.

Fabricators often correct incoming data without charging the customer. Each interpretation or correction, however, can introduce a difference from the original design intent. The goal should be to manufacture what the designer intended, without reconstructing that intent.

Exchange stackup information electronically, before layout. One of the Consortium's earliest innovations, stackup-only exchange, dates to around 2014–2015. High-speed PCB designers and fabricators collaborate early on materials, layer structures, thicknesses and impedance requirements. Traditionally, recommendations arrive in spreadsheets, drawings and emails, and designers must manually re-enter them into PCB design tools.

IPC-2581 allows intelligent stackup information to move electronically in both directions. Polar Instruments discussed its Revision C import/export implementation. This eliminates unnecessary re-entry, reduces errors and helps teams avoid mismatches they might otherwise discover late in the design cycle.

Move technical questions from email to digital exchange. Fabricators and designers still often exchange TQs through emails, spreadsheets, screenshots and documents. Someone forwards each question to the appropriate engineer, who answers it, and then someone manually connects the answer back to the correct PCB revision.

IPC-2581 Revision C introduced the DfX module for electronic exchange of DfM data and TQs, and version 4.0 enhances these capabilities. DiLello discussed Cadence's ongoing vision for an IPC-2581-based digital TQ workflow. The envisioned system would associate questions with board revisions, route them to responsible engineers, manage priorities and deadlines and integrate with enterprise tools.

Importantly, the complete design database need not travel with each question. Users can exchange relevant information separately and securely. Analytics could also reveal recurring issues, training opportunities and supplier trends. The objective is not simply to send emails faster; it is to make the communication itself intelligent.

Improving Interoperability Through Validation

As adoption grows, interoperability becomes increasingly important. Generating an IPC-2581 file does not guarantee that every element conforms to the schema or that every receiving tool will interpret it correctly.

Terry Hoffman of Cisco demonstrated IPC2581 Check, a schema validation tool that identifies nonstandard attributes, invalid structures and other issues. In one real-world case, it detected repeated elements where the schema allowed

only one; the vendor confirmed and corrected the error. Cisco has approved an open-source release, and its internal publication process is underway.

This is another example of collaboration benefiting the industry: A shared validation capability can help both producers and consumers of IPC-2581.

Making the transition: lessons from the field. One of the biggest barriers often isn't technical; it's resistance to change. Organizations have invested years in Gerber scripts, procedures, automation and supplier relationships. Summit participants advised against replacing everything overnight and recommended proceeding collaboratively and systematically:

- Count TQs, emails, engineering hours, documentation discrepancies and supplier data-preparation time.
- Generate IPC-2581 alongside your traditional package and compare the results internally.
- Choose a previously manufactured, known-good PCB for a pilot.
- Send both packages to your manufacturing partner and jointly review the differences; some may reveal issues in the traditional package.
- Repeat across several designs until both parties feel confident.
- Engage suppliers early: "We want to move to IPC-2581. How can we work together to make this successful?"

What's next? Version 4.0 and the digital factory. Summit participants reviewed IPC-2581 version 4.0 and related standards work. The Consortium is also working on DfM rules exchange and on updates to IPC-9252, the electrical test standard. The updates would recognize IPC-2581 and ODB++ rather than relying solely on Gerber, and would reconsider requirements for separate netlists when equivalent intelligent data already exists.

Collaboration makes the difference. No single OEM, software supplier, fabricator or assembler can solve every challenge of digital manufacturing exchange alone. The Consortium offers a forum where competitors collaborate on a common standard while continuing to differentiate their products and services. An OEM identifies a missing capability; a fabricator explains the impact; a software supplier helps implement it; others review, validate and improve the result.

The development priorities of a proprietary format should not constrain innovation. The industry needs a standard that can evolve with its requirements. That is the promise of IPC-2581, and the strength of the Consortium behind it.

The time to begin is now. The third Adoption Summit demonstrated that intelligent PCB data exchange is happening today. One OEM's production experience, Aegis' EMS/CM adoption, a large, influential OEM's move toward bidirectional supplier exchange, Polar's stackup exchange implementation, Cadence's manufacturing specifications and the emerging digital TQ workflow all point in the same direction.

Start with one known-good design. Generate IPC-2581. Compare it with the traditional package. Work with your

manufacturing partner. Learn from the differences and repeat.

If you encounter challenges, reach out to the IPC-2581 Consortium. Members across the design and manufacturing ecosystem will share their experience and expertise. Visit ipc2581.com for information and the software support matrix, or contact info@ipc2581.com.



HEMANT SHAH is an EDA veteran and chair of the IPC-2581 Consortium (ipc2581.com). Shah led the effort to create an industry-wide consortium of design and supply chain companies to get IPC-2581 – the standard for transferring PCB design data to manufacturing – adopted.

He spent 20 years at Cadence as product manager for various PCB design products. Shah also led the industry adoption of the IBIS-AMI algorithmic modeling standard. Prior to joining Cadence, Shah worked at Xynetix and Intergraph. He is passionate about developing and marketing leading-edge software products for PCB design.

"By far the best investment you can make is in yourself."

-Warren Buffett

famous investor-
really rich dude
white hair



Invest in Yourself

PCEA TRAINING

Register Today!

Comprehensive PCB Design Training

NEXT CLASSES:

Jan. 15, 22, 29, Feb. 5, 12
Mar. 19, Apr. 2, 9, 16, 23
Apr. 26-30 (in person at PCB East)

Check the website for more classes added throughout the year.

pceatraining.net

Applying Lean Manufacturing Principles in a High-Mix Environment

Applying Lean manufacturing principles to high-mix electronics assembly can reduce changeover times, streamline production workflows and improve quality through standardized processes and automation.

MILITARY, AEROSPACE AND space hardware often involves low- to medium-volume production and must meet rigorous standards. While applying Lean manufacturing principles to these environments may not yield the same productivity gains as high-volume manufacturing, selective use of Lean principles can improve factory cycle times and eliminate opportunities for defects. Additionally, Lean best practices share many similarities with established practices in the military and aerospace sectors. Axiom Electronics, an electronics manufacturing services (EMS) provider in Hillsboro, Oregon, incorporates Lean principles throughout its production floor.

One example of a parallel practice is foreign object debris (FOD) prevention. Something as simple as a loose screw can cause shorts or other damage if it rolls around inside aircraft hardware during flight. Consequently, most military and aerospace programs require FOD prevention programs. Our team combines FOD prevention and 5S to create a culture of daily cleaning, using checklists to verify that cabinets, workstations, racks, and carts remain clean and organized. Employees update shadow boards and account for all tools, verify their working condition, and confirm compliance with required calibration schedules. They also identify materials in refrigerators and on carts and check consumables against their expiration dates. The team validates adherence to electrostatic discharge (ESD) requirements and removes any material it identifies as FOD from the area. Auditors review the nonconformances that production personnel identify through their checklists to verify compliance.

In the SMT area, the team uses Lean practices to reduce changeover times and streamline first-article documentation. Each line has duplicate feeders, allowing the setup team to prepare feeder tables for the next job while the current job runs. As the previous job finishes, operators switch the tables and return the used tables to the setup team for preparation ahead of subsequent production runs.

The team classifies each production order as either a first-piece job or a rebuild. For first-piece jobs, inspectors must approve the first board before operators queue additional boards for production, since initial production may require process optimization. For rebuild jobs, the first piece still undergoes a full inspection, but operators can queue additional boards through the steps preceding reflow because the team has already validated the process. Once the inspector approves the first piece, the line can immediately begin running.

The company also applies Lean principles to its software choices. While the SMT line software tracks placements,

misaligned parts, and dropped components, sharing that information requires additional interface licensing. The company's manufacturing execution system (MES) can import machine data and optimize groups of SMT jobs to reduce changeover time, so the team now uses MES as its primary line optimization tool.

The MES reviews production schedules and groups jobs by customer, considering component commonality and optimizing reel placement so operators can run multiple jobs for the same customer consecutively without changeovers. The team is also validating the MES software's ability to track component usage and reconcile available component counts within the enterprise resource planning (ERP) system by auditing returned reels with X-ray counters. Operators currently perform this process manually, but once validation is complete, the system will fully automate daily cycle counting and ERP reconciliation.

The company also uses specialized software to meet AS9102 first-article documentation requirements. This software allows the team to prefill initial information and add annotations as products move through production.

The overall factory layout also follows Lean principles. Materials enter one end of the factory and exit through the other. Secondary assembly workbenches feature standardized soldering irons, solder wire, and hand tools. In the system integration area, the company dedicates one work cell to a long-term customer with continuous demand, while other areas serve as flexible work cells with tables on wheels that operators can easily rearrange.

Together, standardized equipment, consistent practices, and appropriate automation reduce the variation that can otherwise lead to mistakes and defects in a high-mix environment. Checklists provide particular value by helping the team address all requirements consistently.



ROB ROWLAND is Axiom Electronics' director of engineering operations. He can be reached at rob.rowland@axiomsmt.com.

360CIRCUITS

Full-Service
Marketing Agency

::: WITH A PASSION FOR ELECTRONICS :::

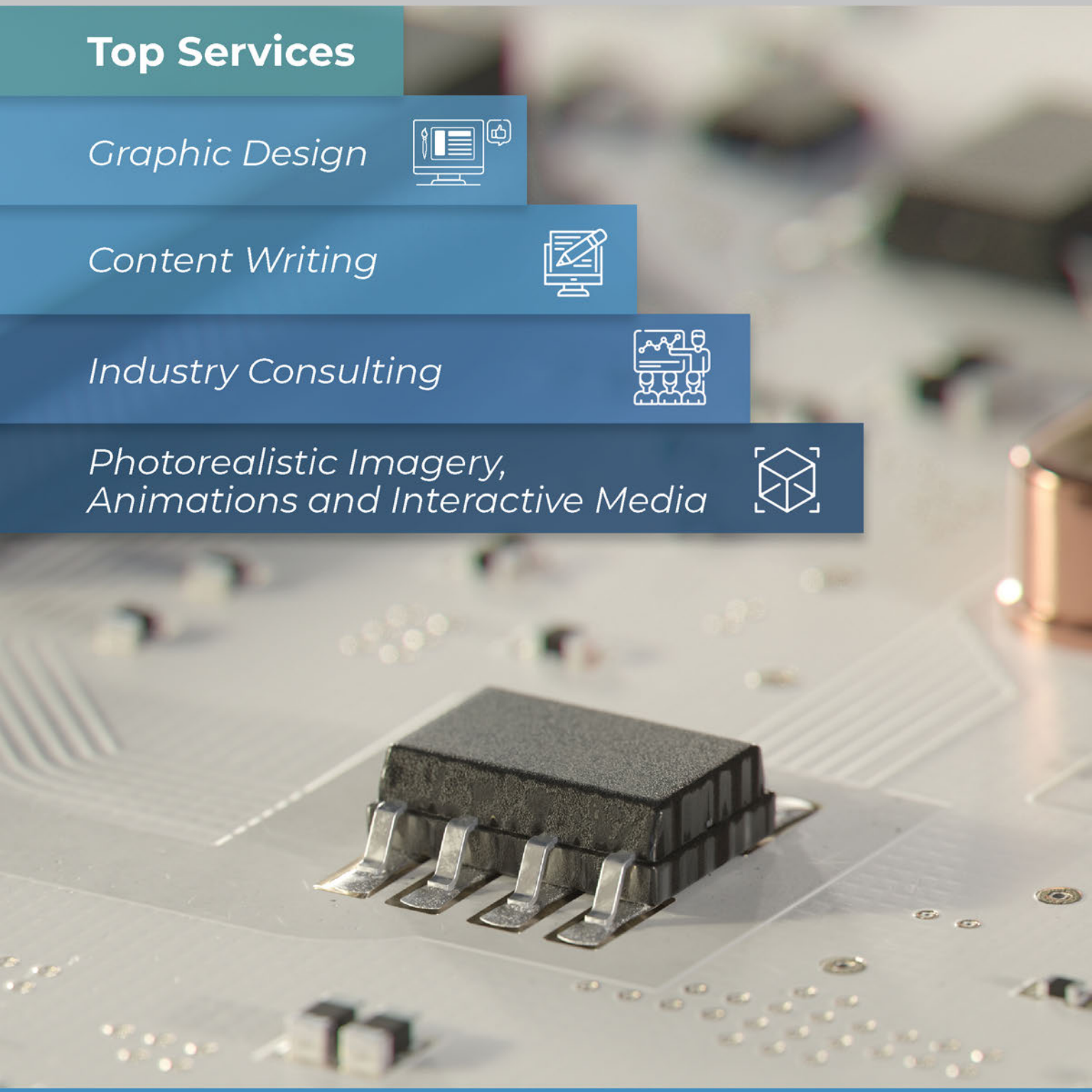
Top Services

Graphic Design

Content Writing

Industry Consulting

Photorealistic Imagery, Animations and Interactive Media



www.360circuits.com

SEEING IS BELIEVING

The Last Word

Eight board revisions, a vanished supplier and a combative purchasing manager turn a routine test fixture project into a costly lesson in accountability.

HEREWITH A CASE study in mistimed malediction. Last year I visited a literary exhibit in New York City with three family members. While minding our own business, enjoying the exhibit, we had an unplanned, non-literary encounter. Two of my family members, who had not seen each other in a year, were chatting, while my other family member and I were absorbed in the exhibit. Suddenly, another visitor to the exhibit started admonishing the two conversationalists for, in his opinion, speaking too loudly. Evidently, their chatter provoked involuntary dyspepsia in the listener, something he did not pay for with his admission ticket. His own concept of injustice provoked rage, and he asserted his rights as he defined them. He complained, loudly, directly, and bitterly, that he did not come to the exhibit to have his thoughts drowned out by idle chatter.

Heavens. When my relatives both begged to differ with his opinion (the term "freedom of speech" was used effusively) – politely telling him, in effect, to get lost – he responded by saying, with remarkable discernment, "Typical liberals." By this point all four of us had abandoned hope of tranquil museum-going and were bracing for battle.

The incongruity of the situation briefly muted my relatives. You don't expect this sort of engagement in a portrait gallery. Maybe New Yorkers are overly sensitive (I've heard rumors). Regardless, we regrouped, girded our loins, and focused our indignation on our antagonist, who vanished when we complained to museum security. I walked away from the incident thinking of a dozen witty comebacks; those perfect putdowns you remember in the shower, under controlled laboratory conditions, the next day, when the crisis has long passed. Add regret about timing, that I wasn't able to respond with impact in the moment.

I was, I confess, frozen in an instant by the abrupt nature of the encounter (Memo to self: reaction times need work). My cousin, by delightful contrast, had no such hesitation. She let him have it, in anatomically explicit, obliterating single-syllable terms, doubtless prompting the "liberals" epithet.

Replaying these episodes risks becoming an obsession. "If only I said this," or "I wish I'd responded that way." Just like it was drawn up. Retaliation is in. We have role models.

One year later.

I've extricated myself from a video meeting with an OEM purchasing manager who graced the proceedings like a malignant toad. The kind that poisons whatever it contacts. The man exuded the discreet charm of a Stalinist prosecutor during 1930s show trials. We were convicted before the trial began. Only sentencing remained. All this

before a word was spoken (if looks could kill). Stereotypes are such great time-savers.

My family believed in having the last word. More than an aspirational goal, it was blood sport. My mother was the oldest of eight siblings. Her mother, my grandmother, overtly and by insinuation, manipulated her brood to compete against one another in every endeavor in life. School. Sports. Extracurricular activities. Relationships. Vacations. Marriages. Neighborhoods. Professions. Possessions. It was made plain they were to play to win, to toughen themselves against the world and especially against each other. Being compliant Irish Catholics, they did and accepted the hard knocks as character-building.

To this day, the siblings can barely endure being in the presence of each other. Funerals and other appeals to maturity aren't enough to bring them together. On those extremely rare occasions when obligation trumped contempt, my aunts and uncles would engage in parlor games of one-upmanship. Naturally, this only reinforced mutual antipathy. Siblings died alone and to the relief of other rival siblings. So, they rarely met. When they did, it wasn't pretty. Leaving the scene having uttered the last word was a winning hand. They kept score. For decades.

So much for warm family history. Back to the Toad and summary judgment. Our heinous crime?

Raising prices.

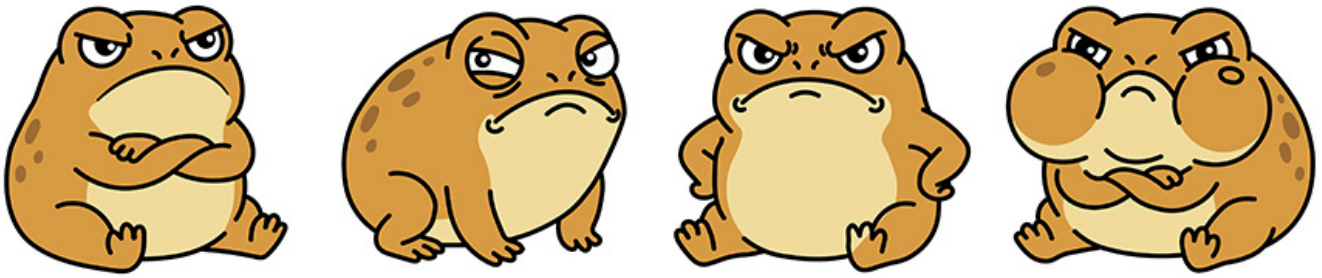


Figure 1. When design changes pile up, someone has to swallow the added costs.

We are trying to build an in-circuit test (ICT) fixture and program for this company. The operative verb is "trying." When we first quoted the project, in December 2025, the board revision was A. It went to C in March, then to F in May. We received an order in June and started pre-production fixture design engineering. Within a week of receiving our PO, we placed a PO with our fixture fabricator, our subcontract machine shop that actually bends metal, wraps wires, and inserts test probes, to our specifications. Four days after our order placement, the OEM's contract manufacturer (our direct customer) put the job on hold, saying that design errors had been found, and the OEM was spinning the revision again.

That was June. In late September, we received fully validated, new-revision files. Revision H.

As responsible test engineers, our job is to review the changes, advise the customer (often two customers, both the

contract manufacturer and their OEM) of the cost ramifications, up or down, and revise our pricing accordingly. Customers frequently make this evaluation unnecessarily hard, failing to document their changes in official ECOs; it falls to us to do their job for them and be detectives, performing side-by-side forensic analysis of old versus new data files, noting the differences, adding and subtracting test probes, and rewiring the fixture accordingly. Naturally, this takes time, time that is billed to the customer. With eight revision changes in nine months (some of which were not shared with us, the test engineers, during the interim stages of design, thereby adding discovery and comparison time), there is much to be discovered, reviewed, and re-engineered. All billable hours. Time remains money.

In addition to eight revision changes, this project was graced with an Act of God: a key parts supplier closed its doors. This board design required the addition of LED probes to the test fixture, to measure color and intensity. The customary LED sensor supplier, rudely, went out of business during the time between being placed on hold in June and the release of new ("definitive") files in late September. A new, and more expensive, LED sensor was now the only available alternative to meet requirements.

The combination of fixture wiring and probe changes dictated by the latest board revision, as well as the switch to a new LED sensor supplier, meant a significant price increase. We revised our quote and sent it to the contract manufacturer, who forwarded it to the OEM, landing on the desk of the purchasing manager (the amphibian-like person). The purchasing manager, doing his job, sent questions back through the contract manufacturer, asking that we explain and justify the extra costs. This we did, in detail, repeatedly, in multiple emails. However, the detail was not sufficiently persuasive to the Amphibian. He called a Teams meeting for Monday morning, early. Just a friendly chat.

We logged into an ambush. The proceedings began with a rant. You know things are going south when the purchasing manager, unsmiling, prefaces the discussion by saying, "I can't believe you want to charge several thousand dollars for additional engineering. These are simple changes. They can be done very quickly, and in far less than the eight hours you're proposing to charge us. Furthermore, the fact that your LED sensor supplier went belly-up doesn't preclude you from finding the same sensors on the grey market. And finally, you should not have started work on this project in June, knowing that additional changes were coming." Thus read the three counts in our Bill of Indictment, cleaned up linguistically for tender ears. Nice to meet you too.

But it's one year later. I'm older. My cantankerous chromosome is taking charge. My I-Don't-Care chromosome is riding shotgun. No more Mr. Nice Guy. Coloring between the lines is for losers. Intimidation wins, especially when it's a cover for ignorance. It also runs the risk of provoking an equal and opposite reaction.

Too bad, Toad. Just your luck that age and frustration and DNA combine in one moment, and that moment is now. Enough with reasoning and propriety. I blast.

"Excuse me? How much time do you think it takes to compare eight revisions? What we are charging you incrementally is *less* than what you *should* be charged. Somebody has to review these changes and determine what they mean, and what they'll add to cost. The LED sensor maker's closure was beyond our control, and there isn't any grey market for these sensors as their applications are semi-custom and, therefore, built to order.

“Finally, to your point that we should have anticipated further changes and not commenced fixture fabrication, two responses: 1) We are test engineers, not clairvoyants; and 2) we start and stop based on instructions from our customer, your supplier, the contract manufacturer. We did as we were told. You made the changes, not us. If you think those changes don’t carry a cost with them, you’re living in a universe of your own making.”

Extended silence followed. On his side, a comeuppance. On our side, therapeutic relief.

The Toad had a companion lurking with him in his office during the call, providing “technical support.” That companion was the board designer—Mr. A through H—who guiltily admitted, tensely, to the purchasing manager that he should have done a better job of keeping him informed of the nine-month parade of board changes. The designer’s voice tightened to a fly-like whisper as the call progressed. Amphibians eat flies.

Better job indeed. Two days later, we got the revised PO, with all requested cost increases included.

And that, my friends, is the last word.



ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.



PCEA Corporate Membership

Enjoy the benefits!

Global reach of **50,000+ industry professionals**

Highlight your **brands, products & services**

Discounted events, exhibits & more

Comprehensive **online reources**

Price points for every budget

PCEA®
PRINTED CIRCUIT ENGINEERING ASSOCIATION

Join today!

pcea.net/pcea-membership

PROTECTION **DECISIONS**

Selecting Via Protection for PCB Design and Manufacturing

Selecting the right via protection method requires balancing design requirements, material properties, assembly reliability and manufacturing costs.

by AKBER ROY

When applying IPC-4761 via protection in PCB design, understanding the standard's seven protection types is only the starting point. Designers must also determine which protection method best suits a particular PCB and why. A via near a component pad may require different protection than a conventional routing via, while high-density layouts, ball grid array (BGA) patterns, via-in-pad structures and sequential lamination introduce additional requirements.

Via protection involves more than appearance. IPC-4761 identifies several practical benefits, including preventing contamination and corrosion, reducing solder migration and solder balling, improving vacuum handling and in-circuit testing, supporting planarity for subsequent dielectric processing, and preventing adhesives or encapsulants from entering vias. However, protection methods also introduce fabrication, assembly, reliability, material and cost considerations.

The appropriate method depends on board layout, circuit density, assembly processes, electrical testing requirements, operating conditions, material compatibility, manufacturing capabilities and cost. Rather than selecting the most elaborate protection method, designers should choose one that meets performance requirements while supporting consistent fabrication and assembly.

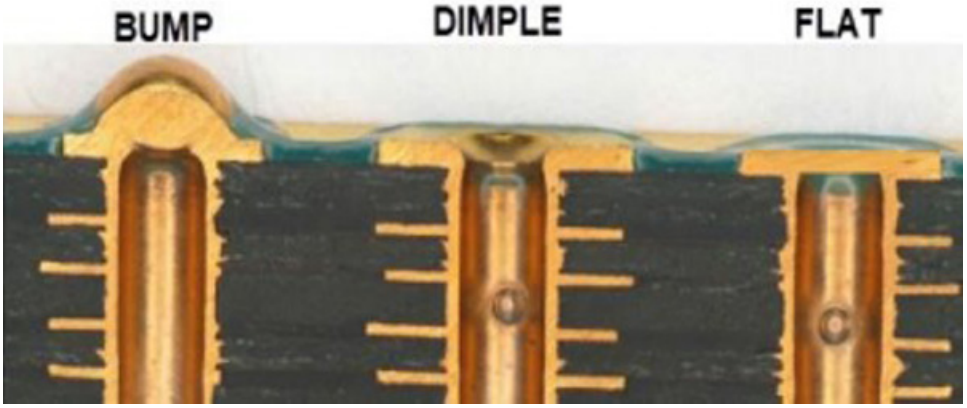


Figure 1. IPC-4761 via protection types illustrate different methods of covering, plugging, filling and capping vias to meet PCB fabrication and assembly requirements.

Beyond Via Protection: Why the Final Surface Matters

The finished surface of a protected via can range from a raised bump to a substantially planar surface. Removing excess plugging or filling material can make the protected area nearly coplanar with the surrounding surface. This distinction matters because surface geometry directly affects assembly.

IPC-4761 notes that solder paste stencils require contact with a relatively flat surface to create an effective seal, or gasketing effect, around solder pad openings. The standard also defines bump height as the difference between the height of the solder mask over the via and the height of the adjacent solderable land.

Bump heights of approximately 0.076mm (0.003in) or greater can prevent proper contact between the stencil and PCB surface during solder paste application. Dimples also raise concerns because they can trap air or contaminants. IPC-4761 notes that air trapped in dimples can contribute to voids in BGA solder joints.

Planarity becomes particularly important when designers place surface-mount technology (SMT) components directly over protected vias. Bulged, erupted or popped vias can interfere with component placement and cause soldering defects.

Designers should not assume that a filled or plugged via has a planar surface. Filling and planarization represent separate manufacturing considerations. The final surface depends on material application, curing and finishing processes, including whether the fabricator removes excess material.

The material inside the via matters. Selecting a via protection type represents only part of the decision. Plugging and filling materials also influence the finished structure because their properties affect filling, curing, shrinkage, planarity, plating, thermal and electrical performance, assembly compatibility and long-term reliability.

IPC-4761 identifies several categories of materials for filled and plugged vias.

Nonconductive, nonimageable organic materials. These polymer-based formulations may contain additives that increase viscosity and reduce shrinkage during processing and curing. Manufacturers use them in many general-purpose applications and typically cure them through thermal processing, ultraviolet (UV) exposure or a combination of both.

Photoimageable materials. Photoimageable materials are particularly useful when protected vias sit among fine-pitch features. The imaging and developing processes remove material outside the intended protection areas.

These materials benefit high-density circuit areas, including BGA patterns, by limiting plugging material spread onto adjacent solderable pads, where contamination could interfere with soldering.

Conductive plugging materials. Conductive plugging materials contain polymers filled with metal particles, typically silver or copper. The polymer composition and metal loading determine their electrical and thermal properties.

Increasing the metal content can reduce shrinkage during curing and may support subsequent plating processes,

depending on the material formulation and process requirements.

The filling method also affects the results. Manufacturers can fill vias through screen printing, direct squeegee application or pressurized dispensing. Filling performance depends on via diameter, aspect ratio, material viscosity, filler particle size, equipment and process parameters.

Via Geometry Matters: Diameter and Aspect Ratio

Via geometry directly affects the ability to consistently plug or fill a hole. IPC-4761 identifies via diameter and aspect ratio as important considerations.

Very small holes can complicate material application, while large holes can also be challenging to fill. As aspect ratio increases, manufacturers generally face greater difficulty achieving a complete, reliable fill.

Designers must evaluate geometry alongside the surrounding PCB layout. Circuit density, particularly the distance between exposed component pads and protected vias, can influence material selection.

In dense BGA patterns, photoimageable plugging materials may help prevent material from spreading onto adjacent solderable pads.

Electrical testing requirements can also influence the decision. Some designs require partially filled vias to preserve access to test points on the opposite side of the board. This requirement can affect PCB construction, surface finish and plugging material selection.

A via that appears straightforward in a computer-aided design (CAD) layout may present a more complex manufacturing challenge.

Fabricators must consider how material enters the hole, whether it fills the opening completely, how it cures, and whether voids or shrinkage may develop. They must also determine whether to remove excess material and whether the finished surface requires plating or another surface treatment.

Manufacturing Considerations: Every Protection Method Has a Cost

Designers may assume that the most advanced via protection method provides the best solution. However, the appropriate method must balance performance requirements with manufacturing practicality and cost.

Via filling and protection can require specialized materials, equipment, processing steps and labor. Material qualification, expected yield, equipment compatibility, curing, void control, planarization and plating all influence manufacturing decisions.

The instruction to simply fill the vias overlooks these variables.

An effective via protection strategy accounts for both design requirements and the fabricator's ability to manufacture

the structure consistently, inspect it reliably and maintain reasonable production costs while meeting applicable IPC-4761 requirements.

Assembly changes the equation. Designers cannot select via protection based solely on PCB fabrication requirements. Protected vias must also withstand assembly temperatures and chemicals without losing adhesion, changing shape or causing defects.

IPC-4761 identifies several considerations when selecting protection materials, including resistance to assembly temperatures and chemicals, surface height and planarity, processing shrinkage, plating adhesion, compatibility with fluxes, cleaning agents and conformal coatings, and compatibility with the PCB substrate.

Surface geometry remains particularly important. Solder paste stencils require relatively flat surfaces for proper contact. Excessive bump height can interfere with stencil gasketing, while dimples can trap air and contribute to BGA solder joint voiding.

Protected vias can also trap flux residues and contaminants that become difficult to remove, particularly beneath component bodies. Via protection can affect solder volume and solder joint formation. Open vias near solderable lands may draw solder away from a joint during reflow.

Trapped air can also expand during reflow and crack a solder mask tent or cover, causing the material to lift and creating coplanarity problems. Moisture introduces another concern. Via-fill materials can absorb moisture during storage. IPC-4761 notes that some PCBs may require baking before soldering to remove moisture and improve protection reliability.

There Is No Universal Best Via Protection Method

No single via protection method suits every PCB.

Designers may need protection to prevent air, solder or chemicals from passing through or becoming trapped in a via. Other applications require protection of dielectric structures, support for sequential lamination, improved surface planarity, thermal conductivity, or prevention of solder and adhesive migration.

A conventional routing via may need only basic protection. In contrast, BGA, sequential-lamination and via-in-pad applications may require tighter surface control or a filled and capped structure, such as IPC-4761 Type VII.

The appropriate choice also depends on whether the application requires protection on one or both sides, the required planarity and reliability, and the fabricator's processing capabilities.

Rather than asking which via protection method is best, designers should ask what the via needs to accomplish and which protection method can meet those requirements reliably and consistently.

AKBER ROY is CEO and founder of RUSH PCB Inc., an electronics manufacturing company specializing in PCB design, fabrication, and assembly services; roy@rushpcb.com (rushpcb.com).

PCB EAST 2027

Conference & Exhibition

Save The Date!

Conference:
April 27 – 30

Exhibition:
Wednesday, April 28

DCU Convention Center
Worcester, MA

colocated with FPGA Horizons

FPGA HORIZONS
BEYOND GATE ARRAYS

pcbeast.com

CONNECTOR **INTEGRITY**

Layout and Connector Footprint Strategies for Industrial EMC and Signal Integrity

Connector footprint design plays a critical role in electromagnetic compatibility and signal integrity, with return paths, shielding and grounding strategies helping ensure reliable performance in industrial electronics.

by DENNIS CHIANG

Industrial controllers, PLCs, machine vision systems and automation electronics move data through electrically noisy environments: near motor drives, contactors, welders and dense cabinets of switch-mode supplies. When fieldbus communication becomes unstable or a product fails a radiated-emissions test, the investigation usually starts at the transceiver or the cable. In many cases, the weak point is much narrower: the transition between the PCB and the external cable, the connector footprint and the centimeter of routing on either side.

Connectors are selected for pin count, current rating and mechanical fit, then dropped onto the layout as a land pattern. Electrically, that footprint is part of the transmission path.

No connector, however well made, fixes an EMC problem by itself. Failures rarely originate in a single component; they appear where PCB layout, connector interface, cable routing, shielding, grounding strategy and mechanical integration meet.

Why Connector Footprints Matter in EMC and Signal Integrity

A PCB connector footprint is not only a mechanical pattern. Every signal that leaves the board does so as a loop: current flows out on a signal pin and returns on a ground pin, a shield or adjacent cable conductors. The footprint and pin field define that loop.

Above a few hundred kilohertz, well within the harmonic content of ordinary digital edges, return current concentrates beneath its signal conductor, following the lowest-impedance path, which at these frequencies is dominated by inductance. Where that current reaches the connector, it must transfer from the reference plane to a physical pin. If the nearest ground pin is several positions away, the return detours through the pin field and the loop area grows abruptly. Larger loop area means higher inductance, more $L \cdot di/dt$ noise, and more conversion of differential-mode content into common-mode noise – the current that drives cable radiation.

Pin arrangement is therefore an EMC decision, not just a pinout decision. Ground pins adjacent to each signal or differential pair keep the interface loop small and bound pin-to-pin crosstalk inside the connector. On connectors

where every position is precious, engineers sometimes assign all pins to signals and reserve a single ground far away; that one choice can dominate the interface's emissions behavior.

The footprint also fixes where the cable shield lands – at the connector shell or on pads immediately adjacent to it, not on a trace routed 30mm to a mounting screw. Mounting-hole clearances can cut into the copper pour the return currents depend on. In EMC PCB design, these few square centimeters around the connector carry a disproportionate share of the risk.

Designing Signal Paths Through Connector Interfaces

Differential interfaces dominate industrial communication: Ethernet (including PROFINET and EtherCAT), CAN and CAN FD, RS-485/RS-422 and their fieldbus descendants. Signal integrity at the connector boundary in PCB layout comes down to three recurring requirements: controlled impedance where the application needs it, symmetry and a continuous return path.

Ethernet. Route the MDI pairs from the magnetics symmetrically, matched within the pair, on an unbroken reference plane. The 100ω differential target comes from the IEEE 802.3 physical-layer specifications; use the PHY and magnetics data for the exact value and tolerance, since the requirement is application-dependent. Keep the segment between transformer and jack short – it sits on the cable side of the isolation barrier and behaves like a piece of the cable. Return the magnetics bias network to the chassis reference, not to quiet logic ground – each center tap and any unused pairs through 75Ω to a common node, and that node to chassis through a high-voltage bypass capacitor.

CAN and RS-485. These buses are designed around roughly 120Ω characteristic impedance (ISO 11898-2 for CAN; TIA-485 practice for RS-485), with termination at the physical ends of the bus. Route the pair together and symmetrically; asymmetry converts differential content into common-mode. Where the network design calls for common-mode chokes or termination, place them close to the connector on the appropriate nodes – termination belongs at the bus ends.

Discontinuities. Any abrupt change in a signal's environment – a via, a layer change, a plane split, a neck-down, a stub – is a discontinuity. Interconnect behaves as a transmission line once its length approaches a tenth of the wavelength of the highest significant frequency, and in digital signaling the edge rate, not the clock frequency, sets that frequency. With nanosecond-class edges on FR-4, the threshold sits in the single-digit-centimeter range, so even slow industrial buses qualify near the connector. The stackup – dielectric heights and laminate properties – sets what impedance the escapes can achieve. Where vias are unavoidable, place a ground via adjacent to each signal via so the return current can follow.

Pad compensation. Connector pads are typically wider than the traces feeding them, so the pad region adds extra capacitance and dips the local impedance; a TDR sweep will show it. You can partially compensate the dip rather than tolerate it. Impedance follows $Z0 = \sqrt{(L/C)}$, so excess pad capacitance can be offset by modifying the local reference structure – removing copper on the plane directly beneath the pads, or letting the pads reference a deeper layer, either

of which raises the effective dielectric height and lowers C. Keep the cutout bounded to the pad envelope: the signal's return current redistributes around the void, and the added inductance is part of the compensation. A void wide enough to become a slot in the return plane – or to cut into adjacent return paths or connector ground stitching – has traded a capacitive discontinuity for an inductive one. Document the cutout dimensions in the fabrication notes so the void does not drift in CAM.

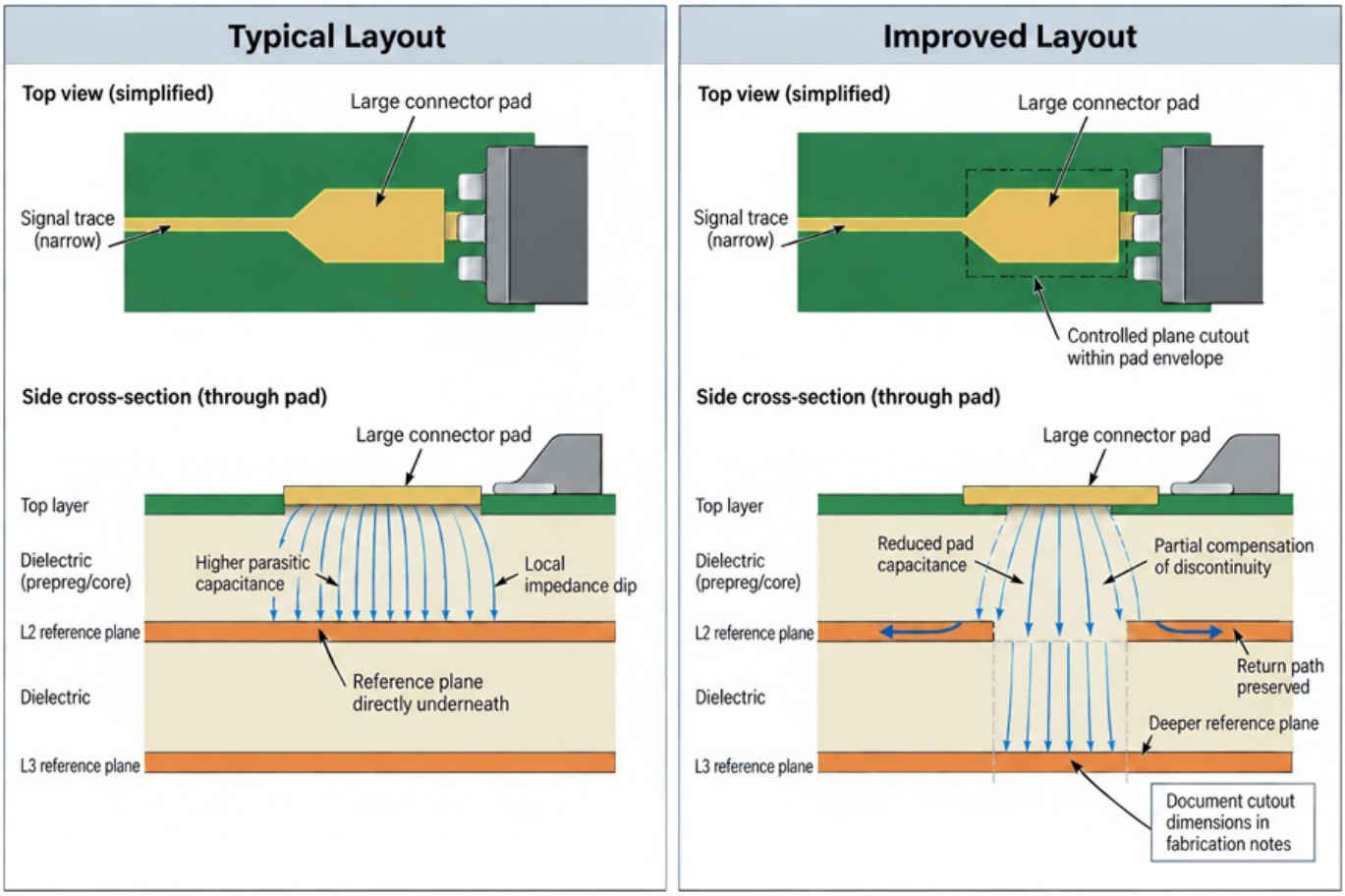


Figure 1. Typical and improved connector pad layouts showing a bounded reference-plane cutout that compensates for pad capacitance while preserving the return path.

Stubs. Through hole and press-fit connectors on 2.0-2.4mm industrial boards add a second mechanism. A signal entering from top-layer pins and escaping on an inner layer leaves the unused drill barrel as a stub, which resonates near a quarter wavelength and appears as a notch in the channel. For multi-gigabit links – machine-vision camera interfaces, 10G backbones – a few millimeters of barrel matter: escape on the layer the pins reach (the bottom layer on a through hole part, so the barrel spans the full board and leaves no stub) or specify back-drilling for the connector via field. For typical fieldbus data rates, stub length rarely limits performance; back-drilling cost is justified mainly on multi-gigabit channels.

In high-speed connector layout, the escape region under the pin field is the densest routing on the board, and pinout options freeze once the connector is placed. Plan ground pins and pair placement against the mechanical constraints early.

Shielding and Grounding Transition Challenges

Connector shielding is only as good as its termination. The common defects in industrial hardware: a cable shield stripped back and soldered to a pigtail running 30 to 50mm to a screw terminal; a shield connected only at the far end or tied to logic ground instead of chassis; and a connector shell with no metal-to-metal contact to the enclosure because paint or anodizing intervenes.

High-frequency noise currents prefer low-inductance paths. A useful rule of thumb holds that a straight round wire is on the order of 10nH per centimeter. A 30mm pigtail therefore represents roughly 30nH, which at 100MHz corresponds to $2\pi fL \approx 19\Omega$. That is no longer a shield connection; it is an inductor in series with the shield, and common-mode current that should have returned along it finds other paths – through the board, along other cables, or out as radiation. For interfaces where the cable shield is intended to control high-frequency common-mode current, 360° termination becomes increasingly important as frequency rises.

The preferred geometry is 360° contact: the shield bonded around its circumference to the connector backshell, and the backshell bonded to the chassis through the connector mounting. On the PCB, this means shell contact pads and mounting features tied to the chassis reference through multiple stitching vias, with copper continuous around the connector perimeter. Where a gap remains between the panel cutout and the connector flange, the gap behaves as a slot antenna; a conductive gasket restores the circumferential bond.

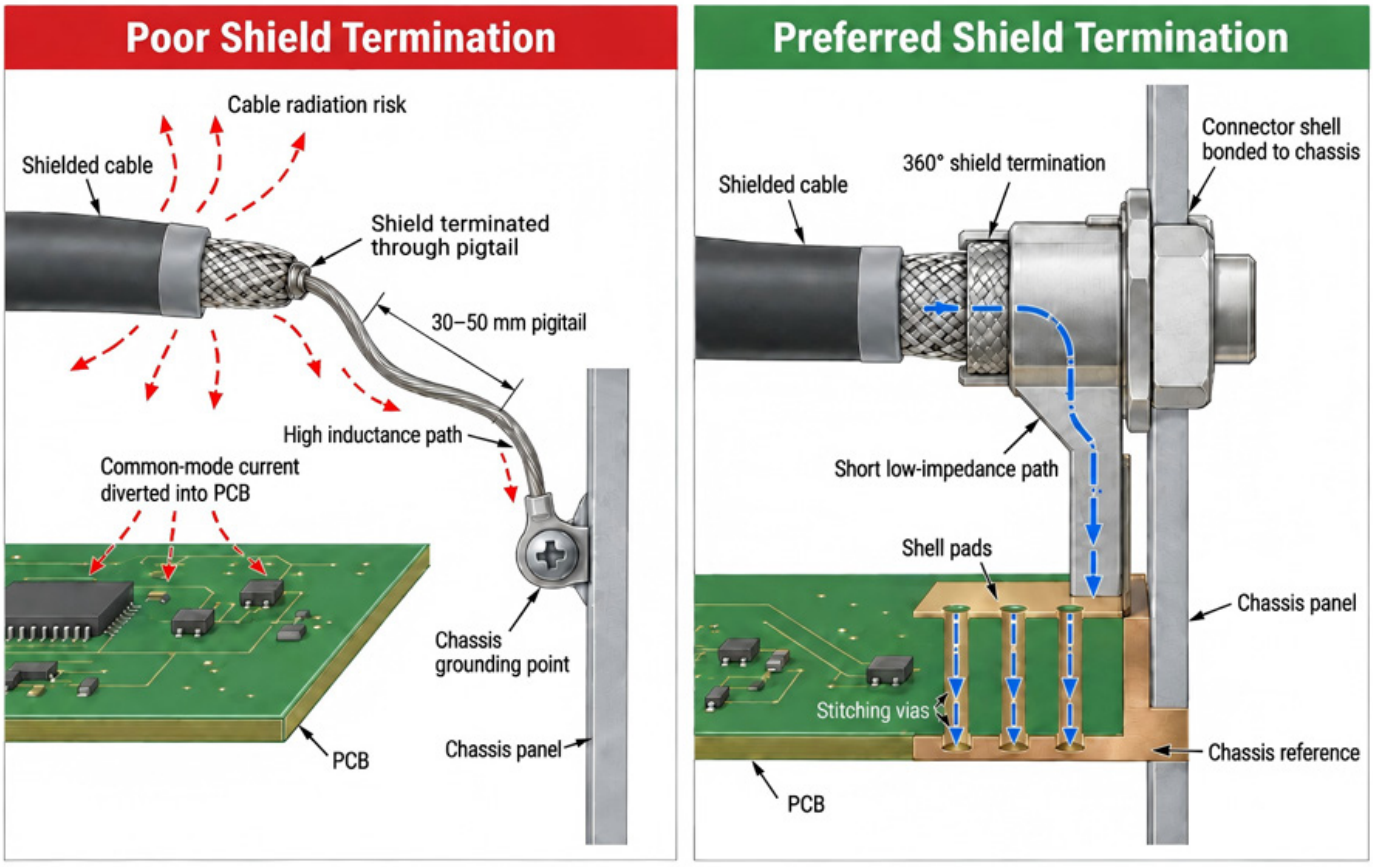


Figure 2. Comparison of poor pigtail shield termination and preferred 360° connector-shell termination with a short low-impedance return path.

The grounding scheme deserves the same attention. Industrial products carry three distinct references: protective earth, the chassis structure and signal ground. PE is a safety function and bonds to the chassis per the applicable standard, typically at power entry. The chassis-to-signal-ground connection is an EMC decision, a direct bond, a single-point connection near the I/O, or an RC network, each suited to different system architectures, safety requirements, and EMC objectives. Hybrid schemes commonly use a safety-rated (Y-class) capacitor in the low-nanofarad range, paralleled by a 1MΩ bleed resistor, across the chassis-to-signal-ground boundary: the capacitor shunts RF common-mode current to chassis while blocking 50/60Hz circulating currents, and the resistor bleeds off static charge. Values vary with the end product's EMC and safety constraints, and must satisfy the leakage-current limits of the governing safety standard.

Protection components obey the same geometry. ESD (IEC 61000-4-2) and electrical fast transients (IEC 61000-4-4) inject pulses at the connector, with peak currents that can reach tens of amperes depending on the test level and coupling path. For signal interfaces exposed to these threats, the TVS normally sits between the connector and the transceiver – the first component the line touches – with its ground pad given the shortest, lowest-inductance path to the chassis reference, typically a wide pad with several vias. Routing the discharge current through the board's digital reference couples it into everything else. Where the interface also carries filtering, isolation or fusing, coordinate the protection order against the threat mix and the channel budget; on high-speed lines, TVS capacitance counts in that budget. Power inputs and surge events call for different protection structures.

Cables are efficient antennas, and from 30-300MHz they often dominate radiation in an industrial product. The shield and its termination keep common-mode noise off those antennas; the footprint determines whether that termination is physically achievable.

A Practical PCB Layout Checklist

1. **Place connectors according to signal flow.** Group interfaces by noise class. Keep power entry, relay and motor-drive circuits away from fieldbus and low-level analog connectors, and keep noisy nets out of the routing between sensitive connectors.
2. **Dedicate board area to shield termination.** Provide shell contact pads, mounting holes and stitching vias at the connector edge, with copper continuous around the perimeter – a chassis-referenced copper strip on the order of 5-10mm is a reasonable starting allocation, to be adjusted to the connector and enclosure interface. Verify that the enclosure actually contacts these features.
3. **Keep protection and filtering at the boundary.** TVS devices, common-mode chokes and ferrites belong immediately at the connector, not centimeters downstream – the unfiltered segment still couples. Route TVS grounds to the chassis reference by the shortest path.
4. **Maintain return-path continuity.** No signal crosses a plane split or a mounting-hole void near the connector. Assign ground pins adjacent to each signal or pair, and pair every layer-change via with a ground return via.
5. **Review mechanical and EMC requirements together.** Shell material, gasket compression, panel cutout,

board-to-panel spacing and stackup determine whether the shield termination designed in copper exists in metal. Bring the enclosure drawing into the layout review.

Example Application Scenario

An anonymized example shows how the weaknesses combine. An industrial controller on packaging machinery suffered intermittent fieldbus dropouts; the faults correlated with motor braking events and appeared only when the controller was mounted in the main cabinet near the drives.

The investigation found two issues at the connector transition area. The fieldbus cable shield was landed on a small pad and routed roughly 40mm across the board to a chassis mounting hole – an inductive termination at exactly the frequencies where braking noise was strongest. The differential pair also escaped from the connector between two mounting holes whose clearance voids interrupted the ground pour, forcing the return path to detour around them. Neither defect was visible in the schematic. Both lived entirely in the layout.

The revision bonded the shield to the connector's shell pads with a row of stitching vias, reassigned the pinout so a ground pin flanked the differential pair, and rerouted the escape clear of the voids. Retested under the same conditions, the faults did not recur. The lesson is not that the connector was wrong; the same connector with a different footprint and pin assignment was adequate. The weak point was the transition, and we corrected it there.

Connector interface design belongs in the PCB architecture phase, not in post-test remediation. By the time a board fails at an EMC lab, the connector is soldered down, the pinout is frozen, and the wide, short, 360° shield bond that should have been designed in has become a pigtail and a screw.

Treat the connector footprint as electrical circuitry: pin assignment chosen for loop area, pad capacitance compensated where impedance matters, stubs removed or back-drilled, escapes routed for symmetry and continuous return paths, shield termination given board area and genuine metal-to-metal contact. In industrial electronics PCB design, these decisions cost little if addressed early. No connector fixes EMC by itself; the layout, connector interface, cable, shielding, grounding and mechanical integration, designed together, determine whether industrial communication remains reliable in the field.

DENNIS CHIANG is a technical engineer at Teyconn, focusing on industrial connectivity, connector reliability and cable assembly solutions for automation, machinery and industrial electronics applications.


NPI
NEW PRODUCT INTRODUCTION AWARD
RECOGNIZING THE
BEST
New Electronics Assembly
Equipment, Materials & Software
Nomination Deadline
December 4, 2026
Sponsored by
CIRCUITS ASSEMBLY

HIDDEN **INTERFERENCE**

Stackup Decisions That Prevent EMI Problems Later

A seemingly harmless low-speed feedback trace caused an 18dB emissions failure, demonstrating why stackup reviews must account for high-impedance nets and return paths.

by UJJWAL DATT SHARMA

Designers make stackup decisions during the initial stages of PCB layout, but the consequences often emerge later in the electromagnetic interference (EMI) laboratory. Layer count, copper weight and component placement rank among the most expensive design elements to change after fabrication.

This article examines an early design mistake on a high-speed PCB. The engineering team evaluated the design during planning, but the board ultimately failed electromagnetic compatibility (EMC) pre-compliance testing. The root cause offers a lesson for high-speed design engineers who may overlook a fundamental principle while managing competing design and debugging tasks.

The board was a typical server-grade motherboard of the kind high-speed design engineers encounter regularly. It included a field-programmable gate array (FPGA), CPU, Ethernet switch application-specific integrated circuit (ASIC), multiphase voltage regulators and low-dropout regulators (LDOs).

The design used a 26-layer stackup, Megtron-class dielectric material and six signal layers, including the top and bottom layers. The layout followed conventional design practices. Low-speed signals occupied the outer layers, while high-speed differential pairs used stripline routing between reference planes. The planes above and below the high-speed signal layers provided return paths and helped contain electromagnetic fields.

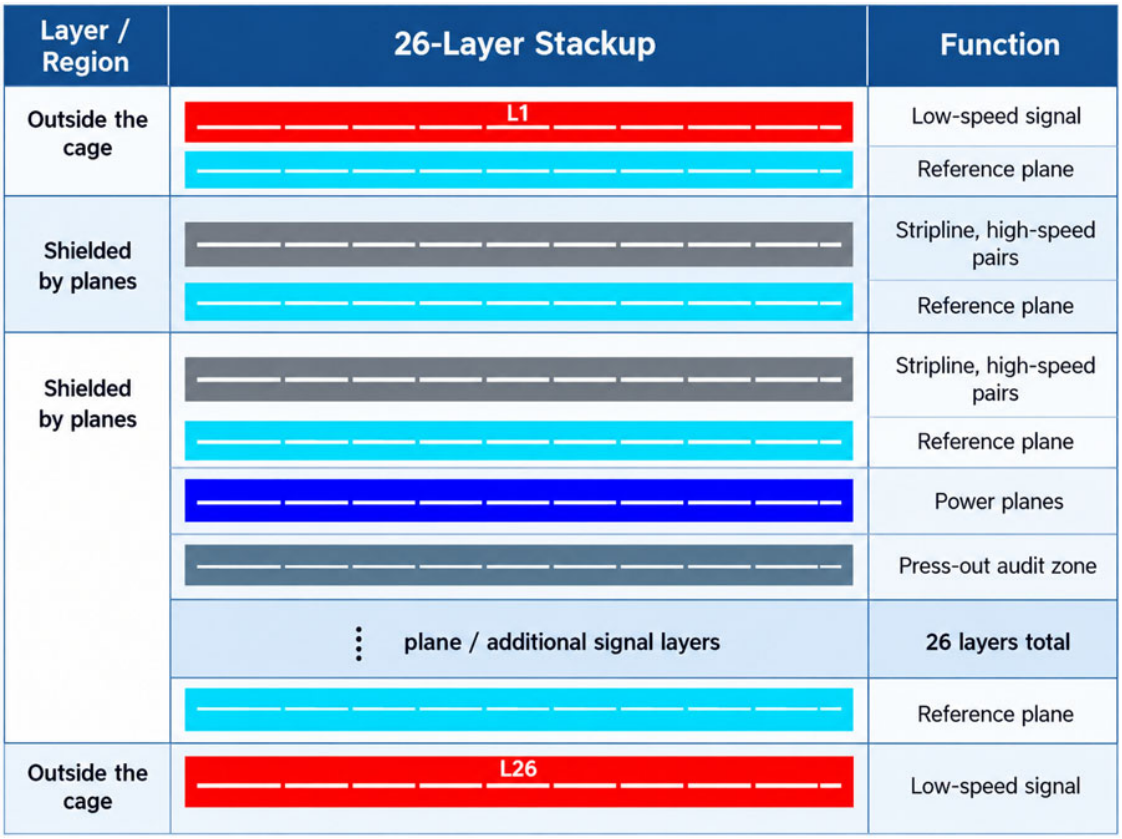


Figure 1. The 26-layer PCB stackup places low-speed signals on the outer layers and high-speed stripline pairs between reference planes.

The failure. The board failed radiated emissions testing by 18dB, with the primary problem occurring near 200MHz. Voltage regulator tuning did not cause the failure. Instead, common-mode noise escaped the PCB through external cabling.

The failure originated in the board's physical design, and a more thorough stackup and routing review could have identified the risk before fabrication.

The emissions-versus-frequency plot showed a peak near 200MHz, indicating that common-mode current coupled into the external cables and caused excessive radiation. This behavior represents a typical EMC pre-compliance failure.

The high-speed signal traces did not cause the emissions problem. Their stripline arrangement provided appropriate reference planes and electromagnetic field containment.

The actual problem escaped attention during stackup review because the team did not classify the affected net as a high-speed signal.

Root cause. The failure originated from a 15kΩ resistor connected to a complex programmable logic device (CPLD) feedback pin. The layout placed the resistor at the end of a long trace on the top layer.

Design reviews often overlook resistor dividers connected to feedback pins because engineers classify these nets as low-speed signals. The DC current through the 15kΩ resistor was approximately 100–200µA, and the design did not

require controlled impedance for the trace.

However, switching noise from a nearby voltage regulator coupled into the long feedback trace. Oscilloscope measurements revealed the resulting common-mode noise, which subsequently coupled into the external cables.

At approximately 200MHz, even a trace measuring only a few centimeters can represent a significant fraction of a wavelength.

Table 1. How a Feedback Node Can Create EMI Issues

Quantity	Calculation	Comments
Rail tolerance	1.0V ±3% = ±30mV	Generic tolerance on a VR
Ripple and noise allocation	10mV	Allowed ripple
Feedback-node impedance	15kΩ	High-impedance termination
Current for 10mV at FB	10mV / 15kΩ ≈ 0.67µA	Current injected
Equivalent current at 50Ω	10mV / 50Ω = 200µA	About 300 times the 15kΩ threshold
Switcher edge estimate	12V / 1.6ns ≈ 7.5V/ns	High-speed edge couples via parasitic capacitance
Frequency estimate	1 / (π × 1.6ns) ≈ 200MHz	Point of failure in EMI scan
Trace length	3–4cm on Layer 1	Exposed path to a high-impedance node

The calculations demonstrate how an early layout decision can create a significant EMC problem. Although the feedback trace carried a low-speed signal, its physical dimensions made it susceptible to radio frequency (RF) coupling.

At approximately 200MHz, a quarter-wavelength in Megtron-class dielectric material can approach 20cm, depending on the effective dielectric constant. A 3-4cm trace therefore represents a meaningful fraction of that length.

A PCB trace may exhibit approximately 10nH/cm of parasitic inductance, depending on its geometry and return path. In this case, the estimated trace inductance reached approximately 35nH.

The switching regulator's MOSFET output capacitance (Coss), along with associated parasitic capacitance, contributed an estimated 18pF. Although the regulator operated at a switching frequency of 500kHz, its fast switching transitions excited higher-frequency behavior in the circuit.

The estimated inductance and capacitance formed a resonant circuit.

Using the LC resonance equation: $f = 1 / (2\pi\sqrt{LC})$

With L = 35nH and C = 18pF, the estimated resonant frequency reaches approximately 200MHz. This calculated frequency closely matched the emissions peak during EMC pre-compliance testing.

The respin. The engineering team made two primary layout changes during the board respin.

First, the team moved the feedback divider network closer to the feedback circuit, reducing the trace length from several centimeters to a few millimeters.

This change eliminated the long trace that had acted as an unintended antenna. Rather than simply reducing the noise amplitude, the modification removed the primary coupling mechanism. Second, the team separated high-speed signal return paths from areas containing dense voltage regulator via structures.

A high-current voltage regulator on a server-grade motherboard can deliver up to 250A. Its layout typically uses numerous vias to distribute current and manage thermal performance.

These vias and their associated antipads can interrupt nearby reference planes and force high-frequency return currents to follow longer paths. The team moved high-speed traces away from these via-dense regions to preserve continuous adjacent reference planes and minimize return-current loop areas.

This approach reduced the need for return currents to detour around large antipads and other plane discontinuities.

The revised board passed EMC pre-compliance testing, although the remaining margin was narrow. The redesign resolved the original 18dB emissions failure, and the team planned additional margin improvements for the next stackup revision.

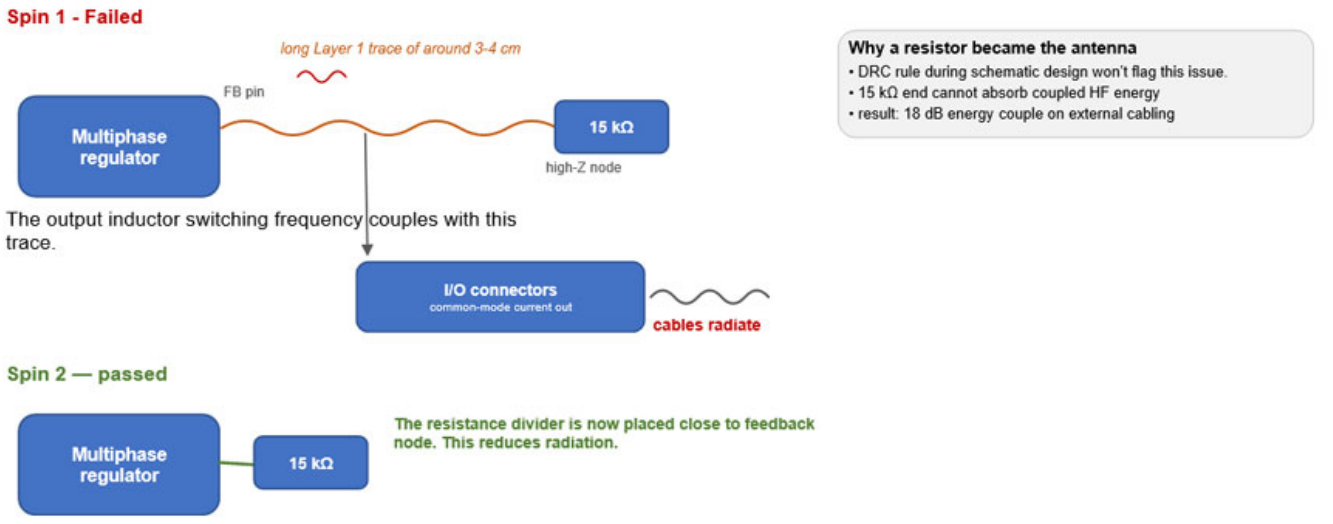


Figure 2. The estimated 35nH trace inductance and 18pF parasitic capacitance produce a resonant frequency near 200MHz, corresponding to the observed radiated emissions peak.

New Considerations for Stackup Reviews

Designers should evaluate any potentially noise-sensitive net as an RF coupling path, regardless of its nominal operating frequency.

Feedback dividers, sense lines, enable pull-ups and other high-impedance connections can become susceptible to switching noise when long traces expose them to nearby electromagnetic fields.

Whenever practical, designers should place these components within a few millimeters of their destination pins. The critical question extends beyond how much current a voltage regulator carries. Engineers must also consider what happens to the switching energy that couples into surrounding circuitry.

In this design, the high-speed traces followed established routing guidelines. The internal reference planes provided shielding that helped contain electromagnetic fields, much like a Faraday cage. However, the emissions problem originated on an outer layer, where the design routed low-speed signals.

Outer-layer routing therefore deserves the same scrutiny as internal high-speed routing, particularly when those signals connect to high-impedance nodes or interact with circuitry near the chassis boundary.

Designers should also review the fabricated stackup rather than relying exclusively on nominal design values.

Heavy copper on internal power planes can affect lamination behavior and dielectric thickness through the board's Z-axis. These variations can influence the finished impedance of high-speed transmission lines.

Before approving a stackup, engineers should verify the fabricator's core and prepreg thicknesses against the impedance requirements and confirm that the finished construction supports the intended transmission-line geometry.

Conclusion

The 26-layer stackup performed as intended for the board's high-speed signal routing, but the design review failed to identify a vulnerable low-speed feedback trace.

Although the internal reference planes contained the high-speed signals, the board still exceeded the radiated emissions limit by 18dB because common-mode noise coupled into external cabling.

The failure demonstrates that stackup design and net placement must work together. Engineers cannot rely on reference-plane shielding alone while overlooking high-impedance signals on outer layers.

A thorough review should consider not only high-speed routing and impedance control but also the placement, length and electromagnetic exposure of sensitive low-speed nets. Otherwise, the engineering team may discover these problems only after the board reaches the anechoic chamber.

UJJWAL DATT SHARMA is a hardware engineer working on high-speed board design, power delivery, and system validation for data center hardware. The board described is from independent research; ushar1@unh.newhaven.edu.

PCB WEST 2026

Conference & Exhibition

ENGINEERING *TOMORROW'S* ELECTRONICS

Thank You

TO OUR SPONSORS

ASC

cadence®

cofactr

EMA Design Automation®

NextPCB

SCREAMING CIRCUITS

Polar® 50 Years

ZENODE

Brought to you by

PCEA®

PRINTED CIRCUIT ENGINEERING ASSOCIATION

pcbwest.com

EMBEDDED **POWER**

Embedded Die Substrate Technology

Embedded die substrate technology combines thick copper heat spreaders, sintered silver die attach and copper microvias to improve thermal management, reduce parasitic inductance and increase switching performance in wide-bandgap power electronics.

by CHRIS PARKER

GaN and SiC transistors switch at high speeds, enabling smaller passive components, higher power density, and improved efficiency. However, the packages, interconnects, and PCB traces surrounding these devices introduce parasitic inductance into the power loop. Even small amounts of inductance can cause voltage overshoot and limit switching performance.

Studies of conventional wire-bonded power modules report loop inductances ranging from 6.7 to 15nH. Reducing loop inductance can decrease voltage overshoot, improving efficiency and reliability. As switching speeds continue to increase, package and layout design can become limiting factors rather than the transistors themselves.

Thermal management presents a similar challenge. Traditional power modules conduct heat through multiple layers, including die attach, substrate, baseplate, thermal interface material (TIM), and heat sink. Each layer adds thermal resistance, while FR-4 circuit boards further restrict heat flow because of their low thermal conductivity.

Embedded die packaging addresses these electrical and thermal limitations by placing the die inside the PCB structure and replacing wire bonds with short copper microvias. This approach can reduce inductance and improve heat transfer.

The embedded die substrate (EDS) architecture developed by TCLAD uses a thick copper heat spreader as its structural foundation rather than an organic laminate core. This construction shortens the thermal path and allows designers to integrate electrical interconnections using established PCB fabrication processes.

Existing Embedded Die Approaches

Several embedded die packaging approaches replace wire bonds with copper microvias and integrate semiconductor dies within PCB structures. The primary differences involve die support, electrical isolation, and heat removal.

For example, Infineon's S-Cell and Schweizer Electronic's p^2 Pack embed prepackaged SiC switching cells within multilayer PCB structures. Published results indicate parasitic inductance of approximately 1–1.5nH. However, heat must pass through a thermally conductive prepreg layer before reaching the cooling system. Reported thermal

resistance for individual cells can be approximately 20% higher than that of comparable ceramic-substrate modules. Distributing multiple cells across a larger board can reduce thermal interaction between devices.

Other approaches, including AT&S's embedded component packaging (ECP), use laser-machined cavities in laminate layers to accommodate embedded components. Fraunhofer IZM has also demonstrated embedded SiC devices using sintered die attach on insulated metal substrate (IMS) or direct bonded copper (DBC) structures, reporting low loop inductance and voltage overshoot of approximately 4% during switching.

In some embedded constructions, heat must pass through an organic material with thermal conductivity of approximately 3W/m·K before reaching a metal heat spreader.

The EDS architecture differs by placing a thick copper heat spreader directly beneath the die at the beginning of the stackup. Rather than relying on a laminate core for structural support, the copper layer serves as both the die carrier and the primary heat-spreading element. This changes the thermal path and reduces dependence on organic materials for heat transfer.

Table 1. Embedded Die Architectures for Power Electronics

Approach	Die Attach	Die Carrier	Isolation to Heat Sink	Loop Inductance
TCLAD EDS (this work)	Low-pressure silver sinter, ≥150W/m·K	Milled pocket in thick Cu spreader, up to 1mm	10W/m·K dielectric (SPL-15)	1–2nH measured
Infineon S-Cell / Schweizer p² Pack	Diffusion solder or Ag sinter	1.27mm Cu leadframe in 6-layer PCB	≥3W/m·K prepreg, 50µm	~1–1.5nH
AT&S ECP	Not published	Thin Cu in laminate core	Laminate build-up	Not published
Fraunhofer IZM	Ag sinter	Cu foil, then laminated	IMS dielectric or ceramic	4% overshoot at 950V
Wire-bonded module (baseline)	Solder or sinter	DBC or AMB ceramic	Al_2O_3, AlN or Si_3N_4 + TIM	6.7–15nH

Embedded Die Substrate Architecture

The EDS architecture begins with a thick copper layer, up to 1mm, that serves as both a structural element and a heat spreader. Instead of embedding a copper slug in a laminate substrate, this approach machines package features directly into the copper.

The process creates two types of cavities. A thermally conductive, electrically insulating dielectric fills the isolation regions, which the fabrication process then planarizes. Precision machining creates die pockets at controlled depths to establish the required die height.

Low-pressure silver sintering attaches each die inside its pocket. Sintered silver provides thermal conductivity of 150W/m·K or greater, compared with approximately 58W/m·K for SAC305 solder.

The process forms the sintered joint at approximately 250°C. Because silver has a melting point of 961°C, the joint does not remelt during conventional subsequent board processing.

Published reliability data indicate that sintered silver die attach can achieve power cycling lifetimes up to 10 times longer than solder attach, although actual performance depends on the materials, joint geometry, and operating conditions.

The recessed die placement also supports the flat surface required for subsequent lamination. After die attach, the process laminates copper foil over the embedded devices under controlled temperature and pressure. Laser drilling and copper plating create microvias that connect directly to the gate, source, and drain pads.

These plated connections replace conventional wire bonds.

Designers can then add additional routing layers sequentially, allowing them to place gate-drive and control circuitry above the embedded power stage.

The evaluated construction uses SPL-15, an electrically insulating dielectric with thermal conductivity of 10W/m·K, between copper layers. This is higher than the approximately 3W/m·K conductivity reported for some embedded leadframe insulation materials.

Higher dielectric thermal conductivity can support greater insulation thickness while limiting the corresponding increase in thermal resistance. Designers must still account for dielectric breakdown strength, operating voltage, material thickness, and applicable safety requirements.

Architecture Development and Stackup Considerations

Two earlier prototype constructions informed the evaluated architecture.

The first placed a semiconductor die on a 3mm copper slug embedded in thick FR-4. Differences in the coefficient of thermal expansion (CTE) among the copper, FR-4, and build-up materials produced stresses that cracked the microvias.

The second construction replaced the copper slug with a balanced stackup consisting of two thick copper layers on opposite sides of an SPL-15 dielectric core. The symmetrical structure distributed thermal and mechanical stresses more evenly, maintained panel flatness, and eliminated the microvia cracking observed in the earlier prototype.

These results illustrate the importance of mechanical balance when combining embedded semiconductor devices, thick copper, dielectric materials, and plated interconnections. Material selection and stackup symmetry should be evaluated together rather than independently.

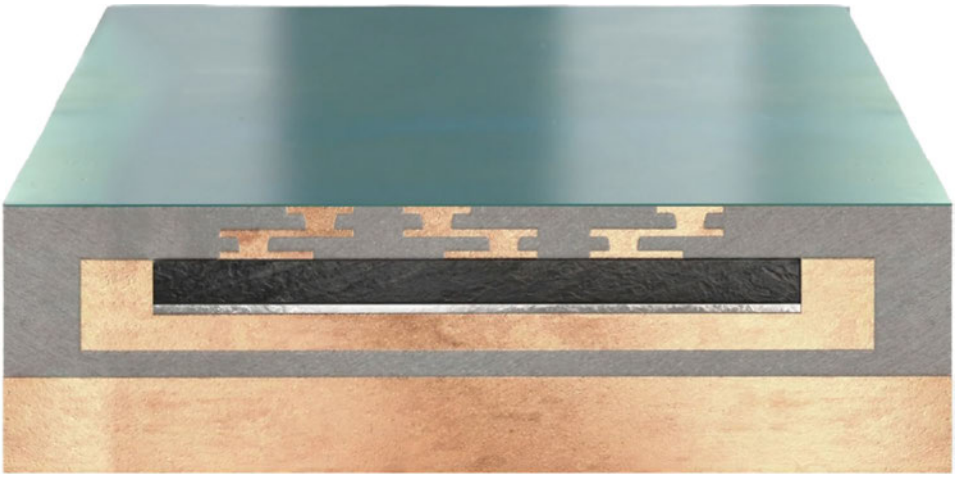


Figure 1. Comparison of the initial copper slug construction and revised balanced stackup, illustrating how symmetrical copper layers and a thermally conductive dielectric core reduce mechanical stress and prevent microvia cracking.

Half-Bridge Demonstrator

A half-bridge circuit served as the test vehicle for the EDS architecture. Half-bridge circuits are common building blocks for inverters and DC-DC converters.

The evaluation involved collaboration with a U.S. aerospace and defense manufacturer. The fabrication process placed bare GaN and SiC dies into precision-milled pockets and attached them using sintered silver. Plated copper microvias provided electrical connections to the embedded devices.

Two additional signal and drive layers were laminated above the power stage.

Figure 2 shows a cross section of the assembled test coupon. The demonstrator used standard FR-4 for the build-up layers because those layers carried only low-power control signals.

Applications requiring the build-up layers to carry additional heat or current may use higher-thermal-conductivity materials, including SPL-15 or SFL-series laminates, depending on the electrical and thermal requirements.

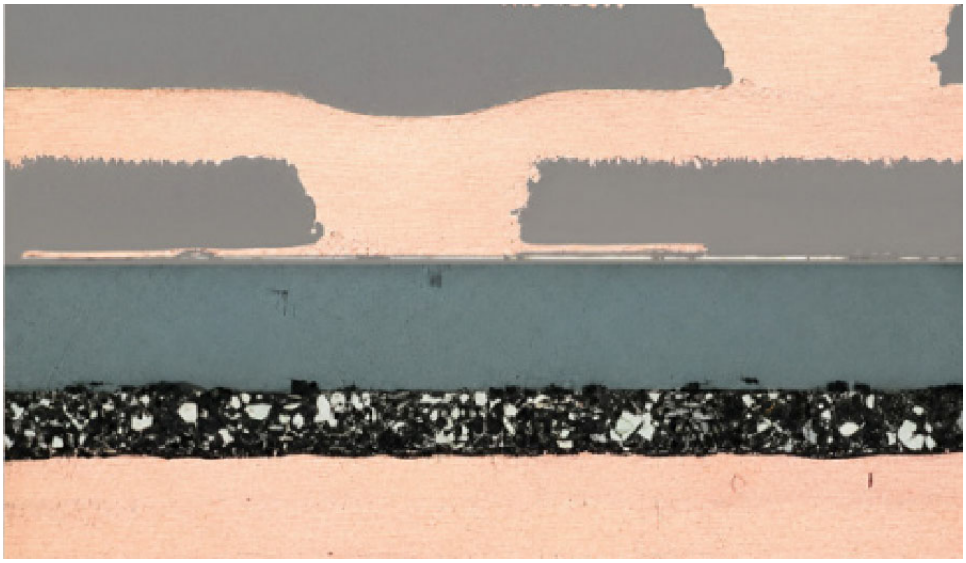


Figure 2. Cross-section of the embedded half-bridge coupon showing vertical microvia interconnections between the embedded dies and the upper circuit layers.

Electrical Performance

All evaluated samples passed functional testing at rated power. Voltage overshoot at the switching node remained below 2% of the supply voltage. The extracted power loop inductance ranged from 1 to 2nH.

The EDS demonstrator also achieved switching speeds approximately six times faster than an equivalent surface-mount design using the same semiconductor devices in standard packages.

Figure 3 illustrates the assembly configuration with two embedded dies.

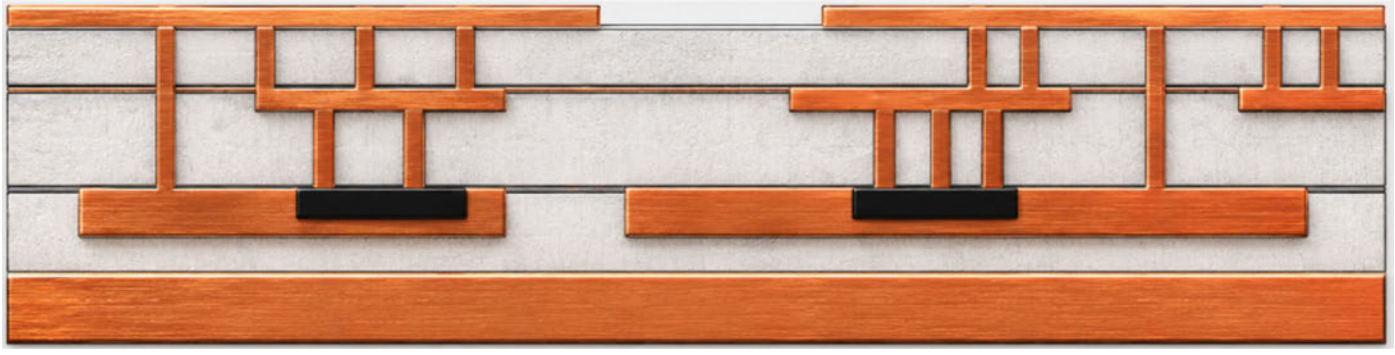


Figure 3. Embedded semiconductor in SPL15-HT.

For comparison, published measurements of conventional wire-bonded modules report loop inductances ranging from 6.7 to 15nH. Other embedded leadframe and laminate constructions have demonstrated values of approximately 1–1.5nH.

These results place the evaluated EDS architecture within the range reported for other low-inductance embedded packaging approaches. Its principal structural distinction is the use of a continuous thick copper heat spreader as the

die carrier rather than a prepackaged leadframe cell or laminate-supported die.

Thermal Path

Thermal performance depends on the number of interfaces along the heat flow path and the thermal resistance of each material.

Table 2 compares the junction-to-heat-sink thermal paths of several power electronics packaging architectures.

Table 2. Junction-to-Heat-Sink Thermal Path Comparison

Construction	Series Path: Junction to Heat Sink	Interfaces
TCLAD EDS	Sintered Ag (≥150W/m·K) → thick Cu spreader → 10W/m·K dielectric → heat sink	2
Leadframe cell embedding	Diffusion solder → 1.27mm Cu cell → ≥3W/m·K prepreg → Cu layer → cooler	3–4
Wire-bonded module	Die solder → DBC/AMB Cu → ceramic → Cu → baseplate solder → baseplate → TIM → heat sink	6+
SMT discrete on FR-4	Die attach → leadframe pad → solder → Cu → thermal via field → Cu → TIM → heat sink	6–7

Conventional wire-bonded power modules may include six or more material interfaces between the semiconductor junction and cooling surface. The evaluated EDS construction uses sintered silver die attach, a thick copper heat spreader, and a thermally conductive isolation dielectric to shorten the thermal path.

Sintered silver provides thermal conductivity of approximately 150W/m·K, compared with approximately 58W/m·K for SAC305 lead-free solder.

The SPL-15 isolation dielectric provides thermal conductivity of 10W/m·K, compared with approximately 3W/m·K for certain prepreg materials used in other embedded constructions.

For a heat transfer area of 1cm^2, a 100µm isolation layer contributes approximately 0.33K/W of thermal resistance at 3W/m·K. At 10W/m·K, the same thickness contributes approximately 0.10K/W.

These calculations illustrate the effect of dielectric thermal conductivity on the heat transfer path. The monolithic copper heat spreader, which can reach 1mm in thickness, also allows heat to spread laterally before reaching the isolation dielectric. Copper has a thermal conductivity of approximately 390W/m·K, making the spreader an important element of the thermal design.

In smaller embedded leadframe cells, the dimensions of the prepackaged cell limit the area available for lateral heat spreading. A continuous copper substrate can distribute heat across a larger area and allow multiple devices to share a common thermal path.

This distinction is particularly relevant when multiple power devices operate within the same substrate. Rather than relying on separate die carriers, the construction provides a shared copper heat-spreading plane.

The evaluated EDS architecture does not include a conventional baseplate-to-heat-sink TIM within the described substrate stack. However, the complete cooling assembly must still account for the thermal resistance of its final mechanical and thermal interfaces.

Reliability Considerations

Embedded die constructions combine semiconductor devices, copper layers, dielectric materials, and plated microvias into an integrated structure.

Temperature changes cause these materials to expand and contract. Differences in CTE can generate mechanical stresses at material interfaces and electrical interconnections.

The initial copper-slug prototype demonstrated this risk when thermal expansion differences contributed to microvia cracking. The revised construction uses SPL-15, which has a CTE of approximately 11.7ppm/°C below its glass transition temperature (Tg), providing a closer match to copper. The dielectric's Tg of approximately 270°C also supports dimensional stability during lamination and reflow processing.

A mechanically balanced stackup, with comparable copper thicknesses on opposite sides of the dielectric core, helps distribute thermal stresses and maintain panel flatness. Sintered silver die attach introduces additional reliability considerations and potential benefits.

The process forms the joint at approximately 250°C, while silver has a melting point of 961°C. Published power cycling comparisons indicate that sintered silver joints can withstand up to 10 times as many cycles as certain solder-attached constructions.

Replacing wire bonds with plated copper microvias also removes the bond-heel fatigue mechanism associated with conventional wire-bonded assemblies.

However, embedded microvias introduce their own reliability requirements, including accurate registration, adequate plating, and resistance to thermomechanical fatigue. The evaluated process identified a via-to-die registration window of approximately 50µm.

Maintaining this registration tolerance is important for consistent electrical connections and manufacturing yield.

Applications and Further Development

Embedded die substrate architectures may support applications that require high power density, efficient heat removal, and fast switching speeds.

Potential applications include high-density DC-DC converters, motor drives, onboard chargers, transformer-integrated power stages, and power electronics for aerospace and defense systems.

These applications place significant demands on electrical interconnections, thermal management, insulation, and mechanical reliability.

The use of established PCB fabrication processes may allow manufacturers to integrate portions of the power semiconductor packaging process into circuit board fabrication.

In the EDS approach, the PCB fabricator can perform several operations traditionally associated with semiconductor packaging, including die integration, electrical interconnection, and substrate-level thermal management.

This could expand the PCB fabricator's role from supplying interconnect structures to integrating portions of the wide-bandgap power stage itself.

However, implementation requires careful control of die placement, sintering, lamination, microvia formation, and material compatibility.

Further development should address via-to-die registration, dielectric material selection, thermal cycling reliability, and the transition from test coupons to full application-level power stages.

Additional comparative testing would also help establish performance differences among thick copper embedded die substrates, laminate-based embedded packages, and conventional power modules under equivalent operating conditions.

Key Takeaways

- The EDS architecture places bare GaN and SiC semiconductor devices inside precision-milled pockets in a thick copper heat spreader, creating a shortened thermal path through the substrate.
- Sintered silver die attach and a 10W/m·K isolation dielectric can reduce thermal resistance compared with certain conventional packaging materials.
- Half-bridge demonstrators achieved power loop inductance of 1–2nH, voltage overshoot below 2%, and switching speeds approximately six times faster than the evaluated surface-mount reference design.
- Balanced stackup construction and CTE compatibility play important roles in maintaining microvia reliability.
- Established PCB fabrication processes can support embedded semiconductor integration, potentially expanding the PCB fabricator's role in wide-bandgap power electronics manufacturing.



Figure 4. Illustration of a conventional wire-bonded power module showing wire interconnections between semiconductor devices and copper conductors.

Conclusion

Embedded die substrate architectures offer an alternative approach to managing the electrical and thermal limitations of wide-bandgap power electronics. By integrating bare semiconductor dies into thick copper substrates and replacing wire bonds with plated microvias, these constructions can reduce power loop inductance and shorten the thermal path between the semiconductor junction and cooling structure.

Tests of GaN and SiC half-bridge demonstrators reported power loop inductance of 1–2nH, voltage overshoot below 2%, and switching speeds approximately six times faster than the evaluated surface-mount reference design.

The results demonstrate the potential of thick copper embedded die constructions while highlighting the importance of stackup balance, dielectric selection, microvia registration, and thermal interface design. The architecture also illustrates how PCB fabrication processes could support greater integration of semiconductor devices, electrical interconnections, and thermal management within a single substrate.

As switching speeds and power densities increase, PCB fabricators may play a larger role in integrating wide-bandgap power stages, provided that the processes meet the electrical, thermal, and reliability requirements of the intended applications.

CHRIS PARKER is product engineering manager at TCLAD (tclad.com); chris.parker@tclad.com.

Printed Circuit University



Stay on the forefront of technology

with the most **comprehensive database**

of online **courses and webinars**

for the **printed circuit engineering** community.

Check it out
TODAY

printedcircuituniversity.com

PCU

MANUFACTURING **INTELLIGENCE**

Manufacturing's Next AI Wave: Notes from the Frontier

> See how the emerging AI manufacturing landscape could transform electronics manufacturing operations through intelligent automation, data integration, and decision-making tools.

by SHIRIN KHANNA

I've spent the last few months talking with founders building AI for manufacturing, from pre-seed teams to growth-stage companies. As an operator at a contract electronics manufacturer, I wanted to understand where AI moves the needle on the shop floor and on the P&L. I came away with a clear view: This is one of the most underrated spaces in AI right now, and the next wave will look very different from the current one.

Most conversations about AI in manufacturing today focus on robots. Robotics startups pulled in over $10 billion in venture capital in 2025. Mind Robotics, a Rivian spinout, crossed $1 billion in cumulative funding inside a year.

Robots are easy to film and easy to fund. That's why they get the headlines.

For most operators, though, robots represent only part of the manufacturing AI landscape. The other part lives in supplier inboxes, RFQ spreadsheets, bills of materials (BoMs) with 300 line items, ERP screens, CAD files, and shop-floor dashboards. That's the part I want to talk about.

A Quick Map of the AI Manufacturing Space

The non-robotics AI manufacturing landscape falls into a handful of problem areas.

Manufacturing intelligence and shop-floor visibility. This is the most mature subcategory. Augury ($369M, Series F) leads in predictive maintenance. First Resonance ($19M, Series A) offers a manufacturing operating system for high-mix, low-volume electronics production. Guidewheel ($30M), Tulip ($152M), and Sight Machine ($87M) cover overall equipment effectiveness (OEE), shop-floor applications, and industrial analytics. Zelos Cloud represents the seed-stage entrants.

Visual inspection and quality. Instrumental ($80M, Series C) is the most established player in PCB and electronics quality inspection. Andrew Ng's Landing AI ($57M, Series B) brings a data-centric approach to small datasets. At the seed stage, Bucket Robotics uses CAD-trained models to deploy visual inspection without manual labeling.

RFQ and quoting. Paperless Parts ($51M, Series B) has tackled this problem for years. The seed-stage wave (Korso, Soff, Arzana) is automating the full quote-to-order workflow.

Procurement and supply chain. This area has the largest cluster of seed-stage activity. Mandel, Lumari, Comena, Vendra, and Cavela are each building AI agents that work with supplier emails. At Series A, Didero ($37M, NYC) is bringing the same approach to enterprise scale.

Design, compliance, security, and ESG. These areas have less activity but still matter. Diode Computers and Prototyping.io focus on design automation. Noetic and Saphira address hardware compliance. Binarly specializes in firmware security, while Coolset focuses on ESG reporting.

One area stood out as underserved: high-mix, low-volume production scheduling. Most manufacturing execution system (MES) tools target high-volume, repetitive production runs. For an electronics manufacturing services (EMS) provider juggling more than 50 different jobs a week across SMT, wave soldering, and automated optical inspection (AOI) lines, spreadsheets still handle much of the scheduling. No seed-stage AI startup currently focuses specifically on this challenge.

Plot these companies by stage and funding, and the shape of the category jumps out: a dense seed-stage cluster on the left and a handful of growth-stage players up and to the right. The companies entering the market today are defining the category.

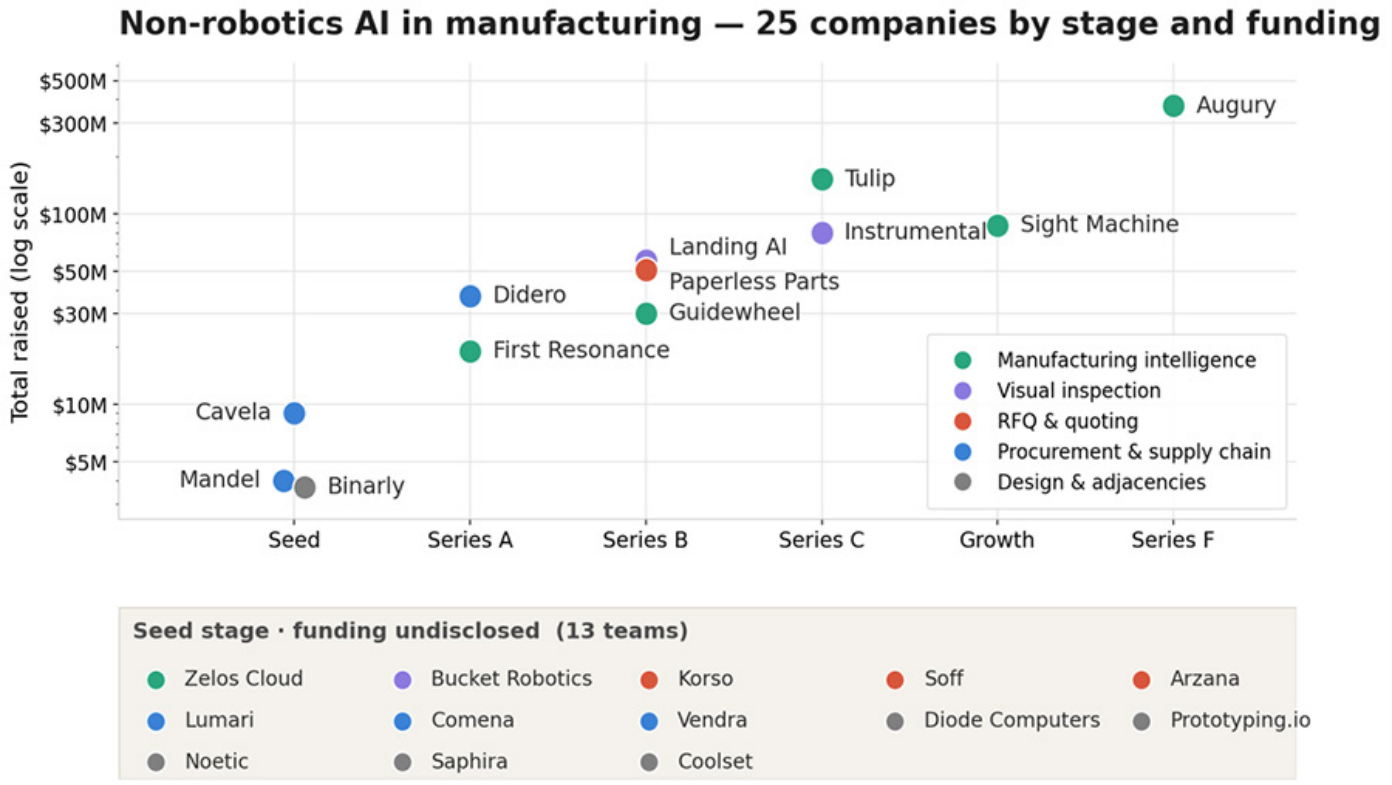


Figure 1. The AI manufacturing startup landscape spans multiple funding stages, with a concentration of seed-stage companies and a smaller group of established, well-funded players.

What I Heard Across the "AI for Manufacturing" Conversations

Three patterns repeated in nearly every meeting. These observations don't reflect any specific team. They reflect the category's current state.

Companies are building AI around unstructured manufacturing data. Suppliers won't adopt portals, engineers won't redo their CAD workflows, and shop-floor operators won't use a new screen. So the dominant architectural approach involves reading data where it already lives. Inboxes and PDFs for procurement. CAD files and camera feeds for inspection. Machine-level signals for the shop floor. The same pattern appears across the category: Read what's already there.

The workflows have converged. What separates teams now is configurability. Within each subcategory, companies now follow a standard core workflow.

- Procurement: ingest → distribute → extract → compare → push to ERP.
- Inspection: CAD → train → deploy → flag.
- Shop floor: sense → capture → surface → recommend.

What separates teams is how easily a manufacturer can encode its own playbook: follow-up cadences, escalation rules, approval hierarchies, and exception thresholds. Every shop runs its own playbook, and the better products let manufacturers keep theirs.

The customer counts are small, which is part of the opportunity. The teams I met range from zero customers to about a dozen. Even the well-funded companies continue to run pilots. I don't see that as a knock. It's the most exciting part of the category. The founders shipping products today are writing the playbook for everyone who comes next.

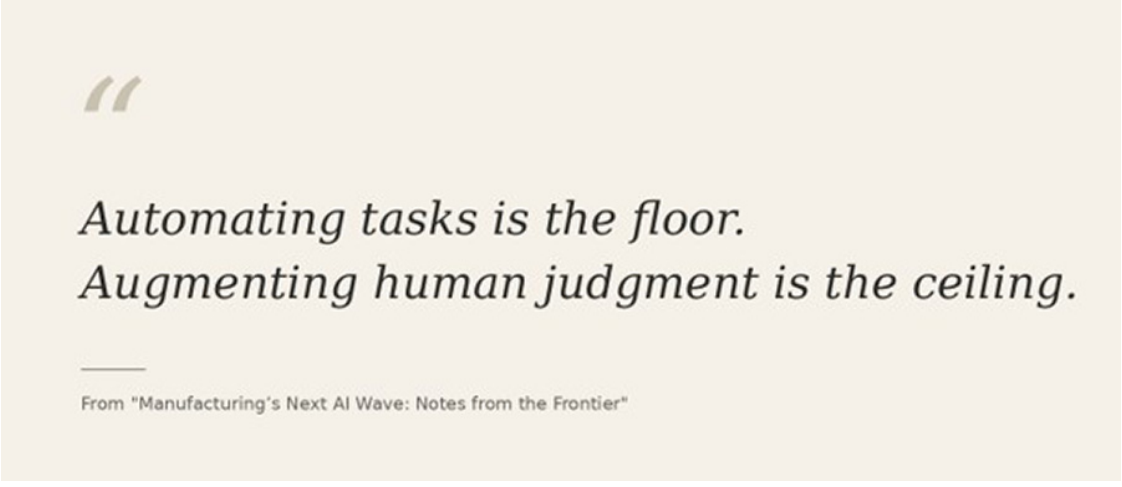


Figure 2. AI manufacturing startups target key operational challenges, including shop-floor visibility, quality inspection, procurement, quoting and design automation, highlighting opportunities for further innovation.

Today's products make existing manual workloads faster and cheaper. For a manufacturer where manual cognitive work accounts for a meaningful share of operating expenses (OpEx), that translates into real money on the P&L. But executing yesterday's workflow faster doesn't necessarily create a fundamentally better business.

The bigger prize lies in expanding what an operator can decide. AI can surface patterns and possibilities operators couldn't see before, letting them manage categories and programs they couldn't handle before. That's not "AI that does my job 10x faster." It's "AI that lets me do a job nobody could do at all."

The teams that define this category long-term won't necessarily have the cleverest agent architectures. They'll be the ones that combine customers' internal data (historical pricing, supplier scorecards, machine logs, quality history, and BoMs) with meaningful external signals: public benchmarks, government data, geopolitical inputs, commodity trends, and historical supply chain disruption data.

That combination helps operators make decisions they could not have reached alone.

Anyone can wrap a large language model (LLM) around a workflow. Very few can build the data graph that makes the model's output useful enough to act on.

The pitches that impressed me most framed the product around a P&L line, not an architecture diagram. "We save $X per shift at a $100M EMS provider" is a different kind of sentence than "we use a 12-step pipeline with custom embeddings." This matters beyond pitching. It shapes the product.

Tech-first products optimize for elegance. Business-first products optimize for the customer's outcome. Over time, the second kind tends to win.

The use case I keep coming back to is an agent that works silently and only interrupts when it has something worth saying. In quality, that's an agent watching every production line and flagging only the process deviations that deserve attention.

In scheduling, it quietly sequences jobs around a delayed shipment. In sourcing, it continuously scans new suppliers and only alerts you when one offers an advantage over your current vendor.

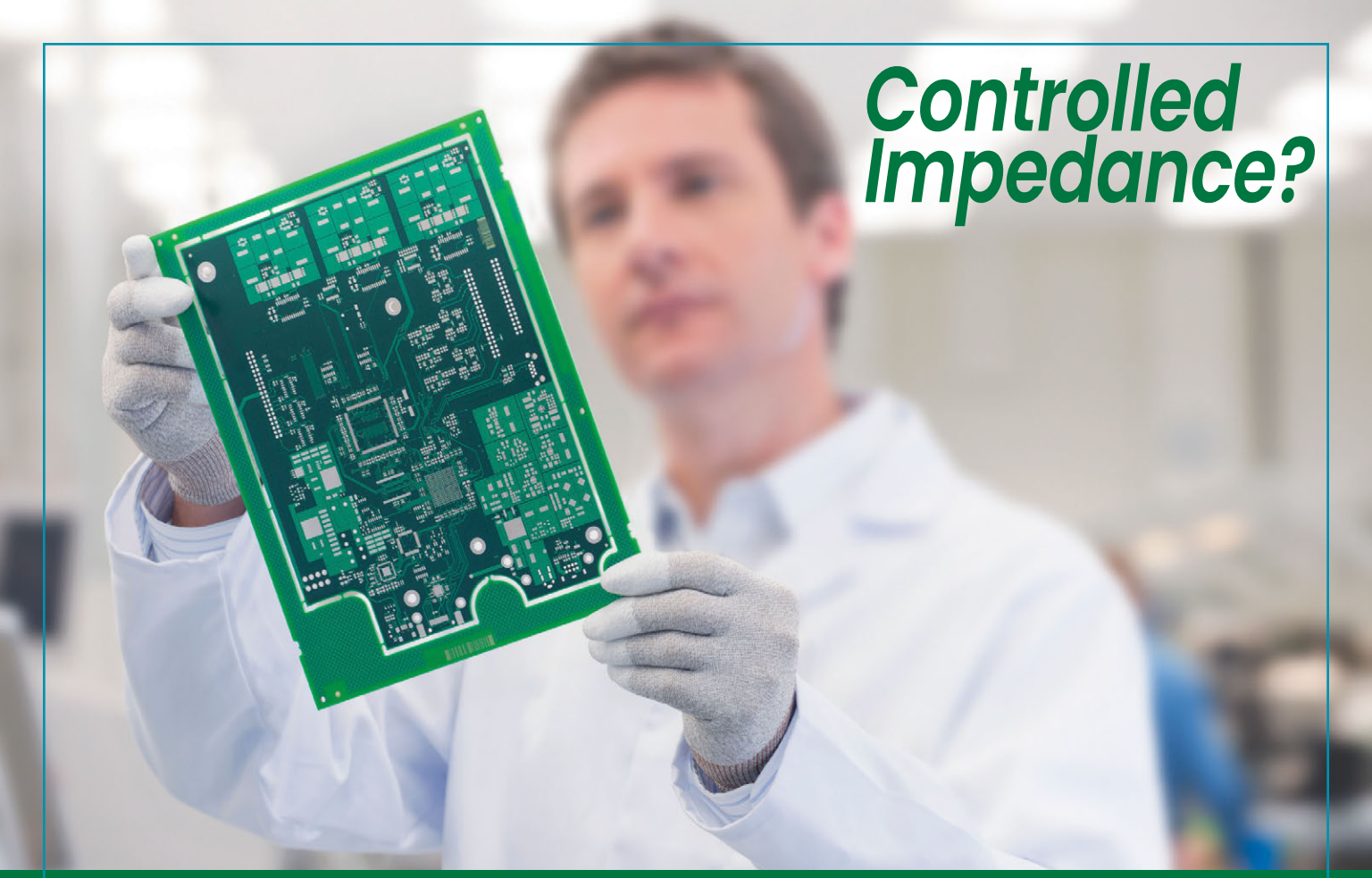
It's the opposite of adding a chatbot on top of a workflow. The better model treats AI as a colleague who walks into your office only when something matters.

Companies are building this category right now. The current wave is laying the foundation: moving manual workloads off the page, building the underlying data infrastructure, and codifying the playbooks manufacturers currently manage by hand.

The next wave excites me most. It will bring products that combine internal and external data to help operators make decisions they couldn't have reached alone. The underlying AI agents will stay quiet until they have something worth saying. And the entire system will focus on business outcomes, not the architecture.

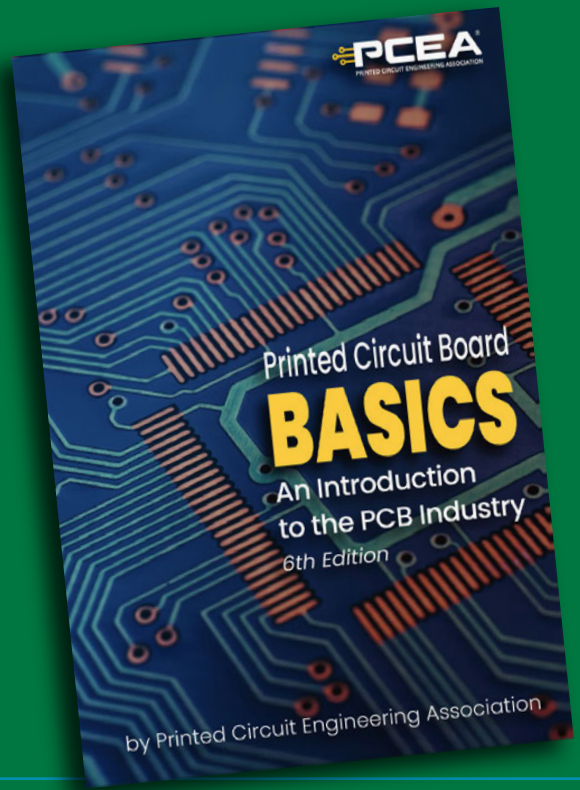
If you're a founder building in this space or an operator at a manufacturing business thinking about where AI moves your P&L, I'd love to compare notes.

SHIRIN KHANNA is a board member at Indic Electronics, a contract electronics manufacturer, where she leads supply chain and procurement. She oversees the end-to-end RFQ process, drives digital transformation on the factory floor through SAP HANA, CalcuQuote and digital manufacturing platforms, and leads go-to-market initiatives that have secured multiple enterprise customers and introduced new revenue streams, including design for manufacturing (DfM) services. She focuses on making industrial operations faster, more transparent and more accountable, from sourcing decisions to shop-floor execution.



Controlled Impedance?

Speak "PCB" with confidence. No degree required.



The handbook for anyone new to PCBs. In plain words.

Download Your FREE Copy Today!

PCEA®
PRINTED CIRCUIT ENGINEERING ASSOCIATION

ELECTRONIC **EVOLUTION**

The Electron: A Biography, Part 2: From the Vacuum Tube to the Data Center

From early radio and television assembly to surface mount technology and AI data centers, the evolution of electronics manufacturing reveals how innovation, miniaturization and automation have transformed the industry.

by **RONALD C. LASKY, Ph.D.**

Last time (with a lot of help from my student researcher Rishaan Nalwar), I left off with a bit of an irony: engineers had been soldering telegraph wires, running telephone lines and lighting up entire cities with electrons for the better part of eighty years before physicists like J. J. Thomson and Robert Millikan actually proved what an electron was. Science had finally caught up with engineering. Now it was time to put this newly confirmed little particle to work in a whole new way.

As electric lights and appliances became more common, radio was emerging. Initially, hobbyists used lead sulfide (galena) crystals to catch weak radio signals drifting through the air. The crystal needed no amplification, but the signal was so faint that you needed headphones pressed right to your ear to hear anything at all. Lee de Forest's triode vacuum tube, shown in **Figure 1**, changed everything: those whisper-quiet signals could now be amplified enough to drive a speaker, and the whole family could gather around and listen together. Surprisingly, radio did not take off overnight. It took nearly a decade for anyone to realize that advertising, not subscriptions, would pay for it all.



Figure 1. Lee de Forest's triode vacuum tube enabled the amplification of weak radio signals, making broadcast radio possible.

Radio

By the 1930s, the radio had become an indispensable part of American life. During the Great Depression, radios served as a primary source of news, entertainment, and connection for many families. Despite financial struggles, the affordability and value of radio made it a staple in American households: by 1930, over 40% of American households owned a radio, and by the end of the decade, that number had more than doubled to 83%.

The radio's role extended well beyond entertainment. It was a tool for unity and reassurance. President Franklin D. Roosevelt's Fireside Chats gave comfort and a direct line of communication to citizens during the hardest years of the Depression and, later, World War II.

Manufacturing all of these radios gave birth to the electronic assembly industry as we know it. A radio like the 1924 Atwater Kent set shown in **Figure 2** would have been assembled entirely by hand, wire by wire, with solder and flux. **Figure 3** shows a modern reproduction of that kind of early radio circuit board up close, and **Figure 4** shows the same kind of bar solder and flux that would have been used to build it, not so different from what is used today. Radio assembly began in earnest in the late 1920s, and under the demands of World War II it had become a genuinely disciplined, methodical process, formalized by new military specifications (MIL-SPECs) that gave the whole industry a rigor it had not had before.



Figure 2. A 1924 Atwater Kent radio. A radio like this would have been assembled by hand, with solder and flux similar to what we use today. (Image courtesy of Wikimedia Commons)

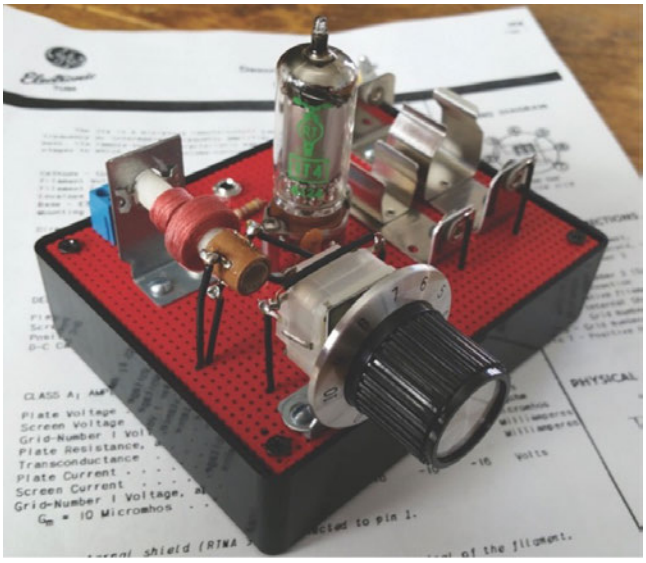


Figure 3. A modern reproduction of an early radio circuit board. A board like this would have been assembled by hand, with solder wire and flux.



Figure 4. Bar solder and flux, little different from what was used to assemble the telegraph, the radio, and the television.

Television

Through the 1950s, radio gave way to television, and electronics assembly grew right along with it. The widespread adoption of the printed wiring board in the 1940s and 50s finally did away with the rat's nest of point-to-point wiring inside a radio or TV chassis. Hand soldering hung around for a while, but by the 1950s, wave soldering had taken over, using the same bar solder and fluxes, we use today, shown in Figure 4. Wave soldering would go on to become the backbone of electronics assembly for the computer industry that followed.

The shift from radio to television did more than change how boards were built, though; it reshaped American culture. Radio had been an imaginative, auditory medium: families gathered around and listened, picturing the events and characters for themselves. Television added moving pictures, and suddenly national events, entertainment, and advertising all became far more vivid and immediate. It nudged American culture toward a shared visual experience, standardizing tastes and values across the country the way only a nightly sitcom or the 1960 Kennedy-Nixon debate could. Advertising became more powerful too, tying products to images of modernity and success, even as television quietly pulled people away from local theaters, radio dramas, and other community-based entertainment, and further into home-centered, suburban life.

Television Transforms Electronics Manufacturing

Television did something else, too: it forced electronics manufacturing to grow up. Radios were relatively simple and could be hand-wired point-to-point by a skilled technician without too much trouble. Televisions were a different animal entirely, with dozens of vacuum tubes, transformers, coils, and capacitors, all packed together at high voltages and radio frequencies. Point-to-point wiring became slow, error-prone, and impossible to scale, so manufacturers turned to printed circuit boards, which offered repeatable layouts, faster assembly, and much easier troubleshooting.

TV design also encouraged a modular approach: a set might be broken into an RF tuner, an IF strip, an audio amplifier, and separate deflection circuits, each built on its own board or sub-chassis. This modularity made assembly and repair simpler and let multiple teams build and test different sections in parallel. Labor itself became specialized. Rather than one technician building an entire set, individual workers handled narrowly defined tasks: inserting components, soldering, or inspecting. It was a real assembly line, and it made electronics manufacturing accessible to a much broader workforce than the radio days had required.

Because televisions ran at higher voltages and frequencies than radios, marginal solder joints could cause failures you could literally see and hear: a flickering picture or a crackling speaker. So manufacturers had to get serious about soldering consistency, flux quality, temperature control, and inspection, which were really the first stirrings of the process control and quality assurance we take for granted in electronics manufacturing today. Jigs, fixtures, and in-line testing became standard, holding boards in place during assembly and checking voltages and signal response at every stage, rather than waiting until the very end to catch a problem.

Television production was still mostly hand-assembled, but its scale and complexity paved the way for what came next. When transistors, and later integrated circuits, replaced the vacuum tube, the modular, PCB-based habits the

television industry had already built made it easy to bring in automated component insertion and wave soldering. In a real sense, television manufacturing was the bridge between handcrafted electronics and the automated board assembly we know today, and it directly enabled the mass production of early computers, military electronics, and eventually the PC and the smartphone.

Miniaturization: Not Just the Smartphone's Story

It is easy to assume the smartphone is responsible for the relentless miniaturization of electronics. It certainly demands more functionality crammed into less space than anything before it. But that is not quite where the story starts.

Miniaturization actually began in the military, aerospace, and medical worlds of the 1950s and 60s, where weight, reliability, and power consumption were life-or-death concerns. Missiles, spacecraft, hearing aids, and portable radios all pushed the development of transistors and integrated circuits, and proved what was technically possible. But these were low-volume, specialized products. They did not yet create the sustained, high-volume commercial pressure needed to make dense electronics a mainstream expectation.

That pressure showed up more clearly in the consumer camera industry of the 1970s, 80s, and 90s as shown in **Figure 5**. Compact 35mm cameras were already packed tight with optics, shutters, film transport, and batteries, yet buyers increasingly expected autofocus, automatic exposure, motorized film advance, and electronic flash, all squeezed into the same small body. Meeting those expectations required dense, low-power electronics tightly integrated with mechanical and optical parts, and camera makers, especially in Japan, became some of the earliest and most aggressive adopters of custom chips, flexible circuits, hybrid assemblies, and miniature motors and sensors. Cameras were genuinely mass-market, global products, and in that environment, miniaturization stopped being a curiosity and became a competitive necessity.



Figure 5. Manufacturing of personal cameras led the way in electronics miniaturization. This film camera was manufactured in 1995.

The shift to digital cameras in the 1990s only raised the stakes: image sensors, high-speed signal processing, memory, and displays all had to fit into a handheld device running on a small battery. A lot of the design tricks that later defined the smartphone, like system-on-chip integration, aggressive power management, and dense packaging, were worked out first inside a camera body.

So rather than being the origin of electronic miniaturization, the smartphone is really its culmination. It inherited a design culture built over decades, first by the military and medical worlds, and then, just as importantly, by the humble camera.

Why Surface Mount Technology Took Over

Surface mount technology, or SMT, did not take over circuit board assembly because of one clever invention. It won because through-hole assembly simply could not keep up with everything the industry was demanding of it at once: more components, better electrical performance, and efficient mass production.

Miniaturization was one big driver. Early radios and TVs, built with point-to-point wiring or through-hole parts, worked fine when circuits were simple, but as integrated circuits packed in more capability, through-hole components, which need drilled holes and generous lead spacing, started eating up board space and limiting components to one side of the board. Surface mount parts could sit directly on the board's surface, at much higher density, and on both sides at once, which mattered enormously for calculators, personal computers, and eventually anything meant to fit in a pocket.

Electrical performance mattered too. As clock speeds climbed, the long leads on through-hole parts introduced parasitic inductance and capacitance that muddied signals and increased interference. Surface mount components, with their short or leadless connections, largely solved that problem and became a natural fit for the performance demands of modern chips.

Then there was plain economics. Through-hole assembly depended on manual labor for component insertion and soldering, which was hard to scale and hard to keep consistent. Rising labor costs and rising volumes pushed manufacturers toward automation, and SMT enabled fully automated lines: pick-and-place machines, solder paste printing, and reflow soldering, all faster, more repeatable, and far more amenable to real process control than anything that came before.

None of this would have worked without supporting technology catching up too. PCB fabrication improved to support finer traces and more reliable vias. Solder pastes and flux chemistries matured for precise deposition and consistent wetting during reflow. Vision-guided placement equipment and automated inspection cut defects further. And as IC pin counts climbed, packages like SOICs, QFPs, and eventually ball grid arrays let manufacturers pack in hundreds or thousands of connections in a compact footprint, something through-hole packaging simply could not do.

Finally, once high-volume consumer electronics created the economic case for automated SMT lines, and military and aerospace applications validated it for weight and reliability, the outcome was not really in doubt. Through-hole

technology still has its place for certain mechanical or high-power jobs, but SMT became, and remains, the foundation of modern electronics manufacturing.

Today, and Some Thoughts on Tomorrow

It is worth stepping back and appreciating just how far we have come. For most of human history, right up through Andrew Jackson's time, communication and travel changed hardly at all. If you had lived in Boston and been invited to Jackson's 1829 inauguration, the invitation would have taken two weeks to reach you, and a good, fast stagecoach trip to Washington would have taken about another week. Twenty-five years later, thanks to the telegraph and the railroad, a message could arrive almost instantly, with the traveler following a day behind.

Our own era's version of that leap is arguably even more dramatic. The first electronic computer, ENIAC, shown in **Figure 6**, managed about 500 floating-point operations per second, cost the equivalent of about $8 million in today's dollars, ate as much electricity as 100 homes, and broke down every day or two whenever one of its 18,000 vacuum tubes gave out. Today's smartphone has more than a billion times ENIAC's computing power and a billion times its memory, all for under $1,000.

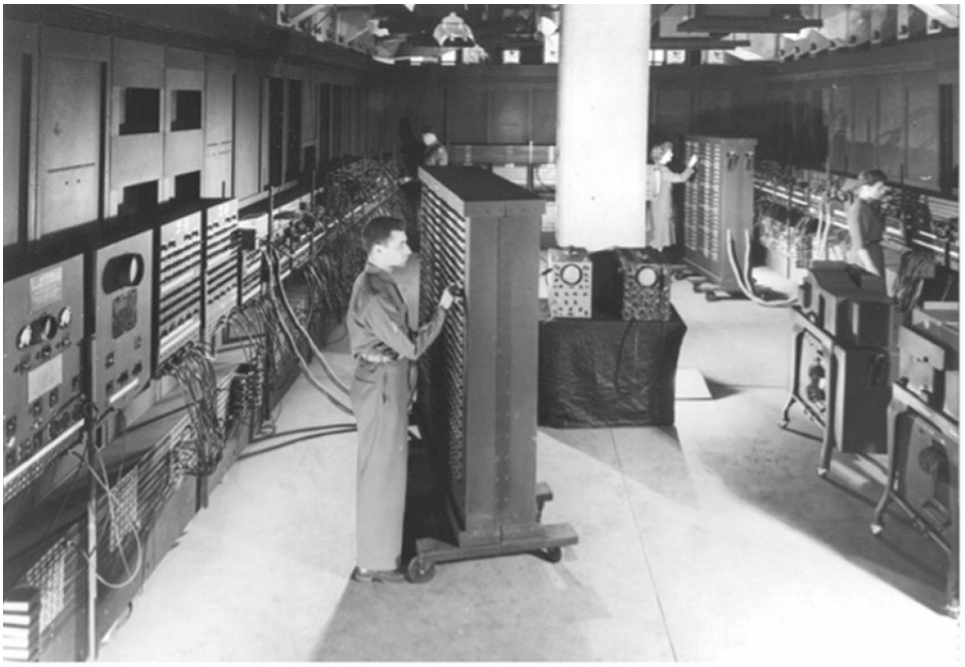


Figure 6. ENIAC cost about $8 million in 2026 dollars, used as much electricity as 100 homes, and broke down about every day or two, whenever one of its 18,000 vacuum tubes failed.

And we are not slowing down. A single rack of Nvidia's newest DGX GB200 supercomputer draws 120 kilowatts, enough to power around 100 homes, and delivers 1.44 exaflops of performance, more than 100,000 times what is in your smartphone, for about $15 an hour to run. Data centers built to house racks like these are now being planned at the 10-gigawatt scale; at ten cents a kilowatt-hour, that is on the order of a million dollars an hour, just to keep the lights, or rather the electrons, flowing.

It is a fun bit of trivia that, over an average American lifetime, roughly ten to the twenty-fifth power electrons pass through a given cross-section of wire to support that lifestyle. That is about how many electrons each of us "uses" in a lifetime, a genuinely staggering number for a genuinely tiny particle.

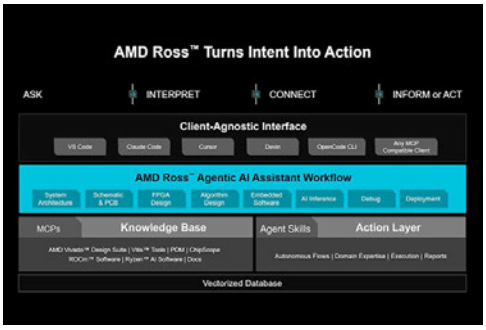
Conclusion

The electron may be the single most important thing nature has given us. It provides every chemical bond that holds matter together, from the simplest virus to the largest star, and, as this pair of posts has hopefully shown, humanity has spent the last two centuries putting it to increasingly remarkable use: the telegraph, the telephone, the light bulb, the radio, the television, the computer, and now the AI data center.

We are standing at the edge of some genuinely new territory: artificial intelligence, quantum computing, autonomous vehicles, and technologies we probably have not even named yet. AI is beyond impressive on a screen, but it has not yet shown it can do much in the physical world; autonomous vehicles still seem years away from really arriving; and quantum computing, at least for now, still feels like a solution in search of a problem. Time will tell how all of this shakes out. But if the last 200 years are any guide, electricity, and the humble electron carrying it, will remain the indispensable infrastructure underneath whatever comes next.

RONALD C. LASKY, PH.D., P.E., is a senior technologist at Indium Corporation and a professor of engineering at Dartmouth College.

PCD&F



AMD ROSS AGENTIC AI ASSISTANT

Ross agentic AI assistant supports embedded system development from architecture through deployment, including PCB design, schematic review, hardware optimization, debugging, embedded software and edge AI implementation. Integrates with AMD Embedded development tools for FPGAs, adaptive SoCs and x86 processors. Features natural-language interaction, reusable engineering workflows, expert-developed agent skills and an AMD Knowledge Base. Uses Model Context Protocol (MCP) servers and AMD-validated vector databases to execute commands, analyze timing, optimize high-level synthesis and support hardware-software partitioning. Supports multiple large language models, integrated development environments and command-line tools. For embedded system design, PCB layout review and edge AI development.

AMD

amd.com



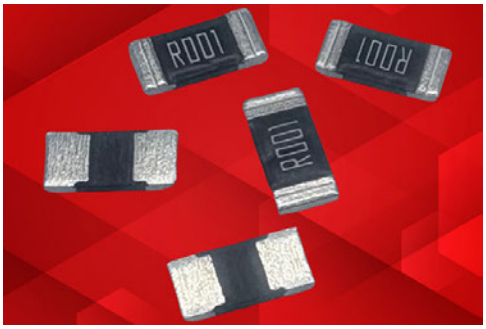
HIROSE FX36 SERIES FLOATING BOARD-TO-BOARD CONNECTOR

FX36 Series floating board-to-board connector features a 0.5mm pitch for high-density PCB layouts. Part of the FunctionMAX family, withstands temperatures up to 125°C and accommodates misalignment of ±0.7mm in the X and

Y directions and ±0.5mm in the Z direction. Floating structure absorbs up to 0.05mm of vibration amplitude in the Z direction, while a two-point contact design supports electrical connections under vibration. Supports compact board layouts and automated assembly. For battery electric vehicle (BEV) and hybrid electric vehicle (HEV) powertrain systems, including multifunctional X-in-1 units.

Hirose Electric

hirose.com

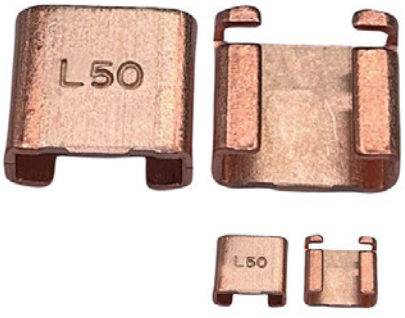


STACKPOLE CSSU CURRENT-SENSE RESISTORS

CSSU series metal-alloy current-sense resistors add 25mΩ and 30mΩ resistance values for low-current sensing applications. Higher resistance values generate stronger sensing voltages to improve measurement resolution and reduce the effects of noise and offset errors. Feature low temperature coefficient of resistance (TCR), long-term stability and power ratings up to 5W in a 2512 package. Meet AEC-Q200 requirements. For battery management systems, automotive electronics, motor controls, DC-DC converters and industrial power supplies.

Stackpole Electronics

seielect.com



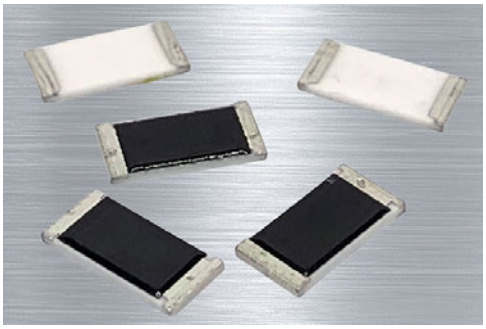
STACKPOLE HCSK1216 SHUNT RESISTOR

HCSK1216 Kelvin-termination metal-alloy shunt resistor delivers up to 10W at 70°C in a 1216 footprint, using 75% less PCB area than a conventional 2725 component. Four-terminal Kelvin design separates current and voltage-sense paths to reduce lead-resistance measurement errors. Elevated resistive element reduces PCB thermal stress, while all-metal construction provides low inductance and high pulse capability. Operates from -55°C to 170°C and comes in 0.3, 0.5, 1 and 2mΩ resistance values, with tolerances as low as 1% and TCR as low as 50ppm/°C. Meets AEC-Q200,

RoHS and REACH requirements. For AI server power systems and high-current sensing applications.

Stackpole Electronics

seielect.com



STACKPOLE RMAN ALUMINUM NITRIDE CHIP RESISTORS

RMAN series thick-film chip resistors use aluminum nitride (AlN) substrates for improved thermal conductivity and heat dissipation. Deliver power ratings up to 2.4W in a 1206 package and 3.4W in a 2512 package. Maintain electrical insulation while reducing localized heating under sustained loads. Support gate-drive and snubber circuits for IGBT, SiC and GaN power modules, along with precharge, discharge, bleeder and current-sensing functions. For industrial motor drives, inverters, power supplies, electric vehicle battery management systems, onboard chargers and DC-DC converters.

Stackpole Electronics

seielect.com

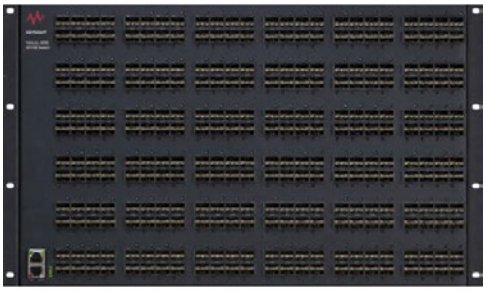
CA

GREATWALL GW-TO70WV12 OPEN FRAME POWER SUPPLY

GW-TO70WV12 open frame power supply delivers 70W of output power and a regulated 12VDC output. Supports input voltages of 90–290VAC or 192–288VDC for operation across varying power environments. Open frame construction permits integration into compact equipment enclosures while accommodating system-level airflow and thermal management. Designed for continuous-duty operation and carries CCC, CB and CE safety certifications. For embedded systems, industrial controls, communications equipment, monitoring devices and other OEM electronics requiring internal 12V power delivery.

Greatwall

powernexu.com



KEYSIGHT VELOCITY 4900 SERIES AUTOMATION SWITCHES

Velocity 4900 Series Layer 1 automation switches provide software-controlled physical connectivity and automated testbed configuration. Velocity 4902 supports Ethernet speeds from 100Mbps to 100Gbps and features 72 QSFP28 ports for up to 288 connections with breakouts. Velocity 4906 provides 288 SFP28 ports supporting 100Mbps to 25Gbps. Both models feature low-latency Layer 1 switching and support single-mode and multimode fiber, direct-attach copper and active optical cables. Include per-port speed and media configuration, port tapping and one-to-many traffic replication. Integrate with Keysight Velocity software for resource reservation, lab orchestration and automated testing. For AI, 6G and next-generation network validation.

Keysight Technologies

keysight.com



MICROCARE FRC2 GENERAL PURPOSE FLUX REMOVER

FRC2 general purpose flux remover is an HFC-free cleaning formulation for removing no-clean and rosin flux residues from electronic assemblies. Nonflammable, non-corrosive solution evaporates quickly without leaving residue or requiring rinsing. It is ESD-safe and compatible with most plastics, including epoxies, nylon, polyethylene, and polypropylene. Available in aerosol and bulk liquid formats, with the aerosol compatible with the TriggerGrip cleaning tool. For SMT, through-hole and BGA assemblies, cables, connectors, benchtop cleaning, rework, repair and production applications.

MicroCare

microcare.com



SAKI 3DI-LS3BX INLINE 3-D BOTTOM-SIDE AOI

3Di-LS3BX inline 3-D bottom-side automated optical inspection (AOI) system inspects through-hole solder joints and PCB surfaces following selective, wave and dip soldering without flipping boards. Combines 3-D measurement, proprietary inspection algorithms, a high-rigidity gantry and dome lighting for inspection of component pins and solder fillets. Full Memory Technology detects solder balls as small as 200µm and foreign object debris across PCB surfaces. Uses the same software platform as Saki's solder paste inspection and post-reflow AOI systems. Optional return conveyor supports integration into existing production lines. For automated through-hole solder inspection and PCB assembly quality control.

Saki Corporation

sakicorp.com



TDK SENSEI EDGERX STARTER PREDICTIVE MAINTENANCE SOLUTION

edgeRX Starter predictive maintenance solution combines AI-driven multimodal sensing with analytics to monitor industrial equipment performance and identify developing faults. Continuously collects vibration and temperature data to detect changes in machine behavior and identify anomalies. Provides early warnings and maintenance recommendations to help reduce unplanned downtime and extend equipment life. Designed for deployment by industrial teams without extensive in-house predictive maintenance expertise. For industrial equipment monitoring, condition-based maintenance and production operations.

TDK SensEI

sensei.tdk.com



VISCOM IX7059 SMT EDITION 3-D INLINE AXI

iX7059 SMT Edition inline 3-D automated X-ray inspection (AXI) system combines high-resolution imaging, 3-D volume visualization and AI-powered analysis software for inspection of electronic assemblies. Designed for high-throughput SMT manufacturing with demanding quality requirements and short cycle times. Inspects BGAs, hidden solder joints and other difficult-to-access assembly features. Incorporates automated image analysis for defect detection and inspection efficiency while maintaining production throughput. For complex PCB assemblies, SMT production lines and automated solder joint inspection.

Viscom
viscom.com

In Case You Missed It

Additive Manufacturing

"Ultrafast Laser Direct Writing of Highly Conductive Copper Micropatterns"

Authors: S.Y. Xue, *et al.*

Abstract: Copper (Cu) interconnects are fundamental to advanced optoelectronic systems. Femtosecond laser direct writing (FsLDW) employing particle-free Cu ion inks provides a compelling "cold processing" approach; however, it frequently results in porous, high-resistivity structures caused by disordered grain growth and solvent-induced micro-explosions. Here, the authors report a high-precision FsLDW strategy utilizing a specifically formulated metal-organic complex ink. By decreasing the reduction energy barrier and regulating crystallization via a composite amine complex, combined with a pre-baking step to suppress micro-explosions, the authors achieve Cu micropatterns with a highly dense surface morphology under ambient conditions. The resulting structures demonstrate a minimum resistivity of 9.34μΩ·cm (approximately 5.5 times that of bulk Cu) while maintaining sub-10μm linewidths. Moreover, this method exhibits broad processing adaptability and substrate compatibility, facilitating reliable metallization on flexible substrates, macroscopic wafers and curved surfaces. The fabricated Cu interconnects function as stable signal and power transmission pathways within a fully FsLDW-patterned UV photodetector. This study establishes a practical route for deploying high-performance conductive networks in advanced electronic systems. *(Opto-Electronic Manufacturing,* vol. 1, article 260002, 2026, https://doi.org/10.29026/oem.2026.260002*)*

Flexible/Wearable Electronics

"Programmable Spinning of Integrated Circuit Fibers"

Authors: Fengqiang Sun, *et all.*

Abstract: Textiles based on electronic fibers can be used to integrate sensing, processing, and feedback into a single wearable platform. However, embedding circuit-level functionality directly into fibers remains challenging due to poor fiber utilization and unstable interconnects. Here the authors report a programmable microfluidic spinning process to fabricate integrated circuit fibers. The approach combines conductive layers with different functional layers to create distinct modules capable of electron–photon conversion, electron–electron conversion, electron–ion carrier conversion and electro-quasistatic modulation. By arranging and integrating these modules during microfluidic spinning, customizable circuits within a single fiber can be built. The fibers can then be woven, sewn and arranged into textiles and can withstand repeated deformation and washing. The authors use the approach to create electroluminescent fibers for light emission, resistor and capacitor fibers for analog signal processing, organic

electrochemical transistor fibers for digital logic operations, and electro-quasistatic fibers for touchless sensing and control. *(Nature Electronics,* Oct. 2026, https://www.nature.com/articles/s41928-026-01712-2*)*

Inspection

"CDA-YOLO: An Improved YOLOv11 Model for PCB Defect Detection"

Authors: Anlong Yuan and Jingmin Li

Abstract: Printed circuit boards (PCBs) are fundamental to modern electronic systems, and their manufacturing quality directly determines the performance and reliability of the final product. However, existing YOLO-based defect detection models still face critical challenges, including high miss rates for tiny defects and frequent false positives caused by complex background textures. To address these issues, the authors propose CDA-YOLO, an enhanced YOLOv11 framework incorporating three key innovations. First, a Cross-level Bidirectional Feature Pyramid Network (CBiFPN) is designed, which effectively alleviates the loss of fine-grained details of small targets as features propagate through deep layers. Second, a lightweight Dual-Scale Convolution module (DualScaleConv) is proposed, which employs a parallel branch structure to simultaneously capture local details and global contextual information. Finally, a parameter-free average attention mechanism (PfAAM) is integrated into the C3k2 module to enhance the feature response in defect-related regions and suppress background noise. Experimental results demonstrate that the proposed model achieves competitive performance on the PCB defect dataset, with mAP@0.5 reaching 96.1% and mAP@0.5:0.95 reaching 56%, corresponding to improvements of 2.8% and 3.4% over the baseline YOLOv11, respectively. These results validate that CDA-YOLO offers an efficient and robust solution for industrial-grade PCB defect detection. *(Scientific Reports,* Oct. 19, 2026, https://doi.org/10.1038/s41598-026-74471-x*)*

Power Electronics

"A 98.8%-Efficient, Thermally-Optimized 48V-to-12V DC–DC Converter for High-Power Data Centers"

Authors: Ziqian Zhang

Abstract: This work presents the design of a 48V-to-12V high-power DC–DC converter based on a resonant switched-capacitor topology. By employing zero-current switching (ZCS) control, the prototype achieves a peak efficiency of 98.8% and a full-load efficiency of 96.1% under a 70 A load condition. To address the stringent power delivery requirements in data center high-performance computing (HPC) applications, particular emphasis is placed on optimizing PCB stack-up and via structures. A comparative study of different substrate designs demonstrates that an optimized multilayer PCB architecture improves the conversion efficiency by an additional 1.5%, while reducing the temperature rise of key power devices by 9.6 °C. Experimental validation confirms that the proposed design not only achieves ultra-high conversion efficiency but also significantly enhances thermal performance. The converter consistently maintains excellent electrical characteristics and thermal stability across a wide load range, meeting the requirements of modern data center power systems for high efficiency, high power density and high reliability. *(Frontiers in Electronics,* vol. 7, article 1697781, Apr. 15, 2026, https://www.frontiersin.org/journals/electronics/articles/10.3389/felec.2026.1697781/full*)*



PCB Chat

pcbchat.com

Recent Chat:

- **Finding Your Place in PCB Design**
  with MIROSLAVA VELASCO

The PCB Podcast