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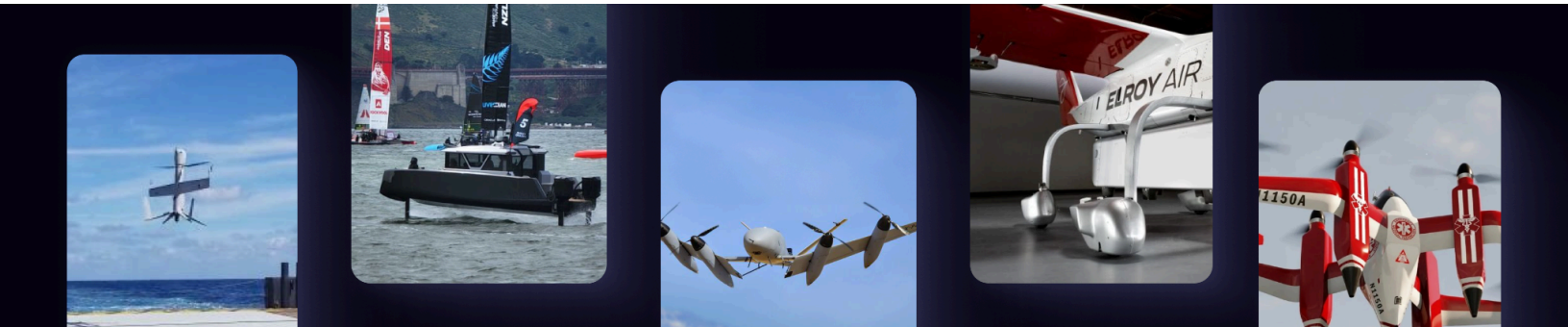
Clio Series B Physical ICD

601-0048-000 Rev. I

The Clio is a computation, communications, and power distribution hub designed to trade off electronics vs harness weight in a hub and spoke system. Depending on client needs the Clio can be just a low power data and power switch, or a high power flight computer.



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Introduction

The allocortech inc. Clio Series B (part number 100-0048) is a communications and power hub intended to bridge between point to point connections and redundant ring networks. The Series B evolved from the Series A by adding more I/O options, and changing processors to focus on performance and safety critical verification activities. In order to maximize flexibility, most communication pair pins can be CAN, RS485 or PWM; and in order to ease harnessing all trunk communications pairs can be daisy chained through to the distribution connector.

The Clio Series B has the following capabilities, although not all can be used at once:

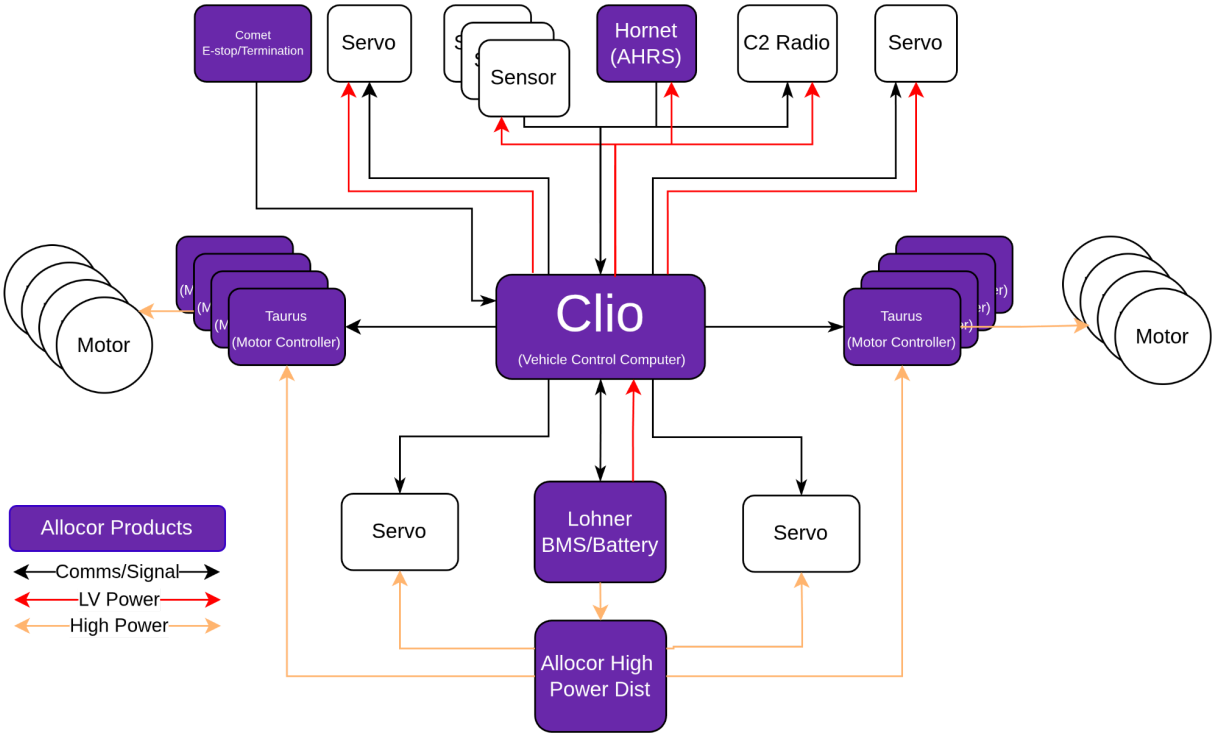
- 4x redundant 12~48VDC 5A power inputs with fault detection and backfeed prevention which can be bussed or split as required to allow for multiple voltage rails.
- 9x 12~48VDC 3.5A individually fused and switched power outputs with electronic circuit breaking.
    - Each output can be configured to turn off during an FTS event using the GPIO controller embedded in the onboard FPGA.
    - 2 of the 9 outputs may draw from a 3A maximum auxiliary buck switched power supply.
- 2x 10/100 auto MDI-X internally switched ethernet ports.
- 10x CAN FD busses up to 8Mbps.
- 15x half duplex RS-485 UARTs up to 8Mbps with hardware options to tie transceiver into receive or transmit only mode.
- 1x 5V full duplex invertible UART up to 1Mbps.
- 1x RS-232 up to 1Mbps.
- 3x isolated 50V/3A general purpose solid state relay switches.
- 2x isolated 50V/3mA general purpose constant current sink inputs.
- 2x +2.8 -2.5 V differential analog inputs with programmable gain.
- 1x 200mA 5V general purpose supply split across 2 supply pins.
- 400MHz ARM Cortex-M7 MCU.
    - Double precision hardware floating point unit.
    - 2MB on chip flash memory.
    - 1MB RAM.
    - 28MB off chip flash memory connected over QSPI.
- Optional expansion board with 3x SPI chip selects and dedicated full duplex UART.
    - Enclosure and boards are designed to allow an SMA connector and coax to the expansion board.

For more information about what options are available, please refer to the capability mapping tables.

Simple Architectural Concept

For a simplex architecture, a Clio Series B can act as an electronics hub to control and manage the entire vehicle. Primary vehicle command and control can all be run off of a single unit while simultaneously acting as a hub to communicate and power peripheral devices and sensors.

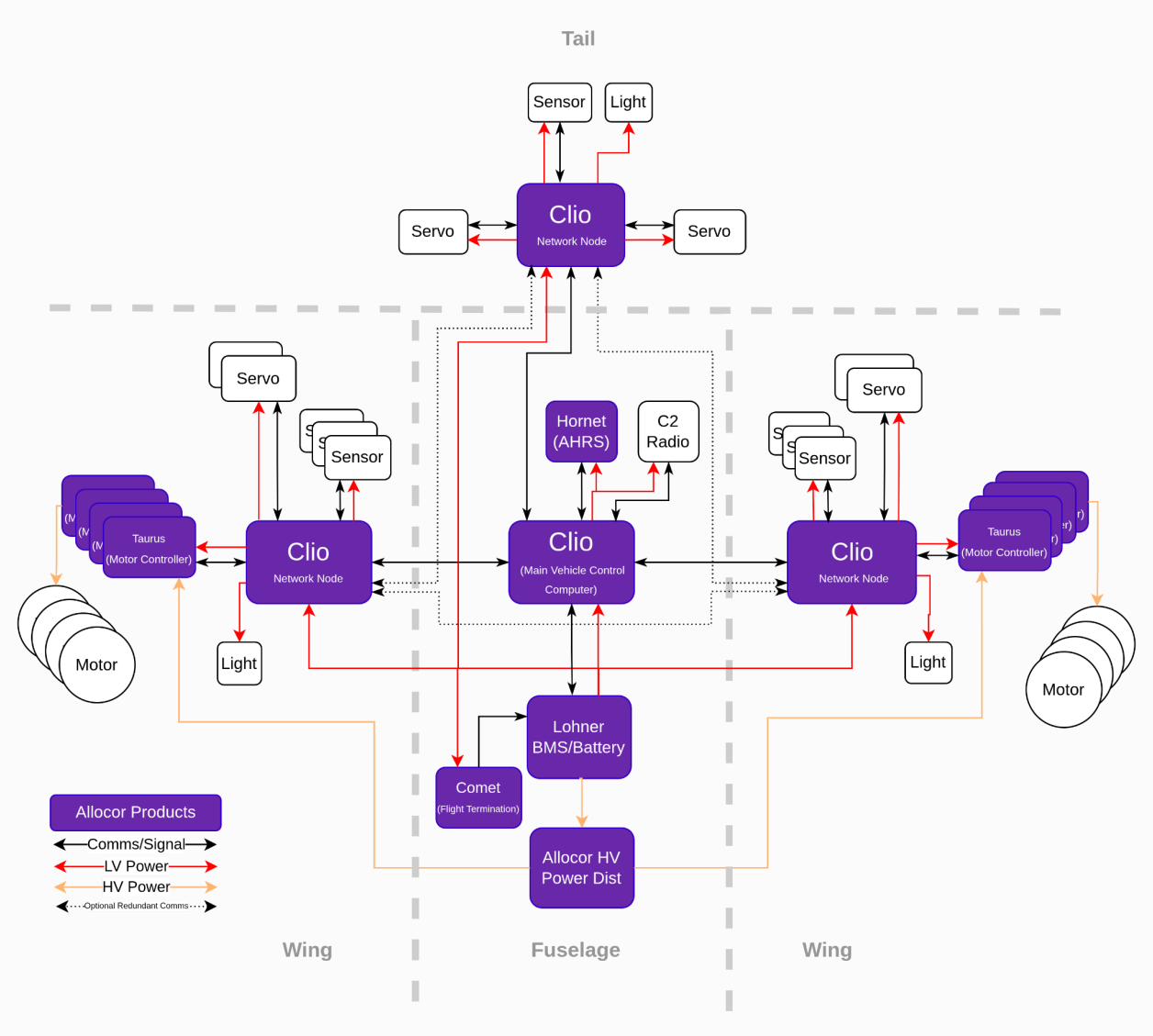
Simple, Centralized Architecture Enabled by Allocortech Products



Networked Architecture Concept

For more complicated vehicle systems that may require more I/O or power than a single Clio can provide, or if redundancy is desired, the diagram below depicts a possible vehicle architecture that utilizes multiple Clios as hubs throughout. This example references an aircraft layout but is equally applicable to other vehicles requiring simplification of distribution harnessing and possible redundancy.

Distributed Architecture for Complex Vehicles Enabled by Allocortech Products



History of Clio Series B

Allocortech has and likely will continue to make improvements to the electrical and mechanical design for reliability and production reasons. We refer to these as Mark numbers, and our practice is to use the first digit of the last triple to indicate what Mark a Clio is. (E.g. a 100-0048-023 and 100-0048-223 have the same configuration string but the first is a Mark I and the second is a Mark III.)

This list of changes is not exhaustive, but covers the high level points.

Mark I

First release of the Clio Series B, inheriting some design language from the Clio Series A but was radically different enough to warrant a new name. Specifically series B changed processors, operating system, added the FPGA for IO expansion, and changed connector series to gain more pins.

Mark II

Only affected the logic board; interrupt lines were remapped so that all SPI CAN devices could have a dedicated interrupt and the ethernet switch changed from LAN9354I/ML to LAN9303M due to part obsolescence.

Mark III

Only affected the connector board, current sensors can now read up to 45A for I^2T fuse emulation, and the current handling of the board was increased with additional copper layers.

Mark IV

Many changes to the logic board. A 1-wire EEPROM was added for storing production data, and the ability to have a personality 1-wire EEPROM in the harness was added. LPUART1 was added to be the debug console on the JTAG connector so that the expansion UART can be dedicated to the expansion connector. And the auxiliary supply can now trim almost the entire range of the input voltage. The maximum input voltage range was expanded to 60V, and customizations are no longer required to optimize the DC/DC supplies across the expected input range.

Mark V

The logic board was modified to make the ST loader port work reliably in ST bootloader mode.

Scope of this Document

This document covers the mechanical and electrical specifications of the allocortech inc Clio Series B (part number 100-0048 and variants.) The software development is discussed in allocortech document 600-0057-000 - SDK User Guide (provided upon request).

Version History

Revision	Changes
A	• Initial Draft
B	• Update GPO max current over temperature Correct Serial table D10 and D11 Correct description of J1:c Update GPO max current limit
C	• Update J2 image to correctly show pin 25 (previously misidentified as 23)
D	• Update Comms naming to match software (all caps)
E	• Signal naming updates for hardware/software/reference consistency • Added PWM support references • Corrected inconsistency in Dist 10 / Dist 11 capabilities • Added additional information on GPO/GPI/Expansion implementations • Added information about ST provided bootrom
F	• Added notes about what load outputs are connected to what power bus • Clarified meaning of 1 vs 0 in part encoder table for Loads 7 and 8
G	• For ease of harnessing and configuration, show all the I/O (except power) on the trunk and dist connectors in the capability mapping table. • Added information about isolated GPI, isolated GPO, and differential analog implementations. • Described the Mark IV 1-wire EEPROM • Updated the variant selection table to account for GPI pullups
H	• Clio architecture examples added • Added dev harness details • Updated current and voltage limits • Added Clio History section • Moved table of contents to top of document. • Added connector PN clarifications • Added additional Clio descriptions and use examples/architectures • Various wordsmithing, acronym updates, typo fixes • Added section for supplemental hardware/harnesses • Removed most references to obsolete Mark version details. • Switched to new template
I	• Added information about the IMU expansion board

List of Abbreviations

4W RS485	Four wire, full duplex, differential serial (aka RS422) with RS485 line levels.
A	Amps
AC	Alternating Current
ADC	Analog to Digital Converter
AUX	Auxiliary
BMS	Battery Management System
C2	Command and Control
CAN	Controller Area Network, serial protocol ISO 11898
CAN FD	Controller Area Network with Flexible Data Rate
DC	Direct Current
DIST	Distribution
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electromagnetic Interference
ETH	Ethernet
FIFO	First In First Out
FPGA	Field Programmable Gate Array
FTS	Flight Termination System
GND	Power or Digital Ground, isolated from Chassis Ground
GPI	General Purpose InputF
GPO	General Purpose Output
GPS	Global Positioning System
IMU	Inertial Measurement Unit
JTAG	Joint Test Action Group
LDO	Low Drop Out
LUT	Look-Up Table, in an FPGA refers to the smallest logic gate
MCU	Microcontroller Unit
MSL	Mean Sea Level
NOR	Not OR
PGA	Programmable Gain Amplifier
PPS	Pulse per Second Time Synchronization
PWM	Pulse Width Modulation
QSPI	Quad SPI, 4 synchronous bidirectional data lines and one clock
RAM	Random Access Memory
RX	Receive
SDK	Software Development Kit
SOA	Safe Operating Area
SPI	Serial Peripheral Interface
TTL	Transistor-Transistor Logic
TX	Transmit
UART	Serial Universal Asynchronous Receiver-Transmitter
V	Voltage
W	Watts

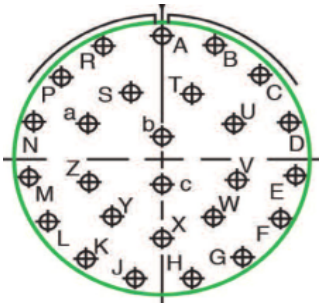
References

Reference	Title, Description, Location
ST AN2606	STM32 Bootloader Manual https://www.st.com/resource/en/application_note/cd00167594.pdf
ST AN3155	USART Protocol Used in the STM32 Bootloader https://www.st.com/resource/en/application_note/cd00264342-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
ST AN3154	CAN Protocol Used in the STM32 Bootloader https://www.st.com/resource/en/application_note/cd00264321-can-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Electrical Interface

Connector Pinouts

J1 - Trunk Connector



Face view of receptacle 38999 17-26P N key. 26x size 20 male pins, 5A each. Reference receptacle part number: D38999/24FE26PN*

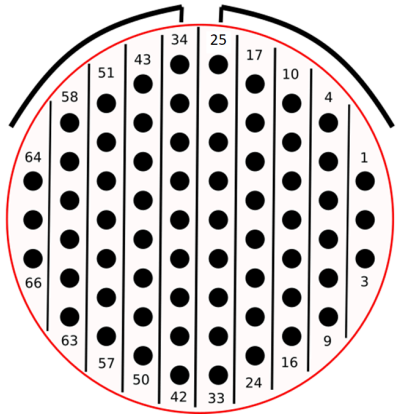
Available in aluminum or composite, with Olive Drab Chromium, Electroless Nickel, or Black Nickel (aluminum only) plating.

Mates with any 38999 tri-start N key compatible 17-26 (E shell) plug with female sockets. Pins usually crimp from AWG 20 thru 24. Reference connector part number: D38999/26FE26SN*

*Note that these can vary depending on the material/finish selected. In the reference PN provided “F” denotes an electroless nickel plating.

Pin	Name	Primary Function	Alt. Function	Notes
A	VIN 2 -	Bus B Return	-	
B	VIN 2 +	Bus B Supply	-	12A Slow Blow Fuse, 50V Max Continuous
C	VIN 1 -	Bus A Return	-	
D	VIN 1 +	Bus A Supply	-	12A Slow Blow Fuse, 50V Max Continuous
E	VIN 0 -	Bus A Return	-	
F	VIN 0 +	Bus A Supply	-	12A Slow Blow Fuse, 50V Max Continuous
G	VIN 3 -	Bus C Return	-	
H	Trunk 3 -	RS485_T3 N	-	Optional daisy chain to J2:29, J2:30 (Chain B) Programmable 120 Ohm termination
J	TRUNK_3 +	RS485_T3 P	-	
K	TRUNK_1 -	CAN_T1 L	-	Optional daisy chain to J2:20, J2:28 (Chain C) Programmable 120 Ohm termination
L	TRUNK_1 +	CAN_T1 H	-	
M	Eth 0 RX -	Ethernet 0	-	
N	Eth 0 RX +	Ethernet 0	-	
P	Eth 0 TX -	Ethernet 0	-	
R	Eth 0 TX +	Ethernet 0	-	
S	Reserved	-	-	
T	FTS Analog +	3A Current Loop	28V Voltage Loop	In voltage mode, optional daisy chain to J2:46, J2:47
U	FTS Analog -			
V	TRUNK_4 -	RS485_T4 N	-	Optional daisy chain to J2:46, J2:47 (Chain A) Programmable 120 Ohm termination Usable as FTS / E-Stop GPIO
W	TRUNK_4 +	RS485_T4 P	-	
X	TRUNK_2 -	RS485_T2 N	-	Daisy chained to J2:61, J2:66 Programmable 120 Ohm termination
Y	TRUNK_2 +	RS485_T2 P	-	
Z	TRUNK_0 -	CAN_T0 L	-	Daisy chained to J2:60, J2:64 Programmable 120 Ohm termination STM32 CAN Bootloader
a	TRUNK_0 +	CAN_T0 H	-	
b	Recovery	MCU Boot Mode	-	Short to ground to enter STM32 bootloader mode. Use CAN_T0 or RS485_D10 to load code.
c	VIN 3 +	Bus C Supply	-	12A Slow Blow Fuse, 50V Max Continuous

J2 - Distribution Connector



Face view of receptacle 38999 19-35S N key. 66x size 22D female sockets, 3.5A each. Reference receptacle part number: D38999/24FF35PN*.

Available in aluminum or composite, with Olive Drab Chromium, Electroless Nickel, or Black Nickel (aluminum only) plating.

Mates with any 38999 tri-start N key compatible 19-35 (F shell) plug with male pins. Pins usually crimp from AWG 22 thru 28. Reference connector part number: D38999/26FF35PN*.

*Note that these can vary depending on the material/finish requirements. In the reference PN provided “F” denotes an electroless nickel plating.

Pin	Name	Primary Function	Alt. Function	Notes
1	DIST_6 +	RS485_D6 P	CAN_D6 H	
2	DIST_5 -	RS485_D5 N	CAN_D5 L	
3	DIST_5 +	RS485_D5 P	CAN_D5 H	
4	DIST_7 +	RS485_D7 P	CAN_D7 H	
5	DIST_6 -	RS485_D6 N	CAN_D L	
6	DIST_11 -	RS485_D11 N	RS232_D11 RX	
7	DIST_11 +	RS485_D11 P	RS232_D11 TX	
8	DIST_4 -	RS485_D4 N	CAN_D4 L	
9	DIST_4 +	RS485_D4 P	CAN_D4 H	
10	DIST_7 -	RS485_D7 N	CAN_D7 L	
11	LOAD_6 +	LOAD_6 Supply	-	Power bus B
12	GPI_1 +	GPI_1 High	-	
13	GPI_1 -	GPI_1 Low	GND	Factory option for GND tie
14	TTL/5V	TTL_D10 TX	200mA 5V	STM32 UART bootloader 5V TTL TX, invertible Power shared with J2:31 Return to pin J2:22
15	DIST_10 +	TTL_D10 RX	RS485_D10 P	
16	DIST_3 -	RS485_D3 N	CAN_D3 L	
17	DIST_9 +	RS485_D9 P	-	
18	GND	LOAD_6 Return	-	
19	GPI 0 -	GPI_0 Low	GND	Factory option for GND tie
20	Chain C -	CAN_T1 L	Analog 0 -	
21	GND	TTL/5V Return	-	Has TVS Diode to TTL_D10
22	DIST_10 -	2.5V TTL Bias	RS485_D10 N	Leave floating when using TTL_D10
23	LOAD_8 +	LOAD_8 Supply	-	Power bus C
24	DIST_3 +	RS485_D3 P	CAN_D3 H	
25	DIST_9 -	RS485_D9 N	-	
26	LOAD_5 +	LOAD_5 Supply	-	Power bus B
27	GPI 0 +	GPI_0 High	-	
28	Chain C +	CAN_T1 H	Analog 0 +	

Pin	Name	Primary Function	Alt. Function	Notes
29	Chain B +	RS485_T3 P	Analog 1 +	
30	Chain B -	RS485_T3 N	Analog 1 -	
31	5V	200mA 5V	-	Power shared with J2:14
32	GND	LOAD_8 Return	-	
33	DIST_2 -	RS485_D2 N	CAN_D2 L	
34	DIST_0	CAN_D0 H	Eth 1 RX -	Reversed polarity between primary and secondary functions.
35	GND	LOAD_4 Return	-	
36	GND	LOAD_5 Return	-	
37	GND	5V Return	-	Notional return for J2:31
38	GND	LOAD_2 Return	-	
39	GND	LOAD_1 Return	-	
40	GND	LOAD_7 Return	-	
41	LOAD_7 +	LOAD_7 Supply	-	Power bus C
42	DIST_2 +	RS485_D2 P	CAN_D2 H	
43	DIST_0	CAN_D0 L	Eth 1 RX +	Reversed polarity between primary and secondary functions.
44	LOAD_4 +	LOAD_4 Supply	-	Power bus B
45	GND	LOAD_3 Return	-	
46	Chain A +	RS485_T4 P	FTS Analog +	
47	Chain A -	RS485_T4 N	FTS Analog -	
48	GND	LOAD_0 Return	-	
49	LOAD_1 +	LOAD_1 Supply	-	Power bus A
50	DIST_1 -	RS485_D1 N	CAN_D1 L	
51	DIST_8	RS485_D8 P	Eth 1 TX -	Reversed polarity between primary and secondary functions.
52	GPO 0 -	GPO_0 Return	GND	Factory option for GND tie
53	GPO 0 +	GPO_0 Input	-	
54	GPO 1 -	GPO_1 Return	GND	Factory option for GND tie
55	GPO 1 +	GPO_1 Input	-	
56	GPO 2 +	GPO_2 Input	-	
57	DIST_1 +	RS485_D1 P	CAN_D1 H	
58	DIST_8	RS485_D8 N	Eth 1 TX +	Reversed polarity between primary and secondary functions.
59	LOAD_3 +	LOAD_3 Supply	-	Power bus A
60	TRUNK_0 +	CAN_T0 H	-	Daisy chained from Trunk connector
61	TRUNK_2 +	RS485_T2 P	-	Daisy chained from Trunk connector
62	GPO 2 -	GPO_2 Return	GND	Factory option for GND tie
63	LOAD_0 +	LOAD_0 Supply	-	Power bus A
64	TRUNK_0 -	CAN_T0 L	-	Daisy chained from Trunk connector
65	LOAD_2 +	LOAD_2 Supply	-	Power bus A
66	TRUNK_2 -	RS485_T2 N	-	Daisy chained from Trunk connector

J3 - Expansion Connector

As a factory option for the purposes of expansion, both the Clio Series B enclosure and PCB assembly have been designed to accommodate a single male SMA connector or pressure barb. A standard enclosure will not have the hole drilled, nor will it have the marking text. Contact allocortech about expansion board options.

Chassis Bond Stud

For enhanced bonding between the Clio Series B and vehicle chassis, a M3 bonding stud can be installed in the baseplate with a countersunk M3 screw with the intent of allowing a low resistance connection.

Electrical Characteristics

Absolute Maximums

Parameter	Min	Max	Unit
Input Voltage on VIN 0-3[1]	12	60	V
Total Current through Single VIN		12	A
Total Combined Current through all VIN (Peak)[2]		48	A
Output Current to LOAD 0-8 (Peak)[3]		6	A
GPI Voltage between +/-	-8.5	60	V
GPI Isolation to GND		60	V
GPO Voltage between +/-		60	V
GPO Current between +/- (AC or DC)[4] @ 25°C		3	A
GPO Isolation to GND		60	V
RS485 / CAN / PWM Common Mode (Continuous)	-25	25	V
RS485 / CAN / PWM Common Mode (Transient)	-58	58	V
RS485 / CAN / PWM Differential (Continuous)	-5	10	V
RS485 / CAN / PWM Differential (Transient)	-17	17	V
FTS Analog Differential Voltage (Voltage Mode, Continuous)	-13	60	V
FTS Analog Current (Current Mode, Continuous)		5	A

[1] Nominal Max voltage is 50V however a 60V option can be provided.
[2] The continuous rating is 5A governed by the pin rating, 20A total
[3] The continuous rating is 3.5A per channel
[4] The full safe operating area (SOA) curve for the GPO optoisolator is given in the Isolated Outputs section.

Parameter	Min	Max	Unit
Auxiliary Analog Inputs to GND (Continuous)	-16	16	V

Power Topology

The Clio series B can provide up to 20A continuous power to nine 3.5A outputs at bus voltage and two 5V (200mA combined max) outputs. Power is broken into three power buses (A, B, and C) which can operate independently or be tied together. The A bus, in addition to powering the switched loads, also powers the processor, transceivers, and 3A auxiliary buck switched mode power supply.

The four power inputs on the Clio are protected by slow blow 10A fuses, transient protection diodes, and an ideal diode preventing power from flowing backwards. Each input monitors the supply voltage and the return current. This monitoring allows detection of blown fuses, broken wires, and potentially ground loops.

The nine 6A outputs are current-monitored by the MCU and are all individually fused with fast blow 6A fuses. It is expected that power supplied to a remote load/device is returned to the Clio on the designated pin. Failure to do so may trip the Clio's ground fault detection feature. Soft start functionality is expected to be present on the remote load if a current draw above 3.5A occurs at startup.

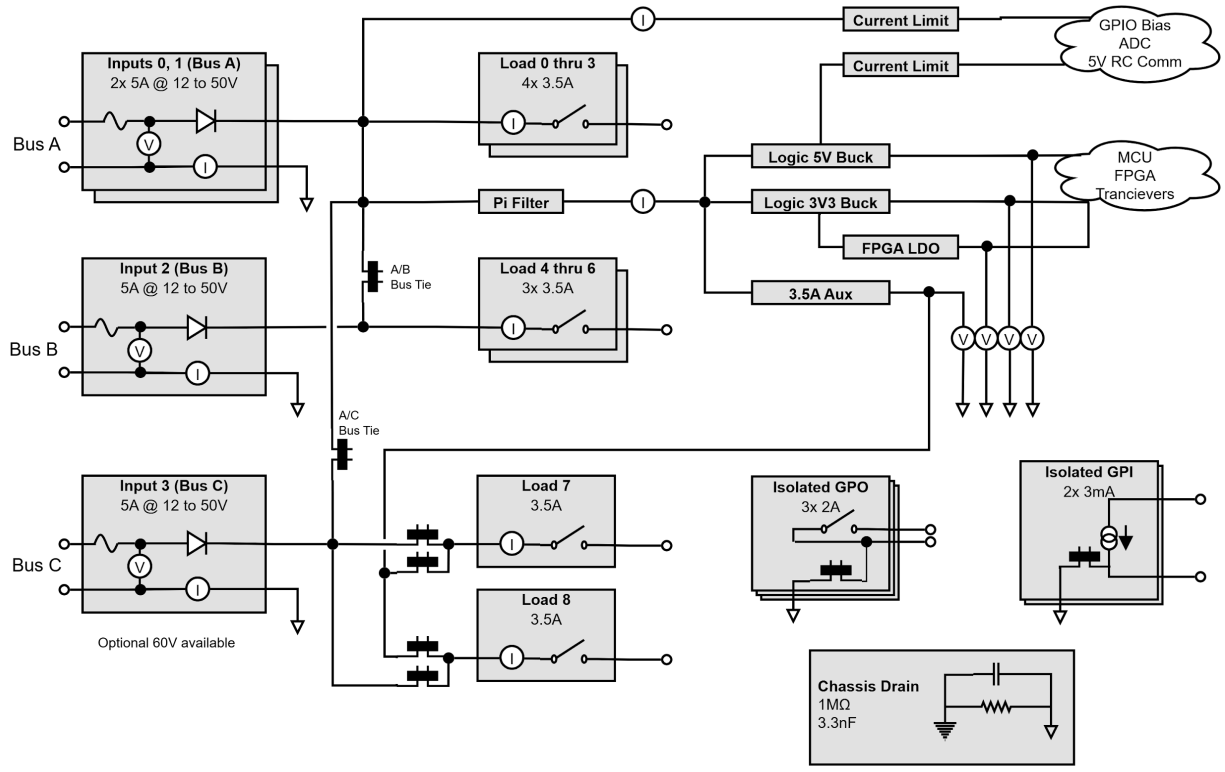
If used, the auxiliary power supply can regulate from within a volt of the Bus A voltage down to 5V in 10mV steps and can supply up to 3A of current.

The Clio (Mark I, II, III) nominally operates from 12 to 36VDC (50VDC maximum), with a factory option to shift the range up from 24 to 48VDC nominal (60V maximum) (Mark IV+).

The worst case power draw for the internal logic is estimated to be no more than 15W if all but one transceiver is operating nominally and one transceiver is driving a shorted bus.

The Clio is not explicitly rated for any specific hold up time in the case of complete power loss although it is capable of several hundred microseconds depending on the load (consult Allocortech for application specific estimates).

The Clio chassis is capacitively and resistively (1 Mega Ohm) coupled to power return for EMI and voltage transients, it is expected that the power sources have a low resistance connection between chassis and return.



Baseline power topology diagram.

Capability Mapping

There are several types of serial communications present on the Clio. Any interface that could be conceptually used as a safety critical trunking interface is brought directly to the MCU, and is chainable. All other communications go through some form of external peripheral controller and are usually overlaid with other compatible communications busses so that many protocols can be served by a single set of hardware.

Pair # *	CAN	485	232	5V TTL	PWM	Eth	ADC	Daisy Chain	Note
TRUNK_0	MCU							Always	STM32 bootloader
TRUNK_1	MCU							C	
TRUNK_2		MCU						Always	
TRUNK_3		MCU						B	
TRUNK_4		FPGA			Y			A	FTS GPIO
TRUNK_5							FPGA	A	FTS Analog
TRUNK_6						Eth 0			
TRUNK_7						Eth 0			
DIST_0	SPI					Eth 1			
DIST_1	SPI	FPGA			FPGA				
DIST_2	SPI	FPGA			FPGA				
DIST_3	SPI	FPGA			FPGA				
DIST_4	SPI	FPGA			FPGA				
DIST_5	SPI	FPGA			FPGA				
DIST_6	SPI	FPGA			FPGA				
DIST_7	SPI	FPGA			FPGA				
DIST_8		FPGA			FPGA	Eth 1			
DIST_9		FPGA			FPGA				
DIST_10		MCU		MCU / RX					STM32 bootloader No termination
DIST_11		FPGA	FPGA		FPGA				
Aux5V_0				MCU / TX					DIST_10 or always on
Aux5V_1									Always on
GPI_0					FPGA				PWM Capture or arbitrary input
GPI_1					FPGA				
GPO_0					FPGA				PWM Generation or arbitrary output
GPO_1					FPGA				
GPO_2					FPGA				

** Note: Pair# here match software registry port names*

Daisy Chaining of Signals

The Clio carries several signal pairs from the J1 Trunk connector to the J2 Distribution connector for the purpose of removing the need for harness breaks when chaining several devices together on the communications trunks. Restated, the Clio itself can act as an inline harness break or signal tee. Of the 5 signal pairs that chain through the Clio, 2 of them (TRUNK_0 CAN and TRUNK_2 RS485) are fixed while the other 3 are factory selectable for which function they perform.

J2 Name	CAN	485	ADC
TRUNK_0	TRUNK_0		
TRUNK_2		TRUNK_2	
Chain A		TRUNK_4	FTS Analog
Chain B		TRUNK_3	Analog_1
Chain C	TRUNK_1		Analog_0

Selection of what signals are present on each chain is a factory option.

The FTS can only be daisy chained in voltage mode.

CAN

The Clio Series B can expose up to ten CAN-FD busses capable of operation up to 8Mbps. Two of the buses are native to the MCU. The remaining eight CAN buses are produced by SPI CAN controllers attached in pairs to dedicated SPI controllers. The two MCU connected CAN busses are connected to the trunk connector and are optionally daisy chainable to the distribution connector.

All CAN buses use Microchip MCP2542 transceivers which feature 13kV ESD protection (IEC 61000-4-2) and +/- 58VDC common mode protection. Trunk CAN lines are further protected with a common mode choke and have programmable, or optionally factory fixed, 120 Ohm termination. Distribution CAN lines have factory installed 120 Ohm termination resistors.

UARTs

Trunk RS-485

The Clio Series B has three half duplex RS-485 pairs present on the trunk connector, all with hardware duplex control and capable of operation up to 8Mbps. Two of these pairs are controlled by the MCU and are powered with 5V for maximum differential voltage swing. The third is controlled by the FPGA, and is powered from 3.3V. All transceivers are fault tolerant to differential shorts, have high common mode range, are further protected with common mode chokes and all have programmable, or optionally factory fixed, 120 Ohm termination.

If required, all trunk transceivers can be factory modified to operate in receive only mode.

As a general rule, Allocortech uses ESD and high common mode tolerant transceivers (such as the THVD2450 and MAX14775) operated at at least 3.3V. However due to part sourcing and board layout considerations the exact parameters may change over time. Contact Allocortech for more information about the specifics in a given Clio part and serial number range.

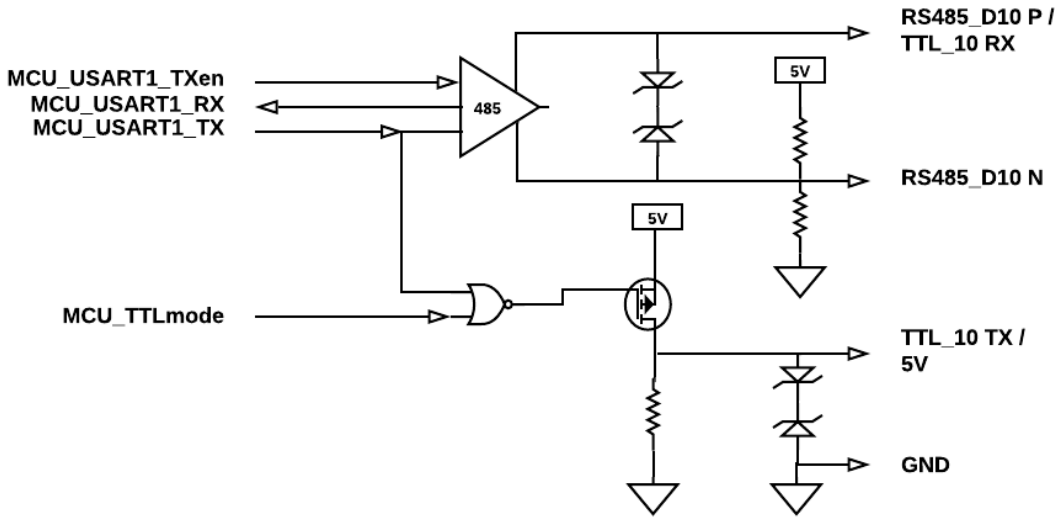
Distribution RS-485

There are eleven half duplex RS-485 pairs present on the distribution connector, all with hardware duplex control and capable of operation up to 8Mbps. Ten of these eleven are connected to the FPGA. The eleventh UART is the STM32 bootloader UART which is connected to the MCU. All transceivers on the distribution are powered from 3.3V, are fault tolerant to differential shorts, have high common mode range, and have fixed termination options, except for the RS-232 capable pair which has programmable termination, and the TTL capable pair which has no termination.

Distribution RS-232 (Dist 11)

Using an LTC2873, the Clio Series B is able to offer a combined RS-232 and RS-485 port. This device turns the differential pair into TX and RX as well as offering a programmable resistor in RS-485 mode.

Distribution 5V TTL (Dist 10)



A single 5V TTL UART is provided for devices such as RC receivers and other low voltage sensors that have short communication runs and are not safety critical. This UART operates by weakly biasing the negative side of a RS485 transceiver at 2.5V. The RX is then expected to exceed 2.5V by at least 200mV; notionally from GND to +5 but GND to +3.3V is also acceptable. The transmit side is operated by using a high side FET and

strong pull down from 5V to GND. This port is software invertible, meaning that mark and space can be either 5V or GND.

When this port is operating in TTL mode, the maximum baud rate is 56kbps. Improvements to the biasing network can be made to improve the performance of this port up to 115.2kbps at the expense of additional power draw when operating in 5V supply mode.

Ethernet

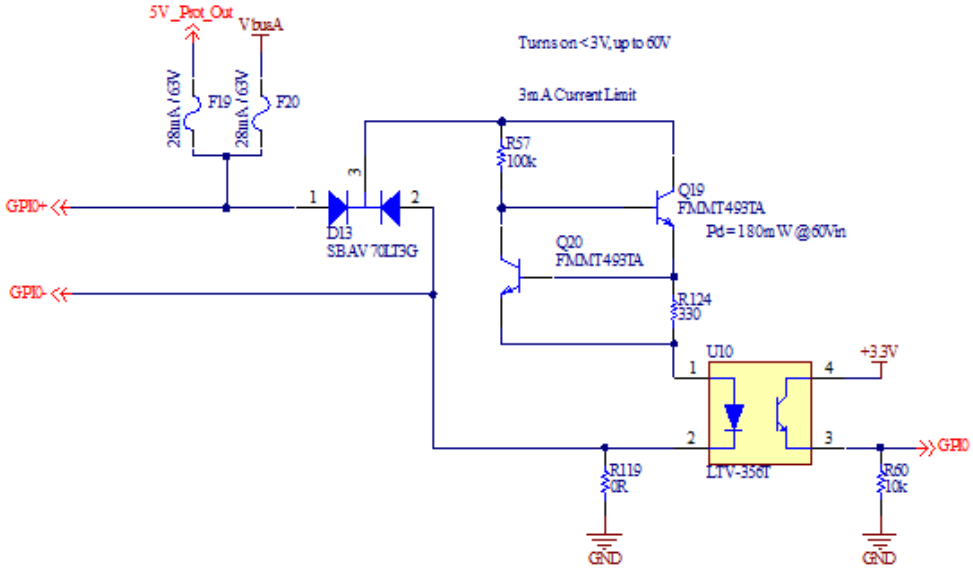
Clio series B offers up to two external 10/00 Auto-MDIX magnetically coupled ethernet ports. These ports are controlled by an internal three port managed switch with the third port directly attached to the native MCU media access controller. The Allocortech SDK provides access to the switch registers over I2C for advanced configuration.

Discrete Digital Inputs / Outputs

Isolated Inputs

Provided on the J2 “Distribution” connector are 2 isolated two port inputs. These are approximately 3mA constant current sinks that have a guaranteed turn off below 1.6V and a guaranteed turn on at or above 3.3V. These voltages are referenced to the Low side return. Logic High can be up to 50V relative to Low. Note that High and Low can not exceed 50V referenced from the Clio power return.

If the device connecting to the Clio does not provide a logic reference, connect Low to the remote device's power return at the remote location. If sufficient signal margin is available with respect to ground differences between the Clio and the remote driver, a factory option to tie the Low side to GND inside the enclosure is available.

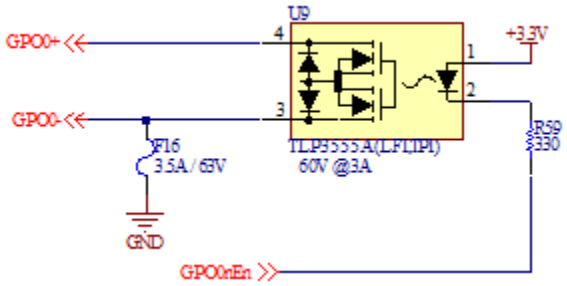


Isolated GPI on Mark III onwards

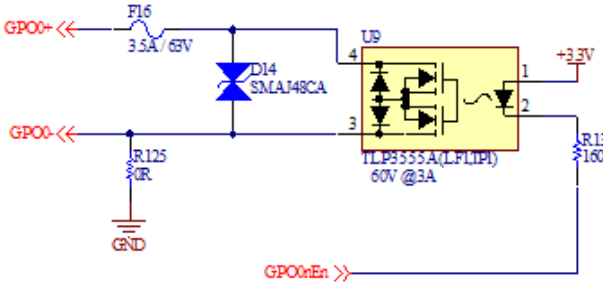
Isolated Outputs

Provided on the J2 “Distribution” connector are 3 isolated relay connections. These can handle up to 50V relative to Clio power return and 3A of AC or DC current. As a factory option, one leg of each GPO may be tied to the internal power ground.

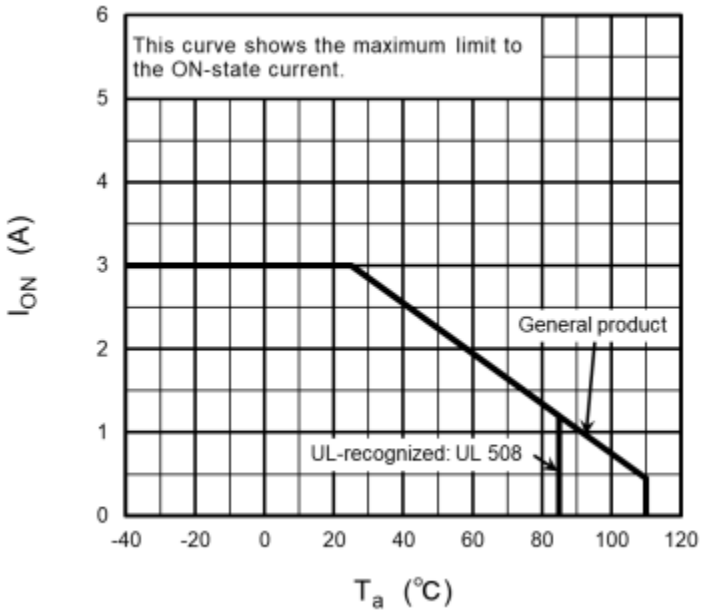
These outputs must be derated for the operating temperature. At the peak operating temperature of the Clio (70°C) the derated current limit is 1.5A.



Isolated GPO on Mark I and II



Isolated GPO on Mark III onwards



Safe Operating Area of TLP3555A Optoisolator

UARTs as Differential GPIO

All UARTs connected to the FPGA can be repurposed as differential GPIO using RS485 signal levels in software. If configured as an output; the output state when the FTS is triggered is software configurable.

UARTs as PWM Outputs

All UARTs connected to the FPGA can be repurposed as pulse width modulated outputs with 16 bit output/compare registers off a 64MHz clock with a 16 bit integer divider. The output state when the FTS is triggered is software configurable.

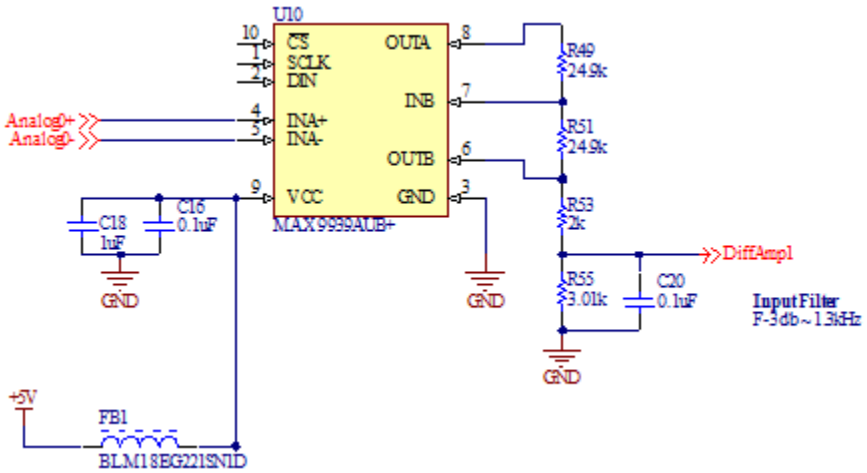
Additional functionality such as PWM capture, or specialty protocols that overlay communications channels on top of the PWM signal are available on request with specialized FPGA firmware builds.

Differential Analog Inputs

Provided on the J2 “Distribution” connector are 2 differential analog inputs. These are -2.5V to +2.8V inputs sampled with a 16 bit ADC and have a 50Hz low pass filter applied. The break frequency for the hardware is 1.3khz and as such sampling can be tailored considering this value and Nyquist sampling theorem. There is a programmable gain stage between the input and ADC which ranges from 0.2 to 157 V/V.

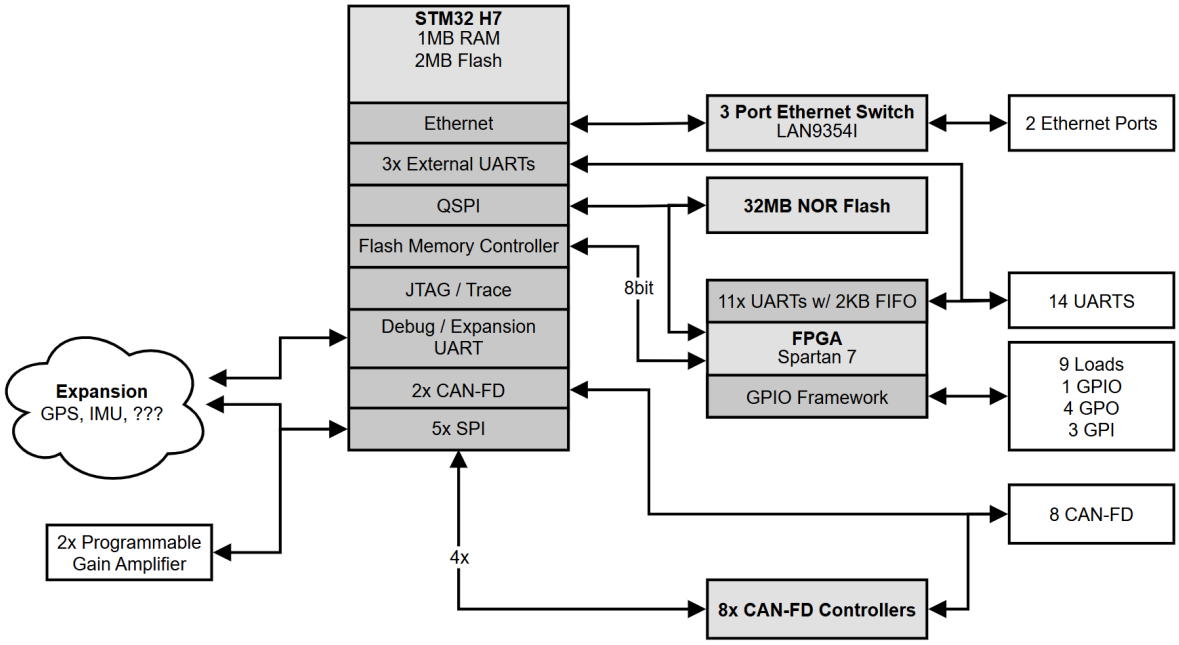
If needed, the analog source can be powered with an internally generated 5V source which is shared with the remote control UART. If the combined load on this supply exceeds 200mA the supply will enter a continuous retry mode.

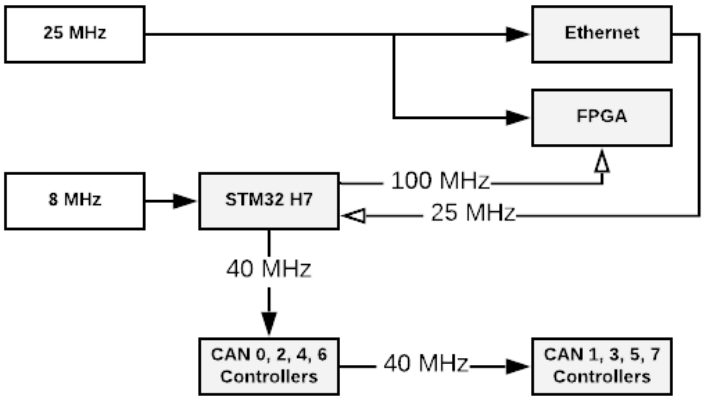
Note that the inputs cannot go below -16V or above +16V referenced to “5V Return”, aka GND. No other protection is applied.



SPI Controlled PGA Network for Differential Analog

Compute Complex





MCU

A mixture of STM32H753 and STM32H743 processors have been used in the various production runs of the Clio Series B due to parts availability. If hardware accelerated cryptography (H753) is desired, contact Allocortech to ensure the shipped product is compliant.

The STM32H7x3 series of MCU are capable of operating up to 400MHz and have 2MB of flash and 1MB of RAM.

FPGA

Attached to the STM32H7 via 8-bit parallel bus is a Xilinx Spartan 7 with at least 25k LUTs. This FPGA is used to control the distribution UARTs, load channels, GPIO, and flight termination analog signal.

Although the FPGA is not capable of offloading general purpose calculations from the MCU due to the bandwidth of the parallel bus, it is able to offload communications packet processing if desired.

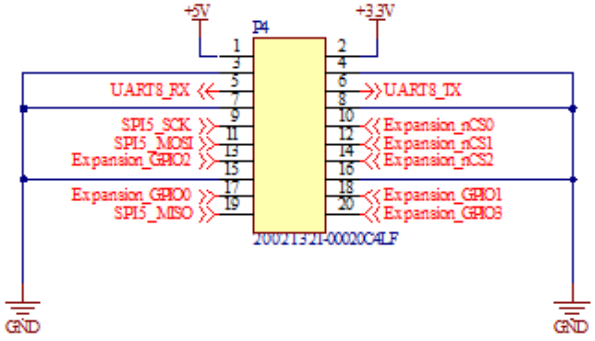
In future revisions of the product, the FPGA may also be responsible for distribution CAN instead of using the MCP2518FD SPI controller.

NOR Flash / QSPI

Attached to both the processor and FPGA via QSPI is a 32MB NOR Flash. The first 4MB of this flash is dedicated to the FPGA firmware, but the remaining 28MB are available to the user, which could be used for anything ranging from storing reference models, flight plans or generally running desired applications. The QSPI flash is mapped into the MCU address space for cached and prefetch capable read operations.

Expansion Connector

Clio Series B provides a user expansion header on the bottom side of the logic board. This header exposes a dedicated SPI bus with 7 GPIO capable of being chip select or interrupt lines and a full duplex UART. Power is provided at 5 and 3.3V. For further information contact allocortech. Note that use of the expansion header may drive small modifications to the enclosure size due to the added internal components.



Status LED

A tri-color daylight-visible status LED is provided, exposed through a light pipe on the top of the enclosure, for user specified informational or debugging purposes.

Allocor's standard bootloader will blink the LED green at 1Hz to indicate it's in bootloader mode. Other typical color coding includes blinking RED for errors.

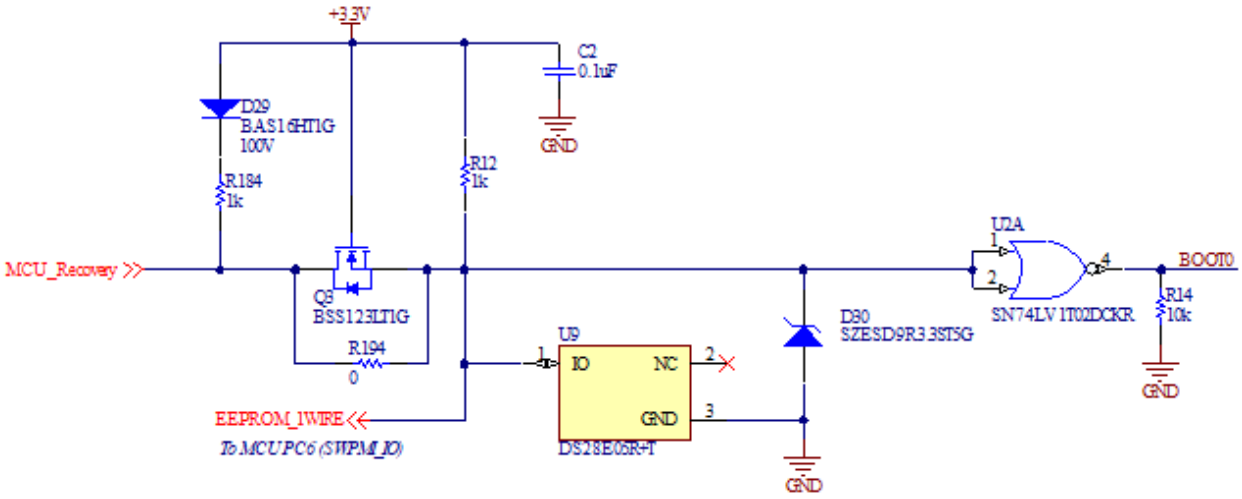
In other instances users have utilized the LED to color code Clio positions or software loads with a solid color of the users choosing. Ex. Blue for Main, White for a forward Unit, Purple for rear.

Bootloading and Vehicle Personality

STMicroelectronics provides the STM32H7 with a serial bootrom, accessible on boot if the Recovery pin (J1:b) is shorted to ground. When the processor is in this mode, communication with the bootrom is possible over Dist 10 (with either RS-485 or TTL) or Trunk 0 (CAN.) See ST AN2606, ST AN3155, and ST AN3154 for further information about interacting with the bootrom.

With the allocortech reference booty bootloader, or a customer supplied bootloader, loading of the MCU internal flash and the FPGA firmware to the QSPI flash is possible over any UART, CAN, or Ethernet connection.

From Mark IV onwards, also attached to the MCU recovery pin is a 112 byte 1-wire EEPROM which allocortech uses to store device revision information and small amounts of configuration. Additional 1-wire devices can be chained in the harness to store end user information as desired, such as addressing units to denote position in a vehicle or other function specific information..



Recovery and 1-Wire EEPROM Network

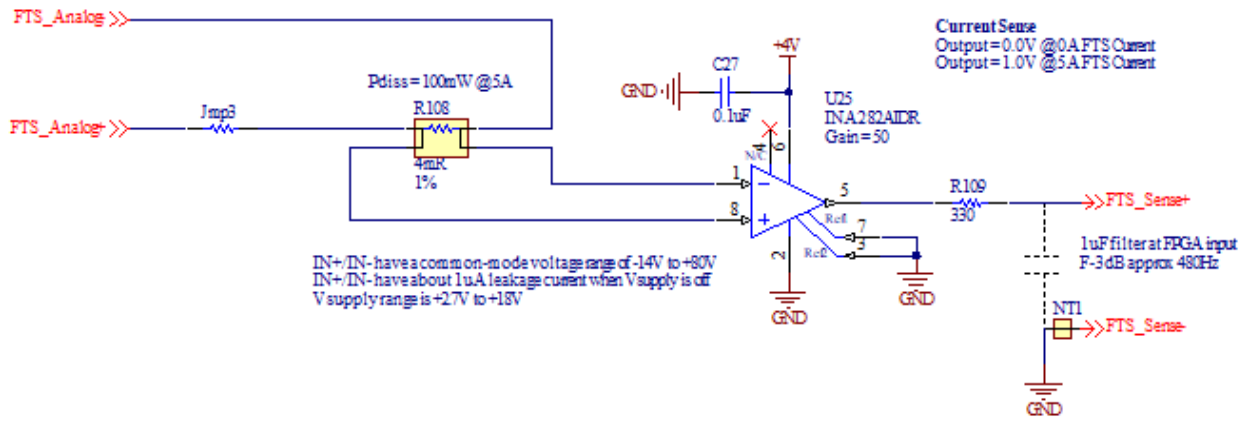
Safety Critical Considerations

Flight Termination System / E-Stop

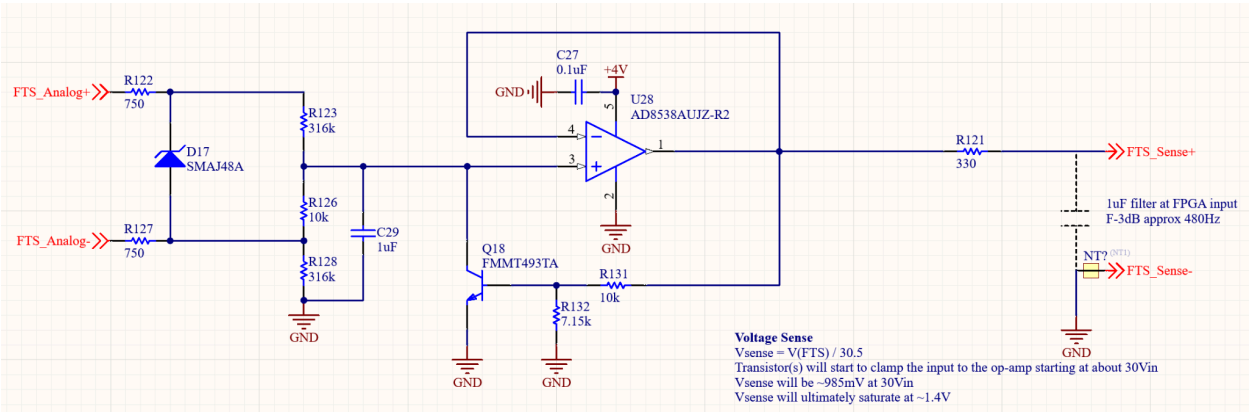
Provided on the J1 “Trunk” connector is an analog input which feeds the FPGA XADC. This analog input is factory selectable as either a current sense or voltage sense input. Notionally this analog input is used as a signal to the FPGA to set all load and GPO signals to a software selectable state, but can be repurposed by the user as desired. When operated as an FTS/e-stop, once configured the operation is independent of MCU operation.

If this input is unused, the pins should be left floating at the connector.

If externally induced FTS/E-stop functionality is required check out allocortech’s Comet system which provides a dedicated vehicle and operator units with a dedicated RF link to provide remote FTS/E-stop for a vehicle.



FTS/E-Stop Current Sense

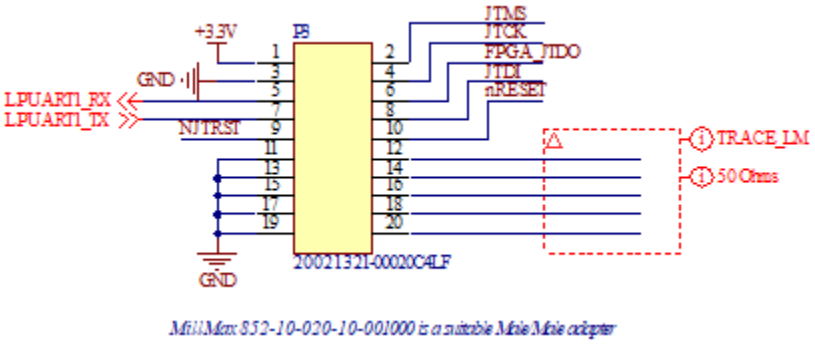


FTS/E-Stop Voltage Sense

MCU Code Coverage

For the purposes of code coverage and on-target debugging, a 4-bit ARM Trace and JTAG connector is present. The JTAG chain includes the FPGA. The pinout chosen is compatible with common trace capable debuggers like those provided by Lauterbach, but adapters can easily be made if required.

Allocortech produces a JTAG adapter board for general purpose embedded debugging, please contact allocortech for more information about part number 120-0061.



Trace Connector (Mark IV onwards)

For use with non-trace capable debuggers, allocortech has produced a common adapter board for the 10-pin ST Link V2, 14-pin STLink V3 (including the UART), 6-pin Digilent JTAG 2, and other common debuggers. Users should contact allocortech for more information.

Hardware in the Loop Emulation

As a special order factory option, the Clio may be fitted with features to facilitate Hardware in the Loop (HIL) testing. These features include raising the effective sensitivity of all current measurements so that heavy loads may be simulated in a HIL environment without heavy cabling and power supply requirements.

Health Monitoring

The Clio Series B contains several sensors designed to monitor the health of the unit including thermistors, input power return current monitoring, and voltage monitoring of all rails

Hardware Monitor

For use in dual-dual or fail stop control schemes, an additional processor can be added to the Clio Series B by use of an interposer circuit board between the logic board and connector boards. Such a processor can be used to monitor all the serial and GPIO signals and override or cut power to the main processor as required.

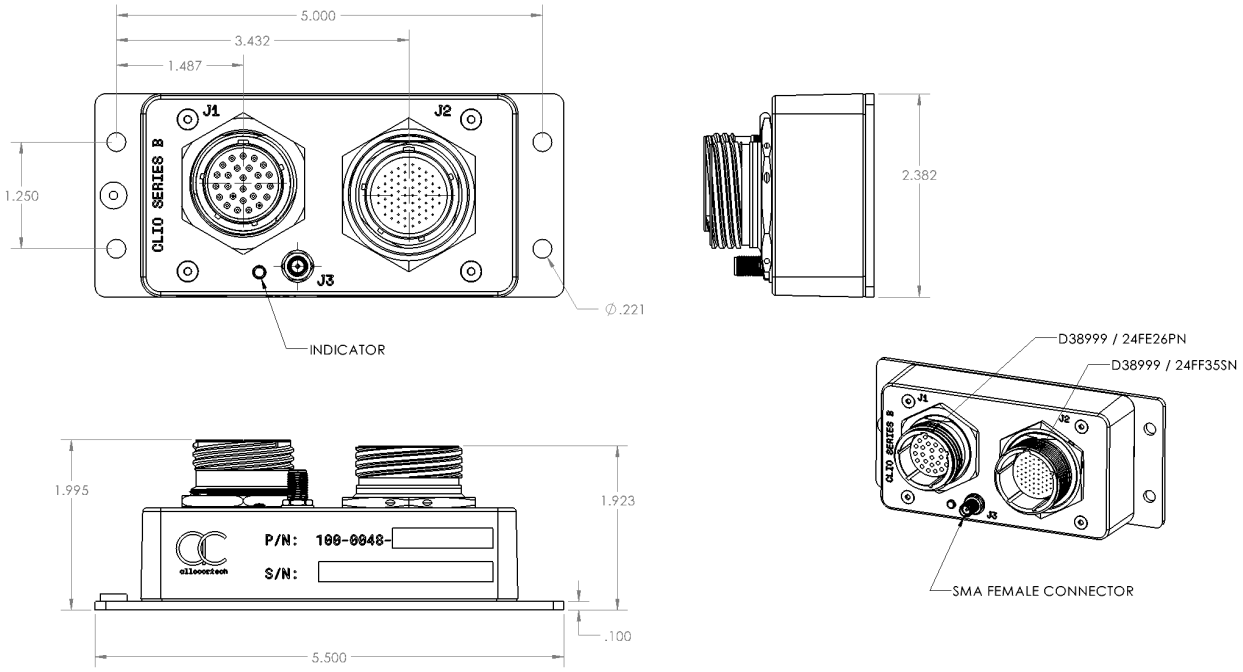
Signal Conditioning / Protection

The Clio Series B is implemented as a logic board containing the MCU, FPGA, and transceivers, and a connector board that performs signal conditioning and power distribution.. If stronger signal or power line protection is required, allocortech can produce and test a custom connector board on request.

Mechanical Interface

Dimensions

Measurements given in inches.



NOTE: The SMA connector shown is optional and would typically only be installed on units with an expansion card for use with a GNSS antenna..

Weight

With aluminum enclosure and connectors: 325g

On request, allocortech can produce a unit with composite enclosure and connectors for ~40g of weight reduction.

Environmental

The below specifications are design goals, and have not been fully qualified through environmental qualification testing.

Grounding and Bonding

As standard, a 3.3nF Y capacitor and 1MΩ drain resistor couple the Clio power ground to its enclosure for EMI rejection through shields and the aircraft bonding network. These values can be customized on request.

The coupling components provide a nominal 350V isolation between chassis and any pin.

To avoid excessive static charge buildup between chassis and the power grounds during flight, it is recommended that a low resistance connection bond be provided between the chassis and power supply returns at the aircraft power supply.

Temperature

Operating: -40°C to 70°C.

Storage: -50° to 85°C.

Vibration and Shock

Designed to meet DO-160 Category R.

Pressure

-5k to 40k feet pressure altitude MSL

Humidity and Water Ingress

Units are sealed and conformal coated to withstand condensing humidity and falling water per DO-160 Category W. Units have demonstrated the ability to withstand submerging suggesting an equivalent IP67 rating, further testing would be required to verify.

Corrosion

Chromate passivized aluminum enclosure, 168+ hours salt fog resistance. Note that the use of chromate does not make units RoHS compliant.
Black zinc nickel coated connectors, 500+ hours salt fog resistance.

Supplemental Components

Customers interested in allocortech providing development harnesses for initial Clio Series B bring up and test, may request quotes for the following Trunk and Distribution harnesses. These are not required and customers may fabricate their own harnesses using the connector details previously outlined in this document.

Trunk Development Harness

This harness provides connections to all J1 pins and terminates using the following connectors:

- Red/Black Banana Jacks (Ponoma 1325-0/2) - VIN, FTS and related shields
- Molex (0050579402 70066-0176) - CAN/RS485 and related shields
- RJ45 (44915-0001) - Ethernet and related shield

Allocortech PN: 130-0080-001

Distribution Test Harness

This harness provides connections to all J1 pins and terminates using the following connectors:

- Molex (43650-0200) - Load Channels
- Molex (0050579402 70066-0176) - Dist Channels (CAN/RS485) and related Shields
- Molex (50-57-9406) - TTL, GPIO and related shields

Allocortech PN: 130-0081-001

Logic Board

The Clio Series B logic board is available as a stand alone PCBA for customers who may desire to package and connectorize the unit themselves. Contact Allocortech directly for more information.

Part Numbers

Generation

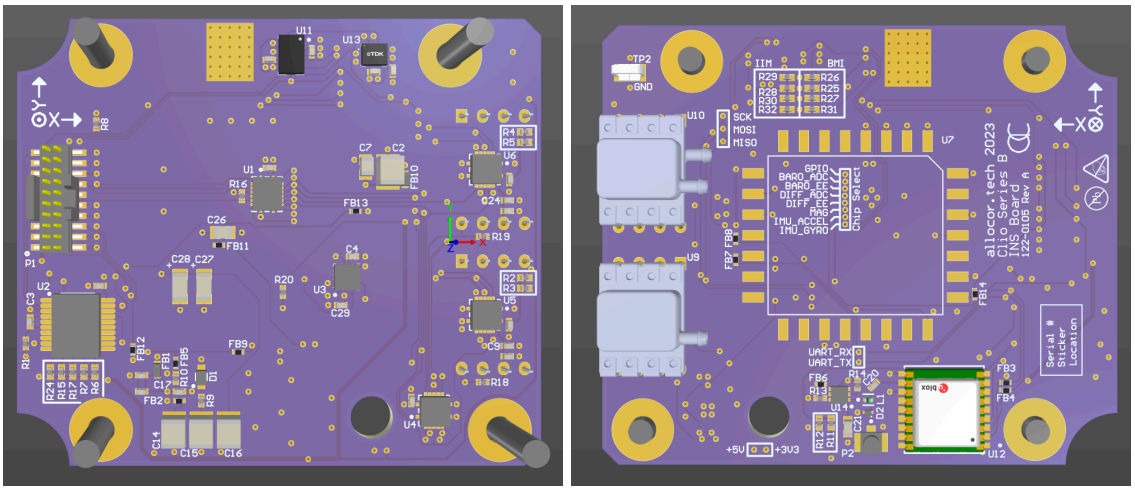
Given the numerous options for customizability, specific part numbers can be generated using the online tool hosted at:

https://www.allocor.tech/tools/product-variants/?product=clio-b-mkv

For additional questions regarding option selection and PN generation contact allocortech directly.

Appendix A - Expansion Board Option

The Inertial Navigation System (INS) Expansion Board is an optional expansion onto the Clio system. The INS board includes an inertial measurement unit (IMU), a magnetometer, a barometric pressure sensor, a differential pressure sensor, and a GNSS (Global Navigation Satellite System). Optionally, a VectorNav VN-300 Inertial Measurement Unit (IMU) and Attitude Heading Reference System (AHRS) can replace the GPS. The VectorNav solution offers dual GNSS ports.



The expansion board connects to the Clio inside the enclosure using a Samtec FTSH-110-01-L-DV-K 20 position header. The expansion board is powered and controlled by the Clio, and because of this, the INS expansion board cannot be operated without being connected to a Clio.

Inertial Measurement Unit (IMU)

Although two IMUs can be placed on the PCB, only one can be used. The option resistors must be configured for either one or the other, and not both.

IMU 1: Bosch BMI088

The BMI088 is an IMU sold by Bosch which includes a 16-bit, three axis accelerometer and a 16-bit, three axis gyroscope. The accelerometer can be configured for a range of +/- 3, 6, 12, or 24g and the gyroscope can be configured for a range of +/- 125, 250, 500, 1000, or 2000 °/s.

IMU 2: InvenSense IIM42652

The IIM42652 is an IMU sold by TDK InvenSense which includes a 16-bit, three axis accelerometer and a 16-bit, three axis gyroscope. The accelerometer can be configured for a range of +/- 2, 4, 8, or 16g and the gyroscope can be configured for a range of +/- 15.625, 31.25, 62.5, 125, 250, 500, 1000, or 2000 °/s.

Magnetometer (Memsic MMC5983)

The MMC5983 is a 3 axis magnetometer sold by Memsic. It has an 18-bit output with a heading accuracy of up to 0.5 degrees. The device has a maximum output data rate of 1000Hz.

Global Navigation Satellite System

The IMU board can optionally socket one of the following GNSS:

- u-blox MAX-M10 series (https://www.u-blox.com/en/product/max-m10-series)
- VectorNav VN-100, VN-200, or VN-300 (https://www.vectornav.com/)

Up to 100mA of 3.3V or 5.0V antenna power can be injected for active antennas.

10 seconds of hold up is provided to the GNSS module.