

allocortech inc.

# Clio Series B Physical ICD

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601-0048-000

Revision G

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<https://allocor.tech>



## Introduction

The allocortech inc. Clio Series B (part number 100-0048) is a communications and power hub intended to bridge between point to point connections and redundant ring networks. The Series B evolved from the Series A by adding more I/O options, and changing processors to focus on performance and safety critical verification activities. In order to maximize flexibility, most communication pair pins can be CAN, RS485 or PWM; and in order to ease harnessing all trunk communications pairs can be daisy chained through to the distribution connector.

The Clio Series B has the following capabilities, although not all can be used at once:

- 4x redundant 12~48VDC 5A power inputs with fault detection and backfeed prevention which can be bussed or split as required to allow for multiple voltage rails.
- 9x 12~48VDC 3.5A individually fused and switched power outputs with electronic circuit breaking.
  - Each output can be configured to turn off during an FTS event using the GPIO controlled embedded in an onboard FPGA.
  - 2 of the 9 outputs may draw from a 3A maximum auxiliary buck switched power supply.
- 2x 10/100 auto MDI-X internally switched ethernet ports.
- 10x CAN FD busses up to 8Mbps.
- 15x half duplex RS-485 UARTs up to 8Mbps with hardware options to tie transceiver into receive or transmit only mode.
- 1x 5V full duplex invertible UART up to 1Mbps.
- 1x RS-232 up to 1Mbps.
- 3x isolated 50V/3A general purpose solid state relay switches.
- 2x isolated 50V/3mA general purpose constant current sink inputs.
- 2x +2.8 -2.5 V differential analog inputs with programmable gain.
- 1x 200mA 5V general purpose supply split across 2 supply pins.
- 400MHz ARM Cortex-M7 MCU.
  - Double precision hardware floating point unit.
  - 2MB on chip flash memory.
  - 1MB RAM.
  - 28MB off chip flash memory connected over QSPI.
- Optional expansion board with 3x SPI chip selects and dedicated full duplex UART.
  - Enclosure and boards are designed to allow an SMA connector and coax to the expansion board.

For more information about what options are available, please refer to the [capability mapping tables](#).



## Scope of this Document

This document covers the mechanical and electrical specifications of the allocortech inc Clio Series B (part number 100-0048 and variants.) The software development interfaces will be covered in other documents.

## Version History

| Revision | Changes   |
|----------|---|
| A        | <ul style="list-style-type: none"><li>● Initial Draft</li></ul>   |
| B        | <ul style="list-style-type: none"><li>● Update GPO max current over temperature</li><li>● Correct Serial table D10 and D11</li><li>● Correct description of J1:c</li><li>● Update GPO max current limit</li></ul>   |
| C        | <ul style="list-style-type: none"><li>● Update J2 image to correctly show pin 25 (previously misidentified as 23)</li></ul>   |
| D        | <ul style="list-style-type: none"><li>● Update Comms naming to match software (all caps)</li></ul>  |
| E        | <ul style="list-style-type: none"><li>● Signal naming updates for hardware/software/reference consistency</li><li>● Added PWM support references</li><li>● Corrected inconsistency in Dist 10 / Dist 11 capabilities</li><li>● Added additional information on GPO/GPI/Expansion implementations</li><li>● Added information about ST provided bootrom</li></ul>  |
| F        | <ul style="list-style-type: none"><li>● Added notes about what load outputs are connected to what power bus</li><li>● Clarified meaning of 1 vs 0 in part encoder table for Loads 7 and 8</li></ul>   |
| G        | <ul style="list-style-type: none"><li>● For ease of harnessing and configuration, show all the I/O (except power) on the trunk and dist connectors in the capability mapping table.</li><li>● Added information about isolated GPI, isolated GPO, and differential analog implementations.</li><li>● Described the Mark IV 1-wire EEPROM</li><li>● Updated the variant selection table to account for GPI pullups</li></ul> |



## List of Abbreviations

|                 |   |
|-----------------|---|
| <b>4W RS485</b> | Four wire, full duplex, differential serial (aka RS422) with RS485 line levels. |
| <b>CAN</b>      | Controller Area Network, serial protocol ISO 11898                              |
| <b>CAN FD</b>   | Controller Area Network with Flexible Data Rate                                 |
| <b>EMI</b>      | Electromagnetic Interference  |
| <b>FPGA</b>     | Field Programmable Gate Array   |
| <b>GND</b>      | Power or Digital Ground, isolated from Chassis Ground                           |
| <b>GPI</b>      | General Purpose Input   |
| <b>GPO</b>      | General Purpose Output  |
| <b>LUT</b>      | Look-Up Table, in an FPGA refers to the smallest logic gate                     |
| <b>MCU</b>      | Microcontroller Unit  |
| <b>PGA</b>      | Programmable Gain Amplifier   |
| <b>PPS</b>      | Pulse per Second Time Synchronization   |
| <b>PWM</b>      | Pulse Width Modulation  |
| <b>QSPI</b>     | Quad SPI, 4 synchronous bidirectional data lines and one clock                  |
| <b>SOA</b>      | Safe Operating Area   |
| <b>SPI</b>      | Serial Peripheral Interface   |
| <b>UART</b>     | Serial Universal Asynchronous Receiver-Transmitter                              |

## References

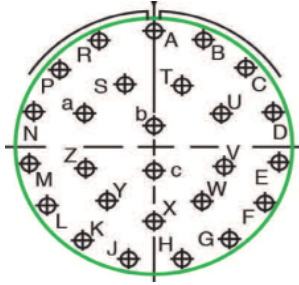
| Reference | Title, Description, Location   |
|-----------|--|
| ST AN2606 | STM32 Bootloader Manual<br><a href="https://www.st.com/resource/en/application_note/cd00167594.pdf">https://www.st.com/resource/en/application_note/cd00167594.pdf</a>   |
| ST AN3155 | USART Protocol Used in the STM32 Bootloader<br><a href="https://www.st.com/resource/en/application_note/cd00264342-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/cd00264342-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf</a> |
| ST AN3154 | CAN Protocol Used in the STM32 Bootloader<br><a href="https://www.st.com/resource/en/application_note/cd00264321-can-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/cd00264321-can-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf</a>       |



# Electrical Interface

## Connector Pinouts

### J1 - Trunk Connector



Face view of receptacle 38999 17-26P N key. 26x size 20 male pins, 5A each.

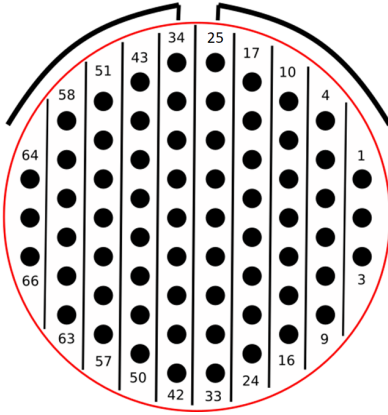
Available in aluminum or composite, with Olive Drab Chromium, Electroless Nickel, or Black Nickel (aluminum only) plating.

Mates with any 38999 tri-start N key compatible 17-26 (E shell) plug with female sockets. Pins usually crimp from AWG 20 thru 24.

| Pin | Name         | Primary Function | Alt. Function    | Notes  |
|-----|--------------|------------------|------------------|--|
| A   | VIN 2 -      | Bus B Return     | -                |  |
| B   | VIN 2 +      | Bus B Supply     | -                | 7A Slow Blow Fuse, 50V Max Continuous  |
| C   | VIN 1 -      | Bus A Return     | -                |  |
| D   | VIN 1 +      | Bus A Supply     | -                | 7A Slow Blow Fuse, 50V Max Continuous  |
| E   | VIN 0 -      | Bus A Return     | -                |  |
| F   | VIN 0 +      | Bus A Supply     | -                | 7A Slow Blow Fuse, 50V Max Continuous  |
| G   | VIN 3 -      | Bus C Return     | -                |  |
| H   | TRUNK_3 -    | RS485_T3 N       | -                | Optional daisy chain to J2:29, J2:30<br>Programmable 120 Ohm termination                 |
| J   | TRUNK_3 +    | RS485_T3 P       | -                |  |
| K   | TRUNK_1 -    | CAN_T1 L         | -                | Optional daisy chain to J2:20, J2:28<br>Programmable 120 Ohm termination                 |
| L   | TRUNK_1 +    | CAN_T1 H         | -                |  |
| M   | Eth 0 RX -   | Ethernet 0       | -                |  |
| N   | Eth 0 RX +   | Ethernet 0       | -                |  |
| P   | Eth 0 TX -   | Ethernet 0       | -                |  |
| R   | Eth 0 TX +   | Ethernet 0       | -                |  |
| S   | Reserved     | -                | -                |  |
| T   | FTS Analog + | 3A Current Loop  | 28V Voltage Loop | In voltage mode, optional daisy chain to J2:46, J2:47                                    |
| U   | FTS Analog - |                  |                  |  |
| V   | TRUNK_4 -    | RS485_T4 N       | -                | Optional daisy chain to J2:46, J2:47<br>Programmable 120 Ohm termination                 |
| W   | TRUNK_4 +    | RS485_T4 P       | -                | Usable as FTS / E-Stop GPIO  |
| X   | TRUNK_2 -    | RS485_T2 N       | -                | Daisy chained to J2:61, J2:66<br>Programmable 120 Ohm termination                        |
| Y   | TRUNK_2 +    | RS485_T2 P       | -                |  |
| Z   | TRUNK_0 -    | CAN_T0 L         | -                | Daisy chained to J2:60, J2:64<br>Programmable 120 Ohm termination                        |
| a   | TRUNK_0 +    | CAN_T0 H         | -                | STM32 CAN Bootloader   |
| b   | Recovery     | MCU Boot Mode    | -                | Short to ground to enter STM32 bootloader mode.<br>Use CAN_T0 or RS485_D10 to load code. |
| c   | VIN 3 +      | Bus C Supply     | -                | 7A Slow Blow Fuse, 50V Max Continuous  |



## J2 - Distribution Connector



Face view of receptacle 38999 19-35S N key. 66x size 22D female sockets, 3.5A each.

Available in aluminum or composite, with Olive Drab Chromium, Electroless Nickel, or Black Nickel (aluminum only) plating.

Mates with any 38999 tri-start N key compatible 19-35 (F shell) plug with male pins. Pins usually crimp from AWG 22 thru 28.

| Pin | Name      | Primary Function | Alt. Function | Notes   |
|-----|-----------|------------------|---------------|---|
| 1   | DIST_6 +  | RS485_D6 P       | CAN_D6 H      |   |
| 2   | DIST_5 -  | RS485_D5 N       | CAN_D5 L      |   |
| 3   | DIST_5 +  | RS485_D5 P       | CAN_D5 H      |   |
| 4   | DIST_7 +  | RS485_D7 P       | CAN_D7 H      |   |
| 5   | DIST_6 -  | RS485_D6 N       | CAN_D L       |   |
| 6   | DIST_11 - | RS485_D11 N      | RS232_D11 RX  |   |
| 7   | DIST_11 + | RS485_D11 P      | RS232_D11 TX  |   |
| 8   | DIST_4 -  | RS485_D4 N       | CAN_D4 L      |   |
| 9   | DIST_4 +  | RS485_D4 P       | CAN_D4 H      |   |
| 10  | DIST_7 -  | RS485_D7 N       | CAN_D7 L      |   |
| 11  | LOAD_6 +  | LOAD_6 Supply    | -             | Power bus B   |
| 12  | GPI_1 +   | GPI_1 High       | -             |   |
| 13  | GPI_1 -   | GPI_1 Low        | GND           | Factory option for GND tie  |
| 14  | TTL/5V    | TTL_D10 TX       | 200mA 5V      | STM32 UART bootloader 5V TTL TX, invertible<br>Power shared with J2:31<br>Return to pin J2:22 |
| 15  | DIST_10 + | TTL_D10 RX       | RS485_D10 P   |   |
| 16  | DIST_3 -  | RS485_D3 N       | CAN_D3 L      |   |
| 17  | DIST_9 +  | RS485_D9 P       | -             |   |
| 18  | GND       | LOAD_6 Return    | -             |   |
| 19  | GPI_0 -   | GPI_0 Low        | GND           | Factory option for GND tie  |
| 20  | Chain C - | CAN_T1 L         | Analog 0 -    |   |
| 21  | GND       | TTL/5V Return    | -             | Has TVS Diode to TTL_D10  |
| 22  | DIST_10 - | 2.5V TTL Bias    | RS485_D10 N   | Leave floating when using TTL_D10   |
| 23  | LOAD_8 +  | LOAD_8 Supply    | -             | Power bus C   |
| 24  | DIST_3 +  | RS485_D3 P       | CAN_D3 H      |   |
| 25  | DIST_9 -  | RS485_D9 N       | -             |   |
| 26  | LOAD_5 +  | LOAD_5 Supply    | -             | Power bus B   |
| 27  | GPI_0 +   | GPI_0 High       | -             |   |
| 28  | Chain C + | CAN_T1 H         | Analog 0 +    |   |
| 29  | Chain B + | RS485_T3 P       | Analog 1 +    |   |
| 30  | Chain B - | RS485_T3 N       | Analog 1 -    |   |



| Pin | Name      | Primary Function | Alt. Function | Notes  |
|-----|-----------|------------------|---------------|--|
| 31  | 5V        | 200mA 5V         | -             | Power shared with P2:14                                    |
| 32  | GND       | LOAD_8 Return    | -             |  |
| 33  | DIST_2 -  | RS485_D2 N       | CAN_D2 L      |  |
| 34  | DIST_0    | CAN_D0 H         | Eth 1 RX -    | Reversed polarity between primary and secondary functions. |
| 35  | GND       | LOAD_4 Return    | -             |  |
| 36  | GND       | LOAD_5 Return    | -             |  |
| 37  | GND       | 5V Return        | -             | Notional return for P2:31                                  |
| 38  | GND       | LOAD_2 Return    | -             |  |
| 39  | GND       | LOAD_1 Return    | -             |  |
| 40  | GND       | LOAD_7 Return    | -             |  |
| 41  | LOAD_7 +  | LOAD_7 Supply    | -             | Power bus C  |
| 42  | DIST_2 +  | RS485_D2 P       | CAN_D2 H      |  |
| 43  | DIST_0    | CAN_D0 L         | Eth 1 RX +    | Reversed polarity between primary and secondary functions. |
| 44  | LOAD_4 +  | LOAD_4 Supply    | -             | Power bus B  |
| 45  | GND       | LOAD_3 Return    | -             |  |
| 46  | Chain A + | RS485_T4 P       | FTS Analog +  |  |
| 47  | Chain A - | RS485_T4 N       | FTS Analog -  |  |
| 48  | GND       | LOAD_0 Return    | -             |  |
| 49  | LOAD_1 +  | LOAD_1 Supply    | -             | Power bus A  |
| 50  | DIST_1 -  | RS485_D1 N       | CAN_D1 L      |  |
| 51  | DIST_8    | RS485_D8 P       | Eth 1 TX -    | Reversed polarity between primary and secondary functions. |
| 52  | GPO 0 -   | GPO_0 Return     | GND           | Factory option for GND tie                                 |
| 53  | GPO 0 +   | GPO_0 Input      | -             |  |
| 54  | GPO 1 -   | GPO_1 Return     | GND           | Factory option for GND tie                                 |
| 55  | GPO 1 +   | GPO_1 Input      | -             |  |
| 56  | GPO 2 +   | GPO_2 Input      | -             |  |
| 57  | DIST_1 +  | RS485_D1 P       | CAN_D1 H      |  |
| 58  | DIST_8    | RS485_D8 N       | Eth 1 TX +    | Reversed polarity between primary and secondary functions. |
| 59  | LOAD_3 +  | LOAD_3 Supply    | -             | Power bus A  |
| 60  | TRUNK_0 + | CAN_T0 H         | -             | Daisy chained from Trunk connector                         |
| 61  | TRUNK_2 + | RS485_T2 P       | -             | Daisy chained from Trunk connector                         |
| 62  | GPO 2 -   | GPO_2 Return     | GND           | Factory option for GND tie                                 |
| 63  | LOAD_0 +  | LOAD_0 Supply    | -             | Power bus A  |
| 64  | TRUNK_0 - | CAN_T0 L         | -             | Daisy chained from Trunk connector                         |
| 65  | LOAD_2 +  | LOAD_2 Supply    | -             | Power bus A  |
| 66  | TRUNK_2 - | RS485_T2 N       | -             | Daisy chained from Trunk connector                         |

### J3 - Expansion Connector

As a factory option for the purposes of expansion, both the Clio Series B enclosure and PCB assembly have been designed to accommodate a single male SMA connector or pressure barb. A standard enclosure will not have the hole drilled, nor will it have the marking text. Contact allocortech about expansion board options.



## Chassis Bond Stud

For enhanced bonding between the Clio Series B and vehicle chassis, a M3 bonding stud can be installed in the baseplate with a countersunk M3 screw with the intent of allowing a low resistance connection.

## Electrical Characteristics

### Absolute Maximums

| Parameter  | Min  | Max | Unit |
|--|------|-----|------|
| Input Voltage on VIN 0-3                                   |      | 60  | V    |
| Total Current through Single VIN                           |      | 10  | A    |
| Total Combined Current through all VIN                     |      | 20  | A    |
| Output Current to LOAD 0-8                                 |      | 4   | A    |
| GPI Voltage between +/-                                    | -8.5 | 60  | V    |
| GPI Isolation to GND                                       |      | 60  | V    |
| GPO Voltage between +/-                                    |      | 60  | V    |
| GPO Current between +/- (AC or DC) <sup>1</sup> @ 25°C     |      | 3   | A    |
| GPO Isolation to GND                                       |      | 60  | V    |
| RS485 / CAN / PWM Common Mode (Continuous)                 | -25  | 25  | V    |
| RS485 / CAN / PWM Common Mode (Transient)                  | -58  | 58  | V    |
| RS485 / CAN / PWM Differential (Continuous)                | -5   | 10  | V    |
| RS485 / CAN / PWM Differential (Transient)                 | -17  | 17  | V    |
| FTS Analog Differential Voltage (Voltage Mode, Continuous) | -13  | 60  | V    |
| FTS Analog Current (Current Mode, Continuous)              |      | 5   | A    |
| Auxiliary Analog Inputs to GND (Continuous)                | -16  | 16  | V    |

## Power Topology

The Clio series B can provide up to 20A continuous power to nine 3.5A outputs at bus voltage and two 5V (200mA combined max) outputs. Power is broken into three power buses (A, B, and C) which can operate independently or be tied together. The A bus, in addition to powering the switched loads, also powers the processor, transceivers, and 3A auxiliary buck switched mode power supply.

<sup>1</sup> The full safe operating area (SOA) curve for the GPO optoisolator is given in the [Isolated Outputs](#) section.





The four power inputs on the Clio are protected by slow blow 10A fuses, transient protection diodes, and an ideal diode preventing power from flowing backwards. Each input monitors the supply voltage and the return current. This monitoring allows detection of blown fuses, broken wires, and potentially ground loops.

The nine 3.5A outputs are current-monitored by the MCU and are all individually fused with fast blow 5A fuses. It is expected that power supplied to the remote device is returned to the Clio on the designated pin. Failure to do so may trip the Clio's ground fault detection feature. Soft start functionality is expected to be present on the remote load if a current draw above 3.5A occurs at startup.

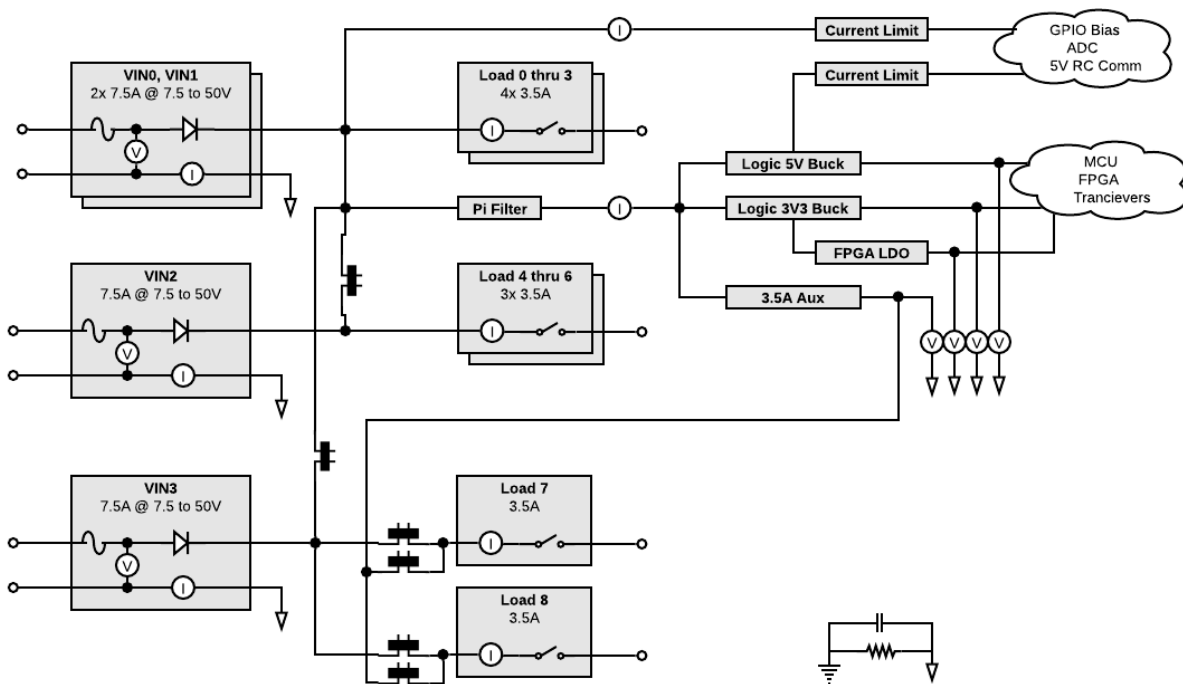
If used, the auxiliary power supply can regulate from within a volt of the A bus voltage (trim network is 28V max on Mark I, II and III; 48V max on Mark IV+) down to 5V in 10mV steps and can supply up to 3A of current.

The Clio nominally operates from 12 to 36VDC (50VDC maximum), with a factory option to shift the range up from 24 to 48VDC nominal.

The worst case power draw for the internal logic is estimated to be no more than 15W if all but one transceiver is operating nominally and one transceiver is driving a shorted bus.

The Clio is not rated for any specific hold up time in the case of complete power loss.

The Clio chassis is capacitively and resistively (1 Mega Ohm) coupled to power return for EMI and voltage transients, it is expected that the power sources have a low resistance connection between chassis and return.





## Capability Mapping

There are several categories of serial communications present on the Clio. Any interface conceptually designed to be used as a safety critical trunking interface is dedicated, brought directly to the MCU, and is chainable. All other communications go through some form of external peripheral controller and are usually overlaid with other compatible communications busses so that many protocols can be served by a single set of hardware.

| Pair #* | CAN | 485  | 232  | 5V TTL   | PWM  | Eth   | ADC  | Daisy Chain | Note                               |
|---------|-----|------|------|----------|------|-------|------|-------------|------------------------------------|
| TRUNK_0 | MCU |      |      |          |      |       |      | Always      | STM32 bootloader                   |
| TRUNK_1 | MCU |      |      |          |      |       |      | C           |                                    |
| TRUNK_2 |     | MCU  |      |          |      |       |      | Always      |                                    |
| TRUNK_3 |     | MCU  |      |          |      |       |      | B           |                                    |
| TRUNK_4 |     | FPGA |      |          | Y    |       |      | A           | FTS GPIO                           |
| TRUNK_5 |     |      |      |          |      |       | FPGA | A           | FTS Analog                         |
| TRUNK_6 |     |      |      |          |      | Eth 0 |      |             |                                    |
| TRUNK_7 |     |      |      |          |      | Eth 0 |      |             |                                    |
| DIST_0  | SPI |      |      |          |      | Eth 1 |      |             |                                    |
| DIST_1  | SPI | FPGA |      |          | FPGA |       |      |             |                                    |
| DIST_2  | SPI | FPGA |      |          | FPGA |       |      |             |                                    |
| DIST_3  | SPI | FPGA |      |          | FPGA |       |      |             |                                    |
| DIST_4  | SPI | FPGA |      |          | FPGA |       |      |             |                                    |
| DIST_5  | SPI | FPGA |      |          | FPGA |       |      |             |                                    |
| DIST_6  | SPI | FPGA |      |          | FPGA |       |      |             |                                    |
| DIST_7  | SPI | FPGA |      |          | FPGA |       |      |             |                                    |
| DIST_8  |     | FPGA |      |          | FPGA | Eth 1 |      |             |                                    |
| DIST_9  |     | FPGA |      |          | FPGA |       |      |             |                                    |
| DIST_10 |     | MCU  |      | MCU / RX |      |       |      |             | STM32 bootloader<br>No termination |
| DIST_11 |     | FPGA | FPGA |          | FPGA |       |      |             |                                    |
| Aux5V_0 |     |      |      | MCU / TX |      |       |      |             | DIST_10 or always on               |
| Aux5V_1 |     |      |      |          |      |       |      |             | Always on                          |
| GPI_0   |     |      |      |          | FPGA |       |      |             | PWM Capture or arbitrary in        |
| GPI_1   |     |      |      |          | FPGA |       |      |             |                                    |
| GPO_0   |     |      |      |          | FPGA |       |      |             | PWM Generation or arbitrary output |
| GPO_1   |     |      |      |          | FPGA |       |      |             |                                    |
| GPO_2   |     |      |      |          | FPGA |       |      |             |                                    |

\* Note: Pair# here match software registry port names



## Daisy Chaining of Signals

The Clio carries several signal pairs from the J1 Trunk connector to the J2 Distribution connector for the purpose of removing the need for harness breaks when chaining several devices together on the communications trunks. Restated, the Clio itself can act as an inline harness break or signal tee. Of the 5 signal pairs that chain through the Clio, 2 of them (T0 CAN and T2 RS485) are fixed while the other 3 are factory selectable for which function they perform.

| J2 Name | CAN     | 485     | ADC        |
|---------|---------|---------|------------|
| TRUNK_0 | TRUNK_0 |         |            |
| TRUNK_2 |         | TRUNK_2 |            |
| Chain A |         | TRUNK_4 | FTS Analog |
| Chain B |         | TRUNK_3 | Analog_1   |
| Chain C | TRUNK_1 |         | Analog_0   |

Selection of what signals are present on each chain is a factory option.

The FTS can only be daisy chained in voltage mode.

## CAN

The Clio Series B can expose up to ten CAN-FD busses capable of operation up to 8Mbps. Two of the buses are native to the MCU. The remaining eight CAN buses are produced by SPI CAN controllers attached in pairs to dedicated SPI controllers. The two MCU connected CAN busses are connected to the trunk connector and are optionally daisy chainable to the distribution connector.

All CAN busses use Microchip MCP2542 transceivers which feature 13kV ESD protection (IEC 61000-4-2) and +/- 58VDC common mode protection. Trunk CAN lines are further protected with a common mode choke and have programmable, or optionally factory fixed, 120 Ohm termination. Distribution CAN lines have factory installed 120 Ohm termination resistors.

## UARTs

### Trunk RS-485

The Clio Series B has three half duplex RS-485 pairs present on the trunk connector, all with hardware duplex control and capable of operation up to 8Mbps. Two of these pairs are controlled by the MCU and are powered with 5V for maximum differential voltage swing. The third is controlled by the FPGA, and is powered from 3.3V. All transceivers are fault tolerant to differential shorts, have high common mode range, are further protected with common mode chokes and all have programmable, or optionally factory fixed, 120 Ohm termination.

If required, all trunk transceivers can be factory modified to operate in receive only mode.

In the first hardware production, a TI THVD2450 was used. In future production runs, this or an equivalent part will be sourced.



## Distribution RS-485

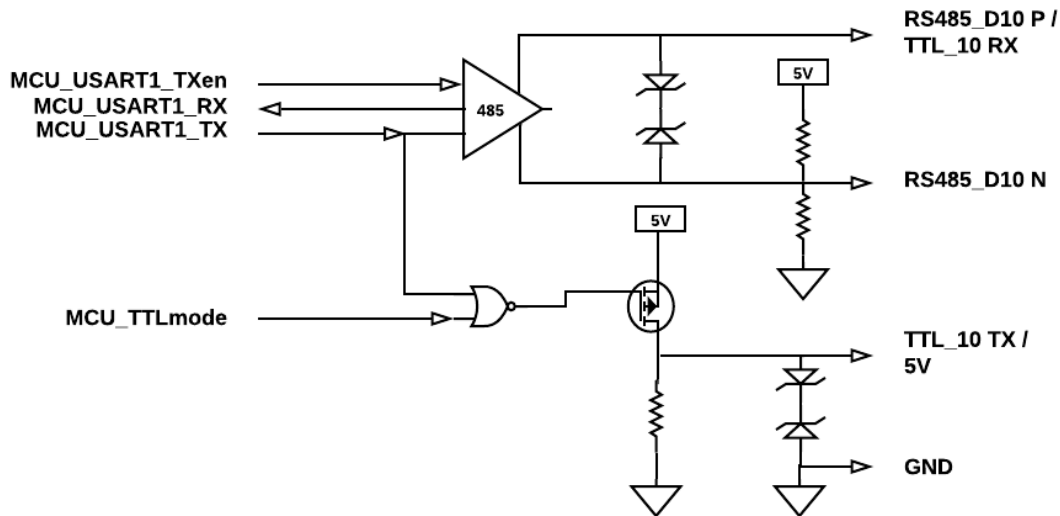
There are eleven half duplex RS-485 pairs present on the distribution connector, all with hardware duplex control and capable of operation up to 8Mbps. Ten of these eleven are connected to the FPGA. The eleventh UART is the STM32 bootloader UART which is connected to the MCU. All transceivers on the distribution are powered from 3.3V, are fault tolerant to differential shorts, have high common mode range, and have fixed termination options, except for the RS-232 capable pair which has programmable termination, and the TTL capable pair which has no termination.

In the first hardware production, a Maxim MAX14775 was used. In future production runs, this or an equivalent part will be sourced.

## Distribution RS-232 (Dist 11)

Using an LTC2873, the Clio Series B is able to offer a combined RS-232 and RS-485 port. This device turns the differential pair into TX and RX as well as offering a programmable resistor in RS-485 mode.

## Distribution 5V TTL (Dist 10)



A single 5V TTL UART is provided for devices such as RC receivers and other low voltage sensors that have short communication runs and are not safety critical. This UART operates by weakly biasing the negative side of a RS485 transceiver at 2.5V. The RX is then expected to exceed 2.5V by at least 200mV; notionally from GND to +5V but GND to +3.3V is also acceptable. The transmit side is operated by using a high side FET and strong pull down from 5V to GND. This port is software invertible, meaning that mark and space can be either 5V or GND.

When this port is operating in TTL mode, the maximum baud rate is 56kbps. Improvements to the biasing network can be made to improve the performance of this port up to 115.2kbps at the expense of additional power draw when operating in 5V supply mode.



## Ethernet

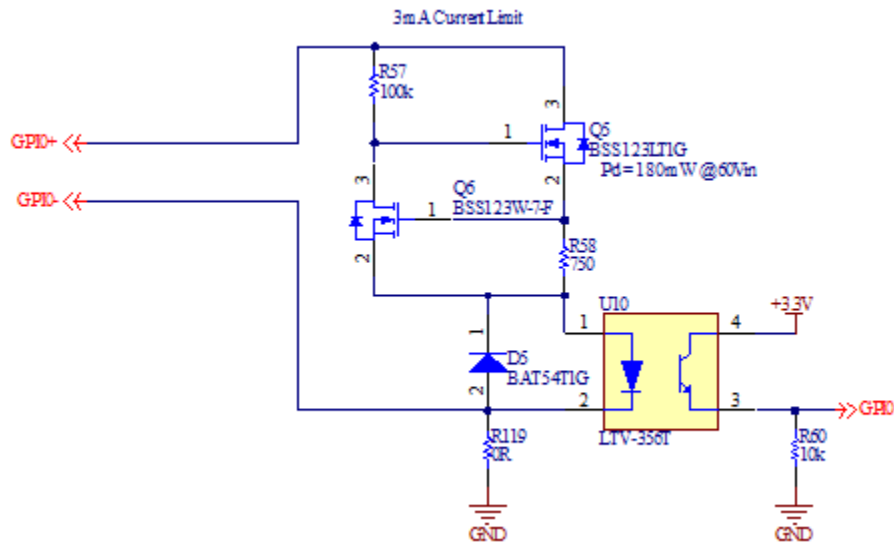
Clio series B offers up to two external 10/00 Auto-MDIX magnetically coupled ethernet ports. These ports are controlled by an internal three port managed switch with the third port directly attached to the native MCU media access controller.

## Discrete Digital Inputs / Outputs

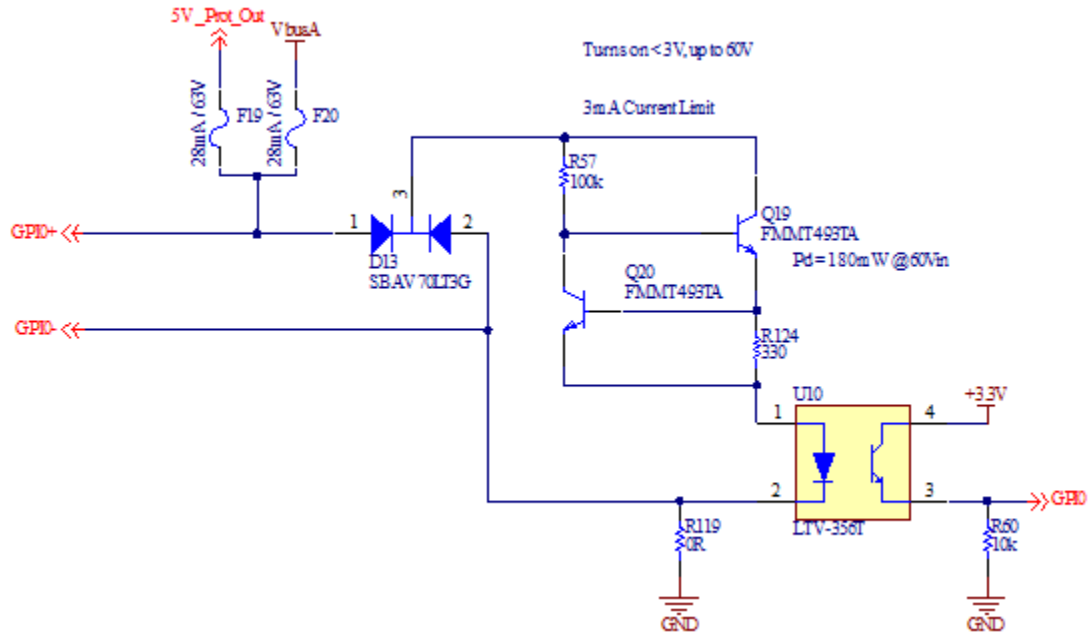
### Isolated Inputs

Provided on the J2 “Distribution” connector are 2 isolated two port inputs. These are approximately 3mA constant current sinks that have a guaranteed turn off below 1.6V and a guaranteed turn on at or above 3.3V. These voltages are referenced to the Low side return. Logic High can be up to 50V relative to Low. Note that High and Low can not exceed 50V referenced from the Clio power return.

If the device connecting to the Clio does not provide a logic reference, connect Low to the remote device's power return at the remote location. If sufficient signal margin is available with respect to ground differences between the Clio and the remote driver, a factory option to tie the Low side to GND inside the enclosure is available.



Isolated GPI on Mark I and II



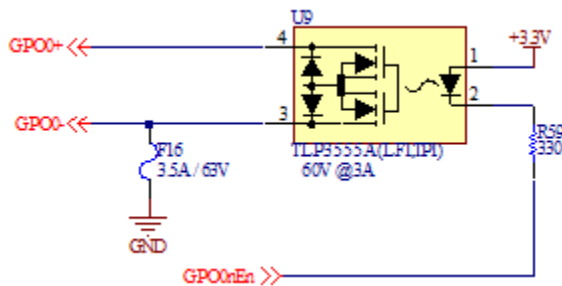
Isolated GPI on Mark III onwards



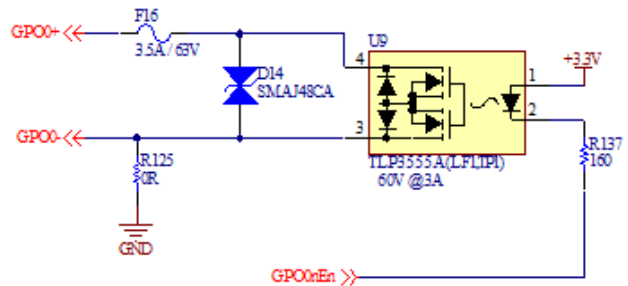
## Isolated Outputs

Provided on the J2 “Distribution” connector are 3 isolated relay connections. These can handle up to 50V relative to Clio power return and 3A of AC or DC current. As a factory option, one leg of each GPO may be tied to the internal power ground.

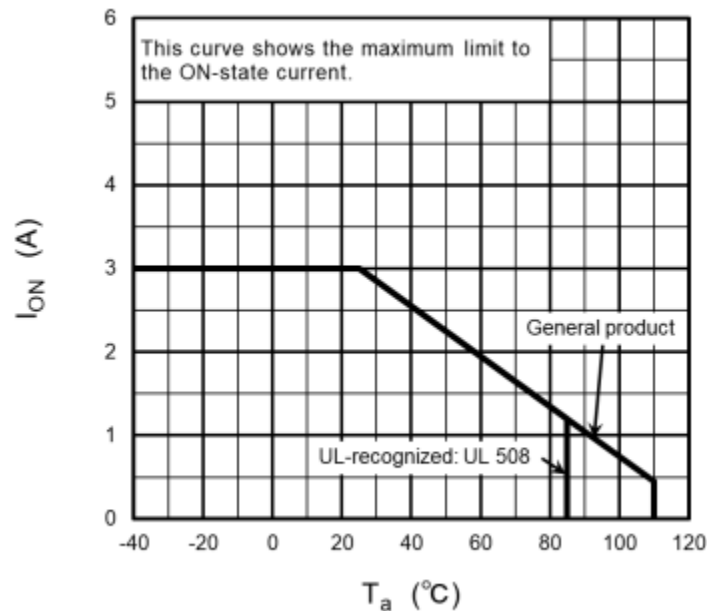
These outputs must be derated for the operating temperature. At the peak operating temperature of the Clio (70°C) the derated current limit is 1.5A.



Isolated GPO on Mark I and II



Isolated GPO on Mark III onwards



Safe Operating Area of TLP3555A Optoisolator



## UARTs as Differential GPIO

All UARTs connected to the FPGA can be repurposed as differential GPIO using RS485 signal levels in software. If configured as an output; the output state when the FTS is triggered is software configurable. UARTs as PWM Outputs

All UARTs connected to the FPGA can be repurposed as pulse width modulated outputs with 16 bit output/compare registers off a 64MHz clock with a 16 bit integer divider. The output state when the FTS is triggered is software configurable.

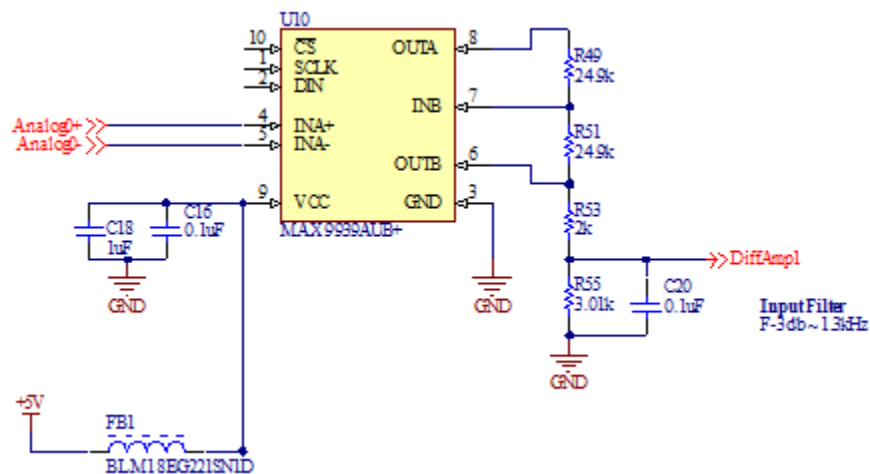
Additional functionality such as PWM capture, or specialty protocols that overlay communications channels on top of the PWM signal are available on request with specialized FPGA firmware builds.

## Differential Analog Inputs

Provided on the J2 “Distribution” connector are 2 differential analog inputs. These are -2.5V to +2.8V inputs sampled with a 16 bit ADC and have a 50Hz low pass filter applied. There is a programmable gain stage between the input and ADC which ranges from 0.2 to 157 V/V.

If needed, the analog source can be powered with an internally generated 5V source which is shared with the remote control UART. If the combined load on this supply exceeds 200mA the supply will enter a continuous retry mode.

Note that the inputs cannot go below -16V or above +16V referenced to “5V Return”, aka GND. No other protection is applied.

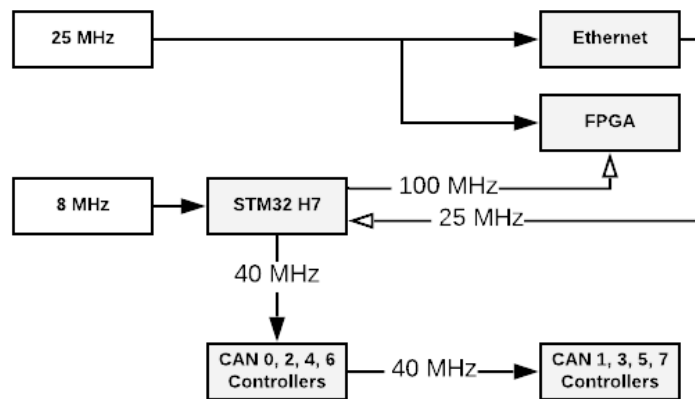
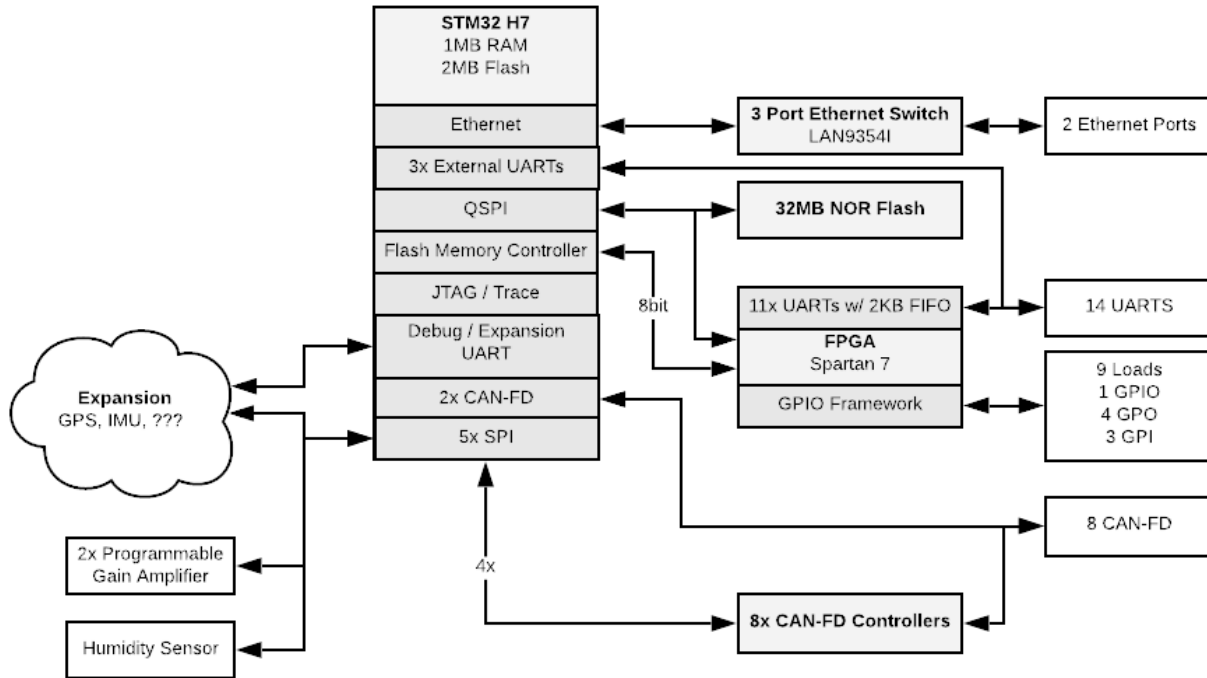


**SPI Controlled PGA Network for Differential Analog**





# Compute Complex





## MCU

A mixture of STM32H753 and STM32H743 processors have been used in the various production runs of the Clio Series B due to parts availability issues. If hardware accelerated cryptography (H753) is desired, contact Allocortech to ensure the shipped product is compliant.

The STM32H7x3 series of MCU are capable of operating up to 400MHz and have 2MB of flash and 1MB of RAM.

## FPGA

Attached to the STM32H7 via 8-bit parallel bus is a Xilinx Spartan 7 with at least 25k LUTs. This FPGA is used to control the distribution UARTs, load channels, GPIO, and flight termination analog signal.

Although the FPGA is not capable of offloading general purpose calculations from the MCU due to the bandwidth of the parallel bus, it is able to offload communications packet processing if desired.

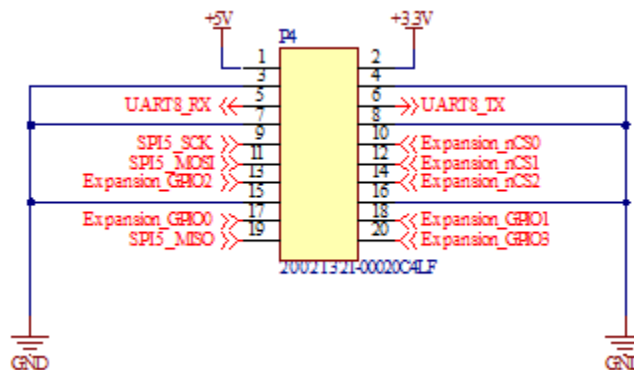
In future revisions of the product, the FPGA may also be responsible for distribution CAN instead of using the MCP2518FD SPI controller.

## NOR Flash / QSPI

Attached to both the processor and FPGA via QSPI is a 32MB NOR Flash. The first 4MB of this flash is dedicated to the FPGA firmware, but the remaining 28MB are available to the user. The QSPI flash is mapped into the MCU address space for cached and prefetch capable read operations.

## Expansion Connector

Clio Series B provides a user expansion header on the bottom side of the logic board. This header exposes a dedicated SPI bus with 7 GPIO capable of being chip select or interrupt lines and a full duplex UART. Power is provided at 5 and 3.3V. For further information contact allocortech.





## Status LED

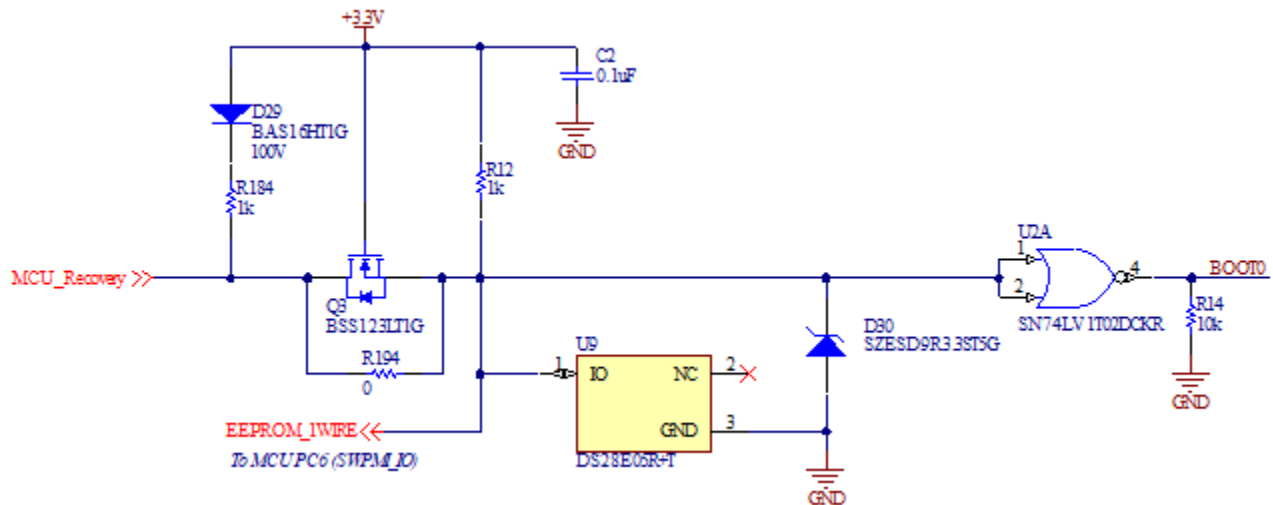
A tri-color daylight-visible status LED is provided, exposed through a light pipe on the top of the enclosure, for user specified informational or debugging purposes.

## Bootloading and Vehicle Personality (1-wire EEPROM)

STMicroelectronics provides the STM32H7 with a serial bootrom, accessible on boot if the Recovery pin (J1:b) is shorted to ground. When the processor is in this mode, communication with the bootrom is possible over Dist 10 (with either RS-485 or TTL) or Trunk 0 (CAN.) See ST AN2606, ST AN3155, and ST AN3154 for further information about interacting with the bootrom.

With the allocortech reference booty bootloader, or a customer supplied bootloader, loading of the MCU internal flash and the FPGA firmware to the QSPI flash is possible over any UART, CAN, or Ethernet connection.

From Mark IV onwards, also attached to the MCU recovery pin is a 112 byte 1-wire EEPROM which allocortech uses to store device revision information and small amounts of configuration. Additional 1-wire devices can be chained in the harness to store end user information as desired.



Recovery and 1-Wire EEPROM Network

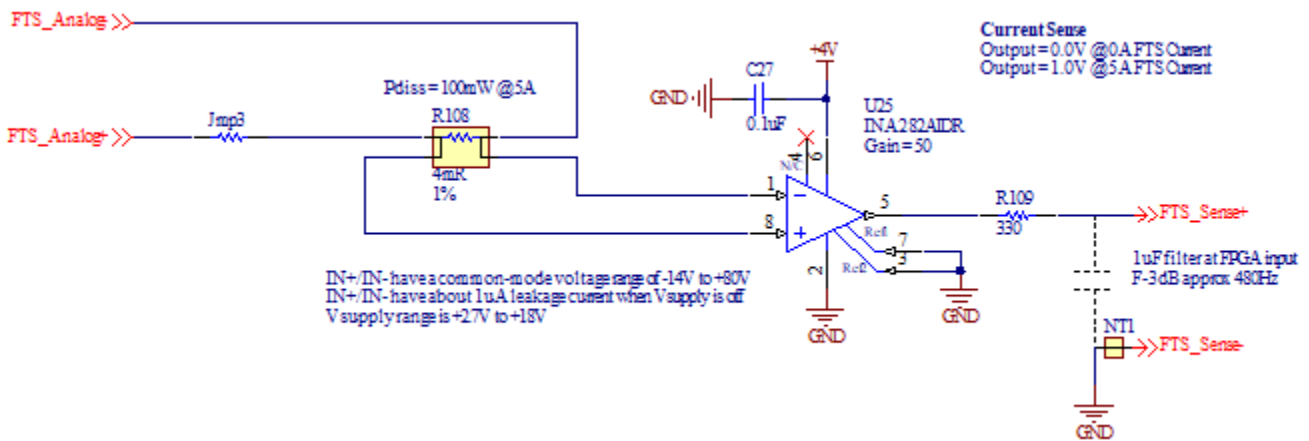


# Safety Critical Considerations

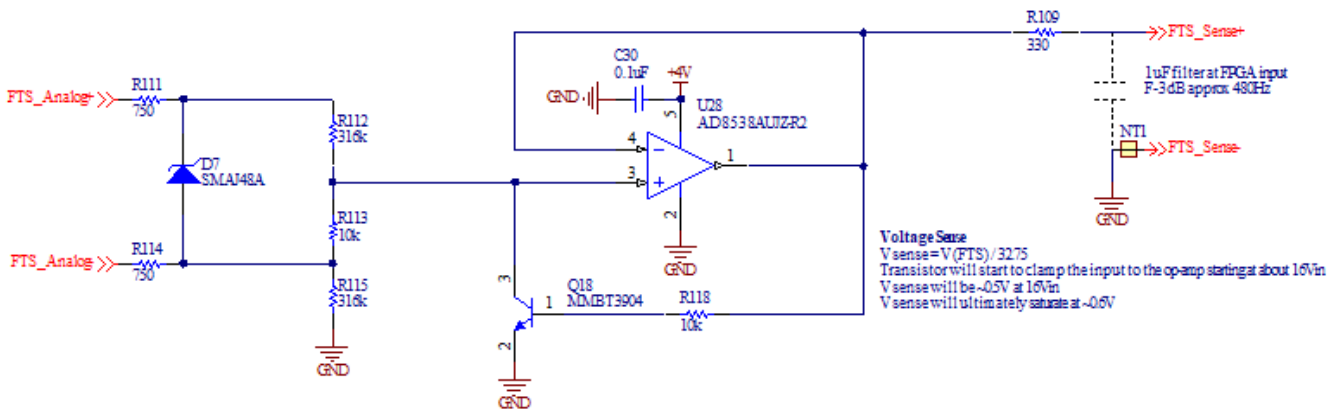
## Flight Termination System / E-Stop Override

Provided on the J1 “Trunk” connector is an analog input which feeds the FPGA XADC. This analog input is factory selectable as either a current sense or voltage sense input. Notionally this analog input is used as a signal to the FPGA to set all load and GPO signals to a software selectable state, but can be repurposed by the user as desired. When operated as an FTS/e-stop, once configured the operation is independent of MCU operation.

If this input is unused, the pins should be left floating at the connector.



**FTS/E-Stop Current Sense**



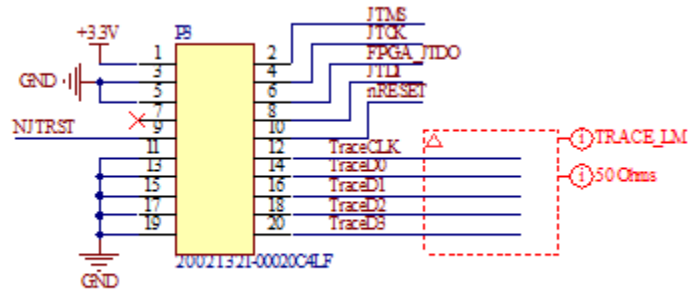
**FTS/E-Stop Voltage Sense**



## MCU Code Coverage

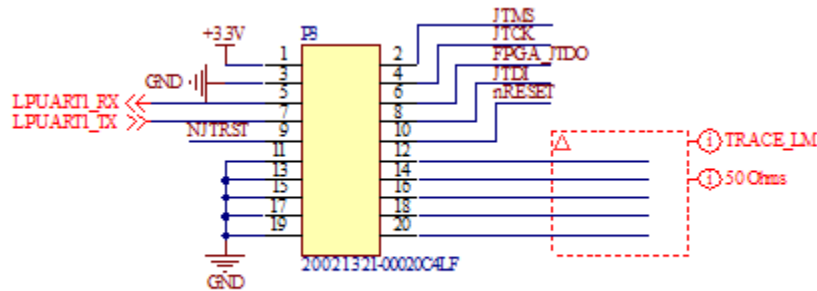
For the purposes of code coverage and on-target debugging, a 4-bit ARM Trace and JTAG connector is present. The JTAG chain includes the FPGA. The pinout chosen is compatible with common trace capable debuggers like those provided by Lauterbach, but adapters can easily be made if required.

Allocortech produces a JTAG adapter board for general purpose embedded debugging, please contact allocortech for more information about part number 120-0061.



*MillMax 852-10-020-10-001000 is a suitable Molex Molex adapter*

**Trace Connector (Mark I thru III)**



*MillMax 852-10-020-10-001000 is a suitable Molex Molex adapter*

**Trace Connector (Mark IV onwards)**

For use with non-trace capable debuggers, allocortech has produced a common adapter board for the 10-pin ST Link V2, 14-pin STLink V3 (including the UART), 6-pin Digilent JTAG 2, and other common debuggers. Users should contact allocortech for more information.



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## Hardware in the Loop Emulation

As a special order factory option, the Clio may be fitted with features to facilitate Hardware in the Loop (HIL) testing. These features include raising the effective sensitivity of all current measurements so that heavy loads may be simulated in a HIL environment without heavy cabling and power supply requirements.

## Health Monitoring

The Clio Series B contains several sensors designed to monitor the health of the unit including thermistors, input power return current monitoring, and voltage monitoring of all rails

## Hardware Monitor

For use in dual-dual or fail stop control schemes, an additional processor can be added to the Clio Series B by use of an interposer circuit board between the logic board and connector boards. Such a processor can be used to monitor all the serial and GPIO signals and override or cut power to the main processor as required.

## Lightning or Other Signal Conditioning / Protection

The Clio Series B is implemented as a logic board containing the MCU, FPGA, and transceivers, and a connector board that performs signal conditioning. If stronger signal or power line protection is required, allocortech can produce and test a custom connector board on request.

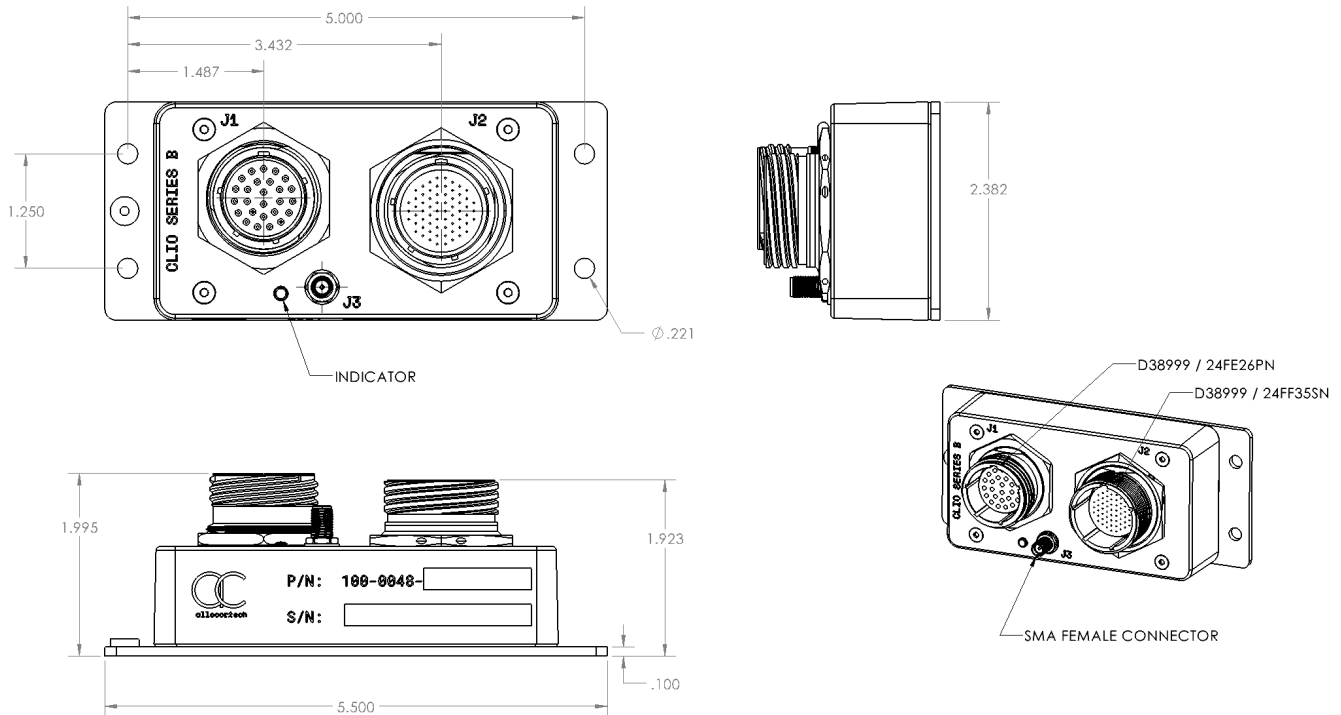


# Mechanical Interface

The Clio Series B is housed in a machined [Hammond Manufacturing 1590B](#) enclosure with the two connectors coming out of the top plate.

## Dimensions

Measurements given in inches.



**NOTE:** The SMA connector shown is optional and would typically only be installed on units with an expansion card.

## Weight

With aluminum enclosure and connectors: 325g

On request, allocortech can produce a unit with composite enclosure and connectors for ~40g of weight reduction.



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## Environmental

The below specifications are design goals, and have not been fully qualified through environmental qualification testing.

### Grounding and Bonding

As standard, a 3.3nF Y capacitor and 1M $\Omega$  drain resistor couple the Clio power ground to its enclosure for EMI rejection through shields and the aircraft bonding network. These values can be customized on request.

The coupling components provide a nominal 350V isolation between chassis and any pin.

To avoid excessive static charge buildup between chassis and the power grounds during flight, it is recommended that a low resistance connection bond be provided between the chassis and power supply returns at the aircraft power supply.

### Temperature

Operating: -40°C to 70°C.

Storage: -40° to 85°C.

### Vibration and Shock

Designed to meet DO-160 Category R.

### Pressure

-5k to 40k feet pressure altitude MSL

### Humidity and Water Ingress

Units are sealed and conformal coated to withstand condensing humidity and falling water per DO-160 Category W.





# Part Numbers

## Generation

To generate a part number suffix for a Clio Series B:

- For rows of options that consist solely of 1 and 0, treat it as a 4 bit hexadecimal number and write the resulting character in the Hex or Option Code column.
- For rows with lettered options, directly write the option letter in the Hex or Option Code column.
- The part number suffix is read down the Hex or Option Code column.

| 100-0048-                                   |   |                    |                       |                       | Hex or Option Code |
|---|---|--------------------|-----------------------|-----------------------|--------------------|
| Tie busses together<br>1(yes) or 0(no)      | Tie bus A to bus B                        | Tie bus A to bus C | Load 8 is Aux (not C) | Load 7 is Aux (not C) |                    |
| Daisy Chain A Option                        | Choose: F(PGA / FTS) or R(S485_T4)        |                    |                       |                       |                    |
| Daisy Chain B Option                        | Choose: R(S485_T3) or A(nalog 1)          |                    |                       |                       |                    |
| Daisy Chain C Option                        | Choose: C(AN_T1) or A(nalog 0)            |                    |                       |                       |                    |
| FTS Option                                  | Choose: C(urrent) or V(oltage)            |                    |                       |                       |                    |
| Trunk Termination                           |   |                    |                       |                       |                    |
| CAN_T0                                      | Choose: A(lways), N(ever), P(rogrammable) |                    |                       |                       |                    |
| CAN_T1                                      | Choose: A(lways), N(ever), P(rogrammable) |                    |                       |                       |                    |
| RS485_T2                                    | Choose: A(lways), N(ever), P(rogrammable) |                    |                       |                       |                    |
| RS485_T3                                    | Choose: A(lways), N(ever), P(rogrammable) |                    |                       |                       |                    |
| RS485_T4                                    | Choose: A(lways), N(ever), P(rogrammable) |                    |                       |                       |                    |
| Trunk RS-485 RX Only<br>1(yes) or 0(no)     | -<br>0                                    | Trunk 4            | Trunk 3               | Trunk 2               |                    |
| 2nd Ethernet                                | Choose: S(erial) or N(etwork)             |                    |                       |                       |                    |
| Distribution Termination<br>1(yes) or 0(no) | Dist 11                                   | -<br>0             | Dist 9                | Dist 8                |                    |
| 1(yes) or 0(no)                             | Dist 7                                    | Dist 6             | Dist 5                | Dist 4                |                    |
| 1(yes) or 0(no)                             | Dist 3                                    | Dist 2             | Dist 1                | Dist 0                |                    |
| Install GPI Ground Tie<br>1(yes) or 0(no)   | -<br>0                                    | -<br>0             | GPI 1                 | GPI 0                 |                    |
| Install GPO Ground Tie<br>1(yes) or 0(no)   | -<br>0                                    | GPO 2              | GPO 1                 | GPO 0                 |                    |
| Expansion Board                             | Choose: A(bsent)                          |                    |                       |                       |                    |
| Install GPI Pull Up<br>1(yes) or 0(no)      | GPI 1: Bus A                              | 5V                 | GPI 0: Bus A          | 5V                    |                    |



## Example

As an example of part number generation, following the rules above:

| 100-0048-                                   |   |                         |                            |                            | Hex or Option Code |
|---|---|-------------------------|----------------------------|----------------------------|--------------------|
| Tie busses together<br>1(yes) or 0(no)      | Tie bus A to bus B<br>0                   | Tie bus A to bus C<br>1 | Load 8 is Aux (not C)<br>0 | Load 7 is Aux (not C)<br>1 | 5                  |
| Daisy Chain A Option                        | Choose: F(PGA / FTS) or R(S485_T4)        |                         |                            |                            | F                  |
| Daisy Chain B Option                        | Choose: R(S485_T3) or A(nalog 1)          |                         |                            |                            | A                  |
| Daisy Chain C Option                        | Choose: C(AN_T1) or A(nalog 0)            |                         |                            |                            | A                  |
| FTS Option                                  | Choose: C(urrent) or V(oltage)            |                         |                            |                            | V                  |
| Trunk Termination<br>CAN_T0                 | Choose: A(lways), N(ever), P(rogrammable) |                         |                            |                            | P                  |
| CAN_T1                                      | Choose: A(lways), N(ever), P(rogrammable) |                         |                            |                            | P                  |
| RS485_T2                                    | Choose: A(lways), N(ever), P(rogrammable) |                         |                            |                            | P                  |
| RS485_T3                                    | Choose: A(lways), N(ever), P(rogrammable) |                         |                            |                            | P                  |
| RS485_T4                                    | Choose: A(lways), N(ever), P(rogrammable) |                         |                            |                            | P                  |
| Trunk RS-485 RX Only<br>1(yes) or 0(no)     | -<br>0                                    | Trunk 4<br>1            | Trunk 3<br>0               | Trunk 2<br>0               | 4                  |
| 2nd Ethernet                                | Choose: S(erial) or N(etwork)             |                         |                            |                            | S                  |
| Distribution Termination<br>1(yes) or 0(no) | Dist 11<br>1                              | -<br>0                  | Dist 9<br>1                | Dist 8<br>0                | A                  |
| 1(yes) or 0(no)                             | Dist 7<br>1                               | Dist 6<br>1             | Dist 5<br>0                | Dist 4<br>1                | D                  |
| 1(yes) or 0(no)                             | Dist 3<br>1                               | Dist 2<br>0             | Dist 1<br>1                | Dist 0<br>1                | B                  |
| Install GPI Ground Tie<br>1(yes) or 0(no)   | -<br>0                                    | -<br>0                  | GPI 1<br>1                 | GPI 0<br>0                 | 2                  |
| Install GPO Ground Tie<br>1(yes) or 0(no)   | -<br>0                                    | GPO 2<br>1              | GPO 1<br>1                 | GPO 0<br>0                 | 6                  |
| Expansion Board                             | Choose: A(bsent)                          |                         |                            |                            | A                  |
| Install GPI Pull Up<br>1(yes) or 0(no)      | GPI 1: Bus A<br>1                         | 5V<br>0                 | GPI 0: Bus A<br>0          | 5V<br>1                    | 9                  |

Yields a final part number of 100-0048-5FAAVPPPPP4SADB26A9

This table is also available as a spreadsheet (601-0048-001) downloadable from our website under the documentation tab at <https://www.allocor.tech/products/clio-series-b/>



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