6EZ

SiC POLISHER

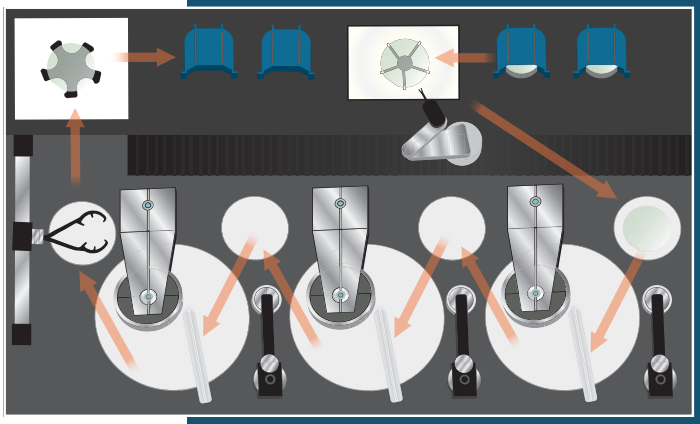
The **6EZ** makes **SiC** polish **EZ!**

KEY FEATURES:

- Fully-automated, cassette-to- cassette handling
- Single wafer processing for excellent wafer-to-wafer control
- Single-side and two-sided polish
- Three tables with dedicated carriers, pad conditioners, and pad cleaners
- Acid-resistant components
- OCR (optional)
- State-of-the-art control architecture and Windows-based operating system
- Two standard slurry delivery lines, optional third slurry line available
- Factory host communication (optional)
- SEMI S2, S8, and CE certified
- 50-wafer processing without operator intervention
- Integrated post-polish clean

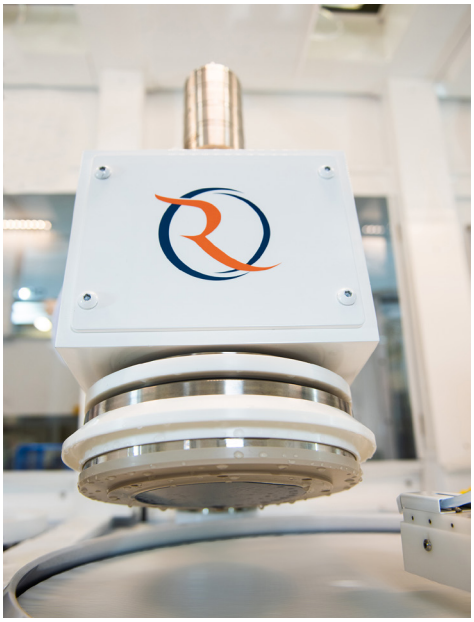
It's no secret that SiC is a hard material to process. We understand the challenges of working with SiC and we have applied our knowledge of SiC grinding, prime wafer polishing, and CMP technology to develop a unique solution that truly makes polishing SiC easy.

We are pleased to introduce you to the **6EZ**, the world's first fully-automated, single wafer, dry-in-dry-out polisher designed specifically for SiC.



POLISH MODULE WITH DEDICATED HARDWARE

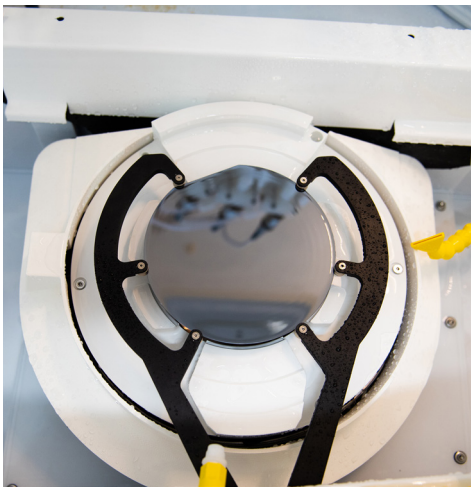
The 6EZ polish section consists of three polish tables, three spindles, and an integrated post-polish cleaning module. Each table comes standard with a dedicated spindle, carrier, pad conditioner and high-pressure spray bar (pad cleaner), which provides the best possible wafer-to-wafer process control. In addition, all tables can be configured with up to three slurries (optional).



INTEGRATED CLEANING

Extra attention has been given to keep the wafers and the polisher clean by integrating wet transfer stations, sprays, rinses and a separate post-polish wafer cleaning module.

Wafers are kept wet in between polish steps. Every wafer is run through a post-polish cleaning for the removal of slurry particles after the final polish and returned to the same cassette and slot at the completion of the polish sequence. The wafers are then ready for a pre-Epi clean.



CLEANROOM READY

HEPA filtration and a cleanroom compatible EFEM offer the option to install the 6EZ either bulkhead or ballroom style.

LOW pH COMPATIBLE

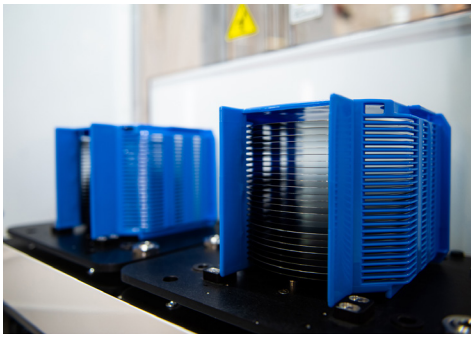
Materials used on the 6EZ are selected to be compatible with acidic SiC slurries.

TTV CONTROL

Plate-style carriers with adjustable back pressure provide superior TTV control without the need for wafer sorting prior to polish.

FULLY-AUTOMATED

Up to 50 wafers can be loaded into the machine and will be automatically polished on either a single side or both sides depending on the recipe selected. In a two-sided polish process, the machine polishes the carbon face first and automatically flips, cleans, and then polishes the silicon face of the wafers without operator intervention.



PRODUCTION PROVEN TECHNOLOGY

Built for high reliability, the 6EZ uses production- proven wafer carrier, spindle overarm, pad conditioning, and table rotation technology.

USER FRIENDLY

The user-friendly GUI and intuitive operator menus make recipe selection quick and simple. Maintenance and pad changes are easy to complete via multiple ergonomic access points around the machine.

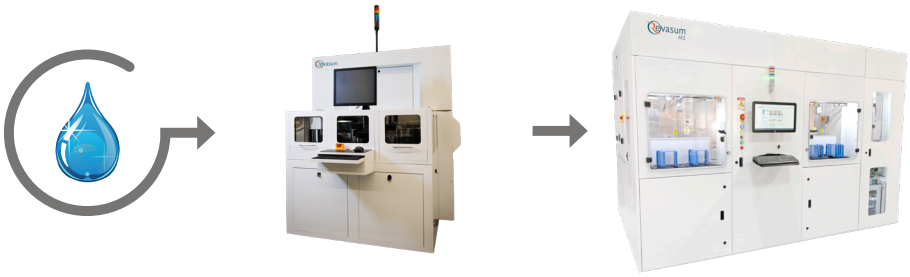
SINGLE WAFER PROCESSING RESULTS IN HIGHER YIELD

Single wafer processing means that each wafer is processed individually, rather than in a batch. Each wafer sees the same process conditions, which results in much better process control and wafer-to-wafer consistency.

Higher wafer yield, however, is the key advantage of single wafer processing.

TYPICAL SiC BATCH PROCESS FLOW

60% FEWER MACHINE-TO-MACHINE HANDOFFS COMPARED TO BATCH



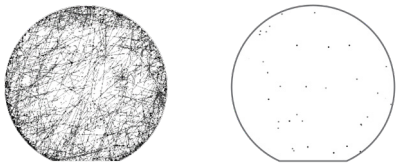
By combining Revasum's 7AF-HMG grinder and the 6EZ polisher, the entire process flow from wire slicing or laser splitting to EPI is synchronized to provide optimum performance and high yields at an affordable cost per wafer. Delivering a production-ready solution for 150mm and 200mm SiC substrate manufacturing.

ADVANTAGES OF SINGLE WAFER POLISHING

Revasum specializes in single wafer processing equipment, because single wafer processing:

- Provides better control over TTV and surface quality
- Eliminates the need for wafer sorting
- Reduces the number of machine-to-machine wafer transfer steps
- Lowers wafer breakage risk
- Improves cleanliness
- Enables process automation
- Increases productivity
- Achieves higher wafer yields

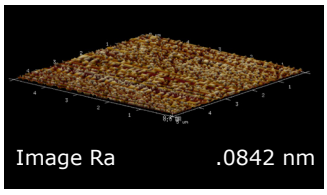
THE 6EZ PRODUCES A DAMAGE-FREE SURFACE



Batch Polish
19,999 scratches

6EZ Single Wafer
0 scratches

SURFACE FINISH SiC Si-FACE



Surface Roughness measured by AFM over 5 µm x 5 µm area, at mid-radius (~35mm) from the wafer center.

Revasum™

revasum.com/6EZ