Chapter 2
TSV-Based 3D Integration

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2.1 Introduction

2.1.1 Initial Studies and Experiments

Theoretical studies in the 1980s [1, 2] suggested that significant reductions in signal delay and power consumption could be achieved with 3D integrated circuits (3D ICs). A 3D IC is a chip that consists of multiple tiers of thinned-active 2D integrated circuits (2D ICs) that are stacked, bonded, and electrically connected with vertical vias formed through silicon or oxide layers and whose placement within the tiers is discretionary. The term "tier" is used to distinguish the transferred layers of a 3D IC from design and physical layers and is the functional section of a chip or wafer that consists of the active silicon, the interconnect, and, for a silicon-on-oxide (SOI) wafer, the buried oxide (BOX). The basic features of a 3D IC are illustrated in Fig. 2.1 in a symbolic drawing along with a cross-section of an actual 3D IC. The TSV (through silicon via) is an essential feature of the 3D IC technology and is the vertical-electrical connection formed between tiers and through silicon or oxide. A TSV is formed by aligning, defining, and etching a cavity between two tiers to expose an electrode in the lower tier; lining the sidewalls of the cavity with an insulator; and filling the cavity with metal or doped polysilicon to complete the connection. A TSV drawing and a cross-section of a TSV are shown in Fig. 2.2.

A 3D IC technology was viewed as necessary to maintain integrated circuit performance on the path described by Moore's law. One issue was the projected increase in chip-operating frequencies that would lead to different clock rise and

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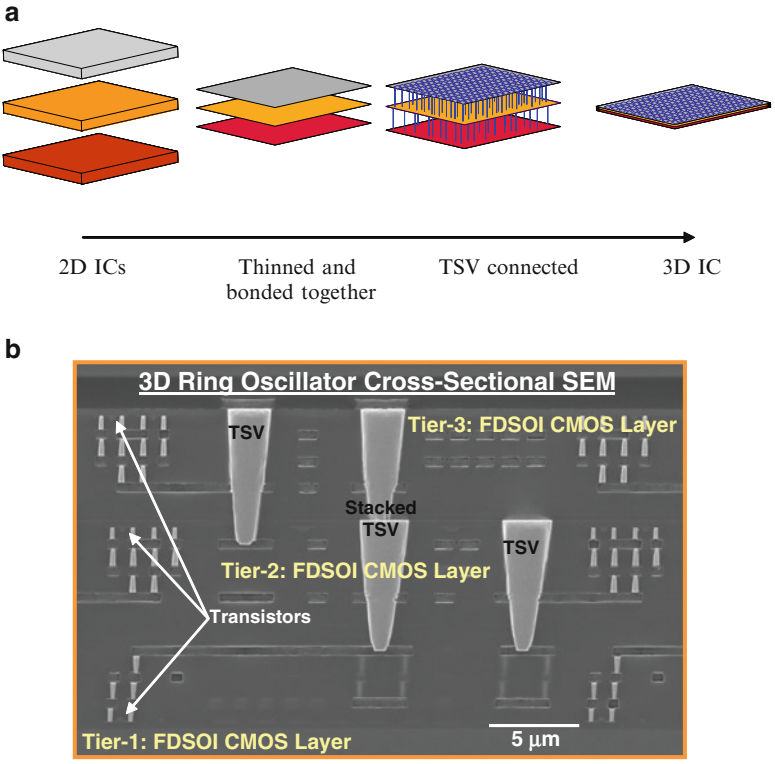

Fig. 2.1 (**a**) An expanded view that illustrates that a 3D IC consists of 2D ICs that are thinned, bonded together, and interconnected with TSVs distributed within the planes of the 2D ICs. (**b**) A cross-section of a 3D ring oscillator built with a fully depleted SOI (FDSOI) technology

fall times within a chip as shown in Fig. 2.3. Numerous theoretical studies examined the performance of 3D ICs as a function of the number of active tiers and the placement of memory, logic, and other functions among and within the active tiers, but early attempts to build even rudimentary 3D ICs were unsuccessful. Those 3D ICs were constructed using epitaxial overgrowth or polysilicon deposition [3] to stack silicon layers, but the transistor characteristics or transistor densities were unsatisfactory. Attempts to create vertical connections through silicon chips were frustrated by the inability to uniformly thin the chips to less than 50 µm and to insulate deep cuts etched through the thinned chips. At the same time IC technology developments led to tighter design rules and improved transistor performance so that IC progress continued to satisfy Moore's Law.

Within the last 10 years it became clear that Moore's law could not be met solely by transistor design and fabrication innovations. Therefore, the development of an alternate technology to design and construct microelectronic systems as 3D devices became essential.

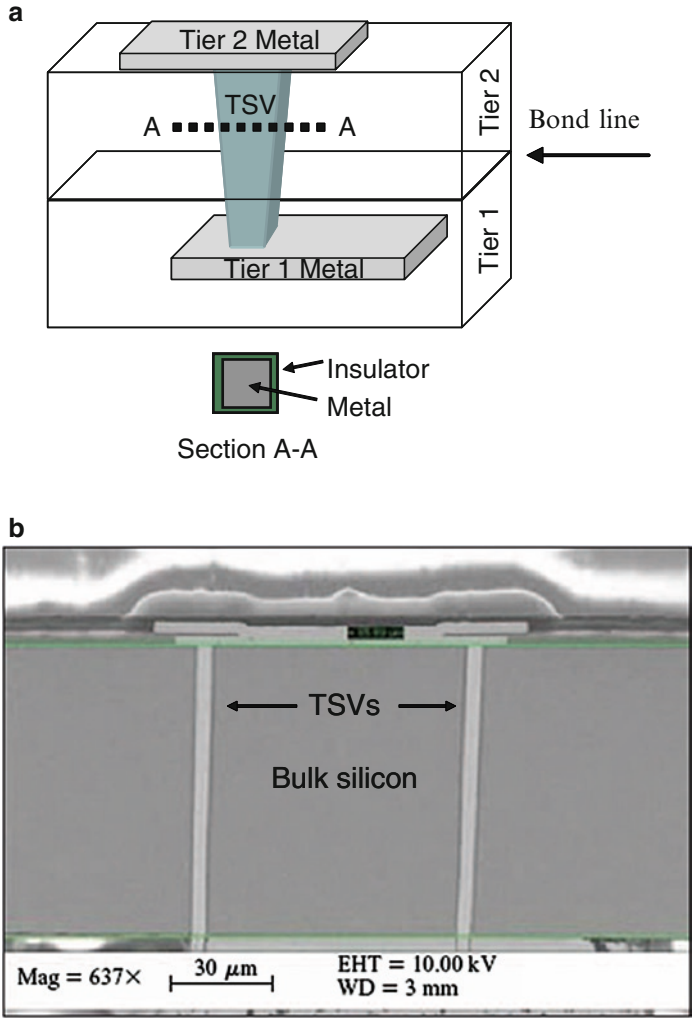

Fig. 2.2 (**a**) A drawing of a TSV and (**b**) a SEM of two parallel TSVs that are ~100 μm deep with an aspect ratio of 20, courtesy of IBM

2.1.2 Advanced 3D Packaging

Many of the gains projected for a 3D IC technology were achieved by advancements in packaging that reduced the interconnect length among chips [4]. Multichip modules, stacked-edge connected chips, and ball-bonded chips are examples of past packaging innovations. Further innovation included dual inline packages (DIP) configured to stack two DIPs with pins inserted into pins and stacked ceramic modules with chips bump-bonded face down to increase the functional density of the

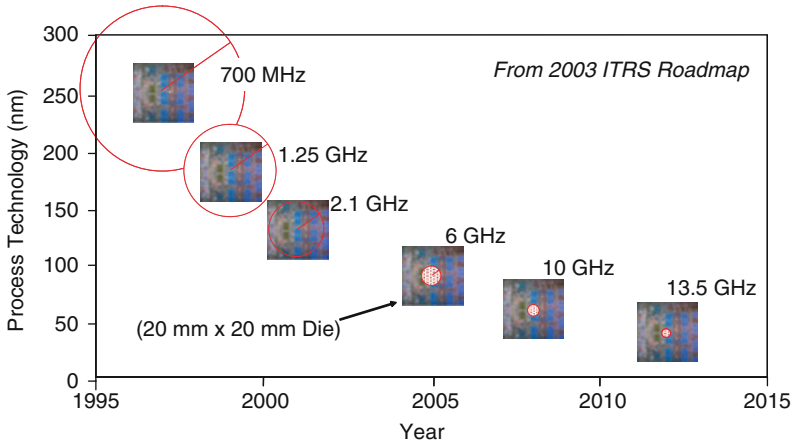

Fig. 2.3 Technology improvements have produced increased chip clock frequencies. The radius of the circle shows the distance a data signal can propagate within a single-clock-cycle as a function of clock frequency and indicates that above ~4 GHz data cannot be reliably clocked across a 20 mm × 20 mm die

package. Products that contain these advanced packages are in today's market place with cell phones being the consumer product that illustrates advanced packaging used to maximize performance, ease of use, and at a minimum size, particularly its thickness. However, the interconnect density in the direction perpendicular to the plane of the cell phone's circuit boards is still a small fraction of the multilevel metallization vias in any of its ICs. This suggests that future cell phones could be more compact and functional if constructed with 3D ICs.

Recent innovations in 3D packaging include a 3D IC system developed by ChipPac as shown in Fig. 2.4 where chips are stacked, bonded, and interconnected at the chips' edges and the stack assembly is attached and connected to a chip carrier. Another 3D packaging approach developed by Irvine Sensors is shown in Fig. 2.5. In this concept the interconnect is designed to extend to the edge of each chip so that when several chips were stacked and bonded together the edge of the assembly could be polished to expose the interconnect at the chips' edges. The compact 3D system was completed by depositing and patterning interconnect metal on the stack's edges.

In a more recent approach to building 3D chips, 2D chips are stacked and either bump- or adhesively bonded to a base wafer. In this design vertical connections are achieved within but not through the chips. The sizes of the chips can be different which permits the integration of chips from different sources and different technologies, but the alignment of the pads on the base wafer and the chips to be attached must be compatible. A Geiger counting imager [5], shown in Fig. 2.6, is an example of such a technology. The base wafer is a CMOS readout to which an avalanche photo diode array is adhesively attached and connections between the imager and the CMOS readout are made by deposited aluminum. The interconnect design limits

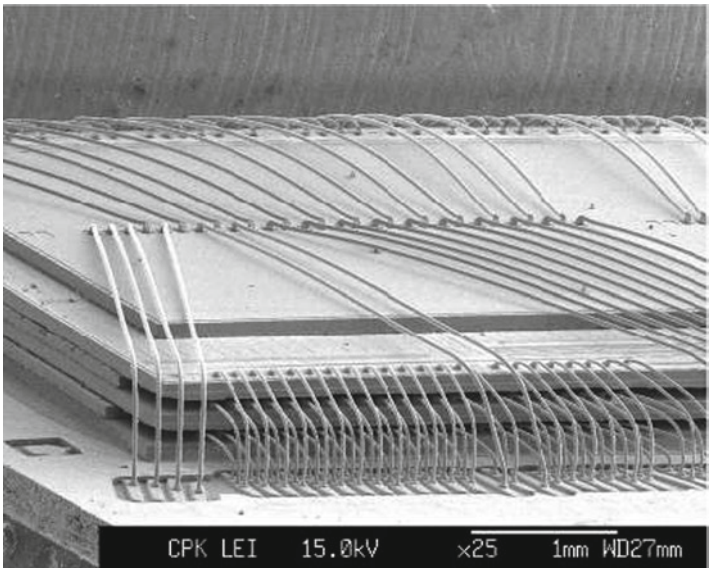

Fig. 2.4 A 3D package by ChipPac consists of four chips that are stacked and bonded. The chips are electrically connected to each other and to the chip carrier by wire bonds

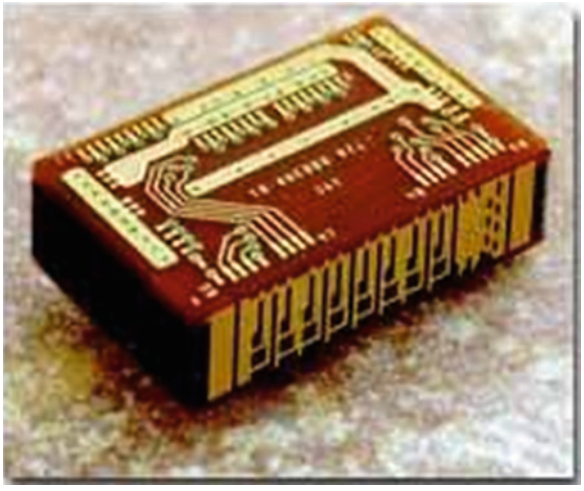

Fig. 2.5 Irvine Sensor's Neo-StackTM technology accommodates a variety of different sized chips that are stacked and edge connected to make a module of 4–50 layers that is less than 13 mm thick

the vertical connection density and image fill factor of the 3D chip. Similar 3D chips have been made using bump bonding techniques, but the density is limited by the size of the bond pads which are a function of the chip–wafer alignment budget and the bond pad size. Note that any of the preceding approaches to 3D construction can be embedded into a multichip module to further increase the packing density of the

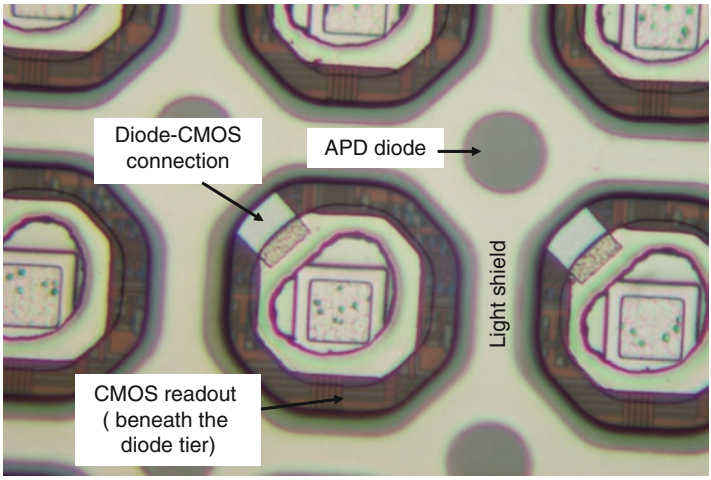

Fig. 2.6 A 32 × 32 Avalanche photo diode array bump-bonded to a CMOS readout with a 100-μm pitch and a 5% fill factor

system. However, none of these approaches has the ability to achieve vertical connections that are distributed within the chip's area with vertical interconnect densities that approach the density of back-end-of-the-line (BEOL) vias.

2.1.3 Recent Progress in 3D IC Technology

Within the last 10 years significant progress has been made in solving a fundamental set of 3D fabrication challenges.

- High strength and void-free chip and wafer-bonding processes [6] evolved from CMP techniques used to fabricate SOI wafers. Further refinements of those CMP processes made it possible to thin wafers to less than 50 μm with a total thickness variation less than 1 μm and without altering transistor parameters.
- The migration of SOI device technology into commercial production presented an alternate path to thin wafers by using the buried oxide as an etch stop to set the final tier thickness to be the sum of the BOX, the SOI layer, and the interconnect layers [7].
- Deep oxide and silicon-etching equipment and processes were developed to etch 50-um deep cavities with near vertical sidewalls.
- Similar improvements in dielectric and metal deposition techniques made it possible to reliably coat the cavities with a dielectric and fill them with conductors such as polysilicon or tungsten to form TSVs [8].
- Thermal compression bonding of copper TSVs became another chip–wafer or wafer–wafer bonding option [9].

- Alignment equipment originally developed for thick film processes was modified to permit improved wafer–wafer alignment with overlays less than 2 µm.
- More recently, the development of a wafer–wafer alignment system that incorporates wafer–stepper alignment principles has demonstrated wafer–wafer overlays less than 500 nm [10].

Numerous institutions are developing 3D IC technologies based on either wafer–wafer or chip–wafer bonding [11–15] and it is conceivable that the topology of advanced 3D ICs will be tailored to the application such as a lens-shaped chip for imaging system or even an irregular surface to mimic the human brain surface. No consensus has emerged as to the optimum path to achieve a 3D IC capability, but current progress has shown that a 3D IC technology is essential and probable rather than desirable and possible.

2.1.4 3D IC Technology in the ITRS Roadmap

The 2007-ITRS roadmap identified the interconnection problem as one of the near-term (through 2015) "grand challenges" since additional device and interconnect scaling alone could not deliver the required increase in IC performance. A 3D technology with TSVs aligned on a tight pitch was one of the new technologies identified to meet that challenge. The 2008 update [16] of the roadmap included increased emphasis on 3D IC technology development and specified a set of TSV-critical dimensions based on a stacked wafer model with wafers thinned to 10 µm. The TSV parameters analyzed are illustrated in Fig. 2.7 and a summary of the update is contained in Table 2.1. The wafer–wafer or chip–wafer alignment problem was defined as a major obstacle to scale the vertical interconnects and new approaches to the alignment problem were seen as necessary. Additional issues such as 3D IC design and thermal–mechanical modeling tools were identified as future challenges.

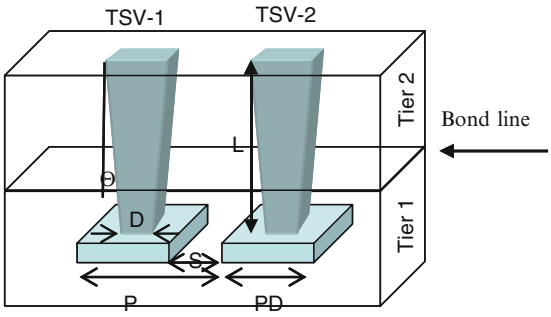

Fig. 2.7 The TSV parameters of Table 2.1 included in the 2008 ITRS update

Table 2.1 High-density through silicon via projections in 2008 ITRS update

	Year							
Principle parameters	2008	2009	2010	2011	2012	2013	2014	2015
TSV diameter, *D* (μm)	1.6	1.5	1.4	1.3	1.3	1.2	1.2	1
TSV pitch, *P* (μm)	5.6	5.5	4.4	3.8	3.8	2.7	2.6	2.5
Pad spacing, *S* (μm)	1	1	1	0.5	0.5	0.5	0.5	0.5
Pad diameter, PD (μm)	4.6	4.5	3.4	3.3	3.3	2.2	2.1	2
Bonding accuracy, Δ (μm), 3sigma	1.5	1.5	1	1	1	0.5	0.5	0.5

2.2 TSV-3D Integration Technologies

2.2.1 Introduction

The TSV is the structure that has the greatest potential for widespread use in advanced 3D ICs because it can be scaled to achieve a vertical connection density that approaches the density of 2D vias and its electrical properties of low electrical resistance, parasitic capacitance, and parasitic inductance are compatible with the requirements of advanced microelectronic systems. Equally important, TSV fabrication uses thin film processes typical of BEOL technologies unlike ball bonds, wire bonds, tape bonds, or solder bonds that are thick film technologies with limited potential to scale the connections.

All 3D IC fabrication process comprise three basic steps, namely wafer thinning, TSV etching and filling, and tier bonding (Fig. 2.1). Depending on the sequence of these steps we can distinguish between different approaches. A process is described as “TSV first” or “TSV last” if the TSVs are fabricated before or after tier bonding, respectively, and the order in which TSVs are fabricated within a 3D IC process is an important process decision to be made before developing a 3D IC technology. The process flows for TSV first, TSV last, and TSV middle – an intermediate flow – are contained in Table 2.2 [17] and 3D IC process flows for TSV-first and TSV-last technologies are illustrated in Figs. 2.8 and 2.9, respectively.

2.2.2 TSV Design

The goal of TSV design is to minimize the size and maximize the TSV pitch without exceeding the maximum resistance permitted by an application. This combination results in a TSV whose low capacitance and resistance leads to a power-efficient design that meets the system’s performance requirements. The resistance, R, of a TSV can be calculated as a function of the features illustrated in Fig. 2.6:

$$R = \rho L / (D - d)\left((D - d) + 2\tan\Theta L\right) \tag{2.1}$$

Table 2.2 TSV process flows

TSV first	TSV middle	TSV last
Etch deep silicon cavities	Etch deep silicon cavities	Fabricate transistors
Insulate cavities	Insulate cavities	Fabricate BEOL interconnect
Fill cavities with a conductor	Fabricate transistors	Bond wafer pair
Fabricate BEOL interconnect	Fill cavities with a conductor	Thin backside of upper wafer
Bond wafer pair	Fabricate BEOL interconnect	Backside etch deep silicon cavities
Thin backside of upper wafer	Bond wafer pair	Insulate cavities
Fabricate BEOL interconnect on upper wafer	Thin backside of upper wafer	Fill cavities with conductor

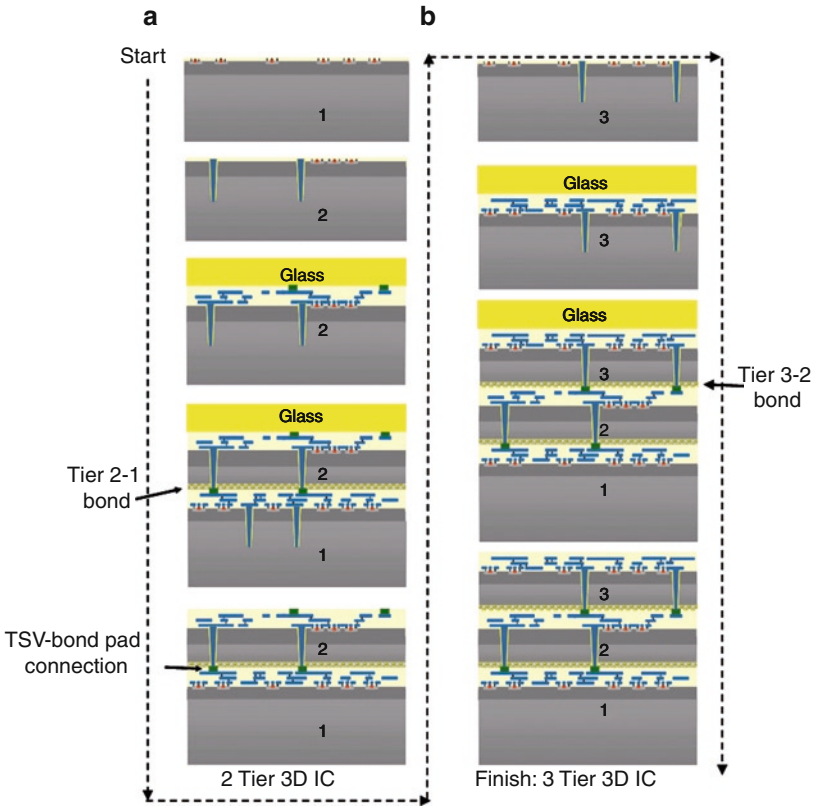

Fig. 2.8 The TSV-first process flow for a three-tier 3D IC. With the exception of the base chip, #1, all wafers have TSVs formed before first metallization. The assembly of a two-tier 3D device from wafers 1 and 2 is shown in column (**a**). The glass layer is bonded to wafer #2 to provide support during substrate thinning to expose the tips of the TSVs. Wafer #2 is aligned to bond pads on the lower tier and bonds are formed through contact with metal pads on the lower tier. After bonding the glass layer is removed. (**b**) Wafer 3 is added to the two-tier assembly to form a three tier 3D device

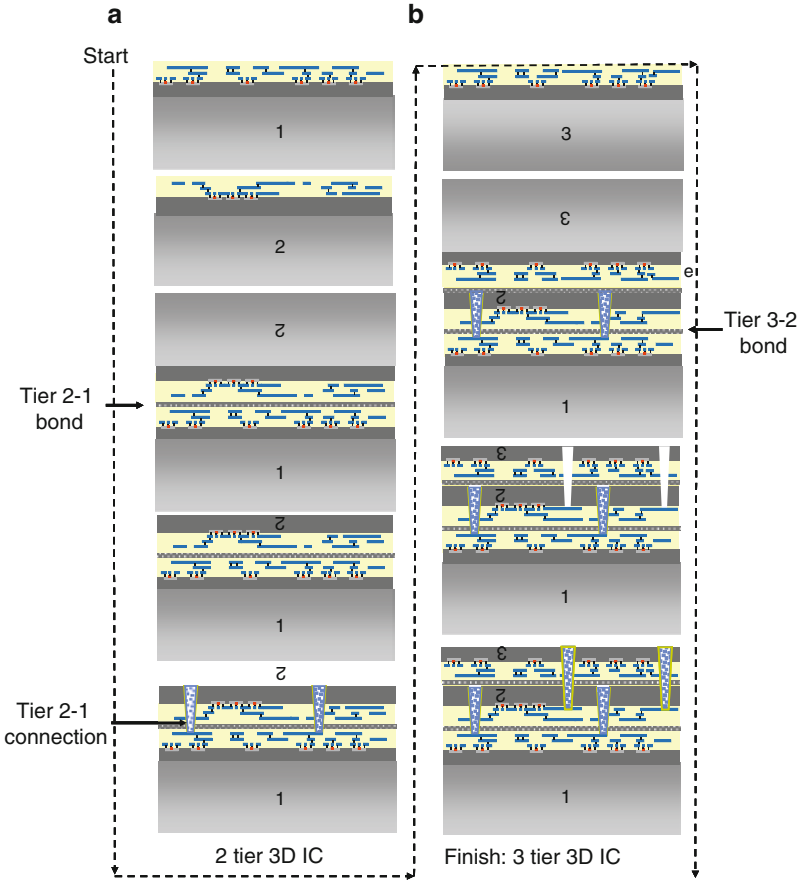

Fig. 2.9 The TSV-last process flow for a two-tier 3D IC is shown in column (**a**). After bonding wafer 2 to wafer 1, the substrate of wafer 2 is thinned then TSVs are formed between the wafers. A continuation of the TSV-last flow is shown in column (**b**) in which wafer 3 is bonded to the two-tier 3D assembly. Substrate thinning of wafer 3 and TSV formation complete the 3D process flow

where ρ is the resistivity of the metal plug, L is the length the TSV, D is the size of the TSV, which is assumed to be square at the bottom contact, d is the thickness of the dielectric on the TSV sidewalls, and Θ is the taper of the TSV cavity. Equation (2.1) indicates that it is desirable to reduce the dielectric thickness on the sidewalls in order to minimize the TSV resistance. From (2.1) we obtain the required size of the bottom contact, D as follows:

$$D = 2d - L\tan\Theta + \sqrt{((L\tan\Theta)^2 + (\rho L / R))} \tag{2.2}$$

We require that the TSV plug be fully landed; that is the plug must not extend beyond the lower metal pad. From this we determine the TSV pitch to be:

$$P = 2\mathrm{WA} + D + S + 2L\tan\Theta \tag{2.3}$$

where WA is the wafer–wafer alignment overlay and S is the minimum metal–metal spacing permitted in the 2D design rules. The final expression is as follows:

$$P = 2\mathrm{WA} + 2d + S + L\tan\Theta + \sqrt{((L\tan\Theta)^2 + (\rho L/R))} \tag{2.4}$$

Equation (2.4) indicates that a minimum TSV pitch requires that the TSV etch process produce vertical sidewalls, the dielectric deposition process produce thin-pinhole free dielectrics, and, most importantly, the alignment tool be capable of sub-micron wafer–wafer alignment.

2.2.3 SOI-Based TSV Technology

TSVs used in the fabrication of SOI-based 3D ICs [14] do not require deposition of a dielectric layer since the TSVs are placed in the field oxide regions of the ICs. As a result, the TSV process is simpler and, for the same pitch, the connection resistance is lower than that for a TSV through bulk silicon since the entire TSV cut is filled with a conductor. Because the TSVs are embedded in the field oxide, the parasitic capacitance and inductance between adjacent connections is reduced. A TSV design used in a SOI-based 3D IC technology is shown in Fig. 2.10. An SOI-based 3D IC technology is not the impediment it had been in the past since SOI wafer fabrication has emerged as a main line technology for high performance ICs and has also transitioned to a foundry.

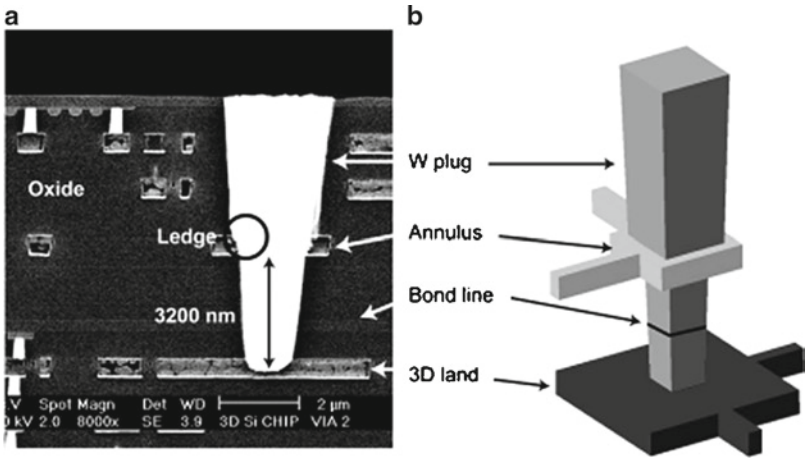

Fig. 2.10 (**a**) Cross-sectional and (**b**) isometric drawing of a TSV used in a SOI-based 3D IC technology. The tungsten plug connects the metal annulus in the upper tier to the metal pad (3D land) in the lower tier. The top of the plug is defined by a resist mask; the metal annulus defines the size of the plug at the 3D land

2.3 TSV Process Integration

2.3.1 Stack Alignment

The TSV pitch is a critical factor in the viability of the 3D technology since for optimal circuit density the minimum pitch of the TSVs should be comparable to that of the 2D vias that connect multilevel metal layers. The principle limit for the TSV pitch has been wafer–wafer alignment as described in the 2008 ITRS roadmap and as seen in (2.4). As an example, consider the layout of the 3D ring oscillator in Fig. 2.1b. The device was successfully fabricated using an SOI-based 3D technology with inverters in two tiers that were connected with TSVs so that the oscillator's signal cycled between tiers as shown in the figure. In the design shown in Fig. 2.10 the bottom metal contact of the TSV is the 3D Land and the TSV cut is the size of the resist mask used to etch the TSV cavity. The 3D Land is:

$$\text{3D Land} = 2\text{WA} + D. \tag{2.5}$$

In the initial set of 3D design rules the 3D Land was 5.5 μm since the wafer–wafer alignment overlay was 2 μm and D was 1.5 μm. An improved alignment system [10] with an overlay of 0.5 μm and an improved TSV etch process with D = 0.5 μm permitted scaling the 3D Land to 1.5 μm and a reduction in pitch from 9 to 4.5 μm. This example illustrates that alignment overlay is a fundamental impediment to decreasing the size of TSVs.

2.3.2 Stack Bonding

Two issues are dominant in the development of a proper bonding technique. The first is establishing the bonding process itself together with the appropriate materials. The second involves maintaining the mechanical stability of the individual tiers and the complete stack during and after the bonding process is complete.

Early attempts to build 3D ICs used adhesives as the bonding technology [18]. Experiments indicated that the TSV pitch could not be scaled to less than 6 μm with an adhesive bond due to outgassing from the adhesive. In addition, the adhesive was not sufficiently stable to develop 3D ICs with three or more tiers. That led to the development of alternate technologies such as low temperature oxide–oxide bond [6] and metal–metal thermal compression bond processes [9]. Any bond process must be compatible with the alignment technique used so that the alignment is not degraded during bonding and the process must also be consistent with stacking more than two tiers for those cases where a 3D IC composed of three or more tiers is required. These requirements mean that the thermal processes of layer bonding must not weaken any bonds and TSV connections previously established.

Metal–metal and metal–oxide bonding techniques have been used for years in lead attachments and glass–metal seals and that technology has been extended to 3D integration. Copper–copper bonding is an attractive candidate for TSV-first processes since it creates a strong bond and an electrical connection simultaneously and the copper layers can aid heat extraction. However, the TSV conductor cannot be a part of the wafer-bonding process for TSV-last processes. In any bonding process, cleanliness is essential to eliminate voids created by particles. An additional void creation mechanism is gaseous reaction products created during silicon and oxide bonding that cause bubbles that create bond voids. The bond is initially formed at room temperatures immediately following alignment and additional processes are required to increase the bond's strength. When successfully implemented, the bond process leads to a very thin bond with no voids and has the strength to maintain wafer–wafer alignment during the addition of one or more tiers to the system.

Wafer distortion during fabrication must be controlled since excess deformation will decrease the wafer bond strength particularly for oxide-fusion processes where intimate contact between surfaces is required to initiate and establish a strong bond. Wafer deformation is reduced by using compensating films on the backside of wafers to decrease the deformation to less than 50 μm for a 150-mm diameter wafer, a value that will not compromise the bond process. In addition, wafer distortion, some times called continental drift, can lead to misalignment between critical features of the TSV. In principle it could be possible to compensate for distortion by measuring wafer distortion and offsetting the distortion with a wafer chuck having the ability to maintain temperature gradients. Ultimately, a process must be characterized to determine the amount of distortion that occurs so that the value can be added to the design of the TSV since distortion is an additive factor in misalignment.

2.3.3 TSV Etching and Filling

In order to minimize the TSV pitch, an etch chemistry is required that maximizes the aspect ratio of the TSV cavity defined as the ratio of the depth to the width of the cavity. In addition the etch process must be selected to avoid resist erosion which can lead to an increase in the lateral size of the cavity at the surface. A mask, such as aluminum, that is not attacked by the etch process can be used to maintain the dimensional integrity of the mask but removal can be a challenge. In all cases mask removal must be compatible with the TSV metals used, particularly for TSV-last processes. Etch reaction products must be monitored and controlled since they can alter or block the deep cavity etch [19]. In the case of a TSV cavity formed through silicon, a pin-hole free insulator must be deposited on the sidewalls, the bottom corners, and the top edges to provide a reliable insulated coating for yield and reliability considerations. Another etch process is required to remove the insulator from the bottom of the cavity to expose the metal pad without attacking the

insulator on the sidewalls or the metal pad. This challenge does not exist for SOI-based 3D IC technologies, since the TSVs are formed in the field oxide. Metal deposition processes must have thermal cycles that do not degrade the 3D bonding and TSV structures previously established. A lesser problem for a TSV design but one that requires some thought is the possibility of field-induced leakage due to a lightly doped substrate so sidewall doping may be required. A TSV-last process that includes SOI and bulk wafer fabrication, oxide fusion bonding, oxide etching to form 8-μm TSV cuts with tungsten connections was used to fabricated three layer 3D ICs [14]. The bond temperature never exceeded 275ºC while the oxide and tungsten deposition temperatures were 450º and 475ºC, respectively.

Finally a thermal analysis of the entire 3D IC fabrication process is required to insure that the 3D IC is thermally stable and the electronic properties of the devices have not been degraded at the completion of the 3D IC process.

2.4 Characterization of TSV Processes

2.4.1 Physical Characterization

Stack bond strength is evaluated by the crack insertion test [20] using a pair of witness wafers. The percentage of bond voids is measured with infrared microscopy using a pair of witness wafers or with an acoustic imaging system using a bonded pair. Experience has shown that the extensive use of witness wafers is essential to maintain control of the bond process since the bond strength measurement is a destructive measurement and a defective bond can lead to the loss of the entire 3D assembly. Wafer–wafer alignment after bonding and substrate thinning is measured using standard lithographic metrology tools but the optical path between alignment structures in both tiers must be free of opaque layers which places restrictions on the design of alignment targets.

2.4.2 Electrical Characterization

Active and passive test devices are required for in-process and completed assembly analysis. Electrical test structures can also be used to measure stack alignment after 3D fabrication either by measuring the via resistance or by measuring the yield of TSV structures designed with varying degrees of misalignment between the TSV cut and pad. The TSV design can be optimized and the process margins determined by measuring the yield of TSV chains designed with a set of TSV sizes and misalignment values. Test transistors are required for testing during the 3D assembly process and at the completion of 3D assembly in order to determine if the 3D process has degraded the devices. Witness wafers with TSV chains and test transistors are valuable tools to

aid the development and control of the 3D IC process. TSVs are required to reach transistors in each of the tiers to determine whether heat dissipation, oxide charge within the 3D assembly, or processing problems have altered transistor performance. In all cases it is essential that those same transistors be measured before the initiation of 3D process to accurately measure device changes due to the 3D process. TSV structures are also required for the extraction of resistance, capacitance and inductance and to optimize CAD software for the analysis of circuit performance. It is important to place standard circuits such as ring oscillators, SRAMs and counters in each of the tiers to assess fabrication effects on circuit yield and at least one of the circuit types should have components distributed in each level since it is difficult to diagnose circuit failure of large 3D circuits. A ring oscillator is a good candidate for this activity.

2.4.3 3D vs. 2D Chip Yield

The major yield detractors for a 3D IC technology are bond defects from stacking, TSV opens, TSV shorts to polysilicon or to the metal interconnect due to stack misalignment, and changes of device parameters due to 3D processing. The latter yield detractor can sometimes be minimized by a post-processing sinter. Singulation, the dicing of a 3D wafer stack into individual 3D chips, can be a loss mechanism due to the 3D assembly delaminating in the dicing streets since the thinned tiers are susceptible to fracture from dicing debris. This failure mechanism can be minimized by layout practices that keep the streets free of metals and polysilicon. Heat buildup within the stack is a unique 3D failure mechanism that can cause parametric drift and circuit failure [21–22] and the removal of heat from a 3D IC chip is a major challenge confronting 3D technology development.

2.5 TSV-Based Chips

2.5.1 3D Design Challenges

Within the last 5 years, 2D circuit design, layout, and circuit extraction tools have been adapted to design 3D circuits and work continues to improve the tools [23–24]. One challenge is to design the CAD tools to be compatible with the different 3D technologies such as TSV-first and TSV-last as well as a bulk wafer vs. a SOI-based 3D technology. 3D IC is an evolving technology and CAD tool development, to be effective, must take place in step with the 3D technology which includes the development of improved models of TSVs so the tools can better simulate 3D IC circuit performance. Visualization of 3D chips from the design data both in cross section as well as in an exploded view is essential both for the chip designer and for the technologist to support yield studies and failure analysis as part of the fabrication and development effort (Fig. 2.11).

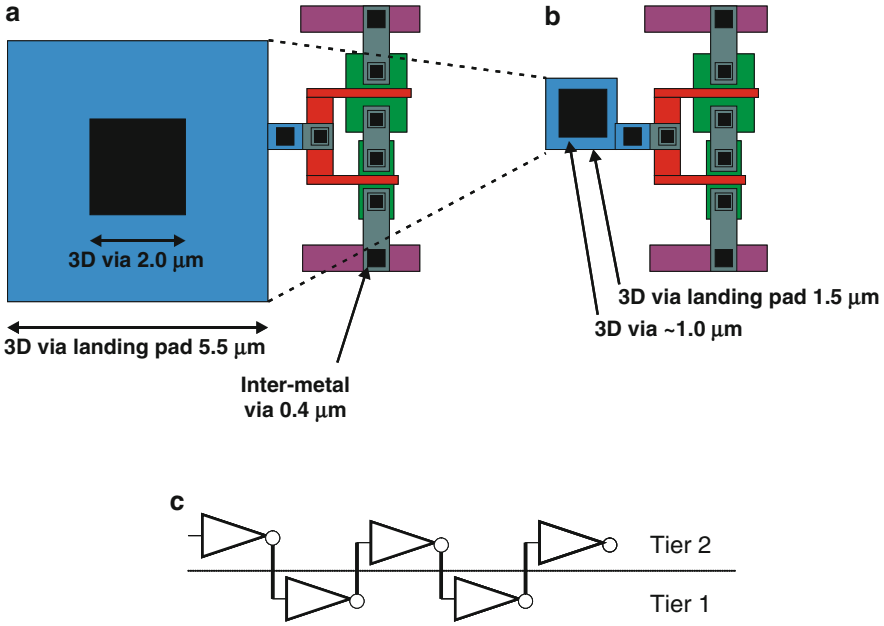

Fig. 2.11 (**a**) The landing pad of a SOI- based 3D inverter fabricated with the TSV of Fig. 2.9 is reduced from 5.5 μm (**b**) to 1.5 μm by a reduction of alignment overlay error and TSV size. (**c**) The inverters are located in two tiers and connected by TSVs to from the 3D ring oscillator in Fig. 2.1

2.5.2 Functional 3D Chips with TSV

A 3D imager is an obvious application of 3D due to the possibility of achieving a 100% fill factor which is an imaging plane unobstructed by interconnections and other opaque features. This is a result that cannot be achieved by scaling a 2D technology. A 3D imager [25] that was reported by Lincoln Laboratory is shown in Fig. 2.12. 3D IC chips with memory attached to a processor chip is another important application since dense TSVs will minimize routing delays as well as delays in obtaining information from the memory and numerous institutions have reported such 3D chips. 3D has been touted as a natural application for ICs with mixed materials and or mixed technologies. The mixed material 3D ICs are of particular interest for building imagers that operate in the ultraviolet and infrared spectrums but utilize silicon readouts and the integration of Indium phosphide with silicon CMOS has already been demonstrated [26]. 3D ICs constructed with different processes are of particular interest and a mixed silicon technology chip has been demonstrated that was composed of three tiers: a photo diode layer, a 3.3-volt CMOS layer, and 1.2 and 1.5-V CMOS layers to form an avalanche photodiode imager [27].

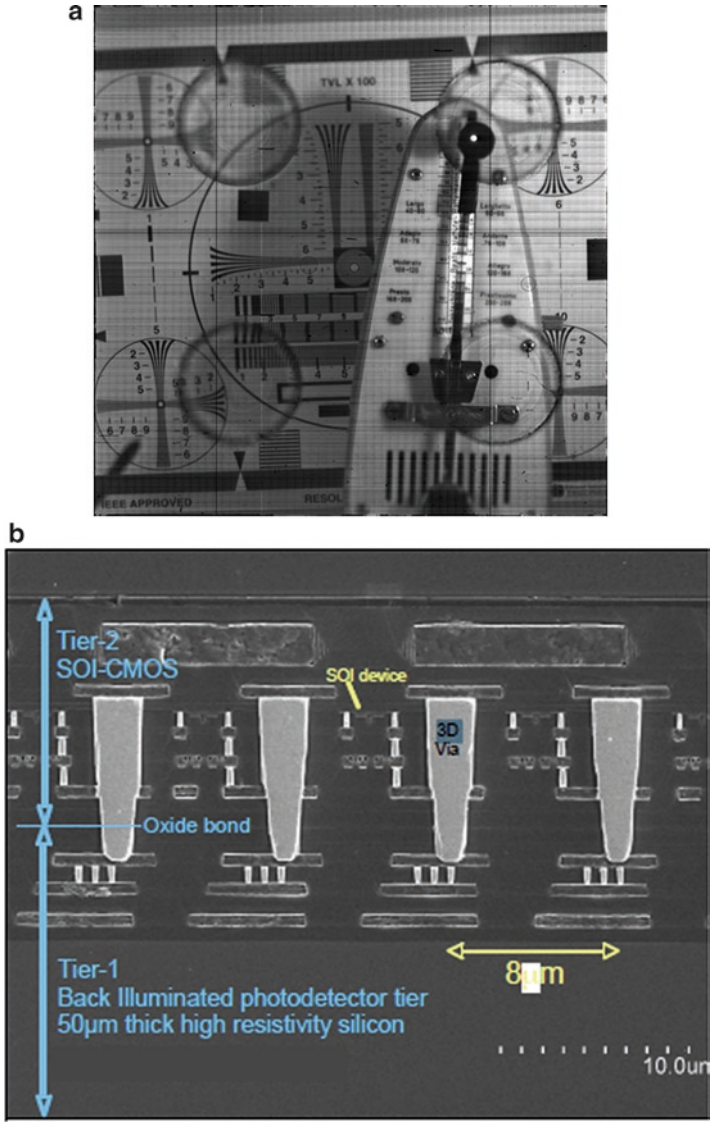

Fig. 2.12 (**a**) Captured raw image from digital tile at 10 fps, with digital data read out in 1 ms and (**b**) cross-sectional SEM micrograph through functional 3D-integrated active-pixel imager

2.6 Future Challenges

The lack of access to 3D fabrication by circuit designers has been an impediment for 3D design and has limited a full exploration of 3D opportunities. However, several institutions have opened their technology to external designers who can

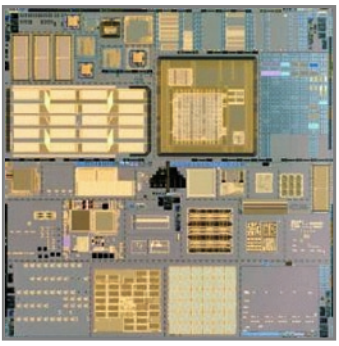

Fig. 2.13 (**a**) Photograph of a 22 × 22 mm 3D multiproject chip fabricated with a SOI-based 3D technology and (**b**) a list of 3D circuits designed by members of the 3D community. Multiproject programs will be the key to future 3D IC design

submit their IC designs for 3D fabrication. Lincoln Laboratory has published 3D design rules and completed three 3D multiproject fabrication runs based on a three-tier technology with TSVs. A photograph of the 3D chip and a list of 3D circuits contained in the chip are shown in Fig. 2.13. Tezzaron has acquired funding to support a 3D multiproject program and IMEC has also established a multiproject capability. However, continued financial support from the microelectronic industry or governments will be required to sustain access to 3D technologies until IC houses commit to establishing a 3D capability. An encouraging development that will aid 3D IC fabrication efforts is the formation of a consortium by equipment suppliers to accelerate the development of 3D IC-specific equipment.

The TSV design must continue to be scaled if 3D is to satisfy new applications. Fabrication advancements and improved wafer–wafer alignment tooling will scale future TSVs. However, each TSV requires a zone about it from which there can be no silicon, polysilicon, or metal interconnect thus decreasing the effective density of the chip. As a result the TSV scaling limit may not be based on feature sizes but on the exclusion zones required by the TSV and work will be required to minimize the impact of those exclusion zones. Layout tools will be required to better partition circuits among tiers to optimize TSV placement and minimize the impact of TSVs on circuit density.

The greatest technological challenge is heat control and removal from within a 3D IC, particularly the embedded layers, and improved CAD tools will be essential for the optimal placement of heat-generating circuits to minimize heat effects on 3D IC performance.

There are also challenges in the factory connected with yield. A wafer-scale 3D technology represents the greatest yield risk since a bond failure could doom at least two wafers if not more. For that reason chip–wafer circuits will continue to receive

careful attention to work around the yield problem. Yield can also be a problem due to the coincidence of defective transistors that would cause 3D circuit failure. Redundancy techniques can be used initially to work around defective regions but eventually test techniques will be required to map the good regions of each wafer in order to match wafers of varying quality prior to 3D assembly. Technology development will be required to introduce conductive features such as heat pipes or cooling channels between or within the tiers to further minimize heat effects on circuits.

In spite of these challenges, the demonstrations of functional 3D imagers, 3D processors with stacked memory, 3D CMOS with stacked MEMS, and 3D ICs with mixed technologies and materials are proofs of concept that a 3D IC technology in the marketplace is within sight.

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