Chapter 2
Gain-Cell eDRAMs (GC-eDRAMs): Review of Basics and Prior Art

2.1 Basics of GC-eDRAM

While 6-transistor (6T)-bitcell static random-access memory (SRAM) macrocells are the mainstream solution for embedded memories in very large scale integration (VLSI) systems-on-chip (SoCs), as discussed in Chap. 1, embedded dynamic random-access memory (eDRAM) macrocells are an interesting area-efficient alternative. The conventional eDRAM bitcell uses a dedicated storage capacitor to store information in the form of electric charge. It further uses a single metal-oxide-semiconductor field-effect transistor (MOSFET) to access the storage capacitor for read and write operations. Unfortunately, such conventional 1-transistor-1-capacitor (1T-1C)-bitcell eDRAM requires special processing steps to manufacture high-density stacked or trench capacitors. It is therefore not directly compatible with standard digital complementary metal-oxide-semiconductor (CMOS) technologies [16] and not readily available for integration with logic in all process flavors and nodes.

As opposed to conventional 1T-1C eDRAM, gain-cell (GC) based eDRAM (GC-eDRAM) is fully compatible with mainstream digital CMOS technologies, since it is built exclusively from MOSFETs and, optionally, the readily available metal stack and vias. MOSFETs are used as access transistors and as MOSCAPs. Metal layers and vias can be used to enhance the storage node capacitance. As such, GC-eDRAM is an interesting alternative to 6T-bitcell SRAM and 1T-1C eDRAM, since it combines many of the advantages of SRAM (e.g., the compatibility with digital CMOS technologies) and 1T-1C eDRAM (e.g., higher storage density than SRAM), while it avoids most of the drawbacks of SRAM (e.g., the large bitcell) and of 1T-1C eDRAM (e.g., the destructive read, write-back operation, and extra cost for special process options). Thanks to its compatibility with standard digital CMOS technologies, GC-eDRAM macrocells can readily be integrated with any digital system at no additional manufacturing cost for special process options, as opposed

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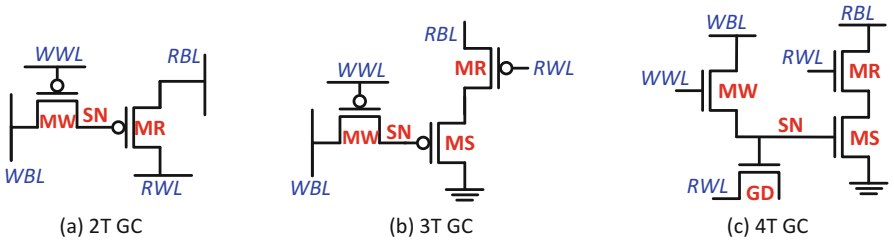


Fig. 2.1 Basic 2–4T gain-cells (GCs). (**a**) 2T GC. (**b**) 3T GC. (**c**) 4T GC

to 1T-1C eDRAM. The main drawback of GC-eDRAM compared to SRAM is the dynamic characteristic of the data retention, which usually requires periodic refresh operations.

A large variety of different GC topologies have been proposed in the last decade, consisting of 2–4 transistors. Basic examples of 2T, 3T, and 4T GCs are shown in Fig. 2.1. All of these circuits exhibit a write transistor (MW) to access the capacitive storage node (SN) and deposit charge on it. Moreover, all GC topologies have an SN capacitor which consists of a dedicated MOSCAP, the junction capacitance of MW, and in some cases of sidewall and parallel-plate capacitors built above the cell footprint with the available metal and via resources. In the smallest 2-transistor (2T) GC configuration (see Fig. 2.1a), the dedicated storage transistor, i.e., the MOSCAP, is also used as read transistor (MR). The slightly larger 3-transistor (3T) GC configuration (see Fig. 2.1b) exhibits a more robust read operation by using a separate MR, which decouples the read bitline (RBL) from MR. Some 4-transistor (4T) GCs (see Fig. 2.1c) use an additional MOSCAP to increase the SN capacitor and to capacitively couple the RBL to the SN for increased read robustness. The term "gain-cell" stems from the transconduction gain of the read transistor MR, which translates a voltage level on the SN, or, equivalently, the gate voltage of MR, into an output sense current, i.e., the drain current of MR. From a similar point of view, the term "gain" can also relate to the fact that a small amount of charge on the SN leads to a large charge flow on the RBL during readout thanks to the use of MR [21].

2.2 Advantages and Drawbacks of GC-eDRAM

GC-eDRAM has several advantages compared to both SRAM and 1T-1C eDRAM. In fact, a GC is significantly smaller than a 6T SRAM bitcell; typically, area savings of at least 50% can be achieved by employing GCs instead of SRAM bitcells. Moreover, GCs have much lower aggregated bitcell leakage currents than SRAM bitcells. This reduced bitcell leakage current can even lead to lower GC-eDRAM data retention power, i.e., the sum of leakage and active refresh power, compared

to the static leakage power of a corresponding SRAM macrocell [6]. Compared to conventional 1T-1C eDRAM, GC-eDRAM does not require any special processing steps to build high-density trench or stacked capacitors [16], which would require 4–6 extra masks and would add cost to a digital CMOS process [14]. As a further advantage compared to 1T-1C eDRAM, GCs enable a nondestructive read operation and thereby avoid the need for a write-back or restore operation.

Furthermore, compared to both the 6T SRAM bitcell and the 1T-1C bitcell, all GC topologies have a separate read and write port, which allows the construction of two-port GC-eDRAM macrocells at virtually no area overhead compared to single-port macrocells. As opposed to that, both the 6T SRAM bitcell and the 1T-1C bitcell share the same bit-line(s) (BL) and word-line (WL) for both write and read accesses. Therefore, additional hardware is required in each basic storage cell to allow simultaneous write and read access to a storage array built from SRAM or conventional DRAM cells. The use of two-port GC-eDRAM macrocells is appealing to ensure high memory bandwidth compared to single-port macrocells [15]. This can be especially interesting to recover some of the speed penalty resulting from voltage scaling, which is required for low power consumption, or simply to ensure high access bandwidth for GC-eDRAMs used as caches in high-performance microprocessors. Finally, the separate write and read ports of all GC topologies allow to independently and simultaneously optimize the bitcell for enhanced write-ability and read-ability. This is especially important for the implementation of embedded memories in aggressively scaled CMOS nodes, characterized by high parametric variations, and/or operated at low voltages, in which case parametric variations become problematic due to degraded on/off current ratios. Note that the possibility of simultaneously and independently sizing the transistors in a GC for robust read and robust write is a unique property of GCs which cannot be found in the 6T SRAM bitcell or in the 1T-1C eDRAM cell. In fact, in case of SRAM bitcells, additional transistors are required to avoid write contention and to improve read-ability.

These various advantages of GCs compared to the traditional 6T SRAM and 1T-1C bitcells motivate the analysis and optimization of GC-eDRAM for use as embedded memories in a large variety of future low-power VLSI SoCs implemented in scaled CMOS nodes and operated a scaled voltages.

Beside this long list of advantages, the main drawback of GC-eDRAM, compared to SRAM, is the dynamic storage mechanism, which requires periodic, power-consuming refresh cycles (unless the memory block is anyway periodically updated, such as the internal memories of the LDPC decoder presented in [27]). Compared to the conventional 1T-1C eDRAM bitcell, the total in-cell storage capacitor of GCs is considerably smaller, which leads to shorter retention times and requires more frequent refresh cycles. Also, there is a large variability of per-cell retention time across a GC-eDRAM array [7, 25], and, unfortunately, the global refresh rate needs to be set according to the GC with the worst retention time, unless spare rows or columns in conjunction with programmable address decoders are used [1]. Later on in this book, in Chaps. 4 through 7, we present several techniques to improve the retention time of GC-eDRAM in order to render it even more attractive for use in

future low-power VLSI SoCs. However, before presenting our novel GC-eDRAM designs, a detailed review of the field of GC-eDRAM is presented in the remainder of this chapter, which also positions the herein presented work with respect to prior-art GC-eDRAM implementations.

2.3 Review of Prior-Art GC-eDRAM Circuit Techniques and Target Applications

2.3.1 Categorization of GC-eDRAM Implementations

From the large amount of recent publications on GC-eDRAM, it is possible to identify four main categories of target applications: (1) high-end processors requiring large embedded cache memories; (2) general system-on-chip designs; (3) low-voltage low-power systems, such as biomedical systems; and (4) fault-tolerant systems including channel decoders for wireless communications. The following sections provide more details on each of these four categories.

2.3.1.1 Gain-Cells for High-End Processors

The vast majority of recent research on GC-eDRAM is dedicated to large embedded cache memories for microprocessors [3–6, 20–22, 29–32]. In fact, GC memories are considered to be an interesting alternative to SRAM, which has been the dominant solution for cache memories for several decades. This is due to the higher density, increased speed, and potentially lower leakage power of GC-eDRAM w.r.t. SRAM. Besides the obvious advantage of high integration density, the main design goals for GC-eDRAMs in this application category are high speed operation and high memory bandwidth, especially for industrial players like IBM [22] and Intel [30, 31], and more recently also for academia [4, 6]. A smaller number of research groups specify low power consumption as their primary design goal [3, 5]. In fact, as mentioned before, a recent study shows that GC-eDRAMs potentially consume less data retention power (sum of leakage and refresh power) than SRAM arrays (leakage power only) [6].

2.3.1.2 General Systems-on-Chip (SoCs)

Several authors are not very specific about their target applications [2, 11, 12], as they only mention general SoCs. However, they follow the same trend as the aforementioned high-end processor community by proposing GC-eDRAMs as a replacement for the mainstream 6T-bitcell SRAM solution. For these SoC applications, the main drivers are the potential for higher density and lower power consumption than SRAM.

2.3.1.3 Gain-Cells for Ultra-Low Power (Biomedical) Systems

While the previously described target applications require relatively high memory bandwidth, several recent GC-eDRAM publications target low-voltage low-power applications, mostly in the biomedical domain. After a short preview in this section, GC-eDRAM design for low-voltage low-power applications will be extensively discussed throughout the remainder of this book. A GC-eDRAM implemented in a mature low-leakage 180 nm CMOS process achieves low retention power through voltage scaling well below the nominal supply voltage [19]. The positive impact of supply voltage scaling on retention time for given access statistics and a given write bit-line (WBL) control scheme is demonstrated in [13] and expatiated on in Chap. 4, proposing near-threshold (near-V_T) operation for long retention times and therefore low retention power. Moreover, a full transmission gate (TG) write port [10], reverse body biasing (RBB) [25], and replica techniques have been proposed in order to further enhance the retention time and reduce the power consumption of near-V_T GC-eDRAM macrocells, as will be shown in Chap. 5. Furthermore, recent studies [24, 26] show that the supply voltage of GC arrays can even be scaled down to the subthreshold (sub-V_T) domain, while still guaranteeing robust operation and high memory availability for read and write operations; more details on these studies are given in Chap. 6. Finally, partial internal feedback is used in [8] in order to increase the data retention time and achieve ultra-low retention power, while area-efficient per-cell redundancy is proposed in [9] for increased soft error tolerance of ultra-low power SoCs; details on these techniques are provided in Chap. 7.

2.3.1.4 Gain-Cells for Wireless Communications Systems

A small number of recently presented GC-eDRAM designs are fundamentally different from the aforementioned works, as they are specifically built and optimized for systems which require only short retention times, and in some cases, are tolerant to a small number of hardware defects (such as read failures) [17]. The refresh-free GC-eDRAM used in a recently published low-density parity-check (LDPC) decoder is periodically updated with new data, and therefore requires a retention time of only 20 ns [28]. Besides safely skipping power-hungry refresh cycles and designing for low retention times, a few works [18, 23] also exploit the fact that wireless communications systems and other fault-tolerant systems are inherently resilient to a small number of hardware defects. In fact, by proposing memories based on multilevel GCs, the storage density of GC-eDRAMs is further increased at the price of a small number of read failures which do not significantly impede the system performance [18, 23].

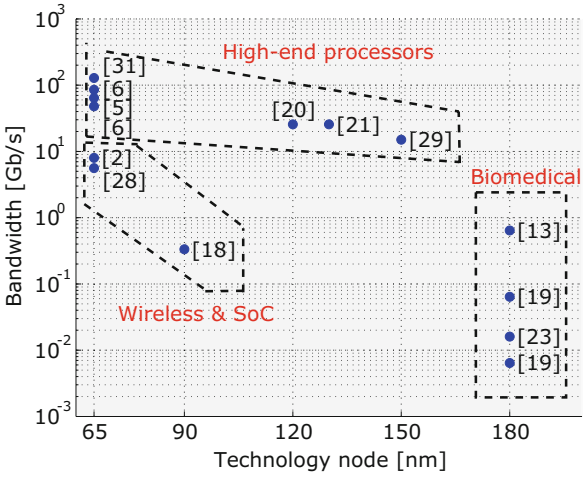


Fig. 2.2 Bandwidth vs. technology node of several published GC-eDRAM implementations

2.3.2 *Comparison of the State-of-the-Art Implementations*

Figure 2.2 shows the bandwidth and the technology node of the state-of-the-art GC-eDRAM implementations, highlighted according to target application categories. References appearing multiple times correspond to different operating modes or operating points of the same design. The figure shows a difference of more than four orders-of-magnitude in the achieved memory bandwidth among the various implementations. GC-eDRAMs designed as cache memory for processors achieve around 10 Gbit/s, if implemented in older technologies, and over 100 Gbit/s if implemented in a more advanced 65 nm CMOS node. Most memories designed for wireless communications systems or generally for SoCs still achieve bandwidths between 1 and 10 Gbit/s. Only the high-density multilevel GC array has a lower bandwidth due to a slow successive approximation multilevel read operation [18]. GC-eDRAMs targeted at biomedical systems are preferably implemented in a mature, reliable 180 nm CMOS node and achieve sufficiently high bandwidths between 10 Mbit/s and several 100 Mbit/s at near-V_T or sub-V_T supply voltages.

Figure 2.3 shows the retention power, i.e., the sum of refresh and leakage power, of previously reported GC-eDRAMs versus their retention time. For energy-constrained biomedical systems, long retention times of 1–10 ms are a key design goal in order to achieve low retention power between 600 fW/bit and 10 pW/bit. The memory banks of the LDPC decoder in [28] have a nominal retention time of 1.6 µs, which is around four orders-of-magnitude lower than that of the arrays targeted at biomedical systems. Even though the reported power consumption of 5 µW/bit corresponds to active power [28], it is fair to compare it to the retention power of other implementations, as data would anyway need to be refreshed at the same rate as new data is written. Interestingly, the power consumption per bit of this refresh-free eDRAM is almost seven orders-of-magnitude higher than the retention power per bit of the most efficient eDRAM implementation for biomedical systems. The retention time and retention power of GC-eDRAMs for processors are in between

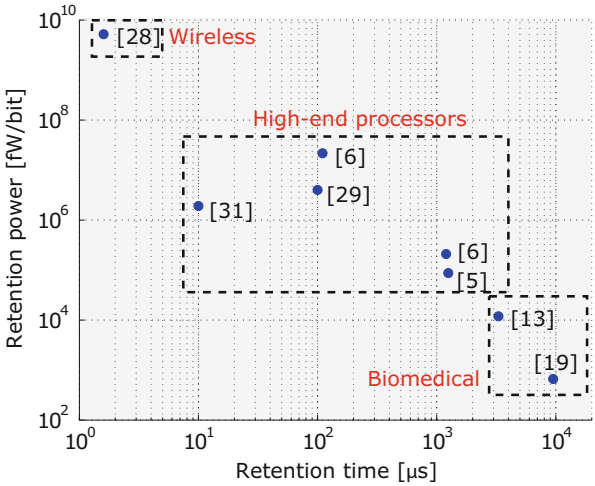


Fig. 2.3 Retention power vs. retention time for several published GC-eDRAM implementations

the values for the wireless and biomedical application domains. Overall, of course, it is clearly visible that enhancing the retention time is an efficient way to lower the retention power.

The *area cost per bit* (ACPB) is defined as the silicon area of the entire memory macro (including peripheral circuits), divided by the storage capacity. As opposed to the simple bitcell size metric, ACPB accounts for the area overhead of peripheral circuits and is a more suitable metric to compare different memory implementations. Moreover, we define the *array efficiency* as the bitcell size divided by the ACPB; note that the array efficiency is a technology-independent metric. Figure 2.4 shows the comparably higher ACPB of biomedical GC-eDRAMs due to the use of a mature 180 nm CMOS node. However, despite their small storage capacity requirements, these implementations achieve a high array efficiency of over 0.5, by using small, yet slow, peripheral circuits [19]. As opposed to this, all GC-eDRAMs targeted at processors, wireless communications, and SoC applications achieve array efficiencies below 0.5, meaning that over half of the area of those macrocells is occupied by peripheral circuits.

2.3.3 Circuit Techniques for Target Applications

GC-eDRAMs have been shown to be an attractive alternative to traditional SRAM arrays for large caches in high-end processors, wireless communication systems, and ultra-low power VLSI systems. Hereinafter, the circuit techniques used in these GC-eDRAM implementations are presented and related to their respective target metrics.

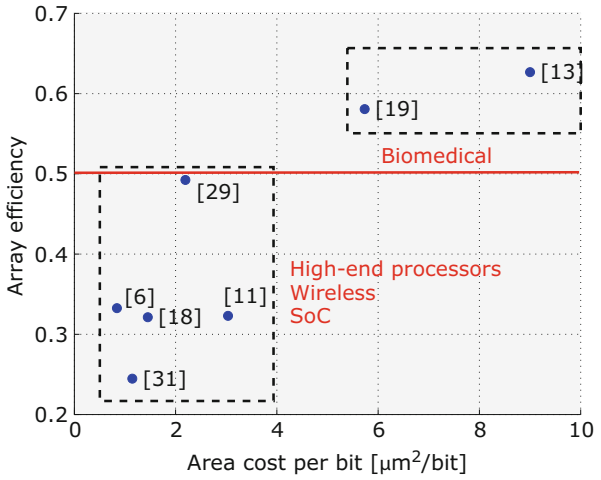
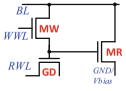
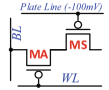
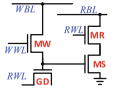
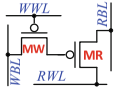
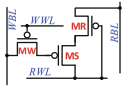
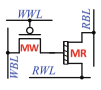


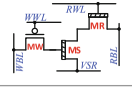
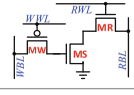
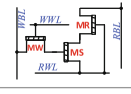
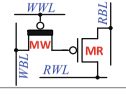
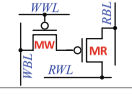
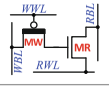
Fig. 2.4 Array efficiency vs. area cost per bit (ACPB) for several published GC-eDRAM implementations

2.3.3.1 Gain-Cell Topologies

An extensive comparison between recent GC topologies is presented in Table 2.1. A common feature of all these circuits is their reduced transistor count, as compared to traditional SRAM circuits. The highest device count appears in [22], comprising three transistors and a "gated diode" (MOS transistor acting as storage device and amplifier for the cell voltage), with all other proposals made up of three [2, 3, 5, 11, 18, 20, 21, 23, 28] or two [6, 13, 19, 24, 26, 29–31] transistors. The obvious implication of the transistor count is the bitcell area; however, the choice of the topology is application dependent, as well. The simple structure of the 2T topologies usually includes a write transistor (MW) and a combined storage and read transistor (MR). Transistor MW connects the write bit-line (WBL) to the storage node (SN) when the write word-line (WWL) is asserted, and transistor MR amplifies the stored charge signal by driving a current through the read bit-line (RBL) when the read word-line (RWL) is asserted. The 2T structure results in capacitive coupling effects between the control lines (WWL, RWL, RBL) and the SN, which can affect the data integrity and degrade performance. Therefore, a third device is often added, primarily to avoid disturbing capacitive couplings from the RWL onto the SN and to reduce RBL leakage. These 3T GC configurations give up some of the density advantage of 2T GCs for the benefit of enhanced speed performance, robustness, and/or retention time. The boosted 3T topology of [5] utilizes the capacitive coupling effect to extend the retention time by connecting the drain of MR to RWL, rather than ground, thereby negating some of the positive SN voltage step inherent to the PMOS MW configurations. Interestingly, large cache memory designs [6, 29, 31] prefer the 2T topology at the cost of additional peripheral circuits to retain high speed performance. An interesting choice of the

Table 2.1 Overview of gain-cell circuit techniques according to target applications

Category	High Performance Processor Caches					
Publication	[20, 21, 2]	[29]	[22]	[30, 31]	[3, 5]	[6]
Bitcell						
Tech. Node	0.12 µm, 0.13 µm, 65 nm PTM	0.15 µm	90 nm	65 nm	65 nm	65 nm
Techniques	Gated Diode, Footer Power Gating, Foot Driver	Multi-Level Bitlines, Hybrid open bitline architecture	Gated Diode Sense Amplifier	RBL Clamping, Pipelined Architecture	Boosted 3T, PVT tracking read reference feedback, Regulated WBL	Half Swing WBL, Stepped WWL
Main Design Metric	400 MHz, 70 µs retention, 100 kbit	400 MHz, 100 µs retention, 1 Mbit	up to 2 GHz, 110 µs retention, 40 kbit	2 GHz, 10 µs retention, 2 Mbit	500 MHz, up to 1.25 ms ret., 64 kbit	667 MHz, 110 µs ret., 192 kbit

Category	General SoC		Wireless	Low Power Biomedical Systems		
Publication	[11]	[27, 18]	[28]	[19]	[13]	[23, 25]
Bitcell						
Tech. Node	90 nm	90 nm	65 nm	0.18 µm	0.18 µm	0.18 µm
Techniques	Forced Feedback, Write Echo Refresh	Multi Level Bitcell, PVT Replica Column	Refresh Free, Sequential Decoding	I/O Write Transistor, Low Area Sense Buffer	Low Area Sense Buffer	Hybrid Cell with I/O MW, Sense Buffer
Main Design Metric	V_{DD} =0.5 V, 180 µA ref. power, 5 MHz	2–50 µs retention, 1.45 µm ^{2}/bit density	32× 1 kbit arrays, 700 MHz, 170 ns retention	V_{DD}=0.75 V, up to 306 ms ret., 0.1–1 MHz, 662 fW/bit ret. power	V_{DD}=0.75 V, 3.3 ms retention, 11.9 pW/bit ret. power	V_{DD}=400 mV, over 40 ms ret., 500 kHz

2T topology is used in [24] even though the target application is a small array for ultra-low power (biomedical) systems. In this case, the stacked readout path of the 3T topology proved to be too slow under sub-V_T supply voltages.

2.3.3.2 Device Choices

The majority of today's CMOS process technologies provide several device choices, manipulating the oxide thickness and channel implants to create several threshold voltage (V_T) and maximum voltage tolerance options. Careful choice of the appropriate device (PMOS/NMOS, standard/high/low V_T) can provide orders-of-magnitude improvement in GC performance, as apparent in Table 2.1. PMOS devices typically suffer from lower drive strength than their NMOS counterparts, but have substantially lower subthreshold and gate leakage currents. For most process technologies, the primary cause of storage node charge loss is subthreshold leakage current through MW, and therefore the ultra-low power implementations [19, 24] employ a high-V_T or I/O PMOS to substantially extend the retention time. In addition to subthreshold leakage, gate leakage current is substantial in thin oxide CMOS technologies. Therefore, the all-PMOS 2T configuration [31] balances the subthreshold and gate leakage currents out of and in to the SN to improve retention time. The decoder system of [28] requires high speed performance with very short retention times, and therefore, an all NMOS low-V_T circuit is used. Low-V_T devices are used in the readout path of several other publications [6, 11] in order to improve the read speed without increasing the static power, since there is a zero drain-to-source voltage drop across MR during write and standby cycles.

The device choices affect the capacitive couplings to and charge injection onto the SN. The MW device type significantly affects the initial voltage level of the SN, depending on several factors. A PMOS write transistor passes a weak "0," and an NMOS passes a weak "1"; therefore, an underdriven (for PMOS MW) or boosted (for NMOS MW) WWL voltage is necessary to pass a full voltage level to the SN. However, the larger the WWL voltage swing is, the larger the capacitively coupled voltage step on the storage node during WWL de-assertion. A PMOS MW is cut-off by the rising edge of WWL, resulting in both capacitive coupling and charge injection to the SN. Therefore, the initial "0" value will always be significantly higher than ground for a PMOS MW. Similarly, the initial "1" value will always be significantly lower than V_{DD} for an NMOS write transistor. This limits the SN voltage range and degrades the overdrive of MR during readout, as well as the retention time. In a 2T GC, using the same device option for MR as for MW induces an additional voltage step in the same direction during read access, further impeding the performance. A hybrid cell, mixing NMOS and PMOS transistors [6, 11, 18, 23, 24], can be used to combat these effects, at a small area overhead for two different wells within each bitcell.

2.3.3.3 Peripheral Circuit Techniques

In addition to the choice of a GC topology and device options, several peripheral circuit techniques have been demonstrated to further improve system performance according to the target application. One simple and efficient technique is the employment of a sense buffer in place of a standard sense amplifier (SA) in low-power systems [13, 19, 24]. This implementation requires a larger RBL swing, trading off speed for area and process, voltage, temperature (PVT) sensitivity. The area trade-off is apparent in Fig. 2.4 as [19] shows exceptionally high array efficiency. Several other SA configurations have been demonstrated to deal with various design challenges. Chun et al. [6] overcome the problem of small RBL voltage swing by using a current mode SA featuring a cross-coupled PMOS latch and pseudo-PMOS diode pairs. Other SA designs include p-type gated diodes [20–22], offset compensating amplifiers [29], single-ended thyristors [28], and standard latches [31]. The most complex sensing scheme is used for multilevel GCs in [18, 23]: a successive approximation sensing scheme deciphers the four data levels.

Several publications [11, 13, 19, 24] discharge WBL during non-write operations to extend retention time that is worse for a stored "0" than a "1" with a PMOS WM. A "write echo refresh" (WER) technique was employed by Ichihashi et al. [11] to further reduce the WBL="1" disturbance. In this technique, the number of "1" write-back operations during refresh are counted and followed by WER operations (with oppositely biased WBL) to combat the disturbance. The authors of [5] recognized that the steady state level of a "1" and "0" is common (and much closer to "1" than to "0"), so they monitor this level and use it as the WBL voltage for writing a "1." This minimizes the "0" level disturbance without impeding the worst-case "1" level. For the system proposed in [6], WBL switching speed is the performance bottleneck, and therefore, a half-swing WBL is employed, improving the write speed and reducing the write power.

An issue that is rarely discussed in 2T GC implementations is the voltage saturation of RBL during readout. Depending on the implementation of MR, readout is achieved by either charging (NMOS) or discharging (PMOS) RBL. However, once RBL crosses a threshold (depending on the current ratio of the selected bitcell and the number of unselected cells), a steady state is reached. This phenomena not only limits the swing available for RBL sensing, but also causes static current dissipation that is present throughout the entire read operation. This is one of the phenomena which should be considered when choosing the appropriate V_{DD} for a low-power GC-eDRAM. Somasekhar et al. [31] combat this self clamping of RBL by explicitly clamping its voltage with designated devices.

2.3.4 Summary and Conclusions

This chapter reviewed and compared recently proposed GC-eDRAMs, categorizing them according to their target applications and overviewing the characteristics that make them appropriate for these applications. A closer look into the circuit design

of these GC-eDRAMs provided further insight into the methods used to achieve the required design metrics through the use of different bitcell topologies, device options, technology nodes, and peripheral circuit implementations. To summarize briefly, the following best-practice guidelines should be used when designing GC-eDRAMs for future applications:

- High-V_T write access transistors for long retention times and low refresh power, in conjunction with area-efficient sense buffers for high array efficiency are most suitable to meet the storage requirements of ultra-low power (biomedical) VLSI SoCs.
- High-speed applications should use sensitive sense amplifiers to overcome small voltage differences, and should consider the use of low-V_T readout transistors for improved read access speed.
- Systems which frequently update their internal memories can sacrifice GC-eDRAM retention time for the benefits of high-speed access and high bandwidth.

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