The Open Source LSR

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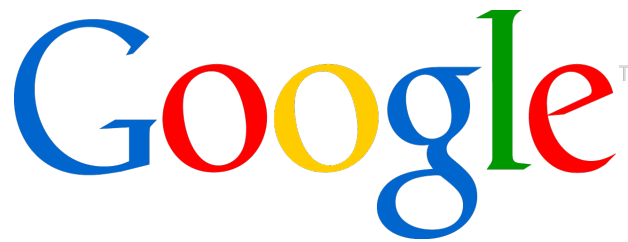


What is an "Open Source LSR"?

- MPLS Label Switching Router
- Running OSPF, LDP
- Hardware Forwarding (4 x 1GigE ports)
- Open Source Software AND Hardware

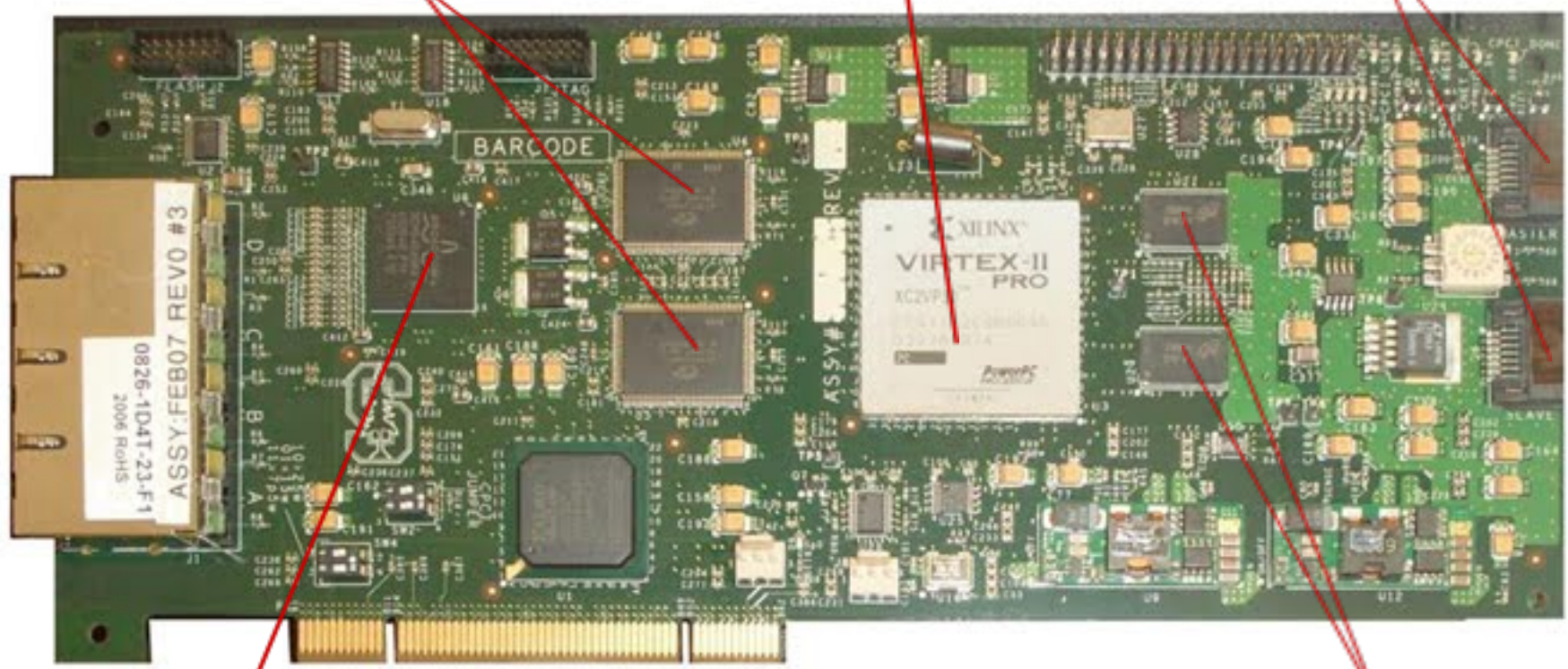
Why build one?

- Most of the parts already exist
- Create community involvement
- Enable interesting network research
- Hardware usually the stopper

Components

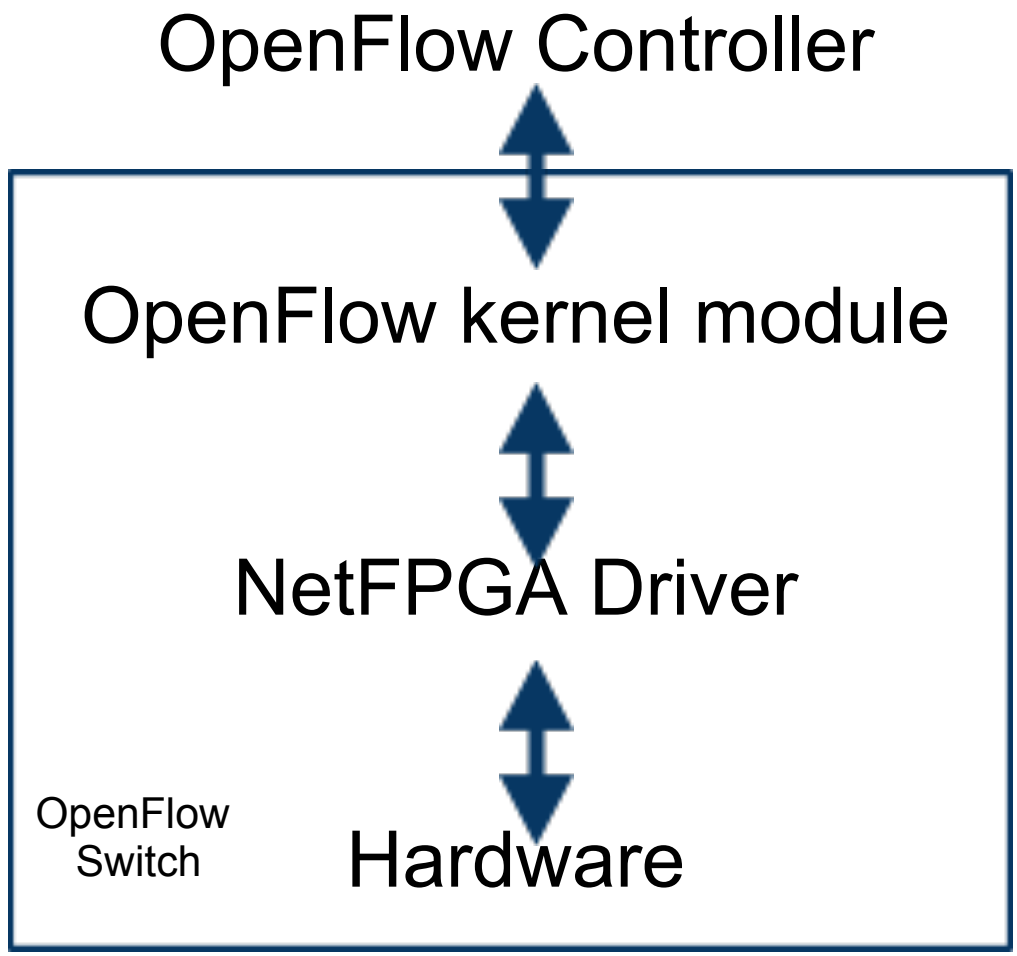
- NetFPGA
- OpenFlow
- mpls-linux
- quagga-ldp
- LSP Synchronizer

Components: NetFPGA



Components: MPLS OpenFlow

Programming the flow table with OpenFlow:



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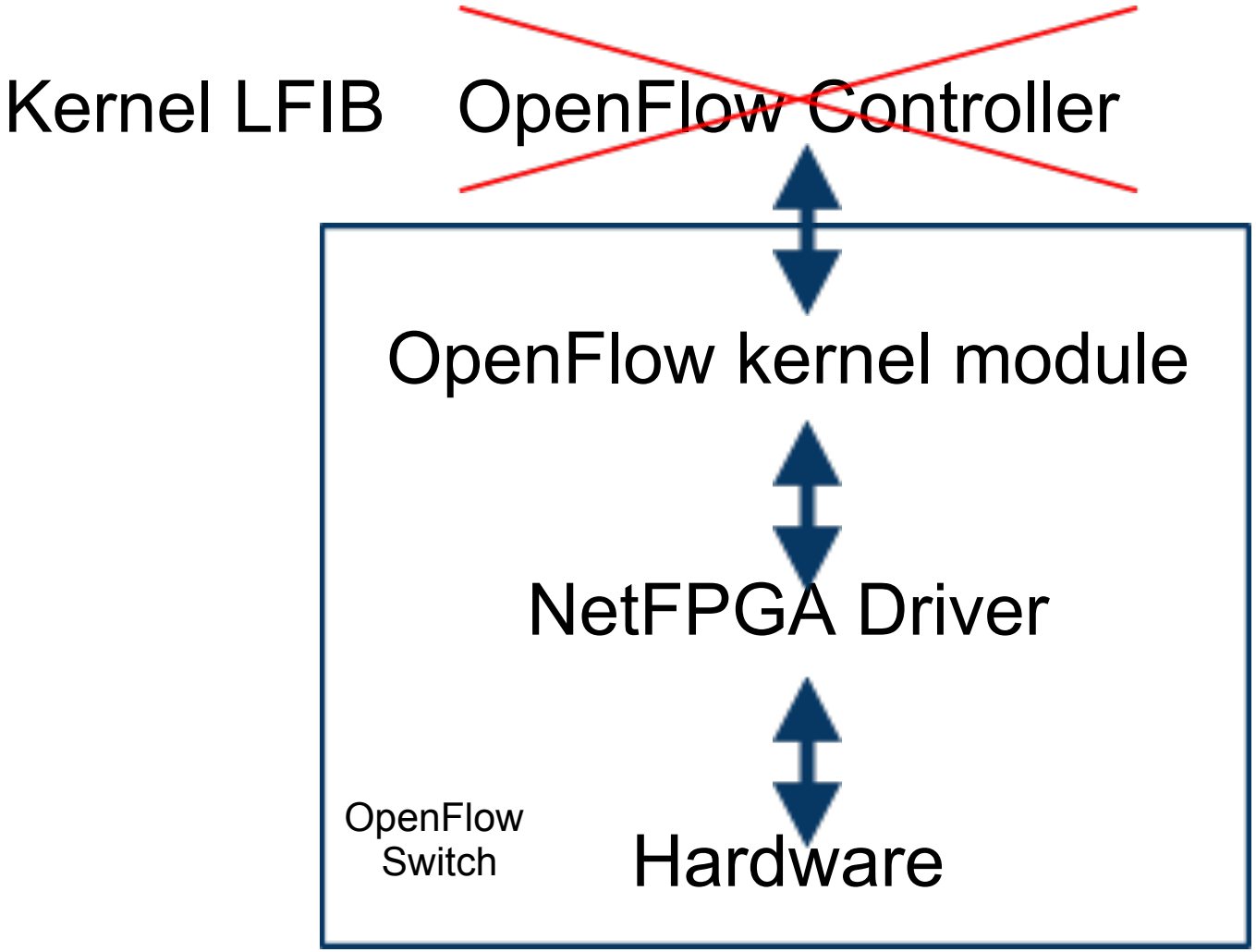
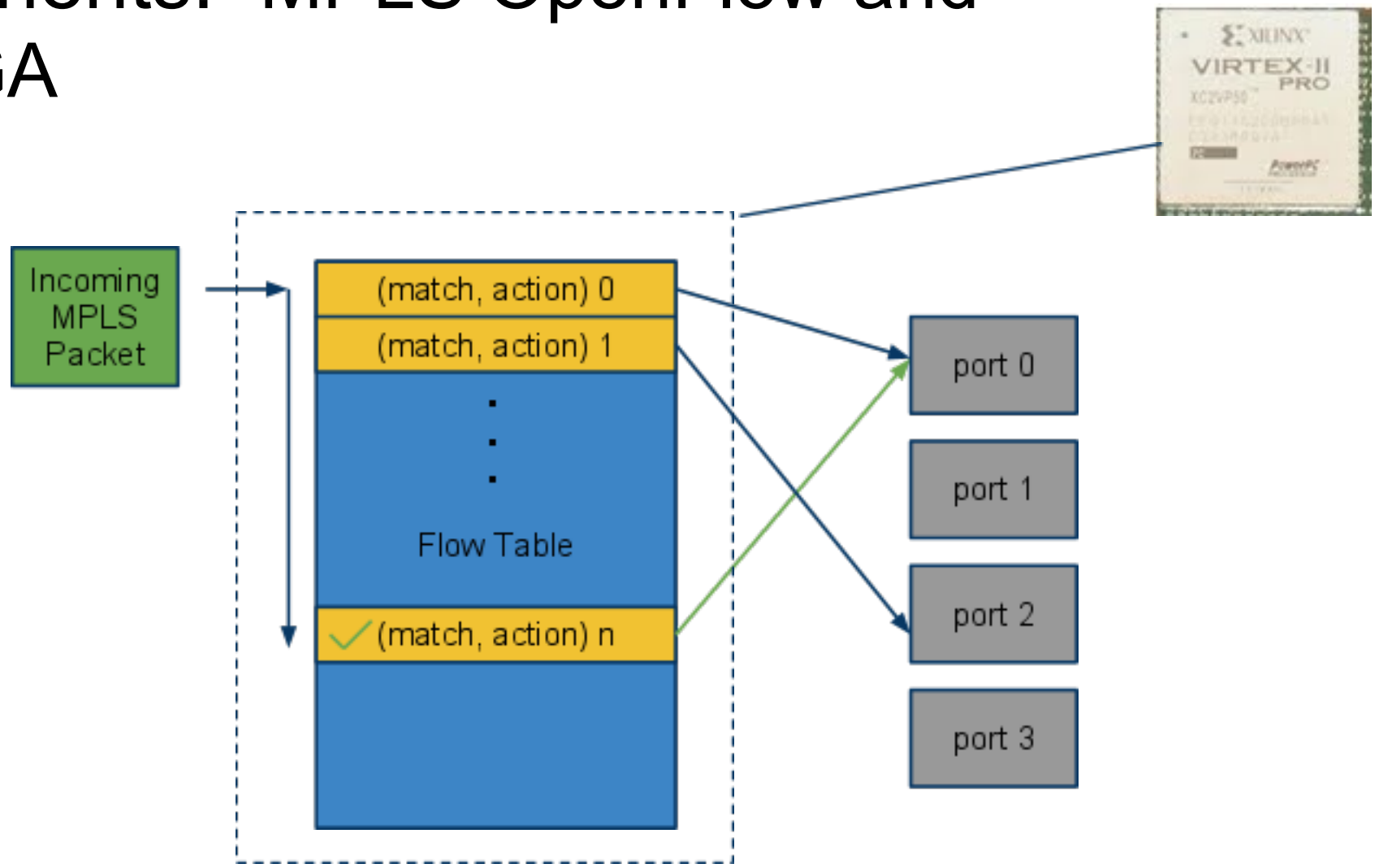


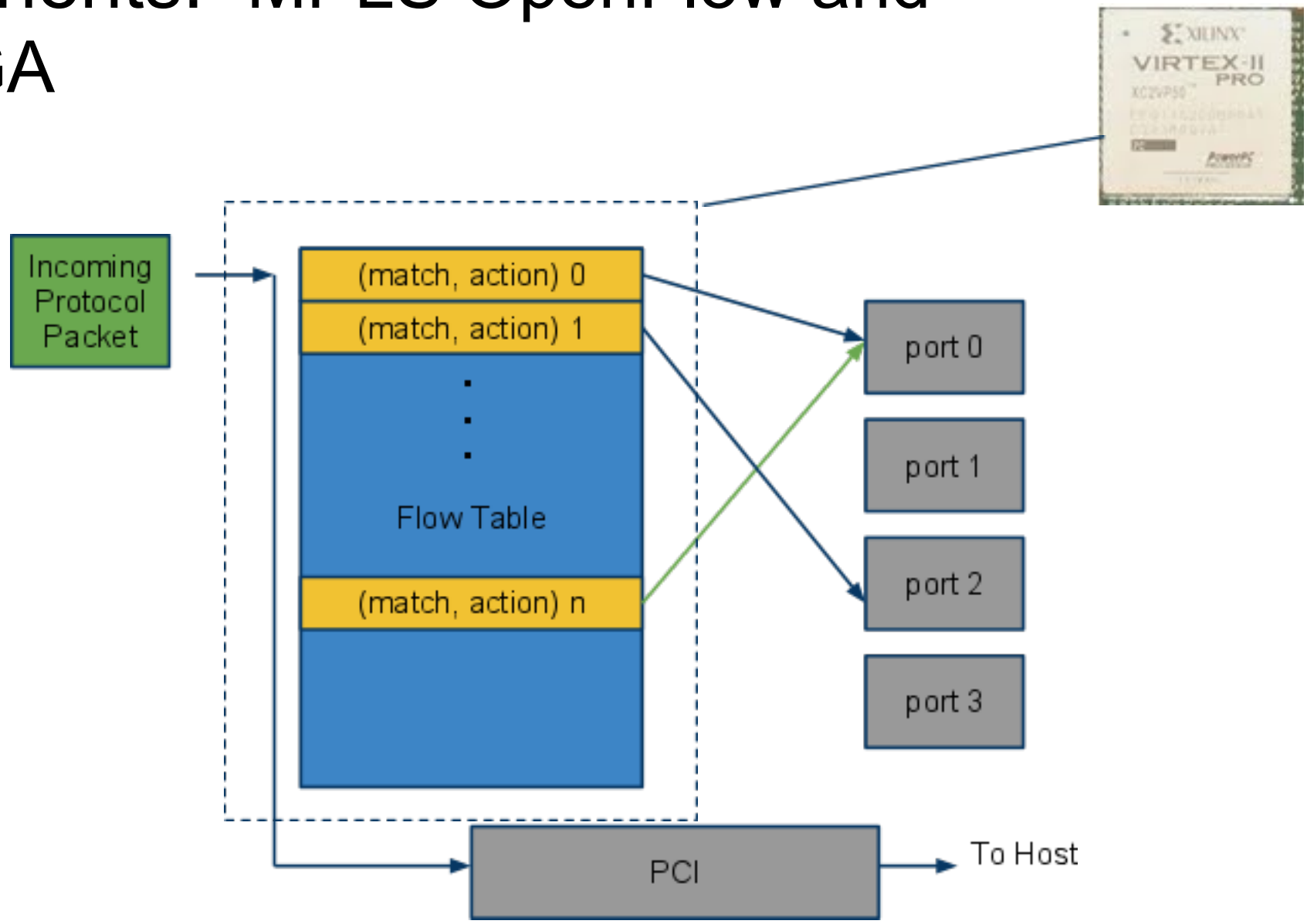
Components: MPLS OpenFlow and NetFPGA



match = match on some MPLS label

action = rewrite label and forward

Components: MPLS OpenFlow and NetFPGA



Packets for host sent to kernel

OSPF, LDP, ssh, etc.

Components: mpls-linux

- Patches for kernel (2.6.32.16)
- Source for building MPLS kernel modules
- Patches for iproute2
  - Updated 'ip' command
  - New 'mpls' command

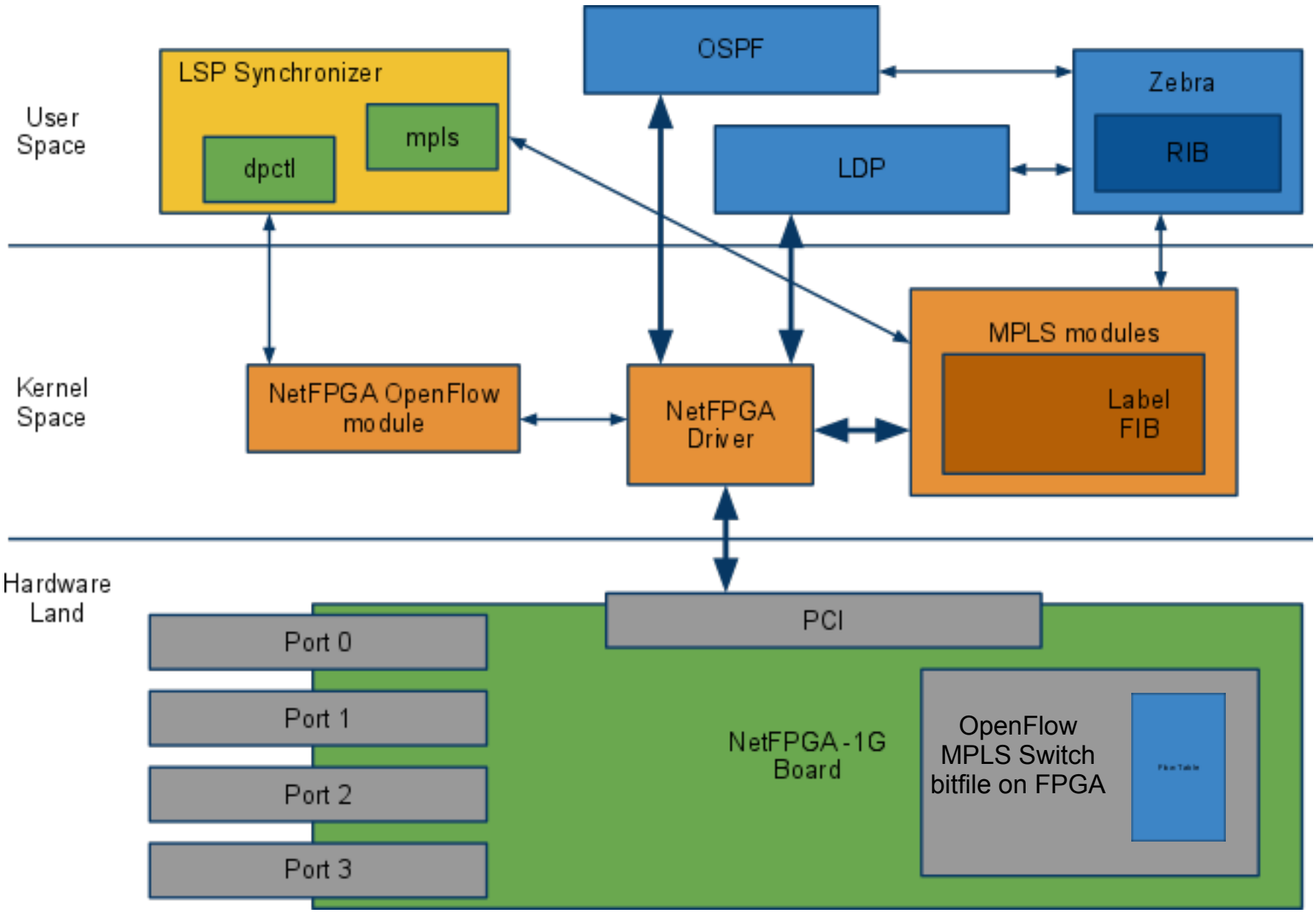
Components: quagga-ldp

- Standard quagga provides OSPF
- This project adds LDP support
- LDP Parameters used:
  - Downstream unsolicited
  - Liberal retention
  - Ordered control

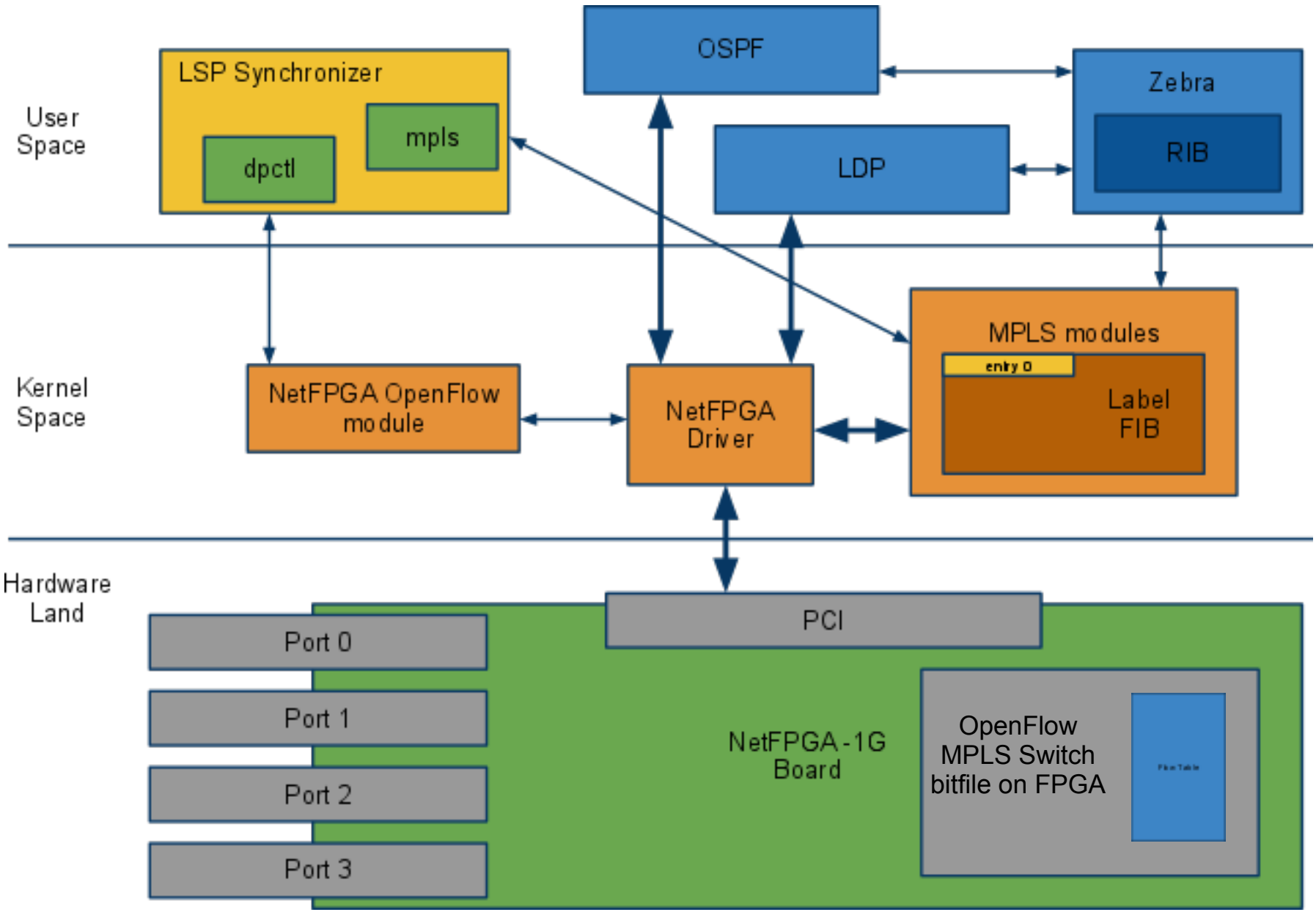
Components: LSP Synchronizer

- quagga provides:
  - labels via ldpd
  - kernel LFIB updates via zebrad
- OpenFlow provides:
  - FIB programming on NetFPGA
- LSP Synchronizer has to:
  - Scan kernel LFIB
  - Compare to FIB on NetFPGA
  - Update FIB as needed

Open Source LSR



Open Source LSR



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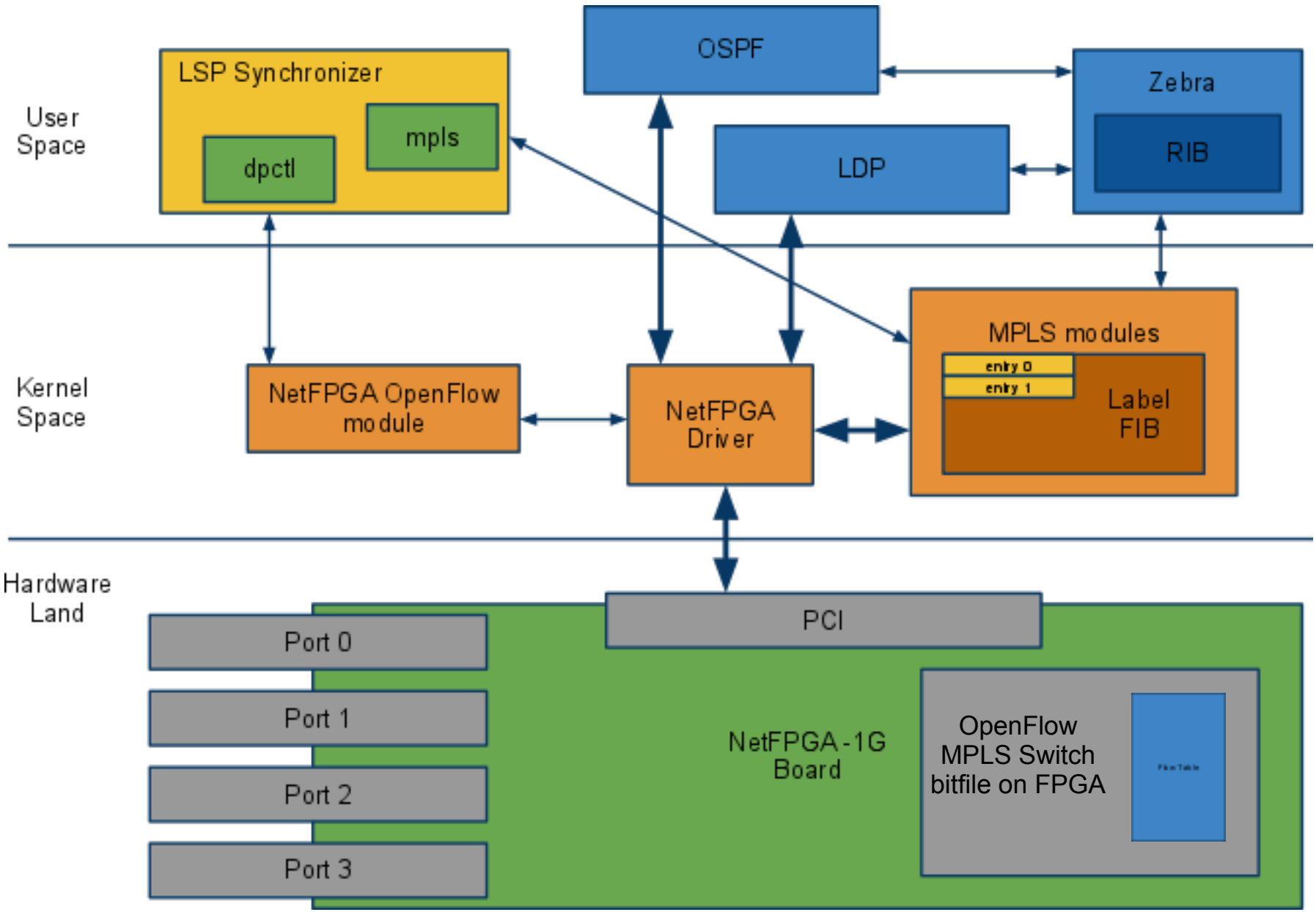

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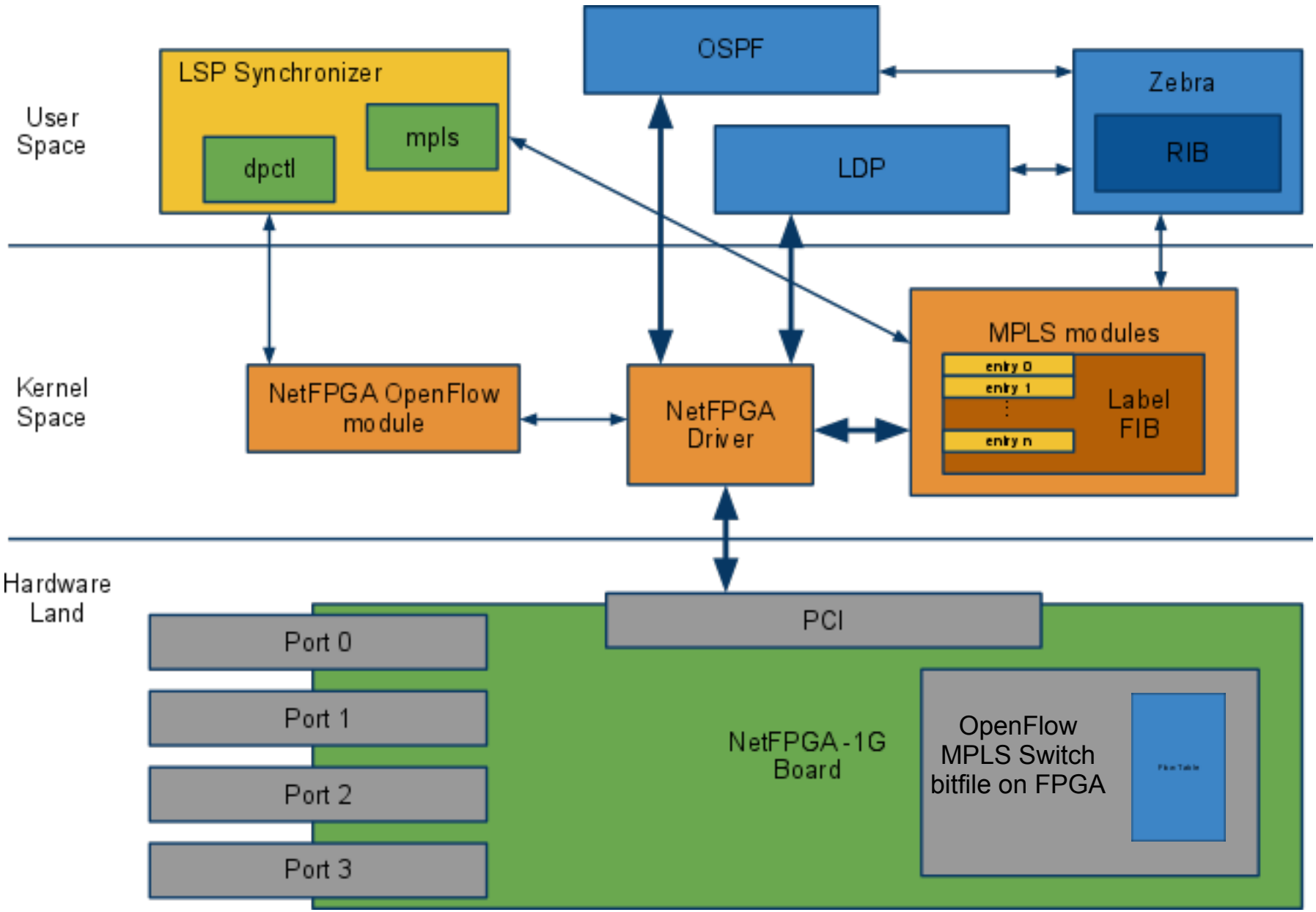

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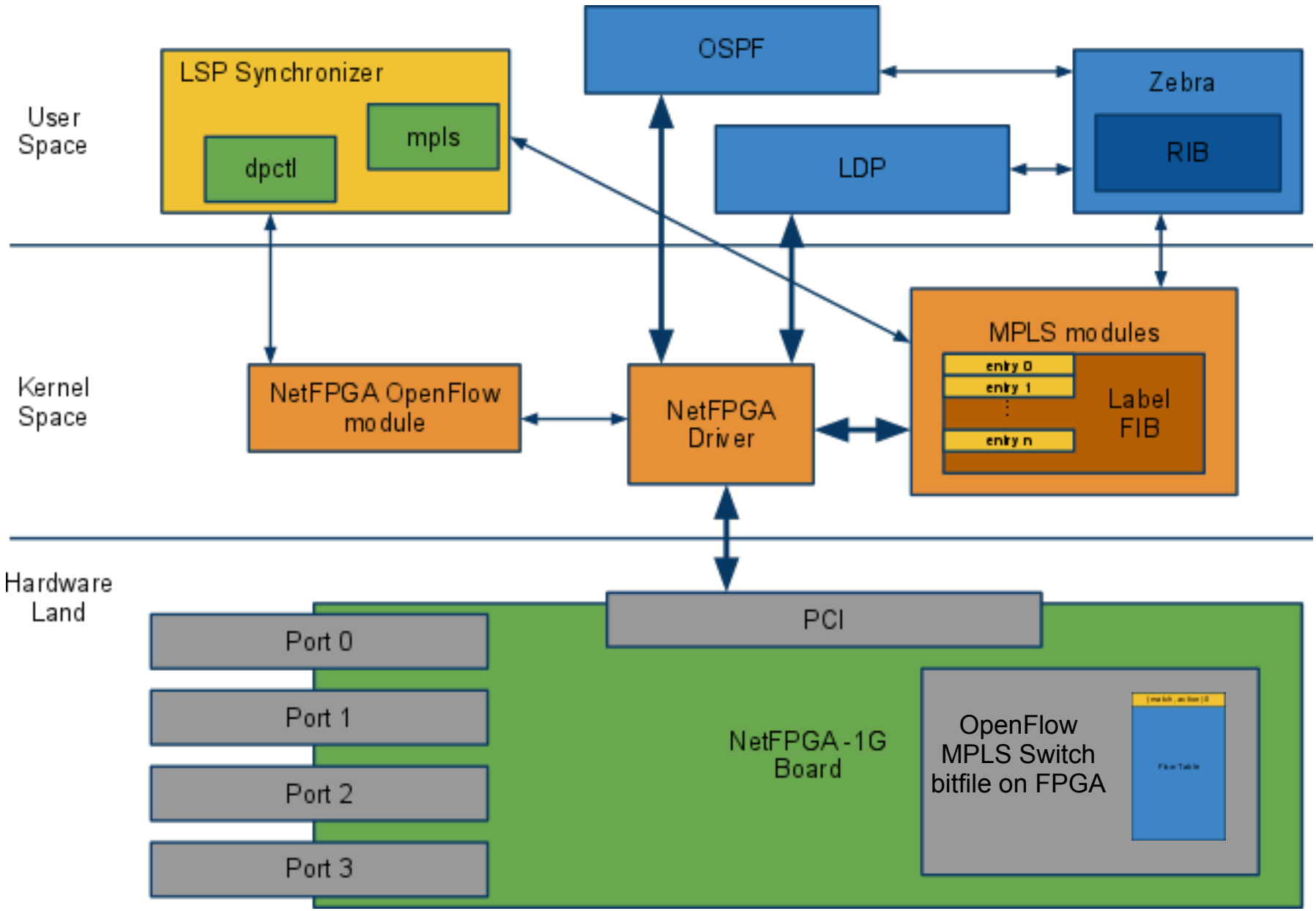

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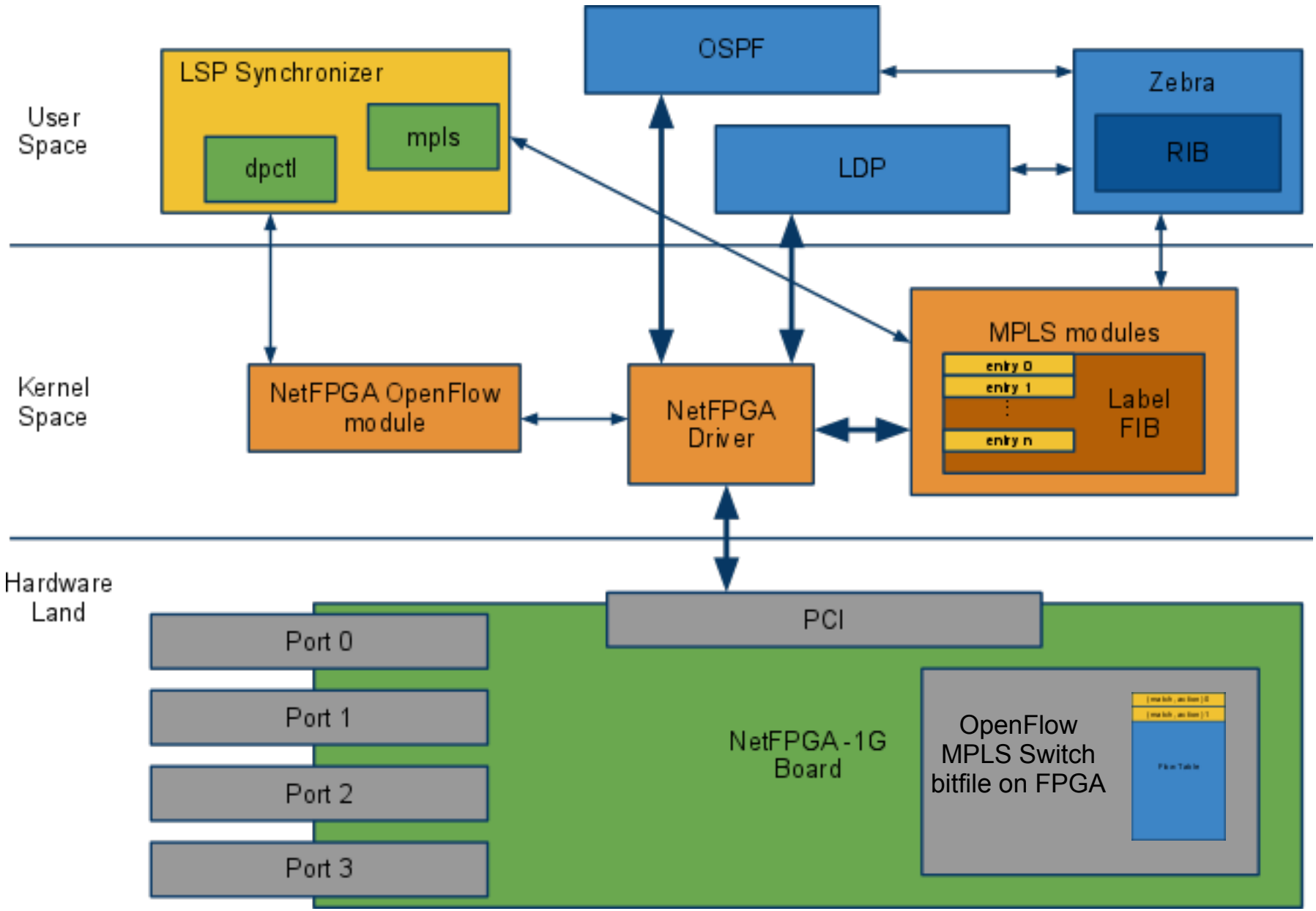

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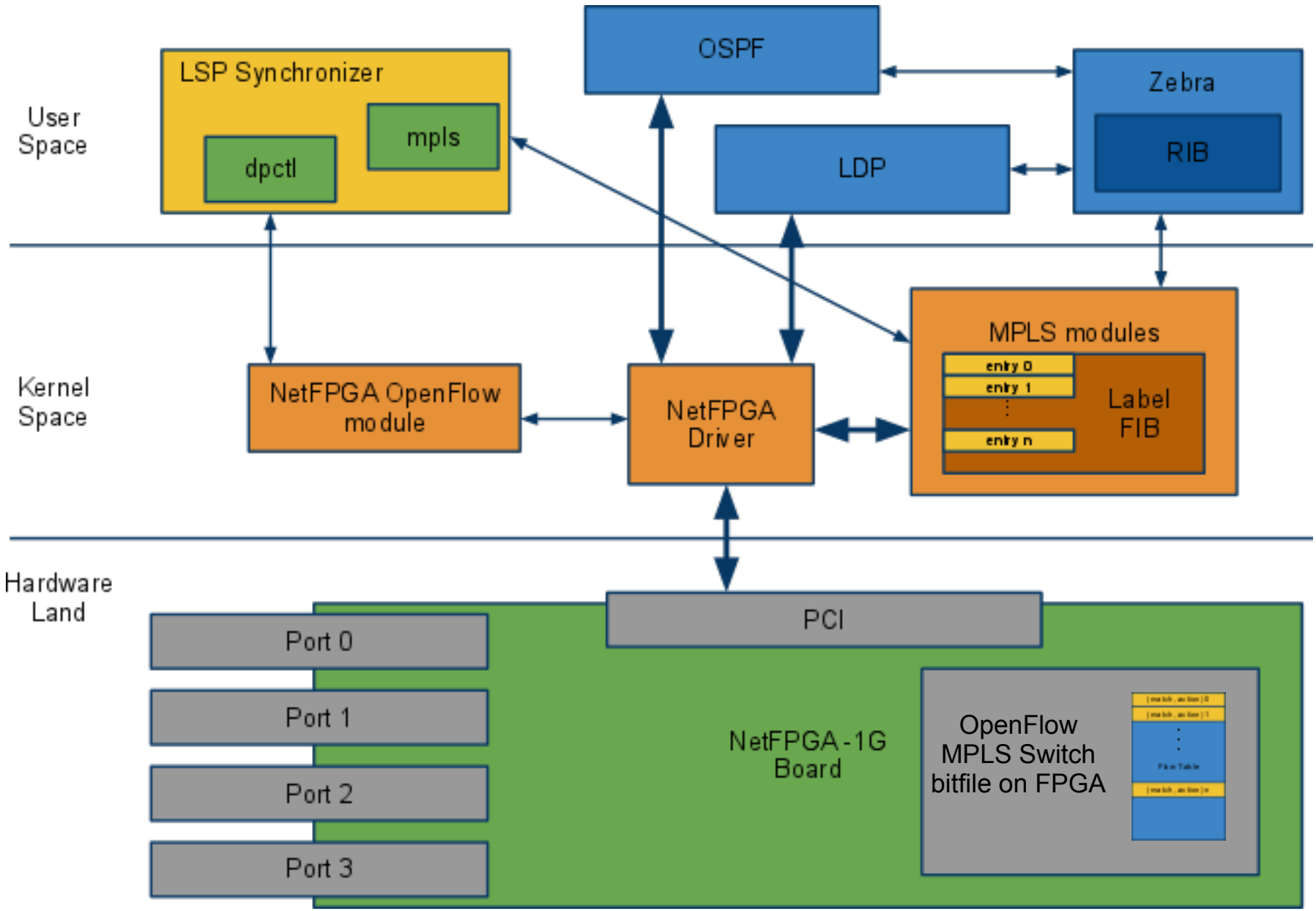
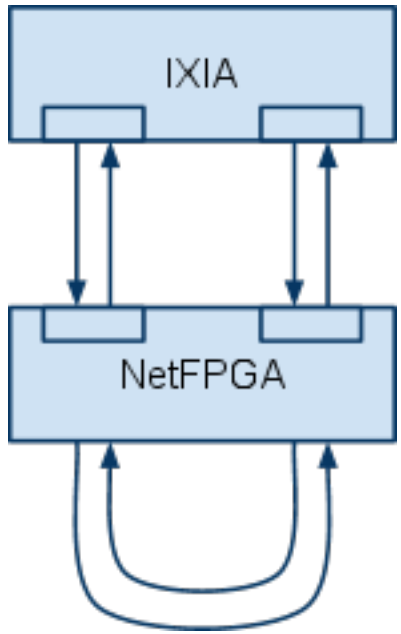
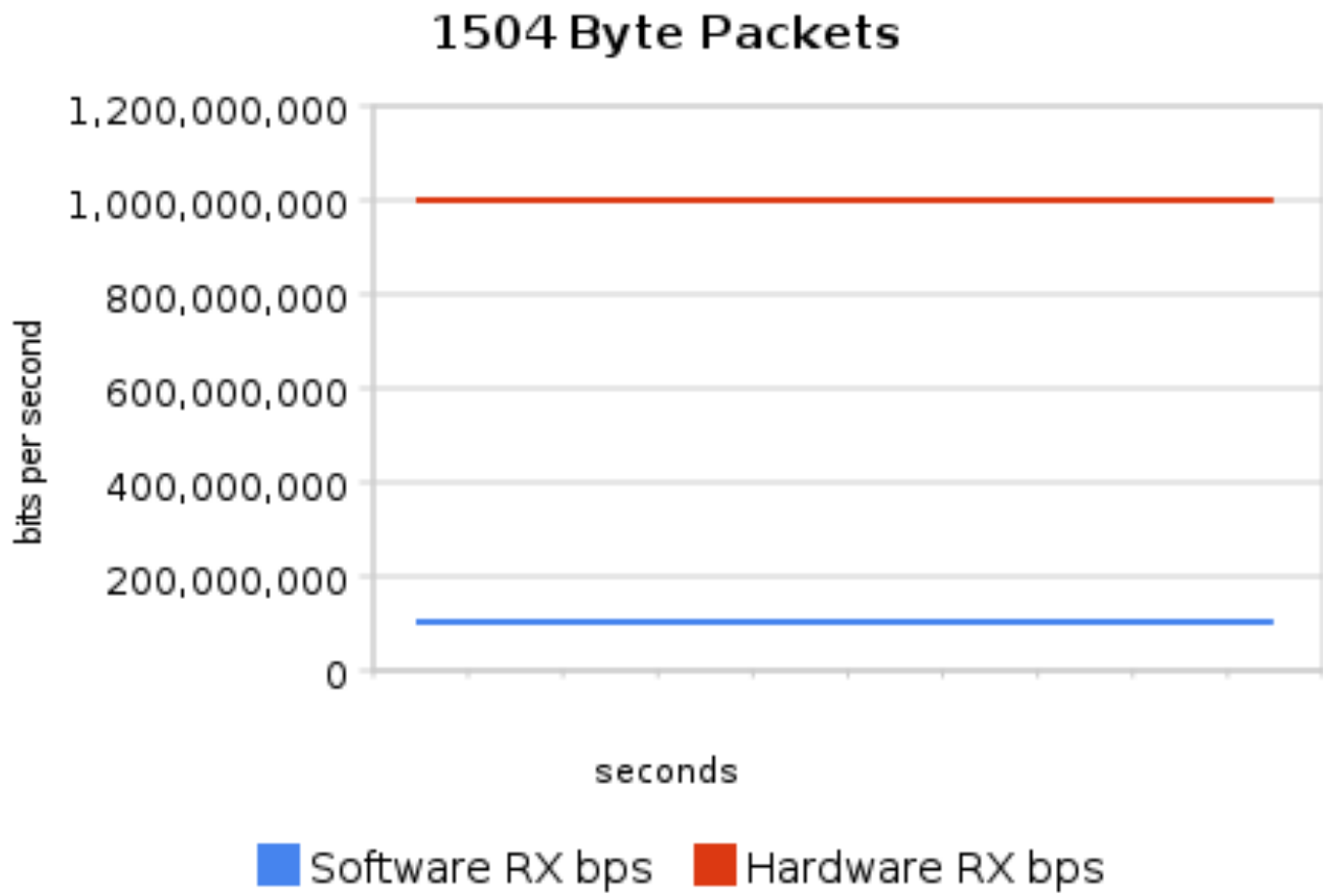


Sofware vs. Hardware Forwarding

- Simple Test
- Bidirectional Throughput
- 68 byte packets
- 1504 byte packets



Software vs. Hardware Throughput



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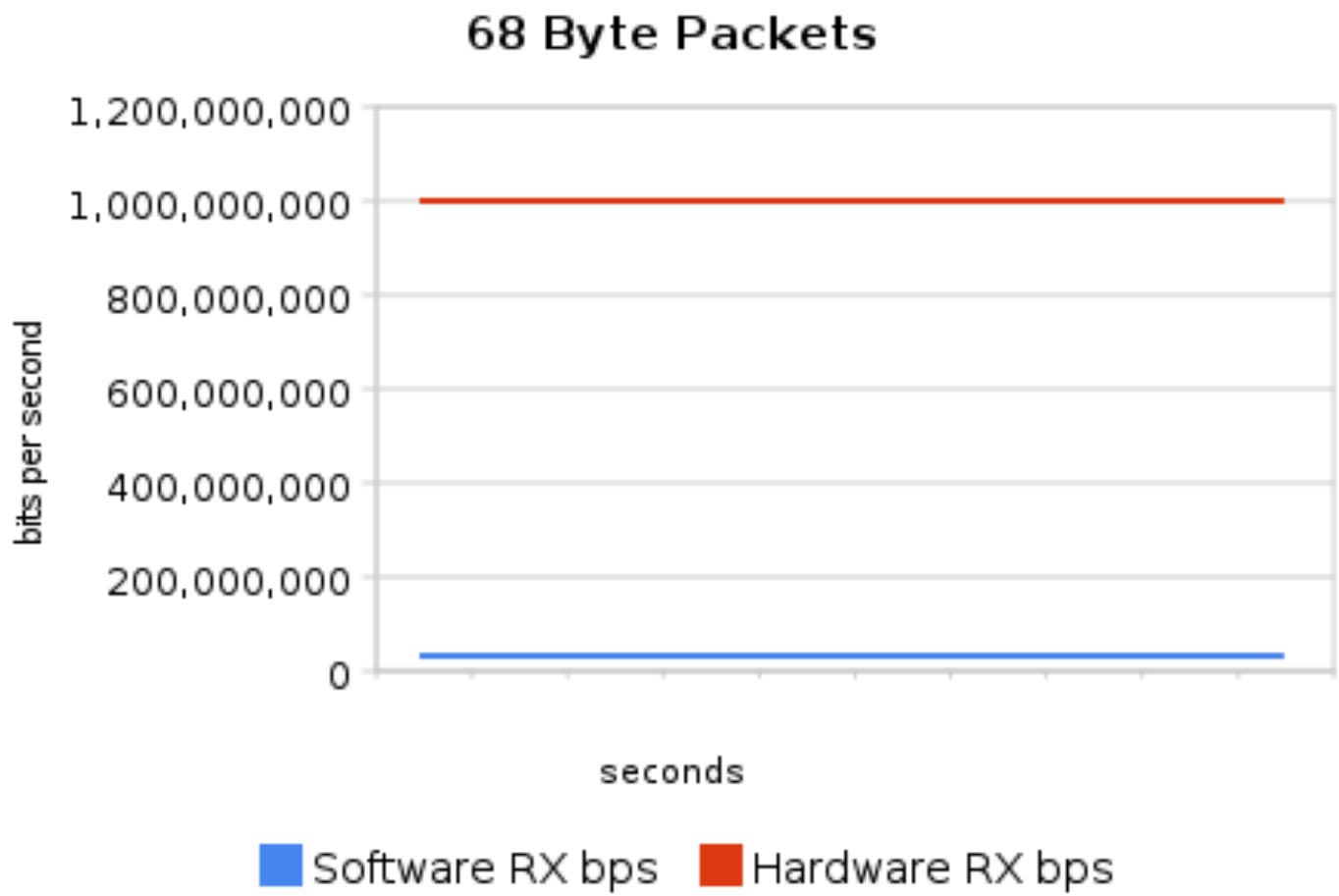
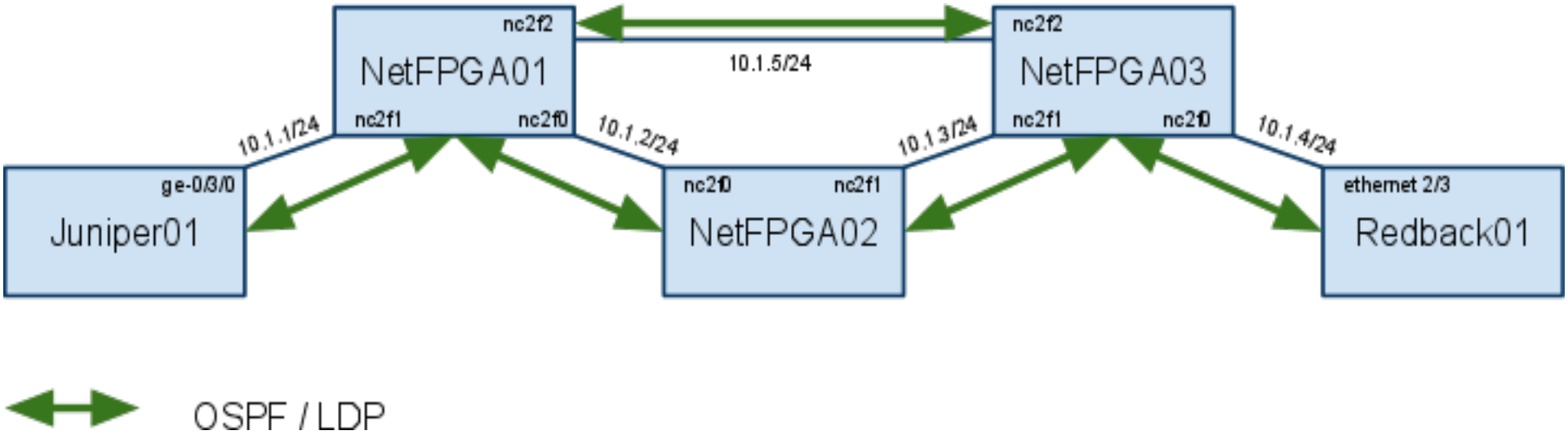
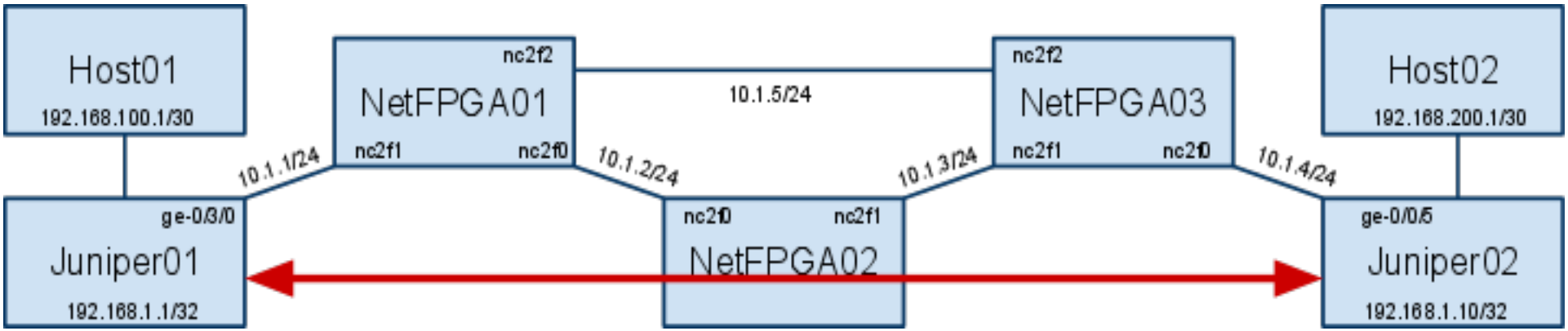


Lab Topology: Verifying MPLS



- OSPF on all devices
- LDP on all devices
- Juniper M10
- Redback SmartEdge100

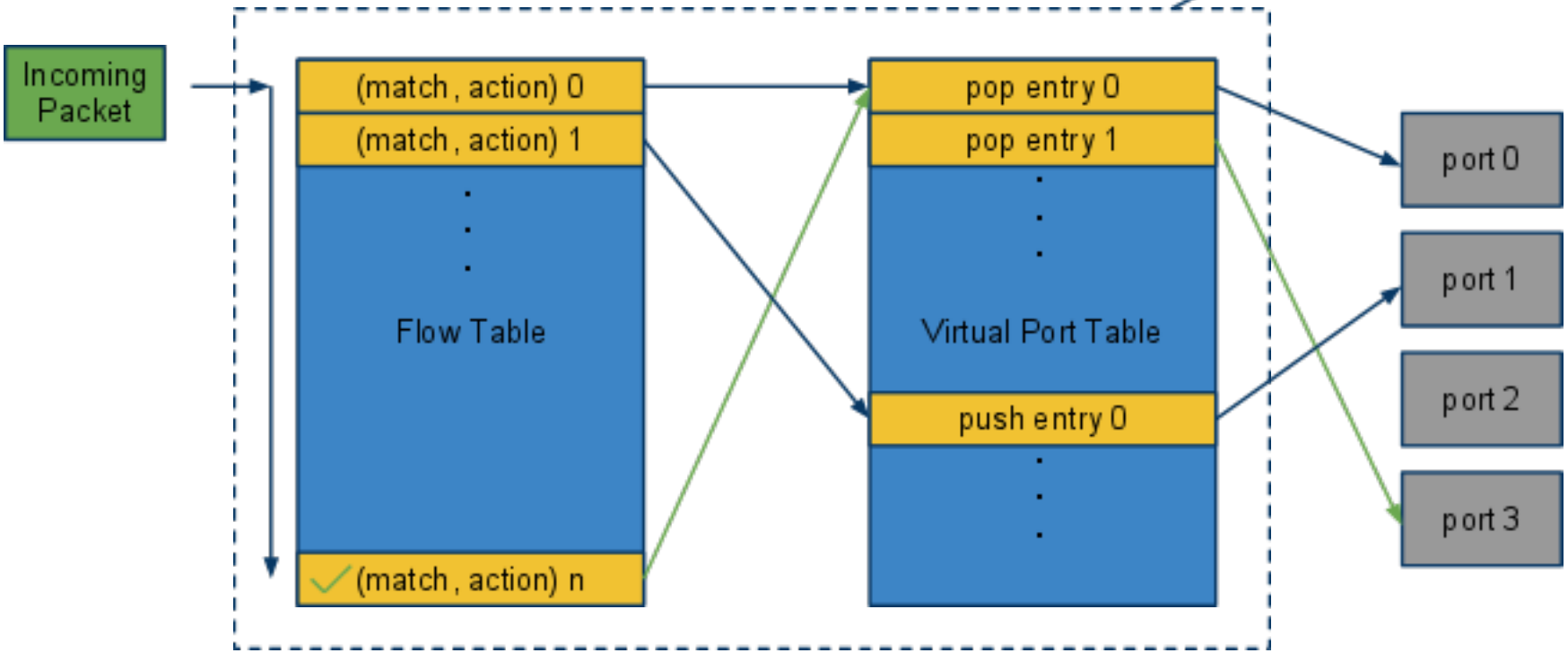
Lab Topology: BGP-free core



- OSPF on all devices
- LDP on all devices
- Juniper M10s as LERs
- iBGP across LSRs

LER?

Hardware allows popping and pushing too...



Future Work

- Near-term
  - Bugfixes
  - 64-bit Linux kernel
  - Port to BSD
  - RSVP-TE support in Quagga
  - 10G NetFPGA card

- Medium-term
  - Centralized control plane via an OpenFlow controller
  - BGP-free core design based on open-source LSRs

Download!

- This project tarball
  - http://code.google.com/p/opensource-lsr/

- Open-source projects integrated in this project
  - mpls-linux
    - http://repo.or.cz/w/mpls-linux.git
  - quagga-ldp
    - http://repo.or.cz/w/jleu-quagga.git
  - NetFPGA / OpenFlow with MPLS support
    - http://netfpga.org/foswiki/bin/view/NetFPGA/OneGig/ProjectsOpenFlowMPLSSwitch
    - http://openflowswitch.org/wk/index.php/OpenFlowMPLS_NetFPGA_Switch

Credits

- The Open Source Projects
  - mpls-linux
  - quagga-ldp
  - OpenFlow-MPLS
  - NetFPGA
- LSP synchronizer, debugging - Jonathan Ellithorpe
- Lab Testing - Richard Hay
- Overall Concept - Stephen Stuart