Coral Dev Board: Baseboard Cover Page

Table of Content

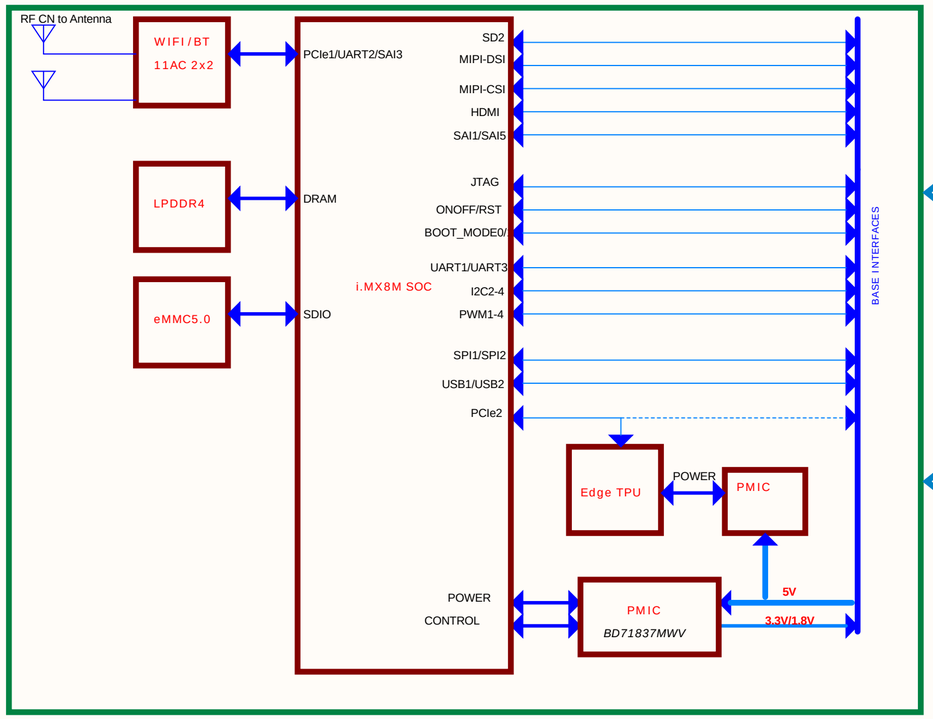
Revision History

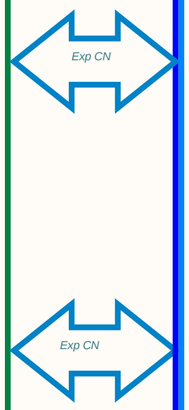
Rev. Code	Date	By	Description
PVT	*2019-08-12*	*Bangfei Pan*	*Clean up the schematic.*

Project:	*Coral Dev Board: Baseboard*	Google LLC 1600 Amphitheatre Parkway Mountain View, CA 94043
Engineer: Bangfei/Michael/Leo	Revision: PVT	
Date: 8/12/2019	Sheet 1 of 11	
File: 01_COVER.SchDoc		

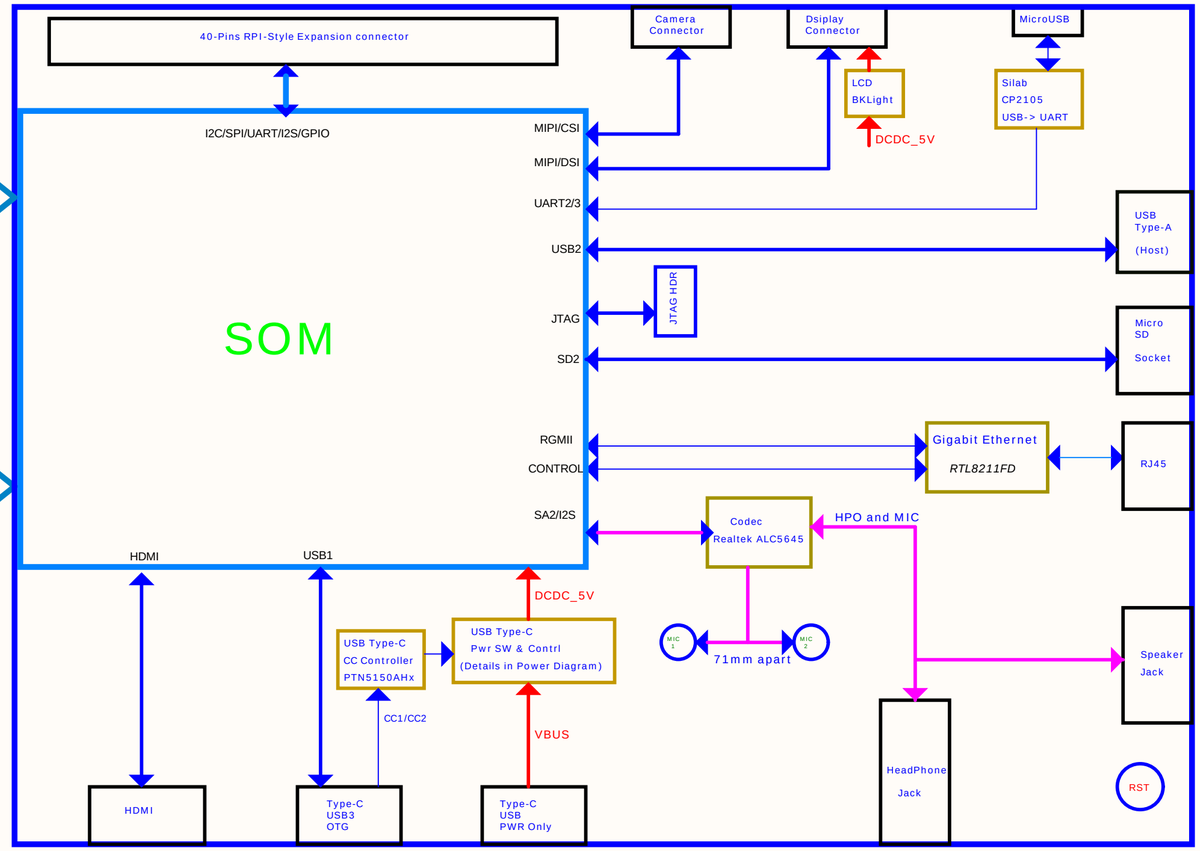
Coral Dev Board Block Diagram

SOM





BASEBOARD



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Engineer: Bangfei/Michael/Leo		Revision: PVT	
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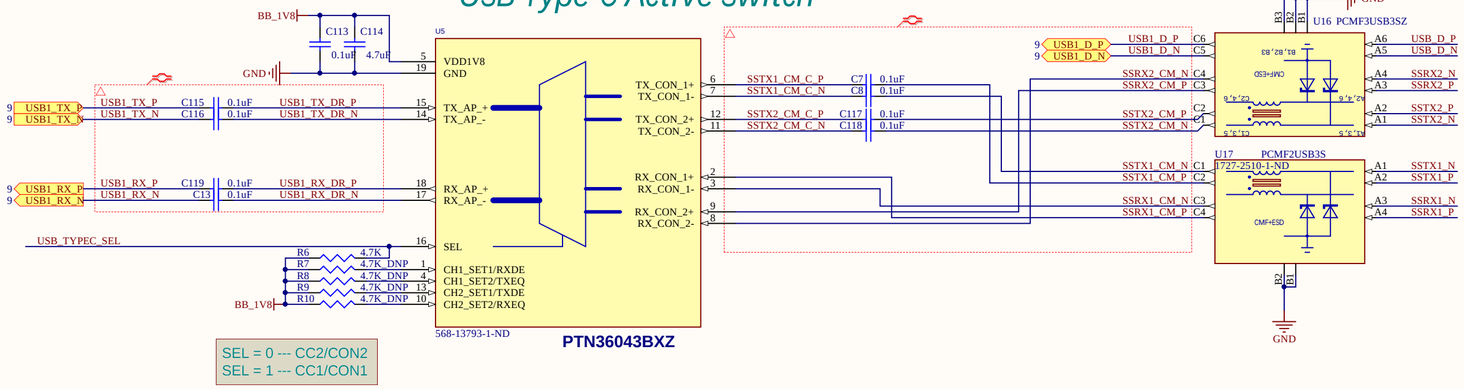
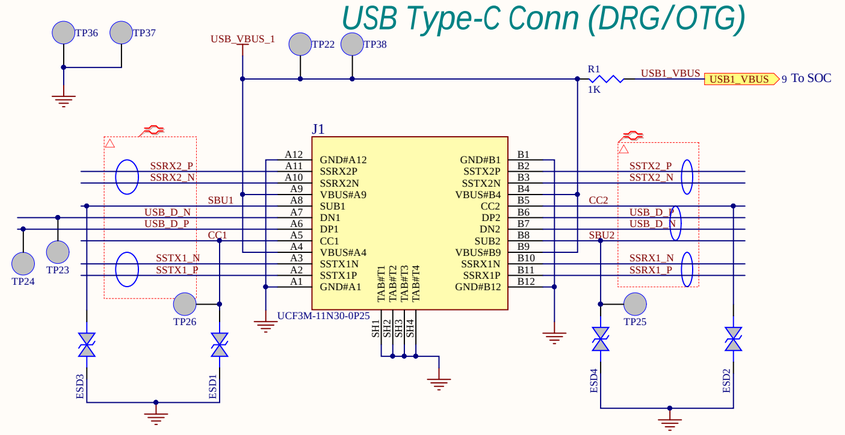
File: 02_BLOCK_DIAGRAM.SchDoc			

USB3.0/2.0 TYPE-C/HOST

USB Type-C Active Switch

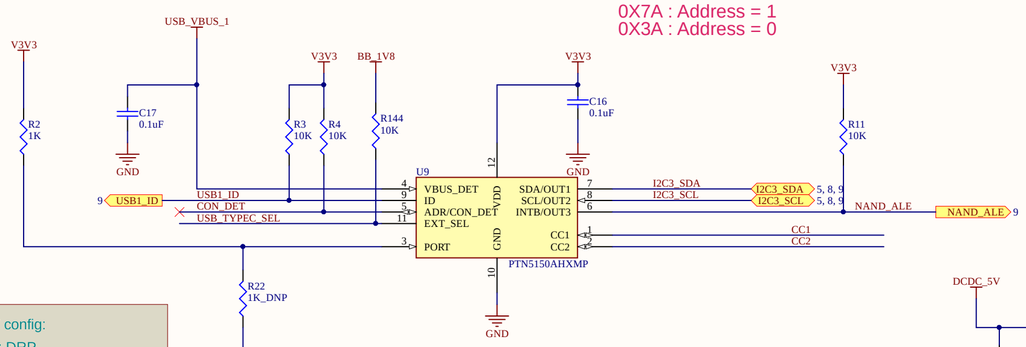


USB Type-C Conn (DRG/OTG)



USB Type-C CC Logic

0X7A : Address = 1
0X3A : Address = 0



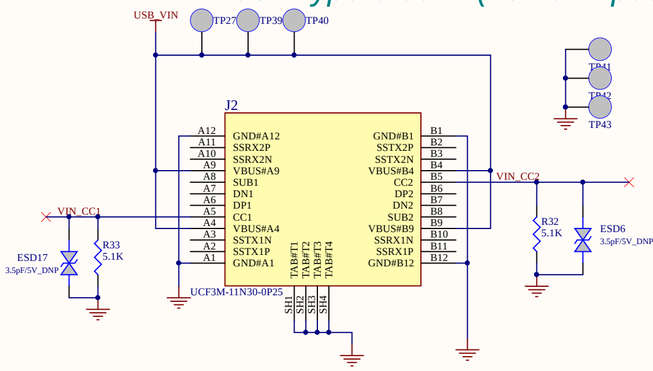
PORT config:
Hi-Z: DRP
Low: UFP
High: DFP

Current Mode detection (as device):
Default: <0.5A/0.9A
Midium: <1.5A
High: <3.0A

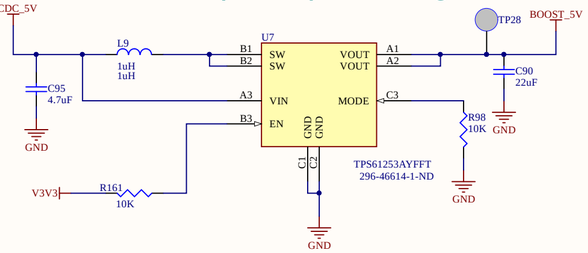
USB_ID=Low for DFP mode detected.
Host mode, plus enable VBUS to device.

EXT_SEL:
LOW= CC2 Orientation.
High= CC1 Orientation
Or no Valid CC1/CC2 detection.

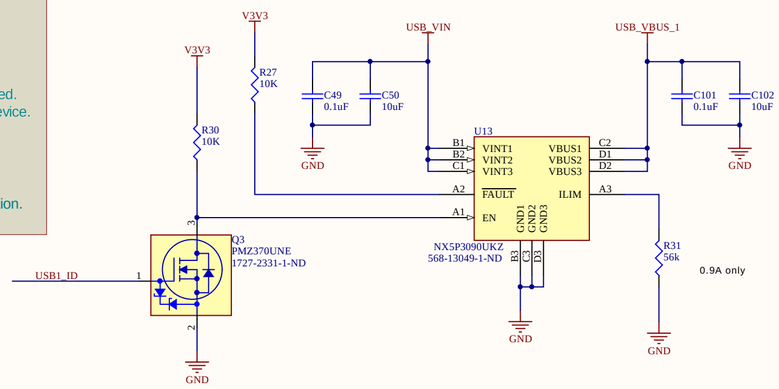
USB Type-C Conn (Power Input ONLY)



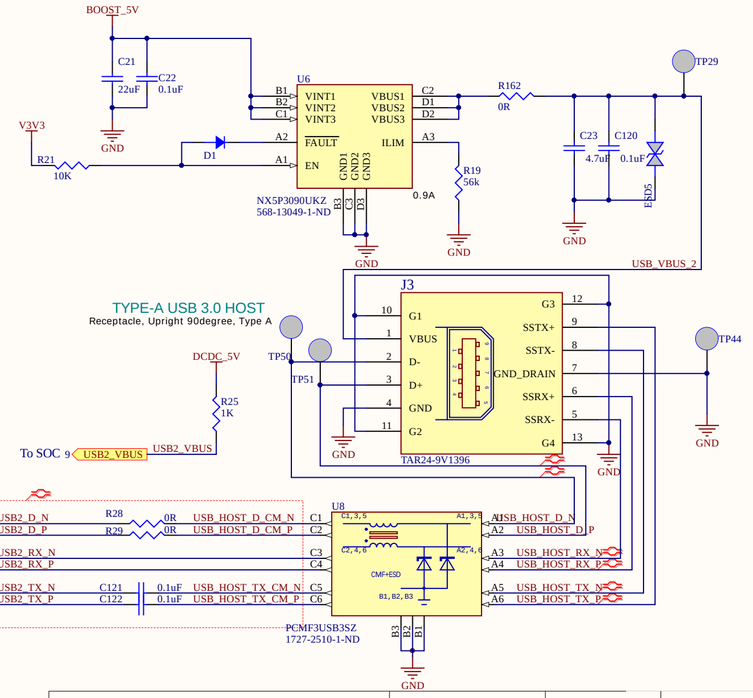
Diode-drop-compensating Boost



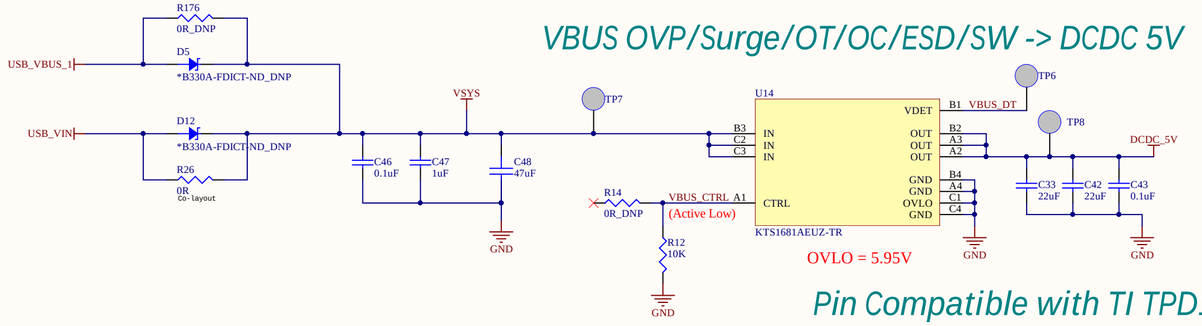
USB-C Power Delivery & Current Limiter



USB Type-A Conn (Host and PWR OUT)



VBUS OVP/Surge/OT/OC/ESD/SW -> DCDC 5V



Pin Compatible with TI TPD1S514-1

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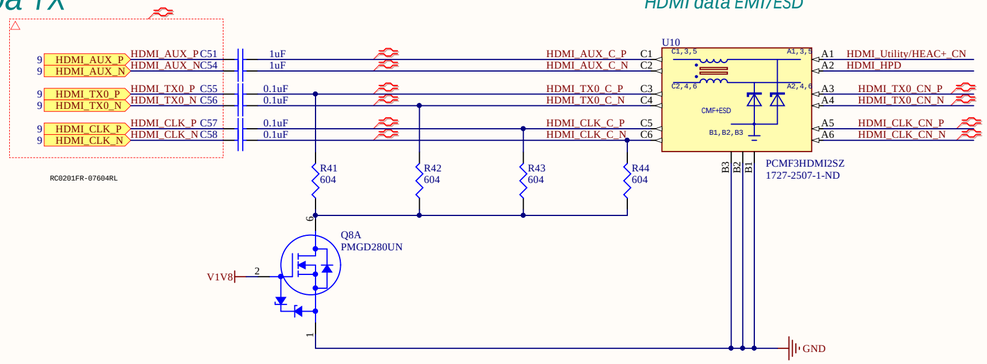
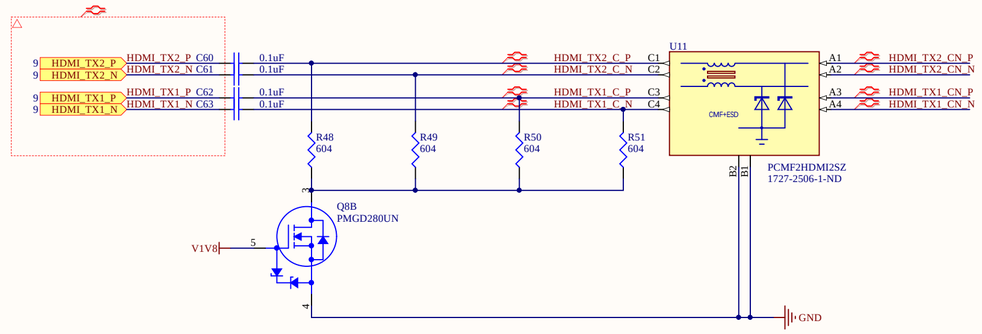
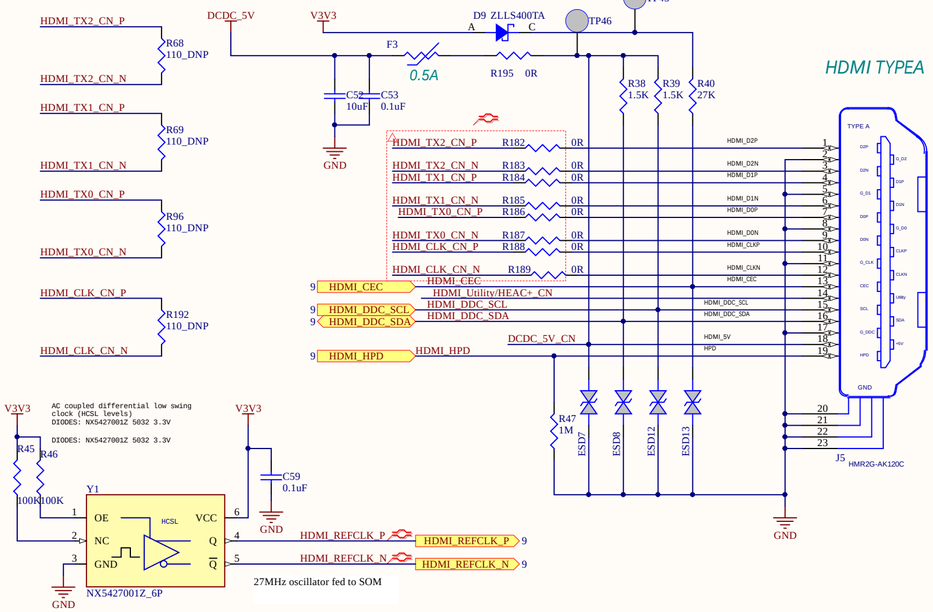
HDMI 2.0a TX

HDMI data EMI/ESD

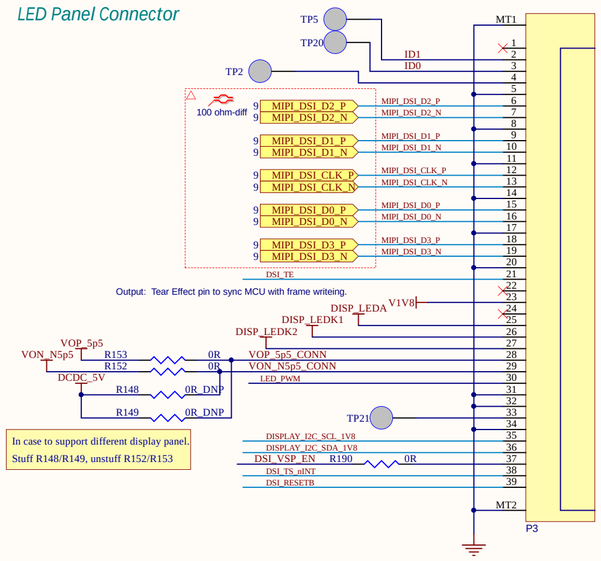


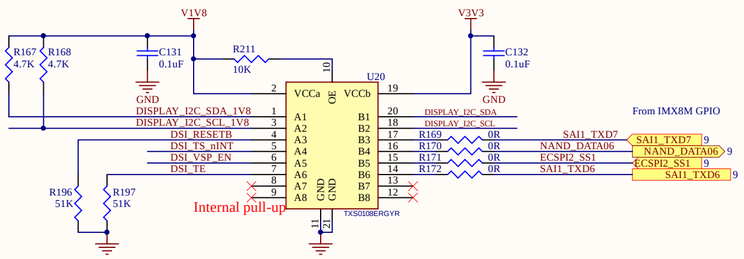




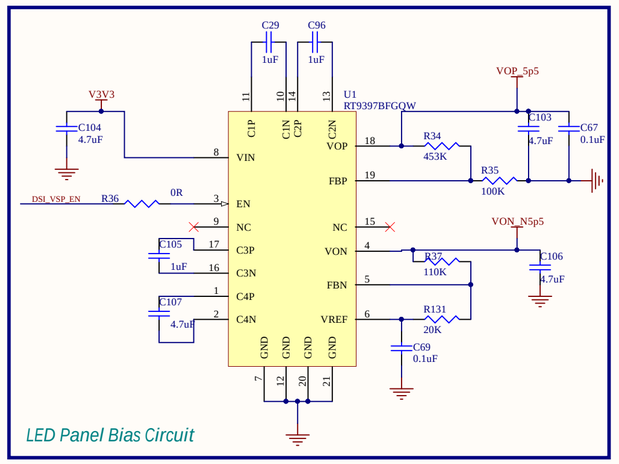
LED Panel Connector

A 39-pin external display interface FPC connector.
Base on TL060FVMS07-00 LCD Panel from Tinama.



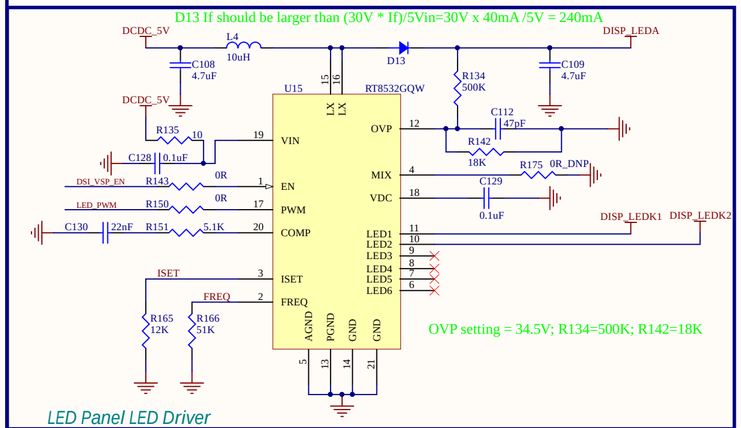


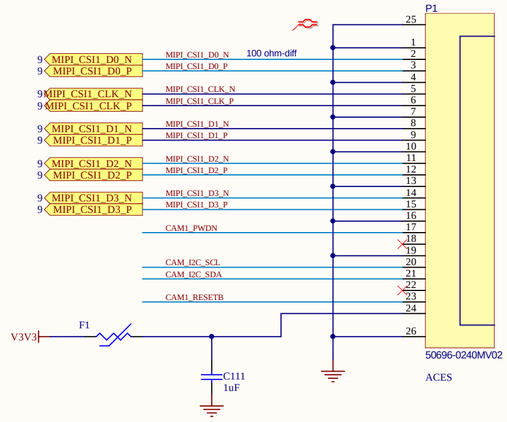
LED Panel Bias Circuit

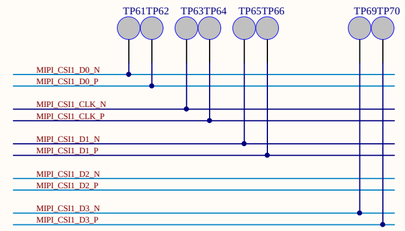


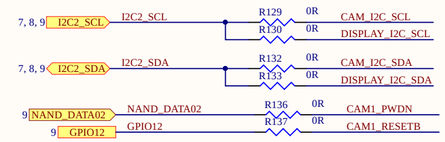
LED Panel LED Driver

D13 If should be larger than (30V * If)/5Vin=30V x 40mA /5V = 240mA









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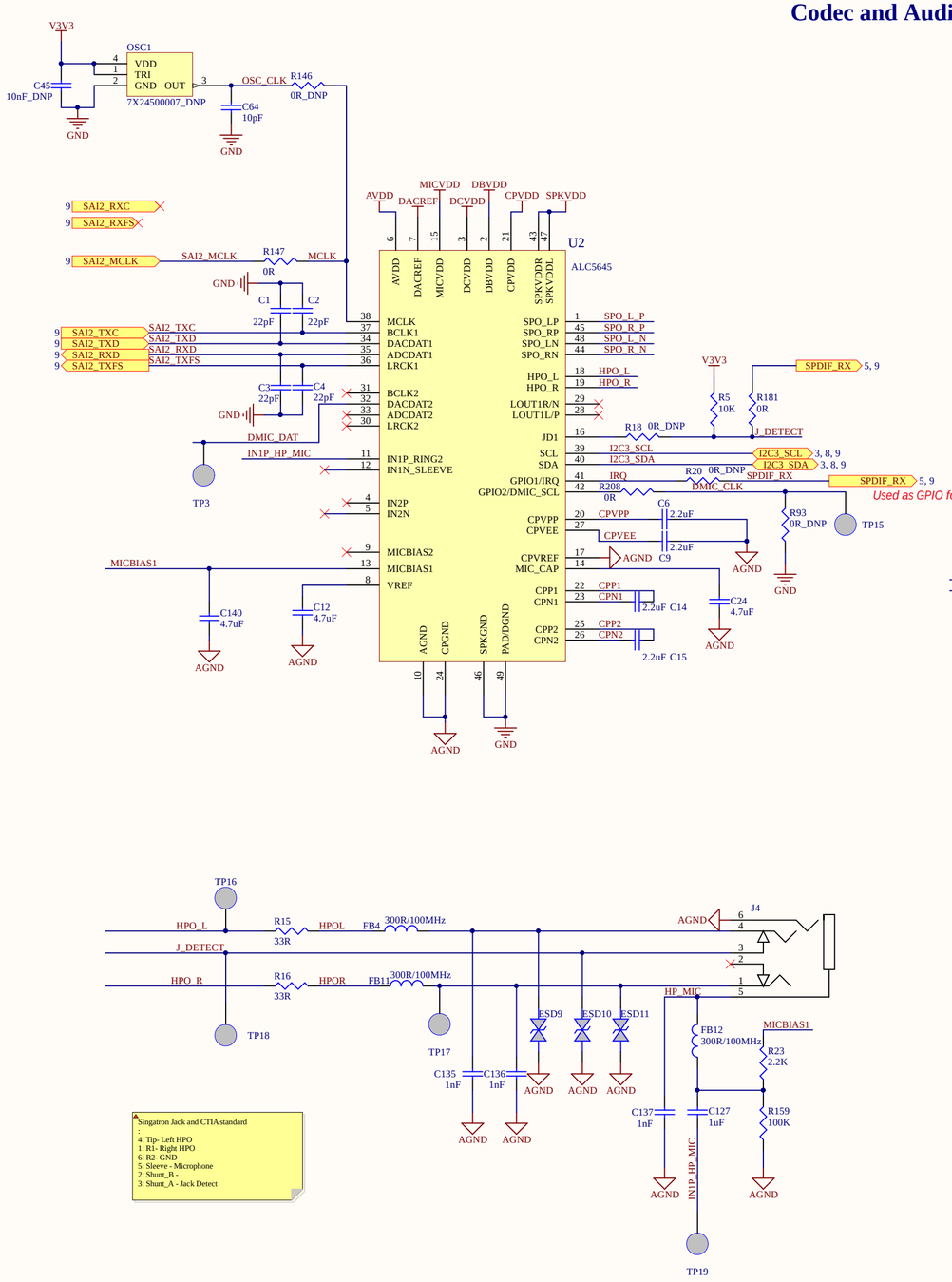
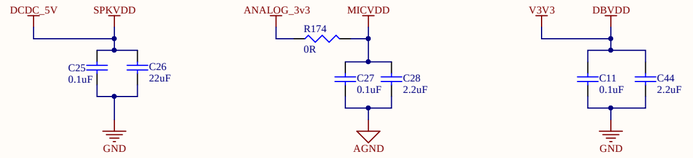
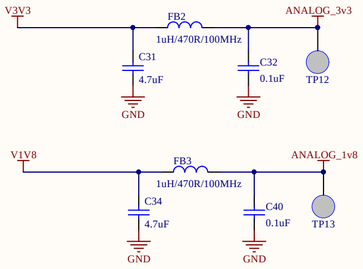
Codec and Audio

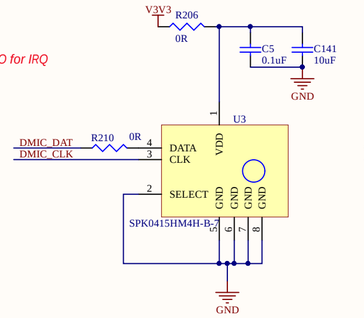


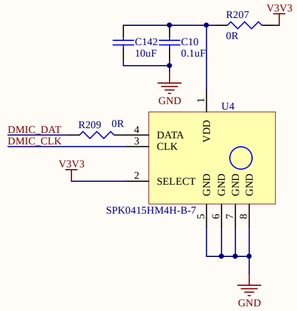
Power Bypass Caps



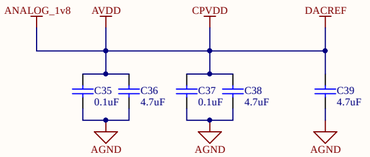
Supply Filtering

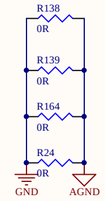




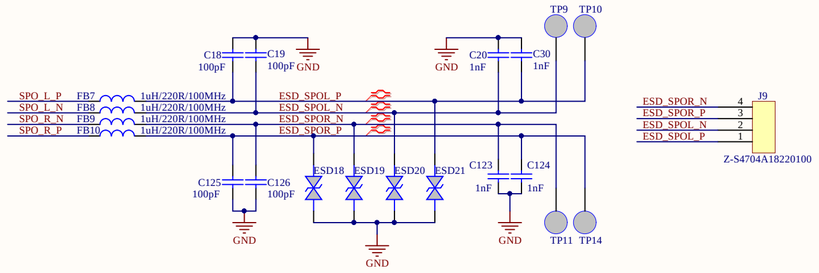


GND Tie





Speaker EMI/ESD



Project:	*Coral Dev Board: Baseboard*		
Engineer:	Bangfei/Michael/Leo	Revision:	PVT
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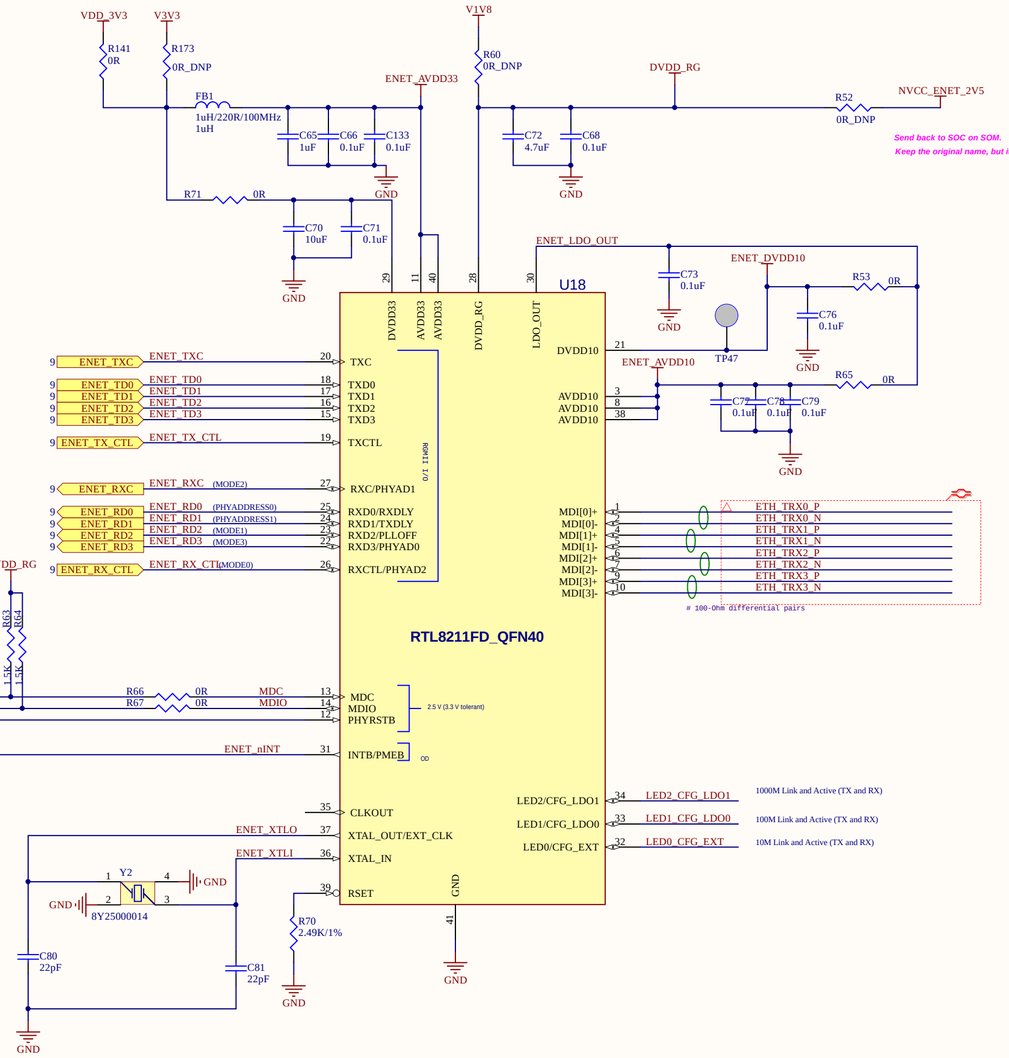
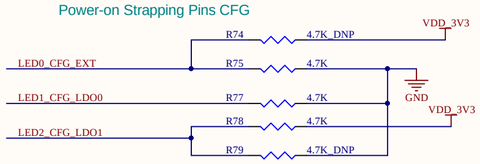
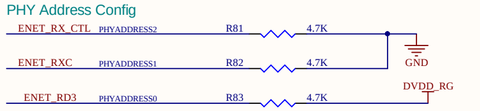


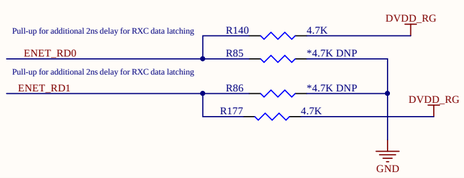
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1'B1	2'B00
External 1.8	1'B1	2'B10
Internal 1.8V(Default)	1'B0	2'B10

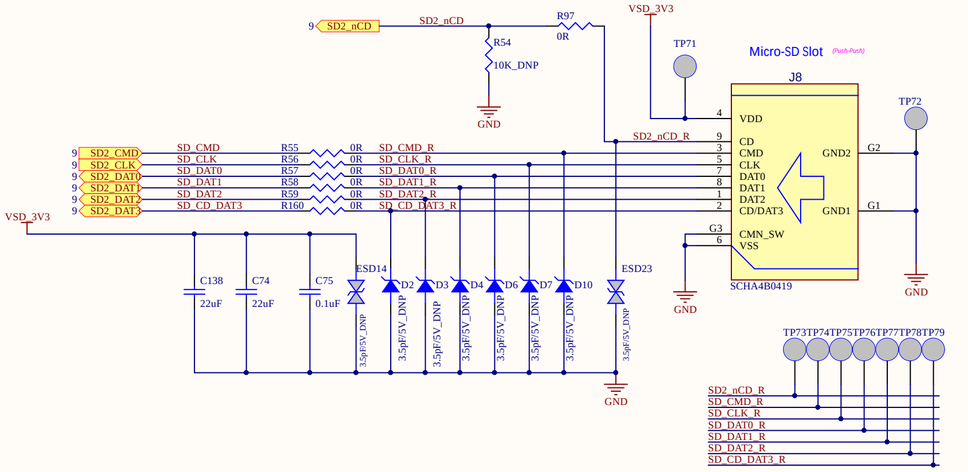
Power-on Strapping Pins CFG



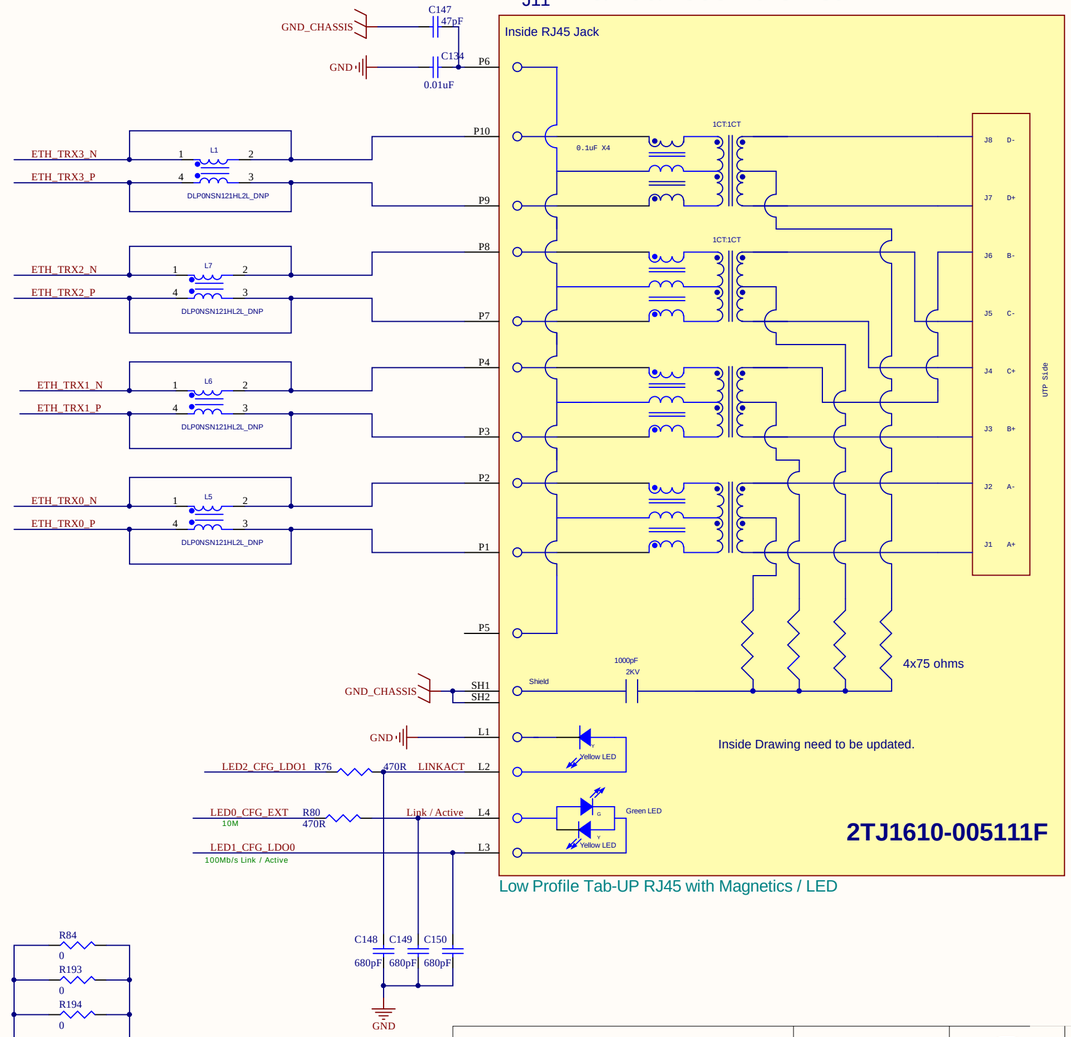
PHY Address Config







J11 10/100/1000 Ethernet



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Engineer: Bangfei/Michael/Leo		Revision: PVT
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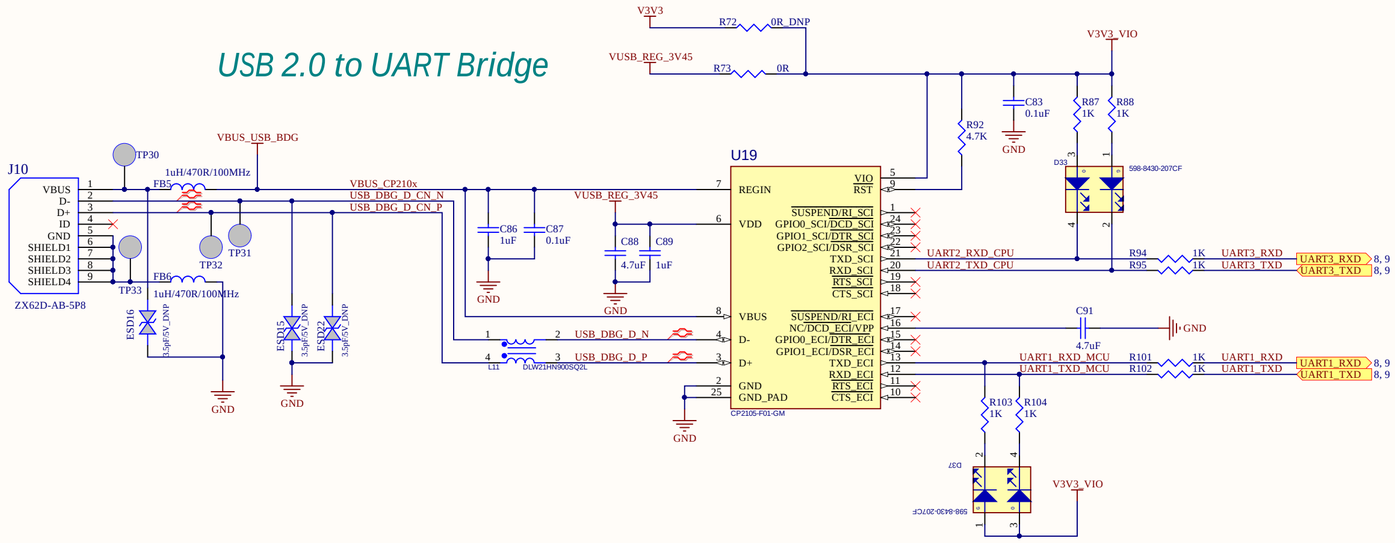
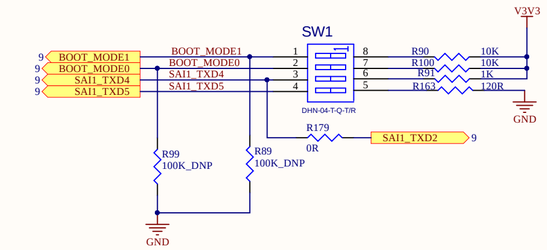
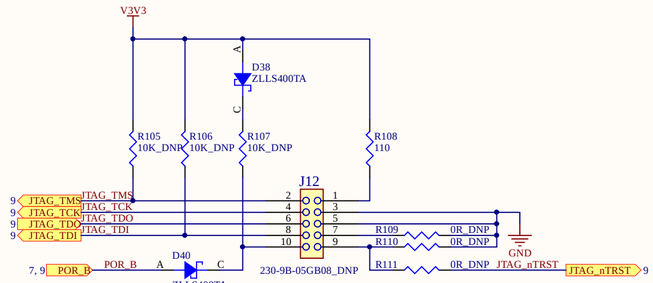
USB 2.0 to UART Bridge



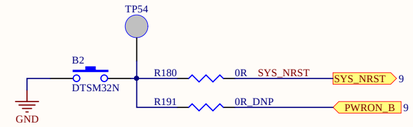


BMODE[1:0]	BOOT TYPE
00	Boot From Fuses (Production on the line).
01	Serial Downloader (from USB to flash image /MFG)
10	Internal Boot (Software Development)
11	Reserved

Boot Device: eMMC/MicroSD

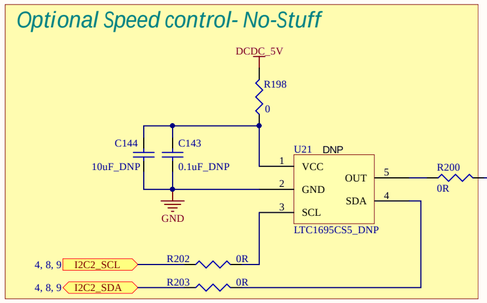


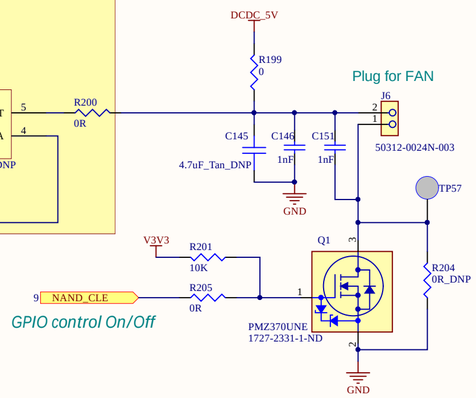
JTAG for Debug



System Reset Button

Optional Speed control- No-Stuff

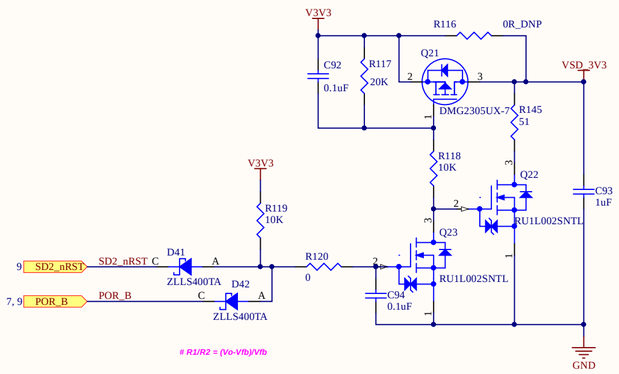




GPIO control On/Off

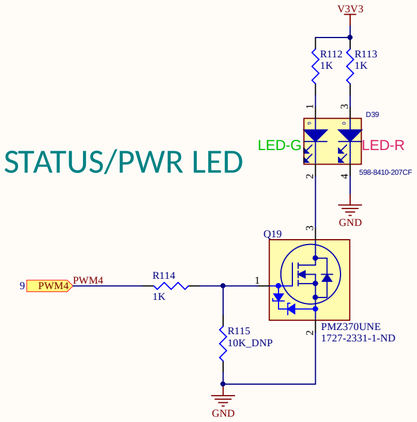
Fan Control

SD3.0 PWR



R1/R2 = (Vo-Vfb)/Vfb

STATUS/PWR LED



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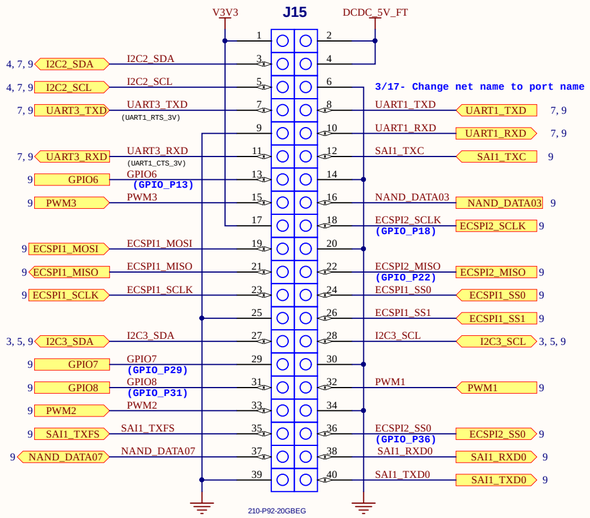
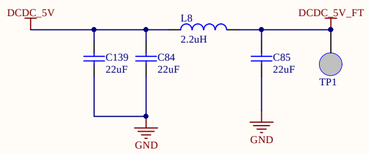
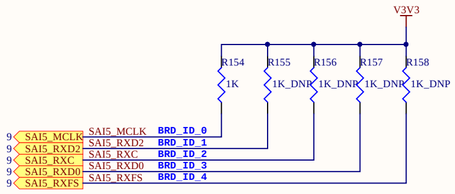
40 Pin Header



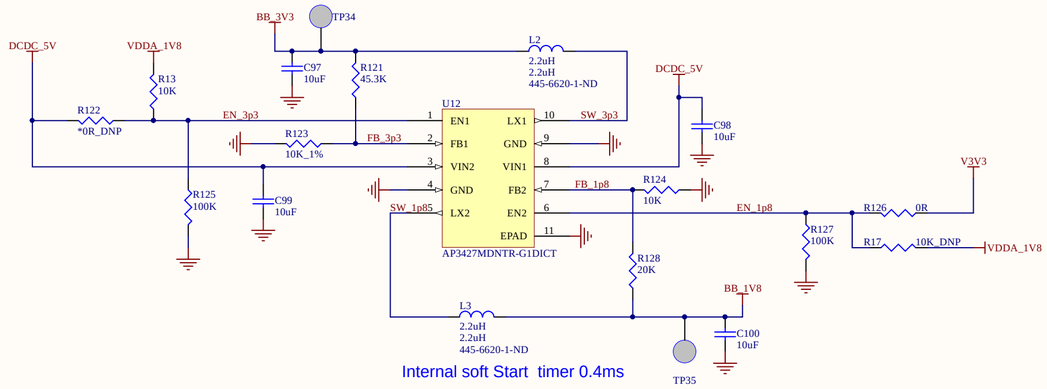
HAT 5v EMI Filtering



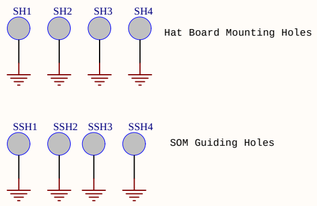


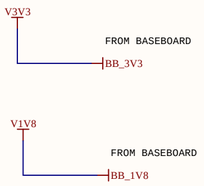
Borad_ID[4:0]:
Coral BaseBoard: 00001 (default).

These SAI5_ pins are GPIO with default 90K PD resistor inside SOC.**



Internal soft Start timer 0.4ms





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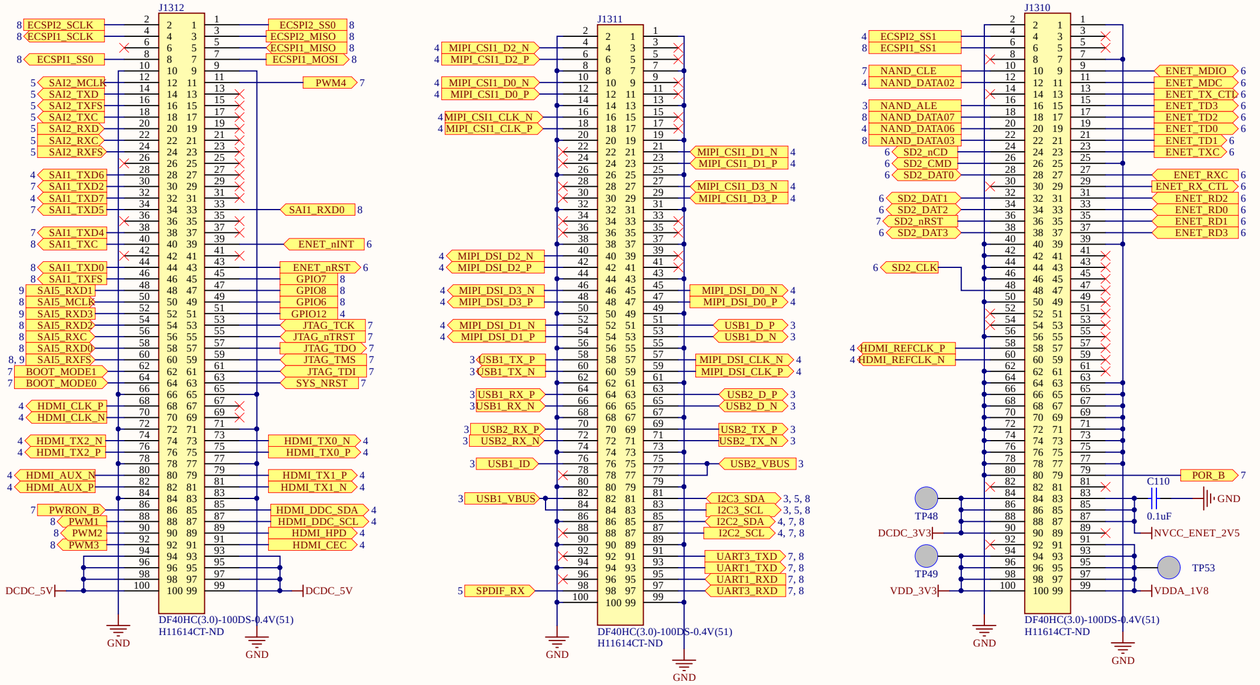
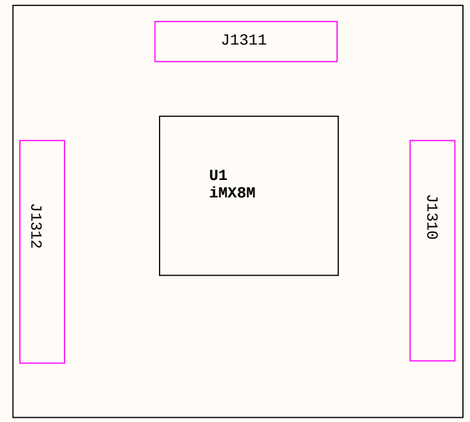
SOM Board-to-Board Connectors





B2B Conncetor Location

(TOP VIEW)

Project:	*Coral Dev Board: Baseboard*		
Engineer:	Bangfei/Michael/Leo	Revision:	PVT
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Mountain View, CA 94043

Coral

Coral Dev Board Power Diagram

Base Board

USB Type-C PWR Only J2 — USB_VIN → VSYS (5V) → OVP/Surge/ESD Protection (<5.95V, 4A) KTS1681 → DCDC_5V

USB Type-C DRP (OTG) J1 — CC1/CC2 → CC Logic PTN5150AHX — USB_ID → Pwr SW NX5P3090 — VBUS1 (5V)

HDMI J5 — Fuse — 5V

USB Type-A Pwer Src J3 — VBUS2(5V/0.9A) ← Pwr SW NX5P3090 ← BOOST_5V ← BOOST TPS61253A ← DCDC_5V

Display Connector P3 — +/-5.5V ← LCD BackLight Ctrl RT8532+RT9397 ← DCDC_5V

Camera Connector P1/P2 — CAM_3V3 ← Fuse ← V3V3

40 pin EXP_CN J15 — DCDC_5V, V3V3

Audio Codec
- SPKVDD_5V
- DBVDD_3V3
- MICVDD_3V3
- AVDD/CPVDD/DACR

V1V8 (BB_1V8) ← BB_1V8; V3V3 (BB_3V3) ← BB_3V3

Dual DC-DC AP3427M — VDDA_1V8; VDD_3V3; DCDC_3V3; VDDA_1V8

GE PHY: RTL8211FD
- VDD3V3
- AVDD3V3

V3V3

NVCC_ENET_2V5 (1.8V) RGMII Voltage

B2B Connectors

SOM

PMIC: BD71837MWV (8 Buck+ 7 LDO)

SEQ	Buck/LDO	
1	LDO1	NVCC_SNVS_3V3
2	LDO2	VDD_SNVS_0V9
RTC_RESET_B	RTC_RESET_B	
3	BL1	VDD_SOC_0V9
3	LDO4	VDDA_0V9
4	BL2	VDD_ARM_0V9
4	BL3	VDD_GPU_0V9
4	BL4	VDD_VPU_0V9
4	BL5	VDD_DRAM_0V9
5	LDO3	VDDA_1V8
5	LDO3	VDDA_DRAM_
6	BL6	NVCC_3V3/VDD_3V3
6	BL7	NVCC_1V8/NVCC_SD1_1V8/VDD_1V8
6	BL8	NVCC_DRAM_1V2
6	MUXSW	NVCC_SD2
POR_B	POR_B	
7	LDO5	VDD_PHY_1V8
7	LDO6	VDD_PHY_0V9
7	LDO7	VDD_PHY_3V3

CPU: i.MX8M (mScale850)

SEQ	PWR	TYP	Curr(mA)
1	NVCC_SNVS	3.3	2
2	VDD_SNVS	0.9	2
RTC_RESET_B			
3	VDD_SOC	0.9	3600
3	VDDA_0P9	0.9	4000
4	VDD_ARM	0.9/1.0	2000
4	VDD_GPU	0.9/1.0	1000
4	VDD_VPU	0.9/1.0	2500
4	VDD_DRAM	0.9	250
5	VDDA_1P8_xxx	1.8	50
5	VDDA_DRAM	1.8	150
6	NVCC_3V3	3.3	100
6	NVCC_1V8	1.8	700
6	NVCC_DRAM	1.1/1.2/1.35	
6	NVCC_SD2	1.8/3.3	
POR_B			50
7	1.8V PHY	1.8	250
7	0.9V PHY	0.9	100
7	3.3V PHY	3.3	

LPDDR4
- VDD1
- VDD2/VDDQ

eMMC
- VCCQ
- VCC

WiFi/BT
- VDD
- VDDIO

PMIC → **Edge TPU**

Project:	*Coral Dev Board: Baseboard*		Google LLC 1600 Amphitheatre Parkway Mountain View, CA 94043
Engineer:	Bangfei/Michael/Leo	Revision: PVT	
Date:	8/12/2019	Sheet 10 of 11	
File:	10_MISC.SchDoc		

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Version	Date	Author	Change Note	Approved
PVT	08/12/2019	Bangfei Pan	Cleanup the schematic	

Project:	*Coral Dev Board: Baseboard*
Engineer: Bangfei/Michael/Leo	Revision: PVT
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File: 11_CHANGE_LOG.SchDoc	

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